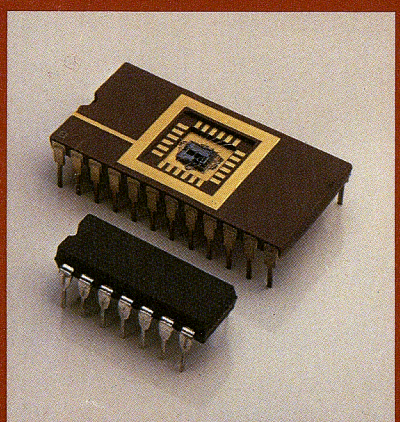


Integrated Circuits

ANALOG DEVICES

How to Find Product Data in This Databook

The Databook contains Data Sheets for all products recommended for new designs, lists of Available Products not databooked here (data sheets upon request), and a Substitution Guide for products no longer available, plus Selection Guides and a wealth of background information.

THERE ARE TWO VOLUMES

VOLUME I contains technical data on our *integrated circuits and hybrids* for data acquisition.
VOLUME II has all data-acquisition products manufactured in the form of *modules, cards, instruments, discrete-assembly subsystems and systems.*

DO YOU KNOW THE MODEL NUMBER?

If you know the model number, turn to the product index on page 1-14 (back of book) and look up the model number. You will find the Volume, Section, and Page location of data sheets bound into Volume I and Volume II.

If you're looking for a form-and-function-compatible version of an integrated circuit or hybrid product originally brought to market by some other manufacturer (second source), add our "AD" prefix (or "ADSP", for digital signal processing ICs) and look it up in the index.

IF YOU DON'T KNOW THE MODEL NUMBER

There are two ways to find a device to perform your function:

1. **FIND YOUR FUNCTION IN THE LIST ON THE OPPOSITE PAGE OR ON PAGE 2–1**
   Turn directly to the appropriate Section (or Volume). You will find one or more functional Selection Guides at the beginning of the Section. The Selection Guides will help you find the products that are closest to satisfying your need, and their Volume-Section-Page locations. Use them to compare all products in the category by salient criteria, no matter which Volume their technical data resides in.

2. **IF THE FUNCTION IS NOT LISTED BY A NAME THAT YOU RECOGNIZE**
   Find it in the diagram (opposite page). It will help you find the Selection Guides for products in that functional category. Then use the Selection Guide(s) to find the Volume-Section-Page locations of products that will come closest to satisfying your need.

A RELATED PRODUCT MAY BE WHAT YOU REALLY WANT

Text in each section often mentions related or complementary product categories having a greater or lesser degree of functional integration.

IF YOU CAN'T FIND IT HERE . . . ASK!

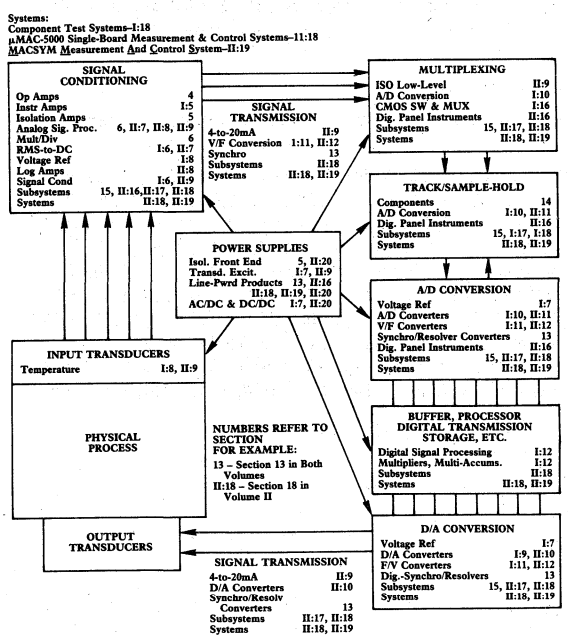
See Worldwide Service Directory, 1–12 and 1–13, at the back of this volume.

ANALOG DEVICES

DATA-ACQUISITION DATABOOK 1984

VOLUME I
INTEGRATED CIRCUITS

PICTORIAL GUIDE TO PRODUCT CATEGORIES



ANALOG DEVICES

DATA-ACQUISITION DATABOOK 1984

VOLUME I
INTEGRATED CIRCUITS

Products in this book may be covered by one or more of the following patents. Additional patents are pending. See individual data sheets for further information:

U.S.: 3,007,114, 3,278,736, 3,355,670, 3,441,913, 3,467,908, 3,500,218, 3,530,390, 3,533,002, 3,685,045, 3,729,660, 3,747,088, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,872,466, 3,887,863, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,092,698, 4,123,698, 4,136,349, 4,141,004, 4,213,806, 4,250,445, 4,270,118, 4,268,759, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,338,591, 4,349,811, 4,363,024, 4,374,314, 4,383,222, 4,395,647, 4,399, 345, 4,400,689, 4,400,690, DES 233,909. U.K.: 964,513, 1,310,591, 1,310,592, 1,364,233, 1,470,673, 1,470,674, 1,537,542, 1,531,931, 1,571,869, 1,590,136, 1,590,137, 1,599,538, 2,008,876, 2,012,135, 2,032,659, 2,040,087, 2,050,740, 2,081,040. France: 70.10561, 71.28952, 74.25263, 75-27557, 76 01788, 76 08238, 77 20799, 79 24021, 80 00960, 111 833. West Germany: 20 14 034, 21 39 560, MR 9379. Italy: 933,798. Japan: 452,263, 1,092,928, 1,101,824, 1,180,463. Canada: 984,015, 1,006,236, 1,025,558, 1,035,464, 1,054,248, 1,141,034, 1,141,820, 1,143,306, 1,150,414, 1,153,607, 1,157,571. Sweden: 7603320-8.

Contents

General Introduction

Analog Devices designs, manufactures, and sells worldwide sophisticated electronic components and subsystems for use in precision measurement and control. More than six hundred standard products are produced in manufacturing facilities located throughout the world. These facilities encompass all relevant technologies, including bipolar, I^2L, CMOS, and hybrid integrated circuits–and assembled products in the form of potted modules, printed-circuit boards, and instrument packages.

State-of-the-art technologies have been utilized (and, in many cases, invented) to provide timely, reliable, easy-to-use advanced designs at realistic prices. Nearly twenty years of successful applications experience and continuing vertical integration insure that these products are oriented to user needs. The continuing application of present state-of-the-art and the invention of future state-of-the-art processes strengthens the leadership position of Analog Devices in data-acquisition products.

MAJOR PROGRESS

Since the publication of our two-volume *1982 Databook* and its 1983 companion update volume, nearly 50 significant new products have been introduced. They are identified by bullets (•) in the index and in the table of contents for each section of this Databook. Examples of these new products include: The AD7226 Quad DAC – 4 bus-interfaced voltage-output 8-bit DACs on a single monolithic CMOS chip; the AD670 8-bit "ADCPORT," a complete ready-to-go monolithic µP-compatible 8-bit a/d converter with on-chip instrumentation amplifier; the AD667 complete 12-bit voltage-output D/A converter with 2µs voltage-settling time; the AD9700 monolithic DAC for raster displays; the ADSP-1110 single-port 16-bit multiplier/accumulator for digital signal-processing; and the complete, expandable, stand-alone µMAC-5000 single-board measurement-and-control system, programmable in powerful µMACBASIC.

INTEGRATED CIRCUITS

The list of product-category "bleed tabs" opposite the "How to Find It" Guides on the inside front cover of this Volume is a functional summary of our integrated-circuit and hybrid component and subsystem product classes. The complete table of contents, starting on page 2-1, provides a detailed panorama of products and functions, irrespective of technology, appearing in both Volumes of this Databook.

TECHNICAL SUPPORT

Analog Devices offers extensive technical literature, which discusses the technology and applications of products for precision measurement and control. Besides comprehensive data sheets, of which there are many outstanding examples in this book, we offer Application Notes, Application Guides, Technical Handbooks (at reasonable prices), and several serial publications; for example, *Analog Productlog*, which provides brief information on new component products being introduced and *Analog Dialogue*, our technical magazine, which provides-in-depth discussions of new developments in analog and digital circuit technology as applied to data-acquisition and control. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to data-book catalogs–such as this one–we also publish several short-form catalogs, on specific product families. You will find typical publications described on page 1-11 at the back of the book.

SALES OFFICES

Backing up our design and manufacturing capabilities and our extensive array of publications is a network of sales offices and representatives throughout the United States and most of the world. They are staffed by experienced sales and applications engineers, and many of them maintain a local stock of Analog Devices products. Our Worldwide Service Directory appears on pages 1-12 and 1-13 at the back of the book.

PRODUCTS NOT CATALOGUED HERE

For maximum usefulness to designers of new equipment, without unwieldy size, we have limited the contents of the Databook to products most likely to be used for the design of new circuits and systems. If the data sheet for a product you are interested in is not in either Volume turn to page 1-9, at the back of this book, where you will find a list of older products for which data sheets are available upon request. On page 1-10 you will find a guide to substitutions for products no longer available.

PRICES

At Analog Devices, we recognize that accurate, up-to-date prices of our products are an important consideration in making a choice among the many available product families. However, since prices are subject to change, current price lists and/or quotations are available upon request from our sales offices.

(this section continues at the back of the book)

Table of Contents

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Operational Amplifiers – Section 4

•New product since publication of *1982 – 1983 Databook Update.*

Instrumentation & Isolation Amplifiers – Section 5

Analog Signal Processing Components – Section 6

•New product since publication of *1982–1983 Databook Update*.

Voltage References – Section 7

Temperature Measurement Components – Section 8

•New product since publication of *1982–1983 Databook Update*.

Digital-to-Analog Converters – Section 9

LOGDAC is a registered trademark of Analog Devices, Inc.
•New product since publication of *1982–1983 Databook Update*.

Digital-to-Analog Converters – Section 9 (continued)

Analog-to-Digital Converters – Section 10

•New product since publication of *1982–1983 Databook Update.*

Analog-to-Digital Converters – Section 10 (continued)

Voltage-to-Frequency & Frequency-to-Voltage Converters – Section 11

Digital Signal Processing Components – Section 12

•New product since publication of *1982–1983 Databook Update.*

Synchro & Resolver Converters – Section 13

Sample/Track-Hold Amplifiers – Section 14

Data Acquisition Subsystems – Section 15

•New product since publication of *1982–1983 Databook Update.*
Inductosyn is a registered trademark of Farrand Industries, Inc.

CMOS Switches & Multiplexers – Section 16

Monolithic Chips – Section 17

BIPOLAR INTEGRATED CIRCUIT CHIPS

•New product since publication of *1982–1983 Databook Update*.
DACPORT is a registered trademark of Analog Devices, Inc.

Monolithic Chips – Section 17 (continued)

Component Test Systems – Section 18

Package Information – Section 19

Application Notes – Section 20

•New product since publication of *1982–1983 Databook Update.*

Ordering Guide

Contents

3

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products, whether you're buying one IC op amp, a multi-option subsystem, or 1000 each of 15 different items. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us.
3. Know our warranty for components and subsystems.

For answers to further questions, call the nearest sales office (listed at the back of the book) or our main office in Norwood, Mass. U.S.A. (617-329-4700).

MODEL NUMBERING

Many of the data sheets in the Databook have an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. I.C. and hybrid part numbers are created using one of these two systems:

Figure 1 shows the form of model number used for our proprietary standard monolithic ICs and many of our hybrids. It consists of an "AD" (Analog Devices) prefix, a 3- or 4-digit model number, an alphabetic performance/temperature-range designator and a package designator. One or two additional letters may immediately follow the digits ("A" for second-generation redesigned ICs, "DI" for dielectrically isolated CMOS switches, e.g., AD536AJH, AD7512DIKD).

Figure 2 shows the somewhat different numbering scheme used by our Computer Labs Division for hybrid circuits. The number starts with a three-character alphabetic prefix, followed by a hyphen, a three- or four-digit number, and alphabetic designators (as applicable) to indicate additional functional designations or options and packaging options.

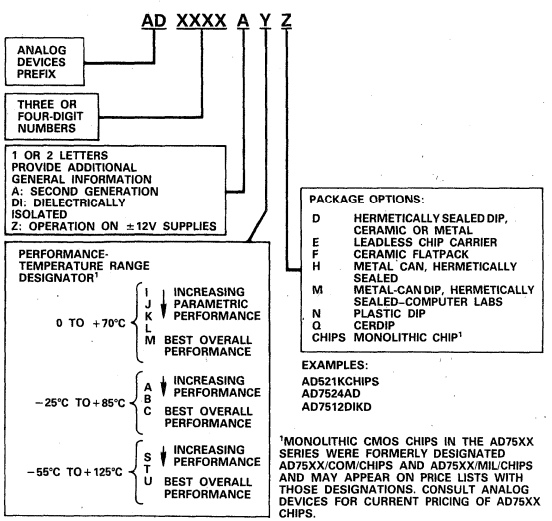

Figure 1. Model-Number Designations for Standard Analog Devices Monolithic and Hybrid IC Products

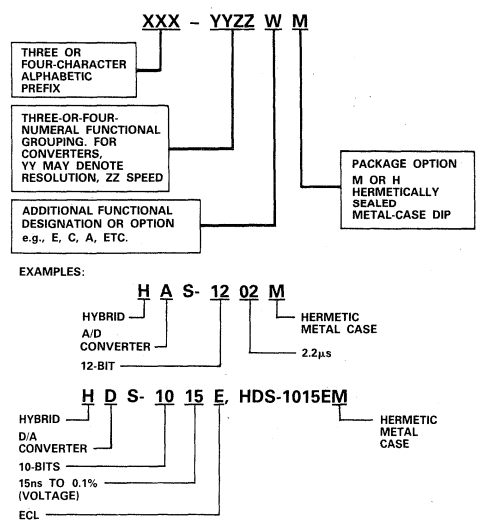

Figure 2. Computer Labs Video Hybrid Product Designations

SECOND SOURCE

In addition to our many proprietary products, we also manufacture devices that are fit-, form-, and function-compatible (and often superior in performance and reliability) to popular products that originated elsewhere. For such products, we add the prefix "AD" to the familiar model number (example: ADDAC85C-CBI-V).

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory. Please specify if air shipment is required.

Place your orders with our local sales office or representative, or directly with our customer service group located in the Norwood facility. Orders and requests for quotations may be telephoned, sent via TWX or TELEX, or mailed. Orders will be acknowledged when received; billing and delivery information is included.

Payments for new accounts, where open-account credit has not yet been established, will be C.O.D. or prepaid. On all orders under fifty dollars ($50.00), a five-dollar ($5.00) processing charge is required.

When prepaid, orders should include $2.50 additional for packaging and postage (and a 5% sales tax on the price of the goods if you are ordering for delivery to a destination in Massachusetts).

WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty, and μMAC and MACSYM systems, which have a 90-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Operational Amplifiers

Contents

•New product since publication of *1982–1983 Databook Update.*

Selection Guide
Operational Amplifiers

General Purpose

		FET INPUT							WIDEBAND		
		171	AD503	AD506	AD542	AD642	AD644	AD544	AD611	AD101 Series	AD741
Monolithic Technology	Bipolar Input										
	J-FET				•			•	•	•	•
	Dual J-FET					•	•				
Multi-Device Technology	Hybrid										
	Module	•	•	•							
High Open Loop Gain	≥100dB	•			•	•					
	≥140dB										
High CMR	>100dB	•									
Low Offset Voltage	≤5mV			•	•	•	•	•	•	•	•
	≤1mV	•			•	•	•	•	•		
	≤50μV										
Low Offset V, vs. Temp	≤5μV/°C				•	•	•	•			
	≤1μV/°C										
	≤0.6μV/°C										
Low Bias Current	≤50pA	•	•	•	•	•	•	•	•		
	≤5pA										
	≤0.5pA										
Fast Settling	≤1μs to 0.1%						•	•	•		
	≤5μs to 0.01%						•	•	•		
Wideband (Unity Gain)	≥2MHz	•					•	•	•	•	
	≥10MHz										
High Slew Rate	≥10V/μs	•					•	•	•	•	
	≥30V/μs										
	≥100V/μs										
	≥1000V/μs										
Low Noise (0.1 to 10Hz) 2μV p-p					•	•	•	•	•	•	
High Voltage Out	≥100V	•									
High Current Out	≥20mA										
Low Power	≤75mW				•	•	•	•	•	•	•
Second Source										•	•
Temperature Range 0 to +70°C		•	•	•	•	•	•	•	•	•	•
-25°C to +85°C										•	
-55°C to +125°C			•	•	•	•	•	•	•	•	•
Dice Availability					•	•	•	•			
Volume		II	I	I	I	I	I	I	I	I	I
Page		4-21	4-35	4-35	4-75	4-95	4-99	4-79	4-91	4-17	4-107

Shading indicates new product since publication of *1982–1983 Databook Update*.

High Accuracy

		LOW V_{OS} DRIFT						LOW BIAS CURRENT		FET INPUT				
		AD504	AD510	AD OP-07	AD OP-27	AD OP-37	AD517	234[1]	235[1]	AD545	AD547	AD647	AD515	52
Monolithic Technology	Bipolar Input	•	•	•	•	•	•				•			
	J-FET											•		
	Dual J-FET													
Multi-Device Technology	Hybrid									•			•	
	Module							•	•					•
High Open Loop Gain	≥100dB	•	•	•	•	•	•	•	•		•	•		•
	≥140dB							•	•					
High CMR	>100dB	•	•	•	•	•	•							•
Low Offset Voltage	≤5mV	•	•	•	•	•	•			•			•	•
	≤1mV										•	•		•
	≤50μV			•	•	•	•	•	•					
Low Offset V, vs. Temp	≤5μV/°C	•	•	•	•	•	•			•	•	•		•
	≤1μV/°C							•	•		•	•		•
	≤0.6μV/°C	•	•	•	•	•		•	•					
Low Bias Current	≤50pA								•	•	•	•	•	
	≤5pA									•			•	•
	≤0.5pA												•	
Wideband (Unity Gain)	>500kHz								•					
	>2MHz				•	•		•						
High Slew Rate	≥10V/μs					•								
	≥30V/μs							•						
	≥100V/μs													
	≥1000V/μs													
Low Noise (0.1 to 10Hz)														
≤4μV p-p											•	•		
≤2μV p-p			•	•			•		•					•
≤1μV p-p		•			•	•		•	•					
High Voltage Out	≥100V													
High Current Out	≥20mA													
Low Power	≤75mW									•	•	•	•	
Second Source				•	•	•								
Temperature Range														
0 to +70°C		•	•	•	•	•	•		•	•	•	•	•	•
-25°C to +85°C														
-55°C to +125°C		•	•	•	•	•	•				•	•		
Dice Availability				•			•				•			
Volume		I	I	I	I	I	I	II	II	I	I	I	I	II
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NOTE

[1] Chopper Stabilized

Shading indicates new product since publication of *1982–1983 Databook Update*.

Selection Guide
Operational Amplifiers

Fast/Wideband

		FET INPUT												UNITY GAIN BUFFER
		AD507	AD509	AD518	AD380	AD381	AD382	AD3554	50, 51	HOS-050	HOS-060	ADLH0032	ADLH0033	HOS-100
Monolithic Technology	Bipolar Input	•	•	•					•					
	J-FET													
	Dual J-FET													
Multi-Device Technology	Hybrid				•	•	•	•		•	•	•	•	•
	Module								•					
High Open Loop Gain	≥100dB	•				•	•	•		•	•			
	≥140dB													
High CMR	>100dB													
Low Offset Voltage	≤5mV	•	•		•		•	•	•			•	•	
	≤1mV					•					•			
	≤50μV													
Low Offset V, vs. Temp	≤5μV/°C					•	•							
	≤1μV/°C													
	≤0.6μV/°C													
Low Bias Current	≤50pA					•	•	•				•	•	
	≤5pA													
	≤0.5pA													
Fast Settling	≤1μs to 0.1%	•	•	•		•	•		•	•	•	•	•	•
	≤5μs to 0.01%				•			•	•	•	•	•		
Wideband (Unity Gain)	≥2MHz					•	•							
	≥10MHz	•	•	•	•			•		•	•	•	•	•
	≥50MHz								•					
High Slew Rate	≥10V/μs	•		•										
	≥30V/μs					•	•							
	≥100V/μs		•		•				•	•	•	•	•	•
	≥1000V/μs							•						
Low Noise (0.1 to 10Hz) ≥2μV p-p						•	•							
High Voltage Out	≥100V													
High Current Out	≥20mA	•			•		•	•	•	•	•		•	•
Low Power	≤75mW													
Second Source		•	•					•				•	•	
Temperature Range														
0 to +70°C		•	•	•	•	•	•		•					
-25°C to +85°C								•				•	•	
-55°C to +125°C		•	•	•	•	•	•	•		•	•	•	•	•
Dice Availability				•										
Volume		I	I	I	I	I	I	I	II	I	I	I	I	I
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Orientation
Operational Amplifiers

The amplifiers listed in this catalog are intended to provide cost-effective solutions to the bulk of op-amp requirements in precision measurement and control, as well as to more-general requirements in electronic circuits. The technical data included here* cover the properties of some 36 op-amp families, comprising about 100 distinct types. Some are general purpose, others provide near-optimum performance for specific classes of applications.

They differ in a variety of ways, for example, circuit technology, circuit architecture, input properties, output properties, operating temperature range and in terms of the many performance specifications.

BACKGROUND

The operational amplifier is today the most-widely used analog subassembly. It is safe to say that its *basic* properties and applications are sufficiently understood by most circuit designers and builders. However, the basis for choice, the subtleties of using op amps in circuits for best results (especially in precision measurement and control), and the varieties of possible applications are less clearly understood by op amp users, in varying degrees.

In these few pages, we shall address the question of making a proper choice of op amp type for an application, in relation to the extensive array of device properties presented in the data sheets that follow.

For those users requiring basic tutorial material, and detailed information on getting the most out of op amps, we have provided on page 4-16 a bibliography that should make available up to 99% of information needed now and then, with "fanout" to the vast body of literature that – with some redundancy – will provide the remainder. It should come as no surprise to successful users of Analog Devices op amps that a number of the references are to the applications sections of data sheets included in this catalog.

SELECTION PRINCIPLES

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured and then must be able to translate these published specifications in terms meaningful to the design requirements.

There are three fundamental aspects to the rational selection of an operational amplifier for a given application: (1) establishing the circuit architecture, (2) defining the performance levels, and (3) choosing the amplifier(s).

1. To obtain a circuit building block to implement a defined functional job, the principal choices are either to purchase a committed functional device or to design a circuit employing op amps to perform the function. For example, to obtain a difference between two voltages, one may either purchase an instrumentation or isolation amplifier, or design a suitable subtraction circuit using op amps. If a committed functional building block, with appropriate specs and price, is not available, the circuit designer must start by developing schematic diagrams of circuits that will perform the function simply using "ideal" operational amplifiers. Many commonly used circuits can be found in textbooks, "cookbooks", and linear circuit books, as well as in application notes and data sheets.

2. Recognizing that the choice of an op amp depends on both the overall circuit requirements and the characteristics of available op amps, the designer should interpret the desired overall performance in terms of the parameters of op amps, and establish acceptable ranges of parameters, and their variation with time, temperature, supply voltage, etc. Examples of the key parameters are the input offset voltage, input bias and offset currents, and the high-frequency performance and transient behavior of the op-amp block (and its effect on the closed-loop circuit) for large and small signals. It will be helpful to develop an application checklist, which includes such considerations as the character of the input signals and their impedance, the output load, the desired accuracy – static and dynamic – and the environmental conditions.

3. The designer must then relate acceptable performance of the op-amp building block to the specifications and prices of available devices from preferred suppliers, bearing in mind a firm understanding of the way in which manufacturers define their specifications, and how definitions can differ in a way that may be misleading. A set of definitions used by Analog Devices follows the next section.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier.

*In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, DC offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the DC discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If DC information is not of interest, a suitable blocking capacitor can be connected at the amplifier input and all of the "drift" specifications may usually be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where DC information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. For example, if the closed-loop gain is 1000, the open-loop gain must be at least 100,000 to yield an error of no more than 1%, and 1,000,000 to yield an error no greater than 0.1%. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the DC offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements and temperature range have been established at this point.)

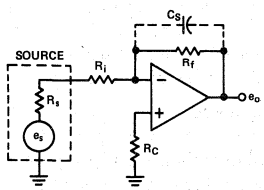
1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_s, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{cm}.

2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a DC input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.



$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i\right]$$

Signal Input Drift Error = V_d

For $R_C = 0$ and $R_s \ll R_i$

$$e_o = -\frac{R_f}{R_i}\left[e_s + e_{os}\frac{R_f + R_i}{R_f} + i_d R_i\right]$$

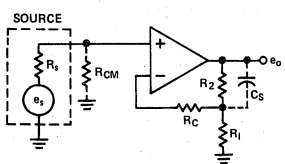
Signal Input Drift Error = V_d

For $R_C = R_i R_f/(R_i + R_f)$ and $R_s \ll R_i$

Input Impedance $R_{IN} \approx R_i$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_b R_s\right] \text{ for } R_C = 0$$

Signal Drift Error = V_d

$$e_o = \frac{R_2 + R_i}{R_i}\left[e_s + e_{os} + i_d R_s\right] \text{ for } R_C = R_s - \frac{R_i R_2}{R_i + R_2}$$

Signal Drift Error = V_d

Input Impedance $R_{IN} \approx R_{CM}$

$$\% \text{ Drift Error} = \frac{100V_d}{e_s}$$

Figure 1B. Noninverting Configuration

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_S for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input impedance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

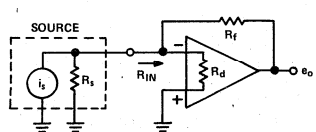
Unfortunately, however, the noninverting configuration cannot always be used since it is not convenient to use for many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of -25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{cm},

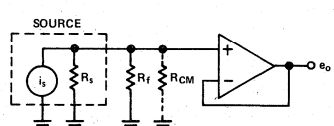


$$e_o = -R_f\left[\underbrace{i_s}_{\text{Signal}} + \underbrace{e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b}_{\text{Drift error} = I\epsilon}\right]$$

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$$

where $1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d}$ $\% \text{ Drift Error} = \frac{100\, I\epsilon}{i_s}$

Figure 2A. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

Input Impedance $R_{IN} \approx R_f$

$$\% \text{ Drift Error} = \frac{100V_d}{R_f i_s}$$

Figure 2B. Voltage Amplifier with Sampling Resistor

for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the DC and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μsec, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm, and stray capacitance, C_S, were one picofarad then the closed loop bandwidth would be limited to 160kHz $(1/(2\pi R_F C_S))$ regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in turn is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_iC_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_s will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

For greater emphasis wideband applications can be separated into two categories — steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is DC coupling required?* If DC information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output DC offset. Your only concern here is that DC offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for AC signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at DC as shown in Figure 3. The gain of these circuits can be small at DC but large at high frequencies.

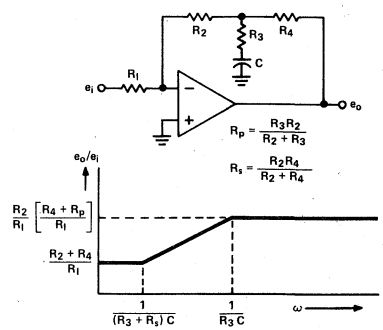


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, $f_{c1}(-3dB)$. For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta$ = A/G). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

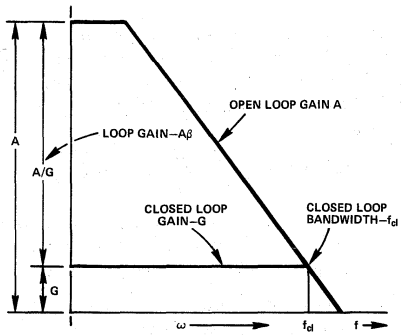


Figure 4. Closed Loop Bandwidth and Loop Gain

a. Closed loop gain stability = $\triangle G/G$
$\triangle G/G = (\triangle A/A)\ [1/(1 + A\beta)]$ where $\triangle A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at DC and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected DC offsets at the output of the amplifier.

For some monolithic amplifier designs available today their frequency response is not a simple 6dB roll-off; the response may be shaped with external RC components for improved performance. Using feedforward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most internally compensated op amps offer a stable 6dB per octave roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 5). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

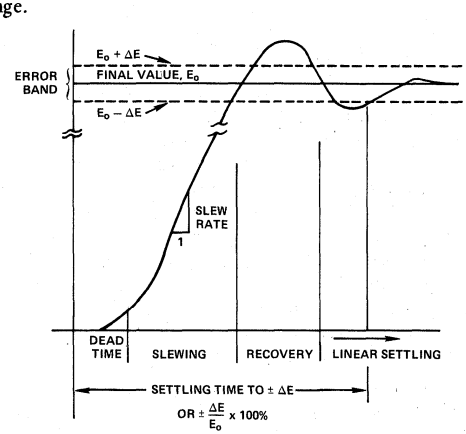


Figure 5. Typical Settling Time Characteristics

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, ideally linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 6.

However, since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

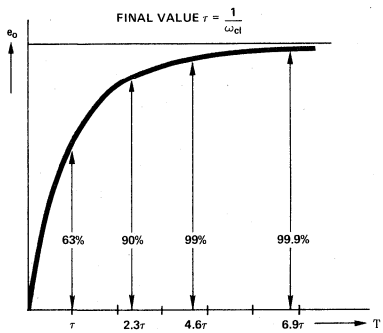


Figure 6. Step Response for Linear 6dB/Octave Amplifier

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier.

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage

K = Boltzman's Constant (1.38×10^{-23} joules/°K)

T = absolute temperature of the resistance, °K

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldy for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100k\Omega}\ (BW)}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

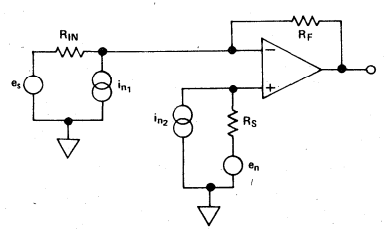
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 7A illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a RMS fashion.

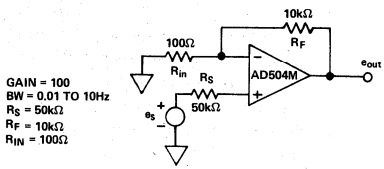


COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}}\ G)^2 + [e_{R_S}\ (G+1)]^2 + e^2 R_F + (i_{n_1} R_F)^2 + [(i_{n_2} R_S)\ (G+1)]^2 + [e_n\ (G+1)]^2}$$

Figure 7A. Noise Components

Figure 7B illustrates how the Rules of Thumb may be applied in a practical case to approximate the total output noise. In this example, AD504, or a low noise type amplifier is being used with a 50kΩ source impedance. The two major noise sources, in addition to the AD504M input voltage noise of 0.6μV p-p, are the Johnson noise (58μV p-p) and current noise (2.5μV p-p).



1) RESISTOR NOISE: R_F → 13nV/√Hz
R_{IN} → (1.3nV/√Hz) 100
R_S → (28nV/√Hz) 101 = 2.8μV/√Hz
TOTAL RESISTOR NOISE IN 10Hz BW =
(2.8μV/√Hz) (√10Hz) 6.6μV p-p/μV rms = 58μV p-p

2) AMPLIFIER CURRENT NOISE: (50pA p-p) (50k) (101) = 252μV
(50pA p-p) (10k) = 0.5μV

3) AMPLIFIER VOLTAGE NOISE: (0.6μV p-p) (101) = 60.6μV p-p

TOTAL OUTPUT NOISE = $\sqrt{(252)^2 + (60.6)^2 + (58)^2} \approx 265\mu V$ p-p

Figure 7B. Design Example

HOW THE OPERATIONAL AMPLIFIERS ARE CLASSIFIED

To assist the designer in distinguishing among the many types available from Analog Devices, we have provided a Selection Guide, in which amplifiers are grouped in terms of common properties which have been optimized in order to satisfy the needs of specific classes of applications. Once the choice has been narrowed to the manageable number of types in any group, distinctions can be drawn in terms of other requirements or considerations.

Temperature Range and Nomenclature. Analog Devices operational-amplifier nomenclature uses suffixes to permit ready identification of the temperature range for which device operation to meet critical specifications has been designed or selected. The most popular range comprises the "commercial" temperatures from 0 to 70°C; it is designated by suffixes such as J, K, L, M, in order of increasingly tighter specs (e.g., AD741L). Also popular is the "extended" range, -55°C to +125°C, designated by S, T, U, (e.g., AD510S); not all families have types with specified performance in this range. There are a few types designed for operation in the "industrial" range, -25°C to +85°C, designated by A, B. Wide-range types will generally meet the same or better specs in a narrower temperature range. A few types are second-sources for products originally introduced by other manufacturers. In those instances, the generic nomenclature is used (AD741C) or enlarged upon, if superior selections are offered (e.g., AD301AL).

1. *General-Purpose ICs.* Amplifiers in this group include our lowest-cost devices. They are best-suited for general purpose designs with moderate drift requirements, down to 5μV/°C max (AD301AL), and gain-bandwidth to 8MHz (AD301A). Typical applications include summing, inverting, impedance buffering (followers), and active filtering. They are also useful for developing nonlinear transfer functions, with appropriate external circuitry. Bipolar monolithic technology is used for all types. The AD741 is internally compensated; it does not require external capacitance for frequency compensation. On the other hand, the AD301A's ability to be externally compensated, by either lag or feedforward circuitry, permits circuits with a wide range of dynamic performance characteristics to be handled. Extended-temperature-range equivalents are the AD101A, AD201A, and AD741.

2. *Low Bias-Current, High Input-Impedance, FET-Input ICs.* These types use the inherently high impedance and low leakage current of junction field-effect transistors (FET's) to deal with configurations that either provide the measurement of low currents or require the use of high-resistance circuitry.

Typical applications range from general-purpose high-impedance circuitry to integrators, current-to-voltage converters, and log-function generation, to measurements with high-impedance transducers, such as photomultipliers, flame detectors, pH cells, and radiation detectors.

The performance range is from the 75fA (75×10^{-15} A) maximum bias current of the AD515L electrometer to the 100pA max of the general purpose, lowest-cost AD611. The AD542 is a low-cost, laser-wafer-trimmed (LWT) monolithic implanted FET input amplifier with low offset and drift. The AD544 is similar, but has higher speed. Low bias current does not necessarily imply large voltage offsets; the AD515K combines a 150fA (0.15pA) max bias current with 1.0mV max offset and 15μV/°C max voltage drift; comparable figures for the AD547L are 25pA, 0.25mV and 1μV/°C.

The types of amplifiers in this group either are completely monolithic or employ matched FET's and a special bipolar amplifier chip designed to accommodate the input FET's electrically. In nearly all the IC's, thin-film resistors are deposited on the chip at critical circuit locations to ensure stability; low offsets and drift are achieved by laser-trimming of circuit balance. All FET-input op amps from Analog Devices are manufactured to meet their published bias-current specifications *after full warmup* (some manufacturers specify *initial* current, which is lower than warmed-up bias current). Our published max bias-current specification applies to either input (some manufacturers call "bias current" the *average* of the two input currents). Bias current of junction FET's approximately doubles for every 10°C increase of temperature.

3. *FET-Input Dual ICs.* The AD642, AD644, and AD647 are a single-chip pair of trimmed implanted-FET-input (TRIFET) op amps similar to the AD542, AD644, and AD547 with low warmed-up bias current (35pA max – K, L, S), low offset voltage (0.5mV max – L), low offset-voltage drift (2.5μV/°C max – L), and excellent V_{OS} matching (0.25mV max – L). Besides applications calling for more than one FET-input op amp at low cost per function, the AD647 is especially useful

in applications calling for matched duals, such as log-ratio amplifiers, FET-input instrumentation amplifiers, and buffering of differential signals. The AD644, a wideband version, was designed for fast DAC amplifiers, sample and hold, filters and wideband instrument amplifiers.

4. *Electrometers.* This class comprises the lowest bias-current devices, the AD515. The AD515L, with its 75fA input bias current, 1mV max offset, and 25μV/°C offset tempco, has differential inputs, and can be used in voltage measurements at high impedance, as a follower, or in current measurements, as an inverter, or even differentially.

5. *High-Accuracy Low-Drift Differential-Input ICs.* "Chopperless" low-drift designs with differential inputs, optimized for voltage offset and drift, dc open-loop gain, and CMR, should be considered for high-accuracy instrumentation, low-level transducer bridge circuits, precision voltage comparators, and for impedance buffer designs.

Performance of internally compensated premium amplifiers in this group ranges from the ADOP-07A's 25μV max offset voltage and 0.6μV/°C drift, and the AD517L's 50μV max offset voltage and 1.3μV/°C drift, combined with 1nA max bias current (1.5nA max over the temperature range), and CMR of 110dB min, to the low-cost AD741L's maximum offset of 0.5mV and max offset tempco of 5μV/°C, with 100nA max bias current over the temperature range, and CMR of 90dB min.

The ADOP-07 is a superior second source to other OP-07 families; for example, ADOP-07AH has minimum gain of 3×10^6 V/V compared to 3×10^5 V/V.

Among *uncompensated* op amps, the premium range is from the AD OP-27 with 25μV maximum offset voltage, 0.6μV/°C max drift, 40nA max bias current over the temperature range, and 114dB CMR, to the low-cost AD301AL, with max offset of 0.5mV, max drift of 5μV/°C, max bias current of 45nA over the temperature range, and minimum CMR of 90dB. For applications in which low noise is essential, the AD OP-27 has 100%-tested guaranteed maximum voltage noise of 0.18μV p-p, for the frequency range 0.1 to 10Hz, and maximum spot noise of 5.5 and $3.8\text{V}/\sqrt{\text{Hz}}$ and 4.0 and $0.6\text{pA}/\sqrt{\text{Hz}}$, at 10Hz, and 1000Hz, respectively.

The AD741J/K/L and the AD301AL are selected from production lots of the generic AD741 and AD101A types. The AD504, AD510, and AD517 are thermally balanced for low drift and high gain (independent of output loading), with inputs that are bootstrapped for high CMR and protected against overloads to prevent bias-current degradation due to reverse breakdown. Thin-film resistors, deposited on the chip, are another key to the stability of these amplifiers. The AD510 and the AD517 employ super-beta input transistors to achieve low bias current, and they are laser-trimmed at the wafer-probe stage (LWT) to achieve their excellent offset-voltage specifications at low cost. Since the bias currents are always of one polarity, they can be nulled at a given temperature with simple circuitry; and the change over the temperature range will be considerably less than for low-cost FET-input amplifiers having comparable specifications.

Extended-temperature-range equivalents are AD504S, AD510S, AD714S, and AD517S.

6. Wide Bandwidth, Fast-Settling ICs. High-speed op amps are characterized by high slewing rates, fast settling time, and wide bandwidth. Fast settling time is especially important in applications with rapidly changing or switched analog data, in buffers, d/a converters, and multiplexer circuitry; wide small-signal bandwidth is important in preamplification and in handling low-level wideband ac signals; high slewing rate is associated with fast settling time and is also important in handling ac signals having large magnitudes with minimal distortion, since the large-signal bandwidth is closely related to the slewing rate.

The products in this category with outstanding specifications are models HOS-050, AD3554 and AD380. Settling of the hybrid HOS-050 is to within 0.01% in 300ns in the inverting connection. Model AD3554 max slewing rate is 1000V/μs inverting, and small-signal unity-gain bandwidth is 70MHz; full-power bandwidth is 16MHz, min. In addition, all of these devices will deliver ±100mA of output current at ±10V, an important factor in video and line-driver circuitry, and in driving capacitive loads. For example, the current required to sustain 500V/μs in a 100pF load is $I = C\,dV/dt = 50\text{mA}$. AD380 is optimized for settling time: 250ns maximum to 0.01%, inverting or noninverting, with output of ±50mA at ±10V.

There are three families of monolithic ICs listed in this category, with slewing rates ranging from 25V/μs min to 100V/μs min. The AD509S is the fastest slewing (100V/μs min) and settling (500ns min to 0.1% and 2.5μs min to 0.01%). The AD507K is the best all-around performer, with small-signal bandwidth of 35MHz, slewing rate of 25V/μs min, and typical settling to 0.1% within 900ns, in addition to open-loop dc gain of 10^5 min, drift of 15μV/°C max, and bias current of 15nA max. The AD518J is the lowest in cost, yet it slews at 50V/μs min, and typically settles to within 0.1% in 800ns, with single-capacitor compensation.

Extended-temperature-range equivalents are models AD507S, AD509S and AD518S.

DEFINITIONS OF SPECIFICATIONS

Absolute Maximum Differential Voltage
Under most operating conditions, feedback maintains the error voltage between inputs to nearly zero volts. However, in some applications, such as voltage comparators, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common-Mode Rejection
An ideal operational amplifier responds only to the difference voltage between inputs ($e^+ - e^-$) and produces no output for a *common-mode voltage*, that is, when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, or variations in offset voltage as a function of common-mode level, common-mode input voltages are not eliminated at the output. If the output error voltage, due to a known magnitude of common-mode voltage, is referred to the input (dividing by the closed-loop gain), it reflects the equivalent *common-mode error voltage* (CME) between the inputs. Common-mode rejection ratio (CMRR) is defined as the ratio of common-mode voltage to the resulting common-mode error voltage. Common-mode rejection is often expressed logarithmically: CMR (in dB) = 20 $\log_{10}$ (CMRR).

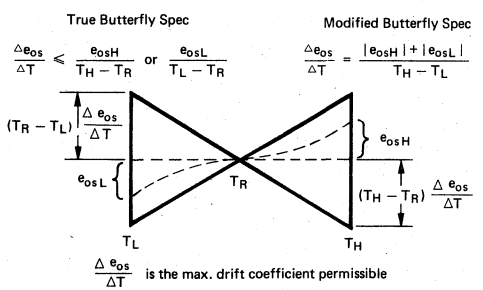
The precise specification of CMR is complicated by the fact that the common-mode voltage error can be a highly nonlinear function of common-mode voltage and also varies with temperature. As a consequence, CMR data published by Analog Devices are average figures, assuming an end-point measurement over the common-mode range specified. The incremental CMR about small values of common-mode voltage may be greater than the average CMR specified (on the other hand, the incremental CMR may be less in the neightborhood of large CMV). Published CMR specifications for op amps pertain to very low-frequency voltages, unless specified otherwise; CMR decreased with increasing frequency.

Common-Mode Voltage, Maximum
For differential-input amplifiers, the voltage at both inputs can swing about ground (power-supply common) level. *Common-mode voltage* is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error. This establishes the maximum input voltage for the voltage-follower connection.

Drift vs. Supply
Offset voltage, bias current, and difference current vary as supply voltage is varied. Usually, dc errors due to this effect are negligible compared to drift with temperature. No inference may be drawn from this low-frequency specification concerning the effects of rapid variation of voltage at the supply terminals.

Drift vs. Temperature
Offset voltage, bias current, and difference current all change, or "drift", from their initial values with temperature. This is by far the most important source of error in most precision applications. The temperature coefficients (tempcos) of those parameters are all defined as the average slope over a specified temperature range. Drift can be a nonlinear function of temperature (though it is often quite linear over limited temperature ranges); the slopes generally are greater at the extremes of temperature than around normal ambient (+25°C), which generally means that for small temperature excursions in the vicinity of +25°C, the specification is conservative.

Analog Devices precision operational amplifiers are specified by three- (or more-) point measurements, at 25°C and at the high and low extremes of the range (T_H, T_L), with the amplifier adjusted to zero at room temperature. The sum of the magnitudes of the drifts in the two ranges must be less than the specified drift rate (μV/°C or nA/°C) multiplied by the total temperature range (modified "butterfly"), or, in some cases, the magnitude of the drifts in both ranges must be less



than the specified drift rate multiplied by the respective temperature ranges ("true butterfly").

The lowest-cost second-source IC amplifiers are specified only in terms of the maximum value of the parameter (e.g., offset voltage) over temperature in the specified range.

Drift vs. Time
Offset voltage, bias current, and difference current change with time as components age. It is important to realize that drift with time is random, and rarely – if ever – accumulates linearly for healthy devices. For example, voltage drift for a chopper-stabilized amplifier might be quoted at 1μV/day, whereas cumulative drift over 30 days might not exceed 5μV, or 15μV in a year (e.g., model 235). A convenient rule of thumb for extrapolation is to divide the drift for a stated interval by the square root of its ratio to any other interval of interest.

Full-Power Response
The large-signal and small-signal response characteristics of operational amplifiers differ substantially. An amplifier's output will not respond to large signal changes as fast as the small-signal bandwidth characteristics would predict, primarily because of slew-rate limiting in the output stages. Full-power response is specified in two ways: full linear response and full peak response. Full linear response is specified in terms of the maximum frequency, at unity closed-loop gain, for which a

sinusoidal input signal will produce full output at rated load without exceeding a pre-determined distortion level. There is no industry-wide accepted value for the distortion level which determines the full-linear-response limitation, but we use 3% as a maximum acceptable limit for modules.

In many applications, the distortion caused by exceeding the full linear response can be comfortably ignored, but a more-serious effect (often overlooked) is an effect equivalent to a dc offset voltage that can be generated when full linear response is exceeded, due to rectification of the asymmetrical feedback waveform or overloading of the input stage by large distortion signals at the summing junction.

Another frequency response that is often if interest is the maximum frequency at which full output swing may be obtained, irrespective of distortion. This is termed "full peak response" and can often be found in a plot of output voltage swing vs. frequency.

Initial Bias Current
Bias current is defined as the current required at either input from an infinite source impedance to drive the output to zero (assuming zero common-mode voltage). For differential amplifiers, bias current is present at both the negative and the positive input. All Analog Devices specifications pertain to the *larger* of the two, *not the average.* For single-ended amplifiers (i.e., chopper types), bias current refers to the current at the input terminal.

Analog Devices specifies initial bias current, I_b, as the bias current at either input, specified at +25°C ambient with the input junctions *at normal operating temperature* (some manufacturers specify initial bias current at power turn-on. Such specifications may be misleading. For example, in FET-input amplifiers, bias current is doubled for each 10°C increase; since junction temperatures may warm up to 20°C or more above ambient, the "initial bias current" spec used by some manufacturers may be met only during a brief interval after the power is burned on, and I_b may be quadrupled under ordinary operation conditions.)

Initial Difference Current
Difference current is defined as the difference between the bias currents at the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current has not been compensated at the input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance
Differential input impedance is defined as the impedance between the two input terminals at +25°C, assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be represented by a capacitor in parallel with a resistor.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, is defined as the impedance between each input and power-supply common, specified at +25°C. For most circuits, common-mode impedance on the negative input has little significance, except for the capacitance which it adds at the summing junction (one exception is electrometer circuitry). However, common-mode impedance on the plus input sets the upper limit on closed-loop input impedance for the non-inverting configuration. Common-mode impedance is a nonlinear function of both temperature and common-mode voltage. For FET-input amplifiers, common-mode resistance is reduced by a factor of two for each 10° of temperature rise. As a function of common-mode voltage, the resistive component is defined as the average resistance for a common-mode change from zero to the maximum common-mode voltage. Incremental resistance may be less than the specified average value, especially at full-scale for some FET-input amplifiers.

Input Offset Voltage
Offset voltage is defined as the voltage required at the input from zero source impedance to drive the output to zero; its magnitude is measured by closing the loop (using low values of resistance) to establish a large fixed gain, measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25°C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Input Noise
Input voltage- and current-noise characteristics can be specified and analyzed in much the same way as offset-voltage and bias-current characteristics. In fact, long-term drift can be considered as noise which occurs at very low frequencies. The primary difference is that, when evaluating noise performance, bandwidth must be considered. Also rms noise from different sources is summed by root-sum-of-squares, rather than linear, addition. Depending on the amplifier design, noise may have differing characteristics as a function of frequency, being dominated by "1/f noise", resistor noise, or junction noise, at various frequencies.

For this reason, several noise specifications are given. Low-frequency noise in the band 0.01 to 1Hz (or 0.1 to 10Hz) is specified as peak-to-peak, with a 3.3σ uncertainty, signifying that 99.9% of the observed peak-to-peak excursions will fall within the specified limits. Wideband noise is specified as rms. For some types, spectral-density plots or "spot noise", at specific frequencies, in $\mu V/\sqrt{Hz}$ or $pA/\sqrt{Hz}$, are provided.

Open-Loop Gain
Open-loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; for this reason, the typical open-loop gain as a function of frequency is published for each amplifier type. See also *unity gain small-signal response.*

Overload Recovery
Overload recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% overdrive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feedback network.

Rated Output
Rated output *voltage* is the minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out-of-spec nonlinearity occurs. Rated output *current* is the minimum guaranteed value of current supplied at the rated output voltage (or other specified voltage). Load impedances less than the specified (or implied) value can be used, but the maximum output voltage will decrease, distortion may increase, and the open-loop gain will be reduced. (All models are short-circuit protected to ground, and many are safe against shorts to the supplies.)

Settling Time
Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required: for the signal to propagate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate-limited overload (if it occurs), and settle to a given error in the linear range. It may also include a "long tail" due to the time required to reach thermal equilibrium, or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels, and no (or a specified value of) capacitive loading, and any specified compensation. A full-scale unipolar step input is used, and both polarities are tested.

Although settling time can generally be grossly inferred from the other amplifier specifications (an amplifier that has extra-wide small-signal bandwidth, extra-fast slewing, and excellent full-power response may reasonably – but not always – be expected to have fast settling), the settling time cannot usually be rationally predicted from the other dynamic specifications.

Slewing Rate
The slewing rate of an amplifier, usually in volts per microsecond (V/μs), defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small-Signal Response
Unity-gain small-signal response is the frequency at which the open-loop gain falls to 1V/V, or 0dB under a specified compensation condition. "Small signal" indicates that, in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or signal rectification. For amplifiers with symmetrical response for signals applied to either input, the dynamic behavior will be consistent for both inverting and non-inverting configurations. However, if feedforward compensation is used, fast response will be available only on the negative input, restricting fast applications of the device to the inverting mode.

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"How to Test Operational Amplifier Parameters", Application Note Section 20 of Volume I

USEFUL TUTORIAL MATERIAL IN DATA SHEETS

Electrometer Circuitry, see AD515

High-Speed Amplifiers, see AD518 and Models 50/51

Low-Drift Differential Op Amp Performance, see AD504

Low-Level Applications of Chopper-Stabilized Amplifiers:
Inverting, see Models 234, 235
Non-Inverting, see Model 261

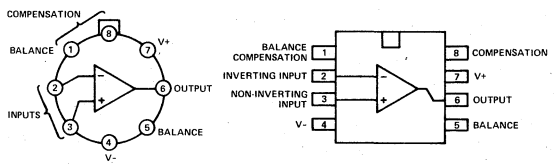
General Purpose Low Cost IC Operational Amplifier

AD101A, AD201A, AD301A, AD301AL

FEATURES

- Low Bias and Offset Current
- Single Capacitor External Compensation for Operating Flexibility
- Nullable Offset Voltage
- No Latch-Up
- Fully Short Circuit Protected
- Wide Operating Voltage Range

AD101 SERIES FUNCTIONAL BLOCK DIAGRAMS



TO-99 MINI DIP

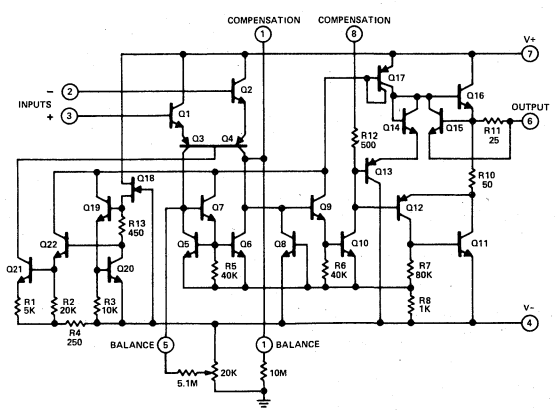
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD101A, AD201A, AD301A and AD301AL are high performance monolithic operational amplifiers. All the circuits feature full short circuit protection, external offset voltage nulling, wide operating voltage range, and the total absence or "latch-up". Because frequency compensation is performed externally with a single capacitor (30pF maximum), the AD101A, AD201A, AD301A and AD301AL provide greater flexibility than internally compensated amplifiers since the degree of compensation can be fitted to the specific system application.

The AD101A and AD201A have identical specifications in the TO-99 package; the former guaranteed over the −55°C to +125°C temperature range, and the latter over −25°C to +85°C. The AD201A is also available in the mini-DIP package for high performance operation over the 0 to +70°C temperature range. The AD301A is specified for operation over the 0 to +70°C temperature range in both the TO-99 and mini-DIP packages. The AD301AL is the highest accuracy version of this series. Improved processing and additional electrical testing allow the user to achieve precision performance at low cost. The device provides substantially increased accuracy by reducing errors due to offset voltage (0.5mV max), offset voltage drift (5.0μV/°C max), bias current (30nA max), offset current (5nA max), voltage gain (80,000 min), PSRR (90dB min), and CMRR (90dB min). The AD301AL is also specified from 0 to +70°C and is available in the TO-99 can or 8-pin mini-DIP.

SCHEMATIC DIAGRAM



SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

ABSOLUTE MAXIMUM RATINGS	AD101A, AD201A, AD301A, AD301AL unless otherwise specified
Supply Voltage	
AD101A, AD201A	±22V
AD301A, AD301AL	±18V
Power Dissipation[1]	
TO-99 (Metal Can)	500mW
Dual In-Line (Mini-DIP)	500mW
Differential Input Voltage	±30V
Input Voltage[2]	±15V
Output Short Circuit Duration[3]	Indefinite
Operating Temperature Range	
AD101A	−55°C to +125°C
AD201A (TO-99)	−25°C to +85°C
AD201A (Mini-DIP)	0 to +70°C
AD301A, AD301AL	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60sec)	300°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise specified)[4]

Parameter	Conditions	AD101A/AD201A Min	AD101A/AD201A Typ	AD101A/AD201A Max	AD301A Min	AD301A Typ	AD301A Max	AD301AL Min	AD301AL Typ	AD301AL Max	Units
Input Offset Voltage	$R_S \leq 50k\Omega$		0.7	2.0		2.0	7.5		0.3	0.5	mV
Input Offset Current			1.5	10		3	50		3	5	nA
Input Biz											
Input Bias Current			30	75		70	250		15	30	nA
Input Resistance		1.5	4		0.5	2		1.5	4		MΩ
Supply Current	V_S = ±20V		1.8	3.0							mA
	V_S = ±15V					1.8	3.0		1.8	3	mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	50	160		25	160		80	300		V/mV
The Following Specifications Apply Over the Operating Temperature Ranges[4]											
Input Offset Voltage	$R_S \leq 10k\Omega$			3.0			10		0.5	1	mV
Input Offset Current				20			70		5	10	nA
Average Temp. Coefficient of Input Offset Voltage	$T_A(min) \leq T_A \leq T_A(max)$		3.0	15		6.0	30		2	5	μV/°C
Average Temp. Coefficient of Input Offset Current	$+25°C \leq T_A \leq T_A(max)$		0.01	0.1		0.01	0.3		0.01	0.1	nA/°C
	$T_A(min) \leq T_A \leq +25°C$		0.02	0.2		0.02	0.6		0.01	0.1	nA/°C
Input Bias Current				100			300		30	45	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 2k\Omega$	25			15			40	100		V/mV
Input Voltage Range	V_S = ±20V	±15									V
	V_S = ±15V				±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	90		90	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		70	96		90	100		dB
Output Voltage Swing	V_S = ±15V, R_L = 10kΩ	±12	±14		±12	±14		±12	±14		V
	V_S = ±15V, R_L = 2kΩ	±10	±13		±10	±13		±10	±13		V
Supply Current	$T_A = T_A$ (max), V_S = ±20V		1.2	2.5					1.8	3	mA

NOTES

[1] The maximum desirable junction temperature of the AD101A is +150°C; that of the AD201A, AD301A and AD301AL is +100°C. For operating at elevated temperatures, devices must be derated based upon a thermal resistance of +150°C/W, junction to ambient, or +45°C/W, junction to case. The thermal resistance of the Dual In-Line package is +160°C/W, junction to ambient.

[2] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

[3] For the AD301A and AD301AL continuous short circuit is allowed for case temperatures to +70°C and ambient temperatures to +55°C.

[4] Unless otherwise specified, these specifications apply for supply voltages and ambient temperatures of ±5V to ±20V and −55°C to +125°C for the AD101A, ±5V to ±20V and −25°C to +85°C for the AD201AH (0 to +70°C for the AD201AN), and ±5V to ±15V and 0 to +70°C for the AD301A and AD301AL.

Specifications subject to change without notice.

ORDERING GUIDE

MODEL	TEMP RANGE	ORDER NUMBER*	PACKAGE OPTION**
AD301AL	0 to +70°C	AD301AL	TO-99, N8A
AD201A	−25°C to +85°C	AD201A	TO-99, N8A
AD301A	0 to +70°C	AD301A	TO-99, N8A
AD101A	−55°C to +125°C	AD101AH	TO-99

*Add package type leter: H = TO-99, N = Mini DIP.
**See Section 19 for package outline information.

FREQUENCY COMPENSATION CIRCUITS

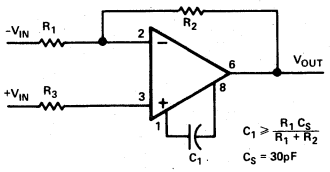


Figure 1. Single Pole Compensation

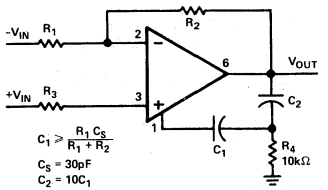


Figure 2. Two Pole Compensation

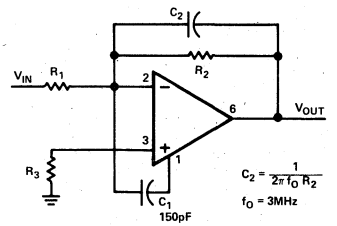
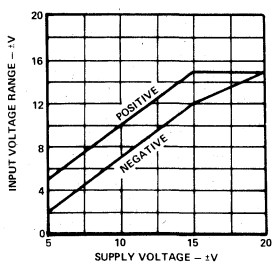
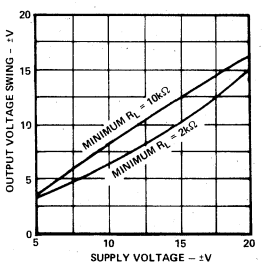


Figure 3. Feedforward Compensation

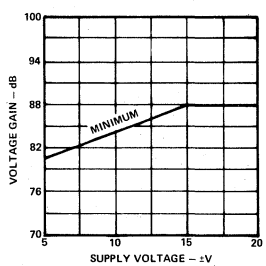
GUARANTEED PERFORMANCE CURVES (Curves apply over the Operating Temperature Ranges)



Input Voltage Range

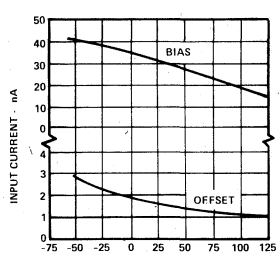


Output Swing

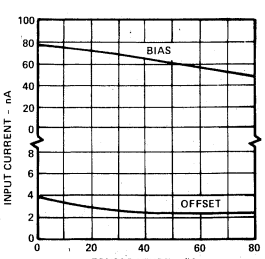


Voltage Gain

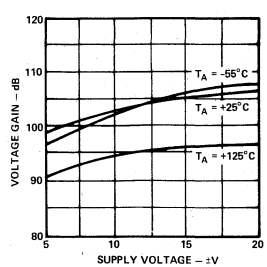
TYPICAL PERFORMANCE CURVES[4]



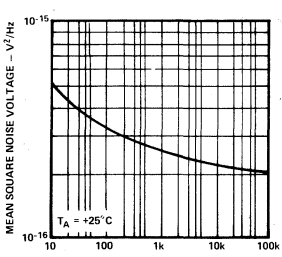
Input Current AD101A, AD201A



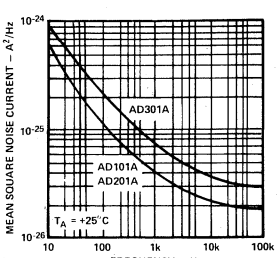
Input Current – AD301A



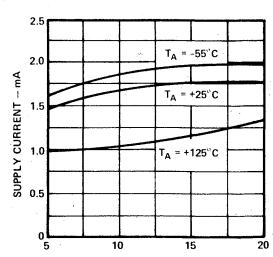
Voltage Gain



Input Noise Voltage

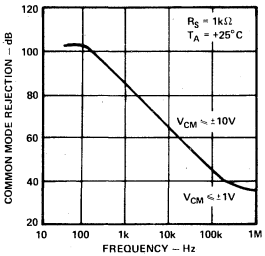


Input Noise Current

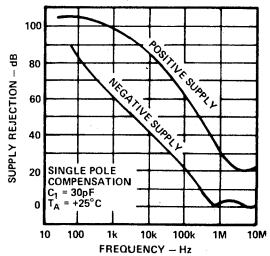


Supply Current

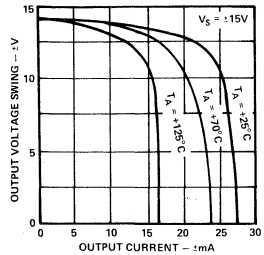
TYPICAL PERFORMANCE CURVES



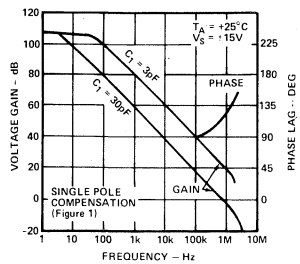
Common Mode Rejection



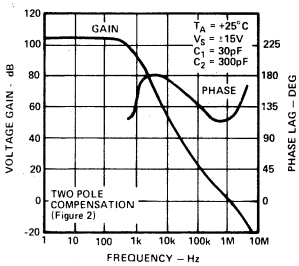
Power Supply Rejection



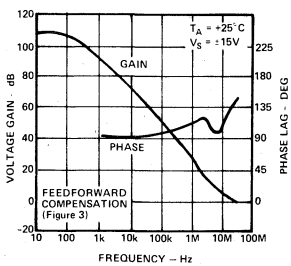
Current Limiting



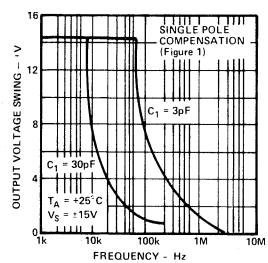
Open Loop Frequency Response



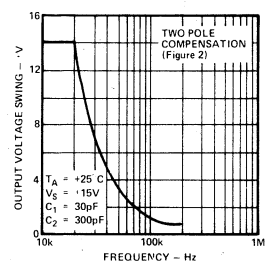
Open Loop Frequency Response



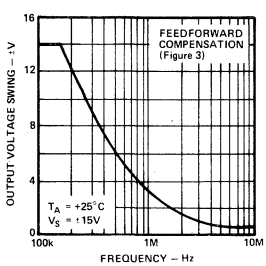
Open Loop Frequency Response



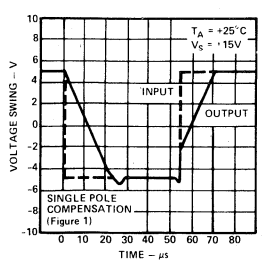
Large Signal Frequency Response



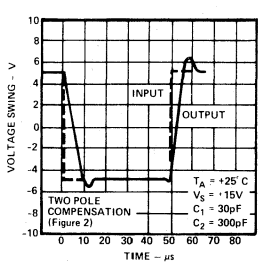
Large Signal Frequency Response



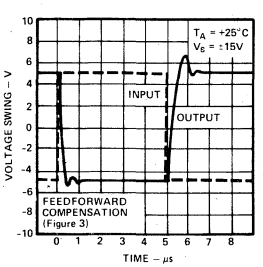
Large Signal Frequency Response



Voltage Follower Pulse Response



Voltage Follower Pulse Response



Inverter Pulse Response

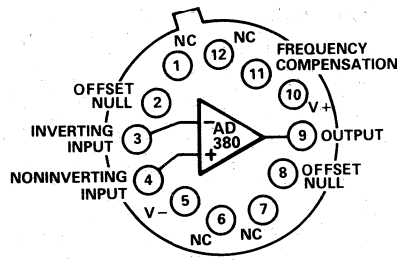
Wideband, Fast-Settling FET-Input Op Amp

AD380

FEATURES

High Output Current: 50mA @ ±10V
Fast Settling to 0.1%: 130ns
High Slew Rate: 330V/μs
High Gain-Bandwidth Product: 300MHz
High Unity Gain Bandwidth: 40MHz
Low Offset Voltage (1mV for AD380K, L, S)

AD380 FUNCTIONAL BLOCK DIAGRAM



12-PIN TO-8 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD380 is a hybrid operational amplifier that combines the low input bias current advantages of a FET input stage with the high slew rate and line driving capability of a fast, high power output amplifier.

The AD380 has a slew rate of 330V/μs and will output ±10V at ±50mA. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate, or settling time for the given application.

A true differential input ensures equally superior performance in all system designs whether they are inverting, noninverting, or differential.

The AD380 is especially designed for use in applications, such as fast A/D, D/A and sampling circuits, that require fast and smooth settling and FET input parameters.

The AD380 is offered in three commercial versions, J, K and L specified from 0 to +70°C and one extended temperature version, the S, specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-8 style cans.

PRODUCT HIGHLIGHTS

1. The AD380's high output current (50mA @ ±10V) makes it suitable for driving terminated 200Ω twisted pairs.
2. The fast settling output (250ns to 0.01%) makes the AD380 an ideal choice for video A/D and D/A converters and sample and hold applications.
3. The settling wave forms are not only fast but are also very smooth. The absence of large overshoot and oscillations makes the AD380 a very predictable and dependable system element.
4. The high gain-bandwidth product (300MHz) ensures low distortion in high frequency applications.
5. Quick, symmetrical overdrive recovery time (250ns) is assured by an internal antisaturation diode. This is useful in applications where large transient signals may occur.
6. The precision input (1mV offset, max), along with fast settling and high current output make the AD380 an excellent choice for:
   - ATE pin drivers
   - precision coax buffers
   - signal conditioning on pulse waveforms
   - high resolution graphics displays.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD380JH	AD380KH	AD380LH	AD380SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, no load	40,000 min	*	*	*
V_{OUT} = ±10V, $R_L \geq 200\Omega$	25,000 min	*	*	*
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 200Ω, T_A = min to max	±12V (±10V min)	*	*	*
Output Impedance (Open Loop)	100Ω	*	*	*
Short Circuit Current	100mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	40MHz	*	*	*
Gain-Bandwidth Product, f = 100kHz, C_C = 1pF	300MHz (200MHz min)	*	*	*
Full Power Response	6MHz	*	*	*
Slew Rate, C_C = 1pF, 20V Swing	330V/μs (200V/μs min)	*	*	*
Settling Time: 10V Step to 1%	90ns	*	*	*
10V Step to 0.1%	130ns	*	*	*
10V Step to 0.01%	250ns	250ns (400ns max)	**	**
INPUT OFFSET VOLTAGE	2.0mV max	1.0mV max	**	**
vs. Temperature[1], T_A = min to max	50μV/°C max	20μV/°C max	10μV/°C max	50μV/°C max
vs. Supply	1mV/V max	*	*	*
INPUT BIAS CURRENT				
Either Input, Initial[2]	10pA (100pA max)	*	*	*
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{11}\Omega \| 6pF$	*	*	*
Common Mode	$10^{11}\Omega \| 6pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[3]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	60dB min	*	*	*
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(6 to 20)V	*	*	*
Quiescent Current	12mA (15mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz to 100Hz	3.3μV p-p (0.5μV rms)	*	*	*
100Hz to 10kHz	6.6μV p-p (1μV rms)	*	*	*
10kHz to 1MHz	40μV p-p (6μV rms)	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance θ_{JA}	100°C/W	*	*	*
θ_{JC}	70°C/W	*	*	*
PACKAGE[4]				
TO-8 Style	H12A	*	*	*

NOTES
[1]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of offset nulled.
[2]Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures see Figure 16.
[3]Defined as the maximum safe voltage between inputs such that neither exceeds ±10V from ground.
[4]See Section 19 for package outline information.

*Specifications same as AD380JH.
**Specifications same as AD380KH.
Specifications subject to change without notice.

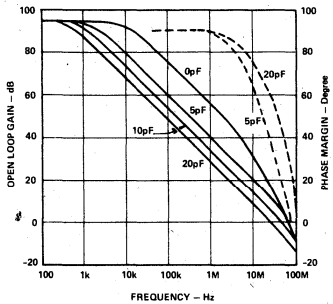


Figure 1. Open Loop Frequency Response

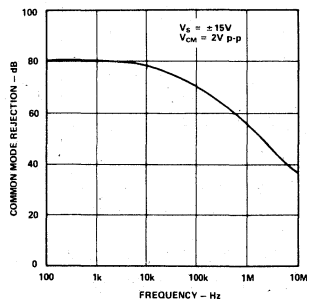


Figure 2. CMRR vs. Frequency

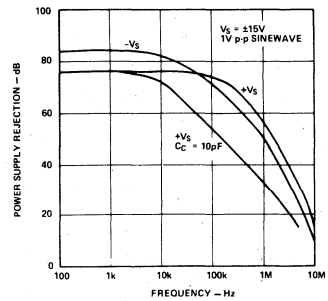


Figure 3. PSRR vs. Frequency

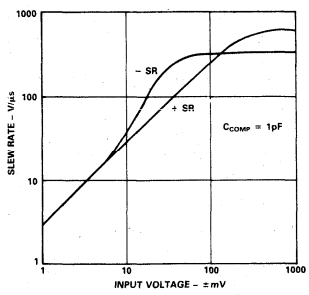


Figure 4. Slew Rate vs. Differential Input Voltage

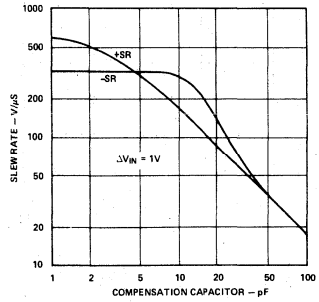


Figure 5. Slew Rate vs. Compensation Capacitor

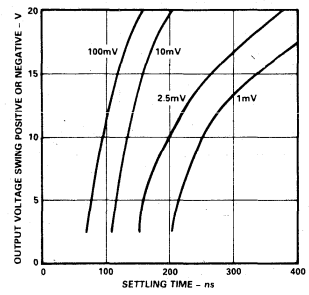


Figure 6. Output Settling Time vs. Output Voltage Swing and Error

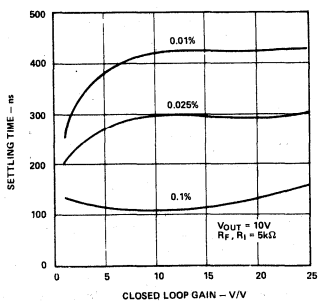


Figure 7. Settling Time vs. Closed Loop Gain

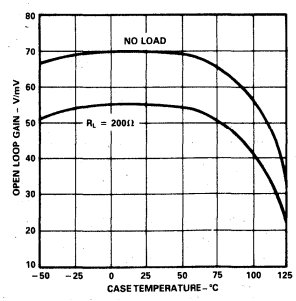


Figure 8. Gain vs. Temperature

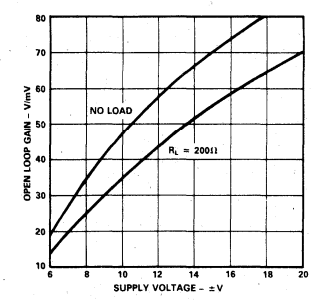


Figure 9. Gain vs. Supply Voltage

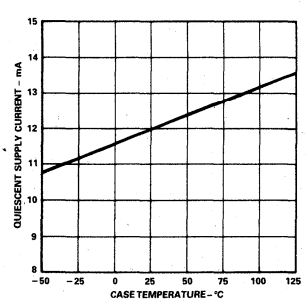


Figure 10. Supply Current vs. Temperature

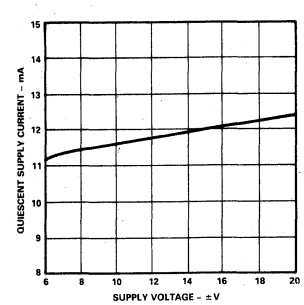


Figure 11. Supply Current vs. Supply Voltage

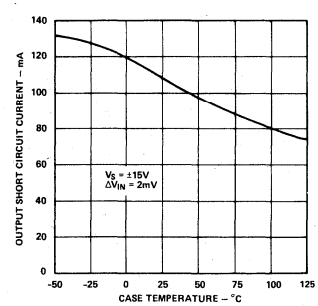


Figure 12. I_{SC} vs. Temperature

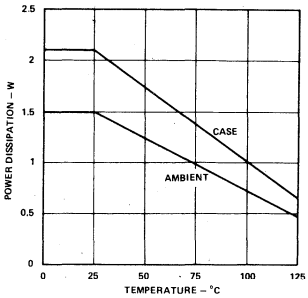


Figure 13. Power Dissipation vs. Temperature

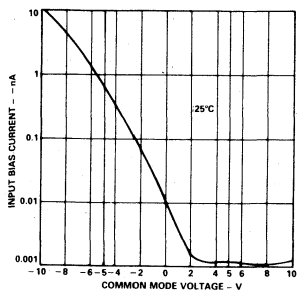


Figure 14. Input Bias Current vs. Common Mode Voltage

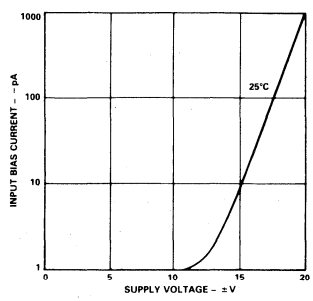


Figure 15. Input Bias Current vs. Supply Voltage

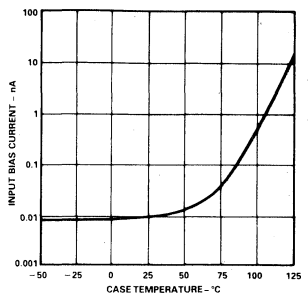


Figure 16. Input Bias Current vs. Temperature

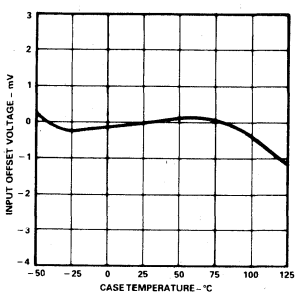


Figure 17. Offset Voltage vs. Temperature

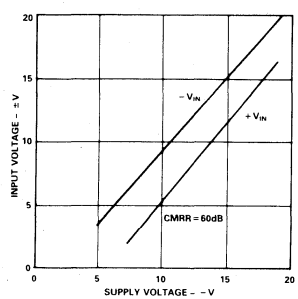


Figure 18. Input Voltage Range vs. Supply Voltage

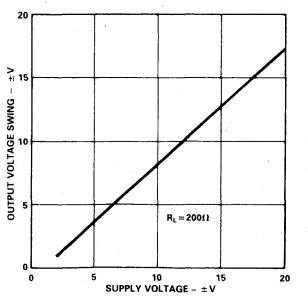


Figure 19. Output Voltage Swing vs. Supply Voltage

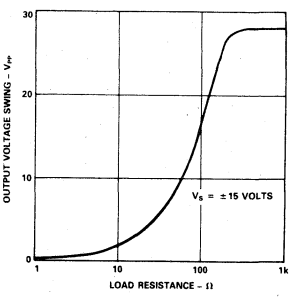


Figure 20. Output Voltage Swing vs. Load Resistance

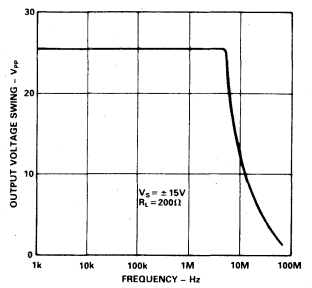


Figure 21. Large Signal Frequency Response

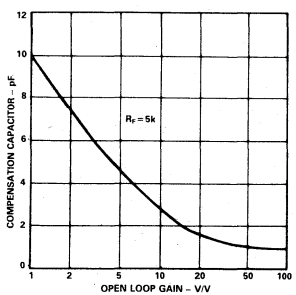


Figure 22. Recommended Compensation Capacitor vs. Closed Loop Gain

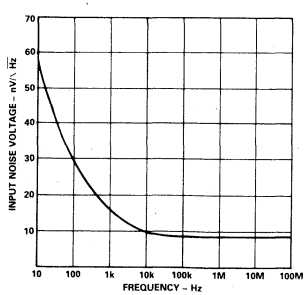


Figure 23. Input Noise Voltage Spectral Density

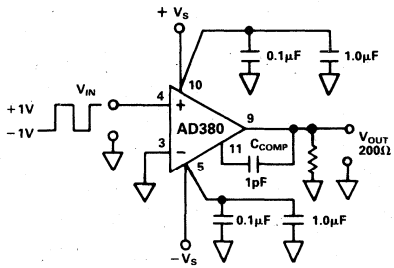


Figure 24a. Overdrive Recovery Test Circuit

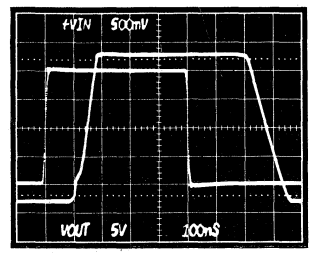


Figure 24b. Overdrive Recovery Response (Symmetrial 20ns Version Available)

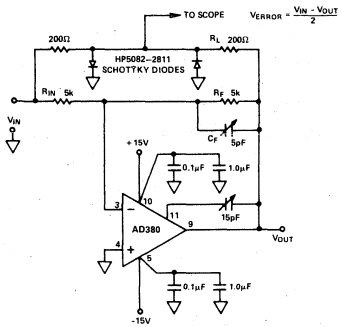


Figure 25a. Unity Gain Inverter Settling Time Test Circuit

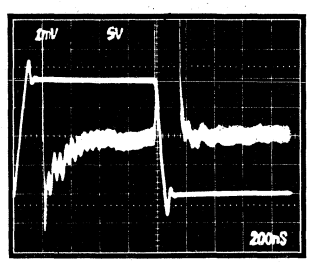


Figure 25b. Unity Gain Inverter Large Signal Response

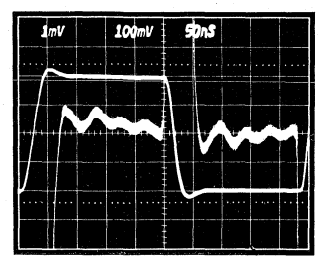


Figure 25c. Unity Gain Inverter Small Signal Response

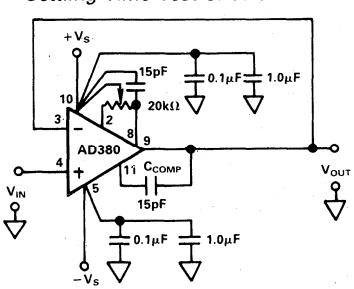


Figure 26a. Unity Gain Buffer Circuit

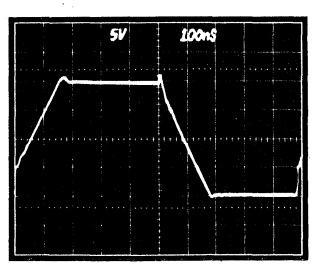


Figure 26b. Unity Gain Buffer Large Signal Response

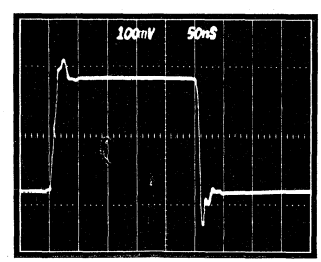


Figure 26c. Unity Gain Small Signal Response

APPLICATIONS INFORMATION

Compensation Capacitor

For low gain applications a 5pF to 27pF capacitor between the frequency compensation input (pin 11) and the output (pin 9) will reduce the risk of oscillation by adding phase margin. A compensation capacitor is especially needed when driving capacitive loads. For gains greater than 30 a 1pF compensation capacitor is recommended; see Figure 22.

For unity gain buffer applications it may be necessary to add a small (10pF to 20pF) capacitor between pins 8 and 10 for improved phase margin; see Figure 26a.

Offset Null

If the initial offset voltage is not low enough for the user's application offset nulling is required. To null the offset tie a 20kΩ potentiometer between the offset null pins (pins 2 and 8). The wiper of the potentiometer is tied to the positive supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

To minimize the effects of offset voltage drift as a function of temperature, null the offset at the midpoint of the operating temperature range. For example, if the operating environment is 0°C to 70°C do the offset nulling at 35°C. This will insure a maximum offset voltage drift of 35 times the V_{OS} drift specification at either temperature extreme.

Typical Circuits

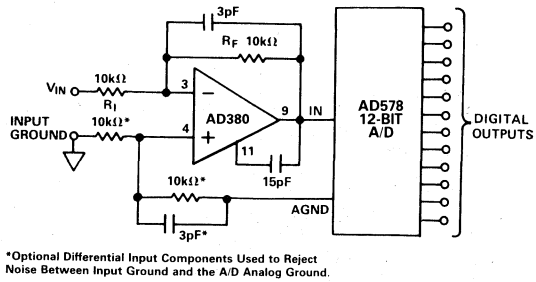


Figure 27. Fast-Settling Buffer

Its quick recovery from load variations makes the AD380 an excellent buffer for fast successive approximation A/D converters; see Figure 27.

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

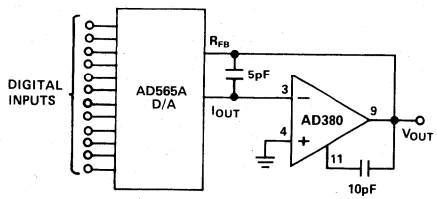


Figure 28. 12-Bit Voltage Output DAC Circuit Settles to 1/2LSB in 300ns

The AD565A 12-bit digital to analog converter with an AD380 output amplifier will give a voltage output that typically settles to within 1/2LSB in less than 300ns. Total settling time is the root mean square of the DAC current output settling time and the output amplifier settling time.

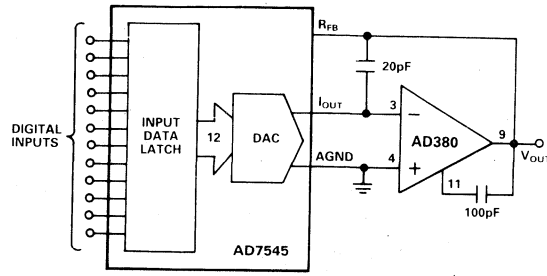


Figure 29. CMOS DAC Output Amplifier

CMOS DAC output amplifiers require low offset voltage op amps. The output impedance of CMOS DACs varies with input code. This can cause a code dependent error term at the output that approaches the op amps' offset voltage. If the DAC has a differential nonlinearity of 1/2LSB, it will require an output amplifier with less than 1/2LSB offset error to remain monotonic. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus, the AD380KH, with only 1mV offset maximum, will contribute less than 1/2LSB to differential linearity error.

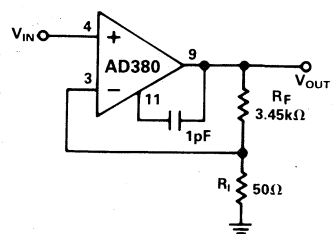


Figure 30. Video Amplifier

The high output current capability of the AD380 makes it suitable for video speed driver applications. In the circuit above the closed loop gain of 70 (37dB) is available over a bandwidth of 5MHz. Note that a 1pF compensation capacitor is required in this high gain application.

ANALOG DEVICES

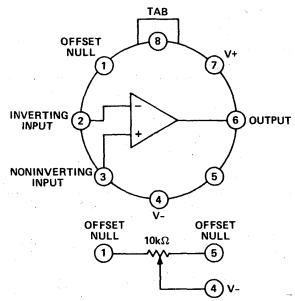
High Speed, Low Drift FET Operational Amplifier

AD381/AD382

FEATURES

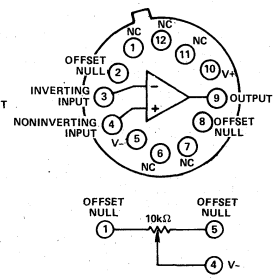
- **High Slew Rate 30V/μs**
- **Fast Settling to 0.1%: 750ns**
- **High Output Current: 50mA for AD382 (10mA for AD381)**
- **Low Drift (5μV/°C–L Grades)**
- **Low Offset Voltage (0.25mV–L Grades)**
- **Low Input Bias Currents**
- **Low Noise (2μV p-p)**

AD381
PIN CONFIGURATION



TOP VIEW

AD382
PIN CONFIGURATION



TOP VIEW

PRODUCT DESCRIPTION

The AD381/AD382 are hybrid operational amplifiers combining the very low input bias current advantages of a FET input stage with high slew rate and line driving capability of a high power output stage.

The offset voltage (0.25mV maximum for the L grades) and offset voltage drift (5μV/°C maximum for the L grades) are exceptionally low for high speed operational amplifiers.

In addition to superior low drift performance, the AD381 and AD382 offer the lowest guaranteed input bias currents of any wideband FET amplifier with 100pA max for the J grades of each and 50pA max for the AD382L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our FET amplifiers are specified under actual operating conditions.

The AD381 and AD382 are especially designed for use in applications, such as precision high speed data acquisition systems and signal conditioning circuits, that require excellent input parameters and a fast, high power output.

The AD381 and AD382 are offered in three commercial versions, J, K and L specified from 0 to +70°C, and one extended temperature version, the S specified from −55°C to +125°C. All grades are packaged in hermetically sealed metal cans.

PRODUCT HIGHLIGHTS

1. Laser trimming techniques reduce offset voltage drift to 5μV/°C max and reduce offset voltage to only 0.25mV max on the L grade versions.
2. Analog Devices FET processing provides 100pA max (20pA typical) bias currents specified after 5 minutes of warm-up.
3. Internal frequency compensation, low offset voltage, and full device protection eliminate the need for external components and adjustments. This reduces circuit size and complexity and increases reliability.
4. The fast settling output (750ns to 0.1%) makes the AD381 and AD382 ideal for D/A and A/D converter amplifier applications.
5. The AD382's high output current (50mA minimum at ±10 volts) makes it suitable for driving terminated (200Ω) twisted pair outputs over the commercial temperature ranges.
6. The high slew rate (30V/μs) and high gain bandwidth product (5MHz) make the AD381 and AD382 an ideal choice for sample and holds and for high speed integrator circuits.

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD381JH AD382JH	AD381KH AD382KH	AD381LH AD382LH	AD381SH AD382SH
OPEN LOOP GAIN				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$ (AD381)	60,000 min	100,000 min	**	**
V_{OUT} = ±10V, R_L = 200Ω (AD382)	25,000 min	35,000 min	**	**
R_L = 10kΩ (AD382)	100,000	150,000	**	**
OUTPUT CHARACTERISTICS (AD382)				
Voltage @ R_L = 200Ω	±12V (±10V min)	*	*	Note 1
Voltage @ R_L = 10kΩ	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	80mA	*	*	*
OUTPUT CHARACTERISTICS (AD381)				
Voltage @ R_L = 1kΩ, T_A = min to max	±12V (±10V min)	*	*	Note 2
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)	*	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)	*	*	*
Short Circuit Current, Continuous	20mA	*	*	*
DYNAMIC RESPONSE				
Unity Gain, Small Signal	5MHz	*	*	*
Full Power Response	500kHz	*	*	*
Slew Rate, Unity Gain	30V/μs (20V/μs min)	*	*	*
Settling Time: 10V Step to 0.1%	700ns	*	*	*
10V Step to 0.01%	1.2μs	1.2μs (2.0μs max)	**	**
INPUT OFFSET VOLTAGE	1.0mV max	0.5mV max	0.25mV max	*
vs. Temperature, T_A = min to max[3]	15μV/°C max	10μV/°C max	5μV/°C max	10μV/°C max
vs. Supply	200μV/V max	100μV/V max	**	**
INPUT BIAS CURRENT[4]				
Either Input	20pA (100pA max)	10pA (50pA max)(* for AD381)	**(* for AD381)	**(* for AD381)
Input Offset Current	5pA	*	*	*
INPUT IMPEDANCE				
Differential	$10^{12}\Omega \| 7pF$	*	*	*
Common Mode	$10^{14}\Omega \| 7pF$	*	*	*
INPUT VOLTAGE RANGE				
Differential[5]	±20V	*	*	*
Common Mode	±12V (±10V min)	*	*	*
Common-Mode Rejection, V_{IN} = ±10V	70dB min	80dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	
Quiescent Current AD382	3.4mA (6mA max)	*	*	*
AD381	3.2mA (5mA max)	*	*	*
VOLTAGE NOISE				
0.1Hz–10Hz	2μV p-p	*	*	*
10Hz	35nV/√Hz	*	*	*
100Hz	22nV/√Hz	*	*	*
1kHz	18nV/√Hz	*	*	*
10kHz	16nV/√Hz	*	*	*
TEMPERATURE RANGE				
Operating, Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
Thermal Resistance – θJA (AD382)	100°C/W	*	*	*
Thermal Resistance – θJC (AD382)	70°C/W	*	*	*

NOTES

[1]The AD381SH has an output voltage of ±12V (±10V min) for a 1kΩ load from T_{min} to +70°C. From +70°C to +125°C the output current is 7mA.

[2]The AD382SH has an output voltage of ±12V (±10V min) for a 200Ω load from T_{min} to +100°C. To +125°C the output current is 35mA.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C for every mV of offset nulled.

[4]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as J grade.

**Specifications same as K grade.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Initial Offset	Offset T.C.	Output	Package[1]
AD381JH	1mV	15μV/°C	10mA	H08B
AD381KH	0.5mV	10μV/°C	10mA	H08B
AD381LH	0.25mV	5μV/°C	10mA	H08B
AD381SH	1mV	10μV/°C	10mA	H08B
AD382JH	1mV	15μV/°C	50mA	H12A
AD382KH	0.5mV	10μV/°C	50mA	H12A
AD382LH	0.25mV	5μV/°C	50mA	H12A
AD382SH	1mV	10μV/°C	50mA	H12A

NOTE

[1]See Section 19 for package outline information.

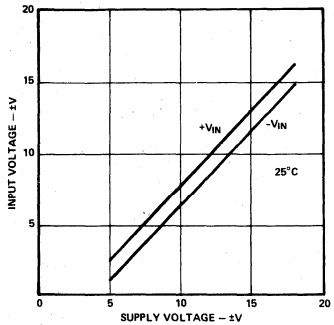


Figure 1. Input Voltage Range vs. Supply Voltage

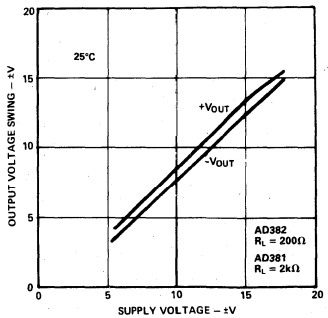


Figure 2. Output Voltage Swing vs. Supply Voltage

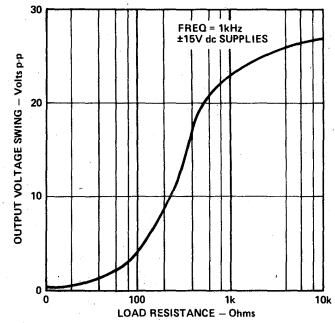


Figure 3a. Output Voltage Swing vs. Load Resistor for AD381

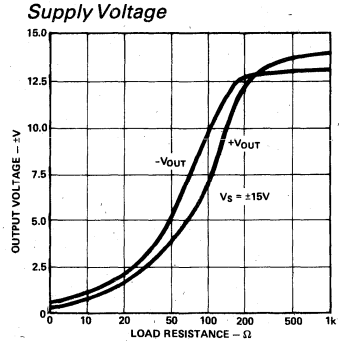


Figure 3b. Output Voltage Swing vs. Load Resistor for AD382

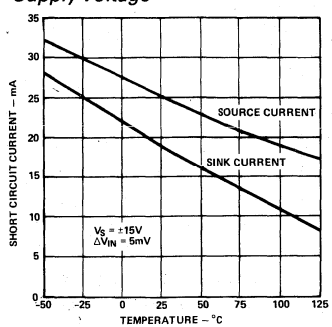


Figure 4a. Short Circuit Current vs. Temperature for AD381

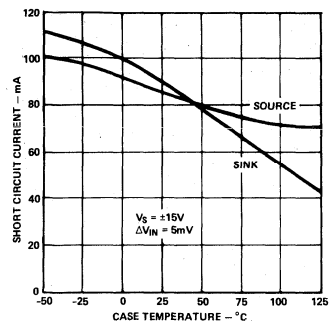


Figure 4b. Short Circuit Current vs. Temperature for AD382

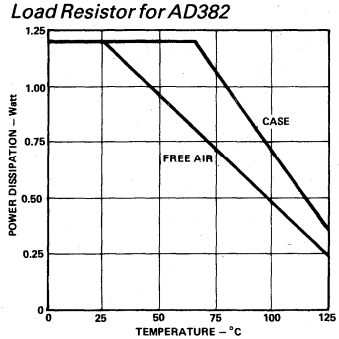


Figure 5. Permitted Dissipation vs. Temperature for AD382

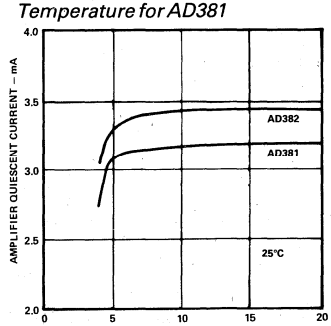


Figure 6. Quiescent Current vs. Supply Voltage

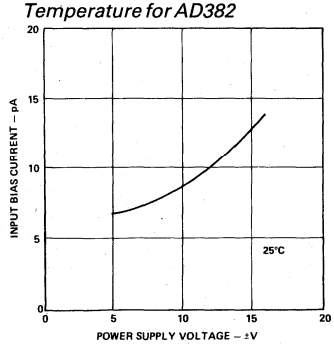


Figure 7. Input Bias Current vs. Supply Voltage

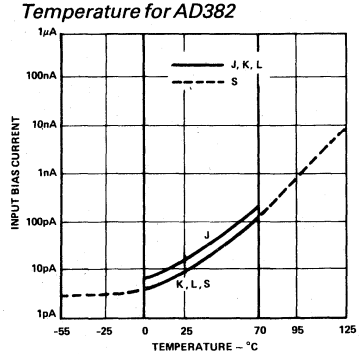


Figure 8. Input Bias Current vs. Temperature

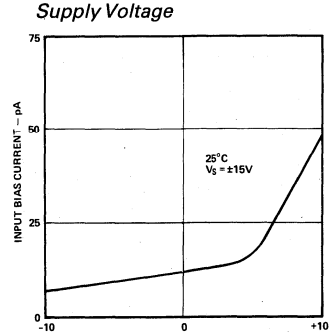


Figure 9. Input Bias Current vs. CMV

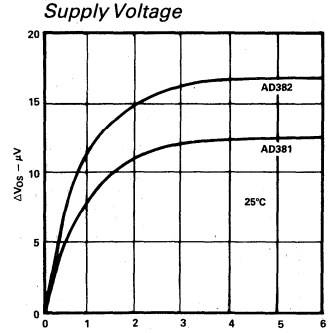


Figure 10. Input Offset Voltage Turn On Drift vs. Time

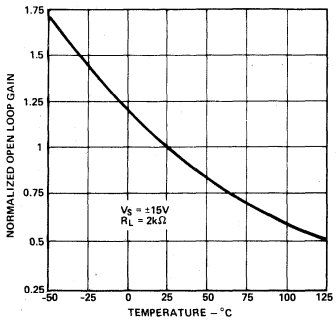


Figure 11a. Open Loop Gain vs. Temperature for AD381

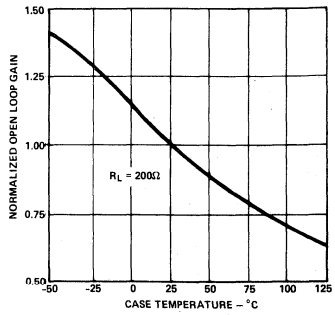


Figure 11b. Open Loop Gain vs. Temperature for AD382

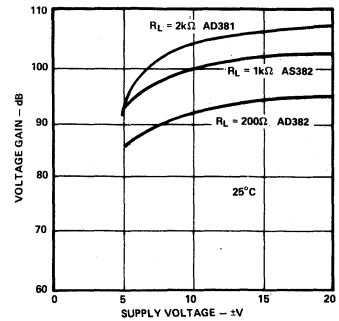


Figure 12. Open Loop Voltage Gain vs. Supply Voltage

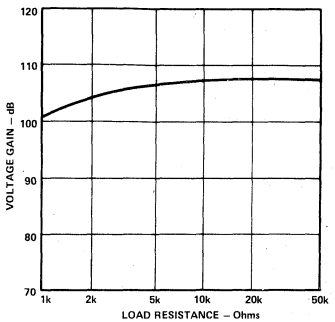


Figure 13a. Voltage Gain vs. Load Resistance for AD381

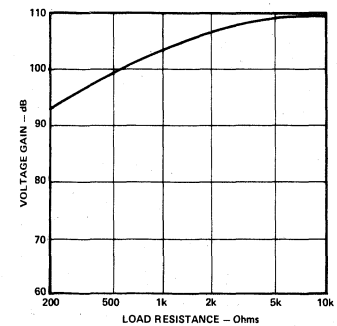


Figure 13b. Voltage Gain vs. Load Resistance for AD382

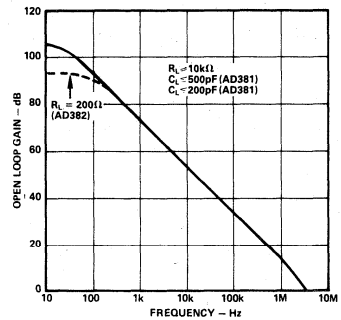


Figure 14. Open Loop Gain vs. Frequency

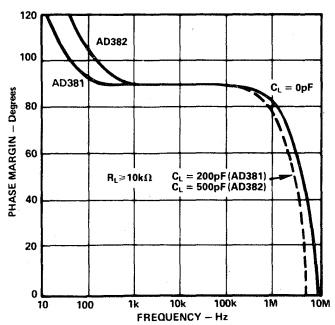


Figure 15. Phase Margin vs. Frequency

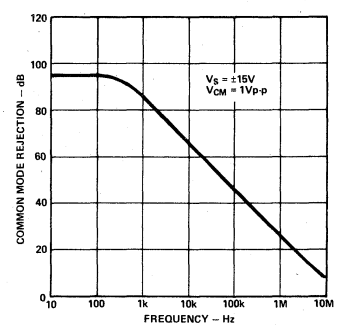


Figure 16. Common-Mode Rejection vs. Frequency

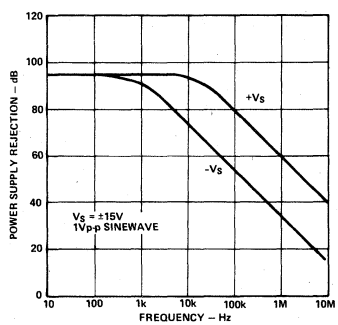


Figure 17. Power Supply Rejection vs. Frequency

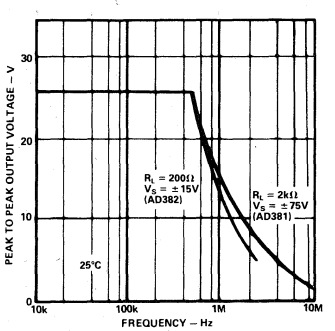


Figure 18. Large Signal Frequency Response

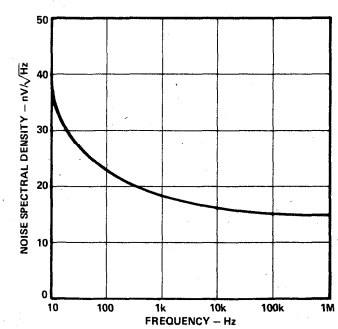


Figure 19. Noise vs. Frequency

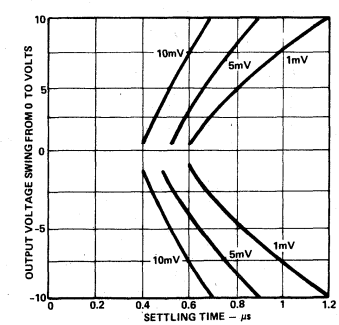


Figure 20a. AD381 Output Settling Time vs. Output Voltage Swing and Error (Circuit of Figure 22a)

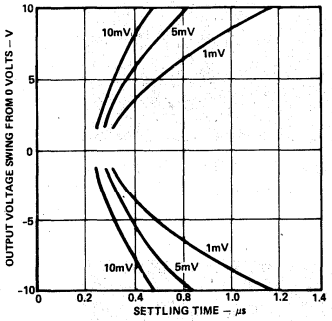


Figure 20b. AD382 Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

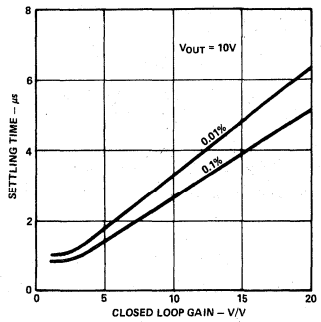


Figure 21. Settling Time vs. Closed Loop Gain (Circuits of Figures 22a & 23a)

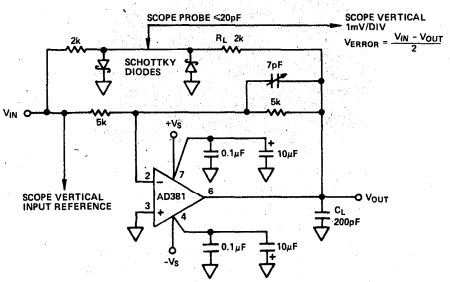


Figure 22a. AD381 Unity Gain Inverter and Settling Time Test Circuit

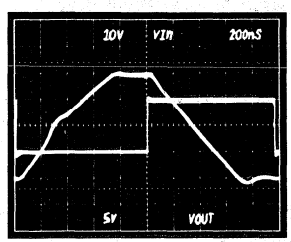


Figure 22b. AD381 Unity Gain Inverter Pulse Response (Large Signal)

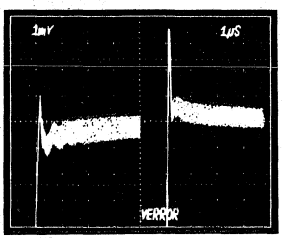


Figure 22c. AD381 Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

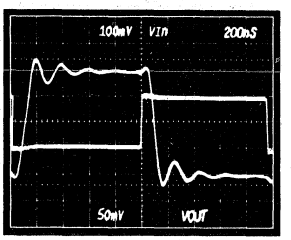


Figure 22d. AD381 Unity Gain Inverter Pulse Response (Small Signal)

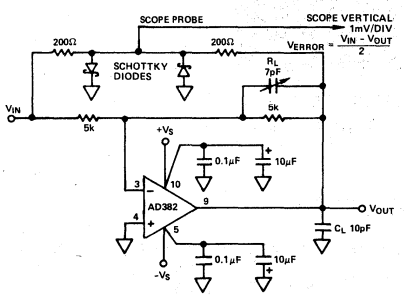


Figure 23a. AD382 Unity Gain and Settling Time Test Circuit

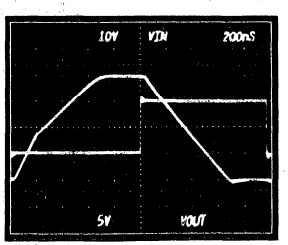


Figure 23b. AD382 Unity Gain Inverter Pulse Response (Large Signal)

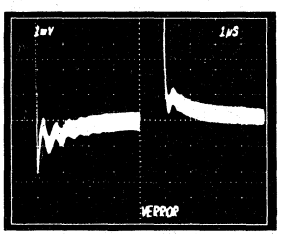


Figure 23c. Unity Gain Inverter Pulse Response (Large Signal Error Voltage)

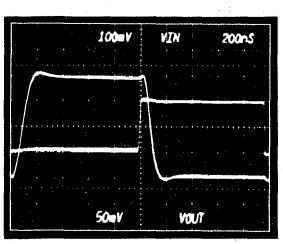


Figure 23d. AD382 Unity Gain Inverter Pulse Response (Small Signal)

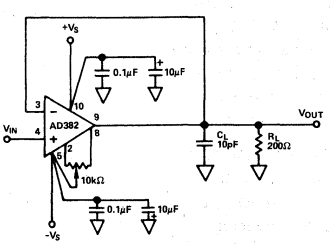


Figure 24a. AD382 Unity Gain Follower

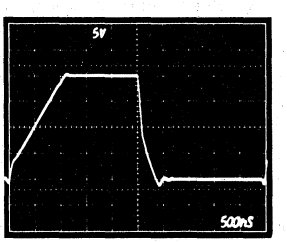


Figure 24b. AD382 Unity Gain Follower Pulse Response (Large Signal)

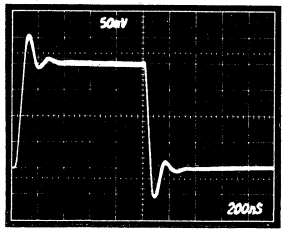


Figure 24c. AD382 Unity Gain Follower Pulse Response (Small Signal)

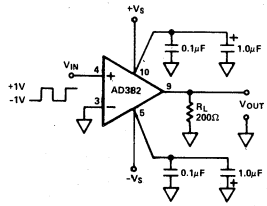


Figure 25a. AD382 Overdrive Recovery Test Circuit

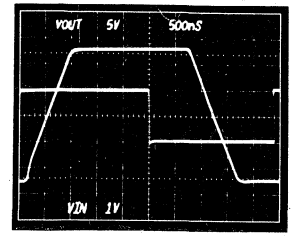


Figure 25b. AD382 Overdrive Recovery Response

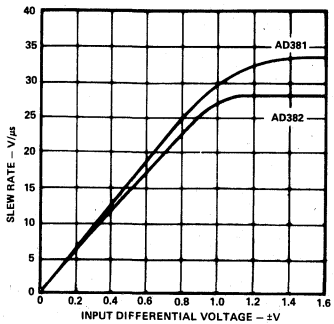


Figure 26. Slew Rate vs. Input Voltage

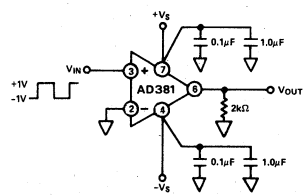


Figure 27a. AD381 Overdrive Recovery Test Circuit

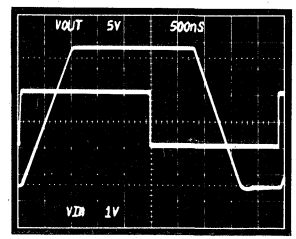


Figure 27b. AD381 Overdrive Recovery Response

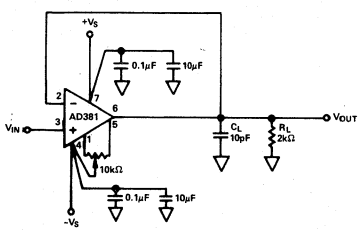


Figure 28a. AD381 Unity Gain Follower

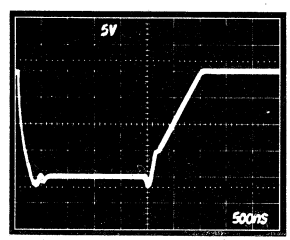


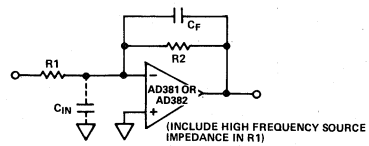
Figure 28b. AD381 Unity Gain Follower Large Signal Pulse Response

Compensation Capacitor

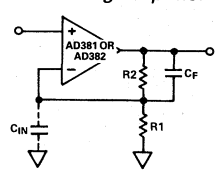
The AD381 and AD382 have sufficient phase margin to insure stability in most applications without compensation. However, in applications with capacitive load, very high speed, low gain or high resistor values ($R_{IN} \geq 5k\Omega$) the high frequency noise rejection will be improved by adding a compensation capacitor. The AD381 and AD382 have an input capacitance of 7pF. When soldered on a printed circuit board or inserted in a socket the total input capacitance could be 10pF. This input capacitance can lower the 0° phase margin crossover point from 8MHz, as shown in Figure 14, to around 1MHz.

By adding a small compensation capacitor in the feedback loop we can cancel the effects of the input capacitance and reduce high frequency noise gain. 5 to 10pF will suffice in most applications. In some current output, digital-to-analog converter applications the output capacitance of the DAC may be 200pF which would require a large compensation capacitor in the amplifier feedback loop.

A scheme for compensating inverting and noninverting circuits is shown in Figure 29. Choose $C_F = C_{IN} \frac{R1}{R2}$.



a. Inverting Amplifier



b. Noninverting Amplifier

Figure 29.

Offset Null

The AD381/AD382 should not have to be offset nulled for most applications because of its low initial offset voltage. If nulling is required for very high precision applications, such as an output amplifier for 13-bit or better digital-to-analog converters, connect a 10kΩ potentiometer between the offset null pins (pins 1 and 5 for the AD381 and pins 2 and 8 for the AD382). The wiper of the potentiometer is tied to the negative supply. With the analog input signal to the circuit grounded, adjust the potentiometer for zero output.

AD382 Heat Sinking

A heat sink for convection cooling is required if operating at full power and at ambient temperatures greater than 70°C. As shown in Figure 5 the free air power dissipation curve for the AD382 crosses the full power dissipation point (0.75W) at 70°C. The power dissipation can be improved by using a heat sink up to the case power dissipation curve (also referred to as the infinite heat sink power dissipation curve). We recommend connecting the heat sink to the AD382 case and keeping the combination ungrounded.

TYPICAL CIRCUITS

In many digital-to-analog converter applications, including automatic test equipment, the load may be large enough to require a buffer amplifier. The AD382 can supply ±10V into a 200Ω load. The AD381 can supply up to ±10V into a 1kΩ load.

The AD381 and AD382 are also well suited for CMOS DAC output amplifier applications due to their low initial offset voltage.

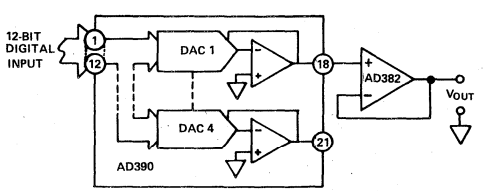


Figure 30. Buffer Amplifier to a 12-Bit Voltage Output DAC

No external trims are required with 12-bit CMOS DACs. Since the output impedance of CMOS DACs varies with input code, the output voltage could appear nonmonotonic if the offset voltage is greater than 1/2LSB. An LSB for a 12-bit DAC such as the AD7545 is 2.44mV (10 volts full scale/4096). Thus the AD381 and AD382, with only 1mV of offset maximum, assure monotonic performance without external trims.

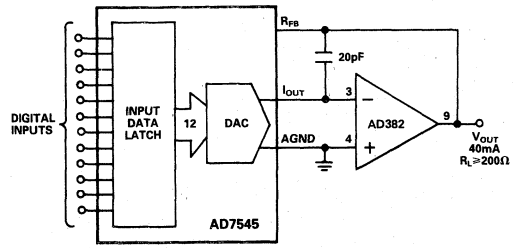
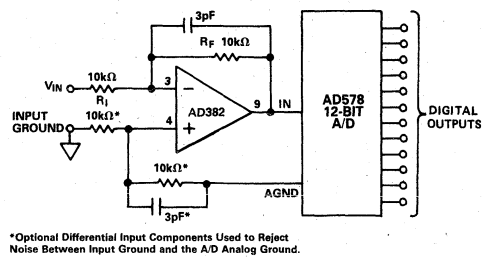


Figure 31. CMOS DAC Output Amplifier



*Optional Differential Input Components Used to Reject Noise Between Input Ground and the A/D Analog Ground.

Figure 32. Fast-Settling Buffer

Many high speed A/D converters require a wideband buffer that can hold a constant output voltage under dynamically-changing load conditions that fluctuate at the bit decision rate.

Its quick recovery from load variations makes the AD382 an excellent buffer for fast successive approximation A/D converters.

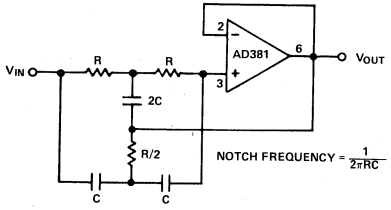


Figure 33. High Q Notch Filter

The above notch filter will have a notch of −55dB. To obtain a Q of 100 the capacitors should be well matched. Polystyrene, Teflon or NPO ceramic capacitors and metal-film resistors are recommended. For low frequency filter applications resistor values will be large. The AD381 is well suited for this application due to its low input bias current. It is also good for high frequency filtering because of its wide gain bandwidth product. This filter is capable of driving 1kΩ loads over a ±10V output range.

Figure 34 shows a fast sample and hold circuit that can acquire a sample to 0.01% in 2μs (20 volt swing). The AD381 is well suited for fast 12-bit sample/hold amplifier circuits. R1 and R2 set the circuit gain. R3 is adjusted for minimum ac feedthrough. Potentiometer R4 is set for minimum sample/hold offset voltage. R6 improves the settling time and circuit stability by adding phase margin. Bias resistors R7 and R8 insure complete shut-off of the D-MOS FET switches at TTL logic zero. Pull up resistors R9 and R10 lower the on resistance of the D-MOS switches. The SD5000 D-MOS switch is recommended for its fast transition speed and low on resistance.

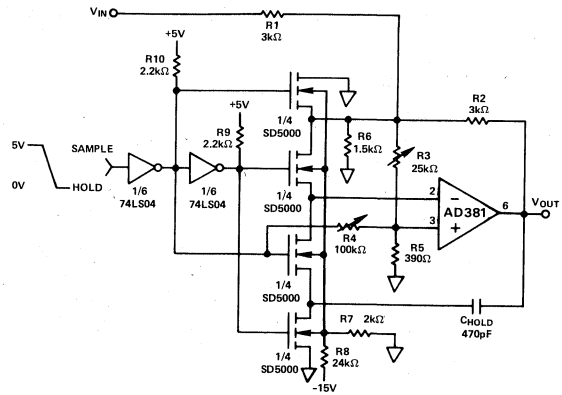


Figure 34. Fast Sample/Hold Amplifier

ANALOG DEVICES

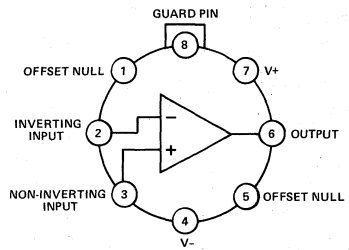
High Accuracy Low Offset IC FET-Input Op Amps

AD503, AD506

FEATURES

Low I_b: 15pA max (AD503J, AD506J)
5pA max (AD506L)
Low V_{OS}: 1mV max (AD506L)
Low Drift: 25μV/°C max (AD503K, AD506K)
10μV/°C max (AD506L)

AD503, AD506 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD503J/AD506J, AD503K/AD506K, AD506L and AD503S/AD506S are IC FET input op amps that provide the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The devices achieve maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. They are free from latch-up and are short circuit protected. No external compensation is required as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance. The AD506, with specifications otherwise similar to the AD503, offers significant improvement in offset voltage and nulled offset voltage drift by supplementing the AD503 configuration with internal laser trimming of thin film resistors to provide typical offset voltages below 1mV.

The AD503 and AD506 are especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503 and AD506 IC FET input amplifiers, therefore, are of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

All the circuits are supplied in the TO-99 package; the AD503J, K and AD506J, K and L are specified for 0 to +70°C temperature range operation; the AD503S and AD506S for operation from -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD503 and AD506 op amps meet their published input bias current and offset voltage specs after full warmup. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD503 and AD506 are specified as a maximum for *either* input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Offset voltage nulling of the AD503 and AD506 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±0.8μV/°C per millivolt of nulled offset for the AD506 and ±2.0μV/°C per millivolt of nulled offset for the AD503, compared to several times this for other IC FET op amps.
4. The gain of the AD503 and AD506 is measured with the offset voltage nulled. Nulling a FET input op amp can cause the gain to decrease below its specified limit. The gain of the AD503 and AD506 is fully guaranteed with the offset voltage both nulled and unnulled.
5. Bootstrapping of the input FET's achieves a superior CMRR of 80dB, while reducing bias currents and maintaining them constant through the CMV range.

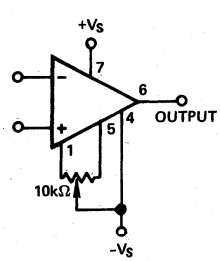
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs. Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV/°C max (20μV/°C typ)
vs. Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	$10^{11}\,\Omega \| 2pF$	*	*
Common Mode	$10^{12}\,\Omega \| 2pF$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	$30.0nV/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*
PACKAGE OPTIONS:[6] TO-99 Style (H08B)	AD503JH	AD503KH	AD503SH

NOTES
[1] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2] A conservative design would not exceed 500pF of load capacitance.
[3] Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5] See comments in Input Considerations Section.
[6] See Section 19 for package outline information.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

AD506J	AD506K	AD506L	AD506S
*	**	75,000 min (100,000 typ)	**
*	**	50,000 min	25,000 min
*	*	*	*
*	*	*	*
1000pF	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
3.5mV max (1.0mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.4mV typ)	1.5mV max (0.5mV typ)
*	**	10μV/°C max (5μV/°C typ)	50μV/°C max (20μV/°C typ)
**	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)	100μV/V max (50μV/V typ)
*	**	5pA max (2pA typ)	**
*	*	*	*
*	*	*	*
40μV (p-p)	*	*	*
8μV (rms)	*	6μV (rms)	*
80nV/√Hz	*	25nV/√Hz	*
±4V	*	*	*
*	*	*	*
*	**	**	**
*	*	*	*
*	*	*	±(5 to 22)V
7mA max (5mA typ)	*	*	*
*	*	*	-55°C to +125°C
*	*	*	*
AD506JH	AD506KH	AD506LH	AD506SH



Standard Offset Null Circuit

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 and AD506 specify maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced in the AD503 and AD506 by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

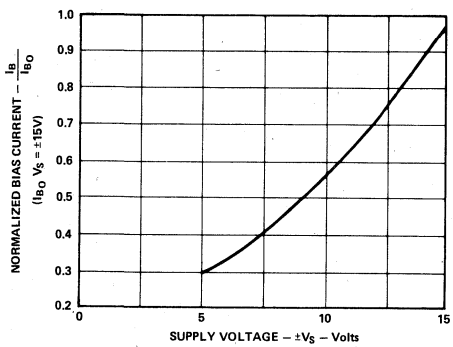


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD503K and AD506K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

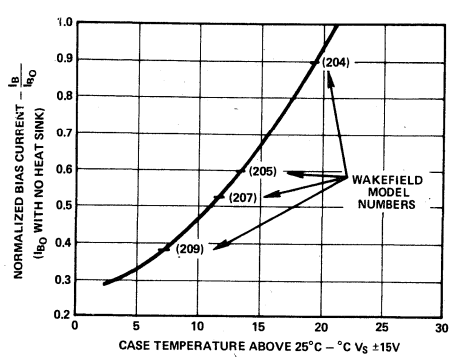


Figure 2. Normalized Bias Current vs. Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503/AD506K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

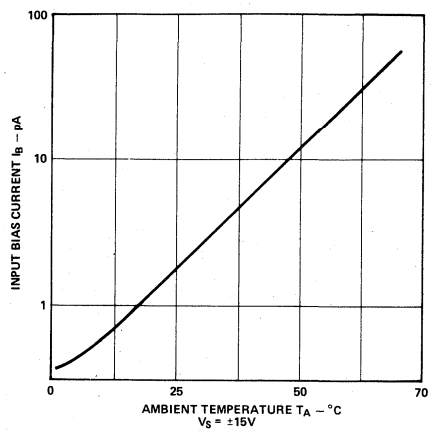


Figure 3. Input Bias Current vs. Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 volts and negative common mode inputs to $-V_S$ are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed $V_{CM} = V_S$.

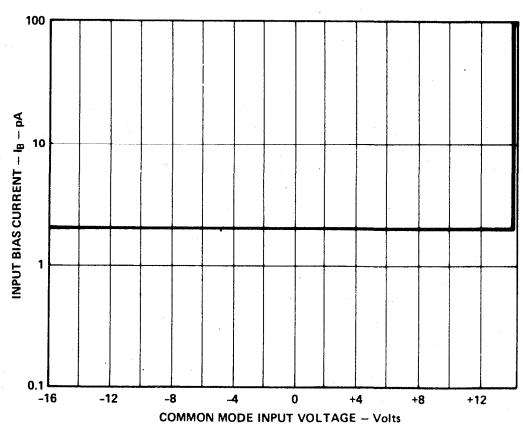


Figure 4. Input Bias Current vs. Common Mode Voltage

Like most other FET input op amps, the AD503 and AD506 display a degraded bias current specification when operated at moderate differential input voltages. The AD503 maintains its specified bias current up to a differential input voltage of ±3V typically, while the AD506's bias current performance is not significantly degraded for $V_{diff} \leqslant 4V$ typically. Above V_{diff} = ±3V in the AD503 and V_{diff} = ±4V in the AD506, the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.

ANALOG DEVICES

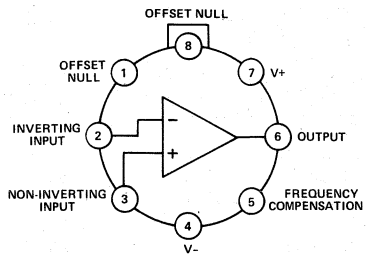
High Accuracy IC Operational Amplifier

AD504

FEATURES

Low V_{OS}: 500μV max (AD504M)
High Gain: 10^6 min (AD504L, M, S)
Low Drift: 0.5μV/°C max (AD504M)
Free of Popcorn Noise

AD504 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD504J, K, L, M and S IC operational amplifiers provide ultra-low drift and extremely high gain, comparable to that of modular amplifiers, for precision applications. A new double integrator circuit concept combined with a precise thermally balanced layout achieves gain greater than 10^6, offset voltage drift of less than 1μV/°C, small signal unity gain bandwidth of 300kHz, and slew rate of 0.12V/μs. Because of monolithic construction, the cost of the AD504 is significantly below that of modules, and becomes even lower with larger quantity requirements. The amplifier is externally compensated for unity gain with a single 470pF capacitor; no compensation is required for gains above 500. The inputs are fully protected, which permits differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits to ground and/or either supply voltage, and is capable of driving 1000pF of load capacitance. The AD504J, K, L and M are supplied in the hermetically sealed TO-99 package, and are specified for operation over the 0 to +70°C temperature range. The AD504S is specified over the -55°C to +125°C temperature range and is also supplied in the TO-99 package.

PRODUCT HIGHLIGHTS

1. Fully guaranteed and 100% tested 1μV/°C maximum voltage drift combined with voltage offset of 500μV (AD504L).
2. Fully protected input ($\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, and is of critical importance in this type of device whose overall performance is strongly dependent upon front-end stability.
3. Single capacitor compensation eliminates elaborate stabilizing networks while providing flexibility not possible with an internally compensated op amp. This feature allows bandwidth to be optimized by the user for his particular application.
4. High gain is maintained independent of offset nulling, power supply voltage and load resistance.
5. Bootstrapping of the critical input transistor quad produces CMRR and PSRR compatible with the tight 1μV/°C drift. CMRR and PSRR are both in the vicinity of 120dB.
6. Noise performance is closely monitored at Outgoing QC to ensure compatibility with the low error budgets afforded by the performance of all other parameters.
7. Every AD504 receives a stabilization bake for 24 hours at 150°C to ensure reliability and long term stability.
8. The 100 piece price of the AD504 is 1/3 to 1/2 less than that of modular low drift operational amplifiers, and is competitive with the price of less accurate IC op amps.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

PARAMETER	AD504J	AD504K	AD504L
OPEN LOOP GAIN			
V_{OS} = ±10V, $R_L \geq 2k\Omega$	250,000 min (4 x 10^6 typ)	500,000 min (4 x 10^6 typ)	10^6 min (8 x 10^6 typ)
$T_{min} \leq T_A \leq T_{max}$	125,000 min (10^6 typ)	250,000 min (10^6 typ)	500,000 min (10^6 typ)
OUTPUT CHARACTERISTICS			
Voltage at $R_L \geq 2k\Omega$, $T_{min} \leq T_A \leq T_{max}$	±10V min (±13V typ)	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal, C_c = 390pF	300kHz	*	*
Full Power Response, C_c = 390pF	1.5kHz	*	*
Slew Rate, Unity Gain, C_c = 390pF	0.12V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k$	2.5mV max (0.5mV typ)	1.5mV max (0.5mV typ)	0.5mV max (0.2mV typ)
vs Temp, $T_{min} \leq T_A \leq T_{max}$, V_{OS} nulled	5.0μV/°C max (0.5μV/°C typ)	3.0μV/°C max (0.5μV/°C typ)	1.0μV/°C max (0.3μV/°C typ)
$T_{min} \leq T_A \leq T_{max}$, V_{OS} unnulled†	10μV/°C max (1.5μV/°C typ)	5.0μV/°C max (1.5μV/°C typ)	2.0μV/°C max (1.0μV/°C typ)
vs Supply	25μV/V max	15μV/V max	10μV/V max
@ $T_{min} \leq T_A \leq T_{max}$	40μV/V	25μV/V max	15μV/V max
vs Time	20μV/mo	15μV/mo	10μV/mo
INPUT OFFSET CURRENT			
@ T_A = 25°C	40nA max	15nA max	10nA max
INPUT BIAS CURRENT			
Initial	200nA max	100nA max	80nA max
T_{min} to T_{max}	300nA max	150nA max	100nA max
vs Temp, T_{min} to T_{max}	300pA/°C	250pA/°C	200pA/°C
INPUT IMPEDANCE			
Differential	0.5MΩ	1.0MΩ	1.3MΩ
Common Mode	100MΩ‖4pF	*	*
INPUT NOISE			
Voltage, 0.1 to 10Hz	1.0μV (p-p)	*	*
100Hz	10nV/√Hz(rms)	*	*
1kHz	8nV/√Hz(rms)	*	*
Current, 0.1 to 10Hz	50pA(p-p)	*	*
100Hz	0.6pA/√Hz(rms)	*	*
1kHz	0.5pA/√Hz(rms)	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, Max Safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min (120dB typ)	100dB min (120dB typ)	110dB min (120dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Current, Quiescent	±4.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)	±3.0mA max (±1.5mA typ)
TEMPERATURE RANGE			
Operating, Rated Performance (T_{min} to T_{max})	0 to +70°C	*	*
Storage	−65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08B)	AD504JH	AD504KH	AD504LH

NOTES
*Specifications same as for AD504J.
[1] See Section 19 for package outline information.

Specifications subject to change without notice.

NOTE
Analog Devices 100% tests and guarantees all specified maximum and minimum limits. Certain parameters, because of the relative difficulty and cost of 100% testing, have been specified as "typical" numbers. At ADI, "typical" numbers are subjected to rigid statistical sampling and outgoing quality control procedures, resulting in "typicals" that are indicative of the performance that can be expected by the user.

AD504M	AD504S(AD504S/883)
10^6 min (8 x 10^6 typ) 500,000 min (10^6 typ)	10^6 min (8 x 10^6 typ) 250,000 min
* * * *	* * * *
* * *	* * *
0.5mV max (0.2mV typ) 0.5μV/°C max (0.2μV/°C typ) 1.0μV/°C max (0.5μV/°C typ) 10μV/V max 15μV/V max 10μV/mo	0.5mV max 1.0μV/°C max (0.3μV/°C typ) 2.0μV/°C max (1.0μV/°C typ) 10μV/V max 20μV/V max 10μV/mo
10nA max	10nA max
80nA max 100nA max 200pA/°C	80nA max 200nA max 200pA/°C
1.3MΩ *	1.3MΩ *
0.6μV (p-p) max 10nV/$\sqrt{Hz}$ max 9nV/$\sqrt{Hz}$ max 50pA p-p max 0.6pA/$\sqrt{Hz}$ max 0.3pA/$\sqrt{Hz}$ max	* * * * * *
* 110dB min (120dB typ)	* 110dB min (120dB typ)
* * ±3.0mA max (±1.5mA typ)	* * ±3mA max (±1.5mA typ)
* *	-55°C to +125°C -65°C to +150°C
AD504MH	AD504SH

OFFSET VOLTAGE DRIFT AND NULLING

Most differential operational amplifiers have provisions for adjusting the initial offset voltage to zero with an external trim potentiometer. It is often not realized that there is a resulting increase in voltage drift which accompanies this initial offset adjustment. The increased voltage drift can often be safely ignored in conventional amplifiers, since it may be a small percentage of the specified voltage drift. However, the voltage drift of the AD504 is so small that this effect cannot be ignored.

To achieve low drift over temperature, it is necessary to maintain equal current densities in the input pair. Unless the initial offset nulling circuit is carefully arranged, the nulling circuits will themselves drift with temperature. The resulting change in the input transistor current *ratio* will produce an additional input offset voltage drift. This drift component can actually be larger than the unnulled drift.

Typically, IC op amps are nulled by using an external potentiometer to adjust the ratio of two resistances. These resistances are part of a network from which the input stage emitter currents are derived. Most commercially available op amps use diffused resistors in their internal nulling circuitry, which typically display large positive temperature coefficients of the order of 2000ppm/°C. As a result of the failure of the external potentiometer resistance to track the diffused resistors over temperature, the two resistance branches will drift relative to one another. This will cause a change in the emitter current ratio and induce an offset drift with temperature.

In the AD504, this problem is reduced an order of magnitude by the use of thin film resistors deposited on the monolithic amplifier chip. These resistors, which make up the critical bias network from which the input stage emitter current balance is determined, display typical temperature coefficients of less than 200ppm/°C, an order of magnitude improvement over diffused types. Thus, when the initial offset of the AD504 is trimmed using a low TC pot in combination with the thin film network, the drift induced by nulling even relatively large offsets is extremely small. This means that AD504 units of all three grades (J, K, L) will typically yield significantly better temperature performance in nulled applications than an all-diffused amplifier with comparable initial offset.

Since the intrinsic offset drift of the amplifier is improved by nulling, the direct measurement of any additional drift induced by differing temperature coefficients of resistors would be extremely difficult. However, the *induced* offset drift can be established by calculating the change in the emitter current ratio brought about by the differing TC's of resistances. From the change in this ratio, the offset voltage contribution at any temperature can be easily calculated.

A simple computer program was written to calculate induced offset drift as a function of initial offset voltage nulled. This calculation was made assuming zero TC of the amplifier resistors, and TC's of 200ppm/°C and 2000ppm/°C for the null pot. These results are very nearly equivalent to the case where the pot has zero temperature coefficient and the amplifier resistors drift. The results of these calculations are summarized graphically in Figure 1.

Figure 1 shows the variation of induced voltage drift with nulled offset voltage for:

a. AD504 op amp.
b. 725 typ op amp.

Note that as a result of nulling 1.4mV of offset, *the AD504 induces 30X less offset drift (only 0.05μV/°C) than the 725 type op amp* with its actual diffused resistor values and the recommended 100k pot to trim the offset. Actual induced drifts from this source for the AD504 may be even lower in the practical case when metal film resistors or pots are used for nulling, since their TC's tend to closely *match* the negative TC's of the thin film resistors on the AD504 chip.

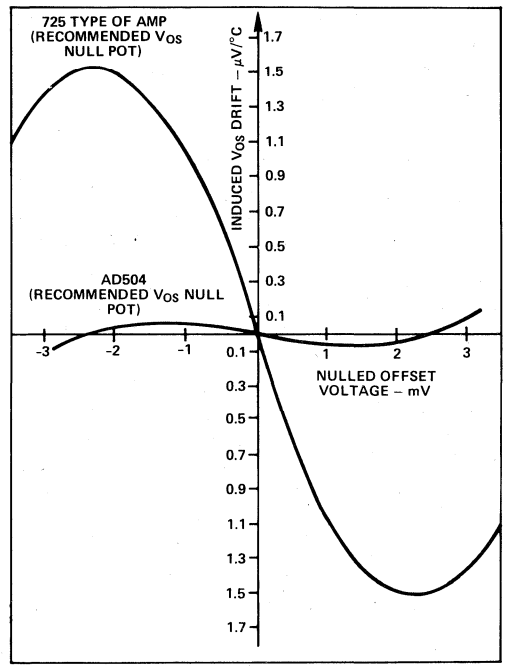


Figure 1. Induced Offset Drift vs. Nulled Offset Using Manufacturer's Recommended Adjustment Potentiometer

NULLING THE AD504

Since calculations show that superior drift performance can be realized with the AD504, special care should be taken to null it in the most advantageous manner. Using the actual values of resistors in the AD504, it is possible to calculate, under worst case conditions, that the total adjustment range of the AD504 is approximately 8mV. Since the amplifier may often be trimmed to within 1μV, this represents an adjustment of 1 part in 8000. This type of accuracy would require a pot with 0.0125% resolution and stability. Because of the problems of obtaining a pot of this stability, a slightly more sophisticated nulling operation is recommended for applications where offset drift is critical (see Figure 2a).

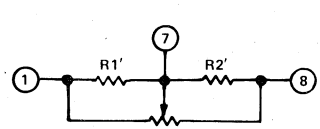


Figure 2a. High Resolution, High Stability Nulling Circuit

NULLING PROCEDURE

1. Null the offset to zero using a commercially available pot (suggest R_P = 10kΩ).
2. Measure pot halves R1 and R2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1},\ R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Insert R1′ and R2′ (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (R_P) to fine tune the trim.

For applications in which stringent nulling is not required, the user may choose a simplified nulling scheme as shown in Figure 2b. For best results the wiper of the potentiometer should be connected directly to pin 7 of the op amp. This is true for both nulling schemes.

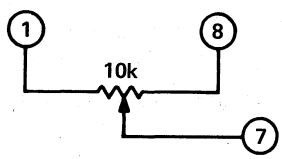


Figure 2b. Simplified Nulling Circuit

INPUT BIAS CURRENT

The input bias current vs. temperature characteristic is displayed in Figure 3.

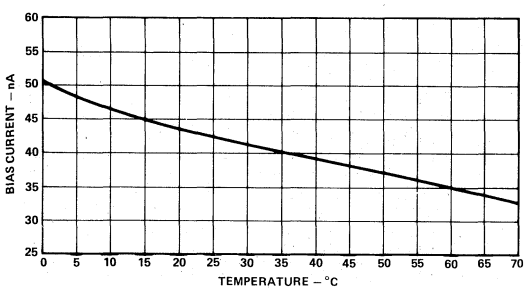


Figure 3. Input Bias Current vs. Temperature

GAIN PERFORMANCE

Most commercially available monolithic op amps have gain characteristics that vary considerably with:

1. Offset Nulling.
2. Load Resistance.
3. Supply Voltage.

Careful design allows the AD504 to maintain gain well in excess of 10^6, independent of nulling, load or supply voltage.

Nulling – The gain of a 741 op amp varies considerably with nulling (see Figure 4).

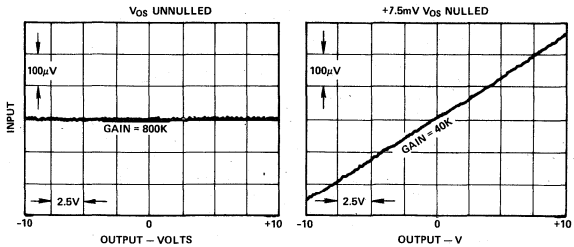


Figure 4. Gain Error Voltage Before and After Nulling a Typical 741 Op Amp

The gain of the AD504 is independent of nulling.

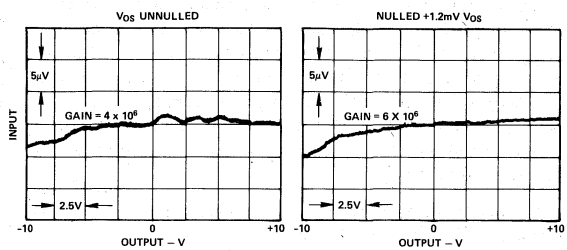


Figure 5. Gain Error Voltage Before and After Nulling the AD504

Load Resistance – The gain of the AD504 is flat with load resistance to 1kΩ loads and below.

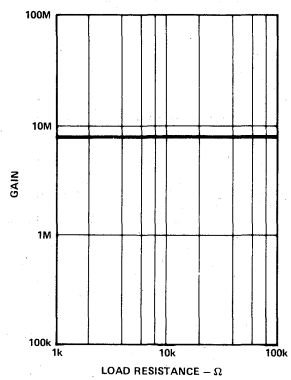


Figure 6. Gain vs. Load Resistance

Supply Voltage – The gain of the AD504 stays well above 1M down to V_S = ±5V.

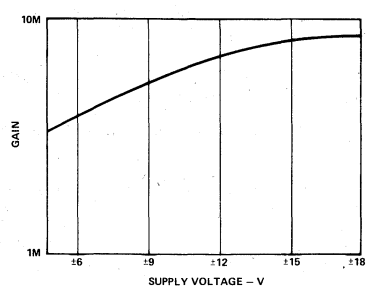


Figure 7. Gain vs. Supply Voltage

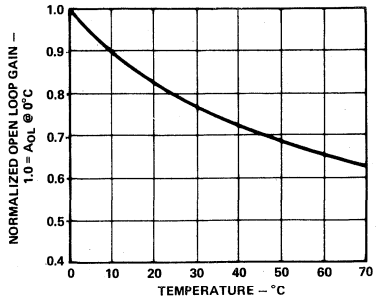


Figure 8. Normalized Open Loop Gain vs. Temperature

NOISE CHARACTERISTICS

An op amp with the precision of the AD504 must have correspondingly low noise levels if the user is to take advantage of its exceptional dc characteristics. Of primary importance in this type of amplifier is the absence of popcorn noise and minimum I/f or "flicker" noise in the 0.01Hz to 10Hz frequency band. Sample noise testing is done on every lot to guarantee that better than 90% of all devices will meet the noise specifications.

Separate voltage and current noise levels referred to the input are specified to enable the designer to calculate or optimize signal-to-noise ratio based on any desired source resistance. The spot noise figures are useful in determining total wideband noise over any desired bandwidth (see Figure 9).

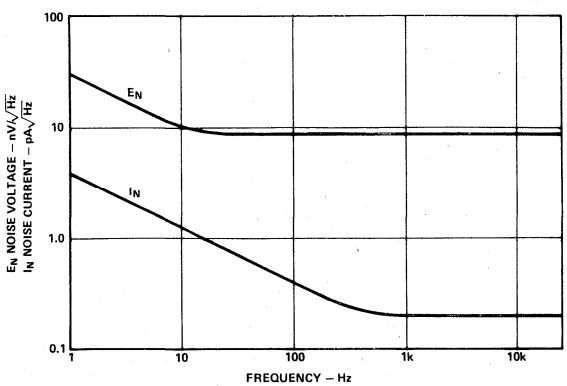


Figure 9. Spot Noise vs. Frequency

The key to success in using the AD504 in precision low noise applications is "attention to detail".

Here are a few reminders to help the user achieve optimum noise performance from the AD504.

1. Use metal film resistors in the source and feedback networks.
2. Use fixed resistors instead of potentiometers for nulling or gain setting.
3. Take advantage of the excellent common-mode noise rejection qualities of the AD504 by connecting the input differentially.
4. Limit the bandwidth of the system to the minimum possible consistent with the desired response time.
5. Use input guarding to reduce capacitive and leakage noise pickup.
6. Avoid ground loops and proximity to strong magnetic or electrostatic fields, etc.

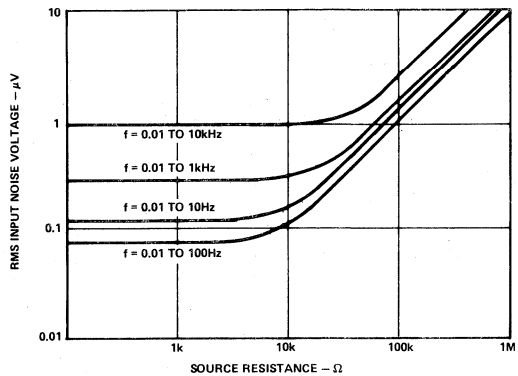


Figure 10. RMS Noise vs. Source Resistance

DYNAMIC PERFORMANCE

The dynamic performance of the AD504, although comparable to most general purpose op amps, is superior to most low drift op amps. Figure 11 shows the small signal frequency response for both open and closed loop gains for a variety of compensating values. Note that the circuit is completely stable for C_C = 390pF with a -3dB bandwidth of 300kHz; with C_C = 0, the -3dB bandwidth is 50kHz at a gain of 2000.

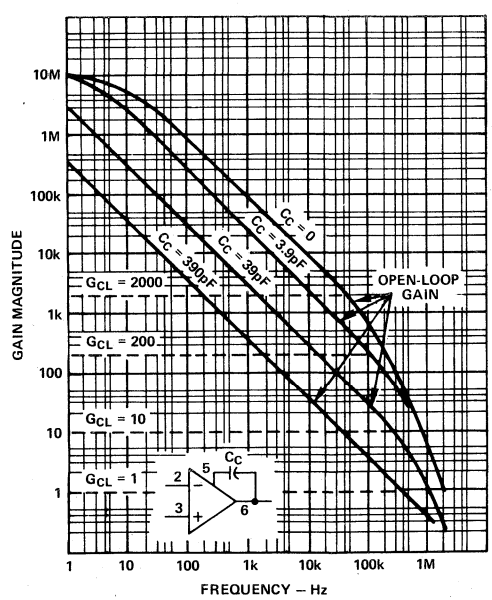


Figure 11. Small Signal Gain vs. Frequency

More important, at unity gain (390pF), full power bandwidth is (Figure 12) 2kHz which corresponds to a 0.12V/μs slew rate. At a gain of 10 (39pF), it increases to 20kHz, corresponding to 1.2V/μs, a considerable improvement over "725 type" amplifiers.

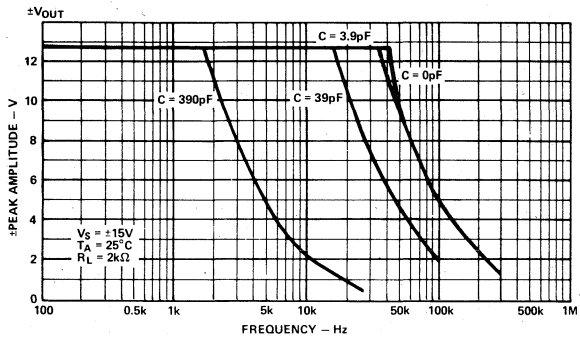


Figure 12. Output Voltage Swing vs. Frequency

Figure 13 shows the voltage follower step response for $V_S = \pm 15V$, $R_L = 2k\Omega$, $C_L = 200pF$ and $C_C = 390pF$.

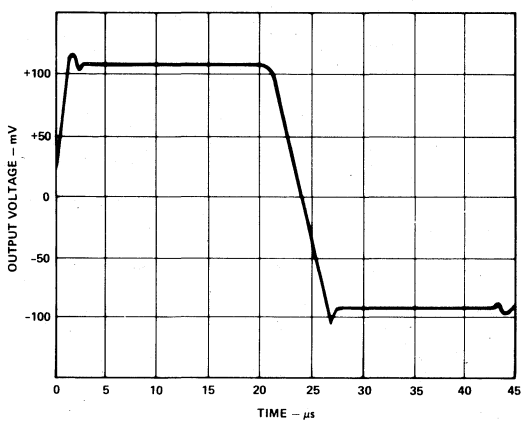


Figure 13. Voltage Follower Step Response

The common mode rejection of the AD504 is typically 120dB, and is shown as a function of frequency in Figure 14.

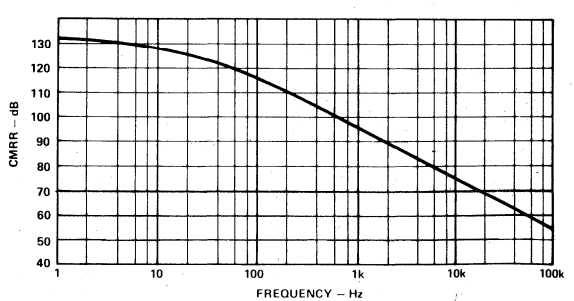


Figure 14. CMRR vs. Frequency

The power supply rejection ratio of the AD504 is shown in Figure 15.

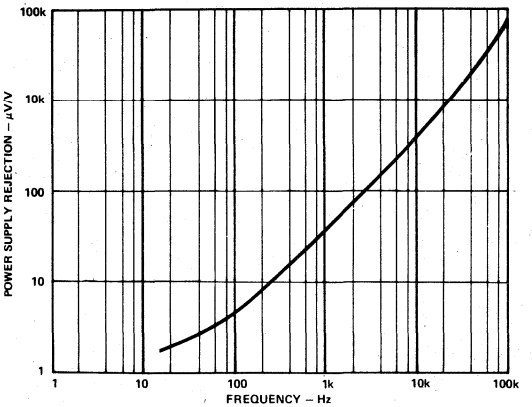


Figure 15. PSRR vs. Frequency

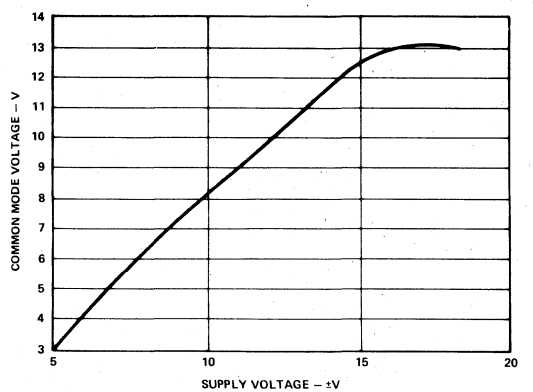


Figure 16. CMV Range vs. Supply Voltage

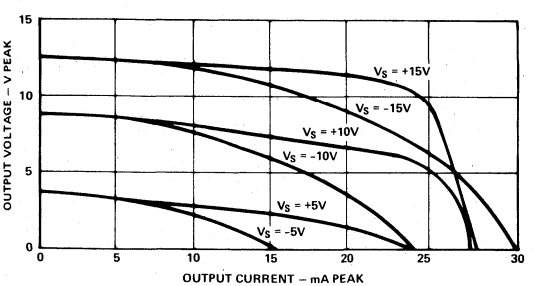


Figure 17. Output Characteristics

THERMAL PERFORMANCE

Temperature Gradients

Most modular and hybrid operational amplifiers are extremely sensitive to thermal gradients. The transient offset voltage response to thermal shock for a high performance modular op amp is shown in Figure 18.

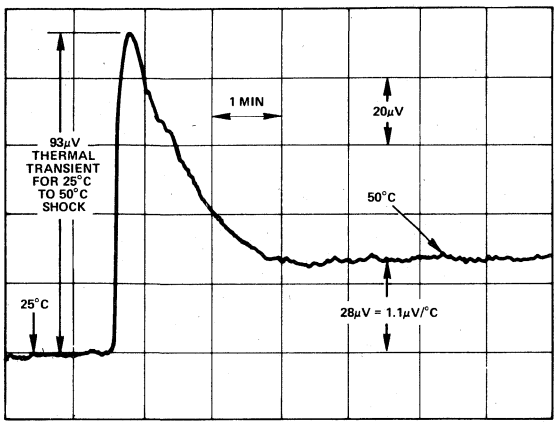


Figure 18. Response to Thermal Shock for High Performance Modular Op Amp

The graph shows the transient offset voltage resulting from a thermal shock when the amplifier's temperature is abruptly changed from 25°C to 50°C by dipping it into a hot silicon oil bath. Note the large overshoot (approximately 60μV) and long settling time (2.5 minutes). Also note the hysteresis of about 30μV.

Monolithic technology affords the AD504 significant improvements in this area. Thermal transients in the AD504 are small and over with quickly (see Figure 19).

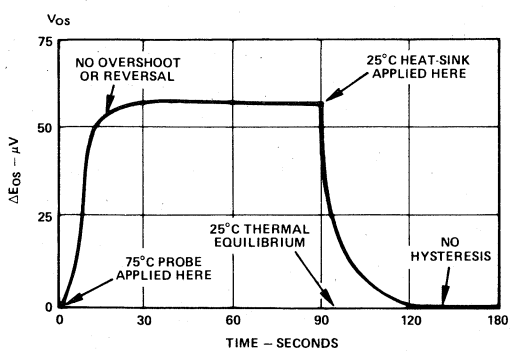


Figure 19. Response to Thermal Shock for AD504

In Figure 19, a 50°C step change in ambient temperature, applied to the can via a room temperature heat sink, then a 75°C thermal probe and back to the heat sink, results in settling to the final value within 30 seconds, for both increases and decreases in temperature. Note that the offset goes directly to its final value, with no spikes or hysteresis.

Warmup Drift

Modular and hybrid op amps have historically been plagued by excessive thermal time constants. Figure 20 shows the typical warmup drift of a high performance modular op amp.

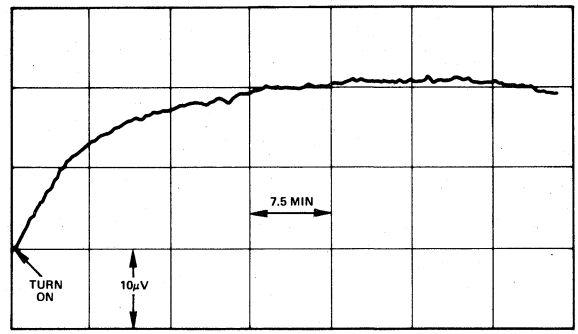


Figure 20. Warmup Voltage Drift for High Performance Modular Op Amp

Note that although warmup drift is low (20μV), it requires a long time to settle (>20 minutes).

Monolithic technology results in significant reduction of thermal time constants (see Figure 21).

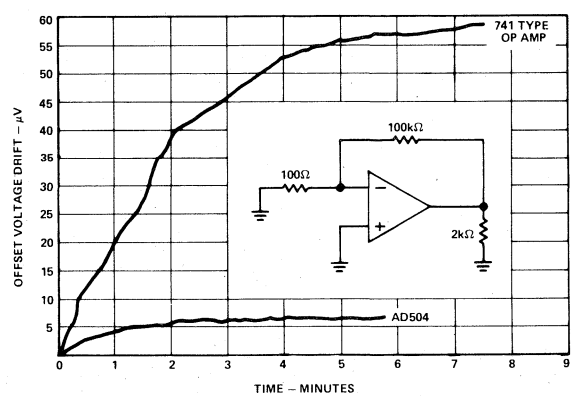


Figure 21. Warmup Voltage Drift for AD504 and 741 Type Op Amp

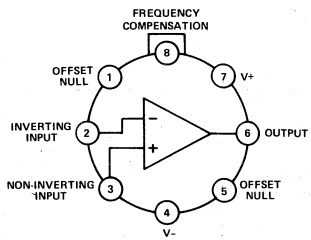
Note that warmup drift remains low (10μV), but that the thermal time constant decreases significantly to about 2 minutes. If a heat sink were used, total settling time would be completed within 30 seconds. Note that the 741 type op amp has a significantly longer warmup drift and thermal time constant.

IC, Wideband, Fast Slewing, General Purpose Operational Amplifier

AD507

FEATURES
Gain Bandwidth: 100MHz
Slew Rate: 20V/μs min
I_B: 15nA max (AD507K)
V_{os}: 3mV max (AD507K)
V_{os} Drift: 15μV/°C max (AD507K)
High Capacitive Drive

AD507 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The Analog Devices AD507J, K and S are low cost monolithic operational amplifiers that are designed for general purpose applications where high gain bandwidth and high speed are significant requirements. The devices also provide excellent dc performance with low input offset voltage, low offset voltage drift and low bias current. The AD507 is a low cost, high performance alternative to a wide variety of modular and IC op amps; a brief review of the specifications confirms its outstanding price/performance characteristics.

The AD507 is recommended for use where low cost and all around performance, especially at high frequencies, are needed. It is particularly well suited as a fast, high impedance comparator, integrator or wideband amplifier and in sample/hold circuits. It is unconditionally stable for all closed loop gains above 10 without external compensation; the frequency compensation terminal is used for stability at lower closed loop gains. The circuit is short circuit protected and offset voltage nullable. The AD507J and K are specified over the 0 to +70°C temperature range, the AD507S over the extended temperature range, −55°C to +125°C. All devices are packaged in the hermetic TO-99 metal can.

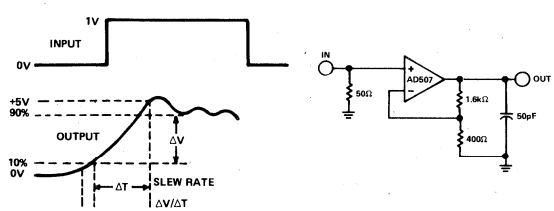
PRODUCT HIGHLIGHTS

1. Excellent dc and ac performance combined with low cost.
2. The AD507 will drive several hundred pF of output capacitance without oscillation.
3. All guaranteed dc parameters, including offset voltage drift, are 100% tested.
4. To insure compliance with gain bandwidth and slew rate specifications, all devices are tested for ac performance characteristics.

SPECIFICATIONS (typical at +25°C and ±15V dc, unless otherwise noted)

PARAMETER	AD507J	AD507K	AD507S
OPEN LOOP GAIN			
R_L = 2kΩ, C_L = 50pF	80,000 min (150,000 typ)	100,000 min (150,000 typ)	100,000 min (150,000 typ)
@ T min to T max	70,000 min	85,000 min	70,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, C_L = 50pF, T_{min} to T_{max}	±10V min (±12V typ)	*	±10V min (±12V typ)
Current @ V_o = ±10V	±10mA min (±20mA typ)	*	±15mA min (±22mA typ)
Short Circuit Current	25mA	*	25mA
FREQUENCY RESPONSE			
Unity Gain, Small Signal			
@ A = 1 (open loop)	35MHz	*	*
@ A = 100 (closed loop)	1MHz	*	*
Full Power Response	320kHz min (600kHz typ)	400kHz min (600kHz typ)	400kHz min (600kHz typ)
Slew Rate	±20V/μs min (±35V/μs typ)	±25V/μs min (±35V/μs typ)	20V/μs min (±35V/μs typ)
Settling Time (to 0.1%)	900ns	*	*
INPUT OFFSET VOLTAGE			
Initial	5.0mV max (3.0mV typ)	3.0mV max (1.5mV typ)	4mV max (0.5mV typ)
Avg vs Temp, T_{min} to T_{max}	15μV/°C	15μV/°C max (8μV/°C typ)	20μV/°C max (8μV/°C typ)
vs Supply, T_{min} to T_{max}	200μV/V max	100μV/V max	100μV/V max
INPUT BIAS CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
INPUT OFFSET CURRENT			
Initial	25nA max	15nA max	15nA max
T_{min} to T_{max}	40nA max	25nA max	35nA max
Avg vs Temp, T_{min} to T_{max}	0.5nA/°C	0.2nA/°C	0.2nA/°C
INPUT IMPEDANCE			
Differential	40MΩ min (300MΩ typ)	*	65MΩ min (500MΩ typ)
Common Mode	1000MΩ	*	*
INPUT VOLTAGE NOISE			
f = 10Hz	100nV/√Hz	*	*
f = 100Hz	30nV/√Hz	*	*
f = 100kHz	12nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential, Max Safe	±12.0V	*	*
Common Mode Voltage Range, T_{min} to T_{max}	±11.0V	*	*
Common Mode Rejection @ ±5V, T_{min} to T_{max}	74dB min (100dB typ)	80dB min (100dB typ)	80dB min (100dB typ)
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	4.0mA max (3.0mA typ)	*	*
TEMPERATURE RANGE			
Rated Performance	0 to +70°C	*	−55°C to +125°C
Operating	−25°C to +85°C	*	−65°C to +150°C
Storage	−65°C to +150°C	*	*
PACKAGE OPTION:[1] TO-99 Style (H08A)	AD507JH	AD507KH	AD507SH

NOTES
*Specifications same as AD507J.
[1] See Section 19 for package outline information.
Specifications subject to change without notice.



Slew Rate Definition and Test Circuit

APPLICATION CONSIDERATIONS

The AD507 combines excellent dc characteristics and dynamic performance with ease of application. Because it is a wideband, high speed amplifier, care should be exercised in its stabilization. Several practical stabilization techniques are suggested to insure proper operation and minimize user experimentation.

GENERAL PURPOSE WIDEBAND COMPENSATION

The following considerations are intended to provide guidance in critical wideband applications. While not necessary in all cases, the considerations are of prime importance for the user attempting to obtain the highest performance from his circuit design.

High Gain Conditions

The AD507 is fully compensated *internally* for all closed loop gains above 10; however, it is necessary to load the amplifier with 50pF. In many applications this minimum capacitive load will be provided by the load or by a cable at the output of the AD507, making an additional 50pF unnecessary. Figure 1 shows the suggested configuration for general purpose use for closed loop gains above 10.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD507 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V- 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagrams show each individual capacitor directly connected to the appropriate terminal (pin 7 [V+] and pin 6 [Output]). In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

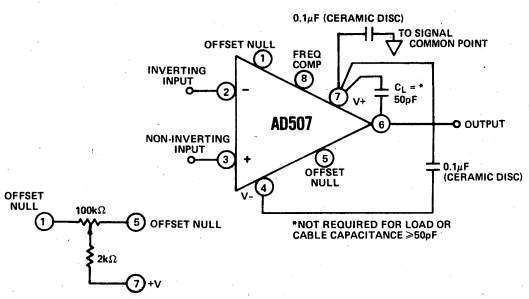


Figure 1. General Purpose Configuration to Closed Loop Gain > 10

Low Gain Conditions

For low closed loop gain applications, the AD507 should be compensated with a 20pF capacitor from pin 8 (frequency compensation) to signal common or pin 7 (V+). This configuration also requires a 30pF feedback capacitor from pin 6 (Output) to pin 8 (see Figure 2). The 50pF minimum load capacitance recommended for uncompensated applications is not required when the AD507 is used in the compensated mode. This compensation results in a unity gain frequency of approximately 10 to 12MHz.

The excellent input characterisitcs of the AD507 make it useful in low frequency applications where both dc and ac performance superior to the 741 type of op amp is desired. Some experimentation may be necessary to optimize the AD507 for the specific requirement. The unity gain bandwidth can be reduced by increasing the value of the compensation capacitor in inverse proportion to the desired bandwidth reduction. It is advisable to increase the feedback capacitor at the same time, maintaining its value about 50% larger than the compensation capacitor. Because the AD507 is fundamentally a wideband amplifier, careful power supply decoupling and compensation component layout are required even in low bandwidth applications.

OFFSET VOLTAGE NULLING

Note that the offset voltage null circuit includes a 2kΩ resistor in series with the wiper arm of the 100kΩ potentiometer. This resistor is not absolutely required, but its use can prevent a condition of false null that can be obtained at the ends of the pot range. The knowledgeable user should have no trouble differentiating between nulling in the pot mid-range and erratic end-range behavior when the wiper is connected directly to V+.

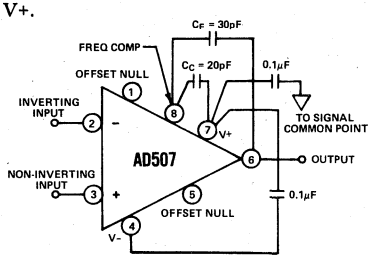


Figure 2. Configuration for Unity Gain Applications

HIGH CAPACITIVE LOADING

Like all wideband amplifiers, the AD507 is sensitive to capacitive loading. Unlike many, however, the AD507 can be used to effectively drive reasonable capacitive loads in virtually all applications, and capacitive loads of several hundred picofarads in a number of specific configurations.

In an inverting gain of ten configuration, the internally compensated amplifier will drive more than 200pF in addition to the recommended 50pF load, or a total of over 250pF. Under such conditions, the slew rate will be only slightly reduced, and the overall settling time somewhat lengthened.

In general, the capacitive drive capability of the AD507 will increase in high gain configurations which reduce closed loop bandwidth.

In any wideband application, it is essential to return the load currents supplied by the amplifier to the power supply without sharing a path with input or feedback signals. This consideration becomes particularly important when driving capacitive loads which may resonate with short lengths of interconnecting wire.

FAST SETTLING TIME

A small capacitor (C_S in Figure 3) will improve the settling time of the AD507, when it is used with large feedback resistors. The AD507 input capacitance (typically 2 or 3pF), together with additional circuit capacitance, will introduce an unwanted pole of open-loop response. The extra phase shift introduced, for example, by 4pF of input capacitance, and

5kΩ input source impedance, will result in an underdamped transient response, and long settling time. A small (1.5 to 3.0pF) feedback capacitor will introduce a zero in the open-loop transfer function, reducing the phase shift and increasing the damping, which will more than compensate for the slight reduction in closed-loop bandwidth.

BIAS COMPENSATION NOT REQUIRED

Circuit applications using conventional op amps generally require that the source resistances be matched at the inputs to cancel the effects of the input currents and take advantage of low offset current. In circuits similar to that shown in Figure 3, the compensation resistance would be equal to the parallel combination of R_I and R_F, and for large values would require a bypass capacitor. The AD507 is specially designed to cancel the input currents so as to reduce them to the offset current level. As a result, optimum performance can be obtained even though no bias compensation is used, and the non-inverting input can be connected directly to the signal common.

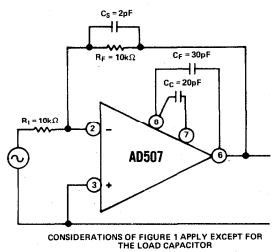
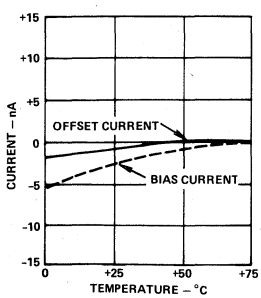
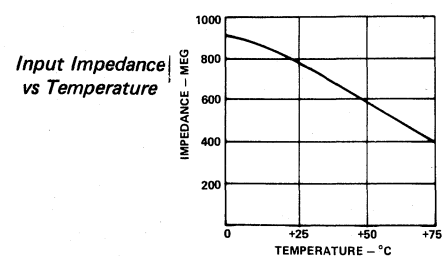


Figure 3. Fast Settling Time Configuration

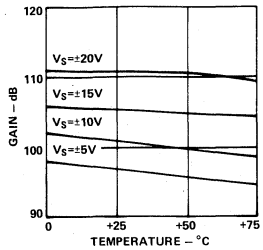
TYPICAL PERFORMANCE CURVES



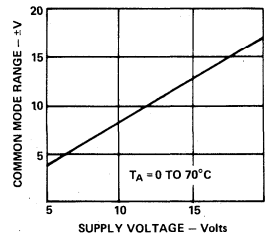
Input Bias Current and Offset Current vs Temperature



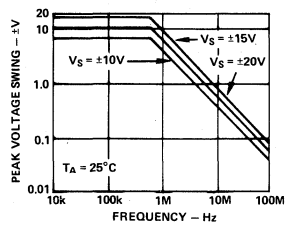
Input Impedance vs Temperature



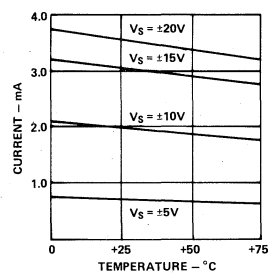
Open Loop Voltage Gain vs Temperature



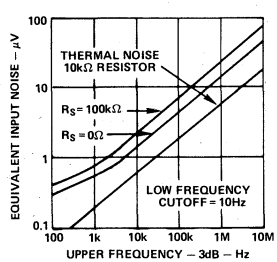
Common Mode Voltage Range vs Supply Voltage



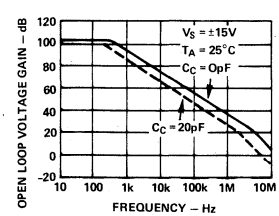
Output Voltage Swing vs Frequency



Power Supply Current vs Temperature



Broadband Input Noise Characteristics



Open Loop Gain vs Frequency

ANALOG DEVICES

High Speed, Fast Settling IC Op Amp

AD509

4

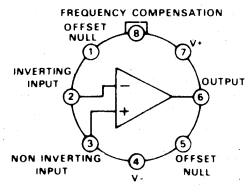
FEATURES

- Fast Settling Time
  - 0.1% in 500ns max
  - 0.01% in 2.5μs max
- High Slew Rate: 100V/μs min
- Low I_{OS}: 25nA max
- Guaranteed V_{OS} Drift: 30μV/°C max
- High CMRR: 80dB min
- Drives 500pF

APPLICATIONS

- D/A and A/D Conversion
- Wideband Amplifiers
- Multiplexers
- Pulse Amplifiers

AD509 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD509J, AD509K and AD509S are monolithic operational amplifiers specifically designed for applications requiring fast settling times to high accuracy. Other comparable dynamic parameters include a small signal bandwidth of 20MHz, slew rate of 100V/μs min and a full power response of 150kHz min. The devices are internally compensated for all closed loop gains greater than 3, and are compensated with a single capacitor for lower gains.

The input characteristics of the AD509 are consistent with 0.01% accuracy over limited temperature ranges; offset current is 25nA max, offset voltage is 8mV max, nullable to zero, and offset voltage drift is limited to 30μV/°C max. PSRR and CMRR are typically 90dB.

The AD509 is designed for use with high speed D/A or A/D converters where the minimum conversion time is limited by the amplifier settling time. If 0.01% accuracy of conversion is required, a conversion cannot be made in a shorter period than the time required for the amplifier to settle to within 0.01% of its final value.

All devices are supplied in the TO-99 package. The AD509J and AD509K are specified for 0 to +70°C temperature range; the AD509S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD509 is internally compensated for all closed loop gains above 3, and compensated with a single capacitor for lower gains thus eliminating the elaborate stabilizing techniques required by other high speed IC op amps.
2. The AD509 will drive capacitive loads of 500pF without deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time.
3. Common Mode Rejection, Gain and Noise are compatible with a 0.01% accuracy device.
4. The AD509K and AD509S are 100% tested for minimum slew rate and guaranteed to settle to 0.01% of its final value in less than 2.5μs.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

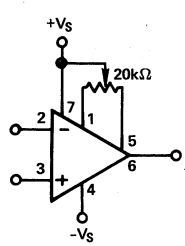
Model	AD509J Min	AD509J Typ	AD509J Max	AD509K Min	AD509K Typ	AD509K Max	AD509S Min	AD509S Typ	AD509S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**75,000**	15,000		**10,000**	15,000		**10,000**	15,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	5,000			7,500			**7,500**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		±**10**	±12		V
FREQUENCY RESPONSE										
Unity Gain Small Signal		20			20			20		MHz
Full Power Response	1.2	1.6		1.5	2.0		1.5	2.0		MHz
Slew Rate, Unity Gain	80	120		80	120		100	120		V/µs
Settling Time										
to 0.1%		200			200			200	500	ms
to 0.01%		1.0			1.0			1.0	2.5	µs
INPUT OFFSET VOLTAGE										
Initial Offset		5	**10**		4	**8**		4	**8**	mV
Input Offset Voltage T_{min} to T_{max}			14			11			**11**	mV
Input Offset Voltage vs. Supply,										
T_{min} to T_{max}			**200**			**100**			**100**	µV/V
INPUT BIAS CURRENT										
Initial		125	**250**		100	**200**		100	**200**	nA
T_{min} to T_{max}			500			400			**400**	nA
INPUT OFFSET CURRENT										
Initial		20	50		10	25		10	25	nA
T_A = min to max			100			50			50	nA
INPUT IMPEDANCE										
Differential	40	100		50	100		50	100		MΩ
INPUT VOLTAGE RANGE										
Differential		±15			±15			±15		V
Common Mode		±10			±10			±10		V
Common Mode Rejection	**74**	90		**80**	90		**80**	90		dB
INPUT NOISE VOLTAGE										
f = 10Hz		100			100			100		nV/√Hz
f = 100Hz		30			30			30		nV/√Hz
f = 100kHz		19			19			19		nV/√Hz
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±20	±5		±20	±5		±20	V
Quiescent Current		4	**6**		4	**6**		4	**6**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[1]										
TO-99 Style (H08A)		AD509JH			AD509KH			AD509SH		

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Simplified Nulling Circuit

APPLYING THE AD509

MEASURING SETTLING TIME. Settling time is defined as that period required for an amplifier output to swing from 0 volts to full scale, usually 10 volts, and to settle to within a specified percentage of the final output voltage. For high accuracy systems, the accuracy requirement is normally specified as either 0.1% (10-bit accuracy) or 0.01% (12-bit accuracy) of the 10 volt output level. The settling time period is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vicinity of 10 volts, and a final time period to recover from internal saturation and other effects, and settle within the specified error band. Because settling time depends on both linear and nonlinear factors, there is no simple approach to predicting its final value to different levels of accuracy. In particular, extremely high slew rates do not assure a rapid settling time, since this is only one of many factors affecting settling time. In most high speed amplifiers, after the amplifier has slewed to the vicinity of the final output voltage, it must recover from internal saturation and then allow any overshoot and ringing to damp out. These definitions are illustrated in Figure 1.

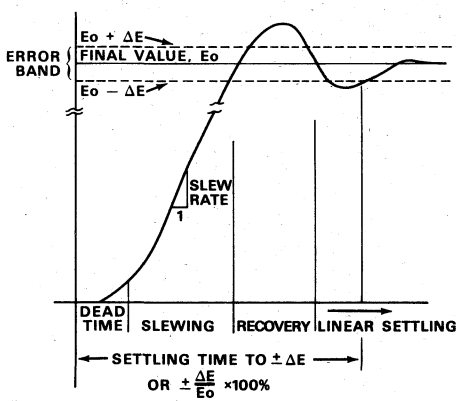


Figure 1. Settling Time

The AD509K and AD509S are guaranteed to settle to 0.1% in 500ns and 0.01% in 2.5μs when tested as shown in Figure 2. There is no appreciable degradation in settling time when the capacitive load is increased to 500pF, as discussed below. The settling time is computed by summing the output and the input into a differential amplifier, which then drives a scope display. The resultant waveform of ($E_O - E_{IN}$) of a typical AD509 is shown in Figure 3. Note that the waveform crosses the 1mV point representing 0.01% accuracy in approximately 1.5μs. The top trace represents the output signal; the bottom trace represents the error signal.

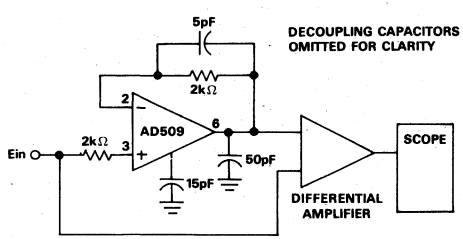


Figure 2. AD509 Settling Time Test Circuit

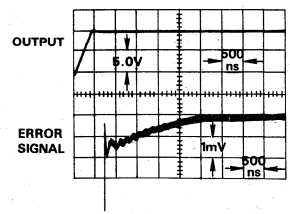


Figure 3. Settling Time of AD509

SETTLING TIME VS. R_f AND R_i. Settling time of an amplifier is a function of the feedback and input resistors, since they interact with the input capacitance of the amplifier. When operating in the non-inverting mode, the source impedance should be kept relatively low; e.g., 5kΩ; in order to insure optimum performance. The small feedback capacitor (5pF) is used in the settling time test circuit in parallel with the feedback resistor to reduce ringing. This capacitor partially cancels the pole formed in the loop gain response as a result of the feedback and input resistors, and the input capacitance.

SETTLING TIME VS. CAPACITIVE LOAD. The AD509 will drive capacitive loads of 500pF without appreciable deterioration in settling time. Larger capacitive loads can be driven by tailoring the compensation to minimize settling time. Figure 4 shows the settling time of a typical AD509, compensated for unity gain with a 15pF capacitor, with a 500pF capacitive load on the output. Note that settling time to 0.01% is still under 2.0μs.

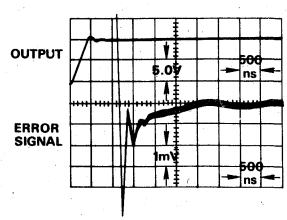


Figure 4. AD509 with 500pF Capacitive Load

SUGGESTIONS FOR MINIMIZING SETTLING TIME. The AD509 has been designed to settle to 0.01% accuracy in 1 to 2.5μs. However, this amplifier is only a building block in a circuit that also has a feedback network, input and output connections, power supply connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost without careful circuit design. Some of the elements of a good high speed design are.....

CONNECTIONS. It is essential that care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.

The 0.1μF ceramic power supply bypass capacitors are considerably more important for the AD509 than for low frequency general purpose amplifiers. Their main purpose is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. The signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal (pin 7 [V+]).

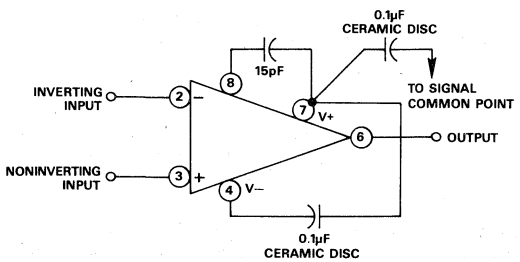


Figure 5. Configuration for Unity Gain Applications

In addition, it is suggested that all connections be short and direct, and as physically close to the case as possible, so that the length of any conducting path shared by external components will be minimized.

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in any feedback networks used with the amplifier. Minimize noise pickup.

DYNAMIC RESPONSE OF AD509

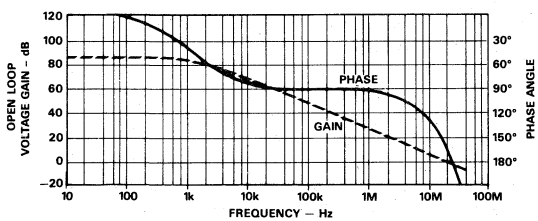


Figure 6. Open Loop Frequency and Phase Response

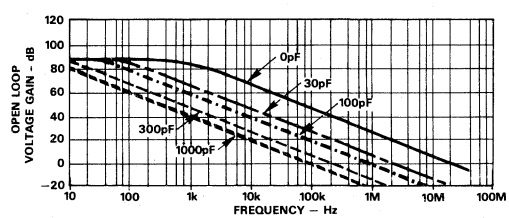


Figure 7. Open Loop Frequency Response for Various C_C's

THE AD509 AS AN OUTPUT AMPLIFIER FOR FAST CURRENT-OUTPUT D-TO-A CONVERTERS

Most fast integrated circuit digital to analog converters have current outputs. That is, the digital input code is translated to an output current proportional to the digital code. In many applications, that output current is converted to a voltage by connecting an operational amplifier in the current-to-voltage conversion mode.

The settling time of the combination depends on the settling time of the DAC and the output amplifier. A good approximation is:

$$t_{s\,TOTAL} = \sqrt{(t_{s\,DAC})^2 + (t_{s\,AMP})^2}$$

Some IC DACs settle to final output value in 100-500 nanoseconds. Since most IC op amps require a longer time to settle to ±0.1% or ±0.01% of final value, amplifier settling time can dominate total settling time. And for a 12-bit DAC, one least significant bit is only 0.024% of full-scale, so low drift and high linearity and precision are also required of the output amplifier.

Figure 8 shows the AD509K connected as an output amplifier with the AD565K, high speed 12-bit IC digital-to-analog converter. The 10 picofarad capacitor, C1, compensates for the 25pF AD565 output capacitance. The voltage output of the AD565K/AD509K combination settles to ±0.01% in one microsecond. The low input voltage drift and high open loop gain of the AD509K assures 12-bit accuracy over the operating temperature range.

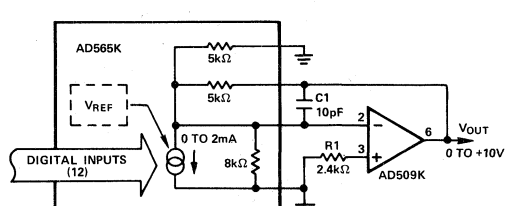


Figure 8. AD509 as an Output Amplifier for a Fast Current-Output D-to-A Converter

ANALOG DEVICES

Low Cost, Laser Trimmed, Precision IC Op Amp

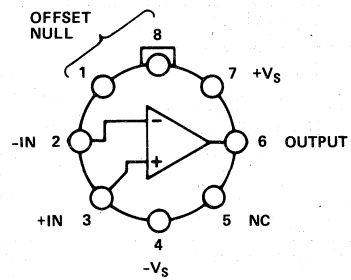
AD510

4

FEATURES

Low V_{OS}: 25μV max (AD510L), 100μV max (AD510J)
Low V_{OS} Drift: 0.5μV/°C max (AD510L)
Internally Compensated
High Open Loop Gain: 10^6 min
Low Noise: 1μV p-p 0.01 to 10Hz

AD510 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD510 is the first low cost high accuracy IC op amp available. Analog Devices' precise thermally-balanced layout combined with high-yield IC processing provides truly superlative op amp performance at the lowest possible cost. The device is internally compensated, thus eliminating the need for an additional external capacitor.

A truly precision device, the AD510 achieves laser trimmed offset voltages less than 25μV max and offset voltage drifts of 0.5μV/°C max (nulled). Bias currents and offset currents are available at less than 10nA and 2.5nA respectively, while open loop gain is maintained at over 1,000,000, even under loaded conditions. Designed along a thermal axis, the AD510 is unaffected by thermal gradients across the monolithic chip caused by current loading.

The AD510 has fully protected inputs, permitting differential input voltages of up to $\pm V_S$ without voltage gain or bias current degradation due to reverse breakdown. The output is also protected from short circuits and drives 1000pF of load capacitance without oscillation.

The AD510 is specifically designed for applications requiring high precision at the lowest possible cost, such as bridge instruments, stable references, followers and analog computation. Packaged in a hermetically-sealed TO-99 metal can, the AD510 is available in three versions of performance (J, K and L) over the commercial temperature range, 0 to +70°C and one version (S) over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage drift is guaranteed and 100% tested on all models with a controlled temperature drift bath with the offset voltage nulled. Offset voltage on the AD510L is tested following a 3 minute warm-up.
2. The AD510 offers fully protected input (to $\pm V_S$) and output circuitry. The input protection circuit prevents offset voltage and bias current degradation due to reverse breakdown, a critical factor in high accuracy op amps where overall performance is strongly dependent on front-end stability.
3. Internal compensation eliminates the need for elaborate and costly stabilizing networks, often required by many high accuracy IC op amps.
4. A thermally balanced layout maintains high gain (1,000,000 min, K, L and S) independent of offset nulling, power supply voltage and output loading.
5. Bootstrapping of critical input transistors produces CMRR and PSRR of 110dB min and 100dB min, respectively.

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD510JH	AD510KH	AD510LH	AD510SH
OPEN LOOP GAIN				
V_{OS} = ±10V, $R_L > 2k\Omega$	250,000 min	10^6 min	**	**
T_{min} to T_{max}	125,000 min	500,000 min	**	250,000
OUTPUT CHARACTERISTICS				
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*	*
Load Capacitance	1000pF	*	*	*
Output Current	10mA min	*	*	*
Short Circuit Current	25mA	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	300kHz	*	*	*
Full Power Response	1.5kHz	*	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*	*
INPUT OFFSET VOLTAGE				
Initial Offset, $R_S \leq 10k\Omega$	100μV max	50μV max	25μV max	**
vs. Temp., T_{min} to T_{max}	3.0μV/°C max	1.0μV/°C max	0.5μV/°C max	**
vs. Supply	25μV/V max	10μV/V max	**	**
T_{min} to T_{max}	40μV/V max	15μV/V max	**	20μV/V max
INPUT OFFSET CURRENT				
Initial	5nA max	4nA max	2.5nA max	**
T_{min} to T_{max}	8nA max	6nA max	4nA max	10nA max
INPUT BIAS CURRENT				
Initial	25nA max	13nA max	10nA max	**
T_{min} to T_{max}	40nA max	20nA max	15nA max	30nA max
vs. Temp, T_{min} to T_{max}	±100pA/°C	±50pA/°C	±40pA/°C	**
INPUT IMPEDANCE				
Differential	4MΩ	6MΩ	**	**
Common Mode	100MΩ‖4pF	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	1μV p-p	*	*	*
f = 10Hz	18nV/$\sqrt{Hz}$	*	*	*
f = 100Hz	13nV/$\sqrt{Hz}$	*	*	*
f = 1kHz	10nV/$\sqrt{Hz}$	*	*	*
Current, f = 10Hz	0.5pA/$\sqrt{Hz}$	*	*	*
f = 100Hz	0.3pA/$\sqrt{Hz}$	*	*	*
f = 1kHz	0.3pA/$\sqrt{Hz}$	*	*	*
INPUT VOLTAGE RANGE				
Differential or Common Mode max safe	$\pm V_S$	*	*	*
Common Mode Rejection, V_{in} = ±10V	94dB min	110dB min	**	**
Common Mode Rejection, T_{min} to T_{max}	94dB	100dB min	**	**
POWER SUPPLY				
Rated Performance	±15V	*	*	*
Operating	±(5 to 18)V	*	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**	**
TEMPERATURE RANGE				
Operating Rated Performance	0 to +70°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTIONS:[1] TO-99 Style (H08B)	AD510JH	AD510KH	AD510LH	AD510SH

NOTES

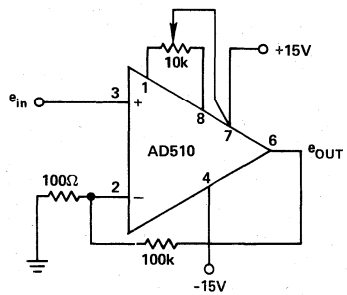
*Specifications same as AD510JH.

**Specifications same as AD510KH.

[1] See Section 19 for package outline information.

Specification subject to change without notice.

TYPICAL
NON-INVERTING AMPLIFIER CONFIGURATION



NULLING THE AD510

Nulling the AD510 can be achieved using the high resolution circuit of Figure 1.

1. Null the offset to zero using a commercially available pot (approximately 10kΩ).
2. Measure pot halves, R_1 and R_2.
3. Calculate . . . $R_1' = \frac{R_1 \times 50k\Omega}{50k\Omega - R_1}$ $R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$
4. Insert R_1' and R_2' (closest 1% fixed metal film resistors).
5. Use an industrial quality 100kΩ pot (r_p) to fine tune the trim.

Nulling to within 1 microvolt can be achieved using this technique. For best results, the wiper of the potentiometer should be connected directly to pin 7 of the op amp.

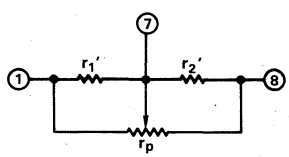


Figure 1. High Resolution, High Stability Nulling Circuit

THE AD510L IN A SIMPLE INSTRUMENTATION AMPLIFIER

The circuit of Figure 2 illustrates a simple instrumentation amplifier suitable for use with strain gauges, thermocouples and other transducers. It provides high input impedance to ground at each of the differential input terminals and excellent common mode rejection.

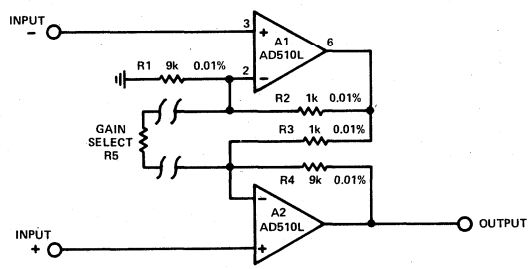


Figure 2. Instrumentation Amplifier

The configuration shown is designed for a gain of 10, however the gain can be varied upwards by adding a gain select resistor R_5. In operation, amplifier A_1 provides a gain of 10/9 for signals at the negative input terminal. This output feeds the inverting amplifier A_2, which has a gain of 9, resulting in an overall gain of 10. For signals at the positive input, the output of A_1 is at ground potential and the amplifier A_2 provides a gain of 10. Thus, the circuit has a gain of 10 for differential signals and 0 for common mode signals; the very high CMRR and open loop gain of the AD510L automatically produces common mode rejection of at least 25,000 at dc at a gain of 10 and over 1,000,000 at a gain of 1000. The common mode rejection, of course, depends upon the resistor ratios and their specified tolerance. Less accurate resistors can be used if the network is trimmed.

For gains of 10 the frequency response is down 3dB at 500kHz, for gains of 1000, 2kHz. Full output of ±10V can be attained up to 1800Hz.

The common mode rejection at 60Hz is limited by the finite gain bandwidth of A_1 causing a phase lag on the negative input signal. At 60Hz the CMRR measures 72dB at a gain of 1000 and 62dB at a gain of 10.

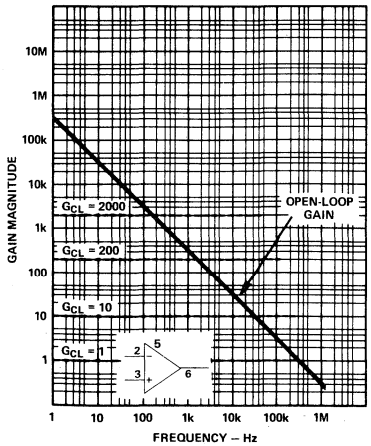


Figure 3. Small Signal Gain vs. Frequency

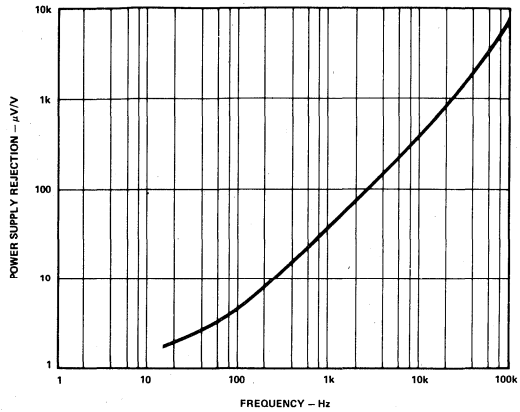


Figure 4. PSRR vs. Frequency

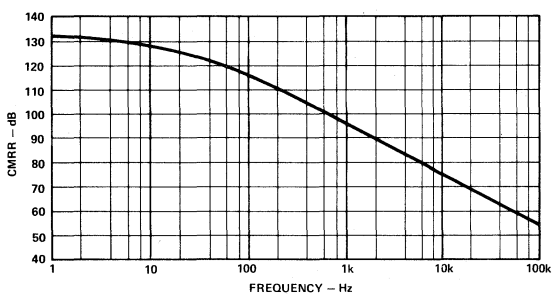


Figure 5. CMRR vs. Frequency

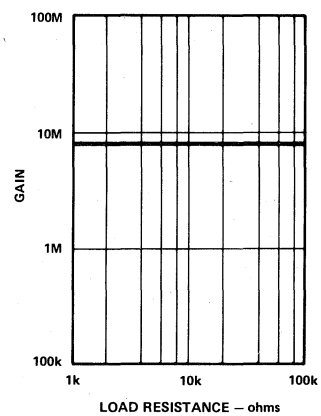


Figure 6. Gain vs. Load Resistance

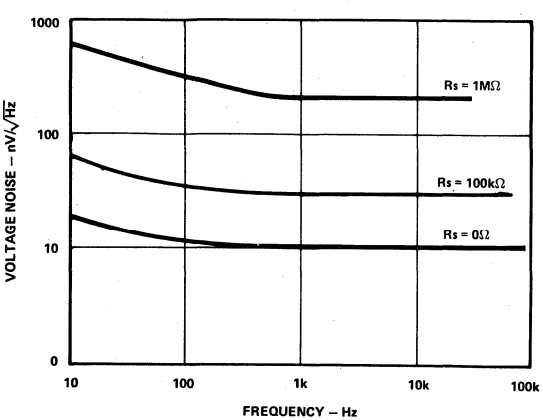


Figure 7. Voltage Noise vs. Frequency

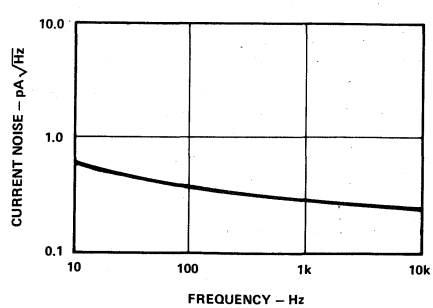


Figure 8. Current Noise vs. Frequency

ANALOG DEVICES

Precision, Low-Power FET-Input Electrometer Op Amp

AD515

FEATURES

Ultra Low Bias Current: 0.075pA max (AD515L)
0.150pA max (AD515K)
0.300pA max (AD515J)

Low Power: 1.5mA max Quiescent Current
(0.8mA typ)

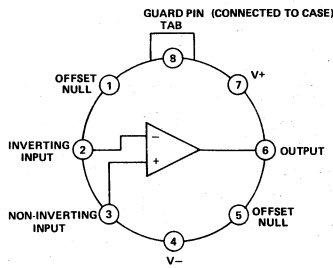
Low Offset Voltage: 1.0mV max (AD515 K & L)

Low Drift: 15μV/°C max (AD515K)

Low Noise: 4μV p-p, 0.1 to 10Hz

Low Cost

AD515 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD515 series of FET-input operational amplifiers are second generation electrometer designs offering the lowest input bias currents available in any standard operational amplifier. The AD515 also delivers laser-trimmed offset voltage, low drift, low noise and low power, a combination of features not previously available in ultra-low bias current circuits. All devices are internally compensated, free of latch-up, and short circuit protected.

The AD515 delivers a new level of versatility and precision to a wide variety of electrometer and very high impedance buffer measurement situations, including photo-current detection, vacuum ion-gauge measurement, long term precision integration, and low drift sample/hold applications. The device is also an excellent choice for all forms of biomedical instrumentation such as pH/pIon sensitive electrodes, very low current oxygen sensors, and high impedance biological microprobes. In addition, the low cost and pin compatibility of the AD515 with standard FET op amps will allow designers to upgrade the performance of present systems at little or no additional cost. The 10^{15} ohm common mode input impedance, resulting from a solid bootstrap input stage, insures that the input bias current is essentially independent of common mode voltage.

As with previous electrometer amplifier designs from Analog Devices, the case is brought out to its own connection (pin 8) so that the case can be independently connected to a point at the same potential as the input, thus minimizing stray leakage to the case. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD515 is available in three versions of bias current and offset voltage, the "J", "K", and "L"; all are specified for rated performance from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The AD515 provides the lowest bias currents available in an integrated circuit amplifier.
   - The ultra low input bias currents are specified as the maximum measured at either input with the device fully warmed up on ±15 volt supplies at +25°C ambient with no heat sink. This parameter is 100% tested.
   - By using ±5 volt supplies, input bias current can typically be brought below 50fA.

2. The input offset voltage on all grades is laser trimmed to a level typically less than 500μV.
   - The offset voltage drift is the lowest available in an FET electrometer amplifier.
   - If additional nulling is desired, the amount required will have a minimal effect on offset drift (approximately 3μV/°C per millivolt nulled).

3. The low quiescent current drain of 0.8mA typical and 1.5mA maximum, which is among the lowest available in operational amplifier designs of any type, keeps self-heating effects to a minimum and renders the AD515 suitable for a wide range of remote probe situations.

4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one Megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristic.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD515J Min	AD515J Typ	AD515J Max	AD515K Min	AD515K Typ	AD515K Max	AD515L Min	AD515L Typ	AD515L Max	Units
OPEN LOOP GAIN[1]										
V_O = ±10V, $R_L \geq 2k\Omega$	**20,000**			**40,000**			**25,000**			V/V
V_O = ±10V, $R_L \geq 10k\Omega$	**40,000**			**100,000**			**50,000**			V/V
T_{min} to T_{max}, R_L = 2kΩ	**15,000**			**40,000**			**25,000**			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ R_L = 10kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		V
Load Capacitance[2]		1000			1000			1000		pA
Short Circuit Current	**10**	25	**50**	**10**	25	**50**	**10**	25	**50**	mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		350			350			350		MHz
Full Power Response	5	16		5	16			5		MHz
Slew Rate, Unity Gain	0.3	1.0		0.3	1.0		0.3	1.0		V/μs
Overload Recover, Inverting Unity Gain		16	100		16	100		16	100	μs
INPUT OFFSET VOLTAGE[3]										
Initial Offset		0.4	**3.0**		0.4	**1.0**		0.4	**1.0**	mV
Input Offset Voltage vs. Temperature			**50**			**15**			**25**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}		50	**400**			**100**			**200**	μV/V
INPUT BIAS CURRENT										
Either Input[4]			**300**			**150**			75	FA
INPUT IMPEDANCE										
Differential		$10^{13}\|1.6$			$10^{13}\|1.6$			$10^{13}\|1.6$		MΩ|pA
Common Mode		$10^{15}\|0.8$			$10^{15}\|0.8$			$10^{15}\|0.8$		MΩ|pA
INPUT VOLTAGE RANGE										
Differential	±20			±20			±20			V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**66**	94		**80**			**70**			dB
INPUT NOISE										
Voltage, 0.1Hz to 10Hz		4.0			4.0			4.0		μV p-p
f = 10Hz		75			75			75		nV/√Hz
f = 100Hz		55			55			55		nV/√Hz
f = 1Hz		50			50			50		nV/√Hz
Current, 0.1Hz to 10Hz		0.003			0.003			0.003		pA (p-p)
10Hz to 10kHz		0.01			0.01			0.01		pA (rms)
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	V
Quiescent Current		0.8	**1.5**		0.8	**1.5**		0.8	**1.5**	mA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[6]										
TO-99 Style (H08B)		AD515JH			AD515KH			AD515LH		

NOTES

[1]Open Loop Gain is specified with or without nulling of V_{OS}.

[2]A conservative design would not exceed 750pF of load capacitance.

[3]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

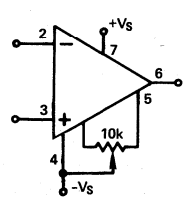
[4]Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5]If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.3mA indefinitely without damage. See next page.

[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading. The AD515, with its combination of low offset voltage (normally eliminating the need for trimming), low quiescent current (minimal source heating, possible battery operation), internal compensation and small physical size lends itself very nicely to installation at the signal source or inside a probe. Also, as a result of the high load capacitance rating, the AD515 can comfortably drive a long signal cable.
2. The use of guarding techniques is essential to realizing the capability of the ultra-low input currents of the AD515. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pick-up and serves an additional function of reducing the effective capacitance to the input line. The case of the AD515 is brought out separately to pin 8 so that the case can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 1 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or a power supply to reduce noise.

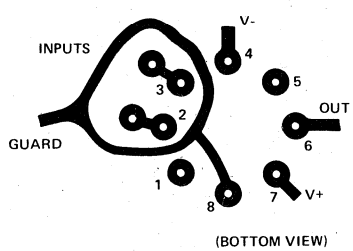


Figure 1. Board Layout for Guarding Inputs with Guarded TO-99 Package

3. Printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance that the AD515 can deliver. The best performance will be realized by using a teflon IC socket for the AD515; but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 1 will minimize leakage as much as possible; the guard ring should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.
4. Another important concern for achieving and maintaining low leakage currents is complete cleanliness of circuit boards and components. Completed assemblies should be washed thoroughly in a low residue solvent such as TMC Freon or high-purity methanol followed by a rinse with deionized water and nitrogen drying. If service is anticipated in a high contaminant or high humidity environment, a high dielectric conformal coating is recommended. All insulation materials except Kel-F or teflon will show rapid degradation of surface leakage at high humidities.

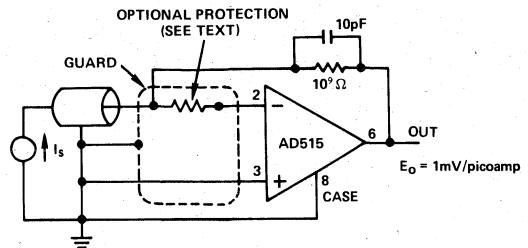


Figure 2. Picoampere Current-to-Voltage Converter Inverting Configuration

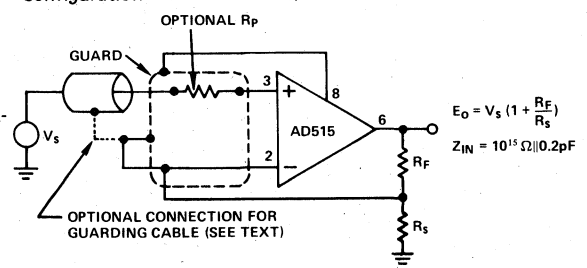


Figure 3. Very High Impedance Non-Inverting Amplifier

INPUT PROTECTION

The AD515 is guaranteed for a maximum safe input potential equal to the power supply potential. The unique bootstrapped input stage design also allows differential input voltages of up to ±20 volts (or within 10 volts of the sum of the supplies) while maintaining the full differential input resistance of $10^{13}\Omega$, as shown in Figure 10. This makes the AD515 suitable for low speed comparator situations employing a direct connection to a high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The AD515 requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 0.5mA (for example, 200kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figures 2 and 3 show proper connections.

COAXIAL CABLE AND CAPACITANCE EFFECTS

If it is not possible to attach the AD515 virtually on top of the signal source, considerable care should be exercised in designing the connecting lines carrying the high impedance signal. Shielded coaxial cable must be used for noise reduction, but use of coaxial cables for high impedance work can add problems from cable leakage, noise, and capacitance. Only the best polyethylene or virgin teflon (not reconstituted) should be used to obtain the highest possible insulation resistance.

Cable systems should be made as rigid and vibration-free as possible since cable movement can cause noise signals of three types, all significant in high impedance systems. Frictional movement of the shield over the insulation material generates a charge which is sensed by the signal line as a noise voltage. Low noise cable with graphite lubricant will reduce the noise, but short rigid lines are better. Cable movements will also make small changes in the internal cable capacitance and capacitance to other subjects. Since the total charge on these capacitances cannot be changed instantly, a noise voltage results as predicted from: $\Delta V = Q/\Delta C$. Noise voltage is also generated by the motion of a conductor in a magnetic field.

The conductor-to-shield capacitance of coaxial cable is normally about 30pF/foot. Charging this capacitance can cause considerable stretching of high impedance signal rise-time, thus cancelling the low input capacitance feature of the AD515. There are two ways to circumvent this problem. For inverting signals or low-level current measurements, the signal is carried on the line connected to the inverting input and shielded (guarded) by the ground line as shown in Figure 2. Since the signal is always at virtual ground, no voltage change is required and no capacitances are charged. In many circumstances, this will de-stabilize the circuit; if so, capacitance from output to inverting input will stabilize the circuit.

Non-inverting and buffer situations are more critical since the signal line voltage and therefore charge will change, causing signal delay. This effect can be reduced considerably by connecting the cable shield to guard potential instead of ground, an option shown in Figure 3. Since such a connection results in positive feedback to the input, the circuit may destabilize and oscillate. If so, capacitance from positive input to ground must be added to make the net capacitance at pin 3 positive. This technique can considerably reduce the effective capacitance which must be charged.

Typical Performance Curves

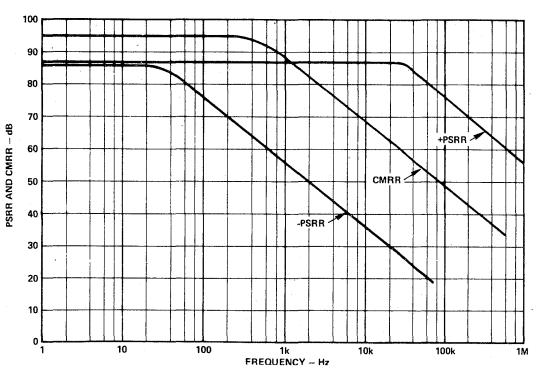


Figure 4. PSRR and CMRR Versus Frequency

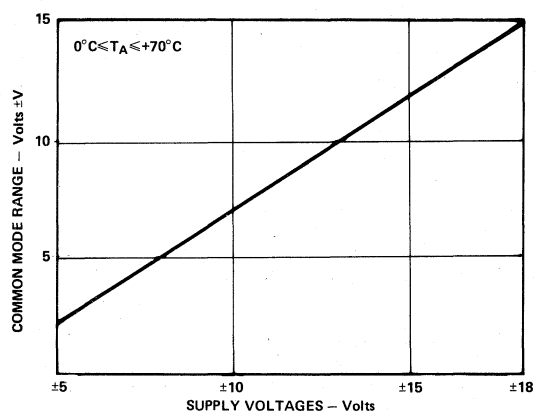


Figure 6. Input Common Mode Range Versus Supply Voltage

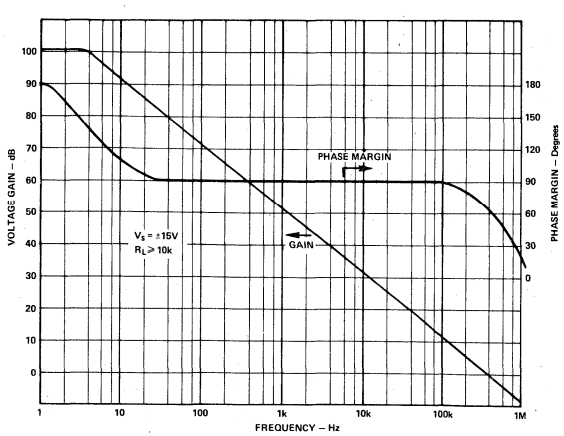


Figure 5. Open Loop Frequency Response

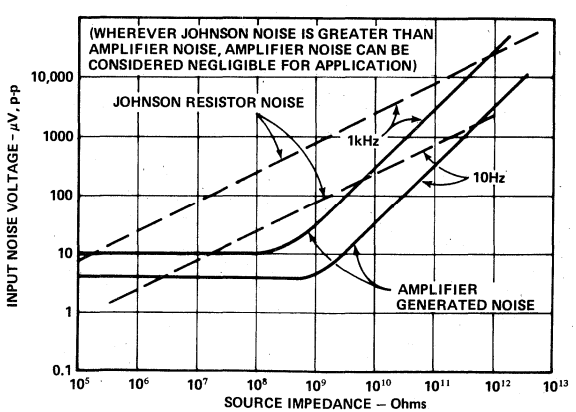


Figure 7. Peak-to-Peak Input Noise Voltage Versus Source Impedance and Bandwidth

ELECTROMETER APPLICATION NOTES

The AD515 offers the lowest input bias currents available in an integrated circuit package. This design will open up many new application opportunities for measurements from very high impedance and very low current sources. Performing accurate measurements of this sort requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD515 and perhaps extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature.
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if it is possible to reduce the required power supplies, this should be done since internal power consumption contributes the largest component of self-heating. To minimize this effect, the quiescent current of the AD515 has been reduced to a level much lower than that of any other electrometer-grade device, but additional performance improvement can be gained by lowering the supply voltages, to ±5 volts if possible. The effects of this are shown in Figure 8, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated. Therefore, although many dc performance parameters are specified driving a 2kΩ load, to reduce this additional dissipation, we recommend restricting the load impedance to be at least 10kΩ.

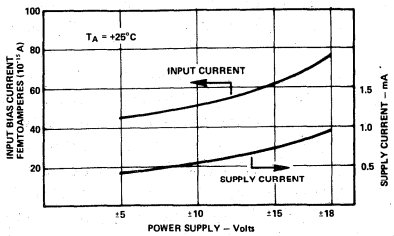


Figure 8. Input Bias Current and Supply Current Versus Supply Voltage

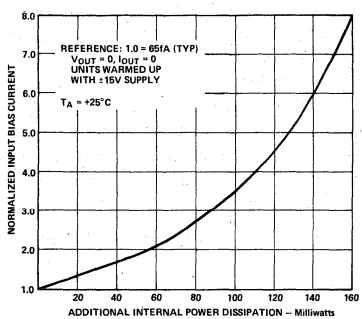


Figure 9. Input Bias Current Versus Additional Power Dissipation

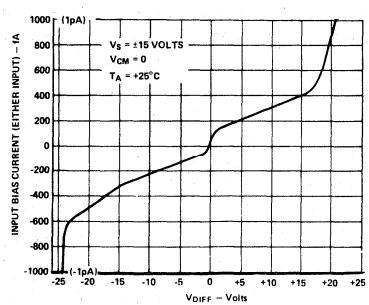


Figure 10. Input Bias Current Versus Differential Input Voltage

AD515 CIRCUIT APPLICATION NOTES

The AD515 is quite simple to apply to a wide variety of applications because of the pre-trimmed offset voltage and internal compensation, which minimize required external components and eliminate the need for adjustments to the device itself. The major considerations in applying this device are the external problems of layout and heat control which have already been discussed. In circuit situations employing the use of very high value resistors, such as low level current to voltage converters, electrometer operational amplifiers can be destabilized by a pole created by the small capacitance at the negative input. If this occurs, a capacitor of 2 to 5pF in parallel with the resistor will stabilize the loop. A much larger capacitor may be used if desired to limit bandwidth and thereby reduce wideband noise.

Selection of passive components employed in high impedance situations is critical. High-megohm resistors should be of the carbon film or deposited ceramic oxide to obtain the best in low noise and high stability performance. The best packaging for high-megohm resistors is a glass body sprayed with silicone varnish to minimize humidity effects. These resistors must be handled very carefully to prevent surface contamination. Capacitors for any high impedance or long term integration situation should be of a polystyrene formulation for optimum performance. Most other types have too low an insulation resistance, or high dielectric absorption.

Unlike situations involving standard operational amplifiers with much higher bias currents, balancing the impedances seen at the input terminals of the AD515 is usually unnecessary and probably undesirable. At the large source impedances where these effects matter, obtaining quality, matched resistors will be difficult. More important, instead of a cancelling effect, as with bias current, the noise voltage of the additional resistor will add by root-sum-of-squares to that of the other resistor thus increasing the total noise by about 40%. Noise currents driving the resistors also add, but in the AD515 are significant only above $10^{11}\,\Omega$.

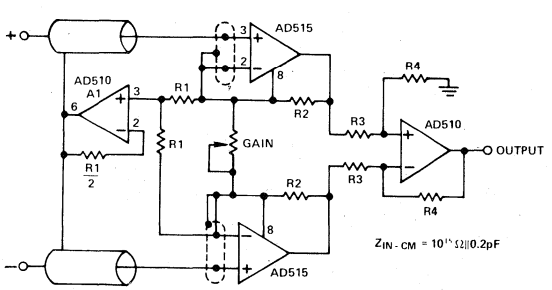


Figure 11. Very High Impedance Instrumentation Amplifier

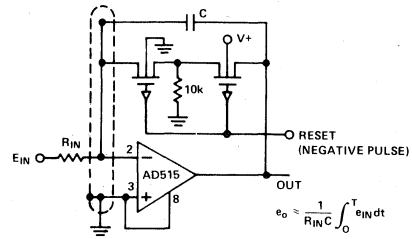


Figure 12. Low Drift Integrator and Low-Leakage Guarded Reset

LOW-LEVEL CURRENT TO VOLTAGE CONVERTERS

Figure 2 shows a standard low-level current-to-voltage converter. To obtain higher sensitivity, it is obvious to simply use a higher value feedback resistor. However, high value resistors above $10^9\,\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 13. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD515 makes the tradeoff easier.

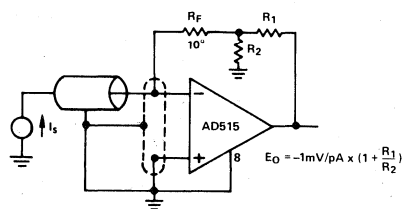


Figure 13. Picoampere to Voltage Converter with Gain

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 14 shows a technique in which the desired bias is applied at the non-inverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD521 instrumentation amplifier converts the floating differential signal to a single-ended output.

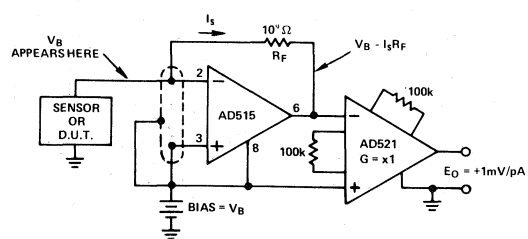


Figure 14. Current-to-Voltage Converters with Grounded Bias and Sensor

ANALOG DEVICES

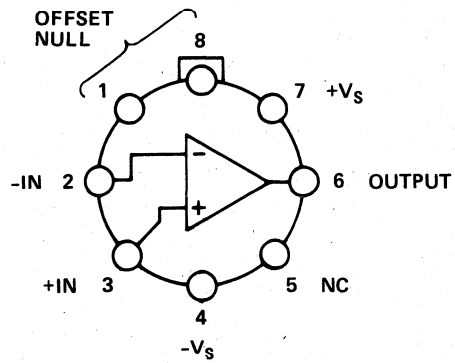
Low Cost, Laser Trimmed, Precision IC Op Amp

AD517

FEATURES

Low Input Bias Current: 1nA max (AD517L)
Low Input Offset Current: 0.25nA max (AD517L)
Low V_{OS}: 50μV max (AD517L), 150μV max (AD517J)
Low V_{OS} Drift: 1.3μV/°C (AD517L)
Internal Compensation

AD517 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD517 is a high accuracy monolithic op amp featuring extremely low offset voltages and input currents. Analog Devices' thermally-balanced layout and superior IC processing combine to produce a truly precision device at low cost.

The AD517 is laser trimmed at the wafer level (LWT) to produce offset voltages less than 50μV and offset voltage drifts less than 1.3μV/°C unnulled. Superbeta input transistors provide extremely low input bias currents of 1nA max and offset currents as low as 0.25nA max. While these figures are comparable to presently available BIFET amplifiers at room temperature, the AD517 input currents decrease, rather than increase, at elevated temperatures. Open-loop gain in many IC amplifiers is degraded under loaded conditions due to thermal gradients on the chip. However, the AD517 layout is balanced along a thermal axis, maintaining open-loop gain in excess of 1,000,000 for a wide range of load resistances.

The input stage of the AD517 is fully protected, allowing differential input voltages of up to $\pm V_S$ without degradation of gain or bias current due to reverse breakdown. The output stage is short-circuit protected and is capable of driving a load capacitance up to 1000pF.

The AD517 is well suited to applications requiring high precision and excellent long-term stability at low cost, such as stable references, followers, bridge instruments and analog computation circuits.

The circuit is packaged in a hermetically sealed TO-99 metal can, and is available in three performance versions (J, K, and L) specified over the commercial 0 to +70°C range; and one version (AD517S) specified over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Offset voltage is 100% tested and guaranteed on all models.
2. The AD517 exhibits extremely low input bias currents without sacrificing CMRR (over 100dB) or offset voltage stability.
3. The AD517 inputs are protected (to $\pm V_S$), preventing offset voltage and bias current degradation due to reverse breakdown of the input transistors.
4. Internal compensation is provided, eliminating the need for additional components (often required by high accuracy IC op amps).
5. The AD517 can directly replace 725, 108, and AD510 amplifiers. In addition, it can replace 741-type amplifiers if the offset-nulling potentiometer is removed.
6. Thermally-balanced layout insures high open-loop gain independent of thermal gradients induced by output loading, offset nulling, and power supply variations.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

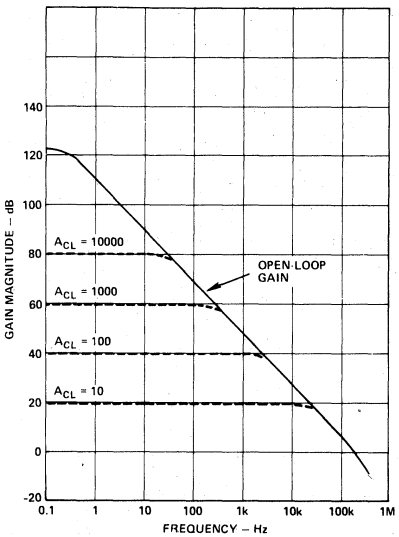
Model	AD517J			AD517K			AD517L			AD517S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**10^6**			**10^6**			**10^6**			**10^6**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	500,000			500,000			500,000			**250,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**			**±10**			**±10**			**±10**			V
Load Capacitance		1000			1000			1000			1000		pF
Output Current	10			10			10			10			mA
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		250			250			250			250		kHz
Full Power Response		1.5			1.5			1.5			1.5		kHz
Slew Rate, Unity Gain		0.10			0.10			0.10			0.10		V/μs
INPUT OFFSET VOLTAGE													
Initial Offset			**150**			**75**			**50**			**75**	μV
Input Offset vs. Temp.			**3.0**			**1.8**			**1.3**			**1.8**	μV/°C
Input Offset vs. Supply			**25**			**10**			**10**			**10**	μV/V
T_{min} to T_{max}			**40**			15			15			**20**	μV/V
INPUT BIAS CURRENT													
Initial			**5**			**2**			**1.0**			**2.0**	nA
T_{min} to T_{max}			8			3.5			1.5			**10**	nA
vs. Temp, T_{min} to T_{max}			±20			±10			±4			±10	pA/°C
INPUT OFFSET CURRENT													
Initial			**1.0**			**0.75**			**0.25**			**2.0**	nA
T_{min} to T_{max}			1.5			1.25			0.4			**10**	nA
INPUT IMPEDANCE													
Differential		15‖1.5			20‖1.5			20‖1.5			20‖1.5		MΩ‖pF
Common Mode		$2.0 \times 10''$			$2.0 \times 10''$			$2.0 \times 10''$			$2.0 \times 10''$		Ω
INPUT VOLTAGE RANGE													
Differential		$\pm V_S$			$\pm V_S$			$\pm V_S$			$\pm V_S$		V
Common Mode Rejection	**94**			**110**			**110**			**110**			dB
Common Mode Rejection													
T_{min} to T_{max}	94			110			100			**100**			dB
INPUT NOISE													
Voltage, 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		$nV/\sqrt{Hz}$
f = 100Hz		25			25			25			25		$nV/\sqrt{Hz}$
f = 1kHz		20			20			20			20		$nV/\sqrt{Hz}$
Current, f = 10kHz		0.05			0.05			0.05			0.05		$pA/\sqrt{Hz}$
f = 100Hz		0.03			0.03			0.03			0.03		$pA/\sqrt{Hz}$
f = 1kHz		0.03			0.03			0.03			0.03		$pA/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**4**			**3**			**3**			**3**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[1]													
TO-99 Style (H08B)		AD517JH			AD517KH			AD517LH			AD517SH		

NOTES

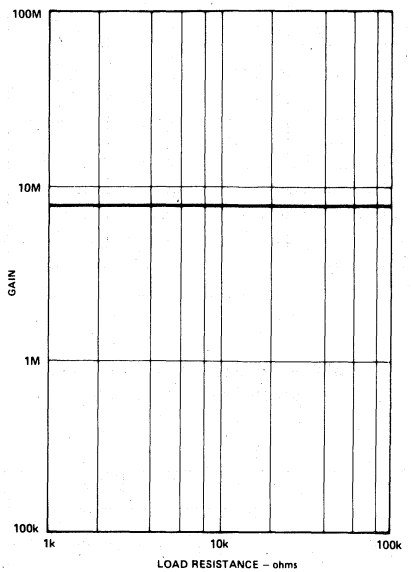
[1]See Section 19 for package outline information.

Specifications subject to change without notice.

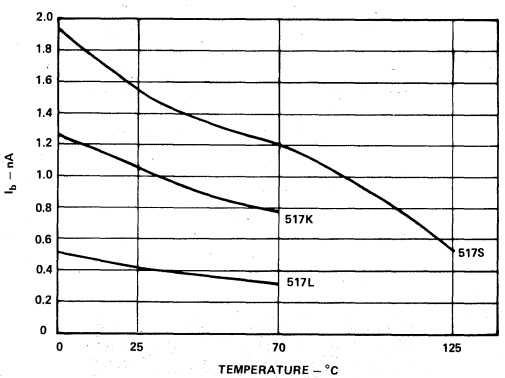
Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



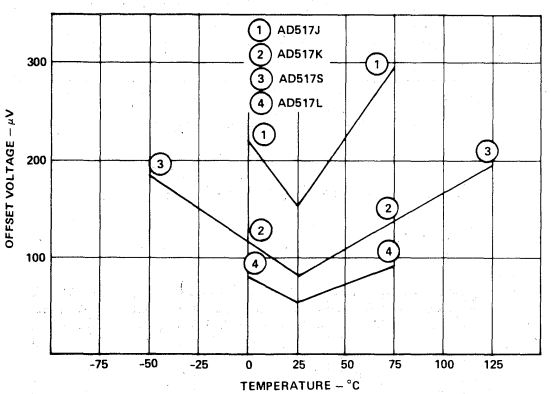
Small-Signal Gain vs. Frequency



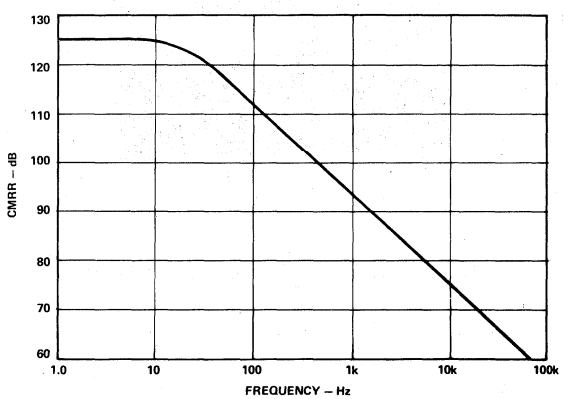
Open-Loop Gain vs. Load Resistance



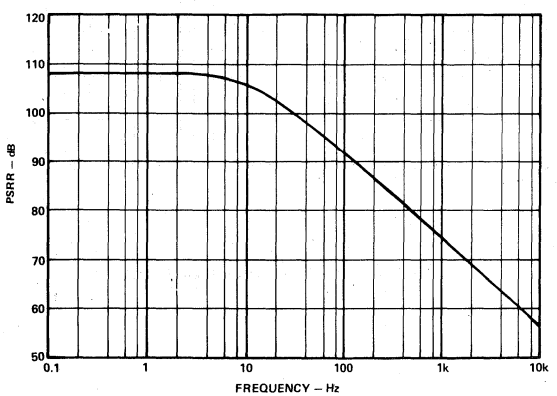
Input Bias Current vs. Temperature



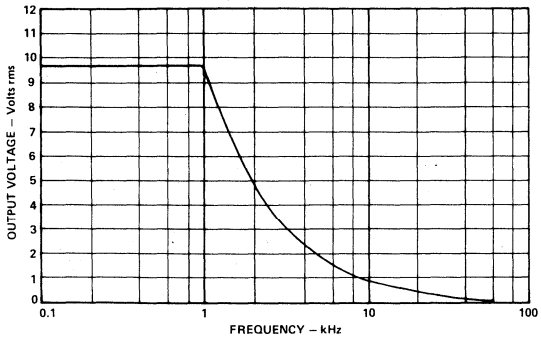
Untrimmed Offset Voltage vs. Temperature



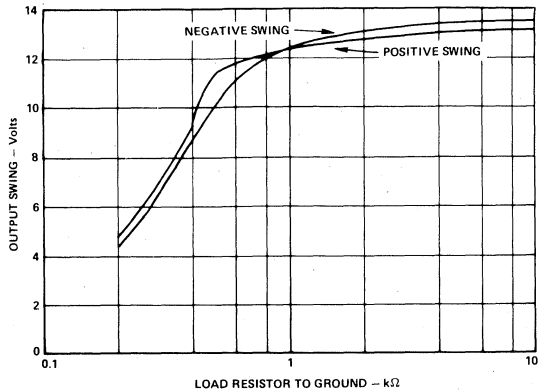
CMRR vs. Frequency



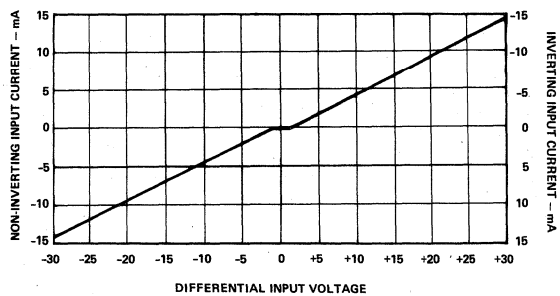
PSRR vs. Frequency



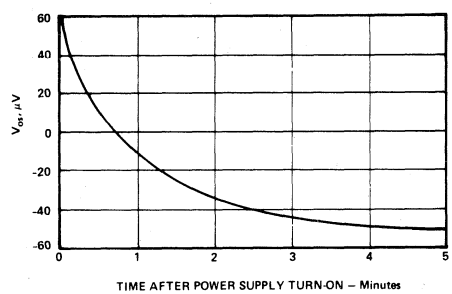
Maximum Undistorted Output vs. Frequency (Distortion ⩽ 1%)



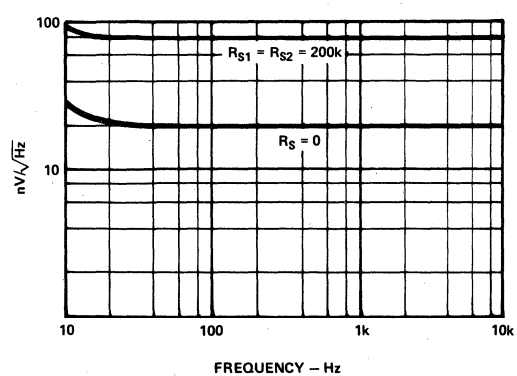
Output Voltage vs. Load Resistance



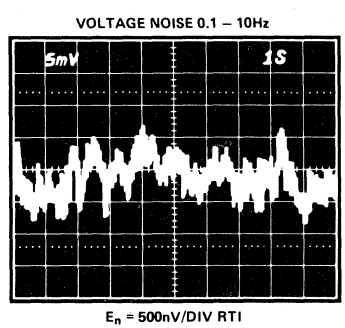
Input Current vs. Differential Input Voltage



Warm-Up Offset Voltage Drift



Total Input Noise Voltage vs. Frequency



Low Frequency Voltage Noise (0.1 to 10Hz)

NULLING THE AD517

The internally-trimmed offset voltage of the AD517 will be low enough for most circuits without further nulling. However, in high precision applications, the AD517 may be nulled using either of the following methods:

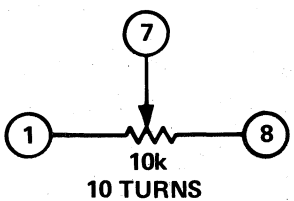
Figure 1A shows a simple circuit using a 10kΩ, ten-turn potentiometer. This circuit allows nulling to within several microvolts.

The circuit of Figure 1B is recommended in applications where nulling to within 1μV is desired. This circuit has the advantage that potentiometer instability effects are reduced by a factor of ten. Values of R_1' and R_2' are calculated as follows:

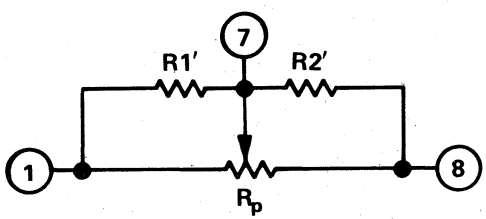
1. Null the offset to zero using a standard 10k pot, as shown in Figure 1A.
2. Measure pot halves R_1 and R_2.
3. Calculate:

$$R_1' = \frac{R_1 \times 50k\Omega,}{50k\Omega - R_1} \qquad R_2' = \frac{R_2 \times 50k\Omega}{50k\Omega - R_2}$$

4. Replace the pot with R_1' and R_2' using the closest value 1% metal film resistors.
5. Use a 100k, ten-turn pot for R_p to complete the nulling.



A. Simple



B. High Precision

Figure 1. Nulling Circuits

AN INSTRUMENT INPUT AMPLIFIER USING THE AD517L

The circuit shown in Figure 2 represents a typical input stage for laboratory instruments and panel meters. The amplifier is non-inverting and offers selectable gains from 1 to 1000 in decade steps.

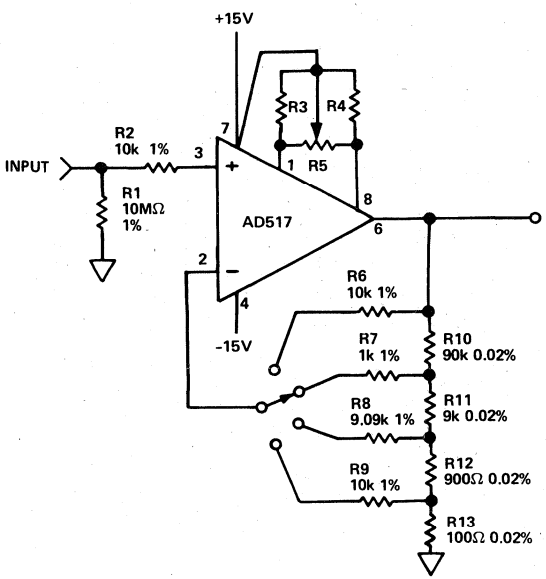


Figure 2. Stable Instrument Input Amplifier

Input impedance of this amplifier is 10 megohms, determined by resistor R_1. The offset nulling network comprised of R_3, R_4 and R_5 is the same one described earlier. If a less precise adjustment can be tolerated, a single 10k potentiometer can be substituted for R_3, R_4 and R_5.

Gain switching is accomplished in the feedback network. The divider consisting of R_{10}, R_{11}, R_{12} and R_{13} determines the gain by dividing the output and returning it to the inverting input of the amplifier. The ratio tolerances of these resistors uniquely determine the gain of the amplifier. The impedance seen by the inverting input is held constant at 10k ohms by R_6, R_7 R_8 or R_9 depending on the gain selected. Since input bias currents flow through equal resistances, the offset voltages produced will cancel each other. The input offset currents will produce an insignificant offset voltage on the order of 1 microvolt. If this offset is nulled out at the highest gain selected, it will be nulled on all ranges.

The AD517 offers excellent temperature stability in this circuit. Once the offset has been zeroed, the error produced by offset current drift will remain quite low due to the extremely low offset current drift of the AD517. A FET-input op amp would not work well in this application, since the input offset currents would double for each 10°C increase in temperature, soon exceeding the input offset currents of the AD517.

ANALOG DEVICES

Low Cost, High Speed, IC Operational Amplifier

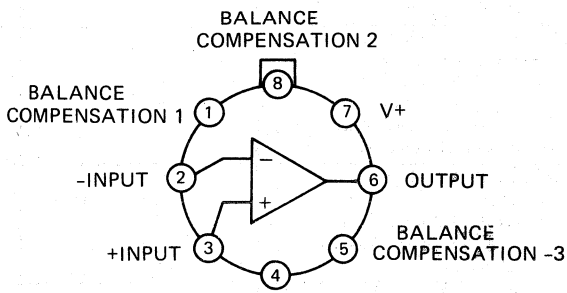
AD518

4

FEATURES

- High Slew Rate: 70V/μs
- Wide Bandwidth: 12MHz
- 60° Phase Margin (At Unity Gain Crossover)
- Drives 300pF Load
- Guaranteed Low Offset Drift:
  15μV/°C Max (AD518K)
- Pin Compatible With 118-Type
  Op Amp Series

AD518 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD518J, AD518K, and AD518S are high speed precision monolithic operational amplifiers designed for applications where slew rate and wide bandwidth are required, but low cost and ease of use are essential. The devices are internally compensated for unity gain applications with a 60° phase margin to insure stability, a minimum unity gain slew rate of 50V/μs, and a typical bandwidth of 12MHz. In addition, in inverting applications external feedforward compensation may be added to increase the slew rate to over 100V/μs, and nearly double the bandwidth. If desired, settling time to 0.1% can be reduced to under 1μs with a single external capacitor.

The AD518's dc performance is consistent with its precision dynamic characteristics. The devices feature offset voltages below 2mV, maximum offset drifts of 15μV/°C, and offset currents below 50nA max.

The high slew rate, fast settling time, ease of use, and low cost of the AD518 make it ideal for use with D/A and A/D converters, as well as active filters, sample-and-hold circuits, and as a general purpose, fast, wideband amplifier. The AD518 is supplied in the TO-99 package. The AD518J and AD518K are specified for operation over the 0 to +70°C temperature range; the AD518S for operation from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD518 offers the user high speed performance and flexibility previously unavailable at low cost . . . . . .
   - Internal compensation for unity gain applications
   - Capability to increase slew rate to over 100V/μs and double the bandwidth by an external feedforward technique
   - Capability to reduce settling time to under 1μs to 0.1% with a single external capacitor
   - Differential input capability
2. The phase margin of the AD518, uncompensated at the unity gain crossover frequency, is 60°, providing unconditional stability for all conditions. This conservative phase margin represents a clear improvement over that of the 118 series IC op amps currently available.
3. The static performance of the AD518 is consistent with its excellent dynamic performance, providing offset voltage drift under 15μV/°C, CMRR of 80dB, and offset current below 50nA.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc unless otherwise specified)

Model	AD518J Min	AD518J Typ	AD518J Max	AD518K Min	AD518K Typ	AD518K Max	AD518S Min	AD518S Typ	AD518S Max	Units
OPEN LOOP GAIN										
V_O = ±10V, $R_L \geq 2k\Omega$	**25,000**	100,000		**50,000**	100,000		**50,000**	100,000		V/V
T_{min} to T_{max}, R_L = 2kΩ	20,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 2kΩ, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		V
Output Current		±10			±10			±10		mA
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain Small Signal		12			12			12		MHz
Slew Rate, Unity Gain	50	70		50	70		50	70		V/μs
Settling Time to 0.1%		800			800			800		ns
Phase Margin, Uncompensated at Unity Gain Crossover Frequency		60			60			60		Degrees
INPUT OFFSET VOLTAGE										
Initial Offset		4	**10**		2	**4**		2	**4**	mV
Input Offset Voltage or T_{min} to T_{max}			15			**6**			**6**	mV
Input Offset Voltage vs. Supply or T_{min} to T_{max}	**65**	80		**80**	90		**80**	90		dB
INPUT BIAS CURRENT										
Initial		120	**500**		120	**250**		120	**250**	nA
T_{min} to T_{max}			750			**400**			**400**	nA
INPUT OFFSET CURRENT										
Initial		30	**200**		6	**50**		6	**50**	nA
T_{min} to T_{max}			300			**100**			**100**	nA
INPUT IMPEDANCE	0.5	3.0		0.5	3.0		0.5	3.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential		±11.5			±11.5			±11.5		V
Common Mode		±V_S			±V_S			±V_S		V
Common Mode Rejection	**70**	100		**80**	100		**80**	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15	**±18**	V
Operating	±5		**±20**	±5		**±20**	±5		**±20**	V
Quiescent Current		5	**10**		5	**7**		5	**7**	μA
TEMPERATURE RANGE										
Operating, Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C
PACKAGE[2]										
TO-99 Style (H08A)		AD518JH			AD518KH			AD518SH		
Plastic MINI DIP (N8A)		AD518JN			AD518KN					

NOTES

[1]The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA

[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STABILITY & PHASE MARGIN

Perhaps one of the most meaningful ways to express the relative stability of a closed loop amplifier is in terms of phase margin. Phase margin is measured at that frequency where the open loop gain of the amplifier becomes unity or 0dB. It is the additional amount of phase shift that, if introduced in the loop, would make the loop unstable.

At very low frequencies the gain of most operational amplifiers is generally large. Moreover, the amplifier output signal is very nearly in phase with the differential input signal. This output is, therefore, nearly 180° out of phase with the feedback signal applied to the inverting input. At sufficiently high frequencies the gain of the amplifier begins to decrease as a function of frequency, with the resulting consequence of a lagging phase characteristic. That is, as the gain falls with increasing frequency, the phase of the output signal at a given frequency will lag the phase of the input signal. The phase shift depends most critically on the slope of the gain curve with respect to the logarithm of the frequency at the frequency where the phase is measured. If the gain changes more rapidly than 12dB/octave over a substantial frequency range, the minimum resulting phase shift may exceed 180°.

To insure amplifier stability, it is necessary that the phase shift near the unity gain frequency (12MHz in the AD518) is less than 180°. Moreover, it is generally required that the phase shift be substantially below the critical stability point to insure proper system performance. If the unity gain phase shift approaches 180°, the system will be on the verge of oscillation. As a result, there will be a large peak in the closed loop response near the unity loop gain frequency. This sharply peaked frequency response generally causes an undesirable small signal transient response with a poorly damped overshoot.

The term *phase margin* refers to the difference between 180° and the actual frequency-dependent phase shift at the system unity gain frequency. It is the margin between the actual system phase shift and the critical phase shift at which oscillation will occur. Not only does it indicate the relative immunity to oscillation, but it also gives some indication about the peaking and overshoot that can be expected.

The simple pole or frequency response of a single R-C network has a gain slope of 6dB/octave. This response has an associated phase shift which is asymptotic to −90°. Linear systems which are dominated by this characteristic in their open loop response are stable. They show no overshoot or ringing in their small signal transient response. Additional poles, either above or below the unity loop gain frequency, will add phase shift. As phase shift increases up to a lagging phase of about 120°, representing a 60° phase margin, little or no peaking will result. As the unity gain phase shift increases, peaking becomes more and more evident. For example, as the phase shift reaches 160° (20° of phase margin), between 9 and 10dB of peaking will occur.

The AD518 has been designed for a 60° phase margin at the unity gain crossover frequency, for absolute stability and absence of ringing and overshoot. (Note the transient response of the AD518 in Figure 1.) Note also in Figure 2 that the phase shift at 12MHz, the unity gain crossover frequency, is 120°, representing 60° of phase margin.

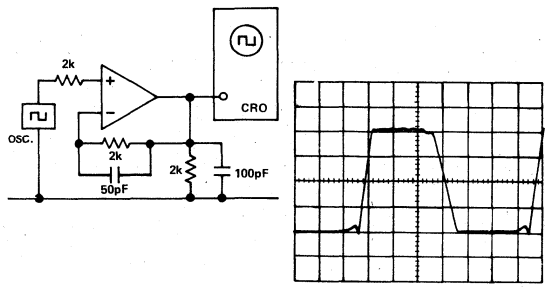


Figure 1. Transient Response of the AD518

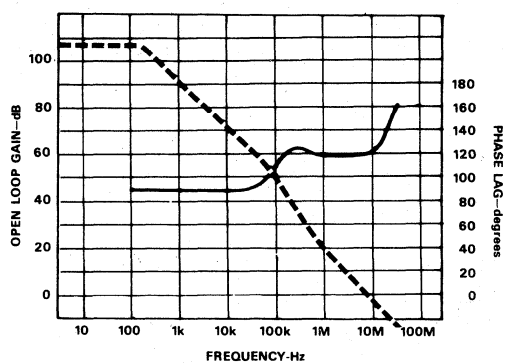


Figure 2. Amplitude and Phase Response of the AD518

THE FLEXIBILITY OF THE AD518

MINIMUM SETTLING TIME APPLICATIONS

For applications where a minimum settling time is desired, the settling time of the AD518 may be reduced significantly by employing the compensation scheme suggested in Figure 3.

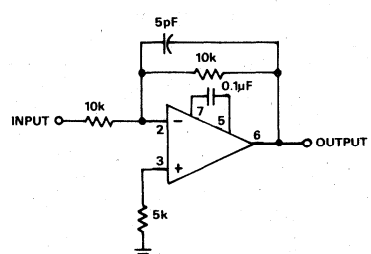


Figure 3. Minimum Settling Time Compensation

Using the 0.1μF capacitor from Pin 5 to V+ (Pin 7), the settling time to 0.1% is reduced from 2μs to 800ns.

HIGHER BANDWIDTH OR
HIGHER SLEW RATE APPLICATIONS

For applications where higher bandwidth is desired, the bandwidth of the AD518 may be increased to nearly 25MHz by using the feedforward technique shown in Figure 4.

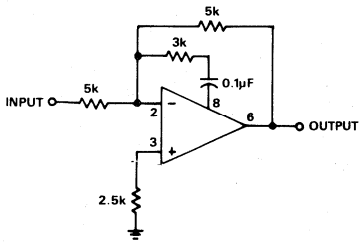


Figure 4. High Bandwidth Configuration

For applications where higher slew rate is desired, the slew rate of the AD518 may be nearly doubled using the technique shown in Figure 5.

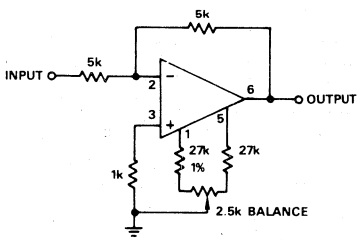


Figure 5. High Slew Rate Configuration

Note that the techniques of Figures 4 and 5 may be used in conjunction with each other to both double the bandwidth to 25MHz and increase the slew rate to 100–140V/μs.

USING THE AD518

The connection scheme employed when using the AD518 is considerably more important than for low frequency, general purpose amplifiers. The primary purpose of the 0.1μF bypass capacitors shown in Figure 6 is to convert the distributed high frequency ground to a lumped single point (the V+ point). The V+ to V− 0.1μF capacitor equalizes the supply grounds, while the 0.1μF capacitor from V+ to signal ground should be returned to signal common. This signal common, which is bypassed to pin 7, is defined as that point at which the input signal source, the feedback network, and the return side of the load are joined to the power common.

When using the AD518, this decoupling configuration should be used in conjunction with the configuration of Figures 3, 4 and 5, depending on the specific application.

Note that the diagram shows each individual capacitor directly connected to the appropriate terminal. In addition, it is suggested that all connections be made short and direct, and as physically close to the can as possible, so that the length of any conducting path shared by external components will be minimized.

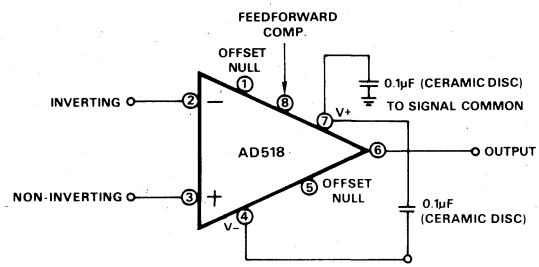
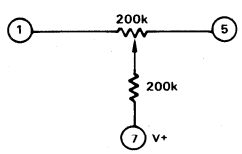


Figure 6. General Purpose Connection Diagram

NULLING THE AD518



OTHER IC HIGH SPEED AMPLIFIERS AVAILABLE

AD507	35MHz Gain Bandwidth Slew Rate of 25V/μs min Bias Current of 15nA max Offset Voltage Drift of 15μV/°C max
AD509	Settles to 0.01% in 1μs Settles to 0.1% in 200ns Slew Rate of 100V/μs min

ANALOG DEVICES

Precision Low Cost BIFET Op Amp

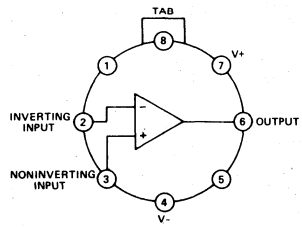
AD542

4

FEATURES

- Low Bias Current: 25pA max, warmed-up (AD542K,L), 50pA max (AD542J)
- Low Offset Voltage: 0.5mV max (AD542L), 1.0mV max (AD542K)
- Low Offset Voltage Drift: 5μV/°C max (AD542L), 10μV/°C max (AD542K) 20μV/°C max (AD542J)
- Low Quiescent Current: 1.5mA max
- Low Price

AD542 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD542 is a precision, monolithic FET-input operational amplifier fabricated with the most advanced BIFET and laser trimming technologies. The AD542 offers bias currents significantly lower than currently available BIFET devices: 25pA max, warmed-up for the AD542K and L, 50pA max for the AD542J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD542L and 1.0mV on the AD542K utilizing Analog's exclusive laser-wafer-trimming (LWT) process. When combined with the AD542's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing BIFET op amps – and at low, BIFET pricing.

The key to BI-FET technology is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. Analog Devices optimizes the BIFET process to produce bias currents lower than other popular BIFET op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1 – 10Hz), and low quiescent current.

The AD542 is recommended for any operational amplifier application requiring excellent dc performance at low and moderate costs. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's excellent combination of low offset voltage and drift, low bias current and low 1/f noise. High common mode rejection (80dB, min on the "K" and "L" versions) and high open-loop gain—even under heavy loading—ensures better than "12-bit" linearity in high impedance buffer applications. Additionally, bandwidth and slew rate are much increased over presently available precision, bipolar op amps.

The AD542 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C extended operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved BIFET processing on the AD542 results in the lowest bias current available in a BIFET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD542 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD542L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (Offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift enhance the AD542's performance as a precision op amp.
6. The 1.5mA max quiescent current enables the device to be used in numerous portable applications where low battery drain is essential. This is achieved without sacrificing open loop gain or the ability to drive up to a 10mA load.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD542J			AD542K			AD542L			AD542S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[2]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage vs. Temp.			**20**			**10**			5			**15**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT													
Either Input[3]			**50**			**25**			**25**			**25**	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		70			70			70			70		$nV/\sqrt{Hz}$
f = 100Hz		45			45			45			45		$nV/\sqrt{Hz}$
f = 1kHz		30			30			30			30		$nV/\sqrt{Hz}$
f = 10kHz		25			25			25			25		$nV/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**1.5**			**1.5**			**1.5**			**1.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD542JH			AD542KH			AD542LH			AD542SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

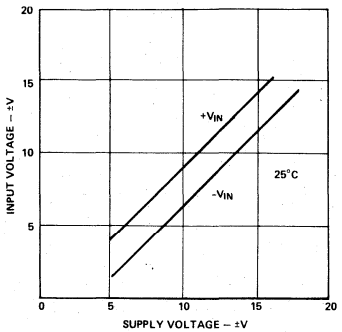


Figure 1. Input Voltage Range vs. Supply Voltage

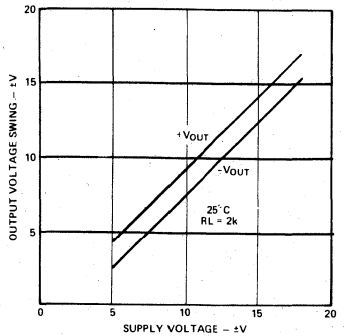


Figure 2. Output Voltage Swing vs. Supply Voltage

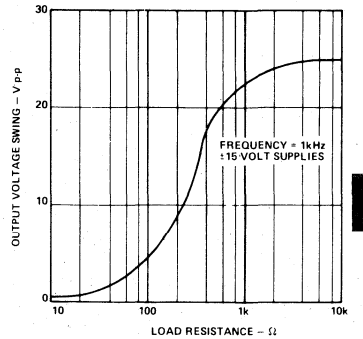


Figure 3. Output Voltage Swing vs. Resistive Load

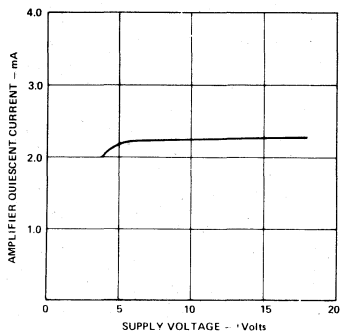


Figure 4. Quiescent Current vs. Supply Voltage

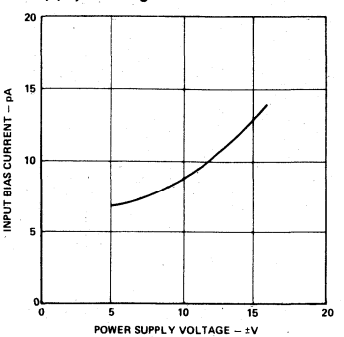


Figure 5. Input Bias Current vs. Supply Voltage

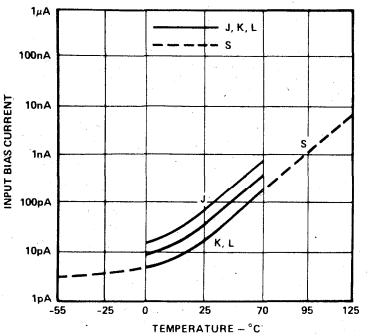


Figure 6. Input Bias Current vs. Temperature

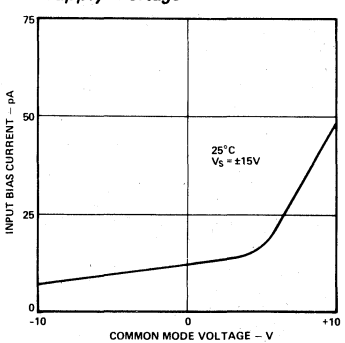


Figure 7. Input Bias Current vs. CMV

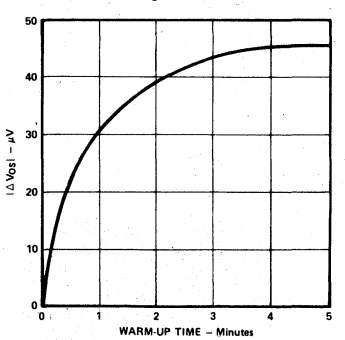


Figure 8. Input Offset Voltage Turn On Drift vs. Time

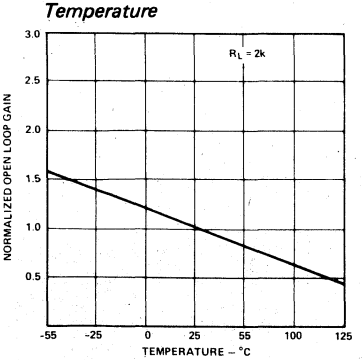


Figure 9. Open Loop Gain vs. Temperature

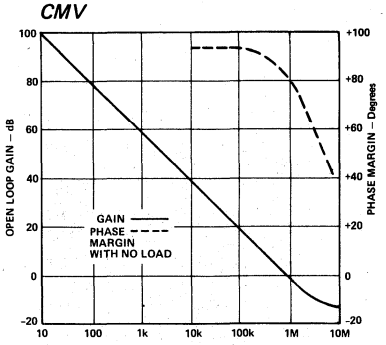


Figure 10. Open Loop Frequency Response

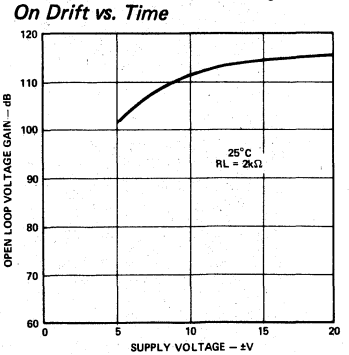


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

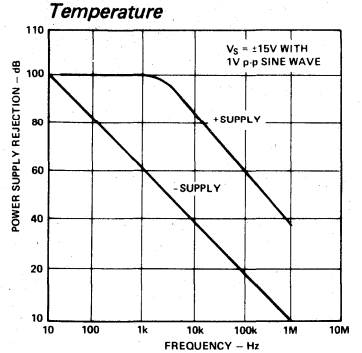


Figure 12. Power Supply Rejection vs. Frequency

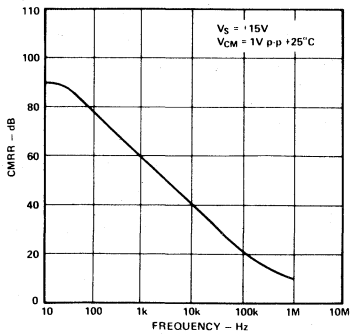


Figure 13. Common Mode Rejection vs. Frequency

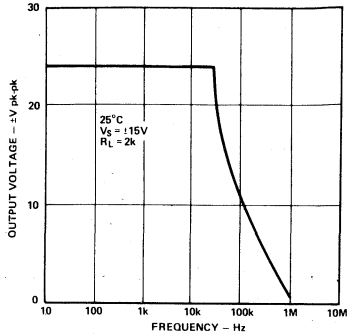


Figure 14. Large Signal Frequency Response

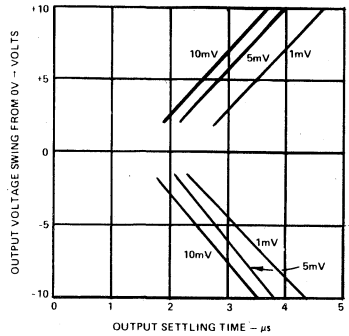


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

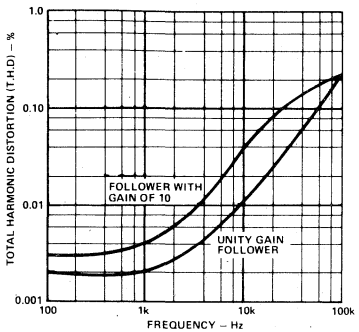


Figure 16. Total Harmonic Distortion vs. Frequency

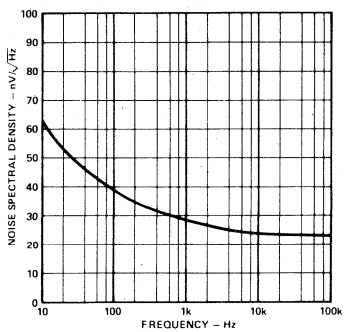


Figure 17. Input Noise Voltage Spectral Density

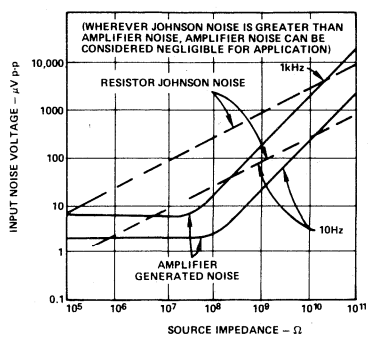
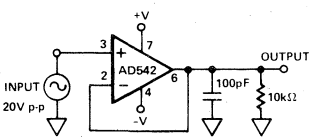
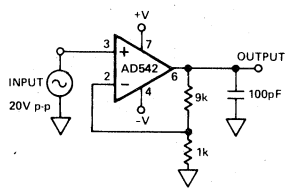


Figure 18. Total Noise vs. Source Resistance

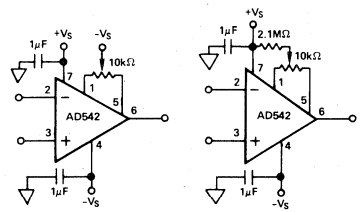


a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits



a. Standard Null Circuit b. Null to +V_S

Figure 20. Offset Voltage Null Circuits

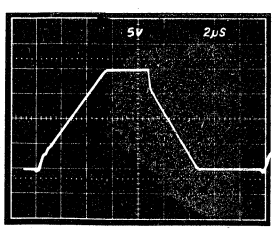


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

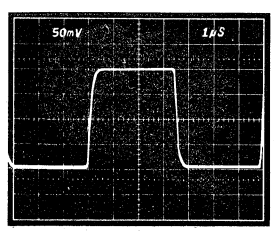


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

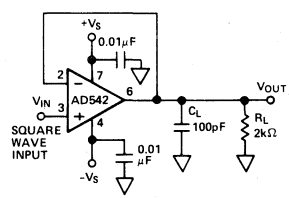


Figure 21c. Unity Gain Follower

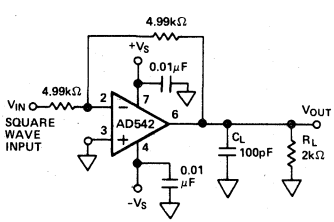


Figure 22a. Unity Gain Inverter

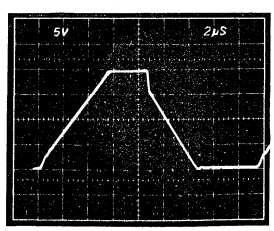


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

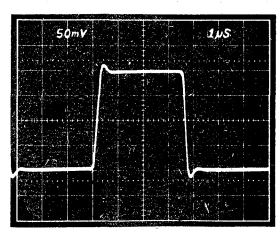


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

High Speed Implanted FET-Input Op Amp

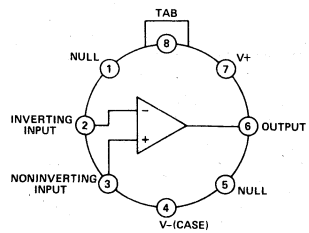
AD544

4

FEATURES

Low Bias Current: 25pA max, warmed-up
Low Offset Voltage: 500μV max
Low Offset Voltage Drift: 5μV/°C max
Low Input Voltage Noise: 2μV p-p
Low Quiescent Current: 2.5mA max
High Slew Rate: 13V/μs
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0015% at 1kHz

AD544 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD544 is a high speed monolithic FET-input operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD544 offers bias currents significantly lower than currently available monolithic FET-input devices: 25pA max, warmed-up for the AD544K and L, 50pA max for the AD544J. In addition, the offset voltage is laser trimmed to less than 0.5mV on the AD544L and 1.0mV on the AD544K utilizing Analog's laser-wafer-trimming (LWT) process. When combined with the AD544's low offset voltage drift (5μV/°C max for "L", 10μV/°C max for "K"), these features offer the user IC performance truly superior to existing FET-input op amps—and at low, monolithic pricing.

The key technology required for monolithic JFET-input op amps is the ion-implanted JFET. Ion-implantation (as opposed to diffusion) permits the fabrication of precision, matched JFET's on a monolithic bipolar chip. Analog Devices optimizes the process to produce bias currents lower than other popular FET-input op amps and specifies each device for the maximum value at either input in the fully warmed-up condition. Additional benefits of this optimization include low voltage noise (2μV p-p, 0.1—10Hz), and low quiescent current.

The AD544 is recommended for any operational amplifier application requiring excellent ac and dc performance at low cost. The 2MHz bandwidth and low offset of the AD544 make it an excellent choice as an output amplifier for current output D/A Converters such as the AD7541, 12-Bit CMOS DAC. High common mode rejection (80dB, min on the "K" and "L" versions) and open-loop gain ensures better than "12-bit" linearity in high impedance buffer applications.

The AD544 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. Improved bipolar and JFET processing on the AD544 results in the lowest bias current available in a high speed monolithic FET op amp.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD544 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max (AD544L), thus eliminating the need for external nulling in many situations.
4. If offset nulling is required, the additional offset voltage drift induced will be minimal. (In some devices, offset voltage drift can increase an additional 3μV/°C per mV of offset nulled.)
5. Low voltage noise (2μV, p-p), and low offset voltage drift (5μV/°C) enhance the AD544's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD544 ideal for D/A, A/D, sample-hold circuits and high speed integrators.
7. Low harmonic distortion (0.0015%) makes the AD544 an ideal choice for audio applications.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD544J			AD544K			AD544L			AD544S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
V_O = ±10V, $R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	20,000			40,000			40,000			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	8.0	13.0		8.0	13.0		8.0	13.0		8.0	13.0		V/µs
Settling Time to 0.01%		3.0			3.0			3.0			3.0		µs
Total Harmonic Distortion		0.0025			0.0025			0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage vs. Temp. or T_{min} to T_{max}			**20**			**10**			**5**			**15**	µV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	µV/V
INPUT BIAS CURRENT[3]													
Either Input		10	**50**		10	**25**		10	**25**		10	**25**	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential[4]		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**74**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		µV p-p
f = 10Hz		35			35			35			35		$nV/\sqrt{Hz}$
f = 100Hz		22			22			22			22		$nV/\sqrt{Hz}$
f = 1kHz		18			18			18			18		$nV/\sqrt{Hz}$
f = 10kHz		16			16			16			16		$nV/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.8	**2.5**		1.8	**2.5**		1.8	**2.5**		1.8	**2.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD544JH			AD544KH			AD544LH			AD544SH			

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

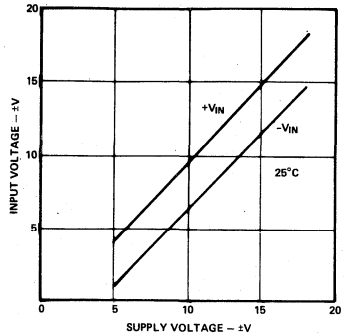


Figure 1. Input Voltage Range vs. Supply Voltage

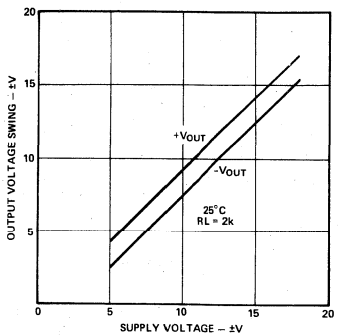


Figure 2. Output Voltage Swing vs. Supply Voltage

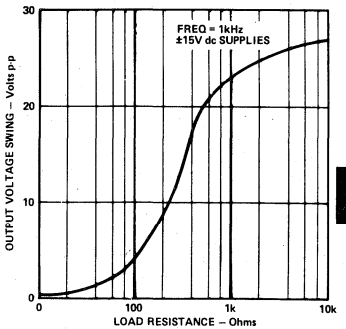


Figure 3. Output Voltage Swing vs. Resistive Load

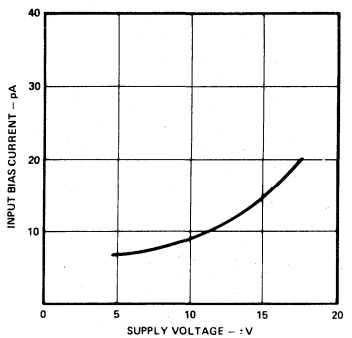


Figure 4. Input Bias Current vs. Supply Voltage

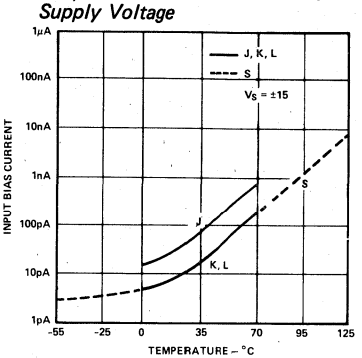


Figure 5. Input Bias Current vs. Temperature

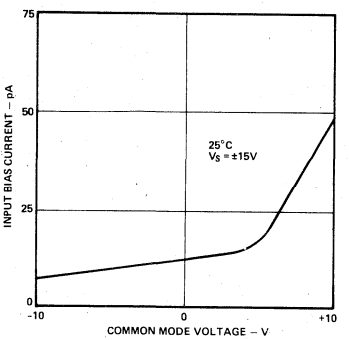


Figure 6. Input Bias Current vs. CMV

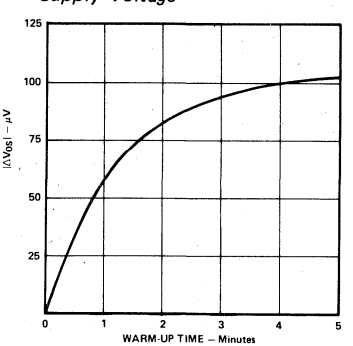


Figure 7. Change in Offset Voltage vs. Warm-Up Time

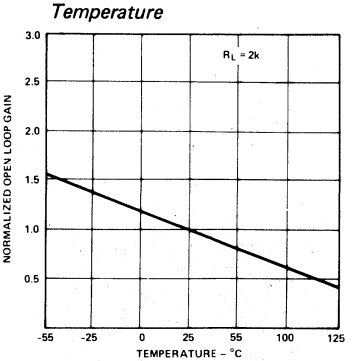


Figure 8. Open Loop Gain vs. Temperature

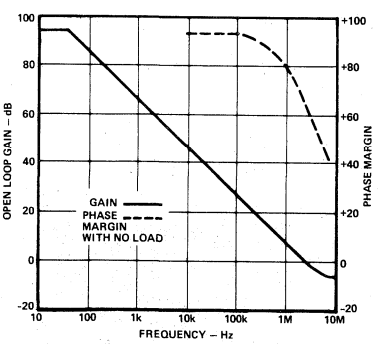


Figure 9. Open Loop Frequency Response

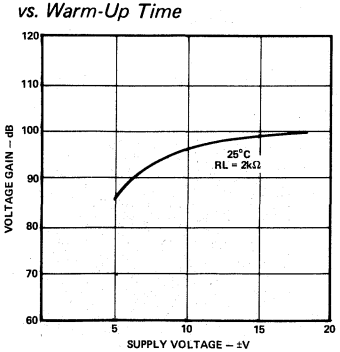


Figure 10. Open Loop vs. Voltage Gain vs. Supply Voltage

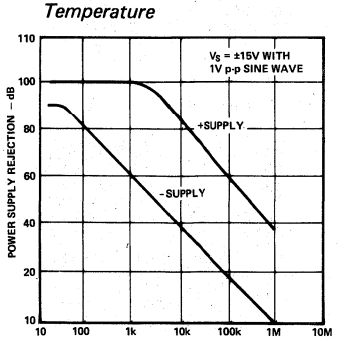


Figure 11. Power Supply Rejection vs. Frequency

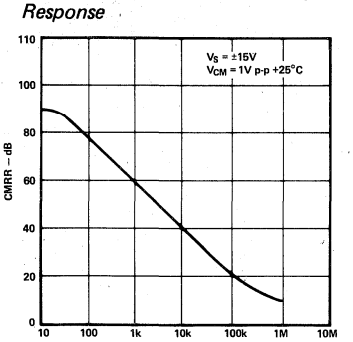


Figure 12. Common Mode Rejection Ratio vs. Frequency

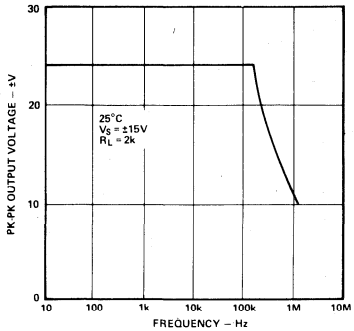


Figure 13. Large Signal Frequency Response

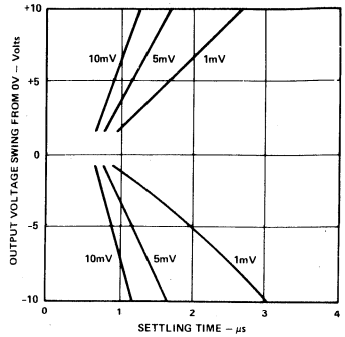


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

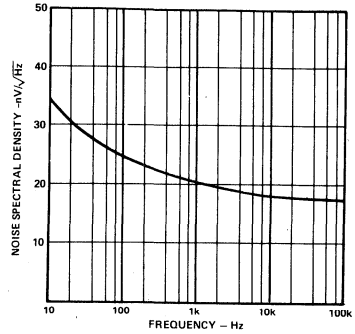


Figure 15. Noise Spectral Density

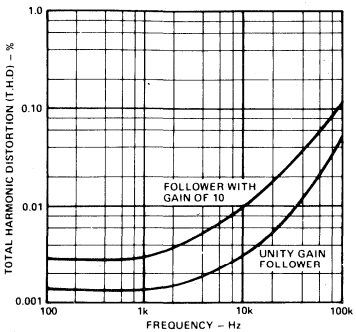


Figure 16. Total Harmonic Distortion vs. Frequency

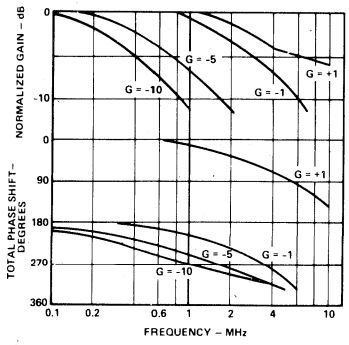


Figure 17. Closed Loop Gain & Phase vs. Frequency

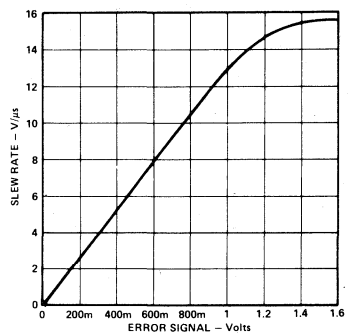
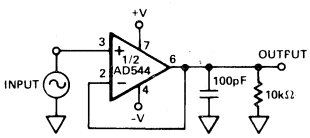
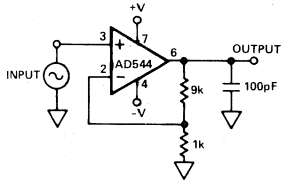


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

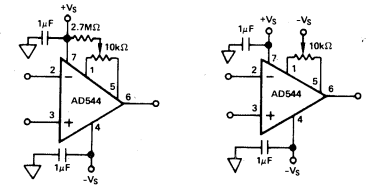


Figure 20. Offset Null Configuration

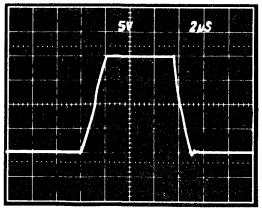


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

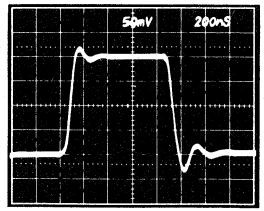


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

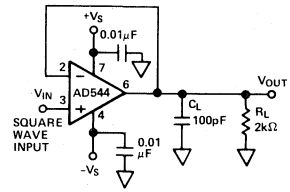


Figure 21c. Unity Gain Follower

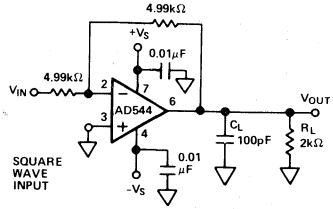


Figure 22a. Unity Gain Inverter

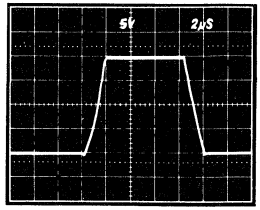


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

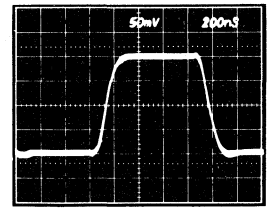


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

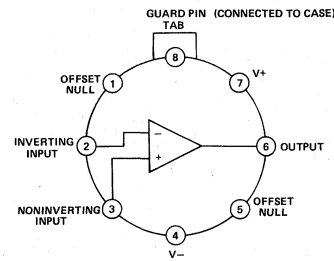
Precision, Low Drift FET-Input Op Amp

AD545

FEATURES

Low Offset Voltage: 0.5mV max (AD545L), 0.25mV max (AD545M)
Low Offset Voltage Drift: 5μV/°C max (AD545L), 3μV/°C max (AD545M)
Low Power: 1.5mA max
Low Bias Current: 1pA max (AD545K, L, M)
Low Noise: 3μV p-p, 0.1 to 10Hz

AD545 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD545 is a precision FET-input operational amplifier with overall performance far superior to the general purpose IC FET-input op amp. The device is fabricated using a low leakage FET paired with a low power op amp. Bias current is specified as 2pA max for the AD545J and 1pA max for the AD545K, L and M. Offset voltage is laser trimmed to 0.5mV max for the AD545L, 0.25mV max for the AD545M. All devices also feature low voltage noise and power consumption. The AD545 is internally compensated, short circuit protected and free of latch-up.

The AD545 series offers a broad combination of performance features previously unavailable from a single device. For precision applications the AD545M specifies a 0.25mV max offset voltage, 3μV/°C max drift and 1pA max bias current. The AD545J, with a 1mV max offset voltage, 25μV/°C max drift and 2pA max bias current, is the best price performance choice.

These devices are recommended for a variety of general purpose and precision applications requiring low bias currents and high input impedance such as pH/plon sensitive electrodes, photo-current detectors, biological microprobes, long term precision integrators and vacuum iongauge measurements. The versatility of the AD545 is further enhanced by its excellent low frequency noise (3μV p-p, 0.1 to 10Hz) and low power consumption (1.5mA max) for portable applications.

As with previous electrometer amplifier designs from Analog Devices, the case is guarded thus minimizing stray leakage. This feature will also shield the input circuitry from external noise and supply transients, as well as reducing common mode input capacitance from 0.8pF to 0.2pF.

The AD545 is available in four versions of bias current and offset voltage, the "J", "K", "L", and "M". All are specified from 0 to +70°C and supplied in a hermetically sealed TO-99 package.

PRODUCT HIGHLIGHTS

1. The offset voltage on the AD545 is laser trimmed to a level typically less than 250μV. Offset voltage drift is significantly lower than previously available FET-input devices (3μV/°C max for the AD545M). If additional external nulling is desired, the effect on drift is minimal (approximately 3μV/°C per millivolt, nulled).
2. Bias current is specified as the maximum measured at either input with the device fully warmed up on ±15V supplies at +25°C ambient.
3. The low quiescent current drain of 0.8mA typical, and 1.5mA max, is among the lowest of any IC op amp and keeps self heating to a minimum.
4. The combination of low input noise voltage and very low input noise current is such that for source impedances from much over one megohm up to 10^{11} ohm, the Johnson noise of the source will easily dominate the noise characteristics.

SPECIFICATIONS (typical @ +25°C with V_S = ±15V dc, unless otherwise specified)

MODEL	AD545J	AD545K	AD545L	AD545M
OPEN LOOP GAIN[1]				
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000V/V min	40,000V/V min	40,000V/V min	40,000V/V min
$R_L \geq 10k\Omega$	40,000V/V min	50,000V/V min	50,000V/V min	50,000V/V min
T_A = min to max $R_L \geq 2k\Omega$	15,000V/V min	25,000V/V min	40,000V/V min	40,000V/V min
OUTPUT CHARACTERISTICS				
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)	*	*	*
@ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)	*	*	*
Load Capacitance[2]	500pF	*	*	*
Short Circuit Current	10mA min (25mA typ)	*	*	*
FREQUENCY RESPONSE				
Unity Gain, Small Signal	700kHz	*	*	*
Full Power Response	5kHz min (16kHz typ)	*	*	*
Slew Rate Inverting Unity Gain	0.3V/μs min (1.0V/μs typ)	*	*	*
Overload Recovery Inverting Unity Gain	100μs max (16μs typ)	*	*	*
INPUT OFFSET VOLTAGE[3]	1.0mV max	1.0mV max	0.5mV max	0.25mV max
vs. Temperature, T_A = min to max	25μV/°C max	15μV/°C max	5μV/°C max	3μV/°C max
vs. Supply, T_A = min to max	400μV/V max (50μV/V typ)	200μV/V max	200μV/V max	200μV/V max
INPUT BIAS CURRENT				
Either Input[4]	2pA max	1pA max	1pA max	1pA max
INPUT IMPEDANCE				
Differential	$1.6pF \| 10^{13}\Omega$	*	*	*
Common Mode	$0.8pF \| 10^{15}\Omega$	*	*	*
INPUT NOISE				
Voltage, 0.1Hz to 10Hz	3.0μV (p-p)	*	*	5μV (p-p) max
f = 10Hz	$55nV/\sqrt{Hz}$	*	*	*
f = 100Hz	$45nV/\sqrt{Hz}$	*	*	*
f = 1kHz	$35nV/\sqrt{Hz}$	*	*	*
Current, 0.1 to 10Hz	0.01pA (p-p)	*	*	*
10Hz to 10kHz	0.03pA rms	*	*	*
INPUT VOLTAGE RANGE				
Differential	±20V min	*	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*	*
Common Mode Rejection, V_{IN} = ±10V	66dB min (80dB typ)	70dB min	76dB min	76dB min
Maximum Safe Input Voltages[5]	±V_S	*	*	*
POWER SUPPLY				
Rated Performance	±15V typ	*	*	*
Operating	±5V min (±18V max)	*	*	*
Quiescent Current	1.5mA max (0.8mA typ)	*	*	*
TEMPERATURE				
Operating, Rated Performance	0 to +70°C	*	*	*
Storage	−65°C to +150°C	*	*	*
PACKAGE OPTION[6]				
TO-99 Style (H08B)	AD545JH	AD545KH	AD545LH	AD545MH

*Specifications same as AD545J.

NOTES

[1] Open Loop Gain is specified with or without nulling of V_{OS}.

[2] A conservative design would not exceed 500pF of load capacitance.

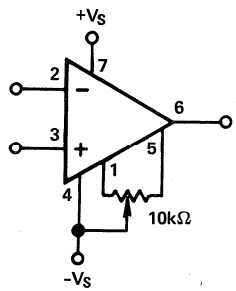
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every +10°C.

[5] If it is possible for the input voltage to exceed the supply voltage, a series protection resistor should be added to limit input current to 0.5mA. The input devices can handle overload currents of 0.5mA indefinitely without damage.

[6] See Section 19 for package outline information.

Specifications subject to change without notice.



Standard Offset Null Circuit

LAYOUT AND CONNECTION CONSIDERATIONS

The design of very high impedance measurement systems introduces a new level of problems associated with the reduction of leakage paths and noise pickup.

1. A primary consideration in high impedance system designs is to attempt to place the measuring device as near to the signal source as possible. This will minimize current leakage paths, noise pickup and capacitive loading.
2. The use of guarding techniques is essential to realizing the capability of the low input currents of the AD545. Guarding is achieved by applying a low impedance bootstrap potential to the outside of the insulation material surrounding the high impedance signal line. This bootstrap potential is held at the same level as that of the high impedance line; therefore, there is no voltage drop across the insulation, and hence, no leakage. The guard will also act as a shield to reduce noise pickup and serves the additional function of reducing the effective capacitance to the input line. The case of the AD545 is brought out separately to pin 8 so that it can also be connected to the guard potential. This technique virtually eliminates potential leakage paths across the package insulation, provides a noise shield for the sensitive circuitry, and reduces common-mode input capacitance to about 0.2pF. Figure 10 shows a proper printed circuit board layout for input guarding and connecting the case guard. Figures 2 and 3 show guarding connections for typical inverting and non-inverting applications. If pin 8 is not used for guarding, it should be connected to ground or one of the amplifier's power supplies to reduce noise.
3. Printed circuit board layout and construction is critical in achieving low leakage performance. The best performance will be realized by using a teflon IC socket for the AD545 but at least a teflon stand-off should be used for the high-impedance lead. If this is not feasible, the input guarding scheme shown in Figure 10 will minimize leakage as much as possible and should be applied to both sides of the board. The guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit; to minimize noise and leakage, they must be carried in rigid, shielded cables.

APPLICATION NOTES

The AD545 offers one of the lowest input bias currents available in an integrated circuit package. Performing accurate measurements with this device requires careful attention to detail; the notes given here will aid the user in realizing the full measurement potential of the AD545 and extending its performance limits.

1. As with all junction FET input devices, the temperature of the FET's themselves is all-important in determining the input bias currents. Over the operating temperature range, the input bias currents closely follow a characteristic of doubling every 10°C; therefore, every effort should be made to minimize device operating temperature
2. The heat dissipation can be reduced initially by careful investigation of the application. First, if possible, reduce the required power supplies, since internal power consumption contributes the largest component of self-heating. The effects of this are shown in Figure 7, which shows typical input bias current and quiescent current versus supply voltage.
3. Output loading effects, which are normally ignored, can cause a significant increase in chip temperature and therefore bias current. For example, a 2kΩ load driven at 10 volts at the output will cause at least an additional 25 milliwatts dissipation in the output stage (and some in other stages) over the typical 24 milliwatts, thereby at least doubling the effects of self-heating. The results of this form of additional power dissipation are demonstrated in Figure 9, which shows normalized input bias current versus additional power dissipated (it doubles every 10°C); we recommend restricting the load impedance to be at least 10kΩ.

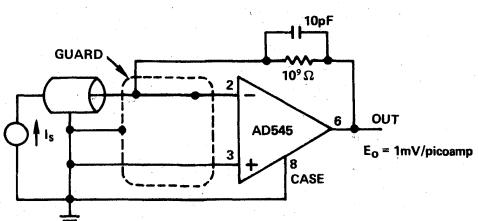


Figure 1. Picoampere Current-to-Voltage Converter Inverting Configuration

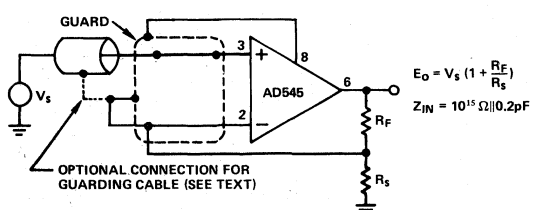


Figure 2. Very High Impedance Non-Inverting Amplifier

Typical Performance Curves

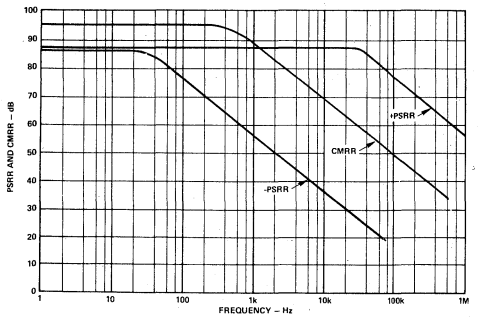


Figure 3. PSRR and CMRR Versus Frequency

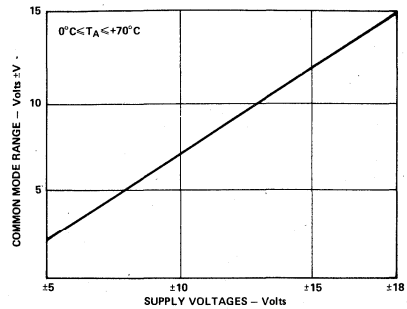


Figure 4. Input Common Mode Range Versus Supply Voltage

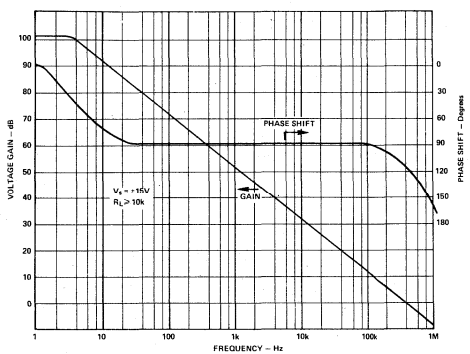


Figure 5. Open Loop Frequency Response

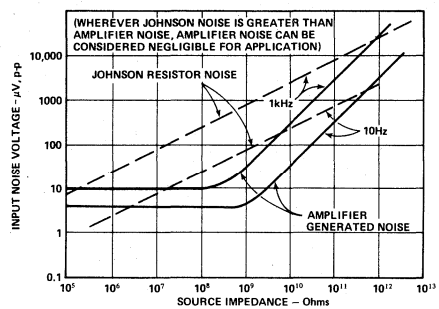


Figure 6. Total Input Noise Voltage Versus Source Impedance and Bandwidth

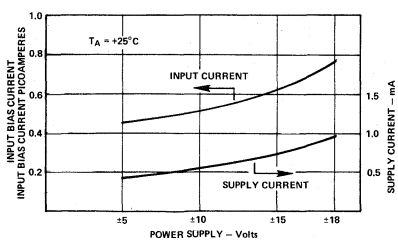


Figure 7. Input Bias Current and Supply Current Versus Supply Voltage

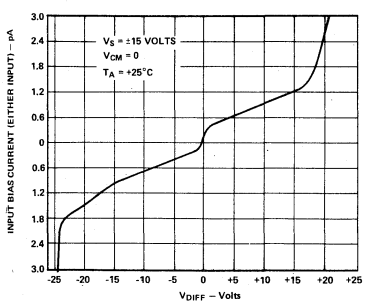


Figure 8. Input Bias Current Versus Differential Input Voltage

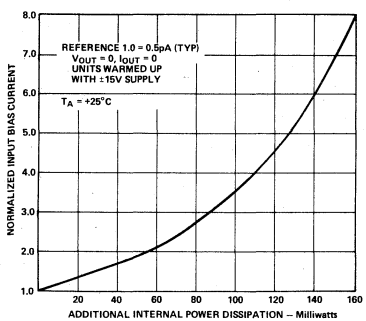


Figure 9. Input Bias Current Versus Addition Power Dissipation

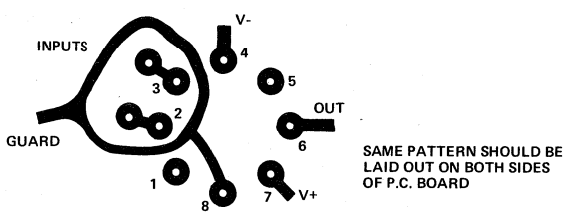


Figure 10. Board Layout for Guarding Inputs with Guarded TO-99 Package

ANALOG DEVICES

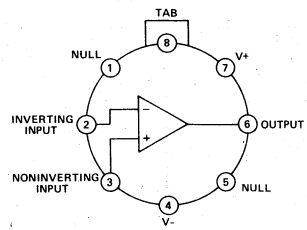
Ultra Low Drift BIFET Operational Amplifier

AD547

4

FEATURES
Ultra Low Drift (1μV/°C–AD547L)
Low Offset Voltage (0.25mV–AD547L)
Low Input Bias Currents (25pA–AD547L, K)
Low Quiescent Current (1.5mA)
Low Noise (2μV p-p)
High Open Loop Gain (110dB–AD547K, L, S)

AD547 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD547 is a monolithic, FET input operational amplifier combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only from high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C–AD547JH, 0.25mV, 1μV/°C–AD547LH).

In addition to superior low drift performance, the AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier with 50pA max for the J grade and 25pA max for the L grade. Since Analog Devices, unlike most other manufacturers, specifies input bias current with the amplifiers warmed-up, our BIFET amplifiers are specified under actual operating conditions.

The AD547 is especially designed for use in applications, such as instrumentation signal conditioning and analog computation, that require a high degree of precision at low cost.

The AD547 is offered in three commercial versions, J, K and L are specified from 0 to +70°C and the S is specified from −55°C to +125°C. All grades are packaged in hermetically sealed TO-99 cans.

PRODUCT HIGHLIGHTS

1. Advanced laser wafer trimming techniques reduce offset voltage drift to 1μV/°C max and reduce offset voltage to only 0.25mV max on the AD547L.
2. Analog Devices BIFET processing provides 25pA max (10pA typical) bias currents specified after 5 minutes of warm-up.
3. Low voltage noise, high open loop gain and outstanding offset performance make the AD547 a true precision BIFET amplifier.
4. The low quiescent supply current, typically 1.1mA, enables the AD547 to bring a new level of precision to applications where low power consumption is essential.
5. A further benefit on the AD547's low power consumption and low offset voltage drift is a minimal warm-up drift after power is applied (typically 7μV shift for the AD547L).

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD547J			AD547K			AD547L			AD547S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN[1]													
V_O = ±10V, $R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[2]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs. Temp.[3]			**5**			**2**			**1.0**			**5.0**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT													
Either Input[4]		10	**50**		10	**25**		10	**25**		10	**25**	pA
Offset Current		5			2			2			2		pA
INPUT IMPEDANCE													
Differential[5]		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				**4**			**4**			**4**	μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		1.1	**1.5**		1.1	1.5		1.1	**1.5**		1.1	**1.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[6]													
TO-99 Style (H08B)		AD547JH			AD547KH			AD547LH			AD547SH		

NOTES

[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3]Input Offset Voltage Drift is specified with the offset voltage unnulled. Nulling will induce an additional 3μV/°C/mV of nulled offset.

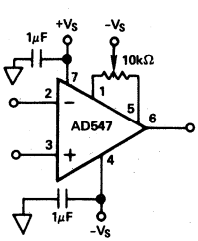
[4]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5]Defined as the maximum safe voltage between inputs, such that neither exceed ±10V from ground.

[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Null Circuit

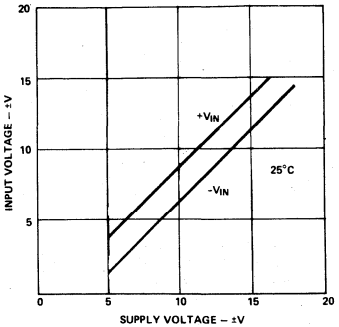


Figure 1. Input Voltage Range vs. Supply Voltage

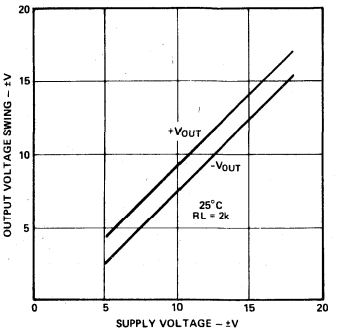


Figure 2. Output Voltage Swing vs. Supply Voltage

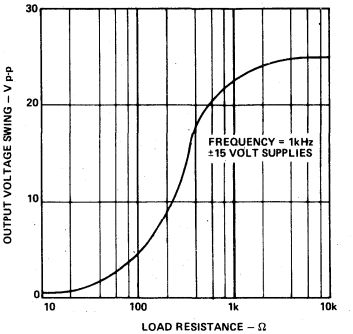


Figure 3. Output Voltage Swing vs. Resistive Load

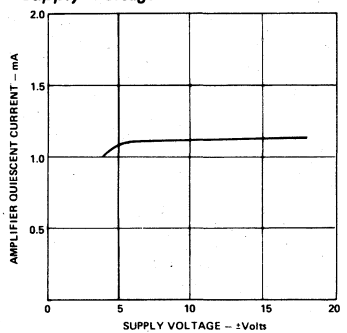


Figure 4. Quiescent Current vs. Supply Voltage

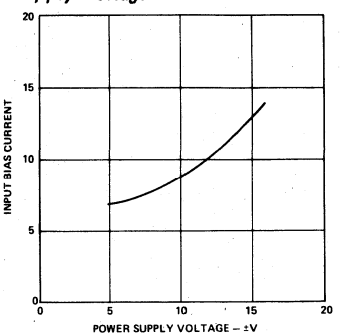


Figure 5. Input Bias Current vs. Supply Voltage

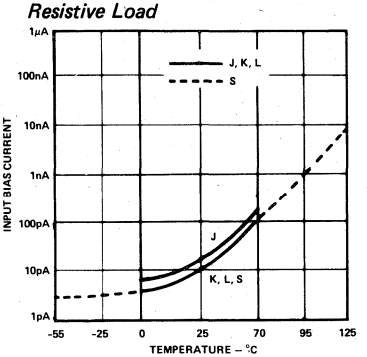


Figure 6. Input Bias Current vs. Temperature

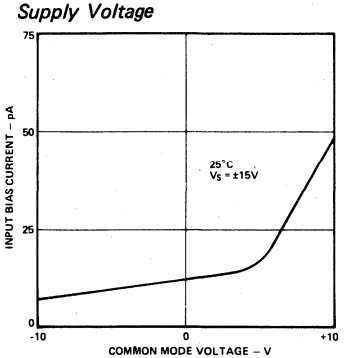


Figure 7. Input Bias Current vs. CMV

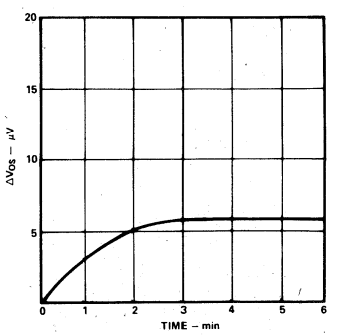


Figure 8. Input Offset Voltage Turn On Drift vs. Time

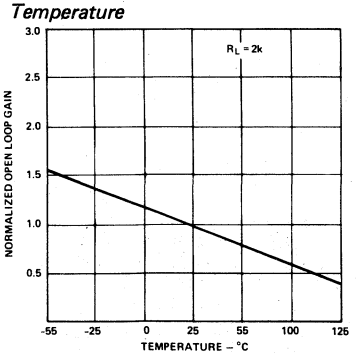


Figure 9. Open Loop Gain vs. Temperature

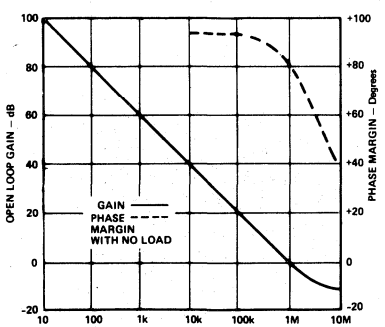


Figure. 10 Open Loop Frequency Response

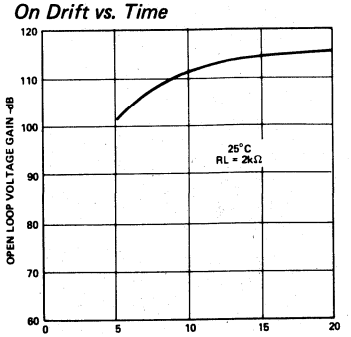


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

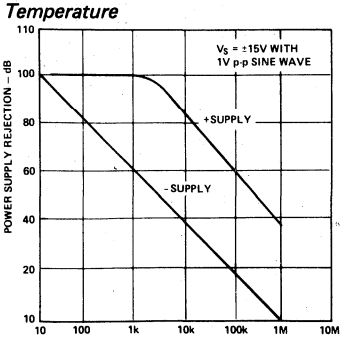


Figure 12. Power Supply Rejection vs. Frequency

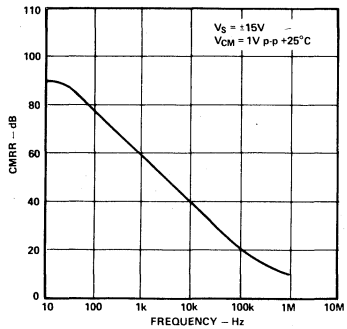


Figure 13. Common Mode Rejection vs. Frequency

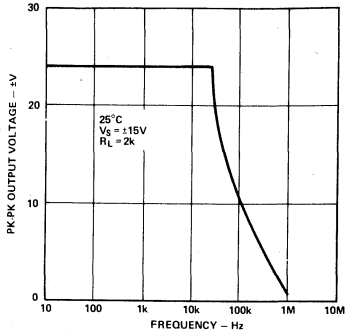


Figure 14. Large Signal Frequency Response

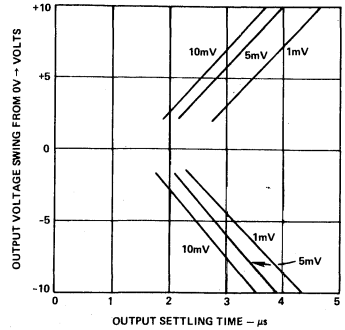


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 20)

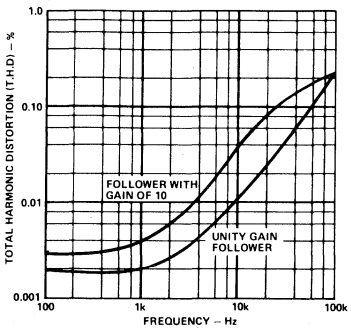


Figure 16. Total Harmonic Distortion vs. Frequency

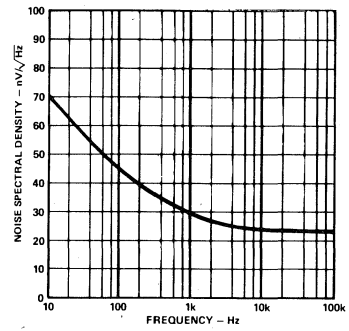


Figure 17. Input Noise Voltage Spectral Density

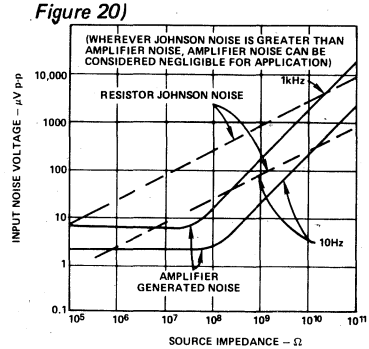
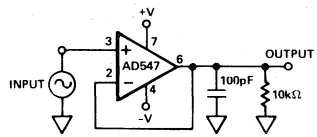
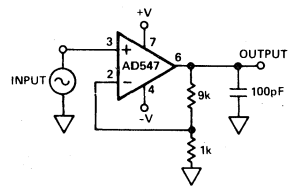


Figure 18. Total Input Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

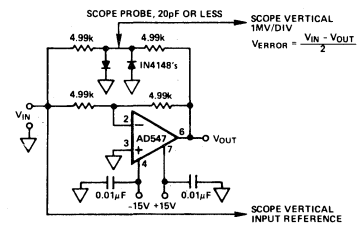


Figure 20. Settling Time Test Circuit

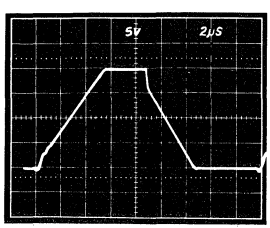


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

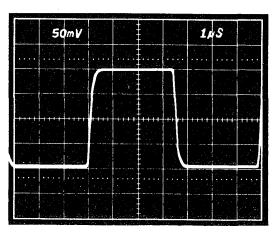


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

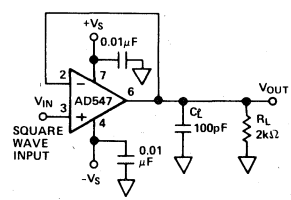


Figure 21c. Unity Gain Follower

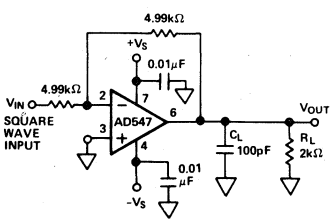


Figure 22a. Unity Gain Inverter

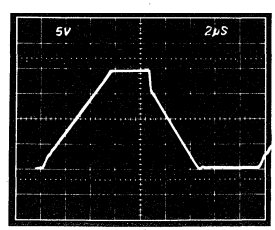


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

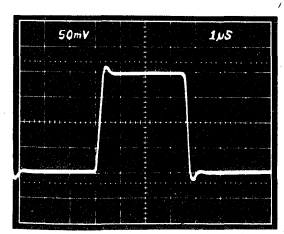


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

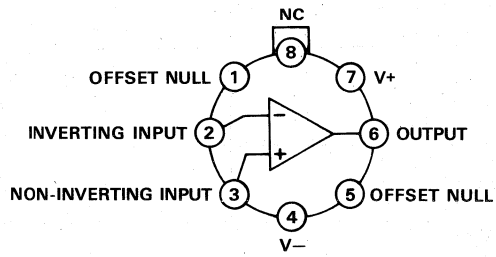
ANALOG DEVICES

Low Cost Implanted FET-Input Op Amp

AD611

FEATURES
Low Offset Voltage: 0.5mV max (AD611K)
Low Offset Voltage Drift: 10μV/°C max (AD611K)
Low Bias Current: 50pA max (AD611K)
High Slew Rate: 8V/μs min
Low Supply Current: 2.5mA max
Fast Settling Time: 3μs

AD611 FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN 4 CONNECTED TO CASE

TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD611 is a precision monolithic BIFET operational amplifier designed and manufactured to offer offset voltages of 0.5mV max and offset voltage drifts of 10μV/°C max, yet is priced in the same range as lower performance devices. Analog Devices precision BIFET fabrication technology and proprietary laser wafer drift trimming process are combined with years of experience in manufacturing precision analog integrated circuits to insure consistently high performance at low cost. The offset voltage specifications mentioned above, coupled with the lowest input bias current of any general purpose BIFET amplifier, 100pA max guaranteed after five minutes of operation, make the AD611 the most precise BIFET amplifier in its price range.

In addition to the excellent dc specifications, the design of the AD611 is optimized to deliver 13V/μs slew rate, 2MHz unity gain bandwidth and a 0.01% settling time of 3μs. This combination of performance makes the AD611 ideal for any FET application where excellent performance at low cost is required. Its wide bandwidth, low offset voltage and fast settling time make this device ideal as an output amplifier for current output D/A converters of all types. 80dB of CMRR and 94dB of open loop gain ensure "12-bit" performance in high speed buffer circuits. The devices' excellent low frequency noise performance and low supply current requirements will benefit any general purpose BIFET application.

The AD611 is available in two grades rated over the 0 to +70°C temperature range; the general purpose AD611J and the high precision AD611K. Both grades are available in hermetically sealed TO-99 packages. The AD611 is pinned out in standard operational amplifier configuration to facilitate low cost upgrading of existing designs using older, less accurate amplifiers.

PRODUCT HIGHLIGHTS

1. The AD611 is laser wafer drift trimmed to offer offset voltages of 0.5mV max and offset voltage drifts of 10μV/°C.
2. Analog Devices BIFET processing results in maximum input bias currents of 50pA, guaranteed after 5 minutes of operation.
3. The high slew rate (8V/μs min.) and fast settling time (3μs to 0.01%) make the AD611 ideal for use in D/A, A/D, sample-hold circuits and precision high speed integrators.
4. Monolithic construction, along with advanced processing and manufacturing technologies result in extremely high performance at very low cost.

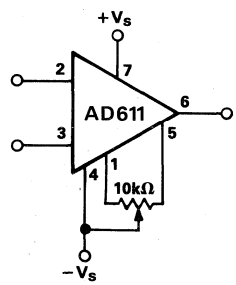
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise noted)

Model	AD611J Min	AD611J Typ	AD611J Max	AD611K Min	AD611K Typ	AD611K Max	Units
OPEN LOOP GAIN[1]							
$V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	**30,000**	80,000		**50,000**	80,000		V/V
T_A = min to max $R_L \geq 2k\Omega$	20,000	50,000		**40,000**	50,000		V/V
FREQUENCY RESPONSE							
Unity Gain, Small Signal		2			2		MHz
Full Power Response		200			200		kHz
Slew Rate, Unity Gain	8	13		8	13		V/μs
Total Harmonic Distortion f = 1kHz		0.0025			0.0025		%
INPUT OFFSET VOLTAGE[2]		0.25	**2.0**		0.25	**0.5**	mV
vs. Temperature		5	20		5	**10**	μV/°C
vs. Supply		50	**200**		50	**100**	μV/V
T_A = min to max		70	200		70	100	μV/V
INPUT BIAS CURRENT							
Either Input[3]		25	**100**		10	**50**	pA
Input Offset Current		10	**50**		5	**25**	pA
INPUT IMPEDANCE							
Differential		$10^{12}\Omega \| 6pF$			$10^{12}\Omega \| 6pF$		
Common Mode		$10^{12}\Omega \| 3pF$			$10^{12}\Omega \| 3pF$		
INPUT VOLTAGE RANGE							
Differential[4]		±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		V
Common-Mode Rejection, $V_{IN} = \pm 10V$	**74**			**80**			dB
POWER SUPPLY							
Operating Range	**±5**		**±18**	**±5**		**±18**	V
Quiescent Current		1.8	**2.5**		1.8	**2.5**	mA
VOLTAGE NOISE							
0.1 – 10Hz		2.0			2.0		μV p-p
10Hz		35			35		$nV/\sqrt{Hz}$
100Hz		22			22		$nV/\sqrt{Hz}$
1kHz		18			18		$nV/\sqrt{Hz}$
10kHz		16			16		$nV\sqrt{Hz}$
TEMPERATURE RANGE							
Operating, Rated Performance	0		+70	0		+70	°C
Storage	−65		+150	−65		+150	°C
PACKAGE OPTIONS[5] TO-99	AD611JH			AD611KH			

NOTES
[1]Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[2]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.
[3]Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.
[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.
[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



Standard Offset Null Circuit

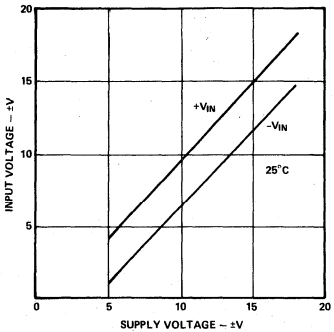


Figure 1. Input Voltage Range vs. Supply Voltage

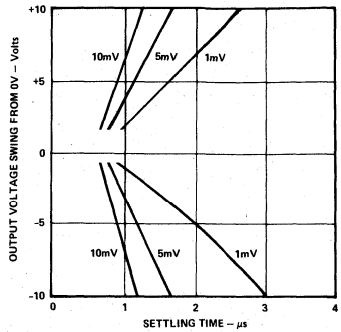


Figure 2. Output Settling Time vs. Output Swing and Error (Circuit of Figure 15a)

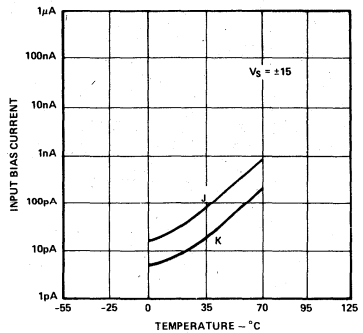


Figure 3. Input Bias Current vs. Temperature

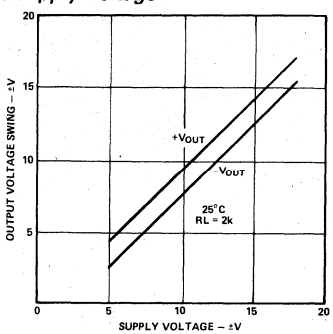


Figure 4. Output Voltage Swing vs. Supply Voltage

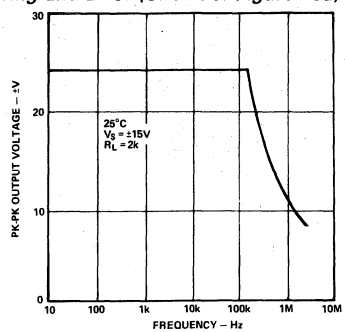


Figure 5. Large Signal Frequency Response

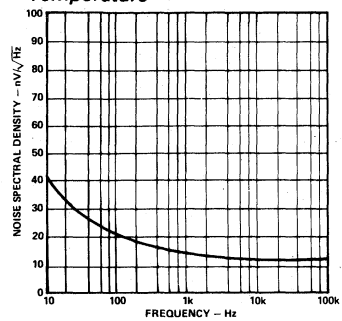


Figure 6. Input Noise Voltage Spectral Density

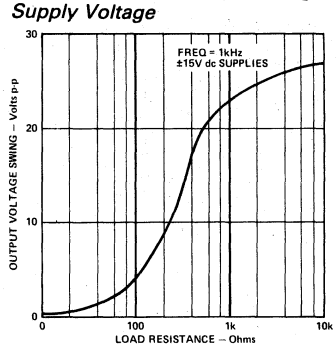


Figure 7. Output Voltage Swing vs. Resistive Load

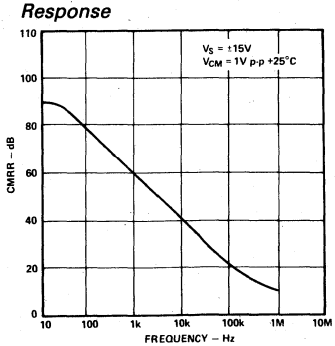


Figure 8. Common-Mode Rejection vs. Frequency

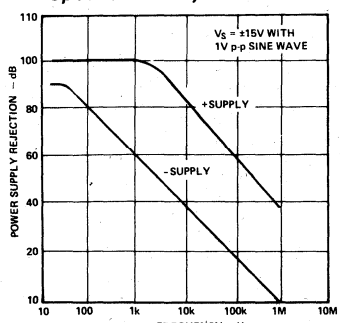


Figure 9. Power Supply Rejection vs. Frequency

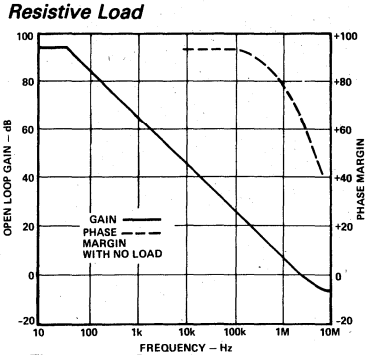


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

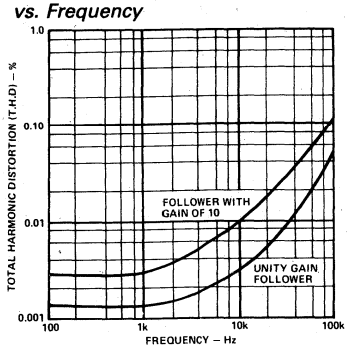


Figure 11. Total Harmonic Distortion vs. Frequency

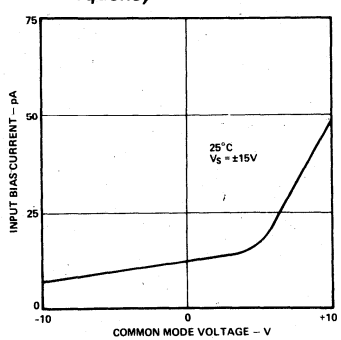


Figure 12. Input Bias Current vs. CMV

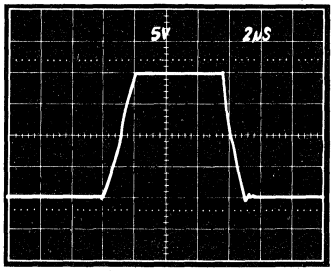


Figure 13a. Unity Gain Follower Pulse Response (Large Signal)

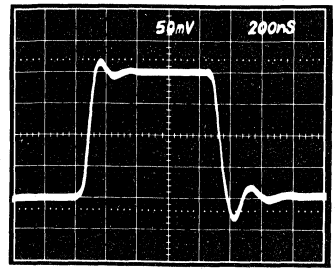


Figure 13b. Unity Gain Follower Pulse Response (Small Signal)

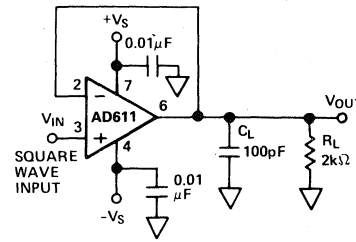


Figure 13c. Unity Gain Follower

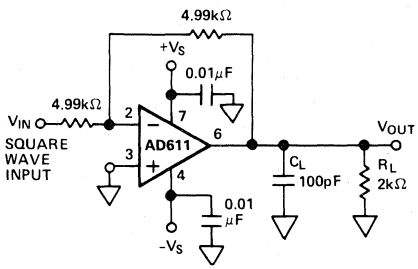


Figure 14a. Unity Gain Inverter

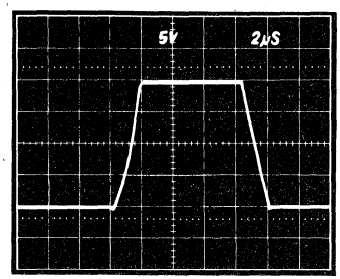


Figure 14b. Unity Gain Inverter Pulse Response (Large Signal)

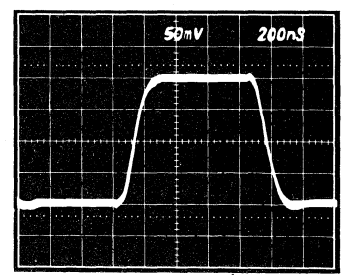


Figure 14c. Unity Gain Inverter Pulse Response (Small Signal)

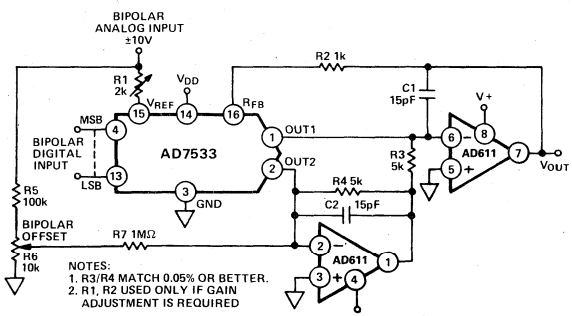


Figure 15a. AD611 Used as DAC Output Amplifiers

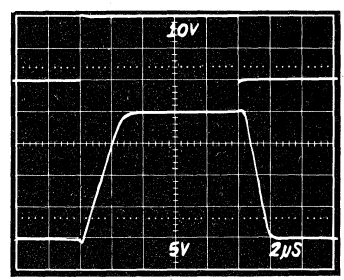


Figure 15b. Large Signal Response

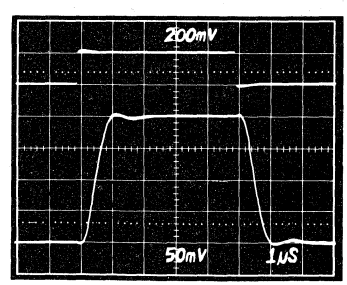


Figure 15c. Small Signal Response

Figure 15a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function. The photos exhibit the response to a step input at V_{REF}. Figure 15b is the large signal response and Figure 15c is the small signal response.

The output impedance of a CMOS DAC varies with the digital word thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The AD611 with trimmed offset will minimize the effect. The Schottky protection diodes recommended for use with many CMOS DACs are not required when using the AD611.

ANALOG DEVICES

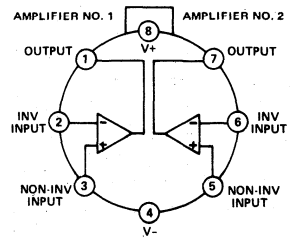
Precision Low Cost Dual BIFET Op Amp

AD642

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Current
Crosstalk-124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Open Loop Gain
Low Quiescent Current: 2.8mA max
Low Total Harmonic Distortion
Standard Dual Amplifier Pin Out

AD642 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic BI-FET operational amplifier fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 35pA max matched to 25pA for the AD642K and L; 75pA max, matched to 35pA for the AD642J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV and matched to 0.25mV for the AD642L, 1.0mV and matched to 0.5mV for the AD642K, utilizing Analog's laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to produce matched bias currents which have lower initial bias currents than other popular BIFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and combined with superior IC processing guarantees offset voltage tracking over the temperature range.

The AD642 is recommended for applications in which excellent ac and dc performance is required. The matched amplifiers provide a low cost solution for true instrumentation amplifiers, log ratio amplifiers, and output amplifiers for four quadrant multiplying D/A converters such as the AD7541.

The AD642 is available in three versions: the "J", "K" and "L", all specified over the 0 to +70°C temperature range and one version, "S", over the -55°C to +125°C extented operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD642 has tight matching specifications to ensure high performance, eliminating the need to match individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD642 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max and matched side to side to 0.25mV (AD642L), thus eliminating the need for external nulling.
4. Low voltage noise (2μV, p-p), and high open loop gain enhance the AD642's performance as a precision op amp.
5. The standard dual amplifier pin out allows the AD642 to replace lower performance duals without redesign.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD642J			AD642K			AD642L			AD642S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	**100,000**			**250,000**			**250,000**			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		45			45			45			45		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±15	±5		±15	±5		±15	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)	AD642JH			AD642KH			AD642LH			AD642SH			

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

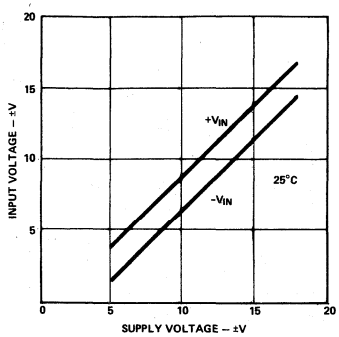


Figure 1. Input Voltage Range vs. Supply Voltage

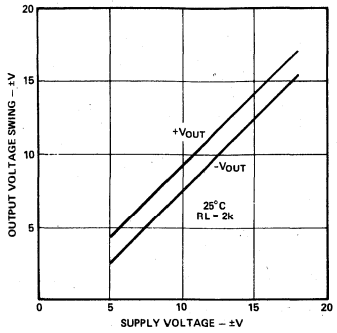


Figure 2. Output Voltage Swing vs. Supply Voltage

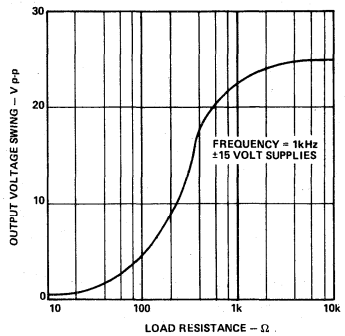


Figure 3. Output Voltage Swing vs. Resistive Load

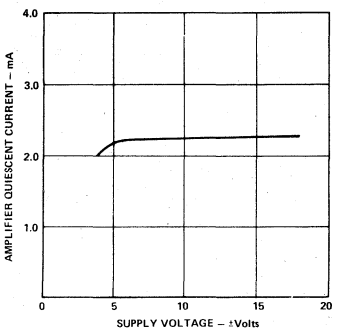


Figure 4. Quiescent Current vs. Supply Voltage

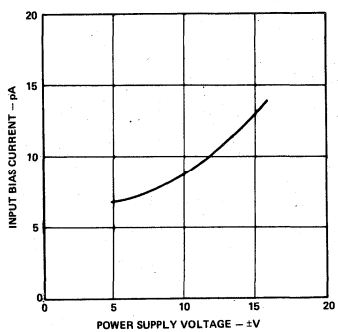


Figure 5. Input Bias Current vs. Supply Voltage

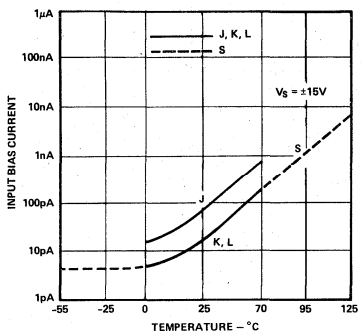


Figure 6. Input Bias Current vs. Temperature

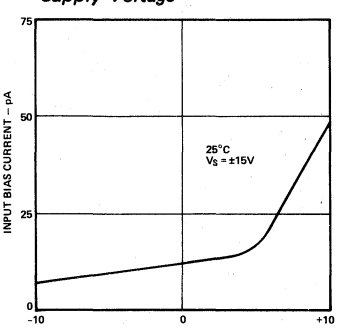


Figure 7. Input Bias Current vs. CMV

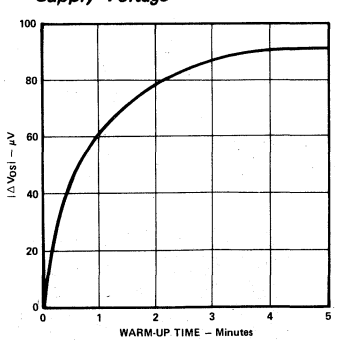


Figure 8. Input Offset Voltage Turn On Drift vs. Time

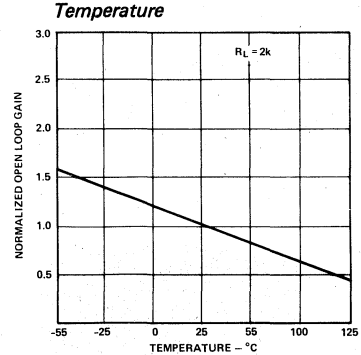


Figure 9. Open Loop Gain vs. Temperature

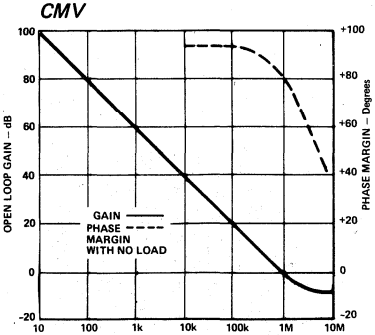


Figure 10. Open Loop Frequency Response

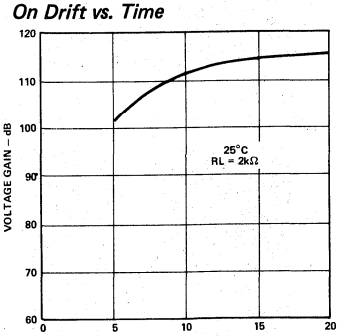


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

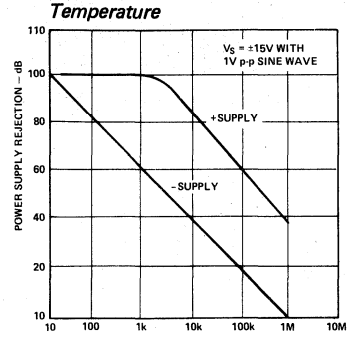


Figure 12. Power Supply Rejection vs. Frequency

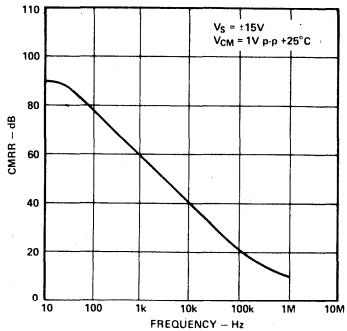


Figure 13. Common Mode Rejection vs. Frequency

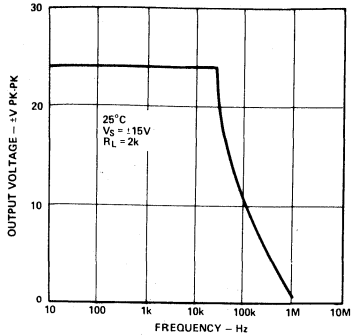


Figure 14. Large Signal Frequency Response

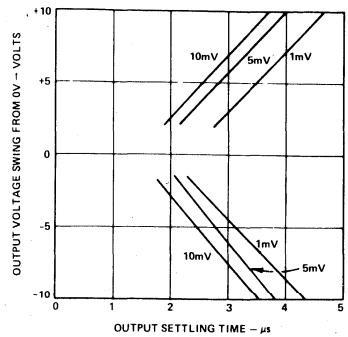


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

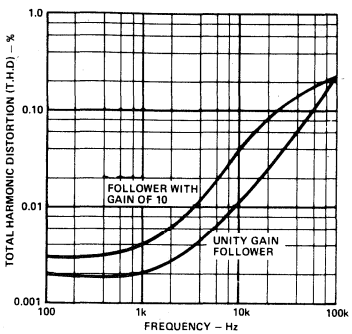


Figure 16. Total Harmonic Distortion vs. Frequency

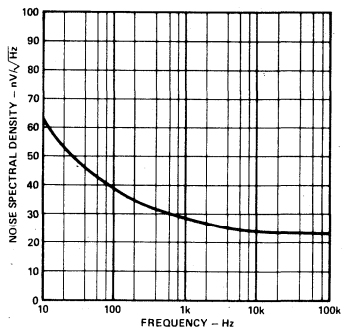


Figure 17. Input Noise Voltage Spectral Density

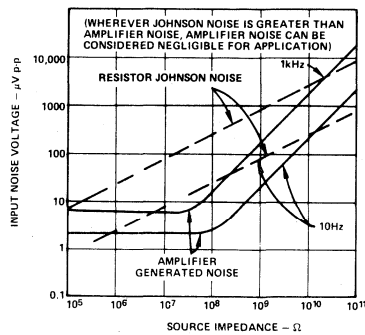
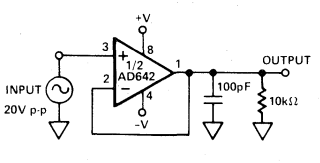
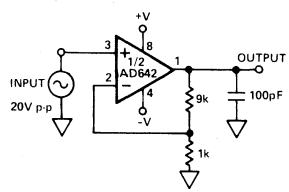


Figure 18. Total Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

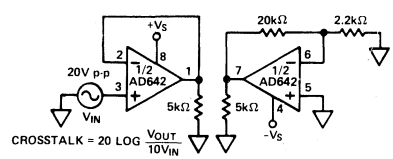


Figure 20. Crosstalk Test Circuit

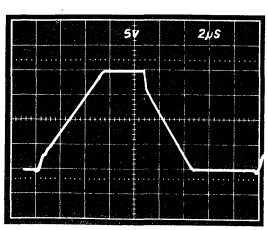


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

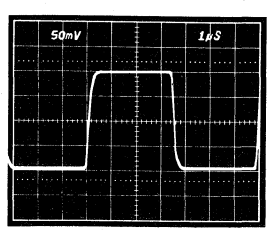


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

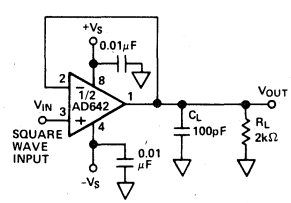


Figure 21c. Unity Gain Follower

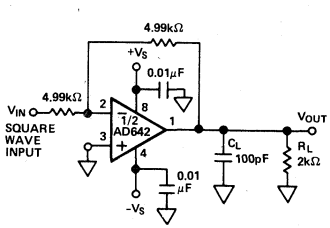


Figure 22a. Unity Gain Inverter

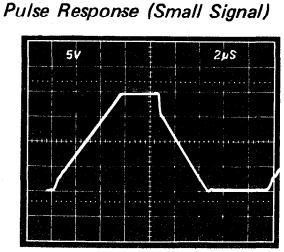


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

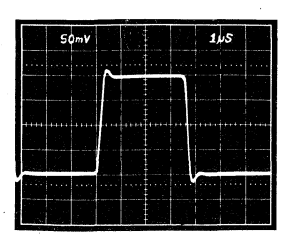


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

Dual High Speed Implanted BIFET Op Amp

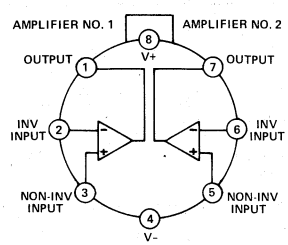
AD644

4

FEATURES

Matched Offset Voltage
Matched Offset Voltage Over Temperature
Matched Bias Currents
Crosstalk -124dB at 1kHz
Low Bias Current: 35pA max Warmed Up
Low Offset Voltage: 500μV max
Low Input Voltage Noise: 2μV p-p
High Slew Rate: 13V/μs
Low Quiescent Current: 4.5mA max
Fast Settling to ±0.01%: 3μs
Low Total Harmonic Distortion: 0.0015% at 1kHz
Standard Dual Amplifier Pin Out

AD644 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD644 offers matched bias currents that are significantly lower than currently available monolithic dual BIFET operational amplifiers: 35pA max, matched to 25pA for the AD644K and L, 75pA max matched to 35pA for the AD644J and S. In addition, the offset voltage is laser trimmed to less than 0.5mV, and matched to 0.25mV for the AD644L, 1.0mV and matched to 0.5mV for the AD644K, utilizing Analog Devices' laser-wafer trimming (LWT) process.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabrication of precision, matched JFETs on a monolithic bipolar chip. This process optimizes the ability to produce matched amplifiers which have lower initial bias currents than other popular BIFET op amps. Laser-wafer trimming each amplifier's input offset voltage assures tight initial match and superior IC processing guarantees offset voltage tracking over the temperature range.

The AD644 is recommended for applications in which both excellent ac and dc performance is required. The matched amplifiers provide a low cost solution to true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

The AD644 is available in four versions: the "J", "K" and "L" are specified over the 0 to +70°C temperature range and the "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed, TO-99 metal can.

PRODUCT HIGHLIGHTS

1. The AD644 has tight side to side matching specifications to ensure high performance without matching individual devices.
2. Analog Devices, unlike some manufacturers, specifies each device for the maximum bias current at either input in the warmed-up condition, thus assuring the user that the AD644 will meet its published specifications in actual use.
3. Laser-wafer-trimming reduces offset voltage to as low as 0.5mV max matched side to side to 0.25mV (AD644L), thus eliminating the need for external nulling.
4. Improved bipolar and JFET processing on the AD644 result in the lowest matched bias current available in a high speed monolithic FET op amp.
5. Low voltage noise (2μV p-p) and high open loop gain enhance the AD644's performance as a precision op amp.
6. The high slew rate (13.0V/μs) and fast settling time to 0.01% (3.0μs) make the AD644 ideal for D/A, A/D, sample-hold circuits and dual high speed integrators.
7. Low harmonic distortion (0.0015%) and low crosstalk (-124dB) make the AD644 an ideal choice for stereo audio applications.
8. The standard dual amplifier pin out allows the AD644 to replace lower performance duals without redesign.

SPECIFICATIONS (@ +25°C and V_S = ±15V dc)

Model	AD644J			AD644K			AD644L			AD644S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
V_O = ±10V, $R_L \geq 2k\Omega$	**30,000**			**50,000**			**50,000**			**50,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	**20,000**			**40,000**			**40,000**			**20,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		2.0			2.0			2.0			2.0		MHz
Full Power Response		200			200			200			200		kHz
Slew Rate, Unity Gain	8.0	13.0		8.0	13.0		8.0	13.0		8.0	13.0		V/μs
Total Harmonic Distortion		0.0015			0.0015			0.0015			0.0015		%
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**2.0**			**1.0**			**0.5**			**1.0**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		10			5			5			5		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**3.5**			**2.0**			**1.0**			**3.5**	mV
Input Bias Current			**35**			**25**			**25**			**35**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ‖pF
Common Mode		$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$			$10^{12}\|3$		MΩ‖pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2			2			2			2		μV p-p
f = 10Hz		35			35			35			35		$nV/\sqrt{Hz}$
f = 100Hz		22			22			22			22		$nV/\sqrt{Hz}$
f = 1kHz		18			18			18			18		$nV/\sqrt{Hz}$
f = 10kHz		16			16			16			16		$nV/\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**		3.5	**4.5**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)		AD644JH			AD644KH			AD644LH			AD644SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

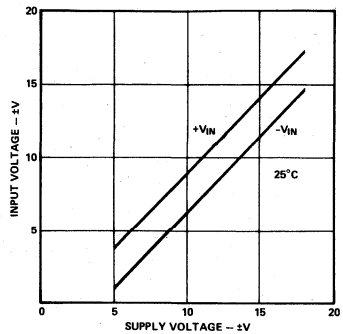


Figure 1. Input Voltage Range vs. Supply Voltage

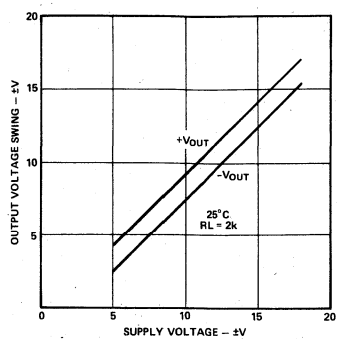


Figure 2. Output Voltage Swing vs. Supply Voltage

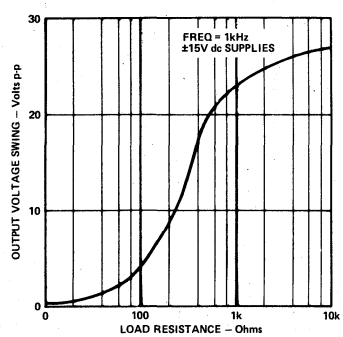


Figure 3. Output Voltage Swing vs. Resistive Load

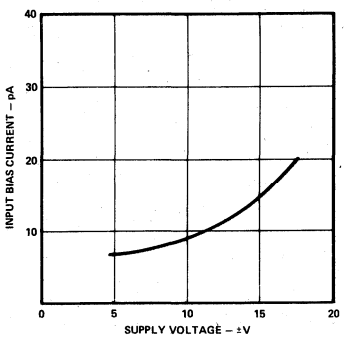


Figure 4. Input Bias Current vs. Supply Voltage

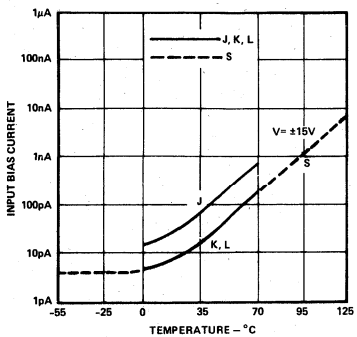


Figure 5. Input Bias Current vs. Temperature

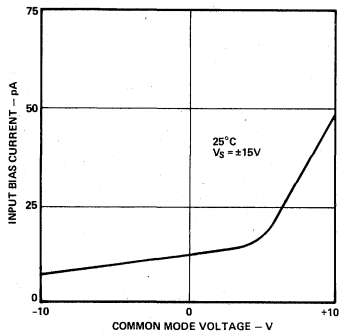


Figure 6. Input Bias Current vs. CMV

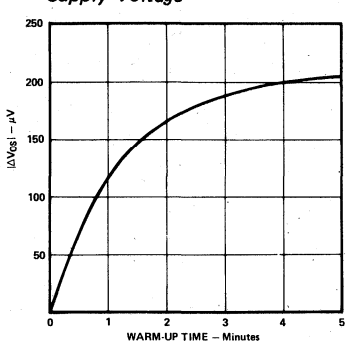


Figure 7. Change in Offset Voltage vs. Warm-Up Time

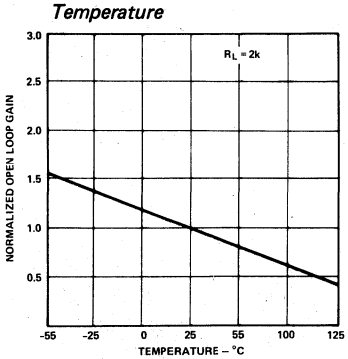


Figure 8. Open Loop Gain vs. Temperature

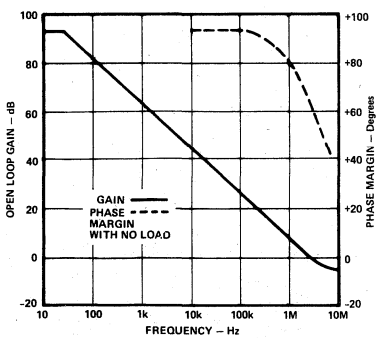


Figure 9. Open Loop Frequency Response

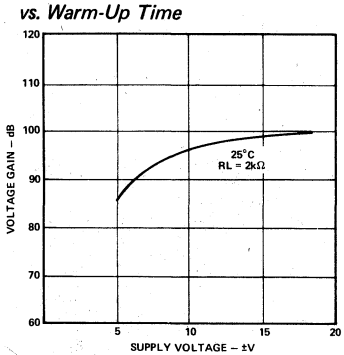


Figure 10. Open Loop Voltage Gain vs. Supply Voltage

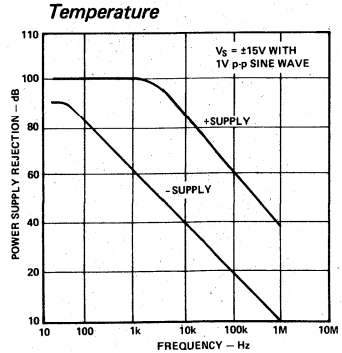


Figure 11. Power Supply Rejection vs. Frequency

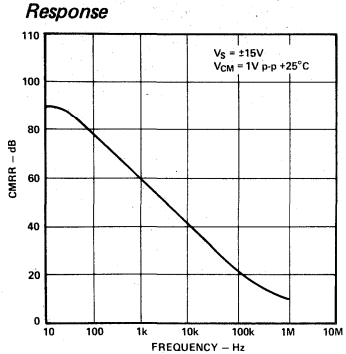


Figure 12. Common Mode Rejection Ratio vs. Frequency

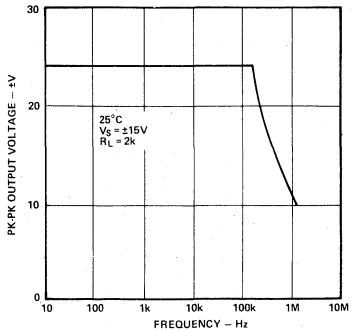


Figure 13. Large Signal Frequency Response

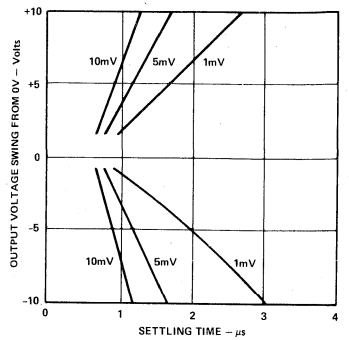


Figure 14. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23a)

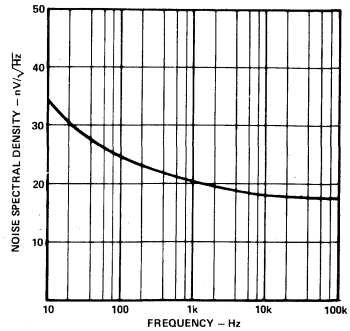


Figure 15. Noise Spectral Density

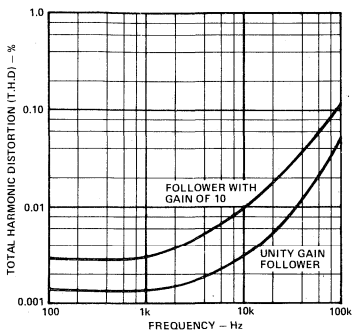


Figure 16. Total Harmonic Distortion vs. Frequency

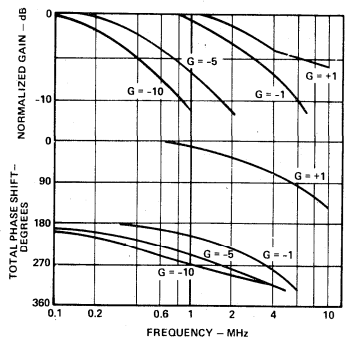


Figure 17. Closed Loop Gain & Phase vs. Frequency

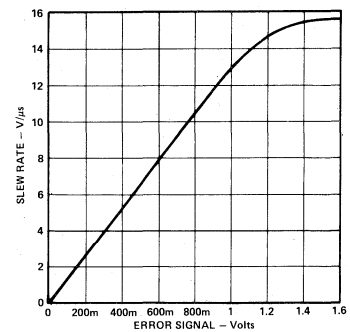
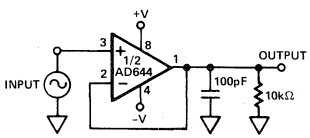
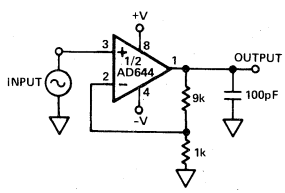


Figure 18. Slew Rate vs. Error Signal



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

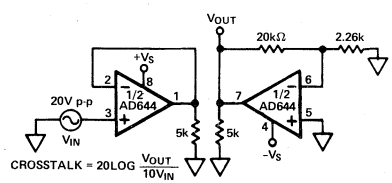


Figure 20. Crosstalk Test Circuit

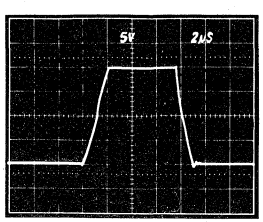


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

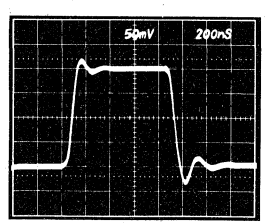


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

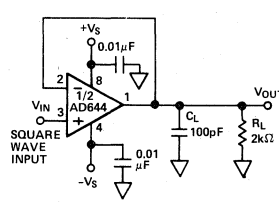


Figure 21c. Unity Gain Follower

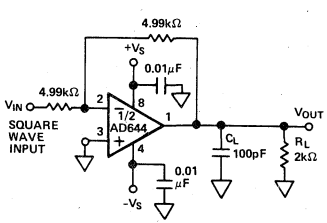


Figure 22a. Unity Gain Inverter

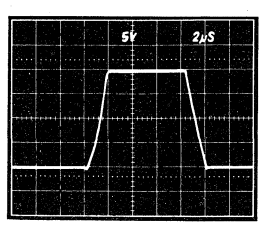


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

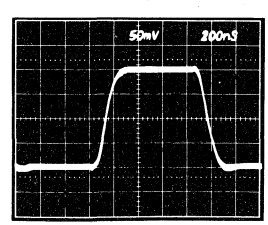


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

Ultra-Low Drift Dual BIFET Op Amp

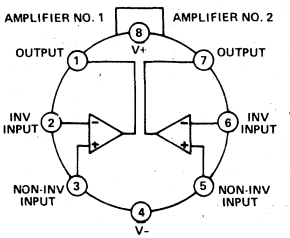
AD647

4

FEATURES

- Low Offset Voltage Drift
- Matched Offset Voltage
- Matched Offset Voltage Over Temperature
- Matched Bias Current
- Crosstalk -124dB at 1kHz
- Low Bias Current: 35pA max Warmed Up
- Low Offset Voltage: 250μV max
- Low Input Voltage Noise: 2μV p-p
- High Open Loop Gain: 108dB
- Low Quiescent Current: 2.8mA max
- Low Total Harmonic Distortion
- Standard Dual Amplifier Pin Out

AD647 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD647 is an ultra low drift dual JFET amplifier that combines high performance and convenience in a single package.

The AD647 uses the most advanced ion-implantation and laser wafer drift trimming technologies to achieve the highest performance currently available in a dual JFET. Ion-implantation permits the fabrication of matched JFETs on a monolithic bipolar chip. Laser wafer drift trimming trims both the initial offset voltage and its drift with temperature to provide offsets as low as 100μV (250μV max) and drifts of 2.5μV/°C max.

In addition to outstanding individual amplifier performance, the AD647 offers guaranteed and tested matching performance on critical parameters such as offset voltage, offset voltage drift and bias currents.

This high level of performance makes the AD647 especially well suited for high precision instrumentation amplifier applications that previously would have required the costly selection and matching of space wasting single amplifiers.

The AD647 also offers high levels of performance for Digital to Analog Converter output amplifiers, and filtering applications.

The AD647 is offered in four performance grades, three commercial (the J, K, and L) and one extended (the S). All are supplied in hermetically sealed 8-pin TO-99 packages.

PRODUCT HIGHLIGHTS

1. The AD647 is guaranteed and tested to tight matching specifications to ensure high performance and to eliminate the selection and matching of single devices.
2. Laser wafer drift trimming reduces offset voltage and offset voltage drifts to 250μV and 2.5μV/°C max.
3. Voltage noise is guaranteed at 4μV p-p max (0.1 to 10Hz) on K, L and S grades.
4. Bias current (35pA K, L, S; 75pA J) is specified after five minutes of operation.
5. Total supply current is a low 2.8mA max.
6. High open loop gain ensures high linearity in precision instrumentation amplifier applications.
7. The standard dual amplifier pin out permits the direct substitution of the AD647 for lower performance devices.

SPECIFICATIONS (@ +25°C and $V_S = \pm 15V$ dc)

Model	AD647J			AD647K			AD647L			AD647S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPEN LOOP GAIN													
$V_O = \pm 10V, R_L \geq 2k\Omega$	**100,000**			**250,000**			**250,000**			**250,000**			V/V
T_{min} to T_{max}, $R_L = 2k\Omega$	100,000			250,000			250,000			**100,000**			V/V
OUTPUT CHARACTERISTICS													
Voltage @ $R_L = 2k\Omega$, T_{min} to T_{max}	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Voltage @ $R_L = 10k\Omega$, T_{min} to T_{max}	**±12**	±13		**±12**	±13		**±12**	±13		**±12**	±13		V
Short Circuit Current		25			25			25			25		mA
FREQUENCY RESPONSE													
Unity Gain Small Signal		1.0			1.0			1.0			1.0		MHz
Full Power Response		50			50			50			50		kHz
Slew Rate, Unity Gain		3.0			3.0			3.0			3.0		V/μs
INPUT OFFSET VOLTAGE[1]													
Initial Offset			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage vs. Temp.			**10**			5			**2.5**			**5.0**	μV/°C
Input Offset Voltage vs. Supply, T_{min} to T_{max}			**200**			**100**			**100**			**100**	μV/V
INPUT BIAS CURRENT[2]													
Either Input		10	**75**		10	**35**		10	**35**		10	**35**	pA
Offset Current		5			2			2			2		pA
MATCHING CHARACTERISTICS[3]													
Input Offset Voltage			**1.0**			**0.5**			**0.25**			**0.5**	mV
Input Offset Voltage T_{min} to T_{max}			**10**			5			**2.5**			**10.0**	μV/°C
Input Bias Current			**35**			**25**			**25**			**25**	pA
Crosstalk		−124			−124			−124			−124		dB
INPUT IMPEDANCE													
Differential		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
Common Mode		$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$			$10^{12}\|6$		MΩ|pF
INPUT VOLTAGE RANGE													
Differential[4]		±20			±20			±20			±20		V
Common Mode	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Common Mode Rejection	**76**			**80**			**80**			**80**			dB
INPUT NOISE													
Voltage 0.1Hz to 10Hz		2				**4**			**4**			**4**	μV p-p
f = 10Hz		70			70			70			70		nV/$\sqrt{Hz}$
f = 100Hz		45			45			45			45		nV/$\sqrt{Hz}$
f = 1kHz		30			30			30			30		nV/$\sqrt{Hz}$
f = 10kHz		25			25			25			25		nV/$\sqrt{Hz}$
POWER SUPPLY													
Rated Performance		±15			±15			±15			±15		V
Operating	±5		±18	±5		±18	±5		±18	±5		±18	V
Quiescent Current			**2.8**			**2.8**			**2.8**			**2.8**	mA
TEMPERATURE RANGE													
Operating, Rated Performance	0		+70	0		+70	0		+70	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
PACKAGE[5]													
TO-99 Style (H08B)		AD647JH			AD647KH			AD647LH			AD647SH		

NOTES

[1]Input Offset Voltage specifications are guaranteed after 5 minutes of operation at $T_A = +25°C$.

[2]Bias Current specifications are guaranteed at maximum at either input after 5 minutes of operation at $T_A = +25°C$. For higher temperatures, the current doubles every 10°C.

[3]Matching is defined as the difference between parameters of the two amplifiers.

[4]Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

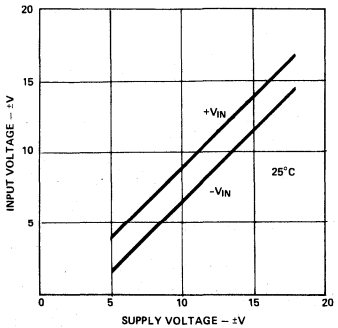


Figure 1. Input Voltage Range vs. Supply Voltage

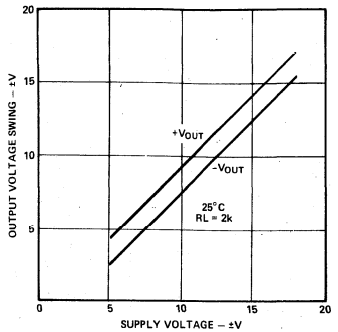


Figure 2. Output Voltage Swing vs. Supply Voltage

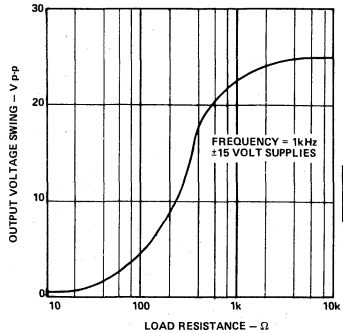


Figure 3. Output Voltage Swing vs. Resistive Load

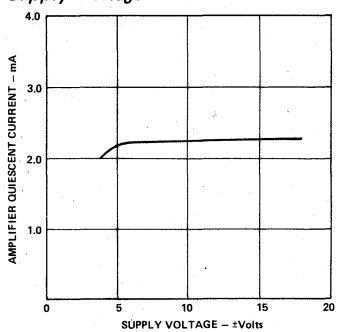


Figure 4. Quiescent Current vs. Supply Voltage

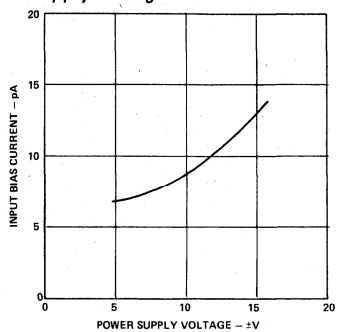


Figure 5. Input Bias Current vs. Supply Voltage

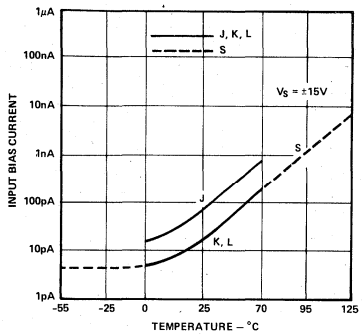


Figure 6. Input Bias Current vs. Temperature

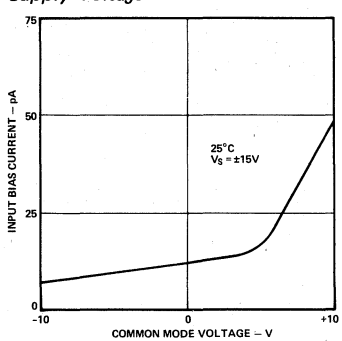


Figure 7. Input Bias Current vs. CMV

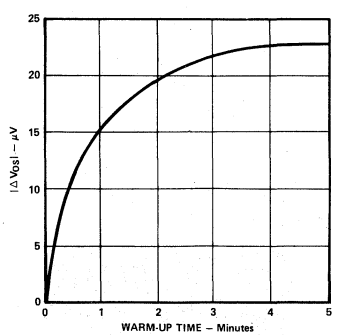


Figure 8. Input Offset Voltage Turn On Drift vs. Time

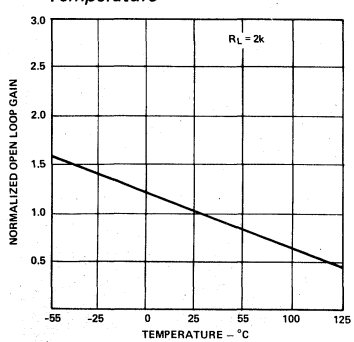


Figure 9. Open Loop Gain vs. Temperature

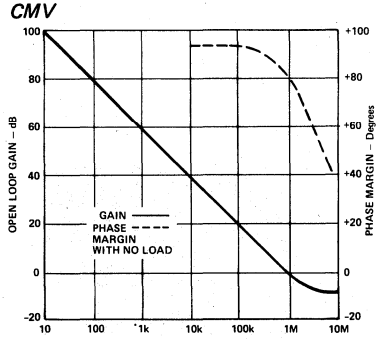


Figure 10. Open Loop Frequency Response

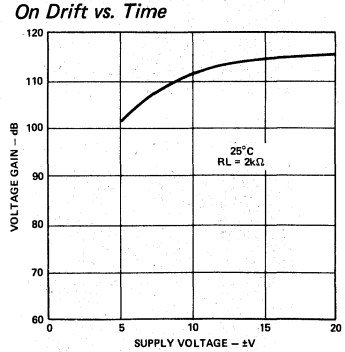


Figure 11. Open Loop Voltage Gain vs. Supply Voltage

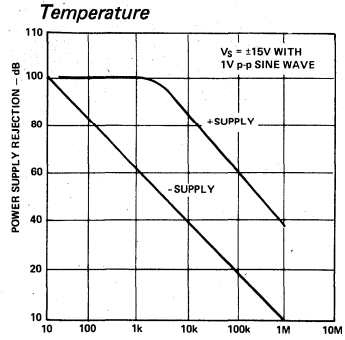


Figure 12. Power Supply Rejection vs. Frequency

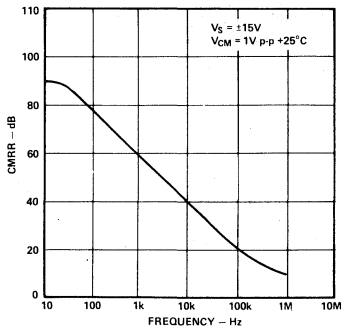


Figure 13. Common Mode Rejection vs. Frequency

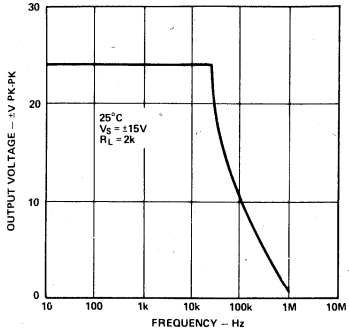


Figure 14. Large Signal Frequency Response

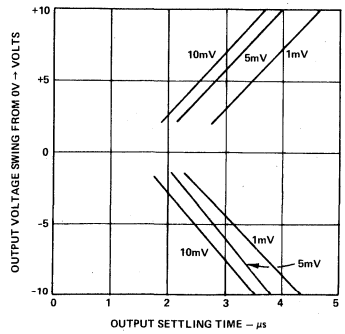


Figure 15. Output Settling Time vs. Output Swing and Error (Circuit of Figure 23)

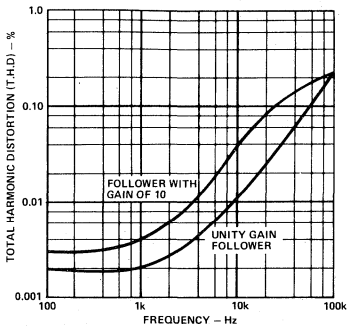


Figure 16. Total Harmonic Distortion vs. Frequency

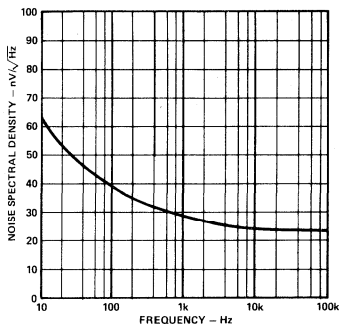


Figure 17. Input Noise Voltage Spectral Density

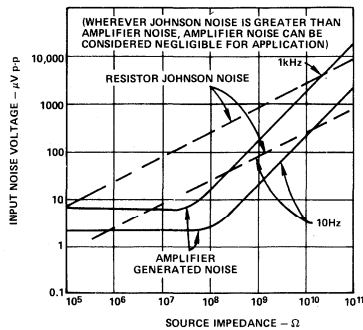
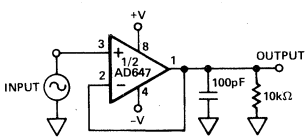
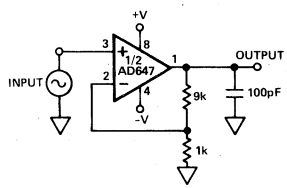


Figure 18. Total rms Noise vs. Source Resistance



a. Unity Gain Follower



b. Follower with Gain = 10

Figure 19. T.H.D. Test Circuits

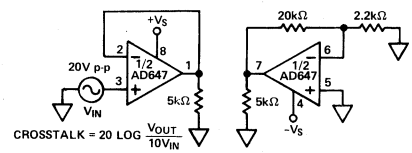


Figure 20. Crosstalk Test Circuit

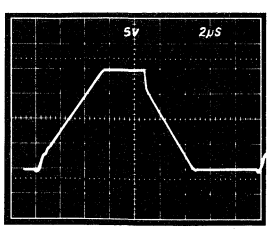


Figure 21a. Unity Gain Follower Pulse Response (Large Signal)

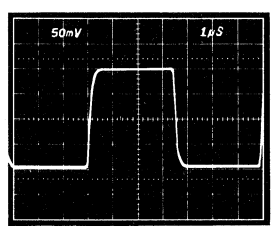


Figure 21b. Unity Gain Follower Pulse Response (Small Signal)

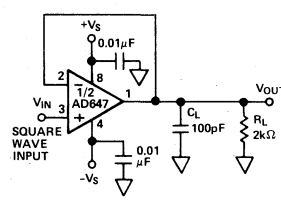


Figure 21c. Unity Gain Follower

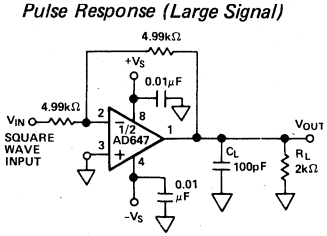


Figure 22a. Unity Gain Inverter

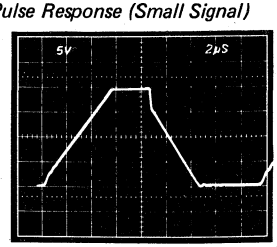


Figure 22b. Unity Gain Inverter Pulse Response (Large Signal)

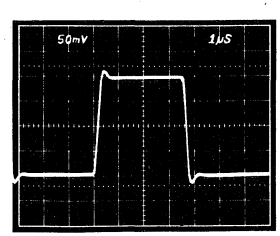


Figure 22c. Unity Gain Inverter Pulse Response (Small Signal)

ANALOG DEVICES

Low Cost High Accuracy IC Op Amps

AD741 SERIES

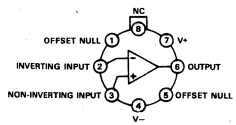
4

FEATURES

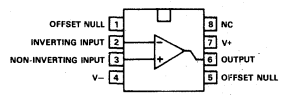
Precision Input Characteristics
- Low V_{OS}: 0.5mV max (L)
- Low V_{OS} Drift: 5μV/°C max (L)
- Low I_b: 50nA max (L)
- Low I_{OS}: 5nA max (L)
- High CMRR: 90dB min (K, L)

High Output Capability
- A_{OL} = 25,000 min, 1kΩ load (J, S)
  T_{min} to T_{max}
- V_O = ±10V min, 1kΩ load (J, S)

AD741 SERIES FUNCTIONAL DIAGRAMS



TO-99
TOP VIEW



8-PIN MINI DIP
TOP VIEW

GENERAL DESCRIPTION

The Analog Devices AD741 series are high performance monolithic operational amplifiers. All the devices feature full short circuit protection and internal compensation.

The Analog Devices AD741J, AD741K, AD741L and AD741S are specially tested and selected versions of the standard AD741 operational amplifier. Improved processing and additional electrical testing guarantee the user precision performance at a very low cost. The AD741J, K and L substantially increase overall accuracy over the standard AD741C by providing maximum limits on offset voltage drift and significantly reducing the errors due to offset voltage, bias current, offset current, voltage gain, power supply rejection, and common mode rejection. For example, the AD741L features maximum offset voltage drift of 5μV/°C, offset voltage of 0.5mV max, offset current of 5nA max, bias current of 50nA max, and a CMRR of 90dB min. The AD741S offers guaranteed performance over the extended temperature range of -55°C to +125°C, with max offset voltage drift of 15μV/°C, max offset voltage of 4mV, max offset current of 25nA, and a minimum CMRR of 80dB.

HIGH OUTPUT CAPABILITY

Both the AD741J and AD741S offer the user the additional advantages of high guaranteed output current and gain at low values of load impedance. The AD741J guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from 0 to +70°C. The AD741S guarantees a minimum gain of 25,000 swinging ±10V into a 1kΩ load from −55°C to +125°C.

All devices feature full short circuit protection, high gain, high common mode range, and internal compensation. The AD741J, K and L are specified for operation from 0 to +70°C, and are available in both the TO-99 and mini-DIP packages. The AD741S is specified for operation from −55°C to +125°C, and is available in the TO-99 package.

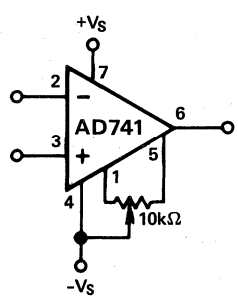
SPECIFICATIONS (typical @ +25°C and ±15V dc, unless otherwise specified)

Model	AD741C Min	AD741C Typ	AD741C Max	AD741 Min	AD741 Typ	AD741 Max	AD741J Min	AD741J Typ	AD741J Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	20,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	15,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max							±10	±13		V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13					V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Response (Unity Gain)										
Rise Time $C_L \leq$ 10V p-p		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq$ 10kΩ, Adj. to Zero		1.0	6.0		1.0	5.0		1.0	3.0	mV
T_A = min to max		1.0	7.5		1.0	6.0			4.0	mV
Average vs. Temperature (Untrimmed)									20	μV/°C
vs. Supply, T_A = min to max								30	100	μV/V
INPUT OFFSET CURRENT										
Initial		20	200		20	200		5	50	nA
T_A = min to max		40	300		85	500			100	nA
Average vs. Temperature								0.1		nA/°C
INPUT BIAS CURRENT										
Initial		80	500		80	500		40	200	nA
T_A = min to max		120	800		300	1,500			400	nA
Average vs. Temperature								0.6		nA/°C
INPUT IMPEDANCE DIFFERENTIAL	0.3	2.0		0.3	2.0			1.0		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe									±30	V
Common Mode, max Safe	±12	±13		±12	±13			±15		V
Common Mode Rejection, $R_S \leq$ 10kΩ, T_A = min to max, V_{IN} = ±12V	70	90		70	90		80	90		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating							±5		±18	V
Power Supply Rejection Ratio		30	150		30	150				μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.2	3.3	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min					60	100				mW
T_A = max					45	75				mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	-55		+125	0		+70	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTES

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.



Standard Nulling Offset Circuit

Model	AD741K Min	AD741K Typ	AD741K Max	AD741L Min	AD741L Typ	AD741L Max	AD741S Min	AD741S Typ	AD741S Max	Units
OPEN LOOP GAIN										
R_L = 1kΩ, V_O = ±10V							50,000	200,000		V/V
R_L = 2kΩ, V_O = ±10V	50,000	200,000		50,000	200,000					V/V
T_A = min to max R_L = 2kΩ	25,000			25,000			25,000			V/V
OUTPUT CHARACTERISTICS										
Voltage @ R_L = 1kΩ, T_A = min to max										V
Voltage @ R_L = 2kΩ, T_A = min to max	±10	±13		±10	±13		±10	±13		V
Short Circuit Current		25			25			25		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			1			1		MHz
Full Power Response		10			10			10		kHz
Slew Rate		0.5			0.5			0.5		V/μs
Transient Respone (Unity Gain)										
Rise Time		0.3			0.3			0.3		μs
Overshoot		5.0			5.0			5.0		%
INPUT OFFSET VOLTAGE										
Initial, $R_S \leq 10k\Omega$, Adj. to Zero		0.5	2.0		0.2	0.5		1.0	2	mV
T_A = min to max			3.0			1.0			4	mV
Average vs. Temperature (Untrimmed)		6.0	15.0		2.0	5.0		6.0	15.0	μV/°C
vs. Supply, T_A = min to max		5	15.0		5	15.0		30	100	μV/V
INPUT OFFSET CURRENT										
Initial		2	10		2	5		2	10	nA
T_A = min to max			15			10			25	nA
Average vs. Temperature		0.02	0.2		0.02	0.1		0.1	0.25	nA/°C
INPUT BIAS CURRENT										
Initial		30	75		30	50		30	75	nA
T_A = min to max			120			100			250	nA
Average vs. Temperature		0.6	1.5		0.6	1.0		0.6	2.0	nA/°C
INPUT IMPEDANCE DIFFERENTIAL		2			2			2		MΩ
INPUT VOLTAGE RANGE[1]										
Differential, max Safe		±30			±30			±30		V
Common Mode max Safe		±15			±15			±15		V
Common Mode Rejection,										
$R_S \leq 10k\Omega$, T_A = min to max										
V_{IN} = ±12V	90	100		90	100		90	100		dB
POWER SUPPLY										
Rated Performance		±15			±15			±15		V
Operating	±5		±22	±5		±22	±5		±22	V
Power Supply Rejection Ratio										μV/V
Quiescent Current		1.7	2.8		1.7	2.8		2.0	2.8	mA
Power Consumption		50	85		50	85		50	85	mW
T_A = min								60	100	mW
T_A = max								75	115	mW
TEMPERATURE RANGE										
Operating Rated Performance	0		+70	0		+70	-55		+125	°C
Storage	-65		+150	-65		+150	-65		+150	°C

NOTES

[1] For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Temperature Range	Package[1]	Initial Off-Set Voltage
AD741CN	0 to +70°C	MINI-DIP (N8A)	6.0mV
AD741CH	0 to +70°C	TO-99	6.0mV
AD741JN	0 to +70°C	MINI-DIP (N8A)	3.0mV
AD741JH	0 to +70°C	TO-99	3.0mV
AD741KN	0 to +70°C	MINI-DIP (N8A)	2.0mV
AD741KH	0 to +70°C	TO-99	2.0mV
AD741LN	0 to +70°C	MINI-DIP (N8A)	0.5mV
AD741LH	0 to +70°C	TO-99	0.5mV
AD741H	-55°C to +125°C	TO-99	5.0mV
AD741SH	-55°C to +125°C	TO-99	2.0mV

NOTE

[1] See Section 19 for package outline information.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings	AD741, J, K, L, S	AD741C
Supply Voltage	±22V	±18V
Internal Power Dissipation	500mW[1]	500mW
Differential Input Voltage	±30V	±30V
Input Voltage	±15V	±15V
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (soldering, 60 seconds)	300°C	300°C
Output Short Circuit Duration	Indefinite[2]	Indefinite

NOTES

[1] Rating applies for case temperature to +125°C. Derate TO-99 linearity at 6.5mW/°C for ambient temperatures above +70°C.

[2] Rating applies for shorts to ground or either supply at case temperatures to +125°C or ambient temperatures to +75°C.

Typical Performance Curves

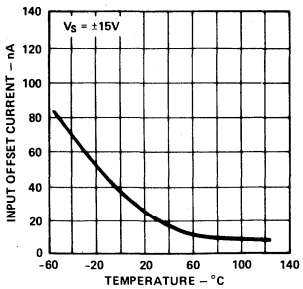


Figure 1. Offset Current vs. Temperature

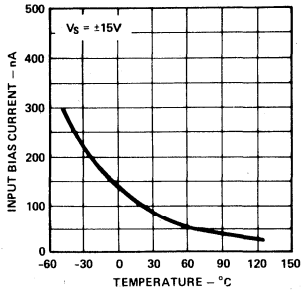


Figure 2. Bias Current vs. Temperature

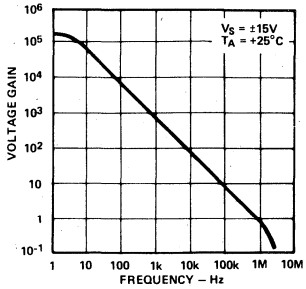


Figure 3. Open Loop Gain vs. Frequency

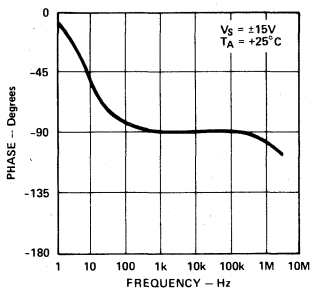


Figure 4. Open Loop Phase Response vs. Frequency

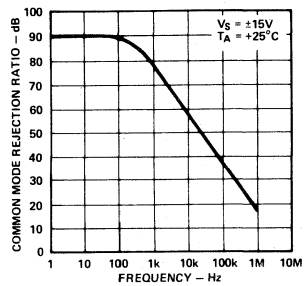


Figure 5. Common Mode Rejection vs. Frequency

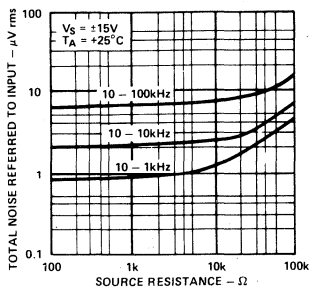


Figure 6. Broad Band Noise vs. Source Resistance

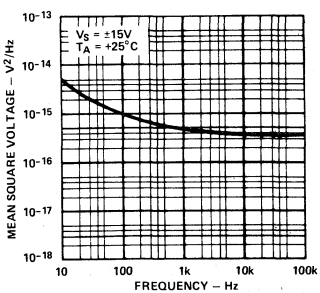


Figure 7. Input Noise Voltage vs. Frequency

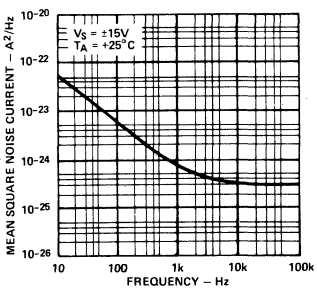


Figure 8. Input Noise Current vs. Frequency

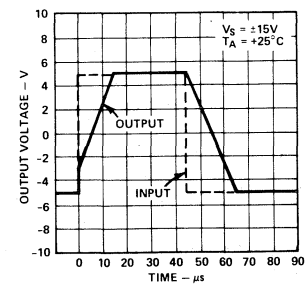


Figure 9. Voltage Follower Large Signal Pulse Response

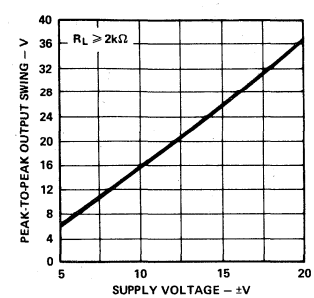


Figure 10. Output Voltage Swing vs. Supply Voltage

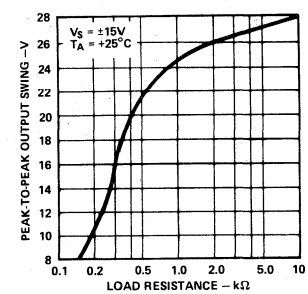


Figure 11. Output Voltage Swing vs. Load Resistance

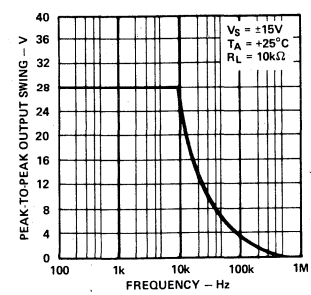


Figure 12. Output Voltage Swing vs. Frequency

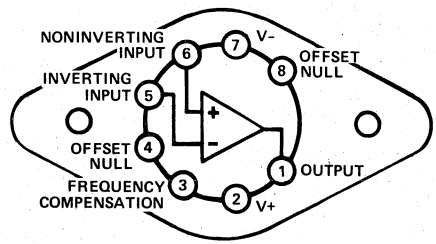
Fast-Settling, Wideband, FET-Input Op Amp

AD3554

FEATURES

Very High Slew Rate: 1000V/μs
Fast Settling: 150ns max to ±0.05%
Gain Bandwidth Product: 1.7GHz typical
High Output Current: 100mA min @ V_{OUT} = 10V
Full Differential Input

AD3554 FUNCTIONAL BLOCK DIAGRAM



TO-3 STYLE
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD3554 is a FET-input, hybrid operational amplifier that features an excellent combination of high slew rate, fast settling time and large gain-bandwidth product. The AD3554 has a full differential input with matched input FETs for low offset voltage.

The AD3554 can supply ±100mA at 10 volts. The slew rate is 1000V/μs minimum; 1200V/μs is typical. Settling time to ±0.05% of final value is only 150ns when configured as an inverting amplifier. The user can optimize the combination of bandwidth, slew rate, and settling time for a particular application by selecting the external compensation capacitor.

The AD3554 is recommended for any operational amplifier application where speed and bandwidth are important considerations. The high slew rate and fast settling time make the AD3554 an excellent choice for use in fast D/A converters, fast current amplifiers, integrators, waveform generators and multiplexer buffers.

The AD3554 is available in three versions: the "A" and "B" are specified over the -25°C to +85°C temperature range and "S" over the -55°C to +125°C operating temperature range. All devices are packaged in the hermetically-sealed TO-3 style metal can.

The AD3554 is a pin-compatible replacement for 3554 devices from other manufacturers.

PRODUCT HIGHLIGHTS

1. The high slew rate (1000V/μs min) and fast settling time to 0.01% (250ns max) make the AD3554 ideal for D/A, A/D, sample-hold, and video instrumentation circuits.
2. Laser trimming techniques reduce initial offset voltage to as low as 1mV max (AD3554B), thus eliminating the need for external nulling in many applications.
3. Very high gain-bandwidth product (1.7GHz typical at A = 1000) makes the AD3554 an ideal choice for high frequency amplifier applications.
4. FET inputs result in a low bias current (50pA max, 10pA typ) in a high gain-bandwidth product operational amplifier.
5. Full differential input makes the AD3554 ideal for all standard operational amplifier applications such as high speed integrators, differentiators, and high gain amplifiers.
6. The 100mA at 10V output makes the AD3554 suitable for many applications that require high output power, such as cable drivers. The capacitance of coaxial cable (e.g., 29pF/foot for RG-58) does not load the AD3554 when the coaxial cable or transmission line is terminated in its characteristic impedance.

SPECIFICATIONS (typical @ T_{CASE} = +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD3554AM	AD3554BM	AD3554SM
OPEN LOOP GAIN			
No Load	106dB (100dB min)	*	*
R_L = 100Ω	96dB (90dB min)	*	*
OUTPUT CHARACTERISTICS			
Voltage @ I_O = ±100mA	±11V (±10V min)	*	*
Output Resistance, Open Loop @ f = 10MHz	20Ω		
Current @ V_O = ±10V	±125mA (±100mA min)	*	*
FREQUENCY RESPONSE			
Bandwidth (0dB, Small Signal, C_F = 0)[1]	90MHz (70MHz min)	*	*
Gain-Bandwidth Product, C_F = 0			
G = 10V/V	225MHz (150MHz min)	*	*
G = 100V/V	725MHz (425MHz min)	*	*
G = 1000V/V	1700MHz (1000MHz min)	*	*
Full Power Bandwidth, C_F = 0, V_O = 20V p-p, R_L = 100Ω	19MHz (16MHz min)	*	*
Slew Rate, C_F = 0, V_O = 20V p-p, R_L = 100Ω	1200V/μs (1000V/μs min)	*	*
Settling Time, A = −1, to ±1%	60ns	*	*
to ±0.1%	120ns	*	*
to ±0.05%	140ns (150ns max)	*	*
to ±0.01%	200ns (250ns max)	*	*
INPUT OFFSET VOLTAGE			
Initial Offset	0.5mV (2.0mV max)	0.2mV (1.0mV max)	**
vs. Temperature	20μV/°C (50μV/°C max)	8μV/°C (15μV/°C max)	12μV/°C (25μV/°C max)
vs. Supply, T_A = min to max	80μV/V (300μV/V max)	*	*
INPUT BIAS CURRENT			
Either Input[2]	10pA (50pA max)	*	*
Initial Difference	2pA (10pA max)	*	*
vs. Supply Voltage	1pA/V	*	*
INPUT IMPEDANCE			
Differential	10^{11} Ω‖2pF	*	*
Common Mode	10^{11} Ω‖2pF	*	*
INPUT VOLTAGE RANGE			
Max Safe Input Voltage, Diff	±($\|V_{CC}\|$−8)	*	*
Common Mode	±($\|V_{CC}\|$−4)	*	*
Common Mode Rejection, V_{CM} = +7V, −10V	78dB (60dB min)	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(7 to 18)V	*	*
Quiescent Current	28mA (45mA max)	*	*
INPUT NOISE[1]			
Voltage, f_o = 1Hz	125nV/√Hz (450nV/√Hz max)	*	*
f_o = 10Hz	50nV/√Hz (160nV/√Hz max)	*	*
f_o = 100Hz	25nV/√Hz (90nV/√Hz max)	*	*
f_o = 1kHz	15nV/√Hz (50nV/√Hz max)	*	*
f_o = 10kHz	10nV/√Hz (35nV/√Hz max)	*	*
f_o = 100kHz	8nV/√Hz (25nV/√Hz max)	*	*
f_o = 1MHz	7nV/√Hz (25nV/√Hz max)	*	*
f_B = 0.3Hz to 10Hz	2μV p-p (7μV p-p max)	*	*
f_B = 10Hz to 1MHz	8μV rms (25μV rms max)	*	*
Current, f_B = 3Hz to 10Hz	45fA p-p	*	*
f_B = 10Hz to 1MHz	2pA rms	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	−25°C to +85°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*
PACKAGE[3] — TO-3 Style (H08C)	AD3554AM	AD3554BM	AD3554SM

NOTES

[1] These parameters are untested and not guaranteed. This specification is established to a 90% confidence level.

[2] Bias Current specifications are guaranteed maximum at either input at T_{CASE} = +25°C. For higher temperatures, the current doubles every 10°C.

[3] See Section 19 for package outline information.

*Specifications same as AD3554AM.

**Specifications same as AD3554BM.

Specifications subject to change without notice.

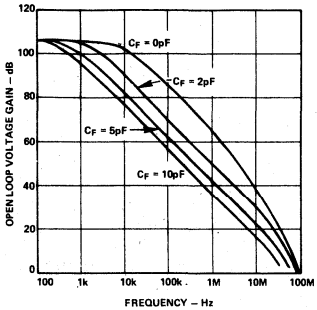


Figure 1. Open Loop Frequency Response (Voltage Gain)

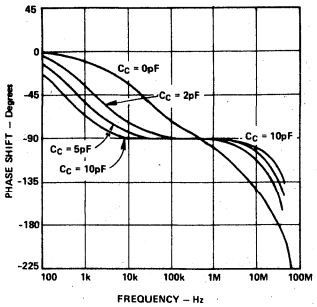


Figure 2. Open Loop Frequency Response (Phase Shift)

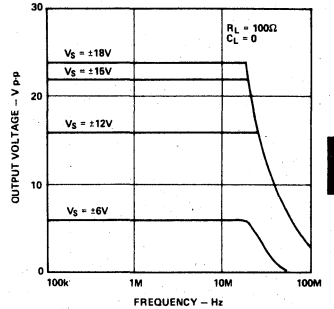


Figure 3. Output Voltage vs. Frequency

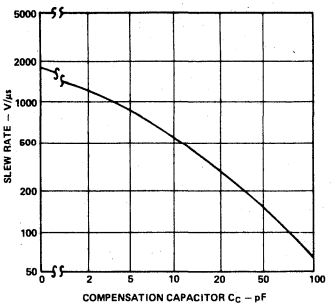


Figure 4. Slew Rate vs. Compensation

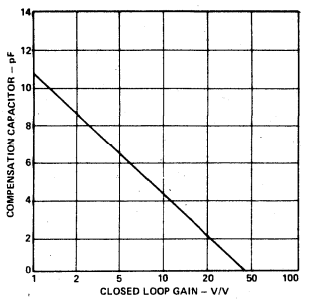


Figure 5. Recommended Compensation Capacitor vs. Closed Loop Gain

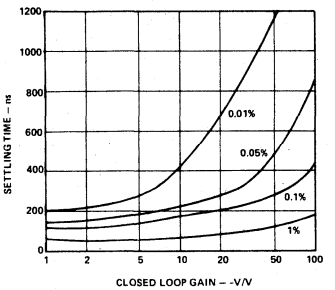


Figure 6. Settling Time vs. Closed Loop Gain (Circuit of Figure 18A)

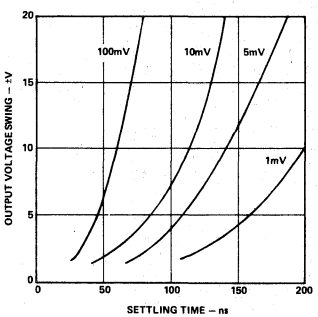


Figure 7. Settling Time vs. Output Voltage Change (Circuit of Figure 18A)

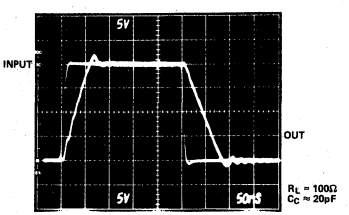


Figure 8. Voltage Follower Large Signal Response

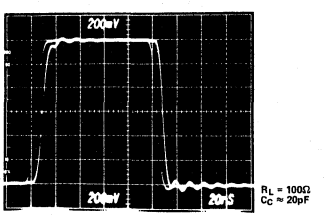


Figure 9. Voltage Follower Small Signal Response

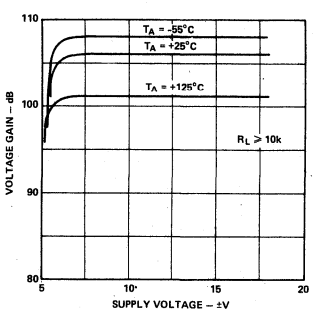


Figure 10. Open Loop Gain vs. Supply Voltage

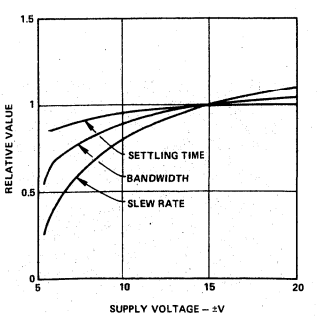


Figure 11. Dynamic Characteristics vs. Supply Voltage

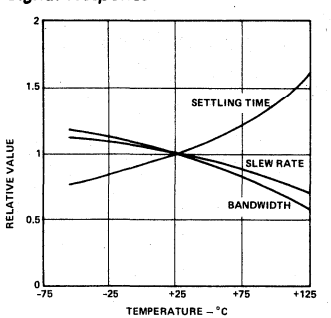


Figure 12. Dynamic Characteristics vs. Temperature

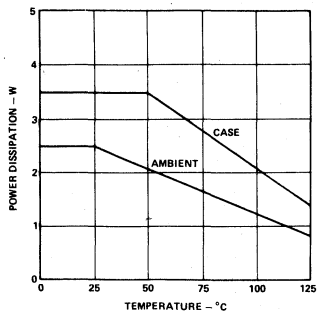


Figure 13. Power Dissipation vs. Temperature

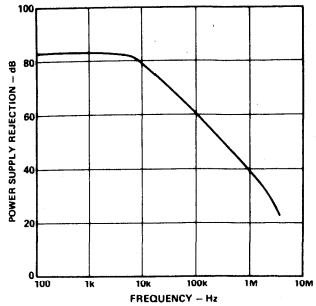


Figure 14. PSRR vs. Frequency

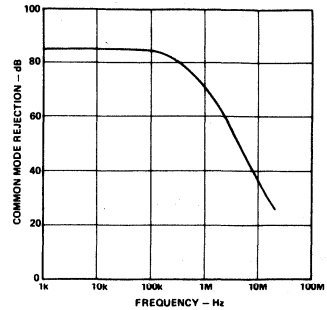


Figure 15. CMRR vs. Frequency

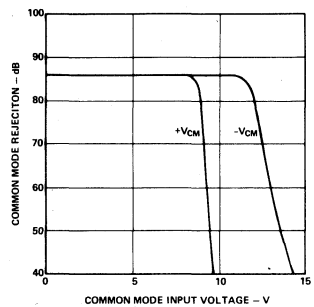


Figure 16. Common Mode Rejection vs. Input Voltage

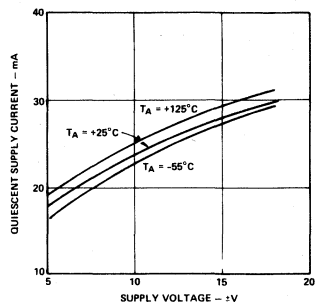


Figure 17. Quiescent Supply Current vs. Supply Voltage

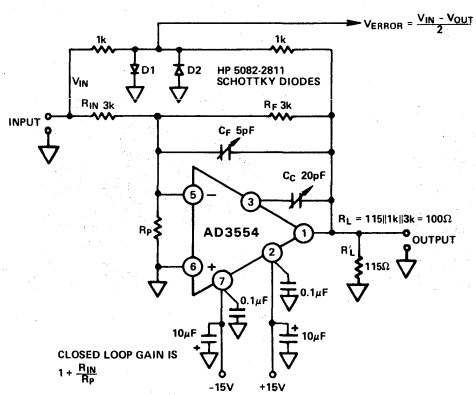


Figure 18A. Settling Time Test Circuit Schematic

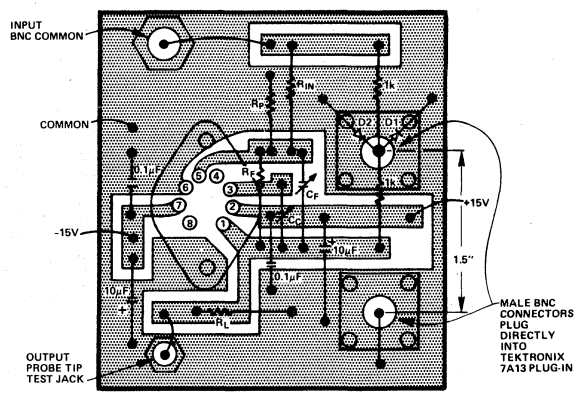


Figure 18B. Settling Time Test Circuit Layout

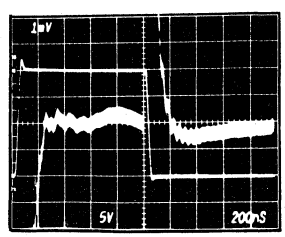


Figure 18C. Unity Gain Inverter Settling Time

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling and stray capacitance.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical, particularly to the inverting input, which is especially sensitive to stray capacitances.

Low value resistors should be used to assure that the time constants formed with the circuit capacitances will not limit the amplifier performance. Resistor values less than 5.6kΩ are recommended.

Each power supply lead should be bypassed to ground as close as possible to the amplifier pins. A 10μF electrolytic or tantalum capacitor in parallel with a 0.01μF ceramic capacitor is recommended.

GROUNDING

Grounding the case will add a slight capacitance to each pin. Therefore, we recommend leaving the case ungrounded.

In inverting applications we recommend grounding the non-inverting input rather than connecting it to a bias current compensating resistor. FET input amplifiers do not require compensating resistors because of their low input bias currents.

GUARDING

In high input impedance applications the input terminals may be surrounded by a conductive path to divert leakage currents. This guard ring should be connected to a low impedance point at the input signal potential.

In high frequency applications guarding may not be desirable as it increases the risk of oscillation due to increased printed circuit board capacitance.

COMPENSATION

The user can optimize the bandwidth, slew rate, or settling time by selecting the external frequency compensation capacitor. No compensation capacitor is required for closed loop gains above 50 and when the load capacitance is less than 100pF. When driving capacitive loads greater than 470pF, in low closed loop gain configurations, connect a 1000pF capacitor between pin 8 and the positive supply. The performance may be improved by connecting a small resistor in series with the output and a small capacitor from pin 1 to 5. See Typical Circuits.

The flat high frequency response of the AD3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin.

The selected compensation capacitor may be a trimmer, a fixed capacitor or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed loop gain.

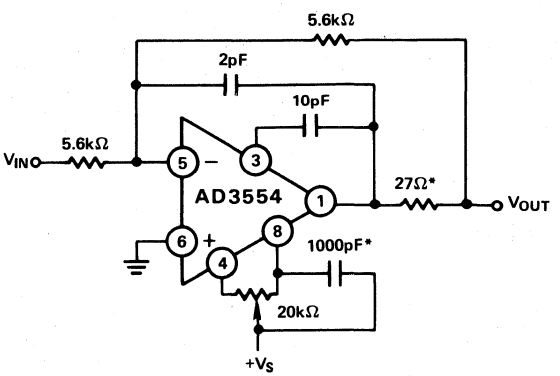
SHORT CIRCUIT PROTECTION

The AD3554 is short circuit protected for continuous output shorts to ground. Output shorts to either supply will destroy the device.

HEAT SINKING

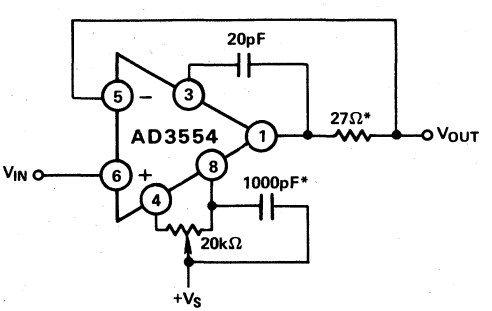
The AD3554 does not require heat sinking for most applications. However, at extreme temperature and full load conditions a heat sink will be necessary as indicated in the maximum power dissipation curve. We recommend connecting the heat sink to the amplifier case and keeping the combination ungrounded.

TYPICAL CIRCUITS



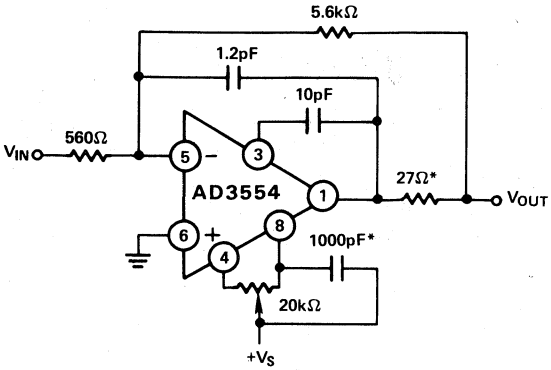
*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 19. Unity Gain Inverter



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 20. Follower



*THESE COMPONENTS MAY BE ELIMINATED WHEN NOT DRIVING LARGE CAPACITIVE LOADS.

Figure 21. Inverting Gain of 10 Amplifier

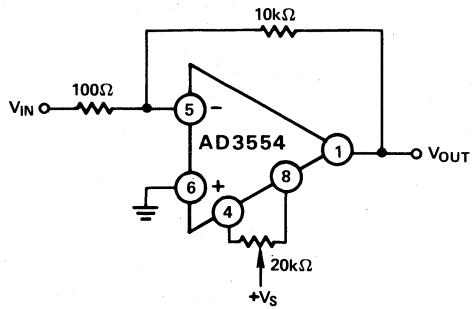


Figure 22. Inverting Gain of 100 Amplifier

AD9685/AD9687

FEATURES

2.2ns Propagation Delay – AD9685BD/BH
2.7ns Propagation Delay – AD9687BD
0.5ns Latch Set-Up Time
Pin-Compatible to Am685/687 but FASTER
+5V, −5.2V Supply Voltages

APPLICATIONS

Ultra-High-Speed A/D Converters
Ultra-High-Speed Line Receivers
Peak Detectors
Threshold Detectors

GENERAL DESCRIPTION

The AD9685BD/BH and AD9687BD are ultra-fast comparators manufactured with a high performance bipolar process which makes it possible to obtain incredibly short propagation delays and latch set-up times.

The AD9685BD/BH is a single comparator which is pin-compatible with the Am685, but has speed capabilities that far outstrip the earlier unit. The AD9687BD is pin-for-pin compatible with the Am687 and, like its predecessor, is a dual comparator; its speed capabilities are far superior to the Am687.

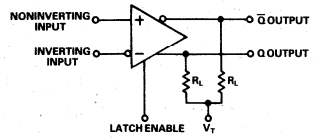
Both Analog Devices units have differential inputs and complementary outputs fully compatible with ECL logic levels. Their output current levels are capable of driving 50Ω terminated transmission lines, and their high resolution make them ideally suited for a variety of analog-to-digital signal processing applications.

AD9685BD/BH Single Comparator

A latch function allows the AD9685BD/BH to be operated in a sample-hold mode. When the Latch Enable (LE) is ECL HIGH, the comparator functions normally. When the Latch Enable is driven LOW, its outputs are locked in the logic state dictated by the input conditions at the time of the latch input transition. If the latch function is not used, the Latch Enable input should be connected to ground.

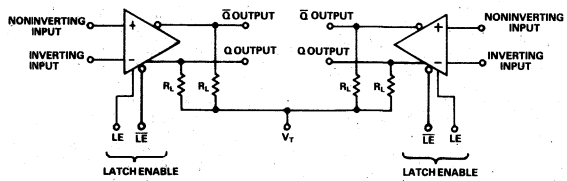
In addition to its speed advantages over the earlier Am685, the AD9685BD/BH also dissipates less power because it operates on a positive 5 volt supply instead of the 6 volts required by the AMD device.

AD9685BD/BH FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD FUNCTIONAL BLOCK DIAGRAM



THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200ΩCONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

AD9687BD Dual Comparator

The latch function of the AD9687BD provides an ability to operate the unit in either a track-hold or sample-hold mode. The latch function inputs are separated on the two comparators and are designed to be driven from the complementary outputs of a standard ECL logic gate. When LE is High and $\overline{LE}$ is LOW, the normal comparator function is in operation. When LE is forced LOW and $\overline{LE}$ is driven HIGH, the outputs of the comparator being exercised are locked in their existing logical states, as determined by the input conditions present at the time of arrival of the latch signal. If the latch function is not used on either one of the two comparators in the AD9687BD, the appropriate Latch Enable input should be connected to ground; the companion $\overline{\text{Latch Enable}}$ input can be left open.

The AD9687BD is basically two AD9685BD/BH units in a single package and operates in a similar fashion to a pair of the single comparators.

SPECIFICATIONS (typical @ +25°C with nominal supply voltages unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS	AD9685BD/BH	AD9687BD
Supply Voltages (V_{CC} and V_{EE})	±6V	*
Power Dissipation	336mW	500mW
Input Voltage	±5V	*
Differential Input Voltage	3.5V	*
Output Current	30mA	*
Operating Temperature Range	−30°C to +85°C	*
Storage Temperature Range	−55°C to +150°C	*
Lead Temperature (soldering, 10 seconds)	300°C	*

ELECTRICAL CHARACTERISTICS	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Input Offset Voltage[1]	V_{OS}	−5		+5	*		*	mV
Temperature Coefficient	$\Delta V_{OS}/\Delta T$		20			*		µV/°C
Input Offset Current	I_{OS}			5			*	µA
Input Bias Current	I_B		10	20		*	*	µA
Input Voltage Range	V_{CM}	−2.5		+2.5	*		*	V
Common Mode Rejection Ratio	CMRR	80			*			dB
Input Resistance	R_{IN}	60			*			kΩ
Input Capacitance	C_{IN}		3			*		pF
Input/Output Logic Levels								
Output HIGH Voltage	V_{OH}	−0.96		−0.81	*		*	V
Output LOW Voltage	V_{OL}	−1.85		−1.65	*		*	V
Positive Supply Voltage	V_{CC}	+4.75	+5	+5.25	*	*	*	V
Negative Supply Voltage	V_{EE}	−4.95	−5.2	−5.45	*	*	*	V
Positive Supply Current	I_{CC}		19	23		30		mA
Negative Supply Current	I_{EE}		23	34		54		mA
Supply Voltage Rejection Ratio	S_{VRR}		60			*		dB
Power Dissipation	P_{DISS}		210	300		430		mW
SWITCHING CHARACTERISTICS								
Propagation Delays[2]								
Input to Output HIGH	$t_{pd}+$		2.2	3		2.7	4	ns
Input to Output LOW	$t_{pd}-$		2.2	3		2.7	4	ns
Latch Enable to Output HIGH	$t_{pd}+(E)$		2.5	3		2.7	4	ns
Latch Enable to Output LOW	$t_{pd}-(E)$		2.5	3		2.7	4	ns
Latch Enable								
Pulse Width	$t_{pw}(E)$	3	2		*	*		ns
Minimum Set-Up Time	t_s		0.5	1		*	*	ns
Minimum Hold Time	t_h			1			*	ns

NOTES
[1]R_S = 100 ohms
[2]Propagation delays measured with 100mV pulse; 5mV overdrive.
*Specifications same as AD9685BD/BH.

Specifications subject to change without notice.

DEFINITION OF TERMS

V_{OS} INPUT OFFSET VOLTAGE – The potential difference required between the input terminals to obtain zero potential difference between the outputs.

I_{OS} INPUT OFFSET CURRENT – The difference between the currents into the inputs when there is zero potential difference between the outputs.

I_B INPUT BIAS CURRENT – The average of the two input currents. This is a chip design trade-off parameter. Internally, it is desirable to have high values of I_B for circuit performance requirements; externally, it is desirable to have I_B as low as possible.

V_{CM} INPUT VOLTAGE RANGE – The range of input voltages for which offset and propagation delay specifications are valid.

CMRR COMMON MODE REJECTION RATIO – The ratio of input voltage range to the peak-to-peak change in input offset voltage over that range.

R_{IN} INPUT RESISTANCE – The resistance looking into either terminal with the other grounded.

C_{IN} INPUT CAPACITANCE – The capacitance looking into either input pin with the other grounded.

V_{OH} OUTPUT HIGH VOLTAGE – The logic HIGH output voltage with an external pull-down resistor returned to a negative supply.

V_{OL} OUTPUT LOW VOLTAGE – The logic LOW output voltage with an external pull-down resistor returned to a negative supply.

I_{CC} POSITIVE SUPPLY CURRENT – The current required from the positive supply to operate the comparator.

I_{EE} NEGATIVE SUPPLY CURRENT – The current required from the negative supply to operate the comparator.

S_{VRR} SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

P_{DISS} POWER DISSIPATION – The power dissipated by the comparator with both outputs terminated in 50 ohms to −2V.

$t_{pd}+$ INPUT TO OUTPUT HIGH DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

$t_{pd}-$ INPUT TO OUTPUT LOW DELAY – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd}+(E)$ LATCH ENABLE TO OUTPUT HIGH DELAY – The propagation delay measured from the 50% point of the Latch Enable (LE) signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd}-(E)$ LATCH ENABLE TO OUTPUT LOW DELAY – The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

$t_{pw}(E)$ MINIMUM LATCH ENABLE PULSE WIDTH – The minimum time the Latch Enable signal must be HIGH to acquire and hold an input signal.

t_s MINIMUM SET-UP TIME – The minimum time before the negative transition of the Latch Enable pulse that an input signal must be present to be acquired and held at the outputs.

t_h MINIMUM HOLD TIME – The minimum time after the negative transition of the Latch Enable signal that an input signal must remain unchanged to be acquired and held at the outputs.

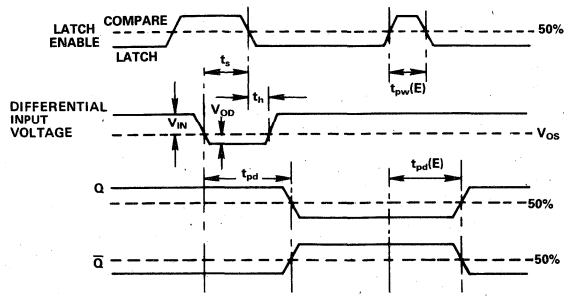
OTHER SYMBOLS

T_C	Case Temperature	V_T	Output load terminating voltage
R_S	Input source resistance	R_L	Output load resistance
V_S	Supply voltages	V_{IN}	Input pulse amplitude
V_{CC}	Positive supply voltage	V_{OD}	Input overdrive
V_{EE}	Negative supply voltage	f	Frequency

TIMING DIAGRAM

The Timing Diagram illustrates a series of events in the AD9685BD/BH; the terms and their relationships are also valid for the AD9687BD. The relationships which are shown should not be interpreted as "typical", since several parameters have multiple values; and the worst case conditions are shown in the Timing Diagram.

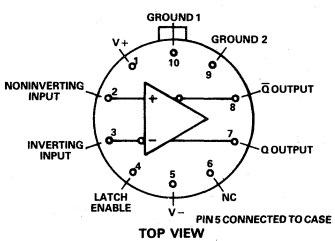
The top line of the diagram shows two Latch Enable (LE) pulses; each is high for "compare" and low for "latch". The first pulse illustrates the compare function in which part of the input action takes place during the "compare" mode. The second one illustrates a compare function interval during which there is no change in input.



The leading edge of the input signal, shown here as a large amplitude, small overdrive pulse, switches the comparator after a time interval t_{pd}. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch trailing (falling) edge and, to be acquired, must be maintained for a time t_h after that edge. After t_h, the output is no longer affected by the input status until the latch is again strobed. A minimum latch pulse width of tpw(E) is required for the strobe operation, and the output transitions occur after a time $t_{pd}(E)$.

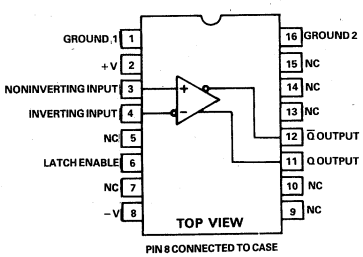
PIN CONFIGURATIONS

TO-100



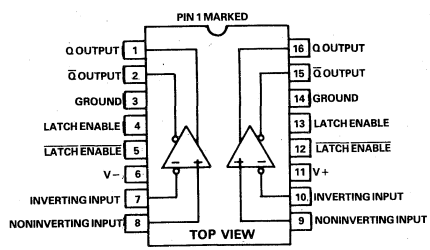
AD9685BH Pin Configuration Package Option[1] — TO-100

DIP



AD9685BD Pin Configuration Package Option[1] — Q16C

DIP



AD9687BD Pin Configuration Package Option[1] — D16A

NOTE
[1] See Section 19 for package outline information.

ANALOG DEVICES

Ultra Fast FET Operational Amplifier

ADLH0032G/ADLH0032CG

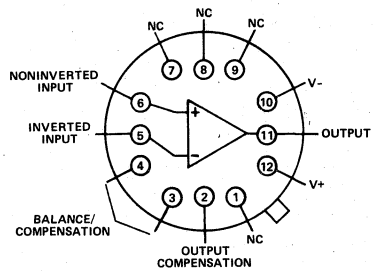
FEATURES

- 2nd Source; Replaces All LH0032G
- High Slew Rate; 500V/μs
- Wide 70MHz Bandwidth
- Operation Guaranteed -55°C to +125°C (ADLH0032G)
- High Input Impedance of $10^{12}\Omega$
- 2mV Input Offset Voltage

APPLICATIONS

- High Speed DAC Comparators
- ADC and SHA Input Buffers
- High Speed Integrators
- Video Amplifiers

ADLH0032G/ADLH0032CG
PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The ADLH0032G and ADLH0032CG are high slew rate, high input impedance, differential operational amplifiers, suitable for numerous applications in high-speed signal processing. These second source devices are the same in every characteristic as other LH0032G/LH0032CG amplifiers, and thus are particularly suited for comparator applications due to their high allowable differential input capabilities (±15V), ease of output clamping, and high output drive capabilities.

Featuring a wide 70MHz bandwidth, high input impedance ($10^{12}\Omega$), and high output drive capacity, the ADLH0032G and ADLH0032CG have already been designed into such applications as summing amplifiers in high-speed DACs, Buffer Amps in ADCs and high-speed SHAs, as well as other applications normally reserved for special purpose video amplifiers.

The ADLH0032G is guaranteed over the extended temperature range from -55°C to +125°C, while the commercial grade ADLH0032CG is guaranteed from -25°C to +85°C. Both devices are packaged in a TO-8 metal can package.

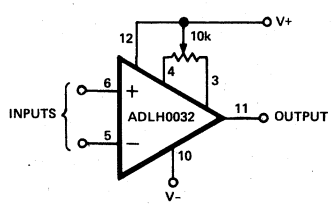


Figure 1. Offset Null

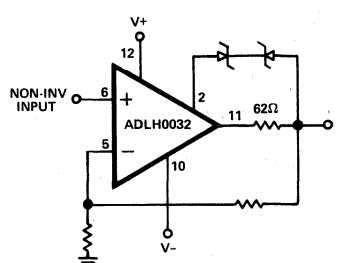


Figure 2. Output Short Circuit Protection

SPECIFICATIONS

Model		ADLH0032G, ADLH0032CG
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage		±18V
Power Dissipation		See Characteristic Curves
Differential Input Voltage		±30V
Input Voltage		$\pm V_S$
Operating Temperature Range	ADLH0032G	−55°C to +125°C
	ADLH0032CG	−25°C to +85°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (soldering, 10sec)		300°C

		ADLH0032G			ADLH0032CG			
Parameter	**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Units**
DC ELECTRICAL CHARACTERISTICS[1]								
Input Offset Voltage[2]	T_J = +25°C		2	5 10		5	15 20	mV
Input Offset Current[2]	T_J = +25°C		5	25 25		10	50 5	pA nA
Input Bias Current[2]	T_J = +25°C		10	100 50		25	200 15	pA nA
Average Offset Voltage Drift			25	50		25	50	µV/°C
Large Signal Voltage Gain	V_{OUT} = ±10V, F = 1kHz, R_L = 1kΩ, T_C = +25°C	60	70		60	70		dB
	V_{OUT} = ±10V, R_L = 1kΩ, F = 1kHz	57			57			dB
Input Voltage Range		±10	±12		±10	±12		V
Output Voltage Swing	R_L = 1kΩ	±10	±13.5		±10	±13		V
Power Supply Rejection Ratio	ΔV_S = ±10V	50	60		50	60		dB
Common Mode Rejection Ratio	ΔV_{IN} = 10V	50	60		50	60		dB
Supply Current	T_C = +25°C		18	20		20	22	mA
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	A_V = +1, ΔV_{IN} = 20V	350	500		350	500		V/µs
Settling Time to 1% of Final Value	A_V = −1, ΔV_{IN} = 20V		100			100		ns
Settling Time to 0.1% of Final Value	A_V = −1, ΔV_{IN} = 20V		300			300		ns
Small Signal Rise Time	A_V = +1, ΔV_{IN} = 1V		8	20		8	20	ns
Small Signal Delay Time	A_V = +1, ΔV_{IN} = 1V		10	25		10	25	ns
MTBF Meantime Between Failures	1.0608 X 10^7 Hours							
PACKAGE OPTION[4]			H12A			H12A		

NOTES
[1] These specifications apply for V_S = ±15V and −55°C to +125°C for the ADLH0032G and −25°C to +85°C for the ADLH0032CG.
[2] Due to high speed automatic test techniques employed these parameters are correlated to junction temperature.
[3] These specifications apply for V_S = ±15V, R_L = 1kΩ, T_C = +25°C.
[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0032CG	−25°C to +85°C
ADLH0032G	−55°C to +125°C

POWER SUPPLY DECOUPLING

The ADLH0032G/ADLH0032CG, like most high-speed circuits, are sensitive to stray capacitances and layout. Power supplies should be bypassed as near to ±V (Pins 10 and 12) as possible, using low inductance capacitors such as 0.01μF disc ceramics. Components for compensation should also be located close to the appropriate pins to reduce stray capacitances. A large ground plane area for low-impedance ground paths is highly recommended.

HEAT SINKING

The ADLH0032G/ADLH0032CG are specified for operation without any heat sink. Since internal power dissipation does create a significant temperature rise, improved bias current performance can be achieved by using a small heat sink such as the Thermalloy 2241 or equivalent. Since the case of the ADLH0032G/ADLH0032CG has no internal connection, it may be electrically connected to the heat sink. This, however, will affect the stray capacitances to all pins, therefore requiring adjustment of all circuit compensation values.

INPUT CAPACITANCE

Inverting Input:

For optimum performance, the inverting input should be compensated by a small capacitance, around 10pF, across the feedback resistor. This is because the 5pF input capacitance may cause significant time constants with high-value resistors. The capacitor value may be changed somewhat depending on the effects of layout and closed loop gain.

Noninverting Input:

To divert leakage currents away from the noninverting input and to reduce the effective input capacitance, it is desirable to bootstrap the case and/or a guard conductor to the inverting input. The resulting input capacitance of a unity gain follower configured this way will be less than 1 picofarad.

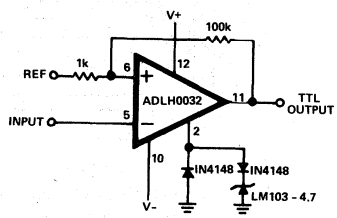


Figure 3. High Impedance, High Speed Comparator

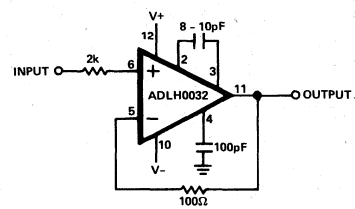


Figure 5. Unity Gain Follower

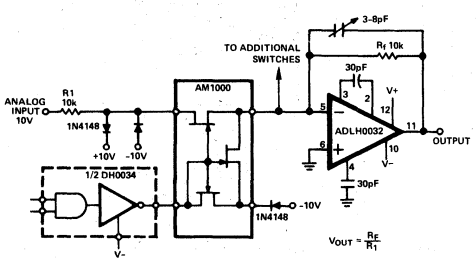


Figure 4. Current Mode Multiplexer

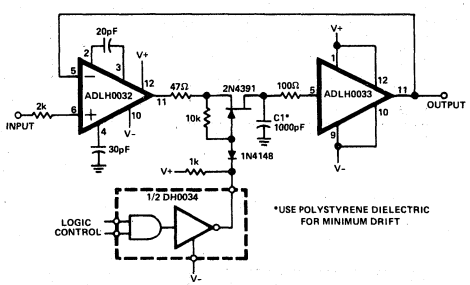
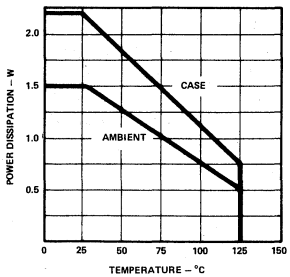
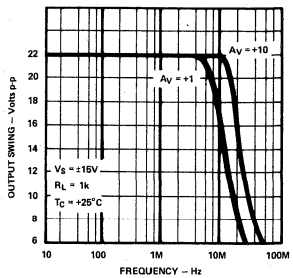


Figure 6. High Speed Sample and Hold

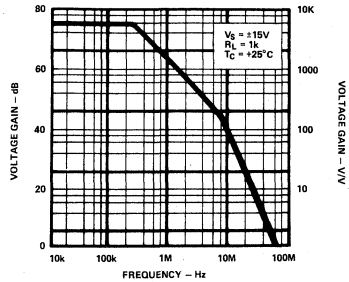
Typical Performance Curves



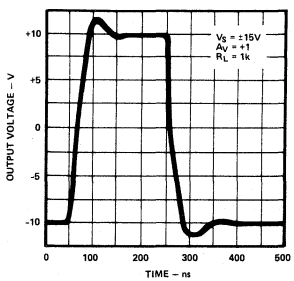
Maximum Power Dissipation



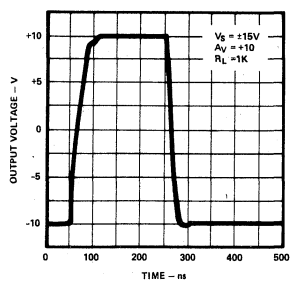
Large Signal Frequency Response



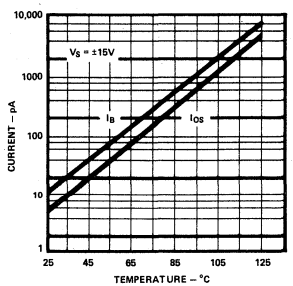
Open Loop Frequency Response



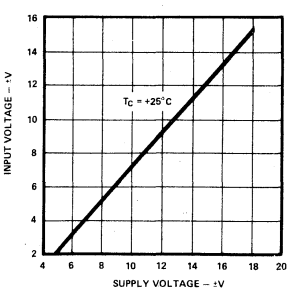
Large Signal Pulse Response



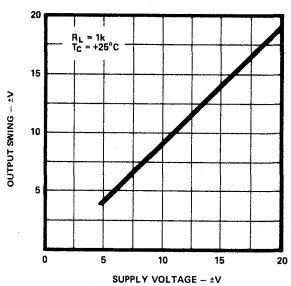
Large Signal Pulse Response



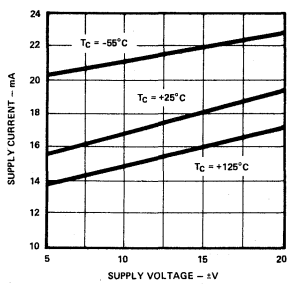
Input Bias and Offset Current vs. Temperature



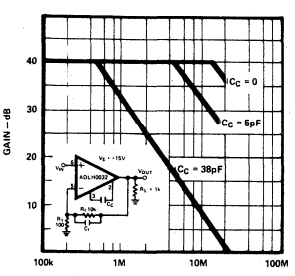
Input Voltage Range



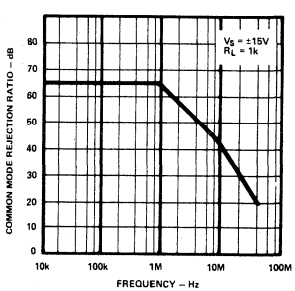
Output Swing



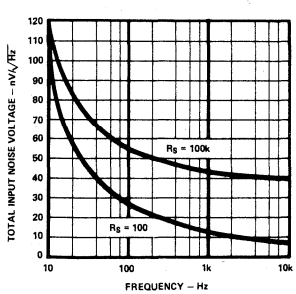
Supply Current vs. Supply Voltage



Closed Loop Frequency Response



Common Mode Rejection Ratio vs. Frequency



*Total Input Noise Voltage vs. Frequency**
**Includes Contribution From Source Resistance*

ANALOG DEVICES

High Speed Buffer Amplifiers

ADLH0033G/ADLH0033CG

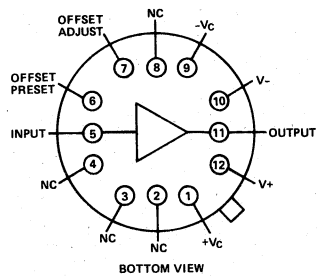
FEATURES

- 2nd Source–Replaces All LH0033G Series
- Wide Bandwidth–dc to 100MHz
- High Slew Rate–1500V/μs
- Operates on Single or Dual Power Supplies
- Operation Guaranteed -55°C to +125°C (ADLH0033G)
- High $10^{11}\ \Omega$ Input Impedance

APPLICATIONS

- High-Speed Line Drivers
- Video Impedance Transformation
- High-Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive

ADLH0033G/ADLH0033CG
PIN DESIGNATIONS



TO-8 PACKAGE

GENERAL DESCRIPTION

The ADLH0033G and ADLH0033CG are superhigh speed (1500V/μs slew rate) and high input impedance ($10^{11}\ \Omega$) buffer amplifiers, designed to replace all LH0033 series amplifiers in applications such as high-speed line drivers or as high impedance buffers for fast A/D converters and comparators.

The ADLH0033G and ADLH0033CG are rated for operation over the voltage range of ±5V to ±20V. The ADLH0033G is guaranteed over the temperature range of -55°C to +125°C, while the commercial grade ADLH0033CG is guaranteed over the range of -25°C to +85°C.

Guaranteed operation over temperature of the ADLH0033G is achieved by using specially selected junction FET's and the latest state-of-the-art laser trimming techniques. They are available in the industry standard 12 pin TO-8 metal can.

OPERATION WITHIN AN OP AMP LOOP

When using the ADLH0033G/ADLH0033CG as a current booster or isolation buffer with op amps such as LH0032, 118, 741, etc., an isolation resistor of at least 47Ω must be used between the op amp's output and the input of the ADLH0033G.

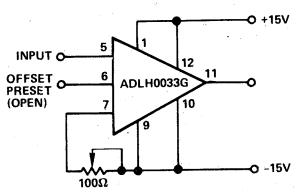


Figure 1. Offset Adjustment

HEAT SINKING

To assure maximum output drive capability of the ADLH0033G/ADLH0033CG over temperature, heat sinks should be used. The cases are electrically isolated from the circuit and thus may be connected to system grounds.

POWER SUPPLY BYPASSING

To prevent oscillation, power supply bypassing is recommended. Use low-inductance ceramic disc caps, keeping lead lengths as short as possible (1/4" to 1/2" max from device package), connected between ground plane and each supply lead. Use one or two 0.1μF caps in parallel with a 4.7μF tantalum for best results.

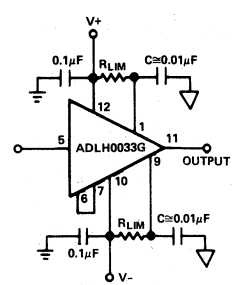


Figure 2. Short Circuit Protection Using Current Limiting Resistors (R_{LIM})

SPECIFICATIONS

	ADLH0033G	ADLH0033CG
ABSOLUTE MAXIMUM RATINGS		
Supply Voltage (V+ – V–)	40V	
Maximum Power Dissipation (see curves)	1.5W	
Maximum Junction Temperature	175°C	
Input Voltage	Equal to Supplies	
Continuous Output Current	±100mA	
Peak Output Current	±250mA	
Operating Temperature ADLH0033G	–55°C to +125°C	
ADLH0033CG	–25°C to +85°C	
Storage Temperature Range	–65°C to +150°C	
Lead Temperature (Soldering, 10 sec.)	300°C	

		ADLH0033G			ADLH0033CG			
Parameter	**Conditions**	**min**	**typ**	**max**	**min**	**typ**	**max**	**Units**
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	$T_C = 25°C$		0.1	0.15		0.15		nA
				10			5	nA
Input Impedance	$R_L = 1k\Omega$	10^{10}	10^{11}		10^{10}	10^{11}		Ω
Voltage Gain	V_{IN} = 1V rms, f = 1kHz, $R_L = 1k\Omega$, $R_S = 100k\Omega$	0.96	0.98	1.0	0.96	0.98	1.0	V/V
Output Offset Voltage	$R_S = 100k\Omega$, $T_C = 25°C$		5	10		12	20	mV
	$R_S = 100k\Omega$			15			25	mV
Output Offset Voltage TC	$R_S = 100k\Omega$		50	100		50	100	µV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz		6	10		6	10	Ω
	$R_S = 100k\Omega$, $R_L = 1k\Omega$							
Output Voltage Swing	$R_L = 1k\Omega$	±12	±13		±12	±13		V
	$R_L = 100\Omega$, $T_C = 25°C$	±9			±9			V
	$V_S = ±5V$, $R_L = 1k\Omega$		6			6		V p-p
Supply Current	$V_{IN} = 0V$, $V_S = ±15V$		20	25		21	25	mA
	$V_S = ±5V$		18			18		mA
Power Consumption	$V_{IN} = 0V$, $V_S = ±15V$		600	660		630	720	mW
	$V_S = ±5V$		180			180		mW
AC ELECTRICAL CHARACTERISTICS ($T_C = 25°C$, $V_S = ±15V$, $R_S = 50\Omega$, $R_L = 1k\Omega$)								
Slew Rate	$V_{IN} = ±10V$	1000	1500		1000	1400		V/µs
Bandwidth	V_{IN} = 1V rms		100			100		MHz
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Rise Time	$\Delta V_{IN} = 0.5V$		2.9			3.2		ns
Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2			1.5		ns
Harmonic Distortion	f>1kHz		<0.1			<0.1		%
MTBF								
Meantime Between Failure	1.962×10^7 hours							
PACKAGE OPTION[3]			H12A			H12A		

NOTES

[1] Unless otherwise specified, these specifications apply for +15V applied to pins 1 and 12, –15V applied to pins 9 and 10, and pin 6 connected to pin 7.

[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the ADLH0033G, and $-25°C \leq T_C \leq +85°C$ for the ADLH0033CG. Typical values shown are for $T_C = 25°C$.

[3] See Section 19 for package outline information.

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range
ADLH0033CG	–25°C to +85°C
ADLH0033G	–55°C to +125°C

LAYOUT CONSIDERATIONS

As is the case with any high-speed design, proper layout is critical to avoid the introduction of unnecessary errors due to high-frequency coupling, stray capacitance, and the like.

Large ground planes should be used whenever possible to provide a low resistance, low inductance circuit path, as well as shielding the effects of high-frequency coupling. Sockets should be avoided, as the increased inter-lead capacitance can degrade bandwidth. Input and output connections should be kept as short as practical.

OFFSET ADJUSTMENT

The ADLH0033G/ADLH0033CG are factory trimmed for output voltage offsets well within the guaranteed limits, thereby eliminating the need to calibrate each device individually. To use this feature, simply connect Pin 6 (OFFSET PRESET) to Pin 7 (OFFSET ADJUST).

When it is desirable to eliminate any errors due to output offsets, the circuit of Figure 1 may be used to adjust these errors to zero.

SHORT CIRCUIT PROTECTION

The circuit of Figure 2 is used to protect the ADLH0033G/ADLH0033CG from short circuits on the output. The value of R_{LIM} is determined by the following:

$$R_{LIM} \cong \frac{V+}{I_{sc}} = \frac{V-}{I_{sc}}$$

Where I_{sc} = Output Current under short circuit conditions $\leqslant$100mA.

Note that output voltage swing will also be somewhat limited in this configuration; however, decoupling of Pins 1 and 9 through disc type capacitors to ground as shown in Figure 2 will restore full output swing for transient pulses.

OPERATION WITH ASYMMETRICAL SUPPLIES

Since Symmetrical Power Supplies may not always be desirable or available, the ADLH0033G/ADLH0033CG is designed to operate on Asymmetrical Supplies. This causes an apparent output offset; however, this is because of the amplifier's gain of less than unity. To accurately predict the output voltage shift due to Asymmetrical Supplies, use the following formula:

$$A_{VO} \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\ (V+ - V-)$$

Where A_V = No Load Voltage Gain, typically 0.99
V+ = Positive Supply Voltage
V– = Negative Supply Voltage

Of course, these apparent offsets may be adjusted to zero by using the circuit shown in Figure 1, OFFSET ADJUSTMENT.

CAPACITIVE LOADING

The ADLH0033G/ADLH0033CG have been designed to drive capacitive loads of several thousand picofarads (such as coaxial cable) without oscillation. In these applications, peak current resulting from (C X dv/dt) should be limited below the absolute maximum peak current rating of ±250mA.

Also, power dissipation due to driving capacitive loads plus standby power should be kept below the total power rating of 1.5W.

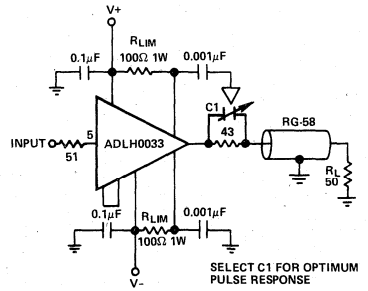


Figure 5. Coaxial Cable Drive

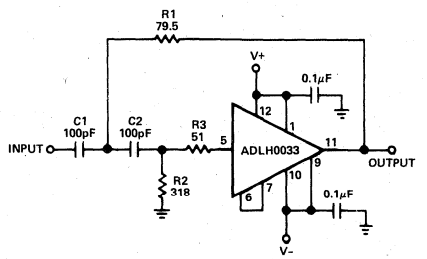


Figure 6. Wideband Two Pole High Pass Filter

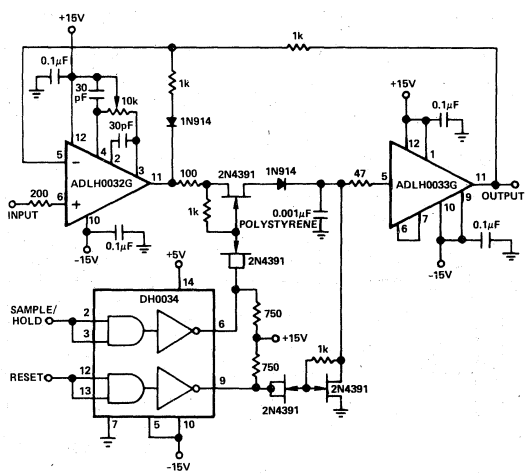


Figure 7. High Speed Peak Detector

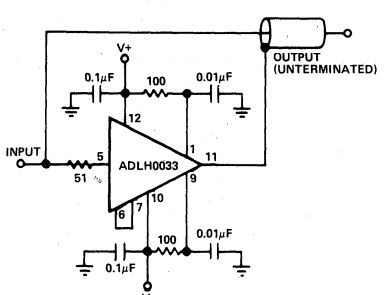
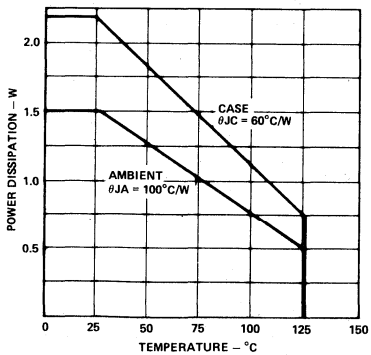
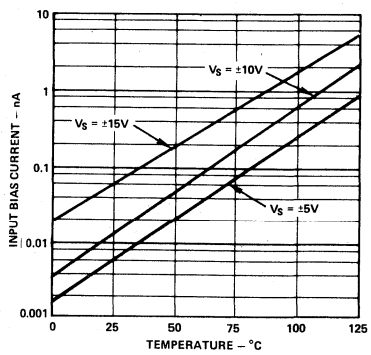


Figure 8. High Speed Shield/Line Driver

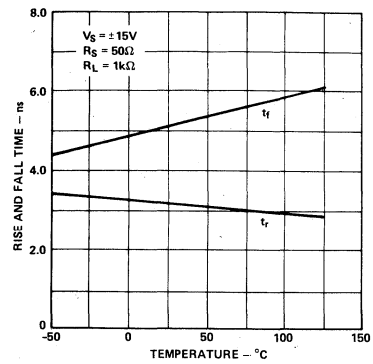
Typical Performance Curves



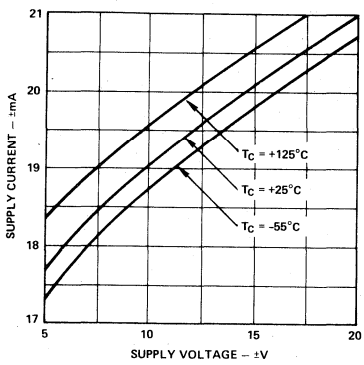
Power Dissipation vs Temperature



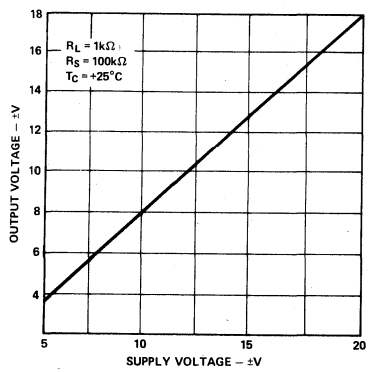
Input Bias Current vs Temperature



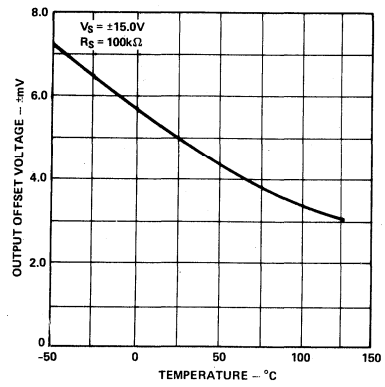
Rise and Fall Time vs Temperature



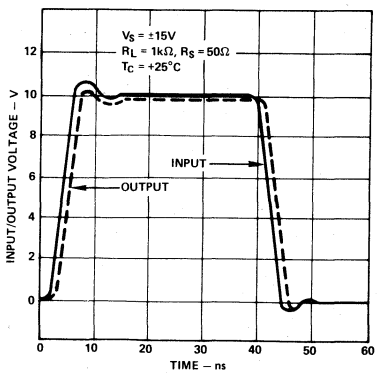
Supply Current vs Supply Voltage



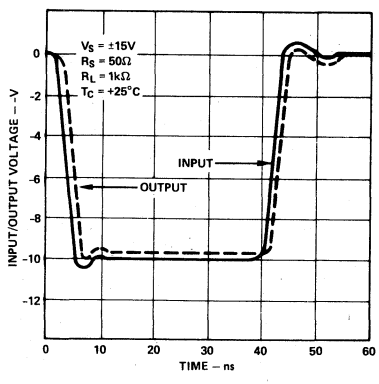
Output Voltage vs Supply Voltage



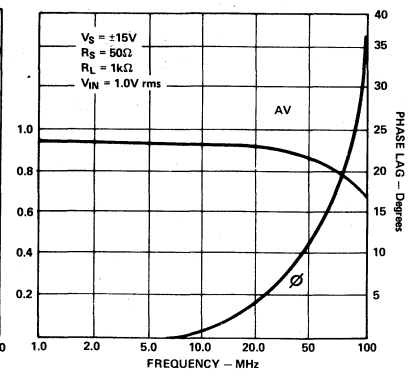
Output Offset Voltage vs Temperature



Positive Pulse Response



Negative Pulse Response



Frequency Response

ANALOG DEVICES

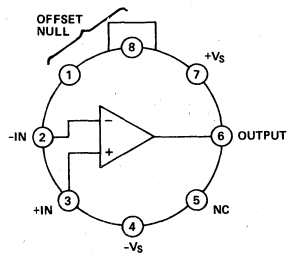
Ultra-Low Offset Voltage Op Amp

AD OP-07

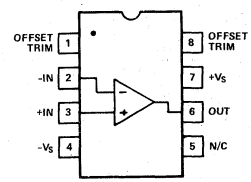
FEATURES

Ten Times More Gain Than Other OP-07 Devices (3.0M min)
Ultra-Low Offset Voltage: 10μV
Ultra-Low Offset Voltage Drift: 0.2μV/°C
Ultra-Stable vs. Time: 0.2μV/month
Ultra-Low Noise: 0.35μV p-p
No External Components Required
Monolithic Construction
High Common Mode Input Range: ±14.0V
Wide Power Supply Voltage Range: ±3V to ±18V
Fits 725, 108A/308A Sockets

AD OP-07 FUNCTIONAL BLOCK DIAGRAM



H-PACKAGE



N-PACKAGE

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed loop gain applications. Input offset voltages as low as 10μV, bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.2μV/°C and long-term stability of 0.2μV/month eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common mode input voltage range (±14V) high common mode rejection ratio (up to 126dB) and high differential input impedance (50MΩ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for -55°C to +125°C operation. The devices are packaged in either TO-99 hermetically-sealed metal cans or plastic 8-pin mini DIPS.

PRODUCT HIGHLIGHTS

1. Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
2. Ultra-low offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
3. Internal frequency compensation, ultra-low input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
5. Monolithic construction along with advanced circuit design and processing techniques result in low cost.
6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS (T_A = +25°C, V_S = ±15V, unless otherwise specified)

MODEL		AD OP-07E			AD OP-07C			AD OP-07D		
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
OPEN LOOP GAIN	A_{VO}	2,000	5,000		1,200	4,000		1,200	4,000	
		1,800	4,500		1,000	4,000		1,000	4,000	
		300	1,000		300	1,000		300	1,000	
OUTPUT CHARACTERISTICS										
Maximum Output Swing	V_{OM}	±12.5	±13.0		±12.0	±13.0		±12.0	±13.0	
		±12.0	±12.8		±11.5	±12.8		±11.5	±12.8	
		±10.5	±12.0			±12.0				
		±12.0	±12.6		±11.0	±12.6		±11.0	±12.6	
Open-Loop Output Resistance	R_O		60			60			60	
FREQUENCY RESPONSE										
Closed Loop Bandwidth	BW		0.6			0.6			0.6	
Slew Rate	SR		0.17			0.17			0.17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	75		60	150		60	150
			45	130		85	250		85	250
Adjustment Range			±4			±4			±4	
Average Drift							(Note 2)			(Note 2)
No External Trim	TCV_{OS}		0.3	1.3		0.5	1.8		0.7	2.5
With External Trim	TCV_{OSN}		0.3	1.3		0.4	1.6		0.7	2.5
							(Note 2)			(Note 2)
Long Term Stability	V_{OS}/Time		0.3	1.5		0.4	2.0		0.5	3.0
INPUT OFFSET CURRENT										
Initial	I_{OS}		0.5	3.8		0.8	6.0		0.8	6.0
			0.9	5.3		1.6	8.0		1.6	8.0
Average Drift	TCI_{OS}		8 (Note 2)	35		12 (Note 2)	50		12 (Note 2)	50
INPUT BIAS CURRENT										
Initial	I_B		±1.2	±4.0		±1.8	±7.0		±2.0	±12
			±1.5	±5.5		±2.2	±9.0		±3.0	±14
Average Drift	TCI_B		13 (Note 2)	35		18 (Note 2)	50		18 (Note 2)	50
INPUT RESISTANCE										
Differential	R_{IN}	15	50		8	33		7	31	
Common Mode	R_{IN} CM		160			120			120	
INPUT NOISE										
Voltage	e_n p-p		0.35	0.6		0.38	0.65		0.38	0.65
Voltage Density	e_n		10.3	18.0		10.5	20.0		10.5	20.0
			10.0	13.0		10.2	13.5		10.2	13.5
			9.6	11.0		9.8	11.5		9.8	11.5
Current	i_n p-p		14	30		15	35		15	35
Current Density	i_n		0.32	0.80		0.35	0.90		0.35	0.90
			0.14	0.23		0.15	0.27		0.15	0.27
			0.12	0.17		0.13	0.18		0.13	0.18
INPUT VOLTAGE RANGE										
Common Mode	CMVR	±13.0	±14.0		±13.0	±14.0		±13.0	±14.0	
		±13.0	±13.5		±13.0	±13.5		±13.0	±13.5	
Common Mode Rejection Ratio	CMRR	106	123		100	120		94	110	
		103	123		97	120		94	106	
POWER SUPPLY										
Current, Quiescent	I_Q		3.0	4.0		3.5	5.0		3.5	5.0
Power Consumption	P_D		90	120		105	150		105	150
			6.0	8.4		6.0	8.4		6.0	8.4
Rejection Ratio	PSRR	94	107		90	104		90	104	
		90	104		86	100		86	100	
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}	0		+70	0		+70	0		+70
PACKAGE OPTION[4]										
"N" Package										
8-Pin MINI DIP – (N8A)			AD OP-07EN			AD OP-07CN			AD OP-07DN	
"H" Package										
TO-99 – (H08B)			AD OP-07EH			AD OP-07CH			AD OP-07DH	

NOTES

[1] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, AD OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

[2] Parameter is not 100% tested; 90% of units meet this specification.

[3] Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the intitial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5μV – Parameter is not 100% tested: 90% of units meet this specification.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

AD OP-07AH			AD OP-07H				
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**	**UNITS**
3,000	5,000		**2,000**	5,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	V/mV
2,000	4,000		**1,500**	4,000		$R_L \geq 2k\Omega$, $V_O = \pm 10V$, T_{min} to T_{max}	V/mV
300	1,000		**300**	1,000		$R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S = \pm 3V$	V/mV
±12.5	±13.0		**±12.5**	±13.0		$R_L \geq 10k\Omega$	V
±12.0	±12.8		**±12.0**	±12.8		$R_L \geq 2k\Omega$	V
±10.5	±12.0		**±10.5**	±12.0		$R_L \geq 1k\Omega$	V
±12.0	±12.6		**±12.0**	±12.6		$R_L \geq 2k\Omega$, T_{min} to T_{max}	V
	60			60		$V_O = 0$, $I_O = 0$	Ω
	0.6			0.6		$A_{VCL} = +1.0$	MHz
	0.17			0.17		$R_L \geq 2k$	V/μs
	10	**25**		30	**75**	Note 1	μV
	25	**60**		60	**200**	Note 1, T_{min} to T_{max}	μV
	±4			±4		$R_P = 20k\Omega$	mV
	0.2	**0.6**		0.3	**1.3**	T_{min} to T_{max}	μV/°C
	0.2	0.6		0.3	1.3	$R_P = 20k\Omega$, T_{min} to T_{max}	μV/°C
	0.2	1.0		0.2	1.0	Note 3	μV/Month
	0.3	**2.0**		0.4	**2.8**		nA
	0.8	**4.0**		1.2	**5.6**	T_{min} to T_{max}	nA
	5	25		8	50	T_{min} to T_{max}	pA/°C
	±0.7	**±2.0**		±1.0	**±3.0**		nA
	±1.0	**±4.0**		±2.0	**±6.0**	T_{min} to T_{max}	nA
	8	25		13	50	T_{min} to T_{max}	pA/°C
30	80		20	60			MΩ
	200			200			GΩ
	0.35	0.6		0.35	0.6	0.1Hz to 10Hz, Note 2	μV p-p
	10.3	18.0		10.3	18.0	f_O = 10Hz, Note 2	$nV/\sqrt{Hz}$
	10.0	13.0		10.0	13.0	f_O = 100Hz, Note 2	$nV/\sqrt{Hz}$
	9.6	11.0		9.6	11.0	f_O = 1kHz, Note 2	$nV/\sqrt{Hz}$
	14	30		14	30	0.1Hz to 10Hz, Note 2	pA p-p
	0.32	0.80		0.32	0.80	f_O = 10Hz, Note 2	$pA/\sqrt{Hz}$
	0.14	0.23		0.14	0.23	f_O = 100Hz, Note 2	$pA/\sqrt{Hz}$
	0.12	0.17		0.12	0.17	f_O = 1kHz, Note 2	$pA/\sqrt{Hz}$
±13.0	±14.0		**±13.0**	±14.0			V
±13.0	±13.5		**±13.0**	±13.5		T_{min} to T_{max}	V
110	126		**110**	126		V_{CM} = ±CMVR	dB
106	123		**106**	123		V_{CM} = ±CMVR, T_{min} to T_{max}	dB
	3.0	**4.0**		3.0	**4.0**	V_S = ±15V	mA
	90	120		90	120	V_S = ±15V	mW
	6.0	8.4		6.0	8.4	V_S = ±3V	mW
100	110		**100**	110		V_S = ±3V to ±18V	dB
94	106		**94**	106		V_S = ±3V to ±18V, T_{min} to T_{max}	dB
-55		+125	**-55**		+125		°C
	—			—			
	AD OP-07AH			AD OP-07H			

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

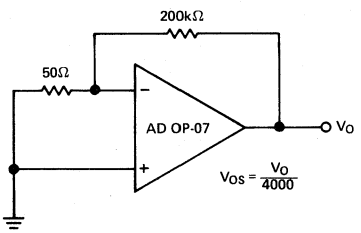
ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . . ±30V
Input Voltage (Note 2) . . . . . ±22V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range
OP-07A, OP-07 . . . . . -55°C to +125°C
OP-07E, OP-07C, OP-07D . . . . . 0 to +70°C
Lead Temperature Range (Soldering, 60sec) . . . . . 300°C

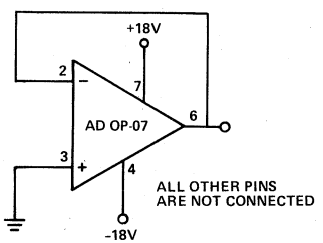
NOTES:
Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.



Offset Voltage Test Circuit



Burn-In Circuit

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be removed (or referenced to $+V_S$). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

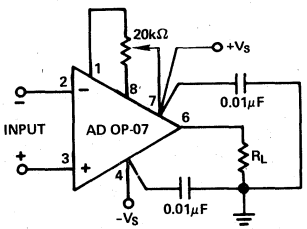


Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

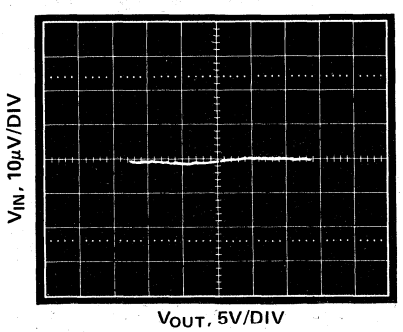
The AD OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with 50Ω resistor.

Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

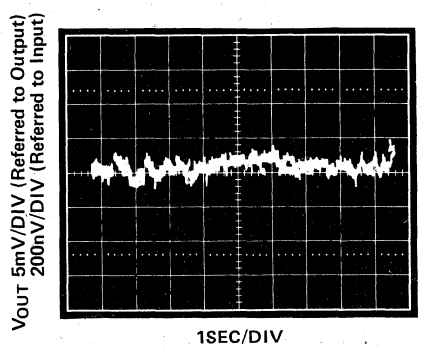
Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality 0.01μF ceramic capacitor as shown in Figure 1.

4

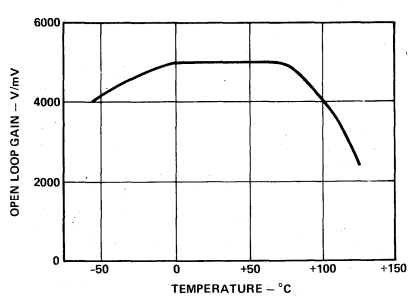
Performance Curves (typical @ T_A = +25°C, V_S = ±15V, AD OP-07 Grade Device unless otherwise noted)



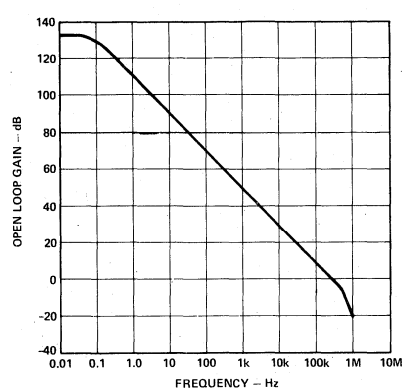
AD OP-07 Open Loop Gain Curve



AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

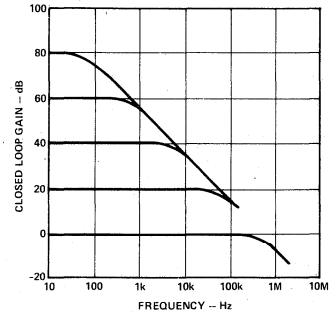


Open Loop Gain vs. Temperature

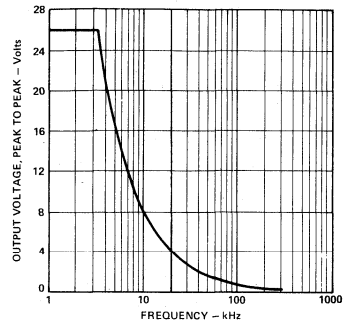


Open Loop Frequency Response

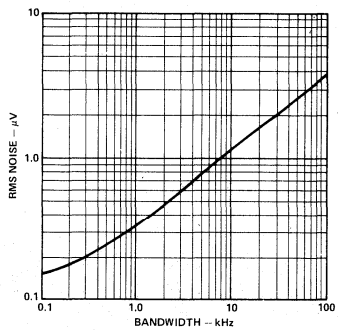
Typical Performance Curves



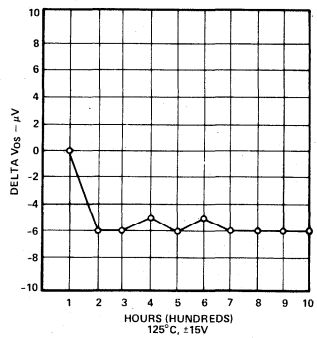
Closed Loop Response for Various Gain Configurations



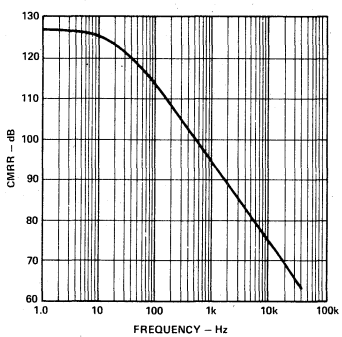
Maximum Undistorted Output vs. Frequency



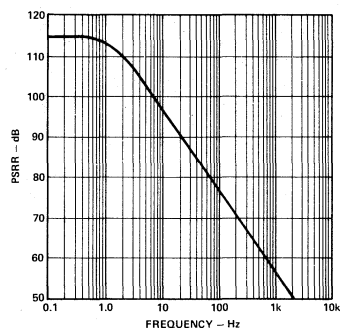
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



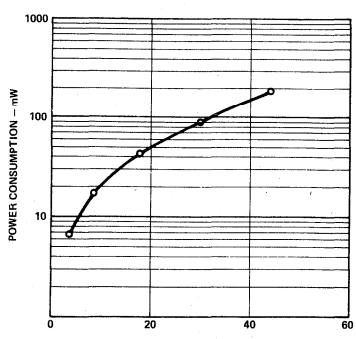
Offset Voltage vs. Time



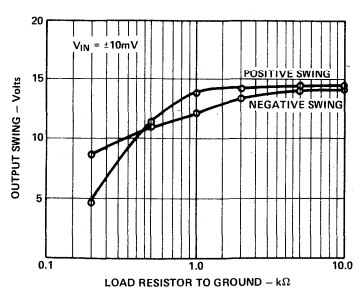
CMRR vs. Frequency



PSRR vs. Frequency



Power Consumption vs. Power Supply



Output Voltage vs. Load Resistance

ANALOG DEVICES

Ultra-Low Noise Precision Op Amp

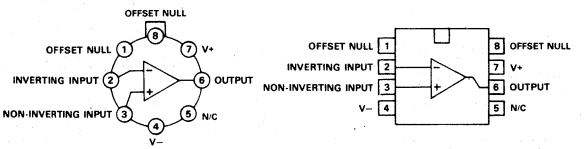
AD OP-27

4

FEATURES

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
High Slew Rate: 2.8V/μs
High Gain Bandwidth Product: 8MHz
Low Offset Voltage: 10μV
High CMRR: 126dB over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, 725, 714 and 741 Sockets

AD OP-27 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

8-PIN MINI DIP
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs slew rate and an 8MHz gain bandwidth product are possible without sacrificing dc accuracy. Long term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-27 is available in six performance grades. The AD OP-27E, AD OP-27F and AD OP-27G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-27A, AD OP-27B and AD OP-27C are specified for −55°C to +125°C operation. All devices are available in TO-99 hermetically sealed metal cans, while the E, F and G grades are also packaged in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. Precision amplification of very low level, low frequency voltage inputs is enhanced by ultra-low input voltage noise.
2. The AD OP-27 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-27G			AD OP-27F			AD OP-27E		
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		–	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		**750**	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		**±11.7**	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	5.0	8.0		5.0	8.0		5.0	8.0	
Slew Rate	SR	1.7	2.8		1.7	2.8		1.7	2.8	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**50**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	**±60**
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	**50**
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		**±10.5**	±11.8	
Common-Mode Rejection										
Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		**110**	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	5.6		3.0	4.6		3.0	4.6
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	**15**
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
T_{MIN}, T_{MAX}		–25		+85	–25		+85	–25		+85

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

[3]Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

Specifications subject to change without notice.

AD OP-27C			AD OP-27B			AD OP-27A			CONDITIONS	UNITS
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
–	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
5.0	8.0		5.0	8.0		5.0	8.0			MHz
1.7	2.8		1.7	2.8		1.7	2.8		$R_L \geq 2k\Omega$	V/μs
	30	**100**		20	**60**		10	**25**	(Note 1)	μV
	70	**300**		50	**200**		30	**60**	T_a = min to max	μV
	0.4	**1.8**		0.3	**1.3**		0.2	**0.6**	T_a = min to max (Note 2)	μV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 3)	μV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	μV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	f_o = 10Hz	nV/√Hz
	3.3	5.6		3.1	4.5		3.1	4.5	f_o = 30Hz	nV/√Hz
	3.2	4.5		3.0	3.8		3.0	3.8	f_o = 1000Hz	nV/√Hz
	1.7	–		1.7	4.0		1.7	4.0	f_o = 10Hz	pA/√Hz
	1.0	–		1.0	2.3		1.0	2.3	f_o = 30Hz	pA/√Hz
	0.4	0.6		0.4	0.6		0.4	0.6	f_o = 1000Hz	pA/√Hz
±11.0	±12.3		**±11.0**	±12.3		**±11.0**	±12.3			V
±10.2	±11.5		**±10.3**	±11.5		**±10.3**	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	5.6		3.0	4.6		3.0	4.6	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	μV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	μV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 3) . . . . . ±0.7V
Differential Input Current (Note 3) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-27A, AD OP-27B, AD OP-27C . −55°C to +125°C
AD OP-27E, AD OP-27F, AD OP-27G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
MINI-DIP (N)	36°C	5.6mW/°C

Note 2: For supply voltages less than ± 18V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

AD OP-27 ORDERING GUIDE

Model	Package Option[1]	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)
AD OP-27-GH	TO-99	−25 to +85	100	1.8
AD OP-27-GN	MINI-DIP (N8A)	−25 to +85	100	1.8
AD OP-27-FH	TO-99	−25 to +85	60	1.3
AD OP-27-FN	MINI-DIP (N8A)	−25 to +85	60	1.3
AD OP-27-EH	TO-99	−25 to +85	25	0.6
AD OP-27-EN	MINI-DIP (N8A)	−25 to +85	25	0.6
AD OP-27-CH	TO-99	−55 to +125	100	1.8
AD OP-27-BH	TO-99	−55 to +125	60	1.3
AD OP-27-AH	TO-99	−55 to +125	25	0.6

NOTE

[1]See Section 19 for package outline information.

APPLICATION NOTES FOR THE AD OP-27

The AD OP-27 can be used in the sockets of many of the popular precision bipolar input operational amplifiers on the market. Elimination of external frequency compensation or nulling circuitry may be possible in many cases. In 741 replacement situations, if nulling has been implemented, it should be modified or removed for optimum AD OP-27 performance.

In applications where the initial factory adjusted input offset voltage provides insufficient accuracy, further offset trimming can be accomplished with the resistor network shown in Figure 1. The adjustment range attainable using a 10kΩ potentiometer will be ±4mV. If a smaller adjustment range is required, the sensitivity of the nulling can be increased by using a smaller potentiometer in series with fixed resistor(s). For example, a 1kΩ pot in series with two 4.7kΩ resistors will yield a ±280μV range.

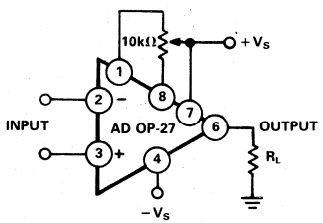


Figure 1. Optional Offset Nulling Circuit

Zeroing the initial offset with potentiometers other than 10kΩ, but between 1kΩ and 1MΩ, will introduce an additional input offset voltage temperature drift error of from 0.1 to 0.2μV/°C. Additionally, by intentionally trimming in a dc level shift a voltage dependent offset drift will be created. It will be approximately the input offset voltage at 25°C divided by 300 (in μV/°C).

Parasitic thermocouple EMF's can be generated where dissimilar metals meet the contacts to the input terminals of the AD OP-27. These temperature dependent voltages can manifest themselves as drift type errors. Optimized temperature performance will be obtained when both contacts are maintained at the same temperature—a temperature close to the device's package.

Output stability with the AD OP-27 is possible with capacitive loads of up to 2000pF and ±10V output swings. Larger capacitances should be decoupled with a 50Ω resistor.

High closed loop gain and excellent linearity can be achieved by operating the AD OP-27 within an output current range of ±10mA. Minimizing output current will provide the highest linearity.

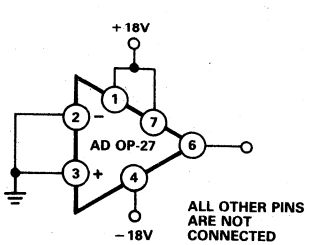


Figure 2. Burn-In Circuit

SLEW RATE DISCUSSION

In unity gain buffer applications with feedback resistances of less than 100Ω where the input is driven with a fast, large (greater than 1V) pulse, the output waveform will appear as in Figure 3.

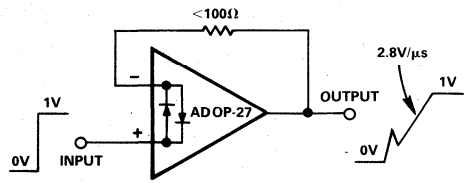


Figure 3. Unity Gain Buffer/Pulsed Operation

During the initial portion of the output slew the input protection back-to-back diodes effectively short the output to the input. A current limited only by the output short circuit protection will be drawn from the source. After the input diodes saturate, the amplifier will slew at its nominal 2.8V/μs. With feedback resistances of more than 500Ω the output is capable of handling the current requirements without limiting (less than 20mA at 10V) and the amplifier will stay in the linear region.

As with all operational amplifiers a feedback resistance of greater than 2kΩ will create a pole with the input capacitance (8pF). Additional phase shift will be introduced and the phase margin will be reduced. A small capacitor (20 to 50pF) in parallel with the feedback resistor will alleviate this problem.

CAUTION: NOISE MEASUREMENTS

Precise measurement of the extremely low input noise associated with the AD OP-27 is a difficult task. In order to observe the rated noise in the 0.1Hz to 10Hz frequency range the following cautions should be exercised.

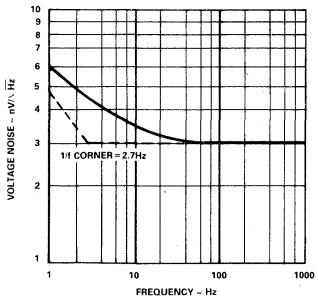
(1) The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds. As shown in the noise test frequency response plot in this data sheet the 0.1Hz corner is only defined by a single zero. A test time of 10 seconds acts as an additional zero to eliminate noise contributions from frequencies lower than 0.1Hz.

(2) Warm-up for a least five minutes will eliminate temperature induced effects. During the first few minutes the offset voltage typically increases 4μV. In a 10 second measurement interval prior to temperature stabilization the reading could include several nanovolts of warm-up offset error in addition to the noise.

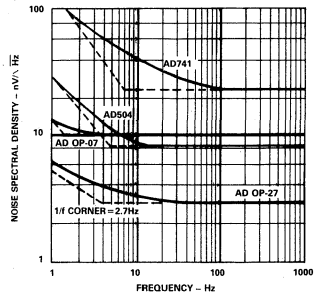
(3) For reasons similar to (2) the device under test should be well shielded from air currents or other heat sinks to eliminate the possibility of temperature changes over time invalidating the measurements. Sudden motion in the vicinity or physical contact with the package can also increase the observed noise.

An input voltage noise spectral density test is recommended when measuring noise on a large number of units. Because the 1/f noise corner frequency is around 3Hz, a 1kHz noise voltage density measurement combined with a 0.1Hz to 10Hz peak-to-peak noise reading will guarantee 1/f and white noise performance over the rated frequency spectrum.

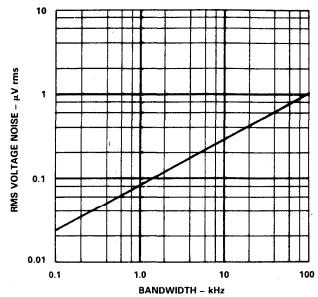
Typical Performance Curves (@ $T_A = +25°C$, $V_S = \pm 15V$)



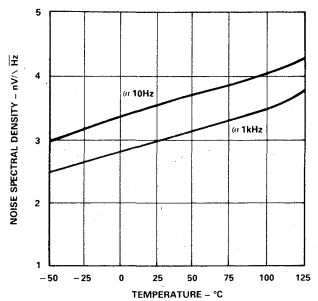
Input Voltage Noise Spectral Density



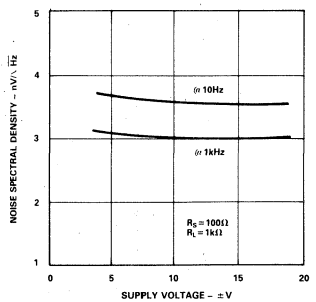
Comparison of Op Amp Input Voltage Noise Spectrums



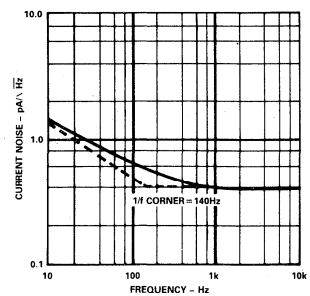
Input Wideband Noise vs. Bandwidth (0.1Hz to Frequency Indicated)



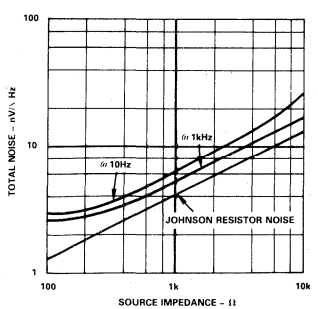
Input Voltage Noise vs. Temperature



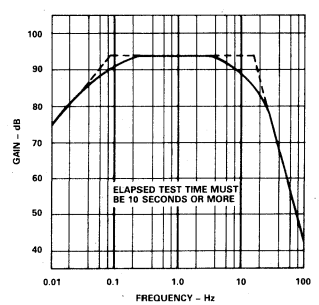
Input Voltage Noise vs. Supply Voltage



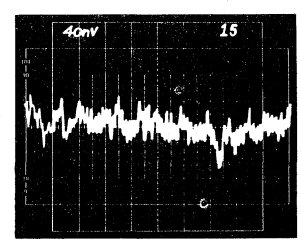
Input Current Noise Spectral Density



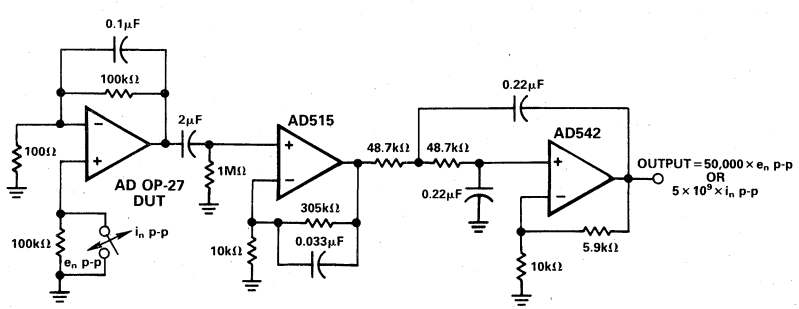
Total Noise vs. Source Impedance



0.1Hz to 10Hz Noise Test Frequency Response

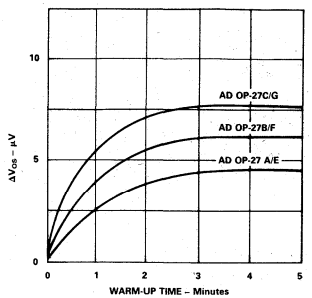


0.1Hz to 10Hz p-p Voltage Noise

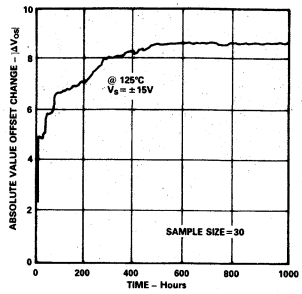


NOTE: ALL CAPACITORS MUST BE NONPOLARIZED

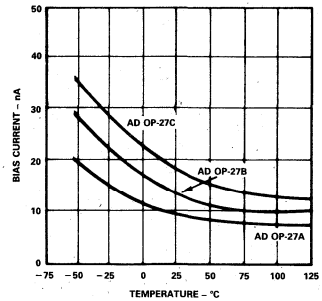
0.1Hz to 10Hz Noise Test Bandpass Filter (Voltage Gain = 50,000)



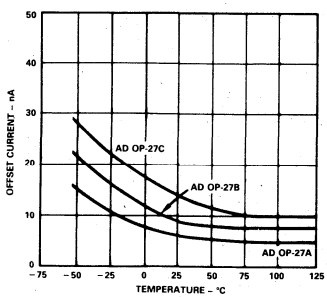
Input Offset Voltage Turn-On Drift vs. Time



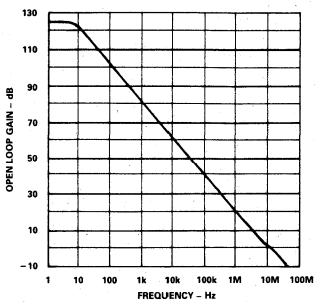
Long Term Offset Stability @ Temperature



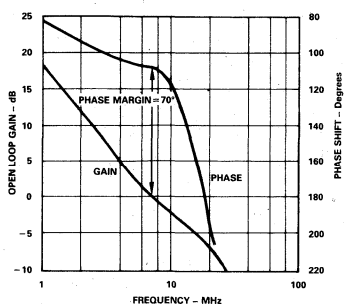
Input Bias Current vs. Temperature



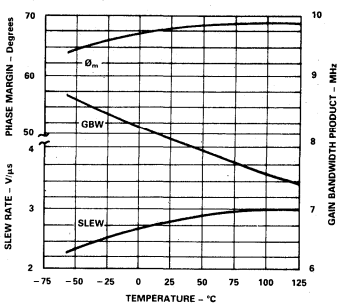
Input Offset Current vs. Temperature



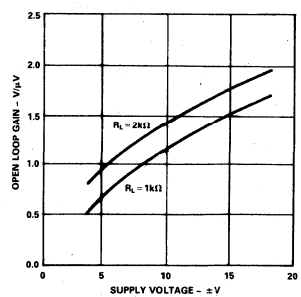
Open Loop Frequency Response



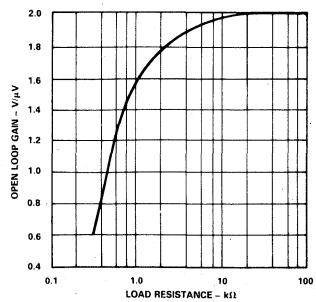
Open Loop Gain and Phase Shift vs. Frequency



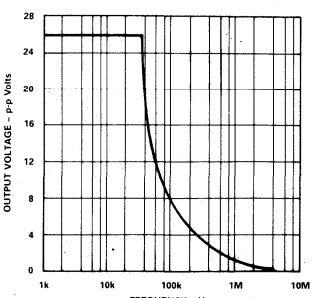
Slew Rate, Gain Bandwidth Product and Phase Margin vs. Temperature



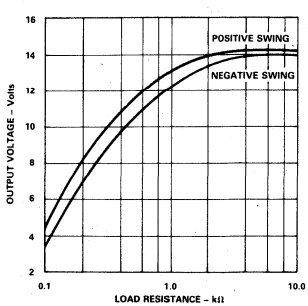
Open Loop Gain vs. Supply Voltage



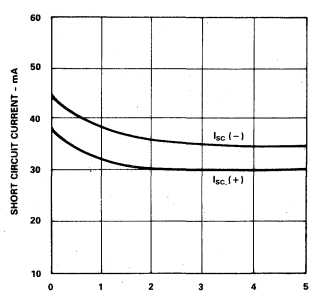
Open Loop Gain vs. Resistive Load



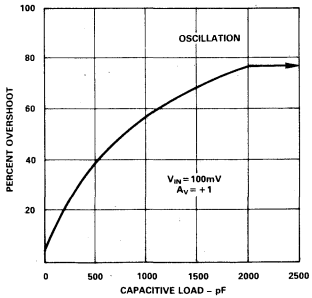
Undistorted Output Swing vs. Frequency



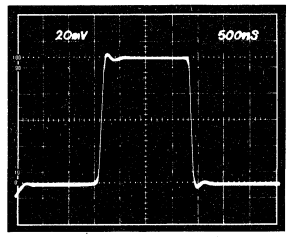
Output Swing vs. Resistive Load



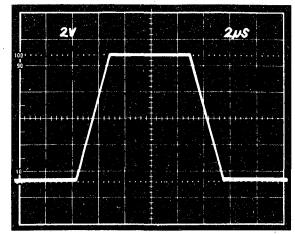
Output Short Circuit Current vs. Time



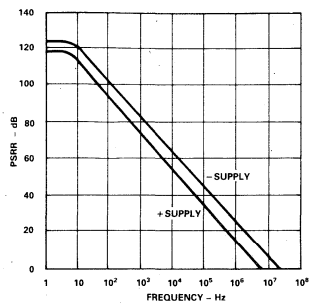
Small Signal Overshoot vs. Capacitive Load



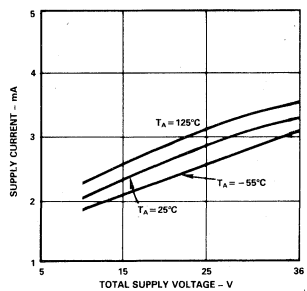
Unity Gain Follower Pulse Response (Small Signal)



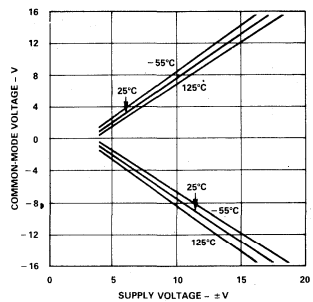
Unity Gain Follower Pulse Response (Large Signal)



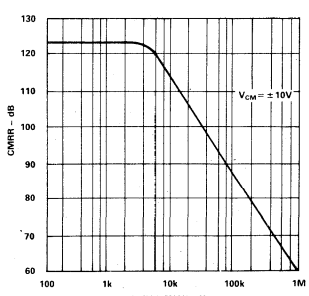
Power Supply Rejection Ratio vs. Frequency



Supply Current vs. Supply Voltage



Common-Mode Input Range vs. Supply Voltage



CMRR vs. Frequency

ANALOG DEVICES

Ultra-Low Noise, High Speed Precision Op Amp

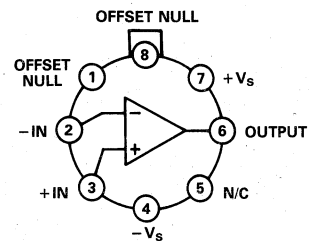
AD OP-37

4

FEATURES

Ultra-Low Noise: 80nV p-p (0.1Hz to 10Hz), 3nV/$\sqrt{Hz}$ at 1kHz
High Speed: 17V/μs
High Gain Bandwidth Product: 63MHz
Ultra-Low Offset Voltage Drift: 0.2μV/°C
High Offset Stability Over Time: 0.2μV/month
Low Offset Voltage: 10μV
High CMRR: 126dB Over ±11V Input Voltage Range
Fits OP-07, OP-05, OP-06, 5534, LH0044, 5130, 3510, 725, 714 and 741 Sockets in Gains > 5

AD OP-37 FUNCTIONAL BLOCK DIAGRAM



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. High speed accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than five. This instrumenation grade op amp features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of 3.0nV/$\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a 17V/μs slew rate and a 63MHz gain bandwidth product. Long term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

The AD OP-37 is available in six performance grades. The AD OP-37E, AD OP-37F and AD OP-37G are specified for operation over the −25°C to +85°C temperature range, while the AD OP-37A, AD OP-37B and AD OP-37C are specified for −55°C to +125°C operation. All devices are available in TO-99 hermetically sealed metal cans, while the industrial grades are also packaged in plastic mini-DIPs.

PRODUCT HIGHLIGHTS

1. High speed accurate amplification (gains > 5) of very low level low frequency voltage inputs is enhanced by a high gain bandwidth product and ultra-low input voltage noise.
2. The AD OP-37 maintains high dc accuracy over an extended temperature range due to ultra-low offset voltage, offset voltage drift and input bias current.
3. Internal frequency compensation, factory adjusted offset voltage and full device protection eliminate the need for additional components. Circuit size and complexity are reduced while reliability is increased.
4. Long-term stability and accuracy is assured with low offset voltage drift over time.
5. Input referred errors are greatly reduced by superior common-mode and power supply rejection characteristics.
6. Monolithic construction along with advanced circuit design and processing techniques result in low cost.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-37G			AD OP-37F			AD OP-37E		
PARAMETER	**SYMBOL**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**
OPEN LOOP GAIN	A_{VO}	**700**	1,500		**1,000**	1,800		**1,000**	1,800	
		400	1,500		**800**	1,500		**800**	1,500	
		200	500		250	700		250	700	
		450	1,000		700	1,300		**750**	1,500	
OUTPUT CHARACTERISTICS										
Voltage Swing	V_O	**±11.5**	±13.5		**±12.0**	±13.8		**±12.0**	±13.8	
		±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5	
		±11.0	±13.3		±11.4	±13.5		**±11.7**	±13.6	
Open-Loop Output Resistance	R_O		70			70			70	
FREQUENCY RESPONSE										
Gain Bandwidth Product	GBW	45	63		45	63		45	63	
		–	40		–	40		–	40	
Slew Rate	SR	11	17		11	17		11	17	
INPUT OFFSET VOLTAGE										
Initial	V_{OS}		30	**100**		20	**60**		10	**25**
			55	220		40	140		20	**50**
Average Drift	TCV_{OS}		0.4	1.8		0.3	1.3		0.2	**0.6**
Long Term Stability	V_{OS}/Time		0.4	2.0		0.3	1.5		0.2	1.0
Adjustment Range			±4.0			±4.0			±4.0	
INPUT BIAS CURRENT										
Initial	I_B		±15	**±80**		±12	**±55**		±10	**±40**
			±25	±150		±18	±95		±14	**±60**
INPUT OFFSET CURRENT										
Initial	I_{OS}		12	**75**		9	**50**		7	**35**
			20	135		14	85		10	**50**
INPUT NOISE										
Voltage	e_n p-p		0.09	0.25		0.08	0.18		0.08	0.18
Voltage Density	e_n		3.8	8.0		3.5	5.5		3.5	5.5
			3.3	5.6		3.1	4.5		3.1	4.5
			3.2	4.5		3.0	3.8		3.0	3.8
Current Density	i_n		1.7	–		1.7	4.0		1.7	4.0
			1.0	–		1.0	2.3		1.0	2.3
			0.4	0.6		0.4	0.6		0.4	0.6
INPUT VOLTAGE RANGE										
Common Mode	CMVR	**±11.0**	±12.3		**±11.0**	±12.3		**±11.0**	±12.3	
		±10.5	±11.8		±10.5	±11.8		**±10.5**	±11.8	
Common-Mode Rejection										
Ratio	CMRR	**100**	120		**106**	123		**114**	126	
		96	118		102	121		**110**	124	
INPUT RESISTANCE										
Differential	R_{IN}	0.8	4		1.2	5		1.5	6	
Common Mode	R_{INCM}		2			2.5			3	
POWER SUPPLY										
Rated Performance			±15			±15			±15	
Operating			±(4–18)			±(4–18)			±(4–18)	
Current, Quiescent	I_Q		3.3	5.6		3.0	4.6		3.0	4.6
Rejection	PSR		2	**20**		1	**10**		1	**10**
			2	32		2	16		2	**15**
Power Consumption	P_d		100	**170**		90	**140**		90	**140**
OPERATING TEMPERATURE RANGE										
T_{MIN}, T_{MAX}		−25		+85	−25		+85	−25		+85
PACKAGE[4]										
TO-99			AD OP-37GH			AD OP-37FH			AD OP-37EH	
MINI-DIP (N8A)			AD OP-37GN			AD OP-37FN			AD OP-37EN	

NOTES

[1]Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A and E grades are guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with $R_p = 8k\Omega$ to $20k\Omega$.

[3]Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. time after the first 30 days.

[4]See Section 19 for package outline information.

Specifications subject to change without notice.

AD OP-37C			AD OP-37B			AD OP-37A			CONDITIONS	UNITS
MIN	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**		
700	1,500		**1,000**	1,800		**1,000**	1,800		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	V/mV
–	1,500		**800**	1,500		**800**	1,500		$R_L \geq 1k\Omega$, $V_{OUT} = \pm 10V$	V/mV
200	500		250	700		250	700		$R_L = 600\Omega$, $V_{OUT} = \pm 1V$, $V_S = \pm 4V$	V/mV
300	800		**500**	1,000		**600**	1,200		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, T_a = min to max	V/mV
±11.5	±13.5		**±12.0**	±13.8		**±12.0**	±13.8		$R_L \geq 2k\Omega$	V
±10.0	±11.5		**±10.0**	±11.5		**±10.0**	±11.5		$R_L \geq 600\Omega$	V
±10.5	±13.0		**±11.0**	±13.2		**±11.5**	±13.5		$R_L \geq 2k\Omega$, T_a = min to max	V
	70			70			70		$I_{OUT} = 0A$, $V_{OUT} = 0V$	Ω
45	63		45	63		45	63		$f_o = 10kHz$	MHz
–	63		–	40		–	40		$f_o = 1MHz$	MHz
11	17		11	17		11	17		$R_L \geq 2k\Omega$	V/µs
	30	**100**		20	**60**		10	**25**	(Note 1)	µV
	70	**300**		50	**200**		30	**60**	T_a = min to max	µV
	0.4	**1.8**		0.3	**1.3**		0.2	**0.6**	T_a = min to max (Note 2)	µV/°C
	0.4	2.0		0.3	1.5		0.2	1.0	(Note 3)	µV/month
	±4.0			±4.0			±4.0		$R_p = 10k\Omega$	mV
	±15	**±80**		±12	**±55**		±10	**±40**		nA
	±35	**±150**		±28	**±95**		±20	**±60**	T_a = min to max	nA
	12	**75**		9	**50**		7	**35**		nA
	30	**135**		22	**85**		15	**50**	T_a = min to max	nA
	0.09	0.25		0.08	0.18		0.08	0.18	0.1Hz to 10Hz	µV p-p
	3.8	8.0		3.5	5.5		3.5	5.5	$f_o = 10Hz$	nV/√Hz
	3.3	5.6		3.1	4.5		3.1	4.5	$f_o = 30Hz$	nV/√Hz
	3.2	4.5		3.0	3.8		3.0	3.8	$f_o = 1000Hz$	nV/√Hz
	1.7	–		1.7	4.0		1.7	4.0	$f_o = 10Hz$	pA/√Hz
	1.0	–		1.0	2.3		1.0	2.3	$f_o = 30Hz$	pA/√Hz
	0.4	0.6		0.4	0.6		0.4	0.6	$f_o = 1000Hz$	pA/√Hz
±11.	±12.3		**±11.**	±12.3		**±11.**	±1			
±10.2	±11.5		**±10.3**	±11.5		**±10.3**	±11.5		T_a = min to max	V
100	120		**106**	123		**114**	126		$V_{CM} = \pm 11V$	dB
94	116		**100**	119		**108**	122		$V_{CM} = \pm 10V$, T_a = min to max	dB
0.8	4		1.2	5		1.5	6			MΩ
	2			2.5			3			GΩ
	±15			±15			±15			V
	±(4–18)			±(4–18)			±(4–18)			V
	3.3	5.6		3.0	4.6		3.0	4.6	$V_S = \pm 15V$	mA
	2	**20**		1	**10**		1	**10**	$V_S = \pm 4V$ to $\pm 18V$	µV/V
	4	**51**		2	**20**		2	**16**	$V_S = \pm 4.5V$ to $\pm 18V$, T_a = min to max	µV/V
	100	**170**		90	**140**		90	**140**	$V_{OUT} = 0V$	mW
−55		+125	−55		+125	−55		+125		°C
AD OP-37CH			AD OP-37BH			AD OP-37AH				
–			–			–				

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation (Note 1) 500mW
Input Voltage (Note 2) . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 3) . . . . . ±0.7V
Differential Input Current (Note 3) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range
AD OP-37A, AD OP-37B, AD OP-37C . −55°C to +125°C
AD OP-37E, AD OP-37F, AD OP-37G . −25°C to +85°C
Lead Temperature Range (Soldering 60sec) . . . . . 300°C

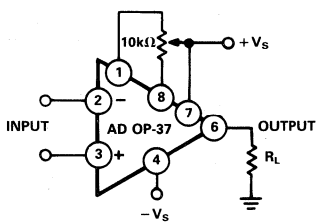
NOTES:

Note 1: Maximum package power dissipation vs. ambient temperature.

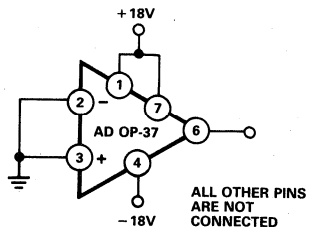
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature
TO-99 (H)	80°C	7.1mW/°C
MINI-DIP (N)	36°C	5.6mW/°C

Note 2: For supply voltages less than ± 18V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: The AD OP-37's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ± 0.7V, the input current should be limited to 25mA.



Optional Offset Nulling Circuit



Burn-In Circuit

AD OP-37 ORDERING GUIDE

Model	Package	Temperature Range (°C)	Max Initial Offset (µV)	Max Offset Drift (µV/°C)
AD OP-37-GH	TO-99	−25 to +85	100	1.8
AD OP-37-GN	MINI-DIP	−25 to +85	100	1.8
AD OP-37-FH	TO-99	−25 to +85	60	1.3
AD OP-37-FN	MINI-DIP	−25 to +85	60	1.3
AD OP-37-EH	TO-99	−25 to +85	25	0.6
AD OP-37-EN	MINI-DIP	−25 to +85	25	0.6
AD OP-37-CH	TO-99	−55 to +125	100	1.8
AD OP-37-BH	TO-99	−55 to +125	60	1.3
AD OP-37-AH	TO-99	−55 to +125	25	0.6

ANALOG DEVICES

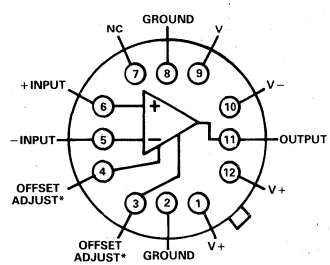
Fast Settling Video Operational Amplifier

HOS-050, 050A, 050C

FEATURES
80ns Settling to 0.1%; 200ns to 0.01%
100MHz Gain Bandwidth Product
55MHz 3dB Bandwidth
100mA Output @ ±10V

APPLICATIONS
D/A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

HOS-050/A/C PIN DESIGNATIONS



*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

TO-8
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-050, HOS-050A, and HOS-050C op amps are very high speed wideband operational amplifiers designed to complement the Analog Devices' lines of high speed data acquisition products. They feature a 100MHz gain bandwidth product; slew rate of 300V/μs; and settling time of 80ns to ±0.1%.

The HOS-050A, HOS-050, and HOS-050C have typical input offset voltages of 10mV, 25mV, and 45mV, respectively.

All models have a rated output of ±100mA minimum, and an exceptional noise spec of only 7μV rms, dc to 2MHz; they are ideally suited for a broad range of video applications.

FAST-SETTLING OP AMPS

At one time, operational amplifiers could be specified according to slew rates, bandwidth, and drive capability; and these parameters would be sufficient. Settling time was not considered until the use of high speed video D/A converters became widespread.

The conversion speed of the D/A can be limited by the settling time of the output amplifier, so it has become essential to select an op amp whose settling time is compatible with the D/A converter.

The increased emphasis on settling time has, in some cases, created a preoccupation with slew rates in the minds of some designers. But slew rate is only one component in establishing settling time.

The amount of overshoot, and the ringing which are present at the end of a step function change also have an effect. These parameters, in turn, are influenced by the bandwidth (or lack of it) when operating the op amp with closed loop gains greater than one.

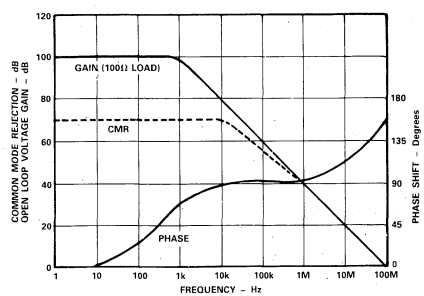


Figure 1. HOS-050 Frequency Response

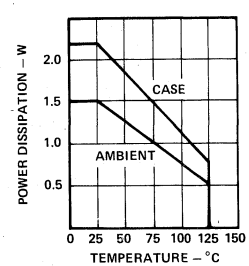


Figure 2. Power Dissipation vs. Temperature

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-050	HOS-050A	HOS-050C
ABSOLUTE MAXIMUM RATINGS			
Supply Voltages (V_S)	±18V	*	*
Power Dissipation	See Figure 2	*	*
Input Voltage	$\pm V_S$	*	*
Differential Input Voltage	$\pm V_S$	*	*
Operating Temperature Range (case)	−55°C to +125°C	*	−25°C to +85°C
Junction Temperature	175°C	*	*
Storage Temperature Range	−65°C to +150°C	*	*
Lead Temperature (soldering, 10 sec.)	300°C	*	*

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100			*			*		dB
Rated Output											
Current											
(not short circuit protected)	R_L = >100Ω		±100			*			*		mA
Voltage	R_L = >200Ω	±10			*			*			V
Input Offset Voltage	Adjustable to Zero										
Initial	@ +25°C		25	35		10	15		45	65	mV
vs. Temperature			50	150		20	35		75	200	µV/°C
vs. Power Supply Voltage			0.5			*			*		mV/V
Input Bias Current											
Initial	@ +25°C		1	2		*	*		*	*	nA
vs. Temperature			Doubles			*			*		/10°C
Input Offset Current											
Initial	@ +25°C		±100			*			*		pA
Input Impedance											
Differential	}In parallel with 5pF		10^{10}			*			*		Ω
Common Mode			10^{10}			*			*		Ω
Input Voltage Range											
Common Mode		±10		±18	*		*	*		*	V
Differential				±18			*			*	V
Common Mode Rejection			70			*			*		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ										
dc to 100kHz			5			*			*		µV rms
dc to 2MHz			7			*			*		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω; Load = 100Ω		300			*			*		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 100Ω		320			*			*		V/µs
Overload Recovery	50% Overdrive		400			*			*		ns
Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100			*			*		MHz
Small Signal Bandwidth, −3dB	A = −1; R_{FF} = R_{FB} = 500Ω		45			*			*		MHz
	A = −1; R_{FF} = R_{FB} = 1000Ω		35			*			*		MHz
	A = −2; R_{FF} = R_{FB} = 500Ω; R_{FB} = 1000Ω		35			*			*		MHz
	A = −4; R_{FF} = R_{FB} = 250Ω; R_{FB} = 1000Ω		30			*			*		MHz
Output Impedance				<1			*			*	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω; 100Ω load; 10pF capacitance										
	5-volt p-p output		25			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		55			*			*		MHz
	A = 3; R_{FF} = 500Ω; R_{FB} = 1000Ω; 100Ω, 1000 Ω; or 2000Ω load; 10pF capacitance										
	10-volt p-p output		17			*			*		MHz
	5-volt p-p output		25			*			*		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued)		HOS-050			HOS-050A			HOS-050C			
Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ωload/10pF capacitance										
	5-volt p-p output		15			*			*		MHz
	4-volt p-p output		30			*			*		MHz
	2-volt p-p output		40			*			*		MHz
	1-volt p-p output		40			*			*		MHz
Full Power Bandwidth (−3dB)	Output = ±5V; A = −1; R_L = 100Ω		20			*			*		MHz
Settling Time to 0.1%	A = −1; R_{FF} = R_{FB} = 500Ω										
Inverting	V_{OUT} = ±5V		100			*			*		ns
(See Figure 5)	V_{OUT} = ±2.5V		80			*			*		ns
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω Max Load capacitance = 75pF										
	V_{OUT} = ±5V		200			*			*		ns
	V_{OUT} = ±2.5V		135			*			*		ns
Harmonic Distortion (See Figure 9)	A = −1; Load = 1000Ω Signal = 4MHz; 2V output		−63			*			*		dB
Noninverting Harmonic Distortion (See Figure 10)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V output		−59			*			*		dB
Power Supply											
Voltage	Rated performance		±15			*			*		V dc
Voltage	Operating range	±12		±18	*		*	*		*	V dc
Current	Quiescent		±20	±25		*	*		*	*	mA
Power Consumption	Quiescent		0.6			*			*		W
Power Dissipation				1.25			*			*	W
Temperature Range											
Operating (Case)	(See Figure 2 for	−55		+125	*		*	−25		+85	°C
Storage	Derating Information)	−65		+150	*		*	*		*	°C
Meantime Between Failures (MTBF)	MIL-HNBK 217; Ground; Fixed; Case = 70°C				6.27 × 10^6						Hours

Notes:
[1]Specification for Inverting Mode unless otherwise noted.
*Specification same as HOS-050

Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.
Specifications subject to change without notice.

PIN DESIGNATIONS[1]

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	− INPUT
6	+ INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

[1]SEE SECTION 19 (H12A) FOR PACKAGE OUTLINE INFORMATION.
*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

The HOS-050 Series stands up under close scrutiny of these characteristics because of its 100MHz gain bandwidth product. The use of these amplifiers in a wide variety of applications has confirmed their suitability for video circuits.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-050 are generally characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A converter output voltage amplification or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed forward resistor for the op amp.

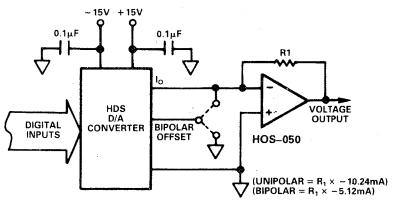


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The HDS Series D/A converters are fast-settling, current output D/As available in 8-, 10-, and 12-bit resolutions. Both TTL and ECL versions are available, and settling times range from 10ns for 8-bit units through 40ns for 12-bit units.

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and bipolar offset grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

An approximation of the total settling time for the D/A op amp combination is calculated by:

$$T_S = \sqrt{T_D^2 + T_O^2}$$

where T_D is D/A settling time and T_O is HOS-050 settling time.

This approximation is valid because both the D/A and the HOS-050 exhibit 6dB/octave roll-off charateristics (single pole response); and the combination of low D/A output capacitance and op amp input capacitance does not materially affect the formula.

The user of the HOS-050 should remember the current flowing in the feedback resistor (R1) must be subtracted from the output available from the HOS-050.

There is a tendency, because of this fact, to use a high value of feedback resistor to assure maximum current drive being available for driving low impedances; but this approach may create undesirable side effects.

Calculating the minimum load that can be driven under two conditions of feedback resistor values will serve to illustrate the difference.

Assume the feedback resistor value is 500Ω. If output voltage of the HOS-050 is 10 volts, and output current is 100mA, minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 20mA} = \frac{10V}{80mA} = 125\Omega \text{ minimum load}$$

where: E_O max = peak voltage needed
I_O max = maximum continuous current HOS-050 can produce
I_{RFB} = current in feedback resistor at peak voltage

Assume the feedback resistor value is 5,000Ω. Minimum load would be:

$$\frac{E_O \text{ max}}{I_O \text{ max} - I_{RFB}} = \frac{10V}{100mA - 2mA} = \frac{10V}{98mA} = 102\Omega \text{ minimum load}$$

Designs which strive for driving a minimum load (by increasing the feedback resistor) can create settling problems because of a fundamental characteristic of op amp circuits . . . the higher the feedback resistance, the slower the system response.

This phenomenon is the result of increased impedance for driving stray capacitances in the circuit employing the op amp, and fixed capacitances in the summing node.

Impedances need to be kept as low as possible consistent with low distortion; and stray capacitances need to be eliminated to the maximum possible extent. A large ground plane structure is recommended to help assure low ground impedances. In addition, 0.1μF ceramic capacitors and 3-10μF tantalum capacitors connected as close as possible to power supply inputs will decrease the potential for parasitic oscillations and other noise signals.

Another argument for limiting the size of the feedback resistor is because of its effect on bandwidth. Bandwidth of the HOS-050 op amp and the value of the feedback resistor are inversely related.

At any given gain of the op amp, the gain setting with the widest bandwidth will be the one which employs the lower value of feedback. As an example, a gain of 1 can be achieved with $R_{FF} = R_{FB} = 500\Omega$; or $R_{FF} = R_{FB} = 1{,}000\Omega$. Small-signal bandwidth for the first combination is typically 45MHz; bandwidth for the second is typically 35MHz.

OFFSET AND GAIN ADJUSTMENT

Figure 4 shows a method of using the HOS-050 op amp which allows adjusting the offset and gain of the output voltage.

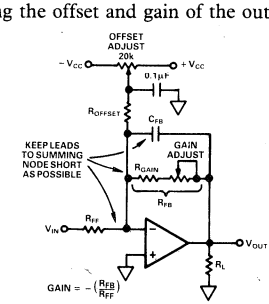


Figure 4. HOS-050 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right)$$

where R_{FB} is the total of R_{GAIN} and Gain Adjust.

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Assume $\pm V_{CC} = \pm 15V$; $R_{GAIN} = 900\Omega$; Gain Adjust = 100Ω; the desired change on the output = ± 1 volt.

Under these conditions, R_{OFFSET} will be $15k\Omega$:

$$R_{OFFSET} = -\left(\frac{15V \times [900 + 100]}{1V}\right)$$

$$R_{OFFSET} = -\left(\frac{15kV}{1V}\right)$$

$$R_{OFFSET} = 15{,}000\Omega$$

Figure 4 shows bipolar output operation. If unipolar output is desired, the appropriate V_{CC} should be removed from the Offset Adjust potentiometer.

The $0.1\mu F$ capacitor attached to the wiper arm of the Offset Adjust control isolates the control and helps prevent adjustment noise from appearing on the output of the HOS-050.

C_{FB} can be any value between 0 and 20pF, depending on the value of R_{GAIN}; and should be selected to optimize settling time for the particular circuit layout in which the HOS-050 is being used.

The Gain Adjust control should be a low value, low inductance cermet trimming potentiometer.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-050 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

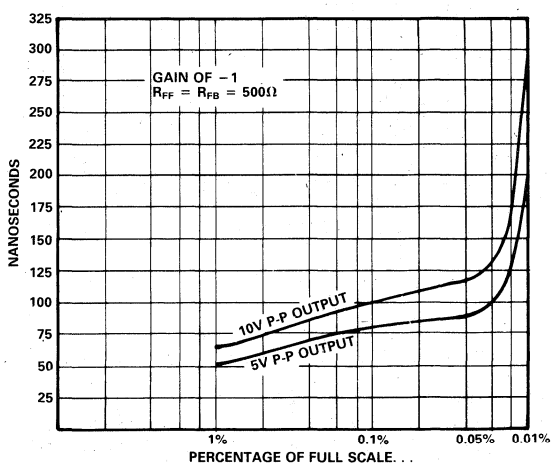


Figure 5. Settling Time – Inverting Mode

SETTLING TIME MEASUREMENT

Although there are some exceptions, most members of industry are in agreement on the description which says settling time is:

> The interval of time from the application of an ideal step function input until the closed-loop amplifier output has entered and remains within a specified error band.

The well-informed user needs to be alert to the consequences of settling time specs which do not meet that description.

This definition encompasses the major components which comprise settling time. They include (1) propogation delay through the amplifier; (2) slewing time to approach the final output value; (3) the time of recovery from the overload associated with slewing; and (4) linear settling to within the specified error band.

Expressed in these terms, the measurement of settling time is obviously a challenge and needs to be done accurately to assure the user that the amplifier is worth consideration for his application.

Figure 6 is the test circuit for measuring settling time to 0.1%. This method creates a "false" summing junction and the error band is observed at that point.

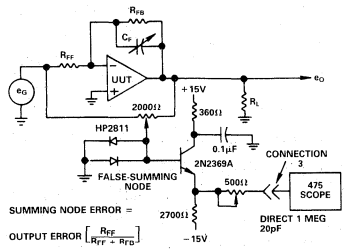


Figure 6. Settling Time Test Circuit for 0.1% Settling

If one were to attempt the measurement at the "true" summing junction of the op amp, the results would be misleading. All scope probes will add capacitance to the input and will change the response of the system. Making the measurement at the output of the amplifier is also impractical, since scope nonlinearities and reading inaccuracies caused by overdriving the scope preclude accurate measurements to the tolerances which are required.

The false summing junction method causes the amplifier to subtract the output from the input; only one-half the actual error appears at the false junction, and it can be measured to the required accuracies.

The false junction is clamped with diodes to limit the voltage excursion appearing at that point. This is necessary because the amplifier will be overdriven and one-half its input voltage will appear at the junction. Without the clamps, the scope used for making the measurement would be overdriven and its recovery time would mask the settling time of the amplifier.

The test circuit for measuring settling time to 0.01%, Figure 7, is simply an extension of the same basic technique. Measuring to the closer tolerance requires additional gain in the circuit driving the oscilloscope.

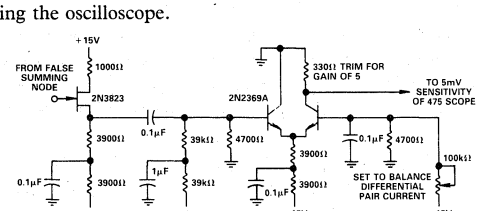


Figure 7. Settling Time Test Circuit for 0.01% Settling

IMPEDANCE MATCHING

The characteristics of the HOS-050 operational amplifier make it an ideal choice for matching the impedances of video circuits to the impedances of transmission lines.

In this application, source and load terminating resistors will cause the output voltage to be halved at the end of the cable

being driven by the op amp. This makes it necessary to set the gain of the circuit to provide twice the desired voltage.

Three different values of resistors and cables are "phantomed" into the figure as examples of possible characteristic impedances which might be used. Figure 8 is *not* meant to imply the HOS-050 can drive three cables simultaneously.

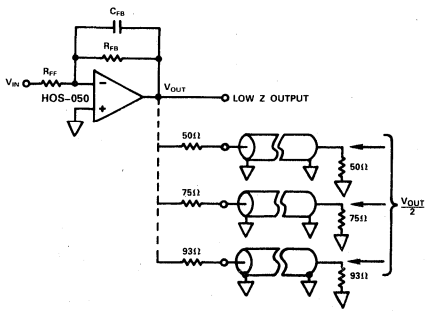


Figure 8. HOS-050 Impedance Matching

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by incresing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The overall input capacitance of the op amp is kept as low as possible in the design; and any mismatch in the capacitance of the two channels appears as an error in the output. Because of the inherently low total input capacitance of the op amp, even a small capacitive mismatch between channels shows up as a large effective error signal.

Decreasing the channel mismatch can be achieved only by complicating the design of the op amp with additional components, and rigorous selection of those components in the manufacturing process.

As a consequence, the mismatch is reduced to the smallest practical value consistent with the economics of producing and using the op amp. But it remains a mismatch, and manifests itself as a difference in performance in the inverting versus noninverting modes.

There are video op amps available at low cost which use a 741-type amplifier for high dc open loop gain in the noninverting channel. The user of these kinds of designs may sometimes gain an economic advantage, but at a high cost in performance. Bandwidths for noninverting applications are often measured in kHz, not MHz, for this approach.

A video op amp is acting as a voltage mode device at both inputs when operating in the noninverting mode. This contrasts with the inverting mode, where it is operating as a current mode device.

The Analog Devices HOS-050 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in many competing units.

The HOS-050 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

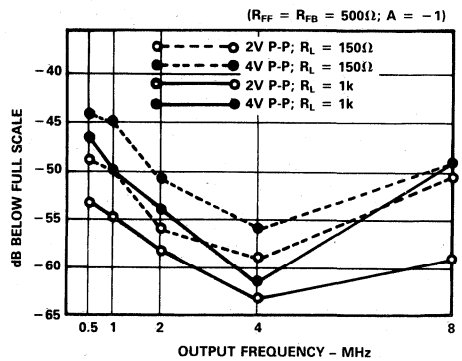


Figure 9. Harmonic Distortion – Inverting

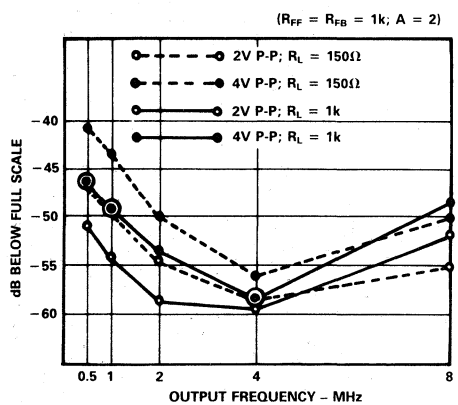


Figure 10. Harmonic Distortion – Noninverting

IN SUMMARY . . . A CAVEAT

Settling time specifications, bandwidth capabilities, harmonic distortion performance, and other parameters for video op amps cannot possibly include all possible situations and applications.

A multitude of seemingly insignificant conditions can have a major impact on the unit and its ability to operate in any given circuit.

The potential user is strongly urged to evaluate the effectiveness of the HOS-050 in the actual circuit in which it will be used. In many instances, the application conditions are different from the conditions used in specifying; there is no substitute for a trial in the proposed circuit to determine if the op amp will provide the desired results.

Low Offset, Fast Settling Video Operational Amplifier

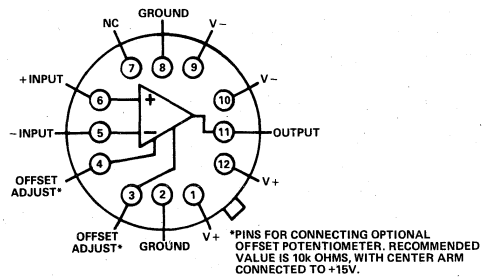
HOS-060

4

FEATURES
<1mV V_{OS}
Low Drift
80ns Settling to 0.1%; 200ns to 0.01%
100mA Output @ ±10V

APPLICATIONS
D/A Current Converter
Video Pulse Amplifier
CRT Deflection Amplifier
Wideband Current Booster

HOS-060 PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-060 Operational Amplifier is an extension of the proven hybrid technology used in the HOS-050 series of op amps.

The FET input and high-performance characteristics, including wide bandwidth and fast settling, make it useful for a variety of applications in the processing of video signals.

Recent innovations in circuit design have been incorporated into the HOS-060 to make it extremely useful to the designer who needs outstanding performance in current boosting, voltage amplification, impedance matching, or a multiplicity of other high-frequency requirements.

Voltage offset and its temperature coefficient have been dramatically improved in the HOS-060; offset is as low as most high performance monolithic op amps.

The HOS-060 op amp is pin-for-pin compatible with its forerunner HOS-050 and is useable in the same diversity of video requirements. The reader is strongly urged to refer to the six-page data sheet for the HOS-050 op amp to obtain additional insight and details on potential uses for the HOS-060.

The HOS-060 Operational Amplifier package is the industry standard TO-8 metal can and operates over a case temperature range of −55°C to +125°C; the model number for the standard unit is HOS-060SH.

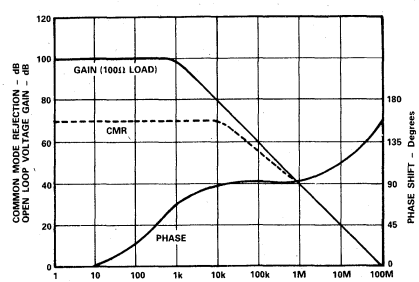


Figure 1. HOS-060 Frequency Response

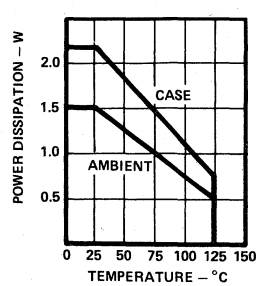


Figure 2. Power Derating

SPECIFICATIONS (typical @ +25°C and ±15V unless otherwise specified)

Model	HOS-060SH
ABSOLUTE MAXIMUM RATINGS	
Supply Voltages (V_S)	±18V
Power Dissipation	See Figure 2
Input Voltage	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Operating Temperature Range (case)	−55°C to +125°C
Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 sec.)	300°C

DC ELECTRICAL CHARACTERISTICS

Parameter	Conditions	Min	Typ	Max	Units
Open Loop Gain	R_L = 100Ω		100		dB
Rated Output					
Current					
(not short circuit protected)	R_L = >100Ω		±100		mA
Voltage	R_L = >200Ω	±10			V
Input Offset Voltage	Adjustable to Zero				
Initial	@ +25°C		±0.5	±1	mV
−25°C to +125°C				±2	mV
vs. Case Temperature					
−55°C to +125°C			10		µV/°C
vs. Power Supply Voltage			0.5		mV/V
Input Bias Current					
Initial	@ +25°C		1	2	nA
vs. Temperature			Doubles		/10°C
Input Offset Current					
Initial	@ +25°C		±100		pA
Input Impedance					
Differential	}In parallel with 5pF		10^{10}		Ω
Common Mode			10^{10}		Ω
Input Voltage Range					
Common Mode		±10		±18	V
Differential				±18	V
Common Mode Rejection			70		dB
Input Noise	R_{FF} = 100Ω; R_{FB} = 1kΩ				
dc to 100kHz			5		µV rms
dc to 2MHz			7		µV rms

AC ELECTRICAL CHARACTERISTICS[1]

Parameter	Conditions	Min	Typ	Max	Units
Slew Rate	A = −1; R_{FF} = R_{FB} = 500Ω; Load = 100Ω		300		V/µs
Noninverting Slew Rate	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 100Ω		320		V/µs
Overload Recovery	50% Overdrive		400		ns
Gain Bandwidth Product	R_{FF} = R_{FB} = 500Ω		100		MHz
Small Signal Bandwidth, −3dB	A = −1; R_{FF} = R_{FB} = 500Ω		45		MHz
	A = −1; R_{FF} = R_{FB} = 1000Ω		35		MHz
	A = −2; R_{FF} = 500Ω; R_{FB} = 1000Ω		35		MHz
	A = −4; R_{FF} = 250Ω; R_{FB} = 1000Ω		30		MHz
Output Impedance				<1	Ω
Noninverting Bandwidth, −3dB	A = 2; R_{FF} = R_{FB} = 1000Ω; 100Ω load; 10pF capacitance				
	5-volt p-p output		25		MHz
	4-volt p-p output		30		MHz
	2-volt p-p output		55		MHz
	A = 3; R_{FF} = 500Ω; R_{FB} = 1000Ω; load = 100Ω, 1000Ω, or 2000Ω; capacitance = 10pF				
	10-volt p-p output		17		MHz
	5-volt p-p output		25		MHz

AC ELECTRICAL CHARACTERISTICS[1] (Continued) — **HOS-060SH**

Parameter	Conditions	Min	Typ	Max	Units
Noninverting Bandwidth, −3dB (continued)	A = 5; R_{FF} = 500Ω; R_{FB} = 2000Ω; 100Ω, 1000Ω, or 2000Ωload/10pF capacitance				
	5-volt p-p output		15		MHz
	4-volt p-p output		30		MHz
	2-volt p-p output		40		MHz
	1-volt p-p output		40		MHz
Full Power Bandwidth (−3dB)	Output = ±5V; A = −1; Load = 100Ω		20		MHz
Settling Time to 0.1%	A = −1; R_{FF} = R_{FB} = 500Ω				
Inverting	V_{OUT} = ±5V		100		ns
	V_{OUT} = ±2.5V		80		ns
Noninverting	A = 2; R_{FF} = R_{FB} = 500Ω Max Load capacitance = 75pF				
	V_{OUT} = ±5V		200		ns
	V_{OUT} = ±2.5V		135		ns
Harmonic Distortion (See Figure 5)	A = −1; Load = 1000Ω Signal = 4MHz; 2V output		−63		dB
Noninverting Harmonic Distortion (See Figure 6)	A = 2; R_{FF} = R_{FB} = 1000Ω; Load = 1000Ω; Signal = 4MHz; 2V output		−59		dB
Power Supply					
Voltage	Rated performance		±15		V dc
Voltage	Operating range	±12		±18	V dc
Current	Quiescent		±20	±25	mA
Power Consumption	Quiescent		0.6		W
Power Dissipation				1.25	W
Temperature Range					
Operating (Case)	(See Figure 2 for	−55		+125	°C
Storage	Derating Information)	−65		+150	°C

NOTES
[1]Specification for Inverting Mode unless otherwise noted.
*Specifications same as HOS-060SH.
Individual socket assemblies (one per pin) are available from AMP as part number 6-330808-0.
Specifications subject to change without notice.

PIN DESIGNATIONS[1]

PINS	FUNCTION
1	+V
2	GROUND
3	OFFSET ADJ*
4	OFFSET ADJ*
5	−INPUT
6	+INPUT
7	NC
8	GROUND
9	−V
10	−V
11	OUTPUT
12	+V

NOTES
[1]SEE SECTION 19 (H12A) FOR PACKAGE OUTLINE INFORMATION.
*PINS FOR CONNECTING OPTIONAL OFFSET POTENTIOMETER. RECOMMENDED VALUE IS 10k OHMS, WITH CENTER ARM CONNECTED TO +15V.

VOLTAGE AMPLIFIERS/CURRENT BOOSTERS

Video op amps such as the HOS-060 are characterized by high gain bandwidth products, fast settling times, and high output drive.

One of the most common uses of video op amps is for D/A current to voltage conversion or current boosting. Figure 3 is one example of this type of application. In this circuit, the internal resistance of the D/A is the feed-forward resistor for the op amp.

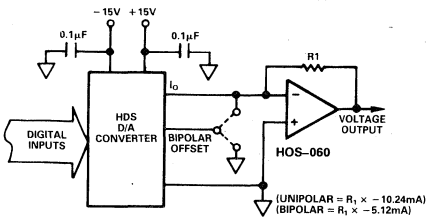


Figure 3. Inverting Unipolar or Bipolar Voltage Output

The circuit which is shown will provide a negative unipolar output with binary coding on the input, and the bipolar offset pin grounded. It will provide a bipolar output with complementary offset binary coding on the input, and bipolar offset connected to I_O.

OFFSET AND GAIN ADJUSTMENT

The low value of offset may preclude the need for adjustment, but Figure 4 shows a method of adjusting both offset and gain.

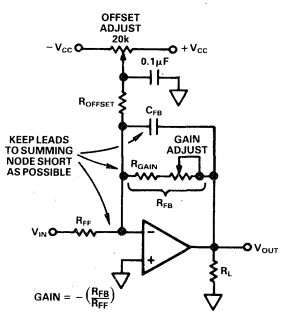


Figure 4. HOS-060 Offset and Gain Adjust

As shown, the gain of the circuit is established by the equation:

$$G = -\left(\frac{R_{FB}}{R_{FF}}\right) \text{ where } R_{FB} = R_{GAIN} + \text{Gain Adjust.}$$

Once the user has established the desired gain for the illustrated circuit, the value of R_{FB} can be used to determine the correct value of R_{OFFSET} with the equation:

$$R_{OFFSET} = -\left(\frac{V_{CC} \times R_{FB}}{\Delta E_O}\right)$$

where ΔE_O is the desired amount of offset on the output.

Note: R_{FF}, R_{GAIN}, C_{FB} and R_{OFFSET} must be located as close to the summing node of the HOS-060 as physically possible. This helps prevent additional capacitance in the summing node and corresponding bad effects on frequency response and settling times.

Variable controls (such as Offset Adjust and Gain Adjust) should never be tied to the summing node of the op amp. Their correct electrical locations are those shown in Figure 4.

NONINVERTING OPERATION

The vast majority of video operational amplifiers display marked differences in settling times and bandwidths when operated in a noninverting mode instead of the inverting mode. There are a number of valid reasons for this characteristic.

Most high-speed op amps use feed-forward compensation for optimizing performance in the inverting mode. This is necessary to obtain wide gain-bandwidth products while maintaining dc performance in these types of devices. In effect, the op amp has a wideband ac channel which is not perfectly matched to the dc channel.

Feed-forward techniques enhance the performance of the op amp in the inverting mode by increasing the slew rate and small-signal bandwidth. These techniques, however, also decrease the amplifier's tolerance to stray capacitances, so must be employed judiciously.

The Analog Devices HOS-060 has different performance characteristics when operating as a noninverting amplifier, but the care used in the design makes the differences less pronounced than they are in the designs of competing units.

The HOS-060 can be considered a true differential video op amp. It requires little or no external compensation because its rolloff characteristics approach a 6dB/octave slope. This helps the user determine summing errors and loop response; and helps assure the stability of the system.

The performance parameters for both inverting and noninverting operation are shown elsewhere in this data sheet (see SPECIFICATIONS section and figures). A comparison of the characteristics will highlight the similarities in performance, with the exceptions noted above.

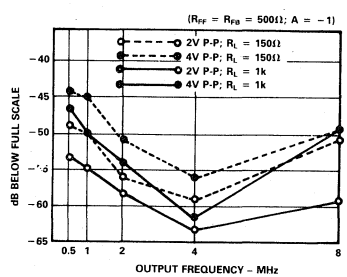


Figure 5. Harmonic Distortion – Inverting

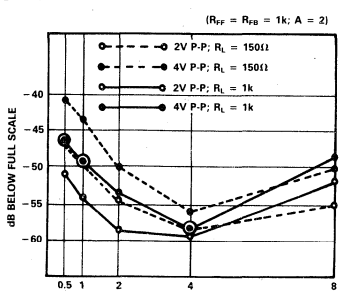


Figure 6. Harmonic Distortion – Noninverting

THE READER IS URGED TO CONSULT THE HOS-050 DATA SHEET FOR ADDITIONAL APPLICATIONS INFORMATION. THE HOS-060 IS PIN-FOR-PIN COMPATIBLE WITH THE HOS-050 SERIES AND CAN BE USED IN SIMILAR WAYS.

ANALOG DEVICES

Wide Bandwidth, High Speed Buffer Amplifiers

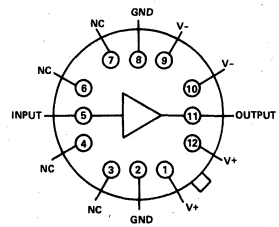
HOS-100AH, 100SH

4

FEATURES
- Wide Bandwidth – dc to 125MHz
- High Slew Rate – 1500V/μs
- Operation Guaranteed -55°C to +125°C (SH)
- High Output Drive – ±10V with 100Ω Load

APPLICATIONS
- Current Boosters
- High Speed A/D Input Buffers
- Nuclear Instrumentation Amplifiers
- Coaxial Cable Drive
- High Speed Line Drivers
- Video Impedance Transformation

HOS-100SH/HOS-100AH PIN DESIGNATIONS



TO-8 PACKAGE
BOTTOM VIEW

GENERAL DESCRIPTION

The HOS-100SH and HOS-100AH Bipolar Buffer Amplifiers are high-speed, voltage follower/buffers designed to provide high-current drive at frequencies from dc to over 125MHz, as well as providing ±10mA into 1kΩ loads (±100mA peak) at slew rates of 1500V/μs. Both units also exhibit excellent phase linearity (2°), and low distortion (<0.1%).

For commercial temperature ranges the HOS-100AH is specified for operation over the range of -25°C to +85°C (case). The HOS-100SH is specified for operation over the extended range of -55°C to +125°C (case).

The HOS-100SH and HOS-100AH are intended to fulfill a wide range of buffer applications, such as video impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high-speed line drivers and nuclear instrumentation amplifiers. Additionally, both amplifiers will continuously drive 50Ω coaxial cables or serve as yoke drives in high resolution CRT displays.

They are particularly well suited for current booster applications (Figure 3) within an op-amp loop where input impedance and bias current requirements are less stringent than in FET design.

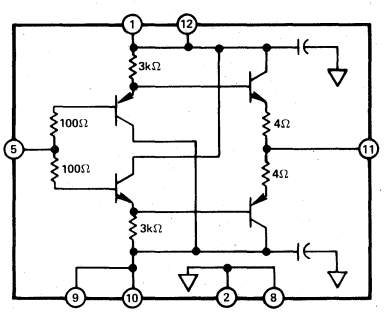


Figure 1. Schematic Diagram HOS-100

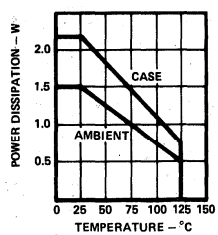


Figure 2. Power Derating

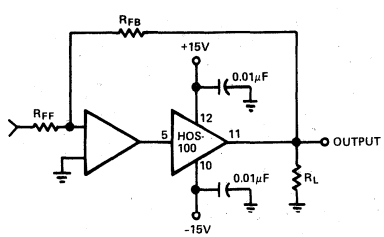


Figure 3. Current Booster

SPECIFICATIONS

PARAMETER	CONDITIONS	HOS-100SH MIN	HOS-100SH TYP	HOS-100SH MAX	HOS-100AH MIN	HOS-100AH TYP	HOS-100AH MAX	UNITS
DC ELECTRICAL CHARACTERISTICS[1,2]								
Input Bias Current	$T_C = 25°C$		5	20		5	25	μA
				25				μA
Input Impedance	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	100	200		100	200		kΩ
Voltage Gain	V_{IN} = 1V rms, f = 1kHz R_L = 1k, $T_C = 25°C$	0.95	0.97	1.0	0.94	0.96	1.0	V/V
Output Offset Voltage	$R_S = 50Ω$, $T_C = 25°C$		5	10		10	25	mV
				25			35	mV
Output Offset Voltage T_C	$R_S = 50Ω$		25	75		25	75	μV/°C
Output Impedance	V_{IN} = 1V rms, f = 1kHz $R_S = 500Ω$, R_L = 1k		8	12		8	12	Ω
Output Voltage Swing	$R_S = 50Ω$, R_L = 1k	±12	±13		±12	±13		V
	$V_S = ±5V$, R_L = 1k		6			6		V
Supply Current	V_{IN} = 0V, $T_C = 25°C$							
	$V_S = ±15$		13	16		15	20	mA
	$V_S = ±5$		10			10		mA
Power Consumption	V_{IN} = 0V, $V_S = ±15V$ $T_C = 25°C$		390	480		450	600	mW
AC ELECTRICAL CHARACTERISTICS[3]								
Slew Rate	$V_{IN} = ±10V$	1000	1500		1000	1400		V/μs
Bandwidth	V_{IN} = 1V rms	100	125		100	125		MHz
Rise Time	$ΔV_{IN}$ = 0.5V		2	5		2	5	ns
Propagation Delay	$ΔV_{IN}$ = 0.5V		1.5			1.5		ns
Phase Nonlinearity	BW = 1 to 20MHz		2			2		Degrees
Harmonic Distortion			<0.1			<0.1		%
MTBF			$1.509×10^7$ hours					
PACKAGE TYPE[4]			H12A			H12A		

NOTES
[1] Unless otherwise noted, these specifications apply for +15V applied to Pin 12, and -15V applied to Pin 10.
[2] Unless otherwise noted, specifications apply over a temperature range, $-55°C \leq T_C \leq +125°C$ for the HOS-100SH, and $-25°C \leq T_C \leq +85°C$ for the HOS-100AH. Typical values shown are for $T_C = +25°C$.
[3] These specifications all measured with the following conditions: $T_C = +25°C$, $V_S = ±15V$, $R_S = 50Ω$, R_L = 1k.
[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ - V-) 40V
Maximum Power Dissipation 1.5W
Input Voltage . . . . . Equal to Supply Voltage
Maximum Continuous Output Current . . . . . ±100mA
Maximum Peak Output Current . . . . . ±250mA
Operating Temperature Range (Case) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Maximum Junction Temperature . . . . . +175°C

ORDERING INFORMATION

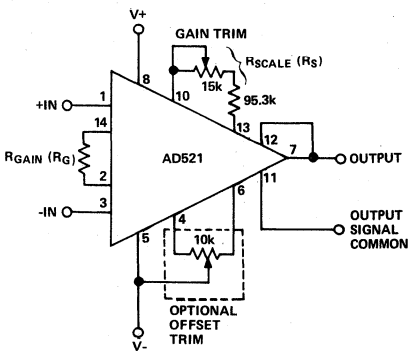
Model	Temperature Range
HOS-100AH	-25°C to +85°C
HOS-100SH	-55°C to +125°C

Instrumentation & Isolation Amplifiers

Contents

•New product since publication of *1982–1983 Databook Update.*

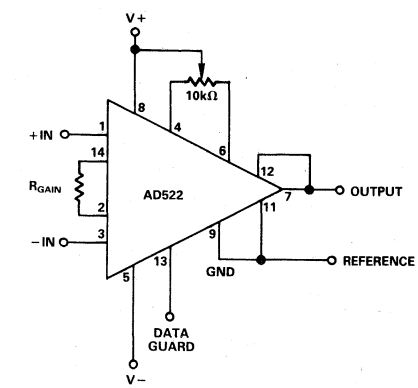
Selection Guide
Instrumentation Amplifiers



AD521

Page

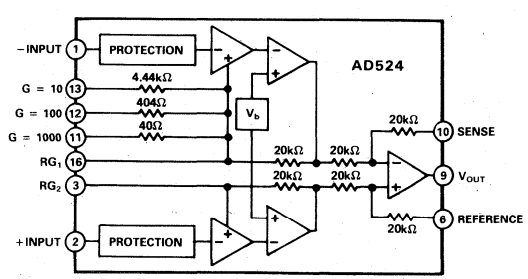
Programmable Gains from 0.1 to 1000 — Vol. I
Differential Inputs — 5-21
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000



AD522

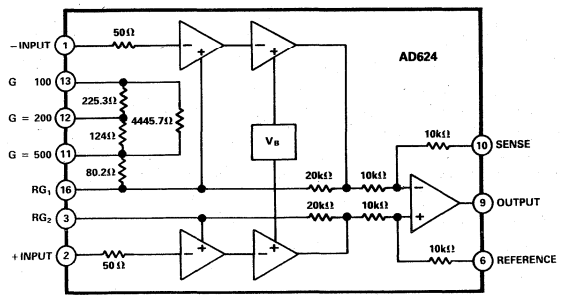
Performance — Vol. I
Low Drift: 2.0μV/°C (AD522B) — 5-27
Low Nonlinearity: 0.005% (G = 100)
High CMRR: >110dB (G = 1000)
Low Noise 1.5μV p-p (0.1 to 100Hz)
Low Initial V_{OS}: 100μV (AD522B)

Versatility
Single-Resistor Gain Programmable: 1≤G≤1000
Output Reference and Sense Terminals
Data Guard for Improving ac CMR



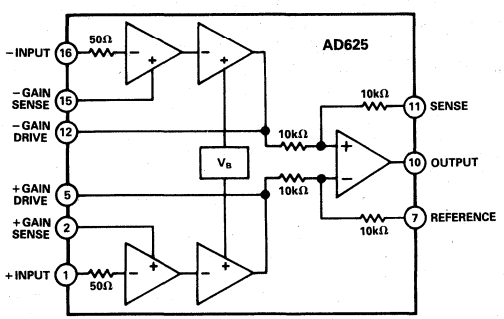
AD524

Low Noise: 0.3μV p-p 0.1Hz to 10Hz — Vol. I
Low Nonlinearity: 0.003% (G = 1) — 5-31
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated



AD624

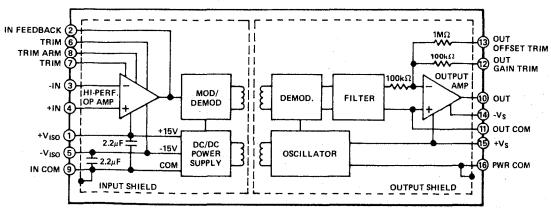
Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB max (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated



AD625

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.001% max (G =1 to 500)
High CMRR: 130dB max (G = 500)
Low Offset Voltage: 25μV max
Low Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Internally Compensated
Versatile Gain Programming
Resistor Programmable Gain Amp
Software Programmable Gain Amp

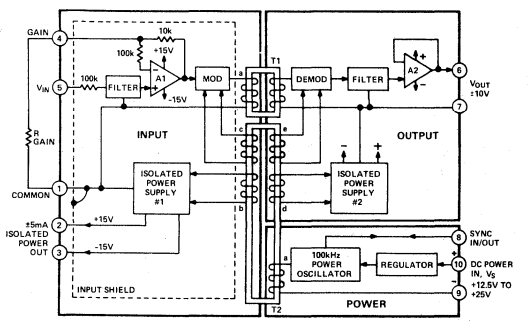
Selection Guide
Isolation Amplifiers



MODEL 277

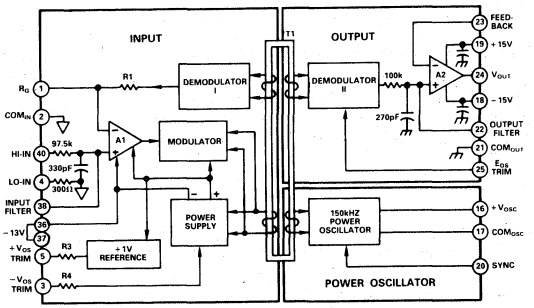
Page

Versatile Op Amp Front End: Inverting, Noninverting, Differential Applications — Vol. II 5–9
Low Nonlinearity: 0.025% max, Model 277K
Low Input Offset Voltage Drift: 1µV/°C max, Model 277K
Floating Power Supply: ±15V dc @ ±15mA
High CMR: 160dB min @ dc
High CMV: 3500V_{rms}



MODEL 289

Low Nonlinearity: ±0.012% max (289L) — Vol. II 5–17
Frequency Response: (−3dB) dc to 20kHz (Full Power) dc to 5kHz
Gain Adjustable 1 to 100V/V, Single Resistor
3-Port Isolation: ±2500V CMV Isolation Input/Output
Low Gain Drift: ±0.005%/°C max
Floating Power Output: ±15V @ ±5mA
120dB CMR at 60Hz: Fully Shielded Input Stage
Meets UL Std. 544 Leakage: 2µA rms max, @ 115V ac, 60Hz



AD293

High Common-Mode Voltage: AD293 ±2500V peak max
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Hermetically Sealed Hybrid Construction

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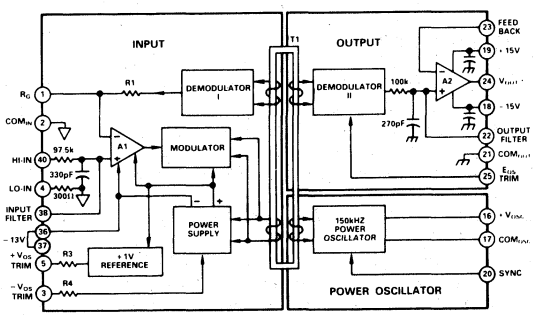
Vol. I
5-13



AD294

High Common-Mode Voltage: ±8000V peak max
Nonlinearity: ±0.05% of max
Adjustable Input & Output Gain: 1V/V to 1000V/V
Complies with NEMA ICS1-111
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz
Hermetically Sealed Hybrid Construction

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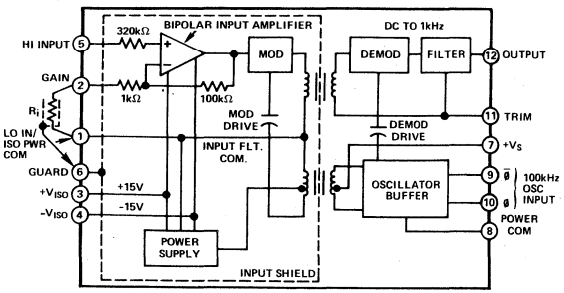
Selection Guide
Isolation Amplifiers



MODEL 284

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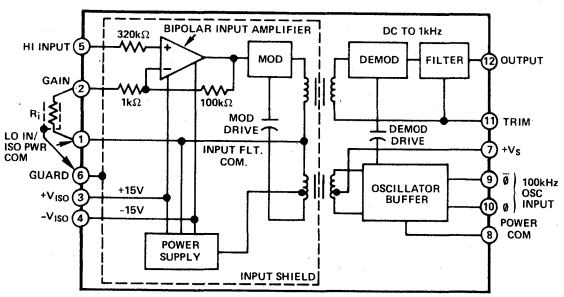
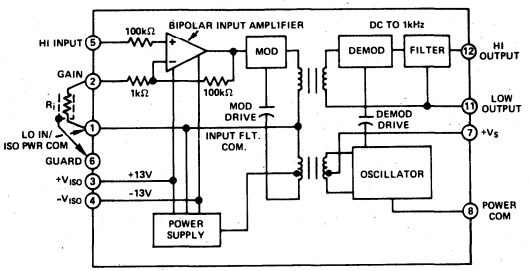
High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
High CMR: 110dB min with 5kΩ Imbalance
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Low Input Offset Voltage Drift: 10μV/°C, G = 100V/V
Resistor Programmed Gain: 1 to 10V/V (284J)
Isolated Power Supply: ±8.5V dc @ ± 5mA (284J)
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.0μA max (284J)



MODEL 286

Vol. II
5-11

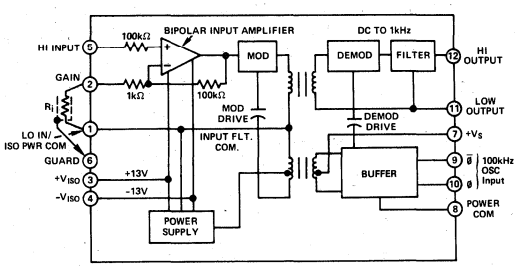
High CMV Isolation: ±5000V pk, 10ms Pulse; ±2500V dc Continuous
High CMR: 110dB min with 5kΩ Imbalance
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Low Input Offset Voltage Drift: 10μV/°C, G = 100V/V
Resistor Programmed Gain: 1 to 100V/V (286J)
Isolated Power Supply: ±15V dc @ ± 15mA (286J)
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage @ 115V ac, 60Hz: 2.5μA max (284J)



MODEL 290A

Page

Isolated Power Supply: ±13V dc @ ±5mA (290A) Vol. II 5-21
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V



MODEL 292A

Multichannel Capability Using External Oscillator (292A) Vol. II 5-21
Isolated Power Supply: ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

Orientation
Instrumentation & Isolation Amplifiers

An instrumentation amplifier is a committed "gain block" that measures the difference between the voltages existing at its two input terminals, amplifies it by a precisely set gain – usually from 1V/V to 1000V/V or more – and causes the result to appear between a pair of terminals in the output circuit. Referring to Figure 1,

$$V_S - V_R = G\,(V^+ - V^-)$$

An ideal instrumentation amplifier responds only to the *difference* between the input voltages. If the input voltages are equal ($V^+ = V^- = V_{CM}$, the *common-mode voltage*), the output of the ideal instrumentation amplifier will be zero.

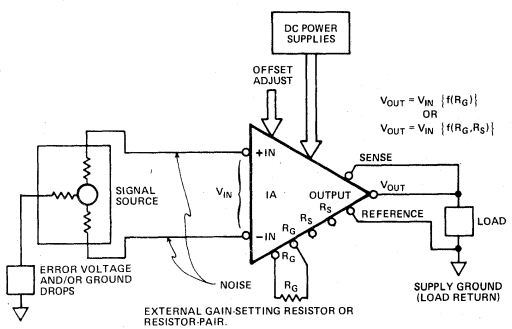


Figure 1. Basic Instrumentation Amplifier Functional Diagram

An amplifier circuit which is optimized for performance as an instrumentation-amplifier gain block has high input impedance, low offset and drift, low nonlinearity, stable gain, and low effective output impedance. It is commonly used for applications which capitalize on these advantages. Examples include: transducer amplification – for thermocouples, strain-gage bridges, current shunts, and biological probes, preamplification of small differential signals superimposed on high common-mode voltages, signal conditioning and (moderate) isolation for data acquisition, and signal translation for differential and single-ended signals wherever the common "ground" is noisy or of questionable integrity.

Instrumentation-amplifiers are usually chosen in preference to user-assembled op-amp circuitry, because they offer optimized, specified performance in low-cost, easy-to-use, compact packages. If the application calls for high common-mode voltages (typically, voltages in excess of the amplifier supply voltage), or if isolation impedances must be very high (e.g., $10^{10}\,\Omega$, with galvanic isolation, as in medical and industrial applications), the designer should consider an isolation amplifier.

SPECIFYING INSTRUMENTATION AMPLIFIERS

The instrumentation amplifier chosen for a given application will be the lowest-cost device that satisfies the performance and environmental requirements. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. It is essential that the designer have a firm understanding of the specifications of instrumentation amplifiers and of the contributions of the various sources of error to the total error. The data sheets provide much useful application data on these devices, as well as examples of basic error analyses.

Definitions of the key specifications follow a brief discussion of instrumentation-amplifier architectures. For more-complete information on the fundamentals and applications of instrumentation amplifiers, a number of publications are available from Analog Devices.[1,2,3]

INSTRUMENTATION-AMPLIFIER ARCHITECTURE

All Analog Devices instrumentation amplifiers have two high-impedance input terminals, a set of terminals for gain-programming, an "output" terminal, and a pair of feedback terminals, labeled *sense* and *reference*, as well as terminals for power supply and offset trim.*

Two basic circuit concepts are employed. The AD522, AD524, AD624 and AD625 use variations of the well-known three-op-amp configuration, consisting of a differential input-output gain stage and subtractor stage. Gain ($\geqslant$1V/V) is set by the choice of a single gain-setting resistor, R_G. When the *sense* (V_S) feedback terminal is connected to the output terminal, and the *reference* terminal (V_R) is connected to power common, the output voltage appears between the output terminal and power common.

The V_S and V_R terminals may be used for remote sensing – to establish precise outputs in the presence of line drops; they may be used with an inside-the-loop booster follower to obtain power amplification without loss of accuracy; and they may be used to establish an output current that is precisely proportional to the difference signal. A voltage applied to the V_R terminal will bias the output by a predetermined amount. It is important always to maintain very low impedance (in relation to the specified V_S and V_R input impedances), when driving the V_S and V_R inputs, in order not to introduce common-mode, gain, and/or offset errors. In devices using the 3-amplifier configuration, the V_R terminal is sometimes used for "tweaking" common-mode rejection.

NOTES

[1] *"Applications Guide for Isolation Amplifiers*, 1984 edition, available upon request.

[2] "A User's Guide to IC Instrumentation Amplifiers," by J. Riskin, 1978, available upon request.

[3] *Transducer Interfacing Handbooks*, D.H. Sheingold, ed., 1980, $14.50, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062.

*In Model 612, *sense* is internally connected to the output terminal.

SPECIFICATIONS

Specification tables are generally headed by the legend: "specifications are typical at $V_S = \pm 15V$, $T_A = +25°C$, and rated load, unless otherwise noted." This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature), the significant effects are usually indicated within the specs. "Typical" means that the manufacturer's characterization process has shown this number to be "average," but individual devices vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Such specs are not uniquely applicable to instrumentation amps.

GAIN These specifications refer to the linear transfer function of the device; for example, the AD524 gain equation is: $G = 1 + \frac{40{,}000}{R_G}$ V/V. The value of R_G for a given gain value is: $R_G = \frac{40{,}000}{G - 1}\ \Omega$. For example, if G is to be 200V/V, $R_G = 201$ ohms.

Gain Range Specified at 1 to 1000, for example, the device may work at higher gains (1 V/V is minimum, except for the AD521), but the manufacturer does not specify performance outside the range. In practice, noise and drift may make higher gains impractical for a given device.

Equation Error (or "Gain Accuracy") The number given by this specification describes deviation from the gain equation when R_G is at its nominal value. The user can trim the gain or compensate for gain error elsewhere in the overall system. Systems using microprocessors (or computers, or other digital "intelligence") can be made self-calibrating, to take into account the lumped gain errors of all the stages in the analog portion of the system, from transducer to a/d converter.

Nonlinearity (or Gain Nonlinearity) Nonlinearity is defined as the deviation from a straight line on the plot of output vs. input. The magnitude of linearity error is the maximum deviation from a "best straight line," with the output swinging through its full-scale range. Nonlinearity is usually specified in percent of full-scale output range.

Gain vs. Temperature These numbers give the deviations from the gain equation as a function of temperature.

SETTLING TIME is defined as that length of time required for the output voltage to approach and remain within a certain (±) tolerance of its final value. It is usually specified for a fast step that will drive the output through its full-scale range and it includes slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%, nor is settling time necessarily proportional to gain. Principal contributing factors include slew-rate limiting, underdamping (ringing), and thermal gradients ("long tails").

VOLTAGE OFFSET Voltage offset and common-mode rejection (see below) specifications are often considered the key figures of merit for instrumentation amplifiers. While initial offset can be adjusted to zero, shifts in offset voltage with time and temperature introduce errors. Systems that involve "intelligent" processors can correct for offset errors in the whole measurement chain, but such applications are still relatively infrequent; in most applications, the instrumentation amplifier's contribution to system offset error must be defined.

Voltage offset and offset drift in instrumentation amplifiers are functions of gain.[4] The offset, measured at the output, is equal to a constant plus a term proportional to gain. For an amplifier with specified performance over a gain range from 1 to 1000, the constant is essentially the offset at unity gain, and the proportionality term (or slope) is equal to the change in output offset between G = 1 and G = 1000, divided by 999. To refer offset to the input (RTI), divide the total output offset by the gain. Since offset at a gain of 1000 is dominated by the proportional term, the slope is often called the "RTI offset, G = 1000." At any value of gain, the offset is equal to the unity-gain offset plus the product of the gain and the "RTI offset".

The same considerations apply to the offset drift. For example, the maximum RTI drift of the AD624C is specified at $0.25\mu V/°C$. Thus, the output drift is $(0.25\mu V/°C \times G) + 10\mu V/°C$ at any gain, G, in the range.

Voltage offset as a function of power supply level is also specified RTI at one or more gain settings.

INPUT BIAS AND OFFSET CURRENTS Input bias currents are those currents needed to bias the input transistors of a dc amplifier or to supply the junction-leakage of FET's. FET-input devices have lower bias currents than those using bipolar transistors, but FET leakage currents increase dramatically with temperature, approximately doubling every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

[4] There is a good explanation of the specification of offset in instrumentation amplifiers in ANALOG DIALOGUE 6–2 (1972), p. 14

Important Note
Although instrumentation amplifiers have differential inputs, there *must* be a return path for the bias currents. If it is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying outputs of "floating" sources, such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to common, or to the *guard* terminal. If a dc return path is impracticable, an *isolator* must be used.

COMMON-MODE REJECTION (CMR) is a measure of the change in output voltage when both inputs are changed by equal amounts. CMR is usually specified for a full-range common-mode voltage change (CMV), at a given frequency, and a specified imbalance of source impedance (e.g. 1kΩ source unbalance, at 60Hz). CMR is a logarithmic expression of the *common-mode rejection ratio* (CMRR): CMR = 20 $\log_{10}$ (CMRR). The common-mode rejection ratio is defined as the ratio of the signal gain, G, to the ratio of common mode signal appearing at the output to the input CMV.

In most instrumentation amplifiers, the CMR increases with gain, because the front-end configuration does not amplify common-mode signals, and the amount of common-mode signal appearing at the output stays relatively constant as the signal gain (G) increases.

However, at higher gains, amplifier bandwidth decreases. Since differences in phase shift through the differential input stage will show up as common-mode errors, CMR becomes more frequency-dependent at high gains.

ISOLATION AMPLIFIERS

The *isolation amplifier* (or *isolator*) has an input circuit that is galvanically isolated from the power supply and the output circuit. Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process-control systems.

Analog Devices Isolators described in this catalog use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input circuit.

CHOOSING AN ISOLATOR

The choice of an isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning), and the availability of isolated power for additional external front-end circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, a designers' guide[1], available upon request, provides information useful to the circuit designer.

Functional Characteristics The basic design of both amplifiers is identical. As shown in Figure 1, an amplifier is divided into three isolated sections—input, output, and power—coupled together by a single transformer. A power oscillator (which may be powered by system power or a separate power source) furnishes isolated power to the input amplifier, plus a carrier, which is modulated by the amplified input signal, coupled across the isolation barrier to the output section, demodulated, and buffer-amplified by a system-powered output amplifier.

Two significant innovations are responsible for the small size and excellent performance of these amplifiers. The first is an ultra-compact transformer, using screened wiring and well-conceived assembly technology. The second is an improvement in the use of the flyback (unclamped) portion of a blocking-oscillator waveform as the modulated signal carrier (U.S. Patent 4,286,225).

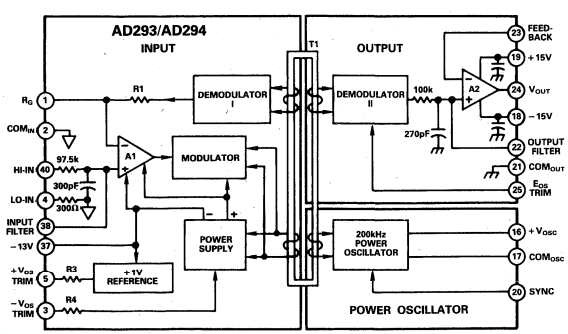


Figure 1. AD293/AD294 Block Diagram

*Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.

[1] *Analog Devices Applications Guide for Isolation Amplifiers* (1984)

As the block diagram shows, the synchronizable oscillator requires a two-wire power supply, which may be different (and (and isolated) from the power supply for the output amplifier, A2. The oscillator's output is coupled to (and loaded by, but isolated from) the circuitry connected to the other five identical transformer windings. One winding delivers power to the input amplifier, A1.

The flyback portion of the oscillator waveform is amplitude-modulate by A1's output signal, then coupled through separate transformer windings to a demodulator (I) in the amplifier's feedback path. Since A1 is an operational amplifier, the feedback signal must replicate the input signal (gain, from 1 to 100V/V, is equal to $1 + R_S/R_G$), and the transformer flux during flyback must be whatever is necessary to make this happen. The common flux, through an identical winding, applied to an identical demodulator (II), causes its output to be very nearly identical to the voltage at the output of the first demodulator, i.e., an accurately amplified version of the input signal. The other winding connected to Demodulator II provides a reference signal. The output of the demodulator is filtered and buffered by output amplifier, A2, which may be connected for gain values from 1 to 10V/V.

The AD293 and AD294 are *3-port* isolators; the input, output, and power sections are mutually isolated from one another. The use of separate substrates for the spiral-winding triplets of the transformer makes possible isolation of ±2500V (peak or continuous) for the AD293, and ±8000V (peak, 10ms pulse) for the AD294, between the input and output/power circuits. The high-temperature-fired dielectrics between the individual windings permit 500V rms of isolation between the output and power ports.

Hybrid Industrial/ Medical Isolation Amplifier

AD293/AD294

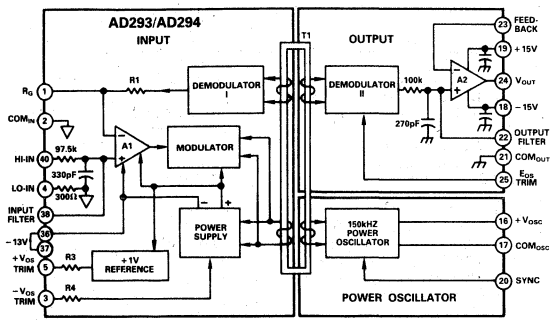
FEATURES

High Common-Mode Voltage:
AD293 ±2500V peak max, cont.
AD294 ±3500 peak max, cont.; ±8000V peak max Pulse
Nonlinearity: ±0.05% max (AD293B)
Adjustable Input & Output Gain: 1V/V to 1000V/V
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Off Ground Signal Measurement
Industrial Control
Nuclear Instrumentation
High Voltage Protection for Data Acquisition Systems
Medical Diagnostic and Patient Monitoring Equipment

AD293/AD294 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD293/AD294 are low cost, high performance isolation amplifiers designed for accurate processing of low level, industrial sensor or biomedical signals, with true galvanic isolation from high common-mode voltages, transients and lethal ground fault currents. The true hybrid architecture of the AD293/AD294 includes a proprietary hybrid magnetic transformer, all housed in a low profile (0.3") epoxy sealed, 40-pin ceramic package.

The AD293 features a maximum nonlinearity of 0.1% (AD293A) or 0.05% (AD293B) and maximum common-mode voltage isolation of either 2500V peak (continuous ac or dc) or 2500V rms (ac 60Hz, 1 minute). The AD294A provides a maximum nonlinearity of 0.1% and maximum common-mode voltage isolation of 3500V peak (continuous ac, dc) and common-mode voltage pulse (defibrillator) or transient protection of ±8000V peak.

In medical applications requiring patient isolation from lethal ground fault currents, the AD293/AD294 meet UL STD 544 leakage requirements by guaranteeing a maximum leakage current of 2μA rms (115V, 60Hz).

All versions provide small signal (−3dB) frequency response of 2.5kHz and a full power response of 200Hz (at gain of 1V/V). Both the input and output sections of the AD293/AD294 are gain programmable, allowing the user to tailor the amplifier to meet an application requirement.

WHERE TO USE THE AD293/AD294

Industrial: In process control systems, high CMV instrumentation and multi-channel computer interface systems, the AD293/AD294 provide guaranteed protection against high transient voltages, lethal ground fault currents and high common-mode voltages.

Medical: In biomedical and patient monitoring equipment such as ECG recorders, diagnostic systems and blood pressure monitors, the AD294A offers protection from lethal ground fault currents as well as 8kV peak defibrillator pulse inputs.

Low level signal recording and monitoring is achieved with the AD294A's low input noise (10μV p-p @ G = 100V/V) high CMR (100dB min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

Adjustable Gain: Gain can be selected at either the input, output, or both. Thus, circuit response can be tailored to the user's application. The input gain can be selected from 1V/V to 100V/V with a single resistor. The output gain can be selected from 1V/V to 10V/V with or without compensation. The AD293/AD294 provides the user with flexibility for circuit optimization without requiring external active components.

Buffered Output: The AD293/AD294 prevent inaccuracies related to low impedance loads by providing an uncommitted output amplifier capable of supplying ±10V @ 5mA min.

SPECIFICATIONS (typical @ + 25°C, & V_S = 15V unless otherwise noted)

MODEL	AD293A	AD293B	AD294A
GAIN			
Range	1 to 1000V/V	*	*
Formula (Input)	$G_{IN} = \left(1 + \frac{100k}{R_G}\right)$; $R_G \geq 1k\Omega$; G_{IN} max = 100		
(Output)	$G_{OUT} = \left(1 + \frac{R_A}{R_B}\right)$; $1 \leq G_{OUT} \leq 10$; G_{OUT} max = 10		
Deviation from Formula			
G = 1	± 1.0%	*	*
G>1	± 3.0%	*	*
vs. Temperature (−25°C to +85°C)[1,2] (Gain = 1)	± 60ppm/°C max	*	*
(Gain >1)	± 120ppm/°C max	*	*
Nonlinearity (± 5V swing)[2]	± 0.1% max	± 0.05% max	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	± 10V min	*	± 5V min
Max Safe Differential Input			
Continuous	120V rms max	*	*
1 Minute	240V rms max	*	*
Max CMV (Inputs to Outputs)			
Continuous (ac or dc)	± 2500V peak	*	± 3500V peak
ac, 60Hz, 1 minute Duration	2500V rms	*	3500V rms
Pulse, 10ms Duration, 1 pulse/10 sec	—	—	± 8000V peak
CMR (60Hz), G = 10V/V			
$R_S \leq 1k\Omega$ Balanced Source Impedance	108dB	*	*
$R_S \leq 1k$ Source Impedance Imbalance	100dB min	*	*
$R_S \leq 5k$ Balanced Source Impedance	—	—	100dB
$R_S \leq 5k$ Source Impedance Imbalance	—	—	95dB min
Leakage Current, Input to Output			
@ 115V ac, 60Hz	2μA rms max	*	*
Input Impedance, G = 1			
Differential	$150pF \| 10^8\Omega$	*	*
Overload	$100k\Omega$	*	*
Common Mode	$30pF \| (5 \times 10^{10}\Omega)$	*	*
Input Bias Current			
Initial @ + 25 °C	2nA (5nA max)	*	*
vs. Temperature	20pA/°C	*	*
Input Noise			
Voltage			
0.05Hz to 100Hz	10μV p-p	*	*
10Hz to 1kHz	5μV rms	*	*
Current			
0.05Hz to 100Hz	50pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal (−3dB) G = 1V/V to 100V/V	2.5kHz	*	*
Full Power, 20V p-p Output (10V p-p AD294)			
G = 1V/V (G_{IN} = 1V/V, G_{OUT} = 1V/V)	200Hz	*	*
G = 100V/V (G_{IN} = 100V/V, G_{OUT} = 1V/V)	100Hz	*	*
G = 10V/V (G_{IN} = 1V/V, G_{OUT} = 10V/V)	1.5kHz	*	*
Slew Rate	9.1V/ms	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Inital, @ +25°C, max	$\left(\pm 3 \pm \frac{22}{G_{IN}}\right)$mV	*	*
vs. Temperature (0 to +70°C)	$\left(\pm 3 + \frac{150}{G_{IN}}\right)$μV/°C		$\left(\pm 10 + \frac{300}{G_{IN}}\right)$μV/°C max
(−25°C to +85°C) max	$\left(\pm 10 \pm \frac{500}{G_{IN}}\right)$μV/°C max	$\left(\pm 5 \pm \frac{250}{G_{IN}}\right)$μV/°C	$\left(\pm 10 \pm \frac{1000}{G_{IN}}\right)$μV/°C
vs. Supply Voltage	$\left(\pm 0.01 \pm \frac{3}{G_{IN}}\right)$mV/V	*	*
RATED OUTPUT			
Voltage, 2kΩ Load	± 10V min	*	*
Output Impedance	< 1Ω	*	*
Output Ripple, (dc to 100kHz) Bandwidth	4mV p-p	*	*
POWER SUPPLY[3]			
Voltage, Rated Performance	± 15V dc ± 3%	*	*
Voltage, Operating[4]	± 12V dc ± 18V dc	*	*
Current, Quiescent (V_S = ± 15V)	+ 1mA, − 1mA	*	*
($+V_{OSC}$ = + 15V)	+ 11mA	*	*
ISOLATED POWER	− 13V dc @ 200μA	*	*
TEMPERATURE RANGE			
Rated Performance	− 25°C to + 85°C	*	*
Operating	− 40°C to + 100°C	*	*
CASE DIMENSIONS	2.64" × 0.86" × 0.35"	*	*
PACKAGE OPTION[5]	HY20A	*	*

NOTES
*Specifications same as AD293A.
[1]Gain temperature drift is specified as a percentage of output signal level @ 10V pk-pk.
[2]Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3]Recommended power supply, ADI Model 904, ± 15V @ 50mA output.
[4]Output Swing = 0.66V_S
[5]See Section 19 for package outline information.
Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	R_G	40	HI-IN
2	COM_{IN}		
3	$-V_{OS}$ TRIM	38	INPUT FILTER
4	LO-IN	37	−13V
5	$+V_{OS}$ TRIM	36	−13V
16	$+V_{OSC}$	25	E_{OS} TRIM
17	COM_{OSC}	24	V_{OUT}
18	−15V	23	FEEDBACK
19	+15V	22	OUTPUT FILTER
20	SYNC	21	COM_{OUT}

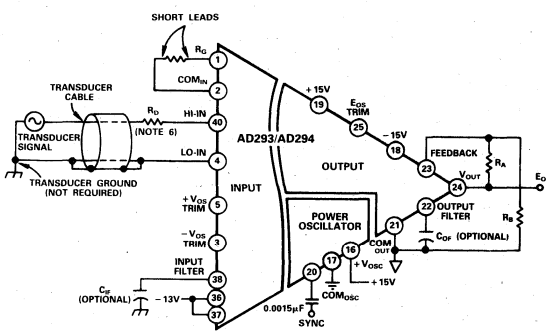
Synchronization: The unique hybrid transformer design and low power consumption of the AD293/AD294 result in very low RFI (carrier) levels which make it unnecessary to synchronize adjacent amplifiers in a multi-channel application, since "beat frequency" and cross talk caused by intermodulation are virtually eliminated.

If desired by the user, multiple AD293/AD294's may be synchronized by connecting a 0.0015μF capacitor in series with each amplifier's SYNC terminal (pin 20) and driving them with a TTL compatible, 150kHz (±10%) source. SYNC input impedance for each amplifier is approximately 8kΩ.

High Reliability: The AD293/AD294 are designed specifically to provide highly reliable operation in extremely harsh environments. These devices are available in epoxy sealed ceramic packages which use hybrid techniques and incorporate a revolutionary new hybrid magnetic transformer eliminating traditional wire wound methods.

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD293/AD294, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable, for the input signal, to reduce inductive and capacitive pickup. The cable shield should be connected to the common-mode signal source and as close as possible to their respective terminal connections so pick-up can be minimized (shown in Figure 1).



NOTES:
1. GAIN RESISTORS R_G, R_A AND R_B, 1% 50ppm/°C METAL FILM TYPE.
2. INPUT GAIN $= 1 + \frac{100k}{R_G}$; $R_G \geq 1k$; MAX INPUT GAIN = 100V/V.
3. OUTPUT GAIN $= 1 + \frac{R_A}{R_B}$; $1 \leq$ OUTPUT GAIN ≤ 10.
   FOR OUTPUT GAIN > 1, A 33pF MAY BE REQUIRED ACROSS R_A.
4. $C_{IF} = \frac{1}{2\pi F(9.75 \times 10^4)}$ FARADS $-330pF$.
5. $C_{OF} = \frac{1}{2\pi F(10^5)}$ FARADS $-270pF$.
6. R_D IS REQUIRED ONLY FOR THE AD294 TO PROVIDE PROTECTION AGAINST DEFIBRILLATOR PULSES. USE TWO 240kΩ 1/2 WATT RESISTORS. WHEN MOUNTING, PLACE THEM IN SERIES AND AWAY FROM THE PCB.

Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD293/AD294 attribute their outstanding performance to the innovation of a hybrid magnetic ceramic transformer T1 (shown in the block diagram of Figure 2). Windings are screened on two ceramic alumina substrates which are placed together separated by a ceramic isolation barrier. Then an E-core is carefully fitted around the substrates to complete the transformer.

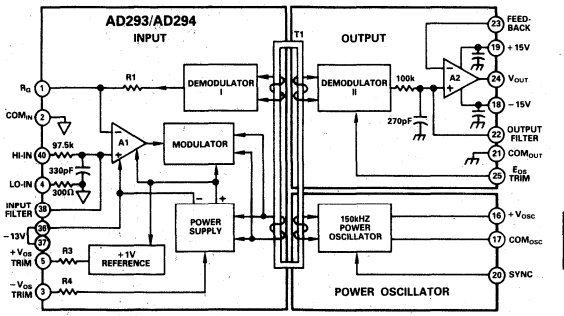


Figure 2. AD293/AD294 Block Diagram

Incorporating the carrier isolation technique, both power and signals are transferred between the amplifier's input stage and output circuitry via T1. The input signal is filtered and appears at the noninverting input of amplifier A1. This signal is then amplified by A1, with its gain (1V/V to 100V/V) determined by the value of resistance connected between R_G and COM_{IN}. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulator output voltage is filtered and then buffered by A2. Output gain (1V/V to 10V/V) and frequency compensation is determined by the value of resistance and capacitance selected between A2's feedback, V_{OUT}, and COM terminals. The 150kHz asymmetric square wave power oscillator drives the primary windings of transformer T1. The secondary windings of T1 then energizes the input power supply and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance effects are developed from stray capacitance that couple the input and output terminals together. The difference shown in Figure 3 between the AD293 and AD294 is a result of the separate transformer designs. Each terminal capacitance is shunted by leakage resistance exceeding $3.4 \times 10^9\Omega$.

Terminal Ratings: CMV performance is given in peak pulse and continuous ac or dc peak ratings. Continous peak ratings apply from dc up to the normal full power response frequencies. Figure 3 illustrates the AD293/AD294 ratings between terminals.

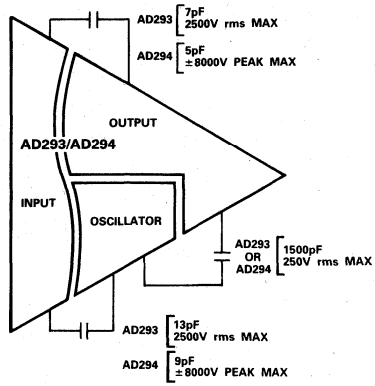


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN TRIM PROCEDURES

The calibration procedure, shown in Figure 4, illustrates the recommended techniques which can be used to minimize output error. In this example, the output span is +10V to −10V and gain = 100V/V (G_{IN} = 10V/V; G_{OUT} = 10V/V).

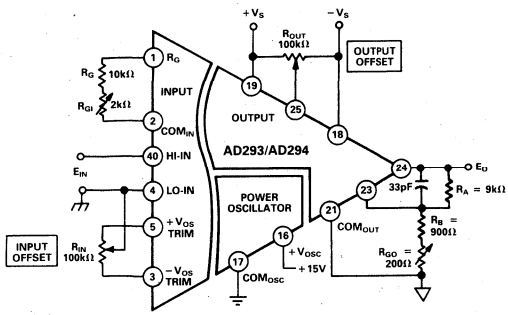


Figure 4. Recommended Offset & Gain Adjustments

Offset Adjustment

1. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
2. Apply E_{IN} = 0 volts and adjust R_{IN} for E_O = 0 volts.
3. Connect R_B to COM.
4. Adjust R_{OUT} for E_O = 0 volts.

Gain Adjustment

5. Set G_{OUT} = 1V/V by disconnecting R_B from COM.
6. Apply E_{IN} = +1.000V and adjust R_{G_I} for E_O = +10.000V.
7. Connect R_B to COM.
8. Apply E_{IN} = +0.100V and adjust R_{G_O} for E_O = +10.000V.

LEAKAGE CURRENT LIMITS

The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms of 115V ac, 60Hz in the AD293/AD294 which meet standards established by UL STD 544.

For medical applications, the AD293/AD294 are designed to improve on patient safety current limits proposed by the F.D.A., U.L., A.A.M.I. and other regulatory agencies.

In patient monitoring equipment, such as ECG recorders, the AD293/AD294 will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. With the use of passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

PERFORMANCE CHARACTERISTICS

Phase vs. Frequency: The phase vs. frequency responses for the AD293/AD294, is shown in Figure 5. The bandwidth is sufficient for the majority of isolation applications where accurate signal measurements must be made in the presence of noise and high common-mode voltages.

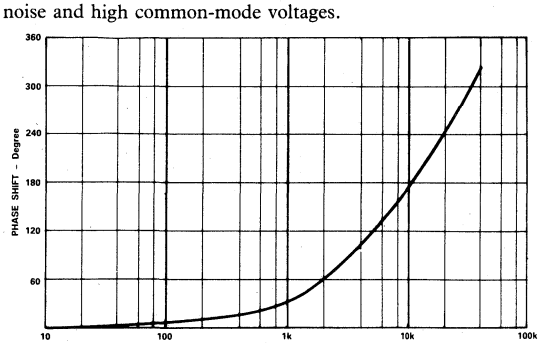


Figure 5. Typical AD293/AD294 – Phase vs. Frequency

Common-Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 60Hz and 1kΩ (AD293)/5kΩ (AD294) source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency characteristics for the AD293/AD294. CMR approaches 144dB at dc with sources impedance as high as 1kΩ (AD293)/5kΩ (AD294). Figure 7

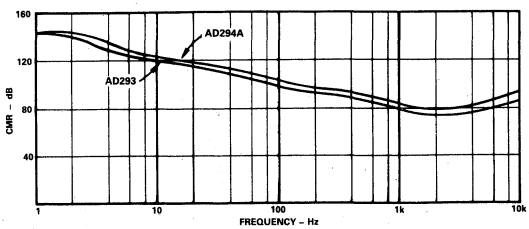


Figure 6. Typical AD293/AD294 – CMR vs. Frequency

illustrates the effect of source impedance imbalance on CMR performance at 60Hz for various gain settings. CMR is maintained greater than 60dB for source imbalances up to 100kΩ. As shown, increasing isolator gain increases CMR.

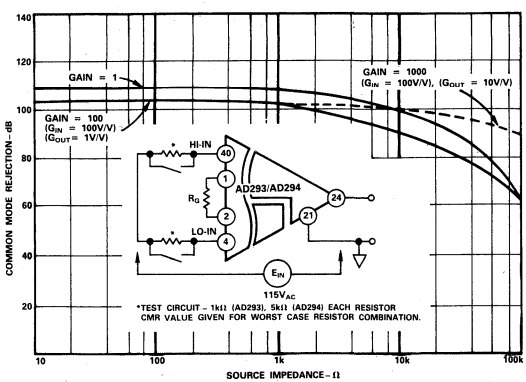


Figure 7. Typical AD293/AD294 – CMR vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise in a bandwidth from 10Hz to 100kHz is shown on the horizontal axis. The peak-to-peak value is derived by multiplying the rms value @ F = 100Hz (0.75μV rms) by 6.6.

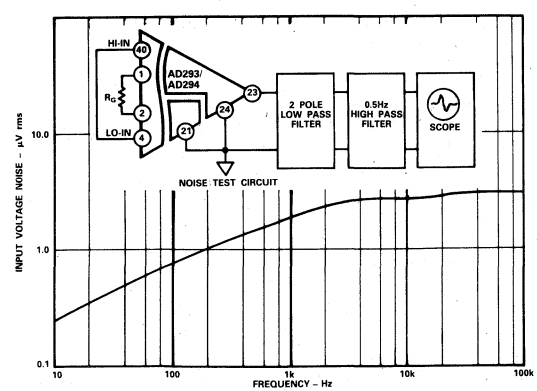


Figure 8. Typical AD293/AD294 – Input Noise vs. Frequency

For applications requiring improved noise performance, additional low pass filters may be placed at either the input or output sections to selectively roll-off noise and undesired signals beyond the bandwidth of interest.

Gain Nonlinearity vs. Gain

Figure 9, shows the AD293/AD294 gain nonlinearity vs. gain as a function of output gain. As input gain is increased, gain nonlinearity increases. Conversely, as output gain is increased to ten, gain nonlinearity decreases.

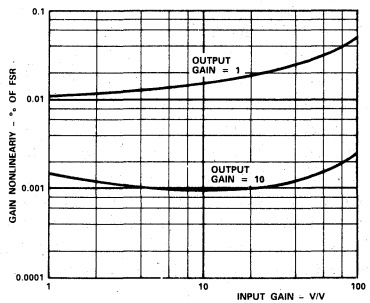


Figure 9. Typical AD293/AD294 – Gain Nonlinearity vs. Gain as a Function of Output Gain

Full Power Bandwidth vs. Gain

Figure 10 shows the full power bandwidth vs. gain with the input and output gain curves shown separately. As shown, the full power bandwidth with gain provided at the input is typically 200Hz. But with gain provided only at the output, the full power bandwidth approaches the small signal bandwidth.

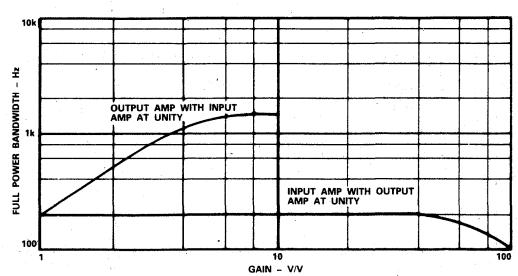


Figure 10. Typical AD293/AD294 - Full Power Bandwidth vs. Gain

Gain Nonlinearity vs. Output Swing

The gain nonlinearity vs. output swing, for the AD293/AD294, is illustrated in Figure 11. As shown, increasing either the input gain or the output swing will cause the gain nonlinearity to increase if the output gain is held to 1V/V.

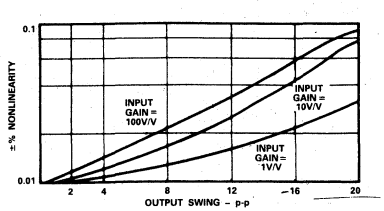


Figure 11. Typical AD293/AD294 - Gain Nonlinearity vs. Output Swing

OPTIMIZING THE AD293/AD294

The AD293/AD294 can be optimized for many applications as shown by the performance charts on the previous page. Gain and filtering can be implemented on both the input and output stages while providing true galvanic isolation. Provisions for an additional two poles of filtration are also available without the addition of external operational amplifiers. Due to their low power consumption and novel transformer design, the beat frequency problem normally associated with adjacent isolation amplifiers is eliminated. A sync terminal is provided for applications where ultra-sensitive circuitry might interpret the isolator carrier frequency.

SELECTING GAIN

The AD293/AD294 contain both input and output amplifiers (see Figures 1 and 2), the gains of which can be set independently. The selection of a particular combination tailors isolator properties to the application, minimizes errors, and optimizes frequency response.

Nonlinearity is the deviation of response from a straight line. This error arises from slight differences in responses of the input demodulator I and demodulator II, their respective transformer windings responses, and rectification of carrier signal in the input stage due to large signal amplitudes in this section. Hence, linearity is best obtained by raising output gain and lowering input gain.

Gain errors are deviations in slope from the predicted gain equation. Gain errors are attributable to the difference in gain between demodulators I and II. These errors are quite small, due to the highly predictable and uniform nature of the thick-film transformer. The gain drift of this portion of gain error is also small. Since this gain error source dominates at unity gain, the unity gain temperature coefficients of these units is very small. As input gain is taken, errors arise due to the inaccuracies of the internal feedback resistor R1, and user selected R_G. Failure of these resistors to temperature track introduces a gain TC. R1 is trimmed within ±3% and has a TC of ±100ppm/°C. Since the temperature coefficient of R1 is not user controllable, best gain TC at low gains is favored by taking output gain. The output stage also contributes gain error only when gain is taken. Here, both the feedback and gain resistors are user supplied and can be made as accurate as desired.

Offset errors are apparent both in the input stage and in the transformer-output stage combination. Provisions are available to eliminate these initial offset errors at both the input and output stages through trim potentiometers. These errors also have temperature dependence where at unity gain, output offset drift dominates. Taking output gain multiplies output drift by the gain taken. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized.

Errors due to small signal and large signal bandwidth limitations can also be optimized in the AD293/AD294. Small signal bandwidth is limited by lack of gain as frequency is raised, a condition caused by the necessity to limit bandwidth internally to preserve stability in the A1, modulator, input demodulator loop. The input stage contains most of the small signal bandwidth limitations thus, taking input gain limits small signal bandwidth (see Figure 10). The demodulators limit slew rate and large signal bandwidth. Apparent slew rate at the isolator output is

multiplied by gain taken in the output stage. With maximum gain taken in the output stage, large signal bandwidth for moderate swings approaches small signal bandwidth (shown in Figure 10). Thus applying input gain limits bandwidth while output gain enhances it.

FILTERING

With the AD293/AD294, the addition of filtering can be implemented in a number of different configurations without the use of external operational amplifiers. Capacitors can be placed in series with the input or output terminals or configured in combination with the gain setting resistors to tailor performance. An input filter terminal and an output filter terminal are provided for user selectable filtration. Characteristics are determined by the formulas shown in Figure 1.

REDUCING NORMAL-MODE VOLTAGE

A prime isolator function is the rejection of common-mode signals. The extremely high input to output resistance of isolators allows excellent rejection of dc common-mode voltages. As frequency rises, the small capacitance across the isolation barrier causes an ac common-mode current to flow through that barrier, which is proportional to applied common-mode voltage, frequency and barrier capacitance. Since the isolation mechanism (transformer T1) is more initimately connected to the input low terminal than the input high terminal, the bulk of common-mode current flows through the input low terminal. Any resistance in series with the input source and the input low terminal then develops a normal-mode voltage, which may constitute objectionable interference.

An isolator cannot separate normal-mode interference from the desired signal without help, but interference can be rejected in several ways.

Conversion of common-mode current to normal-mode voltage can be reduced by minimizing resistance in the input low lead. In the AD293/AD294 CMR is enhanced and input trimming sacrificed by returning the input signal to pin 2. With known stable source resistances common-mode current to normal-mode voltage conversion can also be cancelled as shown in Figure 13.

ISOLATED INDUSTRIAL APPLICATIONS

As illustrated in Figure 14, the AD293 can be applied where differential signal sources are used such as an isolated strain gauge. With a third wire connected to the common-mode potential of that source, a common-mode current is forced to flow through the third wire and through the isolation barrier; thus, sparing the differential input wires the necessity of conducting the common-mode current. In this manner, the isolator is responsive to only the differential inputs while ignoring the passage of common-mode currents. Input gain is selected via R_G and determined by the input gain formula.

MEDICAL APPLICATIONS

In medical applications, a good connection to the patient, even on the third wire cannot be guaranteed due to electrode resistance to and through the skin. Illustrated in Figure 12 is a medical front end with right leg drive powered by the AD294A. Here the common-mode drive amplifier helps force common-mode current to flow in the third wire in preference to the differential input wires. The FET input has low noise current to avoid development of voltage noise in the input protection resistors. These resistors protect the input from defibrillator pulses with the AD294A having the capability of withstanding an 8kV pulse. The patient is also protected from fault currents due to input component failure. It is necessary to connect the third wire to establish the input common-mode level. If not connected the input common-mode level, with respect to common of the input section power supplies, will cause the isolator to drift out of its linear range. Layout is also very important, both for common-mode rejection and isolation.

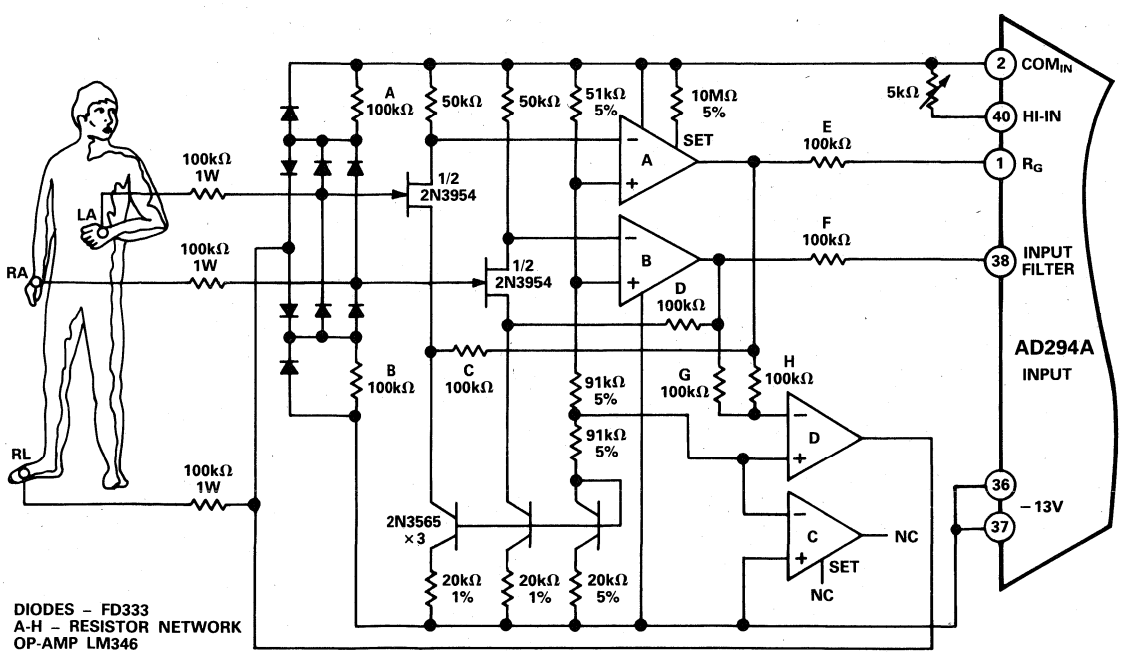


Figure 12. Multilead Medical Application Using the AD294A with Right Leg Drive

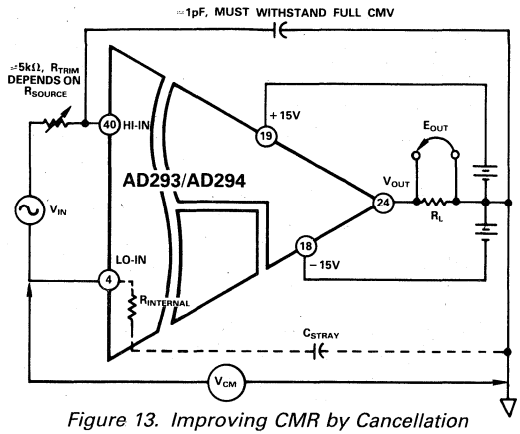


Figure 13. Improving CMR by Cancellation

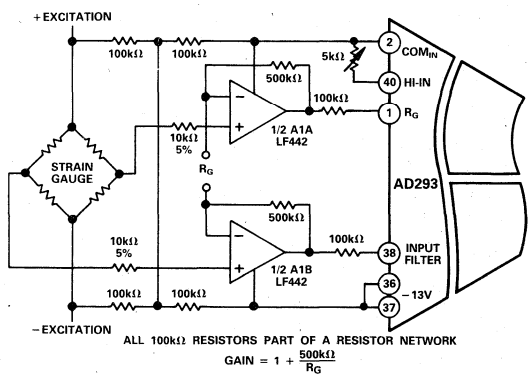


Figure 14. Isolated Strain Gauge Using Front End of AD293

CURRENT LOOP INTERFACE

Illustrated in Figure 15, the AD293 provides an isolated sensor interface that is compatible with standard 4-to-20mA current loops. Here high common-mode rejection and high common-mode voltage suppression are easily attained with the AD293. The AD293 conditions the 0V to 10V input signal and provides a proportional voltage at the isolator's output. Then the circuitry shown converts it into a 4 to 20mA current, which in turn, may be applied to the loop load R_L.

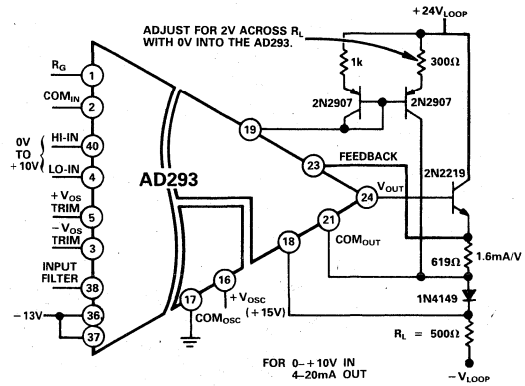


Figure 15. Isolated Current Loop Interface

TEMPERATURE MEASUREMENT AND COLD JUNCTION COMPENSATION

Illustrated in Figure 16, the AD293 can be used for isolated temperature measurements while providing cold junction compensation. With the circuitry connected as shown, the LM334 must be thermally connected to the cold junction terminal for an accurate temperature measurement to be made of this terminal. In this configuration, accurate temperature measurements using the industry's popular J type thermocouple can be made. For example, assume 1V out of the AD293 at 100°C. From the ANSI tables, the output voltage of a J thermocouple at 100°C is 0.005268V. Set the gain of the AD293 at 1V/0.005268V = 189.8, R_G = 530Ω. With the thermocouple junction open, set the voltage between points A and B to 0.015V by adjusting the 500Ω pot. Connect a voltage reference source in place of the thermocouple. Set its output to zero. Set the output of the AD293 to zero by adjusting the 100Ω pot. Set the reference source to 0.005268V. The output of the AD293 should read 1V.

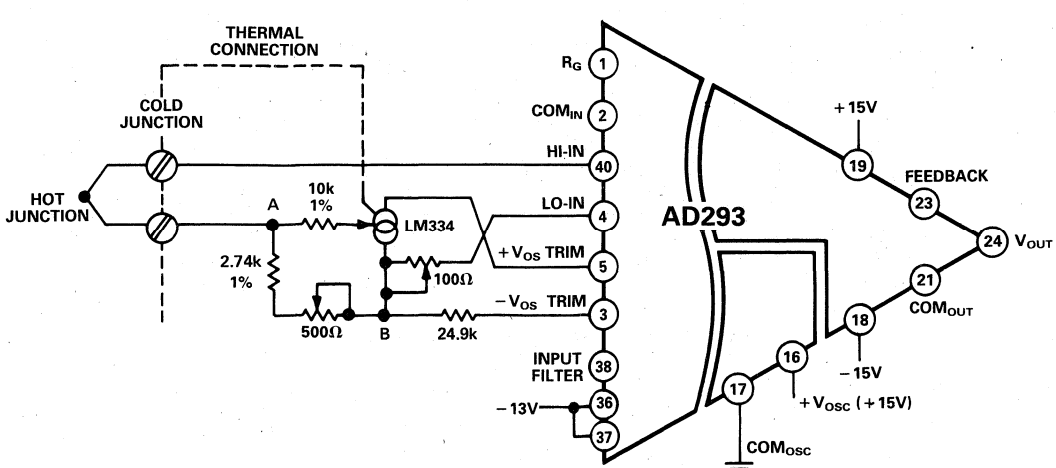


Figure 16. Temperature Measurement & Cold Junction Compensation

DRIVING CAPACITIVE LOADS

For driving capactive loads greater than 1000pF, compensation should be implemented as shown in Figure 17. Here a 100pF capacitor and 100Ω resistor are used to insure that the AD293 output stage remains stable. These components can also be changed to tailor frequency response to the particular application. The 100Ω resistor isolates the output of the AD293 while the 100pF provides response lead.

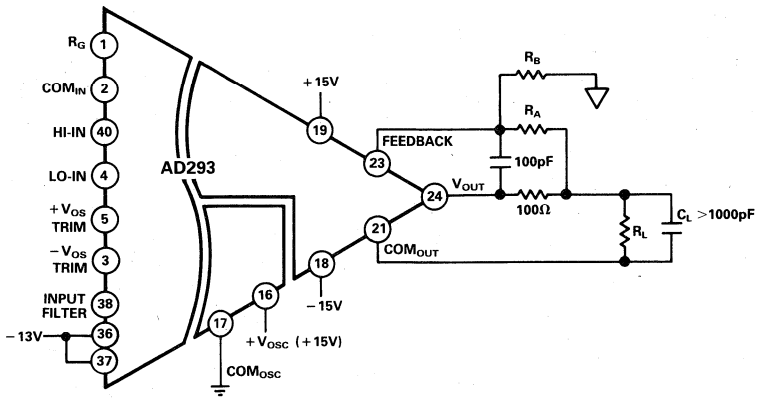


Figure 17. Driving Capacitive Loads

INCREASING OUTPUT DRIVE CAPABILITY

For applications requiring increased output drive, Figure 18 illustrates a single solution. Here the output voltage of the AD293 is conditioned and applied to the drive circuitry. R_A will supply the output stage with unity gain as connected. For gain to be added to the output stage, connect R_B as shown. Output gain will be determined by the output equation previously stated in the specifications. For output gain >1V/V, C_O should also be implemented so output stability will be insured. With this output drive circuitry, 200Ω loads can be easily driven with ±10V @ 50mA.

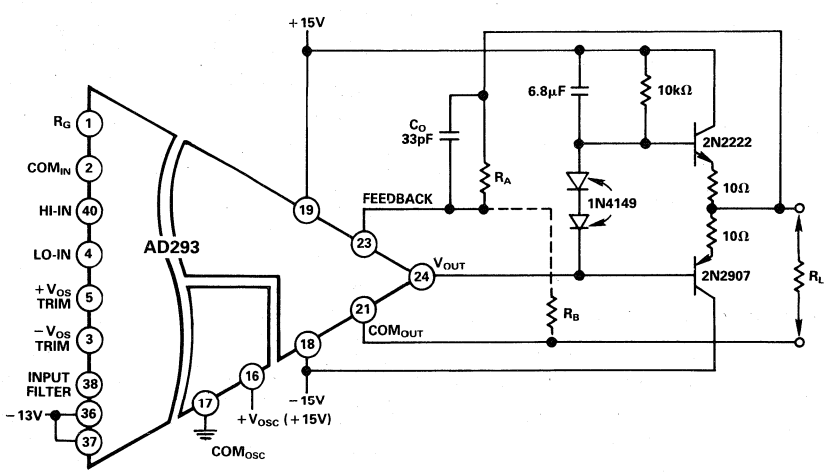


Figure 18. Increasing Output Drive Capability

ANALOG DEVICES

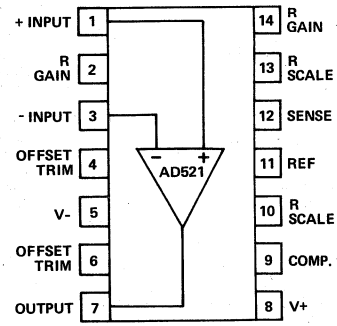
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

Programmable Gains from 0.1 to 1000
Differential Inputs
High CMRR: 110dB min
Low Drift: 2μV/°C max (L)
Complete Input Protection, Power ON and Power OFF
Functionally Complete with the Addition of Two Resistors
Internally Compensated
Gain Bandwidth Product: 40MHz
Output Current Limited: 25mA
Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000

AD521 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9 \Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	*	*	*
Equation	$G = R_S/R_G V/V$	*	*	*
Error from Equation	(±0.25–0.004G)%	*	*	*
Nonlinearity (Note 2)				
1≤G≤1000	0.2% max	*	0.1% max	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, ±10mA min	*	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*	*
Impedance	0.1Ω	*	*	*
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	>2MHz	*	*	*
G = 10	300kHz	*	*	*
G = 100	200kHz	*	*	*
G = 1000	40kHz	*	*	*
Small Signal, ±1.0% Flatness				
G = 1	75kHz	*	*	*
G = 10	26kHz	*	*	*
G = 100	24kHz	*	*	*
G = 1000	6kHz	*	*	*
Full Peak Response (Note 3)	100kHz	*	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*	*
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7μs	*	*	*
G = 10	5μs	*	*	*
G = 100	10μs	*	*	*
G = 1000	35μs	*	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)				
G = 1000	50μs	*	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10μs	*	*	*
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	2μV/°C max	**
vs. Supply	3μV/%	*	*	*
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	75μV/°C max	**
vs. Supply (Note 6)	$0.005V_{OS_O}$/%	*	*	*
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	*	*	*
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	*	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	*	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\,\mu V$	*	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\,\mu V$	*	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*	*
REFERENCE TERMINAL				
Bias Current	3μA	*	*	*
Input Resistance	10MΩ	*	*	*
Voltage Range	±10V	*	*	*
Gain to Output	1	*	*	*
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	*	*	*
Quiescent Supply Current	5mA max	*	*	*
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	*	*	–55°C to +125°C
Operating	–25°C to +85°C	*	*	–55°C to +125°C
Storage	–65°C to +150°C	*	*	*
PACKAGE OPTION[1]: TO-116 Style (D14A)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES
[1] See Section 19 for package outline information.
*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10μs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10μs pulse at a 1kHz rate. (When a common mode signal greater than V_S −0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when $V_S = 0$) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 2 of 3 separate 10 second periods with the test circuit of Figure 8.

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

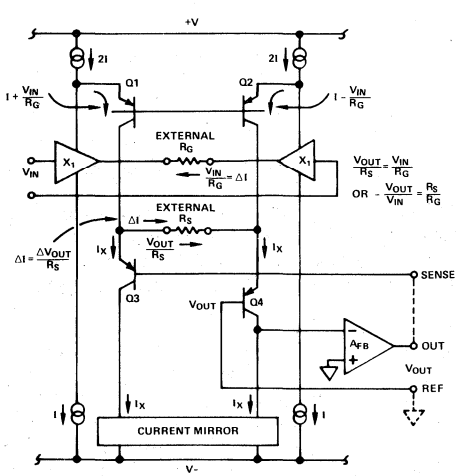


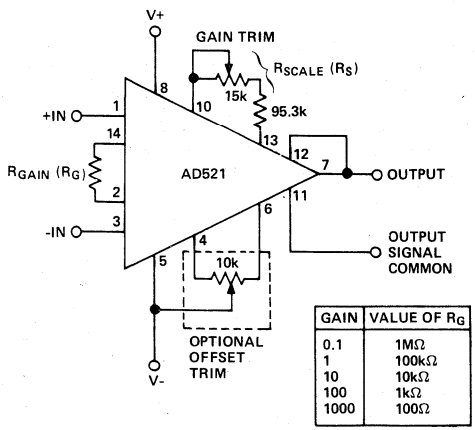
Figure 1. Simplified AD521 Schematic

APPLICATION NOTES FOR THE AD521

These notes ensure the AD521 will achieve the high level of performance necessary for many diversified IA applications.

1. Gains below 1 and above 1000 are realized by adjusting the gain setting resistors as shown in Figure 2 (the resistor, R_S between pins 10 and 13 should remain 100kΩ ±15%, see application note 3). For best results, the input voltage should be restricted to ±10V especially for gain equal to or less than 1.

2. Provide a return path to ground for input bias currents. The AD521 is an instrumentation amplifier, not an isolation amplifier. When using a thermocouple or other "floating" source, this return path may be provided directly to ground or indirectly through a resistor to ground from pins 1 and/or 3, as shown in Figure 3. If the return path is not provided, bias currents will cause the output to saturate. The value of the resistor may be determined by dividing the maximum allowable common mode voltage for the application by the bias current of the instrumentation amplifier.

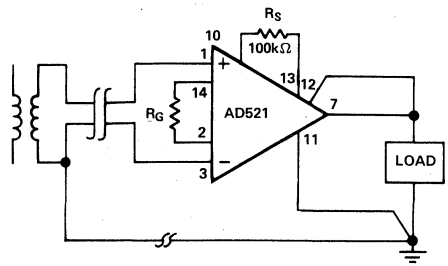


GAIN	VALUE OF R_G
0.1	1MΩ
1	100kΩ
10	10kΩ
100	1kΩ
1000	100Ω

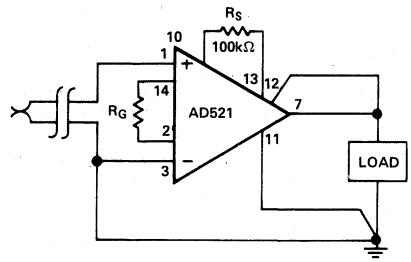
Figure 2. Operating Connections for AD521

3. The resistors between pins 10 and 13, (R_{SCALE}) must equal 100kΩ ±15% (Figure 2). If R_{SCALE} is too low (below 85kΩ) the output swing of the AD521 is reduced. At values below 80kΩ and above 120kΩ the stability of the AD521 may be impaired.

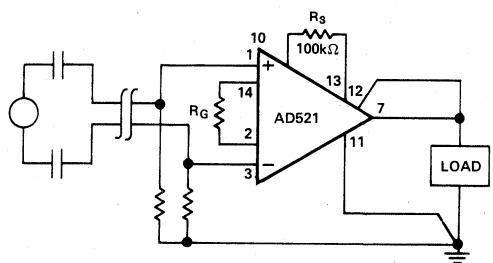
4. Do not exceed the allowable input signal range. The linearity of the AD521 decreases if the inputs are driven within 5 volts of the supply rails, particularly when the device is used at a gain less than 1. To avoid this possibility, attenuate the input signal through a resistive divider network and use the AD521 as a buffer, as shown in Figure 4. The resistor R/2 matches the impedance seen by both AD521 inputs so that the voltage offset caused by bias currents will be minimized.



a). Transformer Coupled, Direct Return

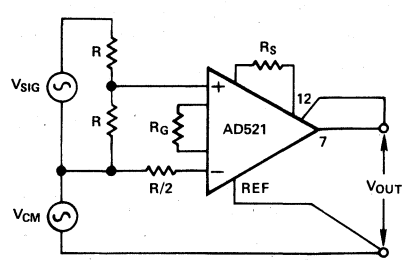


b). Thermocouple, Direct Return



c). AC Coupled, Indirect Return

Figure 3. Ground Returns for "Floating" Transducers



1. INCREASE R_G TO PICK UP GAIN LOST BY R DIVIDER NETWORK
2. INPUT SIGNAL MUST BE REDUCED IN PROPORTION TO POWER SUPPLY VOLTAGE LEVEL

Figure 4. Operating Conditions for $V_{IN} \approx V_S = 10V$

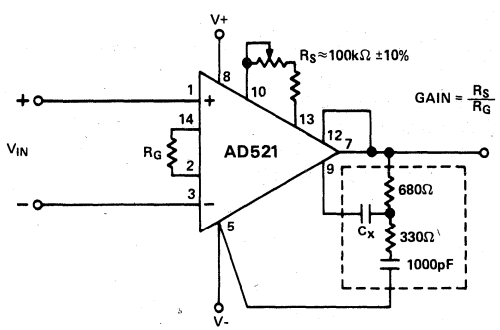
5. Use the compensation pin (pin 9) and the applicable compensation circuit when the amplifier is required to drive a capacitive load. It is worth mentioning that coaxial cables can "invisibly" provide such capacitance since many popular coaxial cables display capacitance in the vicinity of 30pF per foot.

This compensation (bandwidth control) feature permits the user to fit the response of the AD521 to the particular application as illustrated by Figure 5. In cases of extremely high load capacitance the compensation circuit may be changed as follows:

1. Reduce 680Ω to 24Ω
2. Reduce 330Ω to 7.5Ω
3. Increase 1000pF to 0.1μF
4. Set C_X to 1000pF if no compensation was originally used. Otherwise, do not alter the original value.

This allows stable operation for load capacitances up to 3000pF, but limits the slew rate to approximately 0.16V/μs.

6. Signals having frequency components above the Instrumentation Amplifier's output amplifier closed-loop bandwidth will be transmitted from V- to the output with little or no attenuation. Therefore, it is advisable to decouple the V- supply line to the output common or to pin 11.[1]



$$C_X = \frac{1}{100\pi f_t} \text{ when } f_t \text{ is the desired bandwidth.}$$

(f_t in kHz, C_X in μF)

Figure 5. Optional Compensation Circuit

INPUT OFFSET AND OUTPUT OFFSET

When specifying offsets and other errors in an operational amplifier, it is often convenient to refer these errors to the inputs. This enables the user to calculate the maximum error he would see at the output with any gain or circuit configuration. An op amp with 1mV of input offset voltage, for example, would produce 1V of offset at the output in a gain of 1000 configuration.

In the case of an instrumentation amplifier, where the gain is controlled in the amplifier, it is more convenient to separate errors into two categories. Those errors which simply add to the output signal and are unaffected by the gain can be classified as output errors. Those which act as if they are associated with the input signal, such that their effect at the output is proportional to the gain, can be classified as input errors.

As an illustration, a typical AD521 might have a +30mV output offset and a -0.7mV input offset. In a unity gain configuration, the *total* output offset would be +29.3mV or the sum of the two. At a gain of 100, the output offset would be -40mV or: 30mV + 100(-0.7mV) = -40mV.

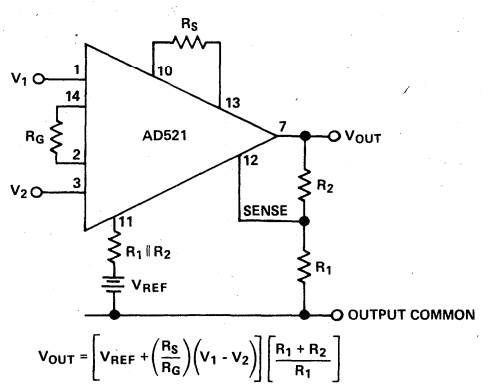
By separating these errors, one can evaluate the total error independent of the gain settings used, similar to the situation with the input offset specifications on an op amp. In a given gain configuration, both errors can be combined to give a total error *referred to the input* (R.T.I.) or *output* (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain x input error) + output error

The offset trim adjustment (pins 4 and 6, Figure 2) is associated primarily with the output offset. At any gain it can be used to introduce an output offset equal and opposite to the input offset voltage multiplied by the gain. As a result, the total output offset can be reduced to zero.

As shown in Figure 6, the gain range on the AD521 can be extended considerably by adding an attenuator in the sense terminal feedback path (as well as adjusting the ratio, R_S/R_G). Since the sense terminal is the inverting input to the output amplifier, the additional gain to the output is controlled by R_1 and R_2. This gain factor is $1 + R_2/R_1$.



$$V_{OUT} = \left[V_{REF} + \left(\frac{R_S}{R_G}\right)(V_1 - V_2)\right]\left[\frac{R_1 + R_2}{R_1}\right]$$

Figure 6. Circuit for utilizing some of the unique features of the AD521. Note that gain changes introduced by changing R1 and R2 will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

[1] For further details, refer to "An I.C. User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by A. Paul Brokaw. This application note is available from Analog Devices without charge upon request.

Where offset errors are critical, a resistor equal to the parallel combination of R_1 and R_2 should be placed between pin 11 and V_{REF}. This minimizes the offset errors resulting from the input current flowing in R_1 and R_2 at the sense terminal. Note that gain changes introduced by changing the R_1/R_2 attenuator will have a minimum effect on output offset if the offset is carefully nulled at the highest gain setting.

When a predetermined output offset is desired, V_{REF} can be placed in series with pin 11. This offset is then multiplied by the gain factor $1 + R_2/R_1$ as shown in the equation of Figure 6.

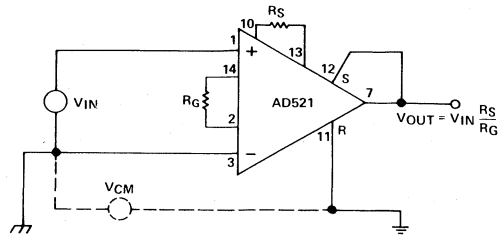


Figure 7. Ground loop elimination. The reference input, Pin 11, allows remote referencing of ground potential. Differences in ground potentials are attenuated by the high CMRR of the AD521.

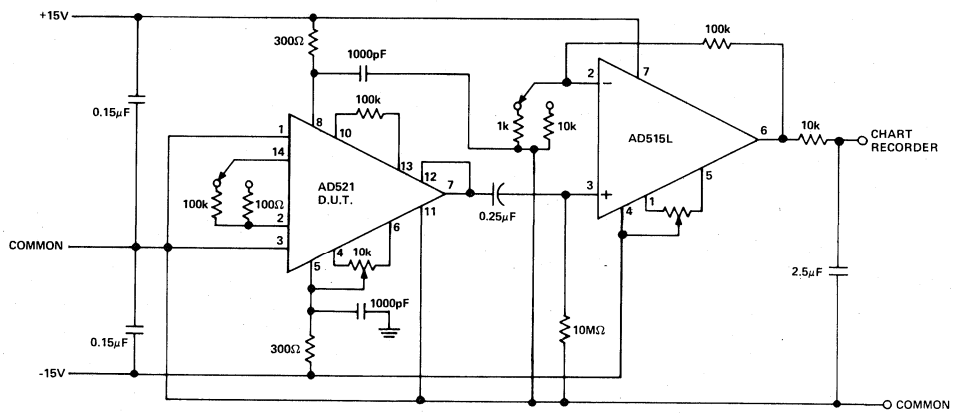


Figure 8. Test circuit for measuring peak to peak noise in the bandwidth 0.1Hz to 10Hz. Typical measurements are found by reading the maximum peak to peak voltage noise of the device under test (D.U.T.) for 3 observation periods of 10 seconds each.

ANALOG DEVICES

High Accuracy Data Acquisition Instrumentation Amplifier

AD522

FEATURES

Performance

- Low Drift: 2.0μV/°C (AD522B)
- Low Nonlinearity: 0.005% (G = 100)
- High CMRR: >110dB (G = 1000)
- Low Noise: 1.5μV p-p (0.1 to 100Hz)
- Low Initial V_{OS}: 100μV (AD522B)

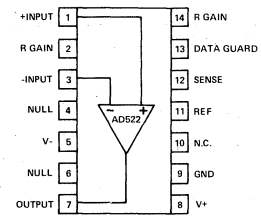
Versatility

- Single-Resistor Gain Programmable: $1 \leqslant G \leqslant 1000$
- Output Reference and Sense Terminals
- Data Guard for Improving ac CMR

Value

- Internally Compensated
- No External Components except Gain Resistor
- Active Trimmed Offset, Gain, and CMR

AD522 FUNCTIONAL BLOCK DIAGRAM



14-PIN DIP

PRODUCT DESCRIPTION

The AD522 is a precision IC instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low voltage drift, and low noise makes the AD522 suitable for use in many 12-bit data acquisition systems.

An instrumentation amplifier is usually employed as a bridge amplifier for resistance transducers (thermistors, strain gauges, etc.) found in process control, instrumentation, data processing, and medical testing. The operating environment is frequently characterized by low signal-to-noise levels, fluctuating temperatures, unbalanced input impedances, and remote location which hinders recalibration.

The AD522 was designed to provide highly accurate signal conditioning under these severe conditions. It provides output offset voltage drift of less than 10μV/°C, input offset voltage drift of less than 2.0μV/°C, CMR above 80dB at unity gain (110dB at G = 1000), maximum gain nonlinearity of 0.001% at G = 1, and typical input impedance of $10^9\Omega$.

This excellent performance is achieved by combining a proven circuit configuration with state-of-the-art manufacturing technology which utilizes active laser trimming of tight-tolerance thin-film resistors to achieve low cost, small size and high reliability. This combination of high value with no-compromise performance gives the AD522 the best features of both monolithic and modular instrumentation amplifiers, thus providing extremely cost-effective precision low-level amplification.

The AD522 is available in three versions with differing accuracies and operating temperature ranges; the "A", and "B" are specified from -25°C to +85°C, and the "S" is guaranteed over the extended aerospace temperature range of -55°C to +125°C. All versions are packaged in a 14-pin DIP and are supplied in a pin configuration similar to that of the popular AD521 instrumentation amplifier.

SPECIFICATIONS[1] (typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25°C$ unless otherwise specified)

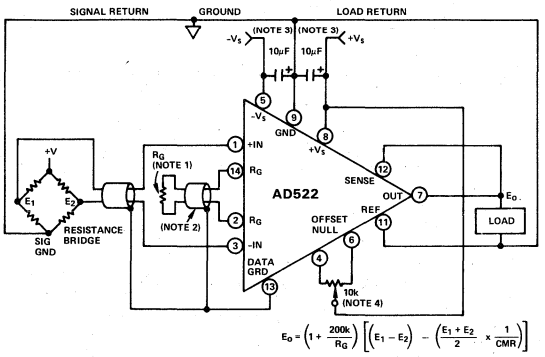
MODEL	AD522AD	AD522BD	AD522SD
GAIN			
Gain Equation	$1 + \frac{2\ (10^5)}{R_g}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max (see Fig. 4)			
G = 1	0.005%	0.001%	**
G = 1000	0.01%	0.005%	**
vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA	*	*
DYNAMIC RESPONSE (see Fig. 6)			
Small Signal (-3dB)			
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adjustable to zero)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max (see Fig. 3)			
G = 1	±50μV/°C (±10μV/°C typ)	±25μV/°C (±5μV/°C typ)	±100μV/°C (±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
$1 < G < 1000$	$\pm(\frac{50}{G} + 6)\mu V/°C$	$\pm(\frac{25}{G} + 2)\mu V/°C$	$\pm(\frac{100}{G} + 6)\mu V/°C$
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	*	*
vs. Temperature	±100pA/°C	*	*
Input Offset Current			
Initial max, +25°C	±20nA	*	*
vs. Temperature	±100pA/°C	*	*
INPUT			
Input Impedance			
Differential	$10^9\Omega$	*	*
Common Mode	$10^9\Omega$	*	*
Input Voltage Range			
Maximum Differential Input, Linear	±10V	*	*
Maximum Differential Input, Safe	±20V	*	*
Maximum Common Mode, Linear	±10V	*	*
Maximum Common Mode Input, Safe	±15V	*	*
Common Mode Rjection Ratio, Min @ ±10V, 1kΩ Source Imbalance (see Fig. 5)			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI (see Fig. 4)			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	**
PACKAGE OPTION[2]	Ceramic[3] – HY14A	Ceramic[3] – HY14A	Metal – HY14D

NOTES
[1] Specifications guaranteed after 10 minute warm-up.
[2] See Section 19 for package outline information.
[3] Analog Devices reserves the right to ship metal packages in lieu of the standard ceramic packages for A and B grades.

*Specifications same as AD522A.
**Specifications same as AD522B.
Specifications subject to change without notice.

GENERAL APPLICATION CONSIDERATIONS

Figure 1 illustrates the AD522 wiring configuration when used in a typical bridge amplifier application. In any low-level, high impedance, noise-dominated environment, proper shielding and grounding are requisite for optimum performance; a recommended technique is shown.



NOTES:
1. GAIN RESISTOR R_G SHOULD BE <5ppm/°C (VISHAY TYPE RECOMMENDED).
2. SHIELDED CONNECTIONS TO R_G RECOMMENDED WHEN MAXIMUM SYSTEM BANDWIDTH AND AC CMR IS REQUIRED, AND WHEN R_G IS LOCATED MORE THAN SIX INCHES FROM AD522. NO INSTABILITIES ARE CAUSED BY REMOTE R_G LOCATIONS. WHEN NOT USED, THE DATA GUARD PIN CAN BE LEFT UNCONNECTED.
3. POWER SUPPLY FILTERS ARE RECOMMENDED FOR MINIMUM NOISE IN NOISY ENVIRONMENTS.
4. NO TRIM REQUIRED FOR MOST APPLICATIONS. IF REQUIRED, A 10kΩ, 25ppm/°C, 25 TURN TRIM POT (SUCH AS VISHAY 1202-Y-10k) IS RECOMMENDED.

Figure 1. Typical Bridge Application

Direct coupling of the AD522 inputs makes it necessary to provide a signal ground return for input amplifier bias currents. This can be achieved by direct connection as shown, or through an indirect path of less than 1MΩ resistance such as other system interconnections.

To minimize noise, shielding should be provided for the input leads and gain resistor connections. A passive data guard is provided to improve ac common mode rejection by "bootstrapping" the capacitance of the input cabling, thus minimizing differential phase shift. This will also reduce degradation of system bandwidth.

Balanced design eliminates the need for external bypass capacitors for most applications. If, however, the power supplies are remotely located (farther than 10 feet or so) or if they are likely to carry more than a few millivolts of noise, local filtering will enable the user to retain optimal performance.

Reference and sense pins are provided to permit remote load sensing. These points can also be used to trim the device CMR, add an output booster, or to offset the output to a reference level. These applications are illustrated in following sections.

It is good practice to place R_G within several inches of the AD522. Longer leads will increase stray capacitance and cause phase shifts that will degrade CMR at higher frequencies. For frequencies below 10Hz, a remote R_G is generally acceptable; no stability problems are caused. Bear in mind that a leakage impedance of 200MΩ between R_G pins will cause an 0.1% gain error at G = 1. Unity gain is not trimmable.

5

TYPICAL APPLICATION AND ERROR BUDGET ANALYSIS (See Figure 1 and Table I)

A floating transducer with a 0 to 1 volt output has a 1kΩ source imbalance. A noisy environment induces a one volt 0 to 60Hz common mode signal in the ground return. This signal must be amplified to interface with a data acquisition system calibrated for a 0 to 10 volt signal range. The operating temperature range is 0 to +50°C and an AD522B is to be used. Table 1 lists error sources and their effect on system accuracy.

The total effect on absolute accuracy is less than ±0.2%, allowing adjustment-free 8-bit operation. In computer or microprocessor controlled data-acquisition systems, automatic recalibration can nullify gain and offset drifts leaving noise, distortion and CMR as the only error sources. In this case, full 12-bit operation is achieved.

Gain Errors: Absolute gain errors can be nulled by trimming R_G. Gain drift is a linear effect, not detrimental to resolution and is caused by the change in value of internal resistors over the operating temperature range. An "intelligent" system can correct for these errors with an automatic calibration cycle. Gain nonlinearity never exceeds 0.002% at G = 10.

Offset Drift & Pins Current Errors: Special care has been taken in the design of the AD522 input stage to minimize offset drift. Unless transducer impedances are unbalanced by more than 2kΩ, errors caused by offset current drift are negligible compared to offset voltage drift. Although initial offset voltages are laser-nulled for most applications, provisions have been made to allow further adjustment to correct for initial system offset. In this example, all offset drifts amount to ±0.014% and do not effect resolution (can be corrected with an automatic calibration cycle).

CMR and Noise Errors: Common mode rejection and noise performance of instrumentation amplifiers are critical because

Error Source	Specification	Effect on Absolute Accuracy, % of F.S.	Effect on Resolution % of F.S.
Gain Nonlinearity	±0.002% max, G = 10 (from Spec. Sheet and Fig. 4)	±0.002	±0.002
Voltage Drift	$\frac{25\mu V/^\circ C}{Gain} + 2.0\mu V/^\circ C = 4.5\mu V/^\circ C$ R.T.I. = 0.00055%/°C (from Spec. Sheet)	±0.011	---
CMR	86dB (from Spec. Sheet, CMR vs. F vs. G, typical curve)	±0.005	±0.005
Noise, R.T.O. (0.1 to 100Hz)	15μV (p-p) R.T.O. (from Spec. Sheet, Noise vs. G typical curve)	±0.0015	±0.0015
Offset Current Drift	±50pA/°C x 1k source imbalance (Spec. Sheet) = ±50μV/°C = ±1.25μV R.T.I.	±0.000125	---
Gain Drift (add 10ppm/°C for external R_G)	60ppm/°C (Spec. Sheet)	±0.15	---

Table I. Error Sources

these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

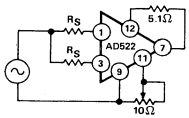


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

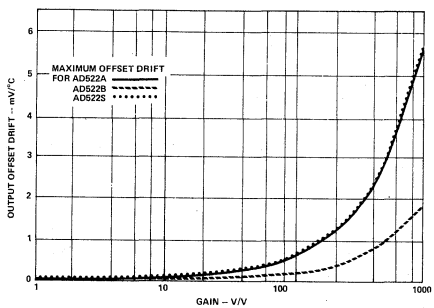


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

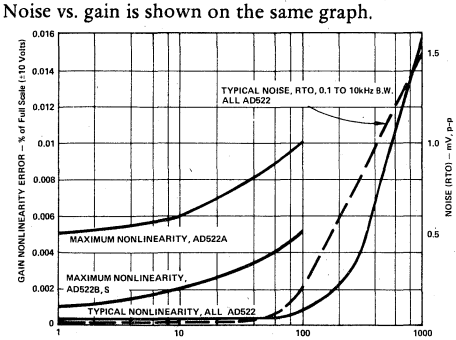


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

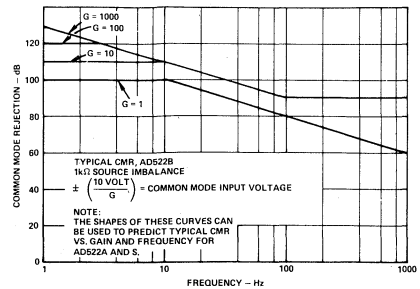


Figure 5. Common Mode Rejection vs. Frequency and Gain

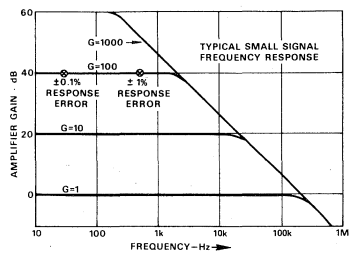


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

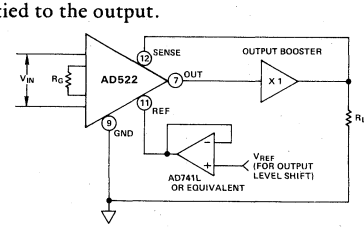


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

ANALOG DEVICES

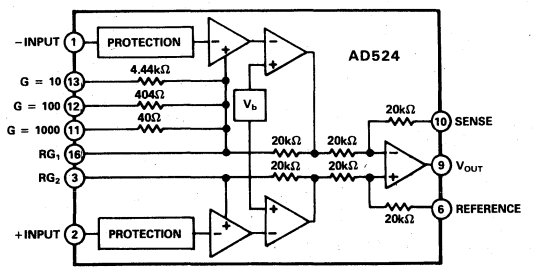
Precision Instrumentation Amplifier

AD524

FEATURES

Low Noise: 0.3μV p-p 0.1Hz to 10Hz
Low Nonlinearity: 0.003% (G = 1)
High CMRR: 120dB (G = 1000)
Low Offset Voltage: 50μV
Low Offset Voltage Drift: 0.5μV/°C
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 10, 100, 1000
Input Protection, Power On – Power Off
No External Components Required
Internally Compensated

AD524 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 10			±0.25			±0.15			±0.1%			±0.25	%
G = 100			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±2.0			±1.0			±0.5			±2.0	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10, 100			±0.01			±0.005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0.01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			250			100			50			100	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	µV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 10	85			95			100			95			dB
G = 100	95			105			110			105			dB
G = 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		±10			±10			±10			±10		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 10	90			95			100			90			dB
G = 100	100			105			110			100			dB
G = 1000	110			115			120			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz

Model	AD524A			AD524B			AD524C			AD524S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate		5.0			5.0			5.0			5.0		V/μs
Settling Time to 0.01%, 20V Step													
G = 1 to 100		15			15			15			15		μs
G = 1000		75			75			75			75		μs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		7			7			7			7		nV/$\sqrt{Hz}$
R.T.O.		90			90			90			90		nV/$\sqrt{Hz}$
R.T.I., 0.1 to 10Hz													
G = 1		15			15			15			15		μV p-p
G = 10		2			2			2			2		μV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			± 10			± 10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	**±6**	±15	**±18**	V
Quiescent Current		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**		3.5	**5.0**	mA
PACKAGE[1]	D16A			D16A			D16A			D16A			

NOTES

[1]See Section 19 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

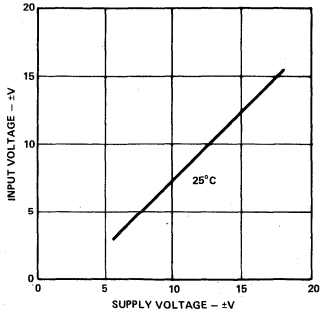


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

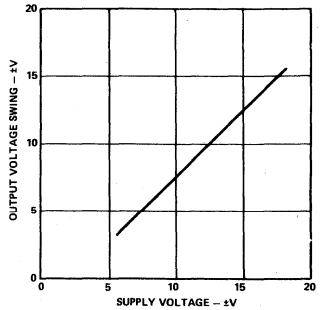


Figure 2. Output Voltage Swing vs. Supply Voltage

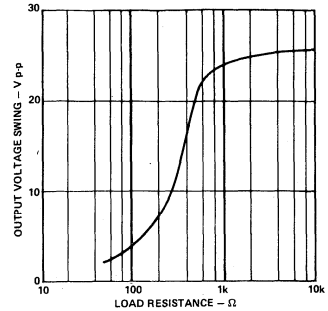


Figure 3. Output Voltage Swing vs. Resistive Load

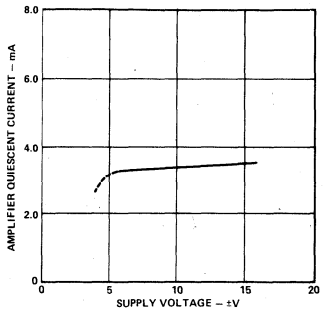


Figure 4. Quiescent Current vs. Supply Voltage

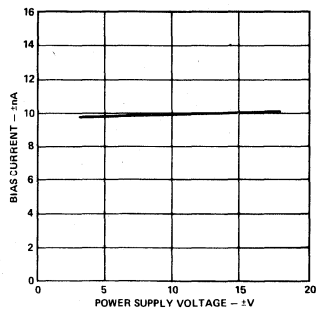


Figure 5. Input Bias Current vs. Supply Voltage

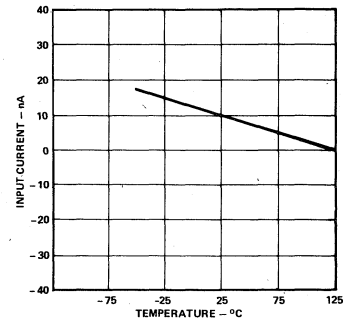


Figure 6. Input Bias Current vs. Temperature

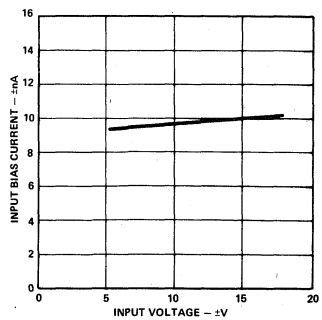


Figure 7. Input Bias Current vs. CMV

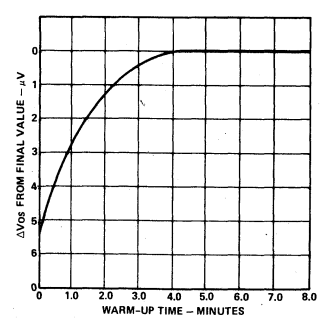


Figure 8. Offset Voltage, RTI, Turn on Drift, G = 1000

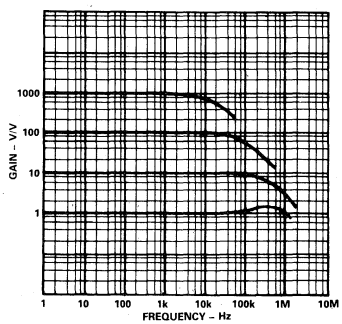


Figure 9. Gain vs. Frequency

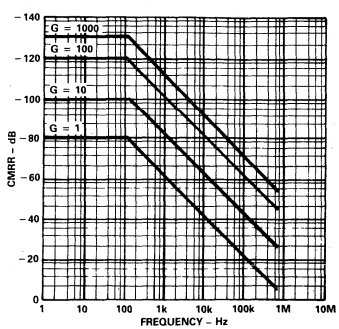


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

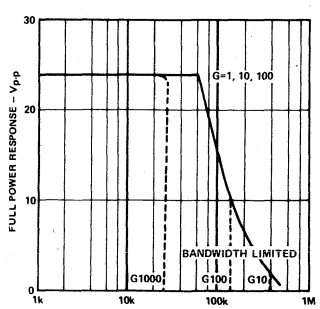


Figure 11. Large Signal Frequency Response

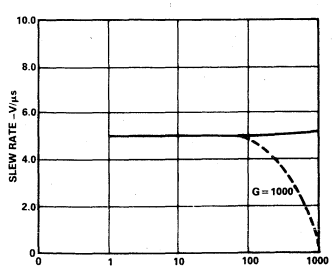


Figure 12. Slew Rate vs. Gain

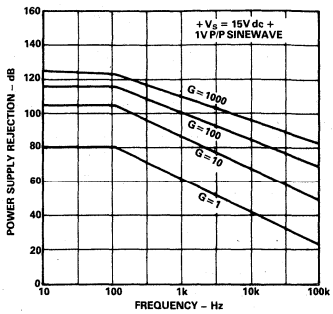


Figure 13. Positive PSRR vs. Frequency

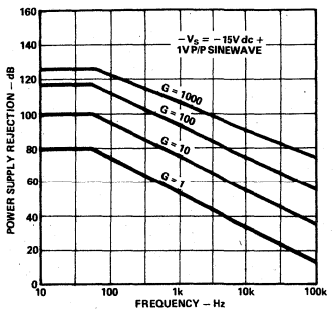


Figure 14. Negative PSRR vs. Frequency

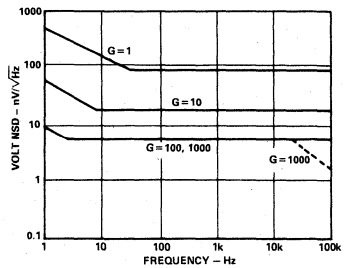


Figure 15. RTI Noise Spectral Density vs. Gain

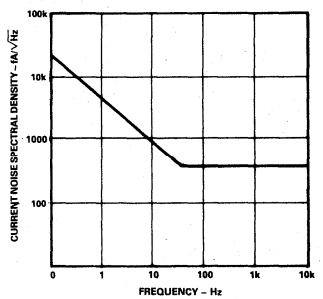


Figure 16. Input Current

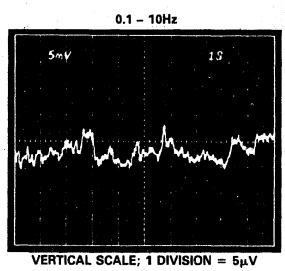


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

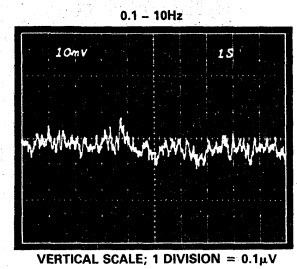


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

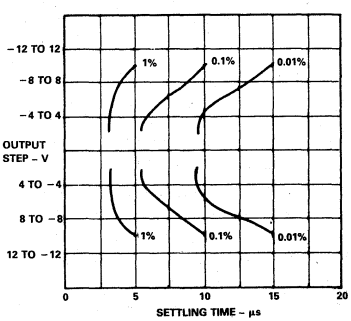


Figure 19. Settling Time Gain = 1

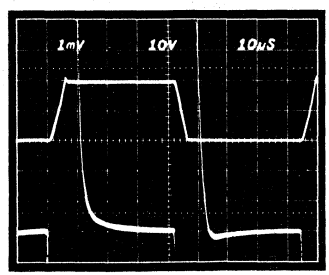


Figure 20. Large Signal Pulse Response and Settling Time – G = 1

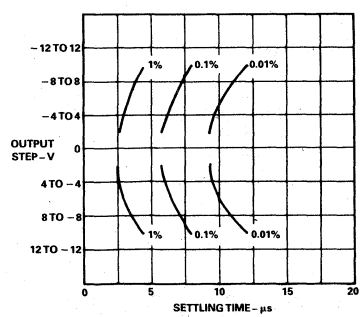


Figure 21. Settling Time Gain = 10

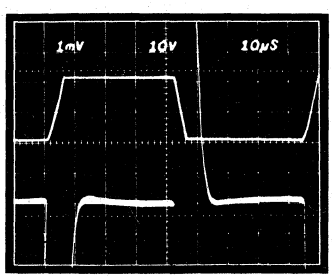


Figure 22. Large Signal Pulse Response and Settling Time G = 10

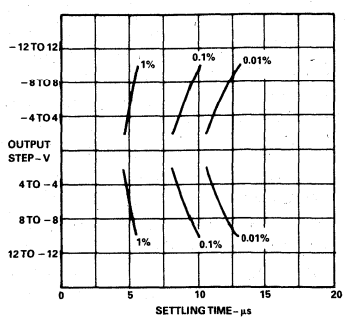


Figure 23. Settling Time Gain = 100

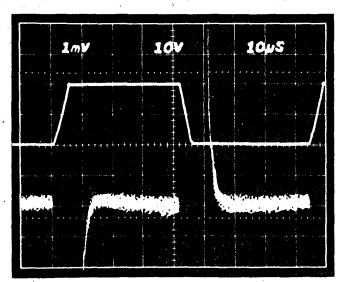


Figure 24. Range Signal Pulse Response and Settling Time G = 100

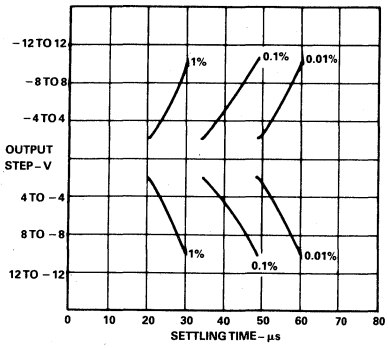


Figure 25. Settling Time Gain = 1000

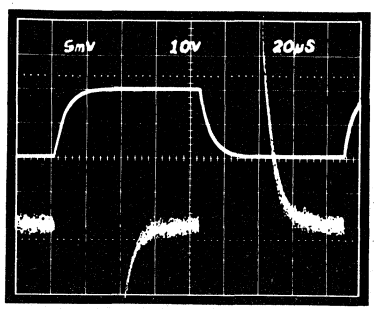


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

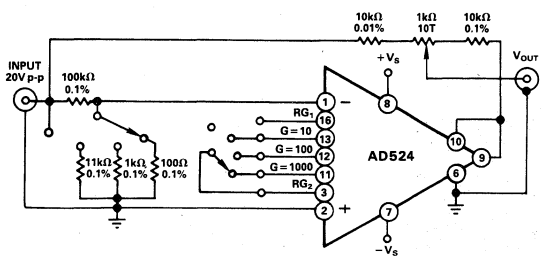


Figure 27. Settling Time Test Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the

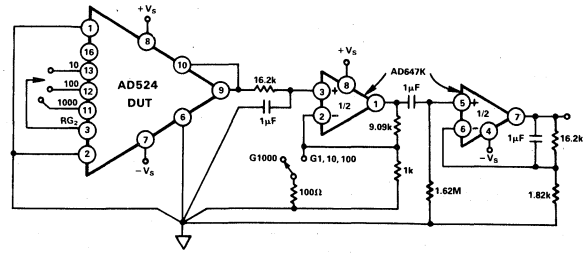


Figure 28. Noise Test Circuit

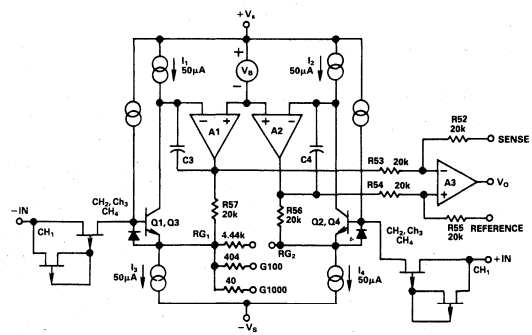


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

gain bandwith product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of 7nV/$\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5mA with a full differential overload (36V) would require over 7k of resistance which would add 10nV$\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance ($\approx$1kΩ) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance ($\approx$3kΩ) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G=1 RG_2 is not connected).

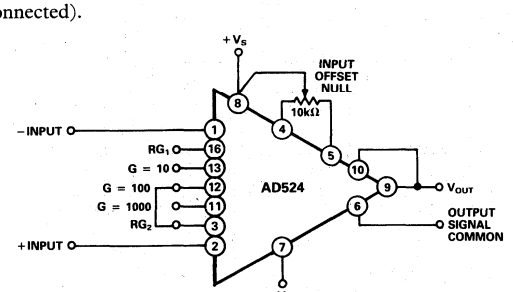


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50ppm/°C typ).

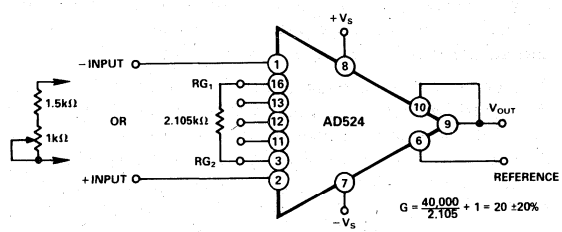


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

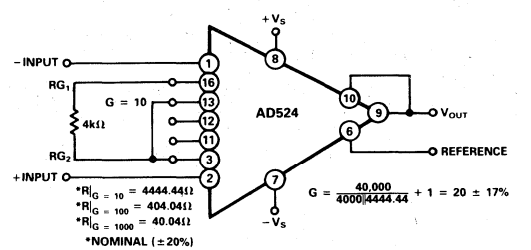


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

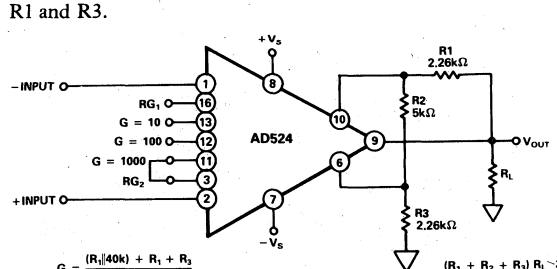


Figure 33. Gain of 2000

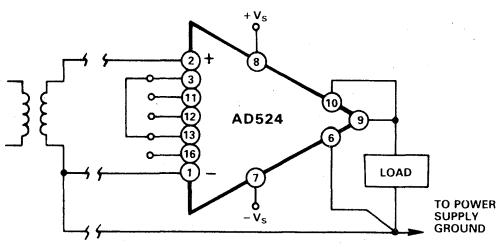
Output Gain	R2	R1,R3	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	1.05kΩ	2.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table I. Output Gain Resistor Values

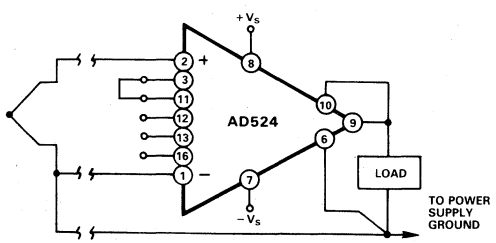
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

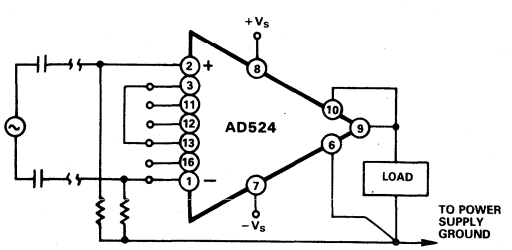
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

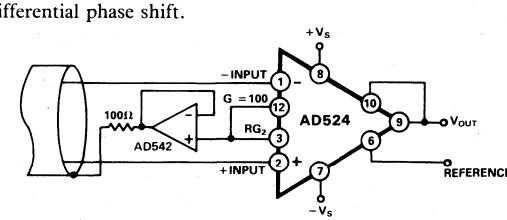


Figure 35. Shield Driver, G ≥ 100

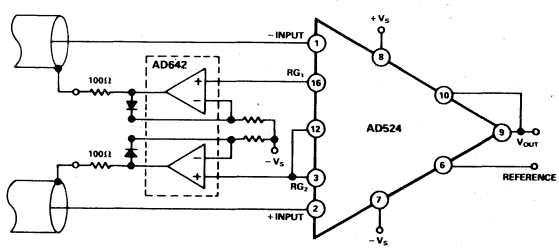


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

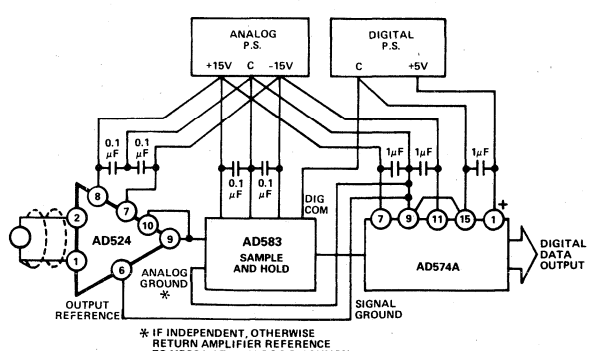


Figure 37. Basic Grounding Practice

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

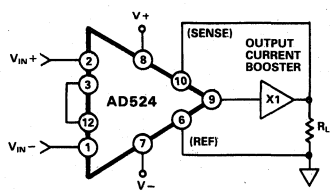


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

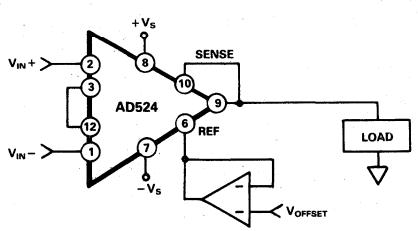


Figure 39. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of $20k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 86dB ($20k\Omega/1\Omega = 86dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.

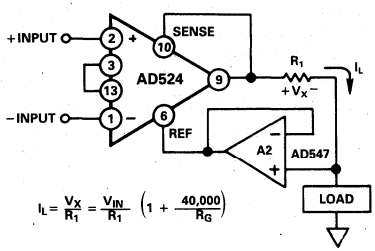


Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

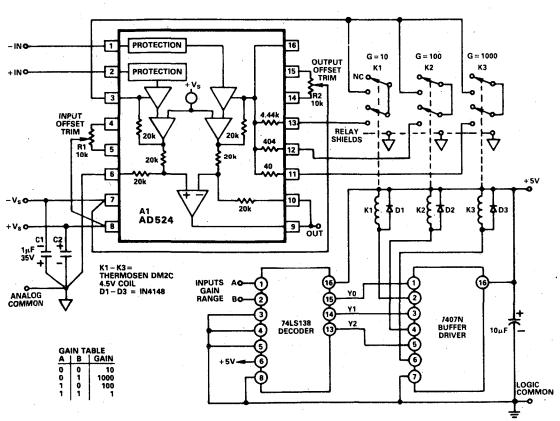


Figure 41. 3 Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

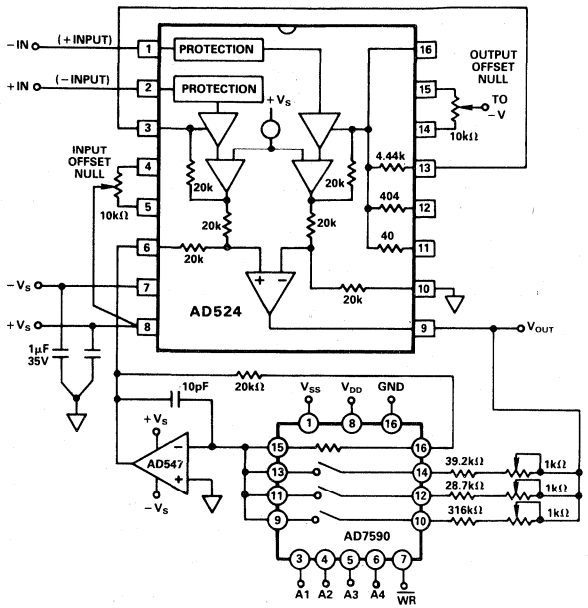


Figure 42. Programmable Output Gain

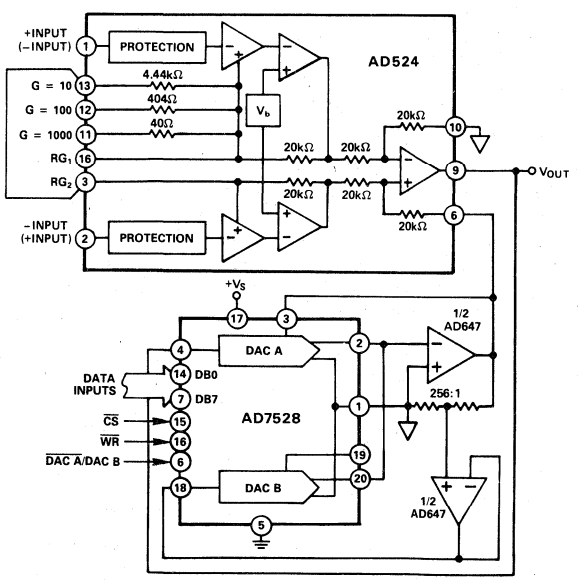


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

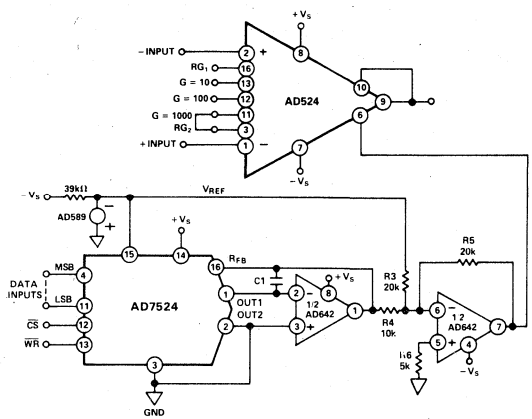


Figure 44. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

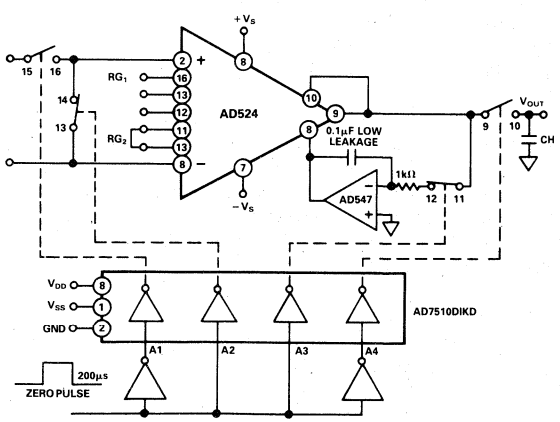


Figure 45. Auto-Zero Circuit

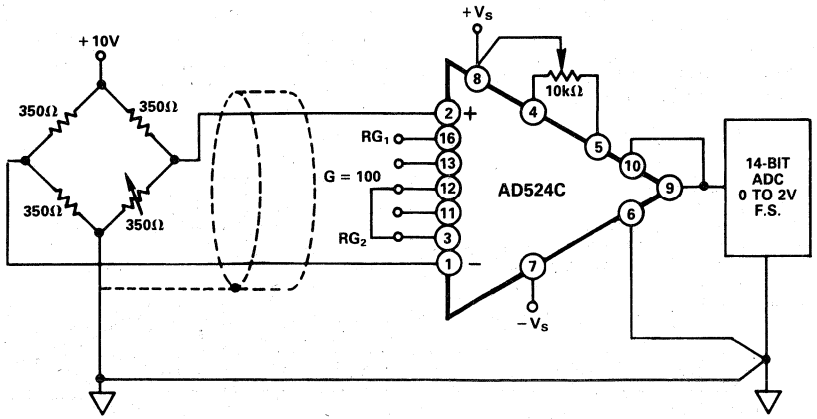


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500ppm	2500ppm	2500ppm	–
Gain Instability	25ppm	(25ppm/°C)(60°C) = 1500ppm	–	1500ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.5μV/°C	(±0.5μV/°C)(60°C) = 30μV			
		30μV/20mV = 1500ppm	–	1500ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±25μV/°C	(±25μV/°C)(60°C) = 1500μV			
		1500μV/20mV = 750ppm	–	750ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(100Ω) = 1.5μV			
		1.5μV/20mV = 75ppm	75ppm	75ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(±100pA/°C)(100Ω)(60°C) = 0.6μV			
		0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV			
		1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(60°C) = 0.6μV			
		0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV			
		3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV			
		1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 8.8μV			
		8.8μV/20mV = 444ppm	444ppm	444ppm	–
Noise, RTI (0.1–10Hz)	0.3μV p-p	0.3μV p-p/20mV = 15ppm	–	–	15ppm
		Total Error	6656.5ppm	10516.5ppm	45ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple–iron(+)–constantan– is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

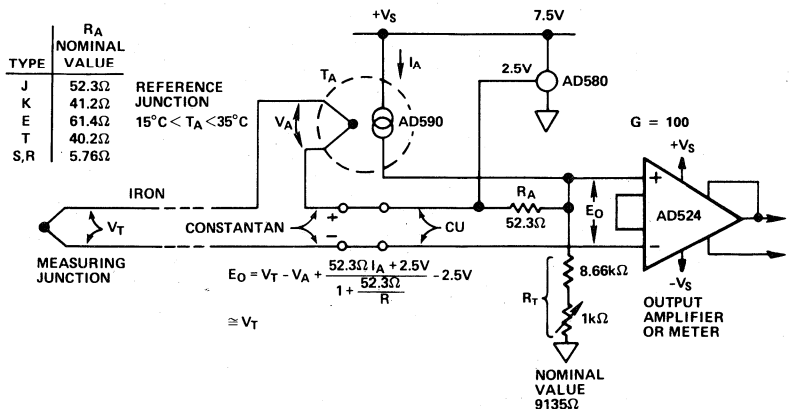


Figure 47. Cold-Junction Compensation

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

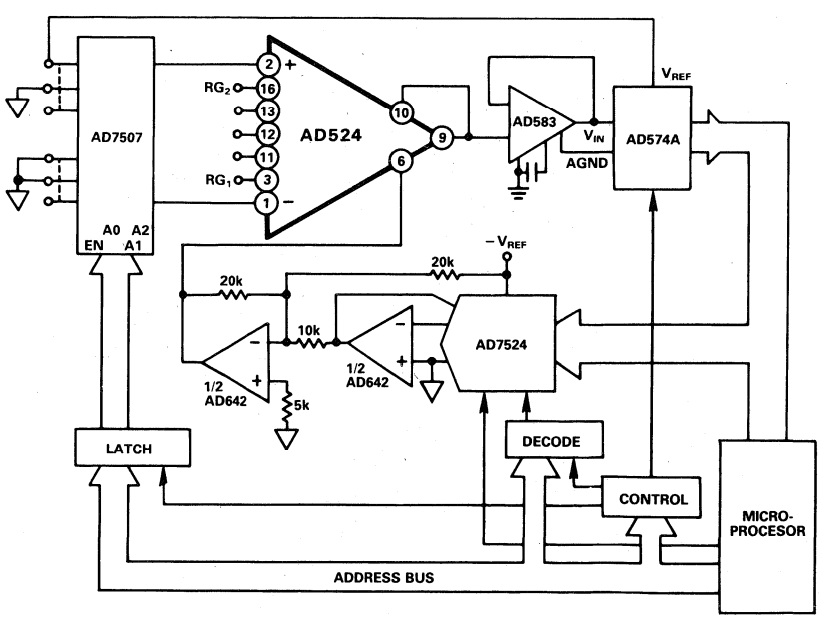


Figure 48. Microprocessor Controlled Data Acquisition System

ANALOG DEVICES

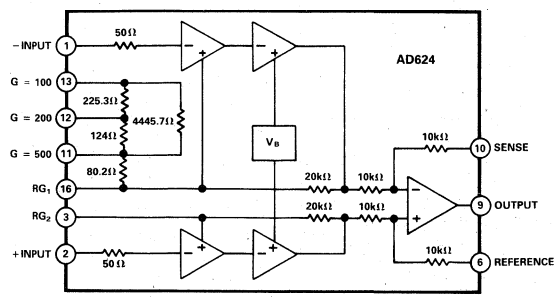
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB max (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD624 is a high precision low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G = 500) and a maximum nonlinearity of 0.001% at G = 1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than $4nV/\sqrt{Hz}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD624A			AD624B			AD624C			AD624S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			**±0.05**			**±0.03**			**±0.02**			**±0.05**	%
G = 100			**±0.25**			**±0.15**			**±0.1**			**±0.25**	%
G = 200, 500			**±0.5**			**±0.35**			**±0.25**			**±0.5**	%
G = 1000			**±1.0**			**±1.0**			**±1.0**			**±1.0**	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			**5**			**5**			**5**			**5**	ppm/°C
G = 100, 200			**10**			**10**			**10**			**10**	ppm/°C
G = 500, 1000			**25**			**15**			**15**			**15**	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			**200**			**75**			**25**			**75**	µV
vs. Temperature			**2**			**0.5**			**0.25**			**2.0**	µV/°C
Output Offset Voltage			**5**			**3**			**2**			**3**	µV
vs. Temperature			**50**			**25**			**10**			**50**	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	**75**			**75**			**80**			**75**			dB
G = 100, 200	**95**			**105**			**110**			**105**			dB
G = 500, 1000	**100**			**110**			**115**			**110**			dB
INPUT CURRENT													
Input Bias Current			**±50**			**±25**			**±15**			**±50**	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			**±35**			**±15**			**±10**			**±35**	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		**±10**			**±10**			**±10**			**±10**		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	**70**			**75**			**80**			**70**			dB
G = 100, 200	**100**			**105**			**110**			**100**			dB
G = 500, 1000	**110**			**120**			**130**			**110**			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz

Model	AD624A			AD624B			AD624C			AD624S			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Slew Rate		5.0			5.0			5.0			5.0		V/μs
Settling Time to 0.01%, 20V Step													
G = 1 to 200		15			15			15			15		μs
G = 500		35			35			35			35		μs
G = 1000		75			75			75			75		μs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		4			4			4			4		nV/√Hz
R.T.O.		75			75			75			75		nV/√Hz
R.T.I., 0.1 to 10Hz													
G = 1		10			10			10			10		μV p-p
G = 100		0.3			0.3			0.3			0.3		μV p-p
G = 200, 500, 1000		0.2			0.2			0.2			0.2		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	±10			±10			±10			±10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	−25		+85	−25		+85	−25		+85	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY													
Power Supply Range	**±5**	±15	**±18**	**±5**	±15	**±18**	**±5**	±15	**±18**	**±5**	±15	**±18**	V
Quiescent Current		3.5	**5**		3.5	**5**		3.5	**5**		3.5	**5**	mA
PACKAGE[1]		D16A			D16A			D16A			D16A		

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

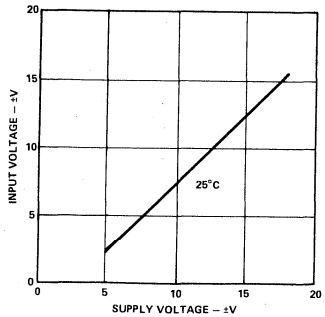


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

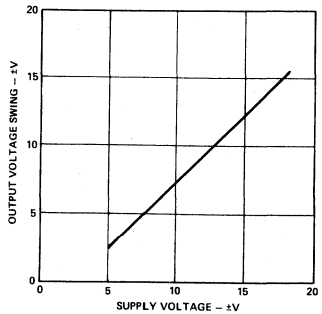


Figure 2. Output Voltage Swing vs. Supply Voltage

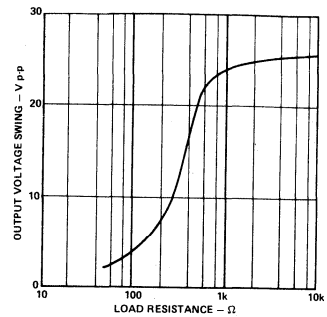


Figure 3. Output Voltage Swing vs. Resistive Load

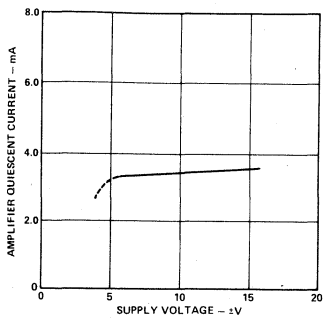


Figure 4. Quiescent Current vs. Supply Voltage

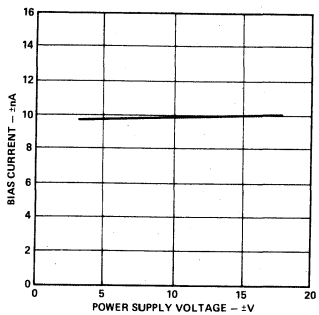


Figure 5. Input Bias Current vs. Supply Voltage

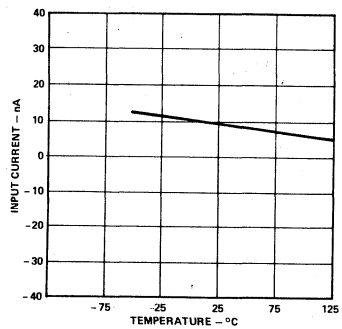


Figure 6. Input Bias Current vs. Temperature

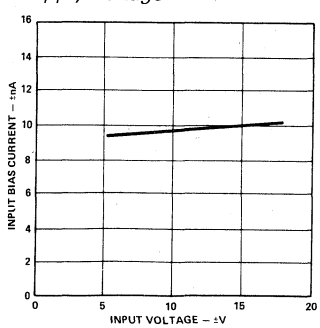


Figure 7. Input Bias Current vs. CMV

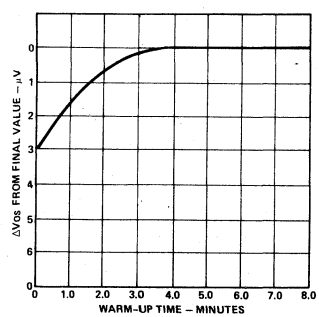


Figure 8. Offset Voltage, RTI, Turn On Drift

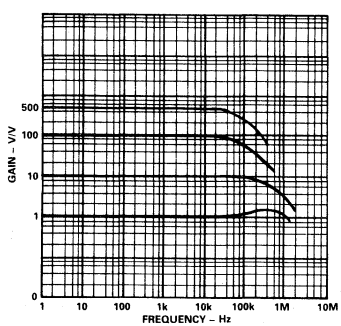


Figure 9. Gain vs. Frequency

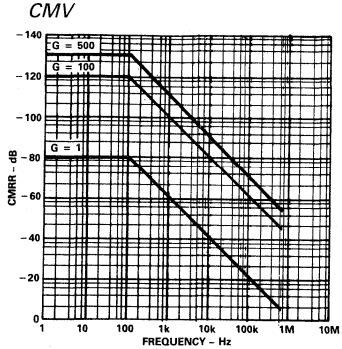


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

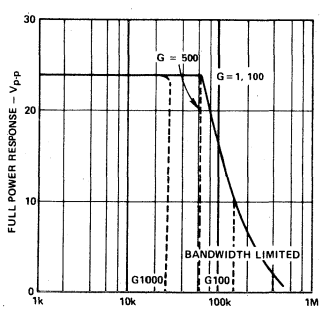


Figure 11. Large Signal Frequency Response

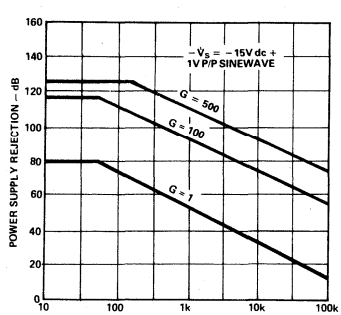


Figure 12. Positive PSRR vs. Frequency

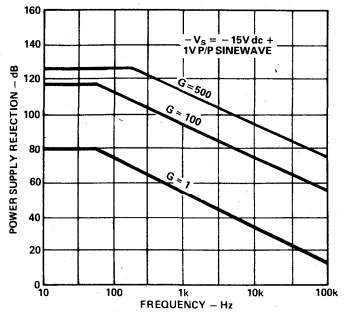


Figure 13. Negative PSRR vs. Frequency

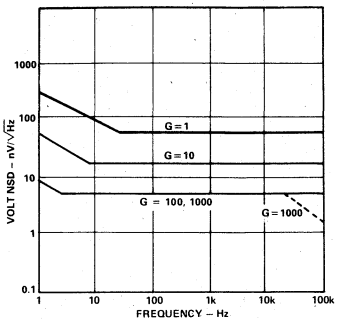


Figure 14. RTI Noise Spectral Density vs. Gain

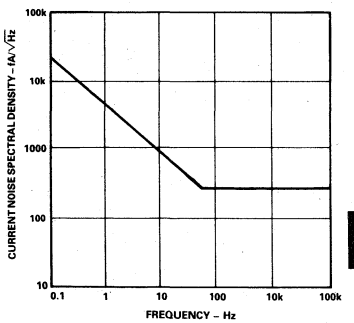


Figure 15. Input Current Noise

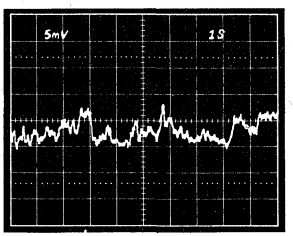


Figure 16. Low Frequency Voltage Noise – G = 1 (System Gain = 1000)

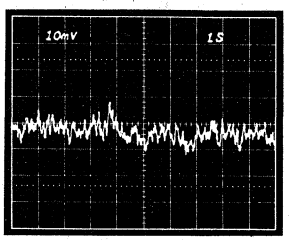


Figure 17. Low Frequency Voltage Noise – G = 1000 (System Gain = 100,000)

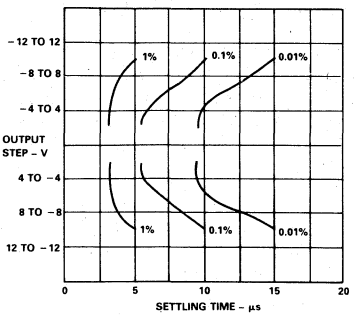


Figure 18. Settling Time Gain = 1

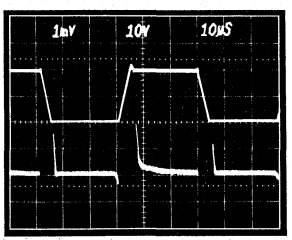


Figure 19. Large Signal Pulse Response and Settling Time – G = 1

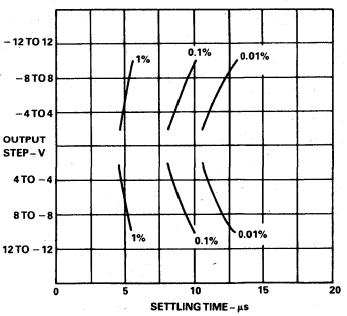


Figure 20. Settling Time Gain = 100

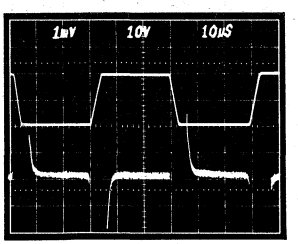


Figure 21. Large Signal Pulse Response and Settling Time G = 100

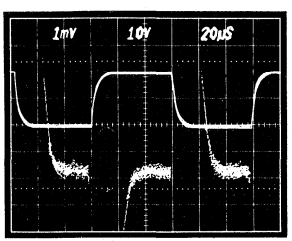


Figure 22. Range Signal Pulse Response and Settling Time G = 500

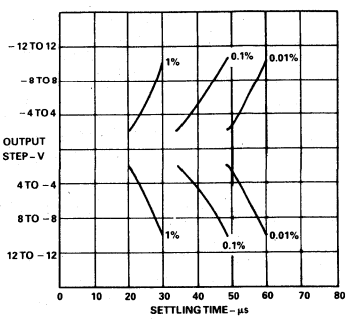


Figure 23. Settling Time Gain = 1000

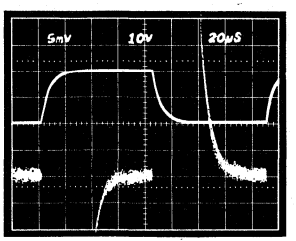


Figure 24. Large Signal Pulse Response and Settling Time G = 1000

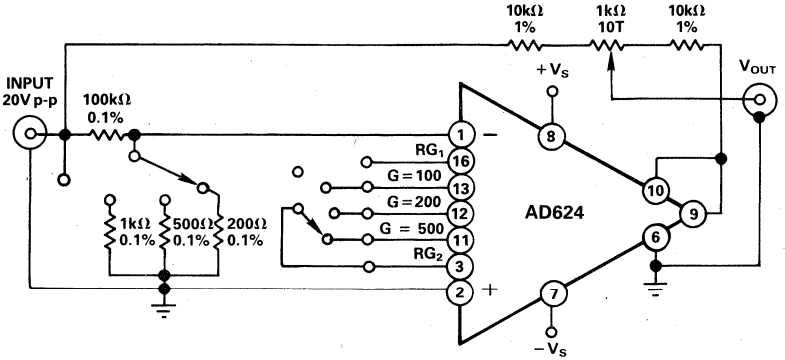


Figure 25. Settling Time Test Circuit

Theory of Operation

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, Gain $= \frac{40k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at G ≥ 500.

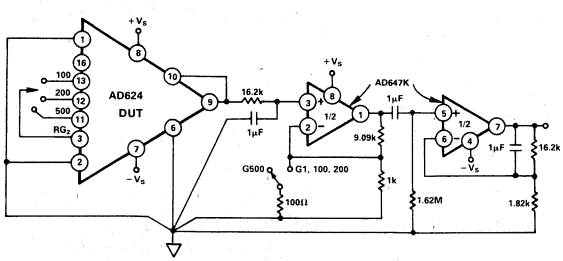


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see $R_G + 100\Omega$ and two diode drops (~1.2V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10mA, the maximum overload voltage is ~ ± 2.5V. While the AD624 can withstand this continuously, momentary overloads of ± 10V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

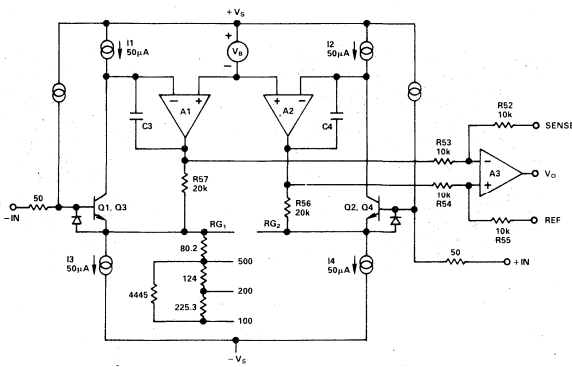


Figure 27. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(RG) + 1. For a Gain of 1, R_G is an Open Circuit.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20V at a gain of 100, 1.9kΩ of resistance is required. The internal gain resistor is 404Ω; the internal protect resistor is 100Ω. There is a 1.2V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400Ω of external resistance would be required (700Ω in series with each input). The RTI noise in this case would be $\sqrt{4KTR_{ext.} + (4nV/\sqrt{Hz})^2} = 6.2nV/\sqrt{Hz}$.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pre-trimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pre-trimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TC's shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

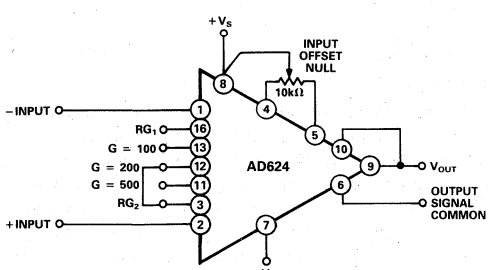


Figure 28. Operating Connections for G =200

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	−1.5ppm/°C	–	–
100	−1.5ppm/°C	13	–
125	−5ppm/°C	13	11 to 16
137	−5.5ppm/°C	13	11 to 12
186.5	−6.5ppm/°C	13	11 to 12 to 16
200	−3.5ppm/°C	12	–
250	−5.5ppm/°C	12	11 to 13
333	−15ppm/°C	12	11 to 16
375	−0.5ppm/°C	12	13 to 16
500	−10ppm/°C	11	–
624	−5ppm/°C	11	13 to 16
688	−1.5ppm/°C	11	11 to 12; 13 to 16
831	+4ppm/°C	11	16 to 12
1000	0ppm/°C	11	16 to 12; 13 to 11

Table I.

pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−15ppm/°C typ), and the temperature coefficient of the internal interconnections.

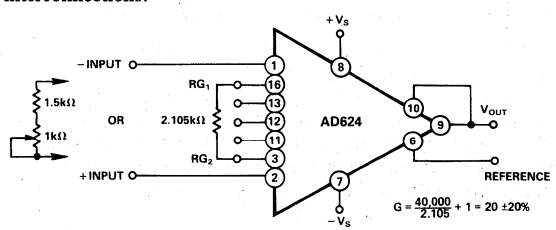


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

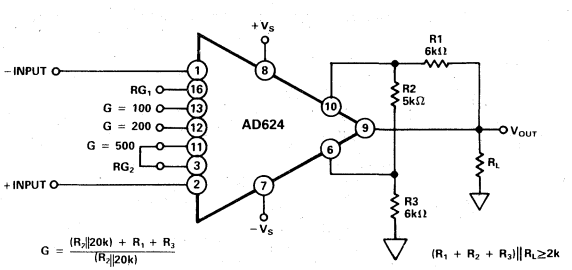


Figure 30. Gain of 2500

NOISE

The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 to 10Hz) voltage noise due to the output stage is 10μV p-p, the contribution of the input stage is 0.2μV p-p. At a gain of 10, the RTI voltage noise would be 1μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2μV p-p $\sqrt{10^2 + (0.2\ (G))^2}$. These calculations hold for applications using either internal or external gain resistors.

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

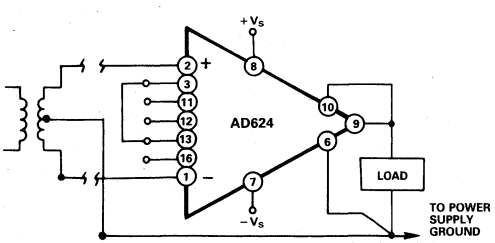


Figure 31a. Transformer Coupled

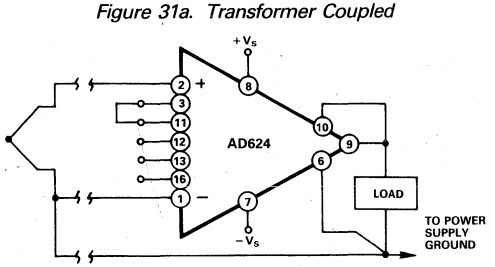


Figure 31b. Thermocouple

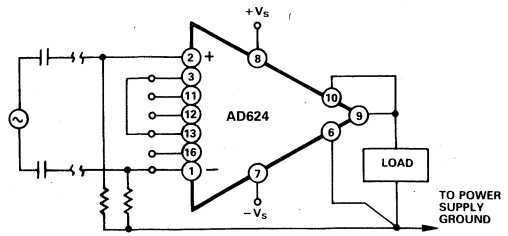


Figure 31c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

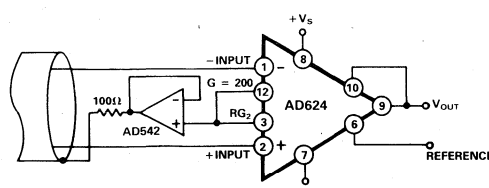


Figure 32. Shield Driver, G ≥ 100

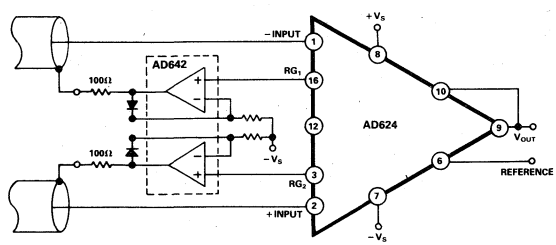


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to

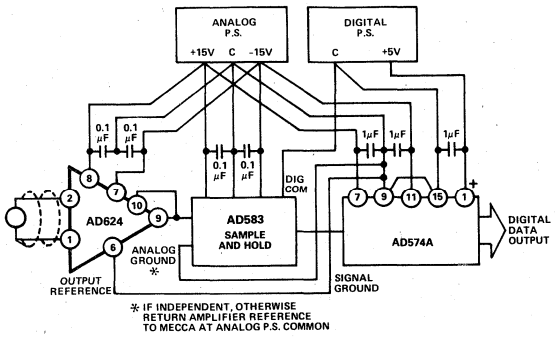


Figure 34. Basic Grounding Practice

minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

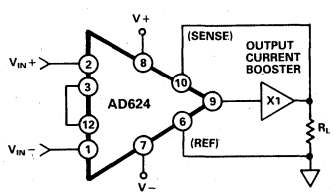


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts, from ground, to be shared between signal and reference offset.

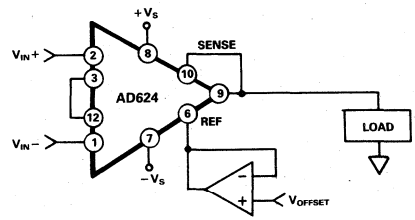


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega = 80dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

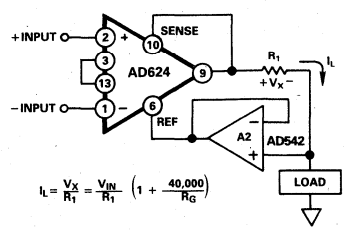


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

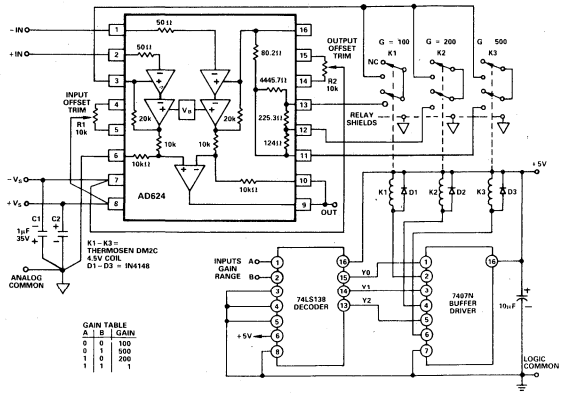


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

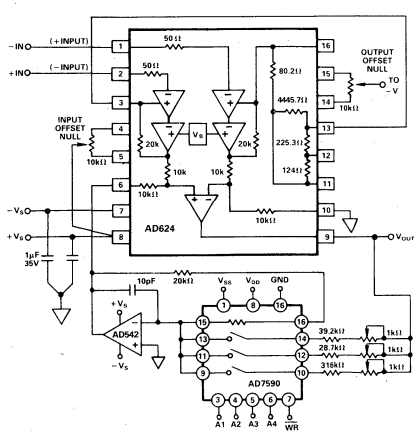


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

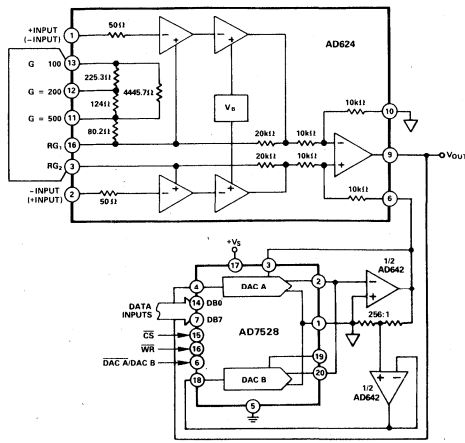


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

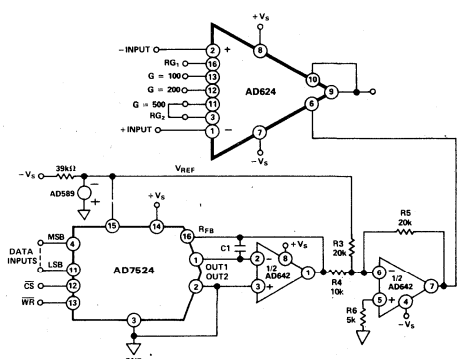


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

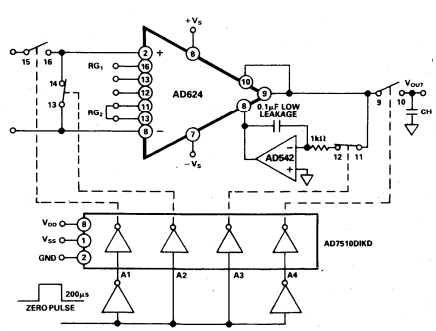


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

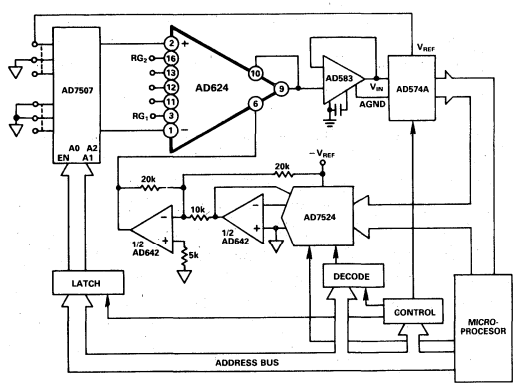


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

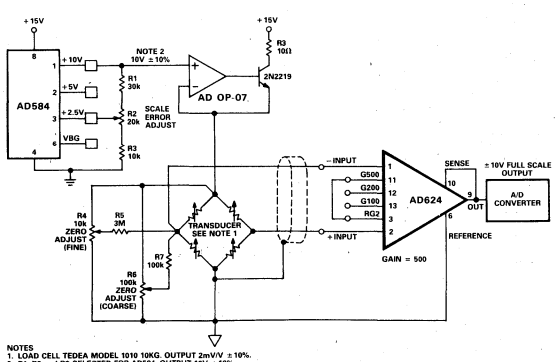


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 6.3mV change in the low pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

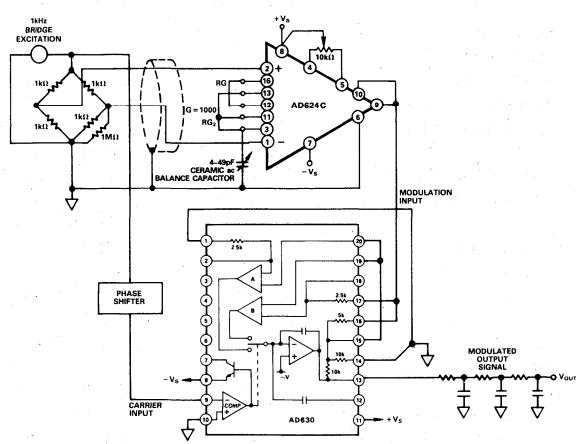


Figure 45. AC Bridge

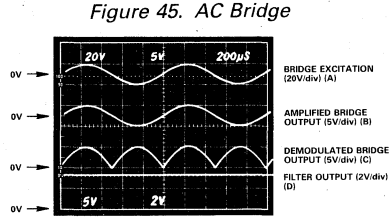


Figure 46. AC Bridge Waveforms

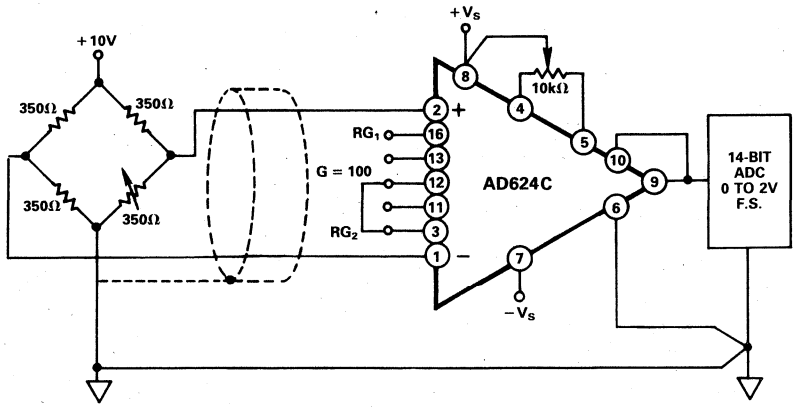


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5Ω, supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm	(10ppm/°C)(60°C) = 600ppm	–	600ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10ppm	–	–	10ppm
Input Offset Voltage	±25μV, RTI	±25μV/20mV = ±1250ppm	1250ppm	1250ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(60°C) = 15μV 15μV/20mV = 750ppm	–	750ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±10μV/°C	(±10μV/°C)(60°C) = 600μV 600μV/20mV = 300ppm	–	300ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(5Ω) = 0.075μV 0.075μV/20mV = 3.75ppm	3.75ppm	3.75ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(5Ω) = 0.050μV 0.050μV/20mV = 2.5ppm	2.5ppm	2.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 9μV 9μV/20mV = 444ppm	450ppm	450ppm	–
Noise, RTI (0.1–10Hz)	0.22μV p-p	0.22μV p-p/20mV = 10ppm	–	–	10ppm
		Total Error	3793.75ppm	5493.75ppm	20ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD624CD in Bridge Application

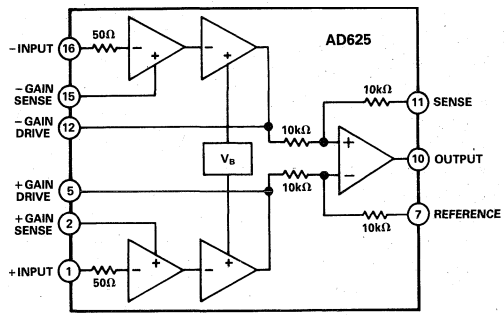
ANALOG DEVICES

Programmable Gain Instrumentation Amplifier

AD625

FEATURES
Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.005% max
Low Noise 4nV/√Hz (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
User Programmed Gains 1 to 10,000

AD625 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier intended for use where flexible gain programmability is required. The performance of the AD625 enables its use in many applications which previously required tradeoffs between expensive external components and performance.

In resistor programmable gain applications (RPGA), as shown in Figure 2, the user can select any gain between 1 and 10,000. Gain programming is accomplished through the use of 3 external resistors. Gain accuracies and temperature coefficients are determined primarily by the match between the user provided gain setting resistors. Common-mode rejection (CMR) ranges from 70dB to 115dB minimum, for overall gains of 1 to 1000, and is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network (see Figure 3). The AD625 based SPGA can be programmed for any set of gains between 1 and 10,000, with completely user-selected gain steps.

The AD625 exhibits excellent ac performance; its 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD625 in high speed data acquisition applications.

PRODUCT HIGHLIGHTS

1. The AD625 allows user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
4. The gain accuracy and gain temperature coefficients of the amplifier circuit are primarily dependent on user selected external resistors.
5. The proprietary design of the AD625 provides the lowest input voltage noise of any resistor programmable instrumentation amplifier – 4nV/√Hz at 1kHz.
6. The match of the two feedback resistors is not critical to maintain high common-mode rejection. This is possible because the gain sense current is insensitive to common-mode voltage.

SPECIFICATIONS (typical @ $V_S = \pm 15V$, $R_L = 2k\Omega$ and $T_A = +25°C$ unless otherwise specified)

Model	AD625A	AD625B	AD625C	AD625S
GAIN				
Gain Equation (External Resistor Gain Programming)	$2\frac{R_F}{R_G} + 1$	*	*	*
Gain Range	1 to 10000	*	*	*
Gain Error, Max	±0.05%	±0.03%	±0.02%	*
Nonlinearity, max	±0.005%	±0.003%	±0.001%	*
Gain vs. Temperature, max	5ppm/°C	*	*	*
VOLTAGE OFFSET (May be Nulled)				
Input Offset Voltage, max	200μV	75μV	25μV	**
vs. Temperature, max	2μV/°C	0.5μV/°C	0.25μV/°C	2μV/°C
Output Offset Voltage, max	5mV	3mV	2mV	**
vs. Temperature, max	50μV/°C	25μV/°C	10μV/°C	50μV/°C
Offset Referred to the Input vs. Supply				
G = 1	70dB	75dB	80dB	**
G = 10	85dB	105dB	110dB	**
G = 100	95dB	105dB	110dB	**
G = 1000	100dB	110dB	115dB	**
INPUT CURRENT				
Input Bias Current, max	±50nA	±25nA	±15nA	*
vs. Temperature	±50pA/°C	*	*	*
Input Offset Current, max	±35nA	±15nA	±10nA	*
vs. Temperature	±20pA/°C	*	*	*
INPUT				
Input Voltage Range				
Max Differ. Input Linear (V_D)	±10V	*	*	*
Max Common Mode Linear (V_{CM})	$12V - \left(\frac{G}{2} \times V_D\right)$	*	*	*
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance, min				
G = 1	70dB	75dB	80dB	*
G = 10	90dB	105dB	110dB	*
G = 100	100dB	105dB	110dB	*
G = 1000	110dB	120dB	130dB	*
OUTPUT RATING	±10V @ 5mA	*	*	*
DYNAMIC RESPONSE				
Small Signal −3dB				
G = 1	650kHz	*	*	*
G = 10	400kHz	*	*	*
G = 100	100kHz	*	*	*
G = 1000	25kHz	*	*	*
Slew Rate	5.0V/μs	*	*	*
Settling Time to 0.01%, 20V Step				
G = 1 to 200	15μs	*	*	*
G = 500	35μs	*	*	*
G = 1000	75μs	*	*	*
NOISE				
Voltage Noise, 1kHz				
R.T.I.	$4nV/\sqrt{Hz}$	*	*	*
R.T.O.	$75nV/\sqrt{Hz}$	*	*	*
R.T.I., 0.1 to 10Hz				
G = 1	10μV p-p	*	*	*
G = 10	1.0μV p-p	*	*	*
G = 100	0.3μV p-p	*	*	*
G = 1000	0.2μV p-p	*	*	*
Current Noise				
0.1Hz to 10Hz	60pA p-p	*	*	*

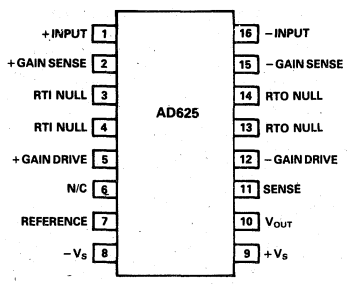
Model	AD625A	AD625B	AD625C	AD625S
TEMPERATURE RANGE				
Specified Performance	−25°C to +85°C	*	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*	*
POWER SUPPLY				
Power Supply Range	±5V to ±18V	*	*	*
Quiescent Current	3.5mA (5mA max)	*	*	*
Gain Sense Current, max	500nA	250nA	100nA	*
Gain Sense Current vs. Temperature, max	25nA/°C	15nA/°C	10nA/°C	*
Gain Sense Offset Current	500nA	250nA	100nA	*
Gain Sense Offset Current vs. Temperature	20nA/°C	10nA/°C	5nA/°C	*
PACKAGE OPTION[1]	D16A AD625AD	D16A AD625BD	D16A AD625CD	D16A AD625SD

NOTES
*Specifications same as AD625A.
**Specifications same as AD625B.

[1]See Section 19 for package outline information.
Specifications subject to change without notice.

5

PIN CONFIGURATION



Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture. A preamp section (Q1-Q4) provides additional gain to A1 and A2, which increases the overall transconductance of the input stage. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant thereby impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain $\left(\frac{2R_F}{R_G} + 1\right)$ times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_O, referred to the reference potential.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, the approach allows the circuit to achieve a very high open-loop gain of 3×10^8 at programmed gains ≥ 500 thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors resulting in an RTI noise of $4nV/\sqrt{Hz}$.

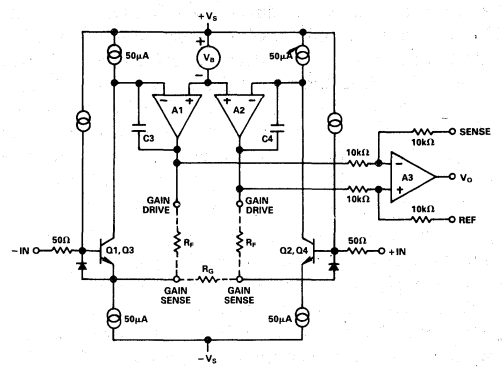


Figure 1. Simplified Circuit of Amplifier

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (see Figure 2) only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pre-trimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625 typically contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors (R_F).

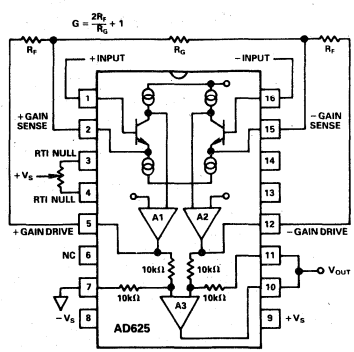


Figure 2. AD625 in Fixed Gain Configuration

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. In the unity gain configuration R_F should be 20kΩ; for gains > 1 R_F can be in the range of 10kΩ to 30kΩ. The gain resistor (R_G) is determined by the formula $R_G = \frac{2R_S}{G-1}$

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the user the abiliy to externally program precision gains from digital inputs. To date, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (Pins 2, 15, 5, 12; see Figure 4). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset voltage error. To clarify this point, an error budget analysis has been performed in Table I. Figure 4 shows the AD625 based SPGA used for the analysis in Table I. The output of the AD625 feeds a 12-bit DAS with a 0-10V input voltage range. The gain used for the RTI calculations is set at 16; as the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will change the values in the table.

Figure 3 shows an SPGA at a gain of 16. To determine the gain, it is necessary to calculate R_G and R_F. R_G equals the resistance between the gain sense lines (Pins 2 and 15) of the AD625. In Figure 3, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, therefore, R_G equals 2600Ω. R_F equals the resistance between the gain sense and gain drive pins (Pins 12 and 15, or Pins 2 and 5). In Figure 3, R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or R_F equals 19.5kΩ. The gain equals:

$$\frac{2R_F}{R_G} + 1 = 2\frac{(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

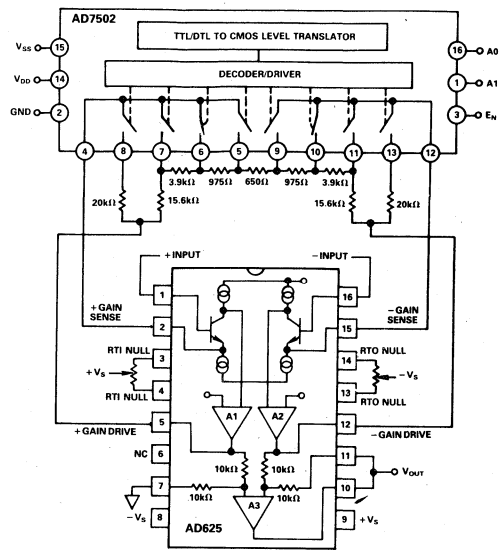


Figure 3. SPGA in a Gain of 16

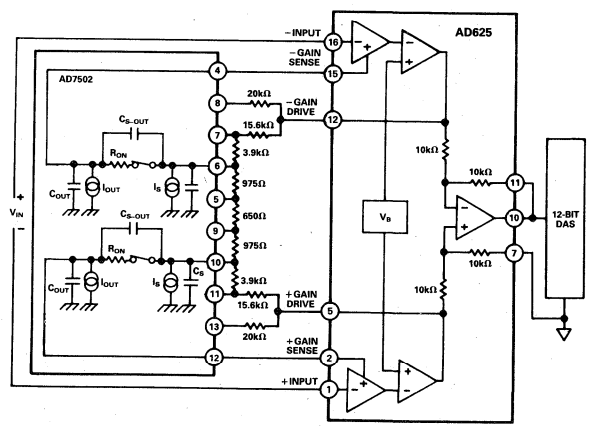


Figure 4. SPGA with Multiplexer Error Sources

Induced Error	Specification AD625	Specification AD7502	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 150nA	Switch Resistance 170Ω	150nA × 170Ω = 25.5μV	25.5μV
RTI Offset Voltage	Gain Sense Current 300nA	Differential Switch Resistance 6.8Ω	300nA × 6.8Ω = 2.04μV	2.04μV
RTO Offset Voltage	Feedback Resistance[1] 20kΩ	Differential Leakage Current (I_S)[2] +0.2nA −02nA	2(0.2nA × 20kΩ) − 8μV	0.5μV
RTO Offset Voltage	Feedback Resistance[1] 20kΩ	Differential Leakage Current (I_{OUT})[2] +1nA −1nA	2(1nA × 20kΩ) = 40μV	2.5μV

NOTES

[1]The resistor for this calculation is the user provided feedback resistance (R_F), 20kΩ is recommended (see resistor programmable gain amplifier section)

[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1), to determine offset voltage. Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculation in Table I. Typical performance will be much better.

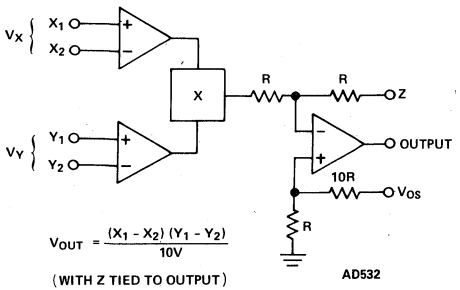
Table I. Errors Induced by Multiplexer to an SPGA

Analog Signal Processing Components

Contents

Selection Guide
Analog Signal Processing Components

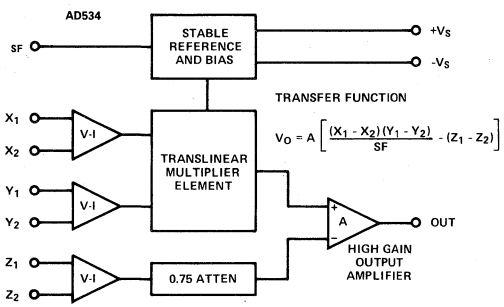
Internally Trimmed Multipliers



AD532

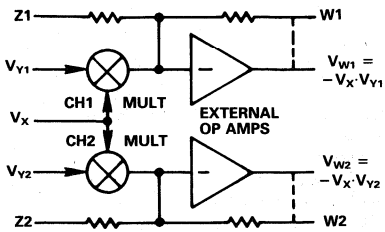
Page

Pretrimmed to ±1.0% (AD532K) Vol. I
No External Components Required 6-17
Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
Diff Inputs for $(X_1-X_2)(Y_1-Y_2)/10$ Transfer Function
Monolithic Construction



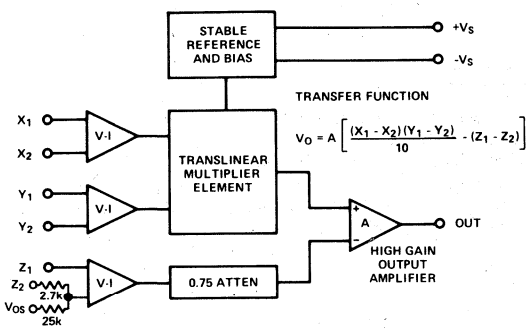
AD534

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L) Vol. I
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function 6-27
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability



AD539

Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control-Bandwidth of 5MHz
Full-Calibrated, Monolithic Circuit

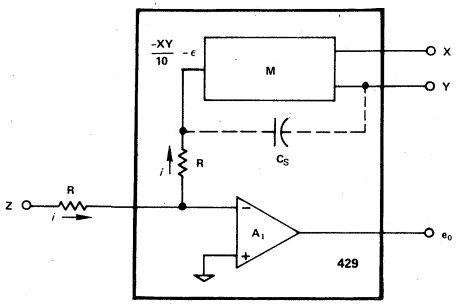


AD632

Pretrimmed to ±0.5% max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance
for $[(X_1 - X_2)(Y_1 - Y_2)/10V] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X10 Gain
Low Noise Design: 90μV rms, 10Hz–10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

Selection Guide
Analog Signal Processing Components

Internally Trimmed Multipliers

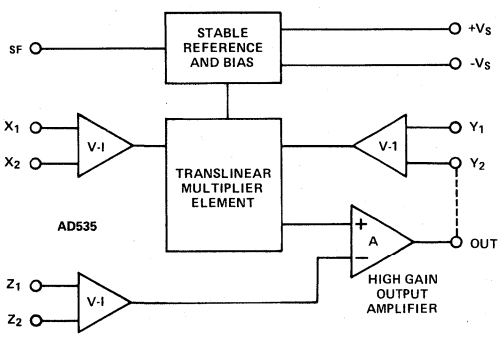


MODEL 429

Page

1.0%/0.5% Accuracy Without Trimming (429A/B) Vol. II 6-9
Low Drift to 1.0mV/°C max
Wideband – 10MHz
0.2% Nonlinearity max (429B)
External Amplifiers not Required
MTBF: 169, 268 Hours

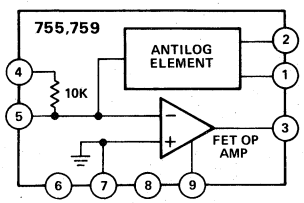
Internally Trimmed Dividers



AD535

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K) Vol. I 6-37
±2.0% max Error, 50:1 Denominator Range (AD535K)
All Inputs (X, Y and Z) Differential
Monolithic Construction

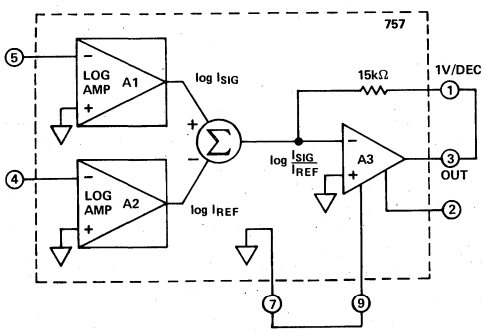
Log-Antilog Amplifiers



MODEL 755, MODEL 759

Page

- **High Accuracy: Models 755N, 755P** — Vol. II 8-7
- **Low Cost: Models 759N, 759P**
- **Complete Log-Antilog Amplifiers: External Components not Required**
- **Temperature-Compensated Internal Reference**
- **6 Decades Current Operation: 1nA to 1mA**
- **1% max Error: 1nA to 1mA (755)**
  20nA to 200μA (759)
- **4 Decades Current Operation: 1mV to 10V**
- **1% max Error: 1mV to 10V (755)**
  1mV to 2V (759)

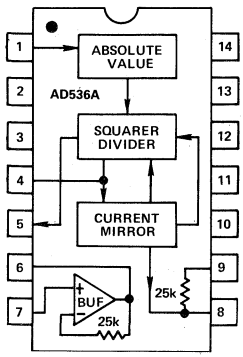


MODEL 757

- **6 Decade Operation – 1nA to 1mA** — Vol. II 8-11
- **1/2% Log Conformity – 10nA to 100μA**
- **Symmetrical FET Inputs**
- **Voltage or Current Operation**
- **Temperature Compensated**
- **Complete Log Ratio Amplifier: External Components not Required**

Selection Guide
Analog Signal Processing Components

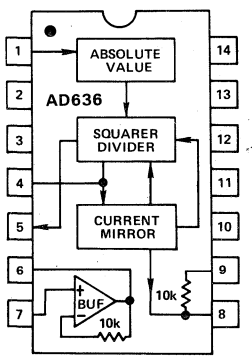
RMS-to-DC Converters



AD536A

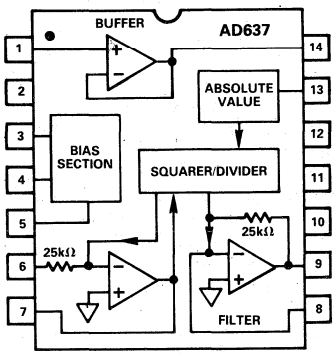
Page

- True rms-to-dc Conversion — Vol. I 6–43
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: V_{rms}>100mV
  - 2MHz Bandwidth: V_{rms}>1V
  - Signal Crest Factor 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- −55°C to +125°C Operation (AD536AS)



AD636

- True rms-to-dc Conversion — Vol. I 6–71
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz −3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit



AD637

Page Vol. I 6-77

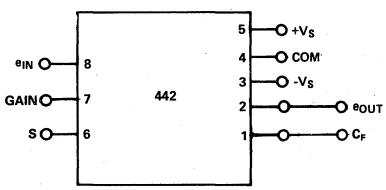
High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Max Error to Crest Factor of 3**

Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**



MODEL 442

Vol. II 7-7

DC to 8MHz Response (−3dB)

High Accuracy:
- **With No Ext. Trim: ±2mV ±0.15% of Rdg., max**
- **With Ext. Trim: ±1mV ±0.05% of Rdg., max**

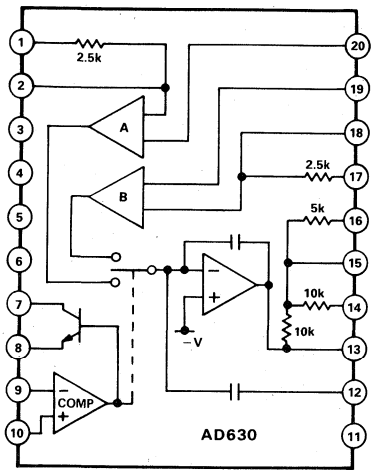
Low Drift: ±(35μV ±0.01% of Reading)/°C max, 442L

Fast Settling Time: 5ms to 1%

All Hermetically Sealed Semiconductors

No External Components Required to Meet Specifications

Selection Guide
Analog Signal Processing Components
Modulator/Demodulator



AD630

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

Orientation
Analog Signal Processing Components

MULTIPLIERS/DIVIDERS

Multiplication For two inputs, V_X and V_Y, a multiplier will provide the output, $E_{out} = V_X V_Y / E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If E_{ref} = 10V, E_{out} = 10V when V_X and V_Y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement, and mathematical operations in analog computing, curve fitting, and linearizing.

If the inputs may be of either positive or negative polarity, and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the 4 quadrants of the X-Y plane.

Squaring If $V_X = V_Y = V_{in}$, a multiplier's output will be V_{in}^2 / E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive, whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads, and mathematical operations.

Division For a numerator input, V_Z, and a denominator input, V_X, an analog divider will provide the output, $E_{out} = E_{ref}(V_Z/V_X)$. If E_{ref} = 10V, E_{out} will be 10V or less for $V_Z \leqslant V_X$. V_X is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_Z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_Z. Analog dividers are used to compute ratios—such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements, and for mathematical operations in analog computing.

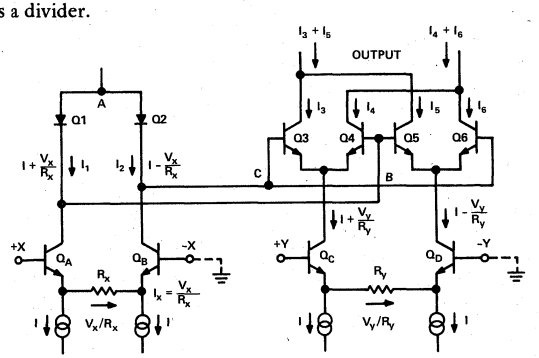
Square rooting For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref} V_{in}}$. A square-rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, etc.

A number of devices are listed here, differing in internal architecture, external functional configuration, device technology, and performance specifications. Some have essentially fixed references; others have an actively variable or programmable reference as a third input (*multifunction devices*), and one type (model 433) performs the one-quadrant operation, $E_o = V_Z(V_Y/V_X)^m$, where m is an exponent adjustable from 1/5 to 5. With one exception (model 436 precision 2-quadrant divider), all of the devices listed here can be used for any of the functions defined above.

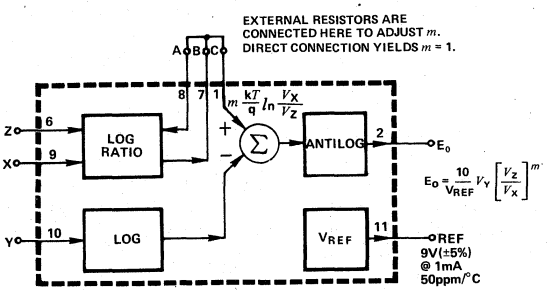
Considerable information on these functions, the nature of devices to perform them, and extensive discussions of their applications can be found in two publications available from Analog Devices.[1,2] A wealth of information is also to be found in the data sheets for the individual devices, published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture All of the devices in this selection rely on the logarithmic properties of silicon P-N junctions. With the exception of models 433 and 436, the circuit employed is basically like that of the "Gilbert cell" (its 4-quadrant-multiplying circuitry and performance are described in (1) and (2), with further references to original sources). The input voltages are converted to currents, the currents are multiplied together and divided by a reference, and the net output current, $I_X I_Y / I_{ref}$, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division. In the AD531[3], the I_{ref} terminals are available for external programming or variation; thus, the AD531 is a 3-variable "multifunction" IC which can divide without external feedback. This versatile feature offers greater bandwidth as a divider.



Basic 4-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2\,V_X\,V_Y}{I\,R_X\,R_Y}$$



Functional Block Diagram of Model 433

In multifunction devices like Model 433, the feedback currents of the input op amps are used to develop logarithmic

[1] *Multiplier Application Guide*, available upon request

[2] *Nonlinear Circuits Handbook*, D. H. Sheingold, ed., 1976, 536pp., $5.95, P.O. Box 796, Norwood MA 02062

[3] Data sheet available upon request.

voltages across transistor base-emitter junctions; these voltages are summed and differenced and produce an exponential current proportional to V_yV_z/V_x via another transistor junction in the input path of the output amplifier. Thus, the output voltage is proportional to V_yV_z/V_x; an internally generated reference voltage is available as a fixed reference for the odd input in two-variable operations. In the 433, the internal emitter-voltage difference proportional to log (V_z/V_x) can be amplified or attenuated by the appropriate connection of a resistive attenuator with an attenuation ratio, m; since the antilog of $m(\log V_z/V_x)$ is $(V_z/V_x)^m$, the output of the 433 is proportional to $V_y(V_z/V_x)^m$. In the model 436 divider, the inputs are scaled and linearly combined, before the log-antilog computation takes place; the result is that the numerator (of V_z/V_x) may have positive or negative values. The 436 circuit is optimized and trimmed for performance as a dedicated divider; it has a fixed reference. Its circuit principles are discussed in some detail on the data sheet.

External functional configuration As noted earlier, with the exception of the model 436 dedicated divider, all of the devices listed here can be used for multiplication, division, squaring, and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. As an example, the AD534 is shown connected for multiplication, and the AD535, which has similar architecture but is optimized for division, is shown connected for division and square-rooting. Performance of pretrimmed devices is optimized in specified modes of operation, usually multiplication. The data sheets show how devices are connected for the various modes of operation; where appropriate, the trim circuits and procedures for optimizing performance are provided.

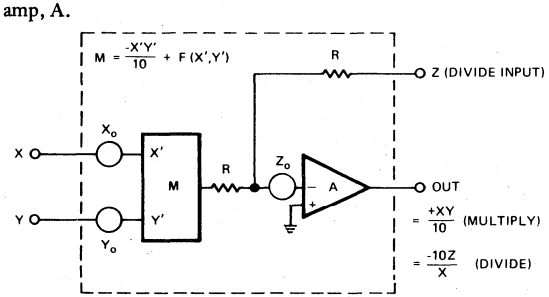
Some devices have differential inputs, which provide a great deal of flexibility. They permit polarity changes without external inversion, direct subtraction of inputs, insertion of bias voltages for additive constants, and direct multiplication of the results of differential measurements.

Technologies The devices described here are either monolithic integrated circuits or high-performance modules. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The modules provide the highest performance: speed (model 429), accuracy as a divider (436), and accuracy in multifunction applications (433). On the other hand, the IC's provide economy of cost and space, and the availability of "mil-temp" range (−55°C to +125°C) versions. The pretrimmed IC's (AD534, AD535 and AD532) use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors to 0.25%, and linearities as yet unmatched in the industry.

Performance Multiplier performance, specifications and test circuitry are described in great detail in the NONLINEAR CIRCUITS HANDBOOK. Here is a brief digest of the factors relating to low-frequency performance.

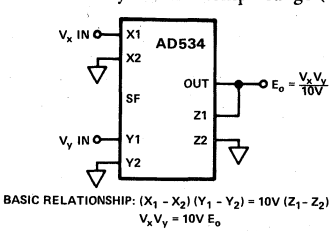
In theory, a multiplier has an output which is ideally the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities, which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practice (see the figure), the multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is the gain-conditioning op amp, A.

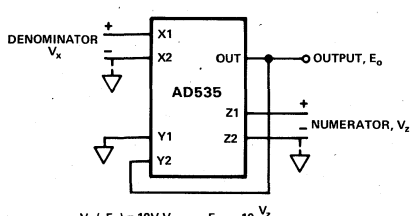


Functional Block Diagram of Typical Multiplier/Divider

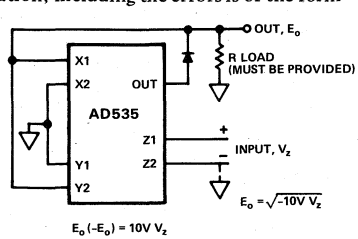
Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model used for considering errors. X_0 and Y_0 are input offset voltages, Z_0 is the offset-referred-to-the-input of the output amplifier, and $F(X', Y')$ is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form



Multiplier



Divider



Square Rooter

$$E_o = \frac{XY}{10B} \pm \left[\frac{X_oY}{10B} \pm \frac{XY_o}{10B} \pm Z_o + f(X,Y)\right]$$

Product; X_{offset}, Y_{offset}; Output offset; Nonlinearity and feedthrough

Linear "Y"; Feedthrough "X"

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by applying external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\epsilon_x + |V_y|\epsilon_y$$

were ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (e.g., 10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

LOGS AND LOG RATIOS

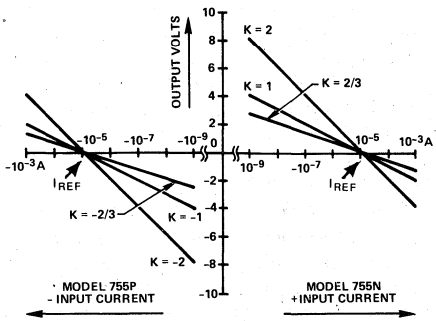
In the *logarithmic* mode, the ideal output equation is

$$E_o = -K \log_{10}\left(\frac{I_{in}}{I_{ref}}\right)$$

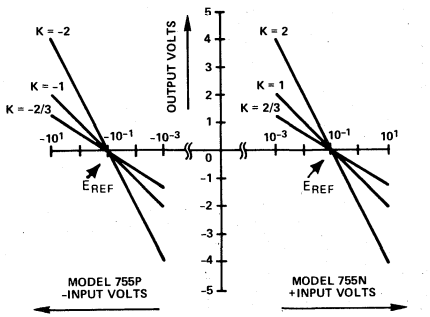
E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin-programmable to be either 1V, 2V, or 2/3V, or externally adjustable to any value $\geqslant$ 2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V, or an arbitrary value adjustable by an external resistance ratio.

I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA (E_{ref} = 0.1V) or externally adjusted; but model 757 is a *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive;* "P" indicates that



Log of Current



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

*A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1000 (3 decades), the output would change by 6V.

only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 755N, with K = +1V, would produce an output voltage, E_o = -1V log (100) = -2V; on the other hand, -10V applied to model 755P, with K = 1V, would produce an output voltage, E_o = -(-1V) log (100) = +2V. The figure shows, in condensed form, the outputs of P and N log-amps, with differing K values, for voltage and current inputs.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs, and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbance as the log-ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multi-term products and ratios.

ANTILOGS

In the *antilogarithmic* (exponential) mode, the ideal output equation is

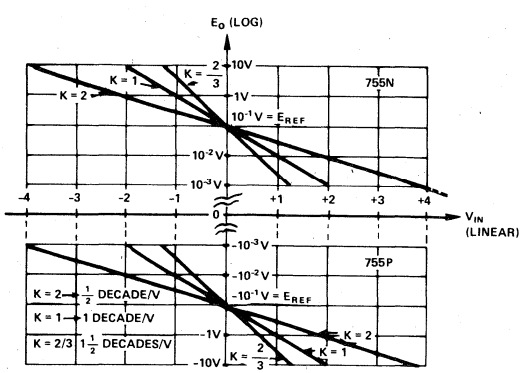
$$E_o = E_{ref} \exp_{10} (-E_{in}/K)$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = -2V, if E_{in} = +4V, and E_{ref} = -0.1V, then

$E_o = -0.1V \cdot 10^{-4/-2}$, or -10V; if E_{in} = -4V, then

$E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure below shows, in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.



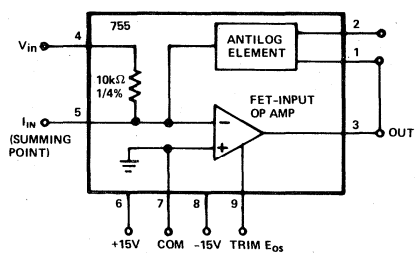
Antilog Operator Response Curves, Semilog Scale
$E_o = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

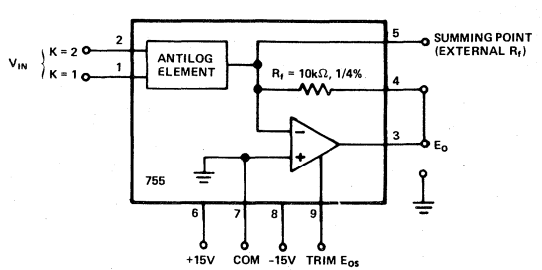
Considerable information regarding log- and antilog-amplifier circuit design, performance, selection, and applications is to be found in the NONLINEAR CIRCUITS HANDBOOK[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



b) Log/Antilog Amplifier Connected in the Exponential Mode

[1] *Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood MA 02062

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

$$I = I_o(e^{qV/kT} - 1) \cong I_o e^{qV/kT}$$

and $V = (kT/q) \ln (I/I_o)$

where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11605° K/V) is the ratio of charge of an electron to Boltzmann's constant, and T is junction temperature kelvin. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o) \\ &= (kT/q) (\ln I_{in} - \ln I_{ref}) + (kT/q) (\ln I_o - \ln I_o) \\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

The temperature-dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade (kT/q) ln10 at room temperature) to 1V/decade.

Errors are introduced by the offset current of the amplifier, and the offset voltage, for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog paper. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output} \\ &= 1V \cdot \log (1.01\ I/I_{ref}) - 1V \cdot \log (I/I_{ref}) \\ &= 1V \cdot \log 1.01 = 0.0043V = 4.3mV\end{aligned}$$

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17.	5.7
3.0	13.	26.	8.6
4.0	17.	34.	11.
5.0	21.	42.	14.
10.0	41.	83.	28.

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction — step changes in the direction of increasing current are responded to more quickly than step decreases of current.

RMS-TO-DC CONVERTERS

The accurate calculation of the root-mean-square of an ac waveform has long been a stumbling block to designers of ac measurement and control instrumentation. Historically, this problem has been addressed by various, each method tailored to the specific application. The rms of ac signals is important because it is a measure of the power in that signal.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of (i.e., full-wave or half-wave rectifying) a signal, filtering it, and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform and will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

Examples of applications include noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True-rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

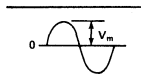
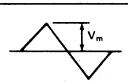
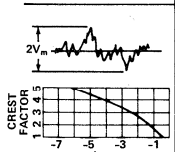
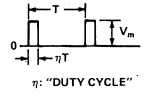
True-rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise, and acoustical noise. The electrical signals produced by these mechanical actions are often noisy, non-periodic, nonsinusoidal, and superimposed on dc levels, and require true-rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

The basic approach used in these converters for computing the rms is to take the absolute value, square it, and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^{\,2}}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^{\,2})}$$

is valid if the averaging time-constant is sufficiently long compared with the periods of the lowest-frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter, using an external filtering capacitance. Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, the data sheets show how an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{ext}.

WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ $0.707\,V_m$	$\frac{2}{\pi}V_m$ $0.637\,V_m$	$\frac{\pi}{2\sqrt{2}} = 1.111$	$\sqrt{2} = 1.414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1.155$	$\sqrt{3} = 1.732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS $= 0.798$ RMS	$\sqrt{\frac{\pi}{2}}$ 1.253	C.F. / q 1 / 32% 2 / 4.6% 3 / 0.37% 3.3 / 0.1% 3.9 / 0.01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2×10^{-9}
	PULSE TRAIN η: "DUTY CYCLE"	$V_m\sqrt{\eta}$	$V_m\eta$	$\frac{1}{\sqrt{\eta}}$	$\frac{1}{\sqrt{\eta}}$
	η / MARK/SPACE 1 / ∞ 0.25 / 0.3333 0.0625 / 0.0667 0.0156 / 0.0159 0.01 / 0.0101	V_m $0.5V_m$ $0.25V_m$ $0.125V_m$ $0.1V_m$	V_m $0.25V_m$ $0.0625V_m$ $0.0156V_m$ $0.01V_m$	1 2 4 8 10	1 2 4 8 10

MODULATION/DEMODULATION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecutre with accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication.

Often in physical processes, it is necessary to determine the amplitude of a very small signal whose phase and frequency is known. In addition, the signal may be masked by broadband noise or dc interference. Some specific instances where this type of signal detection is required include sonar reception, LVDT demodulation, inductive or capacitive bridges, chopped photodetectors, and resistive bridges where a large amount of dc interference exists. The AD630 can extract these tiny signals from the background noise by switching between positive and negative gain each half cycle. This synchronous gain switching rectifies the signal of interest and produces a dc output proportional to the signal amplitude. Other signal components that are of a different frequency (including dc offset) are chopped to an ac frequency that can be filtered out with a simple low pass filter.

DEFINITIONS OF SPECIFICATIONS

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Crest Factor (a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error,* and *settling time.*

Full-power response is the maximum frequency at which the multiplier can produce full-scale voltage into its rated load without noticeable distortion.

Settling time. for the product of a ±10V step and 10Vdc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Slew(ing) rate is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-signal amplitude error is defined in relation to the frequency at which the amplitude response, or scale factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Small-signal bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

Vector error is the most-sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.

Filter Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for ±3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal 30% of reading. It is a function of amplitude.

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

Log-Conformity Error When the parameters have been adjusted to compensate for offset, scale-factor, and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the multiplier may improve small-signal resolution significantly.

Offset Current (I_{OS}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Power Supply: Power-supply range for specified performance, power-supply range for operation, and quiescent current drain. Note that the AD536 can be operated from single or dual supplies.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator, or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements ($T_H - 25^\circ C$), ($25^\circ C - T_L$), when measured.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

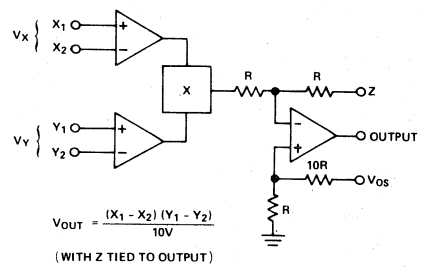
Internally Trimmed Integrated Circuit Multiplier

AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For (X_1-X_2) $(Y_1-Y_2)/10V$ Transfer Function
- Monolithic Construction, Low Cost

APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications

AD532 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

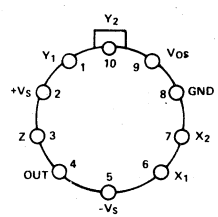
FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as $XY/10V$, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

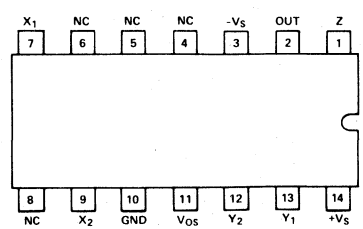
The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of -55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP.

AD532H



TO-100
TOP VIEW

AD532D



TO-116
TOP VIEW

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$, V_{OS} Grounded)

Model	AD532J Min	AD532J Typ	AD532J Max	AD532K Min	AD532K Typ	AD532K Max	AD532S Min	AD532S Typ	AD532S Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error ($-10V \leq X, Y \leq +10V$)		± 1.5	**± 2.0**		± 0.7	**± 1.0**		± 0.5	**± 1.0**	%
T_A = min to max		± 2.5			± 1.5				**± 4.0**	%
Total Error vs Temperature		± 0.04			± 0.03			± 0.01	± 0.04	%/°C
Supply Rejection ($\pm 15V \pm 10$)		± 0.05			± 0.05			± 0.05		%/%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		± 0.8			± 0.5			± 0.5		%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		± 0.3			± 0.2			± 0.2		%
Feedthrough, X (Y Nulled, X = 20V pk-pk 50Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20V pk-pk 50Hz)		30	**15**		25	**80**		25	**80**	mV
Feedthrough vs. Temp.		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		± 0.25			± 0.25			± 0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 pk-pk)		45			45			45		V/μs
Settling Time (to 2%, ΔV_{OUT} = 20V)		1			1			1		μs
NOISE										
Wideband Noise f = 5Hz to 10kHz		0.6			0.6			0.6		mV (rms)
f = 5Hz to 5MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	± 10	± 13		± 10	± 13		± 10	± 13		V
Output Impedance (f ≤ 1kHz)		1			1			1		Ω
Output Offset Voltage		± 40				**± 30**			**± 30**	mV
Output Offset Voltage vs. Temp.		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		± 2.5			± 2.5			± 2.5		mV/%
INPUT AMPLIFIERS (X, Y and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		± 10			± 10			± 10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	μA
X, Y Inputs T_{min} to T_{max}		10			8			8		μA
Z Input		± 10			± 5	**± 15**		± 5	**± 15**	μA
Z Input T_{min} to T_{max}		± 30			± 25			± 25		μA
Offset Current		± 0.3			± 0.1			± 0.1		μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$		
Total Error										
($V_X = -10V$, $-10V \leq V_Z \leq +10V$)		± 2			± 1			± 1		%
($V_X = -1V$, $-10V \leq V_Z \leq +10V$)		± 4			± 3			± 3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$		
Total Error		± 0.8			± 0.4			± 0.4		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function		$(X_1-X_2)^2/10V$			$(X_1-X_2)^2/10V$			$(X_1-X_2)^2/10V$		
Total Error ($0V \leq V_Z \leq 10V$)		± 1.5			± 1.0			± 1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		± 15			± 15			± 15		V
Operating	**± 10**		**± 18**	**± 10**		**± 18**	**± 10**		**± 22**	V
Suply Current										
Quiescent		**4**	**6**		**4**	**6**		**4**	**6**	mA

NOTE

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown on the first page, and the complete schematic in Figure 1. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1-X_2)(Y_1-Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{os} in critical applications . . . . otherwise the V_{os} pin should be grounded.

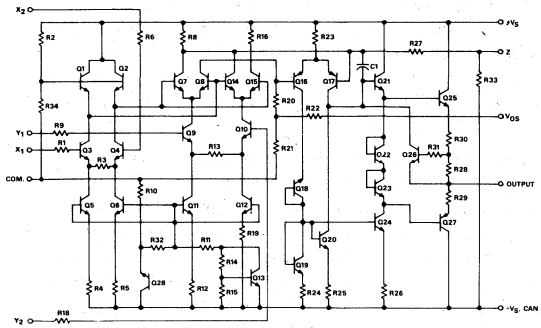


Figure 1. AD532 Schematic Diagram

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ORDERING GUIDE

Model	Package Option[1]	Max Mult Error	Temperature Range
AD532JH	TO–100	±2.0%	0 to +70°C
AD532JD	TO–116 Style (D14A)	±2.0%	0 to +70°C
AD532KH	TO–100	±1.0%	0 to +70°C
AD532KD	TO–116 Style (D14A)	±1.0%	0 to +70°C
AD532SH	TO–100	±1.0%	-55°C to +125°C
AD532SD	TO–116 Style (D14A)	±1.0%	-55°C to +125°C

[1] See Section 19 for package outline information.

AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output amp as shown in Figure 12. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwdith and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 2 and 3 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 3 the sine wave amplitude is 20V (p-p).

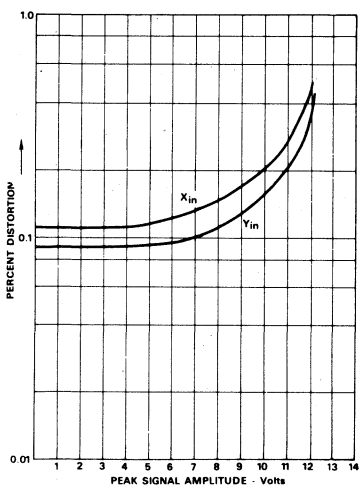


Figure 2. Percent Distortion vs. Input Signal

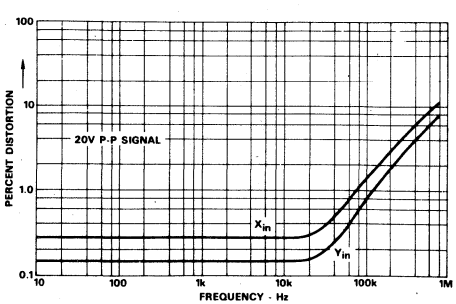


Figure 3. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 4. It is measured for the condition $V_X = 0$, $V_Y = 20V(p\text{-}p)$ and $V_Y = 0$, $V_X = 20V(p\text{-}p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

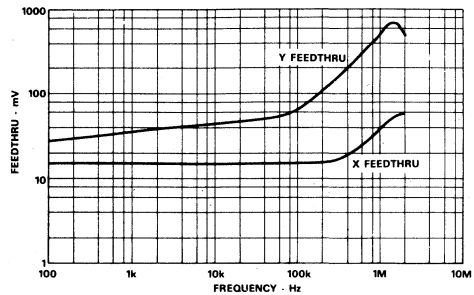


Figure 4. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 5. It is measured with $X_1 = X_2 = 20V$ (p-p), $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p\text{-}p)$, $(X_1-X_2) = \pm 10V$ dc.

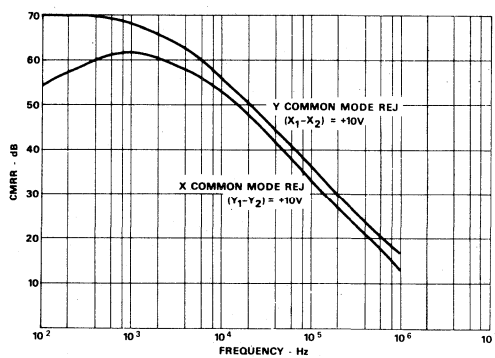


Figure 5. CMRR vs. Frequency

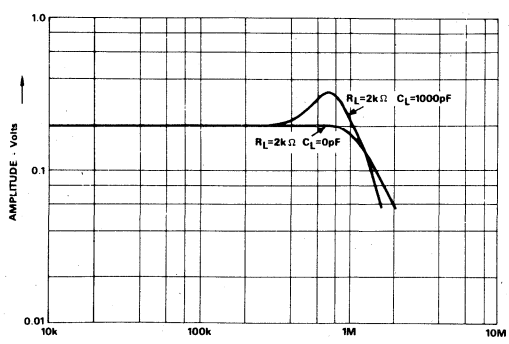


Figure 6. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 6. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 7.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

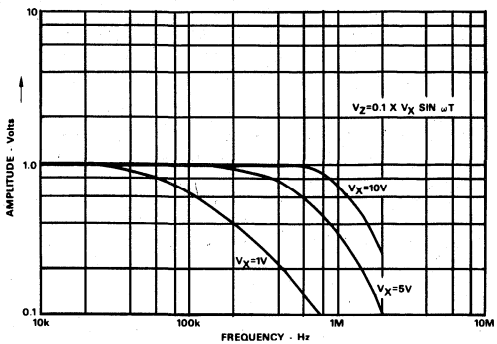


Figure 7. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 8. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

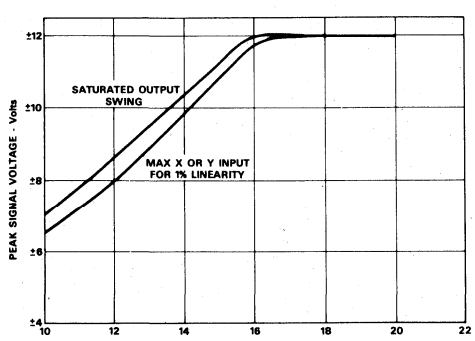


Figure 8. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 9.

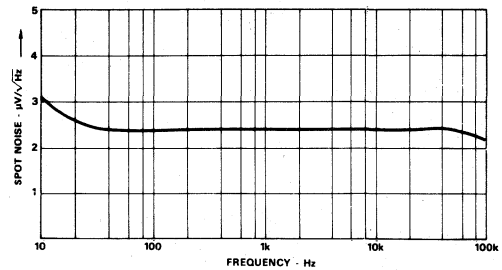


Figure 9. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

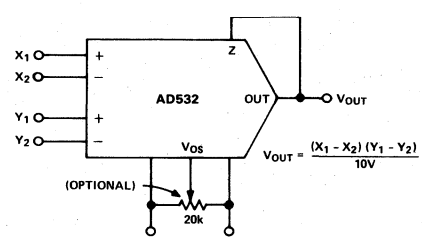


Figure 10. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 10. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see first page). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

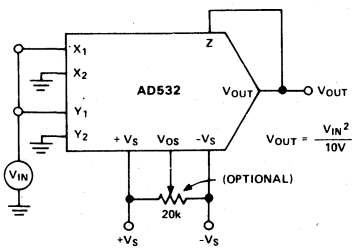


Figure 11. Squarer Connection

The squaring circuit in Figure 11 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

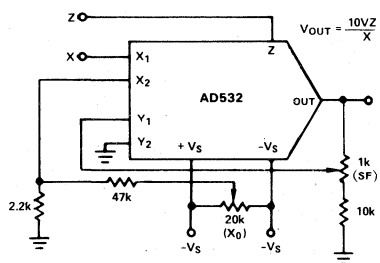


Figure 12. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 12. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to -10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leqslant |(X_1-X_2)| \leqslant 10V$. The voltage offset adjust (V_{os}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

SQUARE ROOT

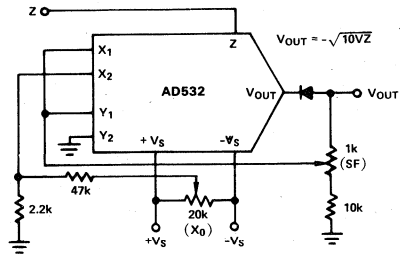


Figure 13. Square Rooter Connection

The connections for square root mode are shown in Figure 13. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain -1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

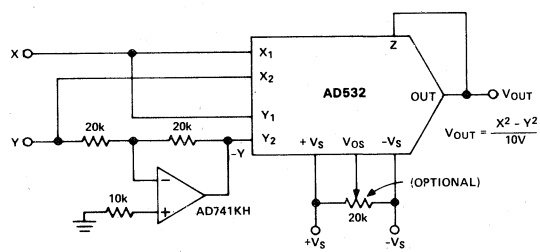


Figure 14. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 14, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	±10V	+10V	−10V
X_o (Offset)	−1V	+0.1V	±10V	+0.1V	−1V

Repeat if required.

ANALOG DEVICES

Low Cost IC Multiplier,Divider,Squarer,Square Rooter

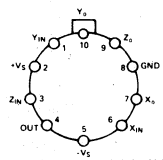
AD533

FEATURES

- **Simplicity of Operation: Only Four External Adjustments**
- **Max 4-Quadrant Error Below 0.5% (AD533L)**
- **Low Temperature Drift: 0.01%/°C (AD533L)**
- **Multiplies, Divides, Squares, Square Roots**

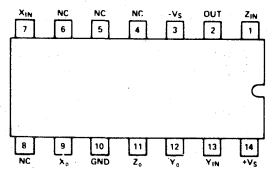
AD533 PIN CONFIGURATIONS

AD533H



TO-100
TOP VIEW

AD533D



TO-116
TOP VIEW

6

PRODUCT DESCRIPTION

The Analog Devices AD533 is a low cost integrated circuit multiplier comprised of a transconductance multiplying element, stable reference, and output amplifier on a monolithic silicon chip. Specified accuracy is easily achieved by the straight-forward adjustment of feedthrough, output zero, and gain trim pots. The AD533 multiplies in four quadrants with a transfer function of XY/10V, divides in two quadrants with a 10VZ/X transfer function, and square roots in one quadrant with a transfer function of $-\sqrt{10VZ}$. Several levels of accuracy are provided: the AD533J, AD533K, and AD533L, for 0 to +70°C operation, are specified for maximum multiplying errors of 2%, 1%, and 0.5% respectively at +25°C. The AD533S, for operation from -55°C to +125°C, is guaranteed for a maximum 1% multiplying error at +25°C. The maximum error specification is a true measure of overall accuracy since it includes the effects of offset voltage, feedthrough, scale factor, and nonlinearity in all four quadrants.

The low drift design of the AD533 insures that high accuracy is maintained with variations in temperature. The op amp output provides ±10 volts at 5mA, and is fully protected against short circuits to ground or either supply voltage: all inputs are fully protected against over-voltage transients with internal series resistors. The devices provide excellent ac performance, with typical small signal bandwidth of 1.0MHz, full power bandwidth of 750kHz, and slew rate of 45V/μs.

The low cost and simplicity of operation of the AD533 make it especially well suited for use in such widespread applications as modulation and demodulation, automatic gain control and phase detection. Other applications include frequency discrimination, rms computation, peak detection, voltage controlled oscillators and filters, function generation, and power measurements.

All models are available in the hermetically sealed TO-100 metal can and TO-116 ceramic DIP packages.

SPECIFICATIONS (typical @ +25°C, externally trimmed and V_S = ±15V dc unless otherwise specified)

PARAMETER	CONDITIONS	AD533J	AD533K	AD533L	AD533S
ABSOLUTE MAX RATINGS					
Internal Power Dissipation		500mW	*	*	*
Input Voltage[1]					
X_{in}, Y_{in}, Z_{in}, X_O, Y_O, Z_O		$\pm V_S$	*	*	*
Rated Operating Temp Range		0 to +70°C	*	*	−55°C to +125°C
Storage Temp Range		−65°C to +150°C	*	*	*
Output Short Circuit	To Ground	Indefinite	*	*	*
MULTIPLIER SPECIFICATIONS					
Transfer Function		XY/10V	*	*	*
	Untrimmed	XY/6V max [XY/10V min]	*	*	*
Total Error (of full scale)		±2.0% max	±1.0% max	±0.5% max	±1.0% max
	T_A = min to max	±3.0%	±2.0%	±1.0%	±1.5%
vs. Temperature	T_A = min to max	±0.04%/°C	±0.03%/°C	±0.01%/°C	±0.01%/°C
Nonlinearity					
X Input	$V_X = V_O$ = 20V(p-p)	±0.8%	±0.5%	**	**
Y Input	$V_Y = V_O$ = 20V(p-p)	±0.3%	±0.2%	**	**
Feedthrough					
X Input	V_X = 20V(p-p), V_Y = 0, f = 50Hz	200mV (p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
Y Input	V_Y = 20V(p-p), V_X = 0, f = 50Hz	200mV(p-p) max	150mV(p-p) max	50mV(p-p) max	100mV (p-p) max
DIVIDER SPECIFICATIONS					
Transfer Function		10VZ/X	*	*	*
	Untrimmed	10VZ/X max [6VZ/X min]	*	*	*
Total Error (of full scale)	V_X = −10V dc, V_Z = ±10V dc	±1.0%	±0.5%	±0.2%	±0.5%
	V_X = −1V dc, V_Z = ±10V dc	±3.0%	±2.0%	±1.5%	±2.0%
SQUARER SPECIFICATIONS					
Transfer Function		$X^2/10V$	*	*	*
	Untrimmed	$X^2/6V$ max [$X^2/10V$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
SQUARE ROOTER SPECIFICATIONS					
Transfer Function		$-\sqrt{10VZ}$	*	*	*
	Untrimmed	$-\sqrt{10VZ}$ max [$-\sqrt{6VZ}$ min]	*	*	*
Total Error (of full scale)		±0.8%	±0.4%	±0.2%	±0.4%
INPUT SPECIFICATIONS					
Input Resistance					
X Input		10MΩ	*	*	*
Y Input		6MΩ	*	*	*
Z Input		36kΩ	*	*	*
Input Bias Current					
X, Y Inputs		3μA	7.5μA max	5μA max	7.5μA max
Z Input		±25μA	*	*	*
X, Y Inputs	T_A = min to max	12μA	10μA	7μA	7μA
Z Input	T_A = min to max	±35μA	*	*	*
Input Voltage	T_A = min to max				
V_X, V_Y, V_Z	For Rated Accuracy	±10V	*	*	*
DYNAMIC SPECIFICATIONS					
Small Signal, Unity Gain		1.0MHz	*	*	*
Full Power Bandwidth		750kHz	*	*	*
Slew Rate		45V/μs	*	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*	*
Sm Sig 1% Vector Error	0.5° phase shift	5kHz	*	*	*
Settling Time	±10V step	1μs to 2%	*	*	*
Overload Recovery		2μs to 2%	*	*	*
OUTPUT AMPLIFIER SPECIFICATIONS					
Output Impedance		100Ω	*	*	*
Output Voltage Swing	T_A = min to max				
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min	*	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*	*
Output Offset Voltage		Trimmable To Zero	*	*	*
vs. Temperature	T_A = min to max	0.7mV/°C	*	*	*
POWER SUPPLY SPECIFICATIONS					
Supply Voltage	Rated Performance	±15V	*	*	*
	Operating	±15V to ±18V	±10V to ±18V	±10V to ±18V	±10V to ±22V
Supply Current	Quiescent	±6mA max	*	*	*
Power Supply Variation	*Includes* Effects of Recommended Null Pots				
Multiplier Accuracy		±0.5%/%	*	*	*
Output Offset		±10mV/%	*	*	*
Scale Factor		±0.1%/%	*	*	*
Feedthrough		±10mV/%	*	*	*

NOTES

[1] Max input voltage is zero when supplies are turned off.

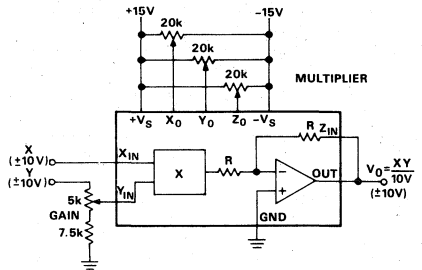
*Specifications same as AD533J.

**Specifications same as AD533K.

Specifications subject to change without notice.

MULTIPLIER

Multiplier operation is accomplished by closing the loop around the internal op amp with the Z input connected to the output. The X_O null pot balances the X input channel to minimize Y feedthrough and similarly the Y_O pot minimizes the X feedthrough. The Z_O pot nulls the output op amp offset voltage and the gain pot sets the full scale output level.



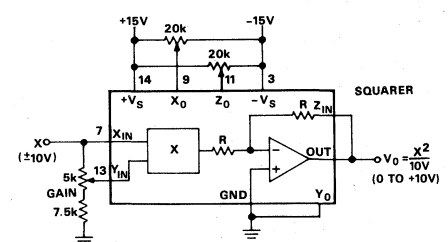
TRIM PROCEDURES

1. With X = Y = 0 volts, adjust Z_O for 0V dc output.
2. With Y = 20 volts p-p (at f = 50Hz) and X = 0V, adjust X_O for minimum ac output.
3. With X = 20 volts p-p (at f = 50Hz) and Y = 0V, adjust Y_O for minimum ac output.
4. Readjust Z_O for 0V dc output.
5. With X = +10V dc and Y = 20 volts p-p (at f = 50Hz), adjust gain for output = Y_{in}.

NOTE: For best accuracy over limited voltage ranges (e.g., ±5V), gain and feedthrough adjustments should be optimized with the inputs in the desired range, as linearity is considerably better over smaller ranges of input.

SQUARER

Squarer operation is a special case of multiplier operation where the X and Y inputs are connected together and two quadrant operation results since the output is always positive. When the X and Y inputs are connected together, a composite offset results which is the algebraic sum of the individual offsets which can be nulled using the X_O pot alone.

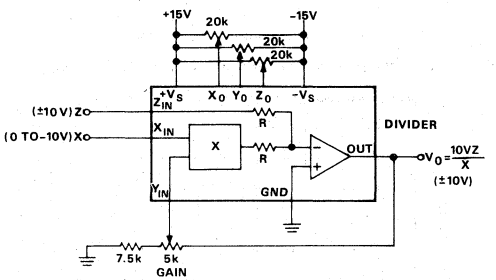


TRIM PROCEDURES

1. With X = 0 volts, adjust Z_O for 0V dc output.
2. With X = +10V dc, adjust gain for +10V dc output.
3. Reverse polarity of X input and adjust X_O to reduce the output error to ½ its original value, readjust the gain to take out the remaining error.
4. Check the output offset with input grounded. If nonzero, repeat the above procedure until no errors remain.

DIVIDER

The divide mode utilizes the multiplier in a fed-back configuration where the Y input now controls the feedback factor. With X = full scale, the gain (V_O/Z) becomes unity after trimming. Reducing the X input reduces the feedback around the op amp by a like amount, thereby increasing the gain. This reciprocal relationship forms the basis of the divide mode. Accuracy and bandwidth decrease as the denominator decreases.

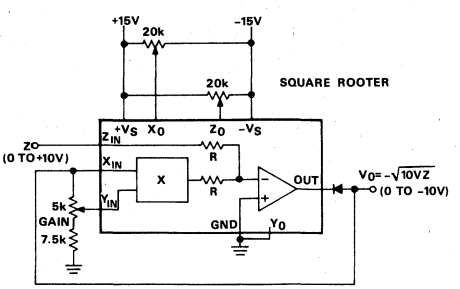


TRIM PROCEDURES

1. Set all pots at mid-scale.
2. With Z = 0V, trim Z_O to hold the output constant, as X is varied from −10V dc through −1V dc.
3. With Z = 0V, X = −10V dc, trim Y_O for 0V dc.
4. With Z = X or −X, trim X_O for the minimum worst-case variations as X is varied from −10V dc to −1V dc.
5. Repeat steps 2 and 3 if step 4 required a large initial adjustment.
6. With Z = X or −X, trim the gain for the closest average approach to ±10V dc output as X is varied from −10V dc to −3V dc.

SQUARE ROOTER

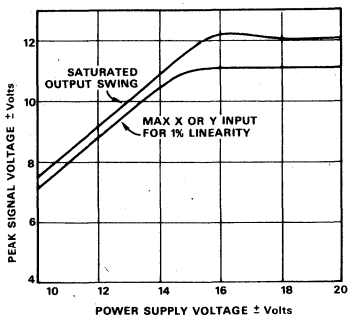
This mode is also a fed-back configuration with both the X and Y inputs tied to the op amp output through an external diode to prevent latchup. Accuracy, noise and frequency response are proportional to $\sqrt{Z}$, which implies a wider usable dynamic range than the divide mode.



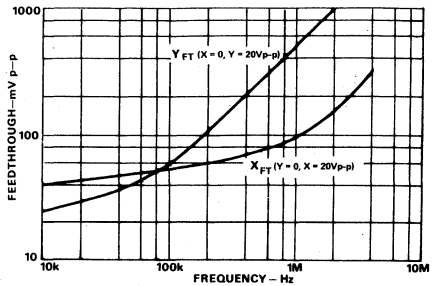
TRIM PROCEDURES

1. With Z = +0.1V dc, adjust Z_O for Output = −1.0V dc.
2. With Z = +10.0V dc, adjust gain for Output = −10.0V dc.
3. With Z = +2.0V dc, adjust X_O for Output = −4.47 ±0.1V dc.
4. Repeat steps 2 and 3, if necessary. Repeat step 1.

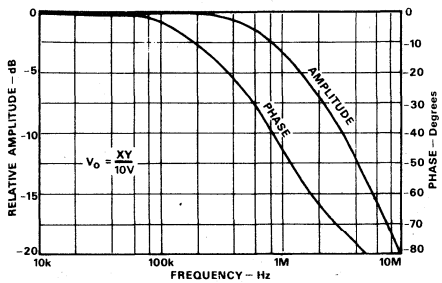
TYPICAL PERFORMANCE CHARACTERISTICS



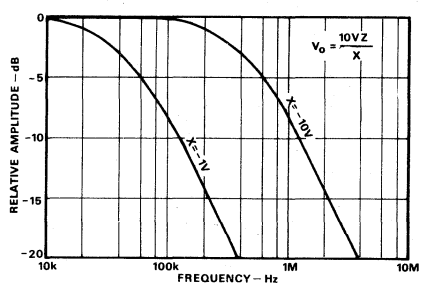
Allowable Signal Swing vs. Supply Voltage



Feedthrough vs. Frequency



Closed Loop Frequency and Phase Response



Divide Mode Frequency Response

ORDERING GUIDE

MODEL	MULT. ERROR (Max @ +25°C)	TEMP. RANGE	ORDER NUMBER	PACKAGE OPTIONS[1]
AD533J	±2.0%	0 to +70°C	AD533JH	TO-100
			AD533JD	TO-116 Style (D14A)
AD533K	±1.0%	0 to +70°C	AD533KH	TO-100
			AD533KD	TO-116 Style (D14A)
AD533L	±0.5%	0 to +70°C	AD533LH	TO-100
			AD533LD	TO-116 Style (D14A)
AD533S	±1.0%	−55°C to +125°C	AD533SH	TO-100
			AD533SD	TO-116 Style (D14A)

[1] See Section 19 for package outline information.

ANALOG DEVICES

Internally Trimmed Precision IC Multiplier

AD534

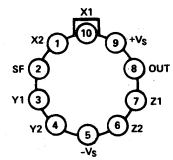
FEATURES

Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

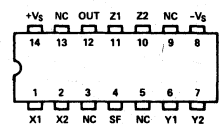
APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters

AD534 PIN CONFIGURATIONS



TO-100



TO-116

TOP VIEW

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS ($T_A = +25°C$, $\pm V_S = 15V$, $R \geq 2k\Omega$)

Model	AD534J			AD534K			AD534L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.05	**0.2**	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \leq Z \leq +10V$)		±0.75			±0.35			±0.2		%
(X − 1V, $-1V \leq Z \leq +1V$)		±2.0			±1.0			±0.8		%
($0.1V \leq X \leq 10V$, $-10V \leq Z \leq 10V$)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{100}+Z_2$			$\frac{(X_1-X_2)^2}{100}+Z_2$			$\frac{(X_1-X_2)^2}{100}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+Y_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	**±8**		**±18**	**±8**		**±18**	**±8**		**±18**	V
Supply Current										
Quiescent		**4**	**6**		**4**	**6**		**4**	**6**	mA
PACKAGE OPTIONS[6]										
H: TO-100 Package		**AD534JH**			**AD534KH**			**AD534LH**		
D: TO-116 Package (D14A)		**AD534JD**			**AD534KD**			**AD534LD**		

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).

[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3V.

[5]See functional block diagram for definition of sections.

[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S			AD534T			Units
	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \le X, Y \le +10V$)			**±1.0**			**±0.5**	%
T_A = min to max			**±2.0**			**±1.0**	%
Total Error vs Temperature			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02				±0.005	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift			**500**			**300**	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1.0			1.0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z			**500**			**300**	µV/°C
CMRR	**60**	80		**70**	90		dB
Bias Current		0.8	2.0		0.8	2.0	µA
Offset Current		0.1	**2.0**		0.1	**2.0**	µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \le Z \le +10V$)		±0.75			±0.75		%
(X = 1V, $-1V \le Z \le +1V$)		±2.0			±2.0		%
($0.1V \le X \le 10V$, $-10V \le Z \le 10V$)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2+Z_2}{10V}$			$\frac{(X_1-X_2)^2+Z_2}{10V}$		
Total Error ($-10V \le X \le 10V$)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \le Z \le 10V$)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	**±8**		**±22**	**±8**		**±22**	V
Supply Current							
Quiescent		4	**6**		4	6	mA
PACKAGE OPTIONS[6]							
H: TO-100 Package		**AD534SH**			**AD534TH**		
D: TO-116 Package (D14A)		**AD534SD**			**AD534TD**		

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections.
[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

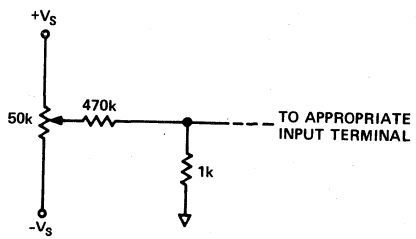
Using the AD534

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

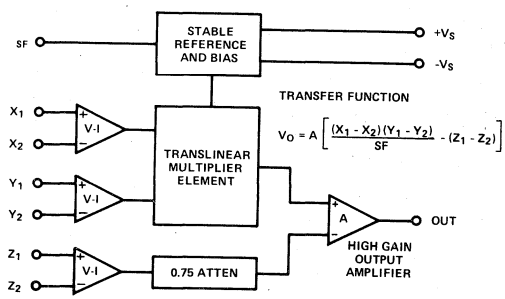


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

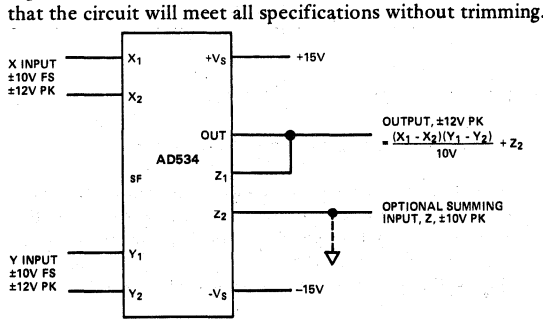


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

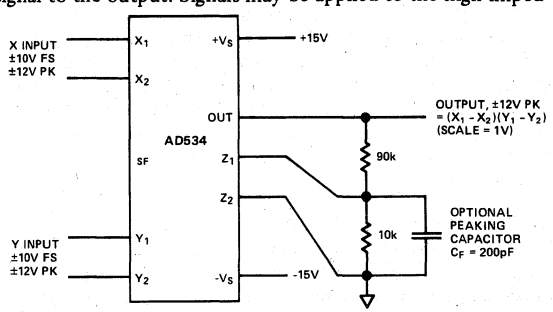


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

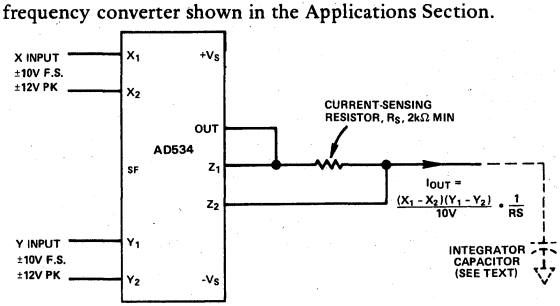


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

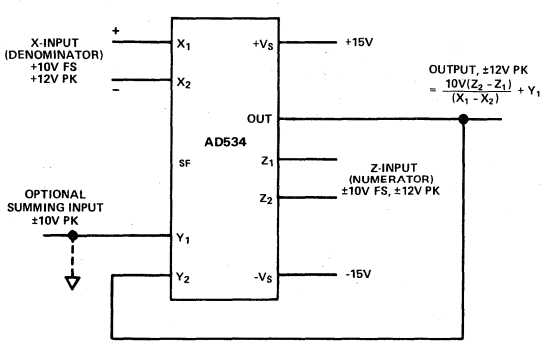


Figure 5. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

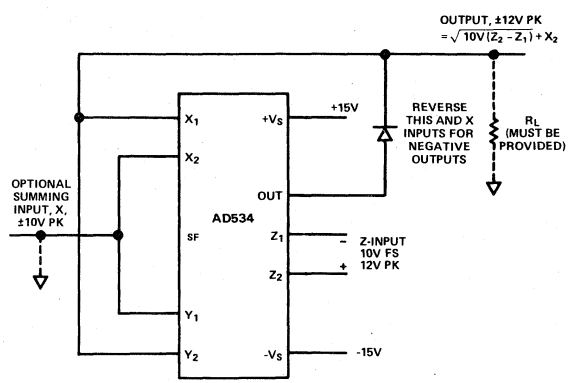


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

*See the AD535 Data Sheet for more details.

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few. These applications along with many other such "idea stimulators" are described in detail in the *Multiplier Application Guide*, available upon request from Analog Devices.

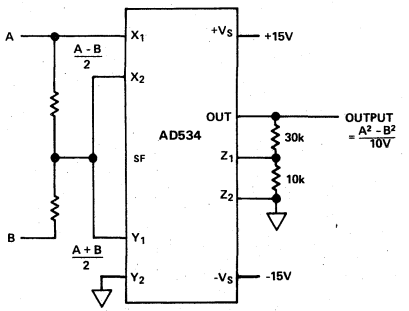
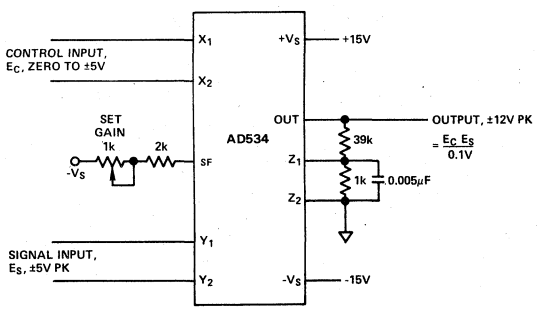
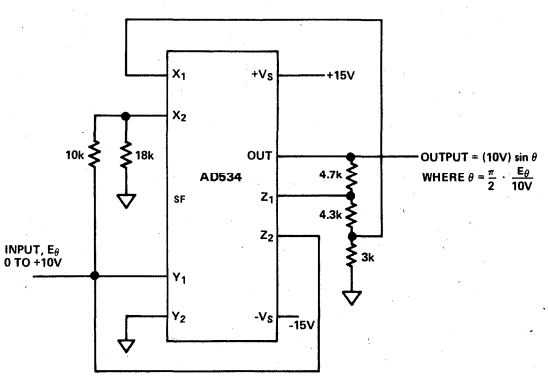


Figure 7. Difference-of-Squares



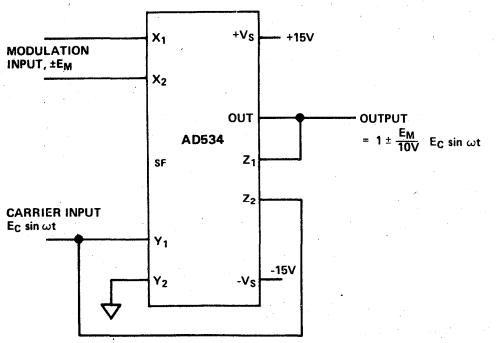
NOTES:
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60μV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



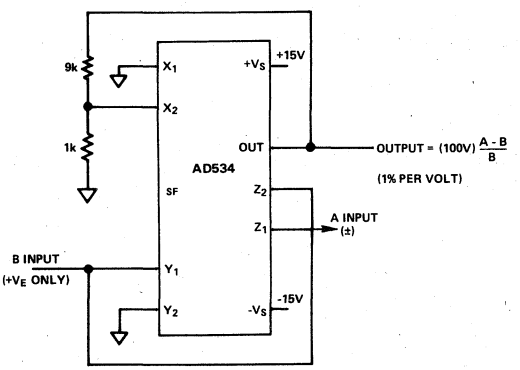
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION. OPERATION FROM A SINGLE SUPPLY IS POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 11. Percentage Computer

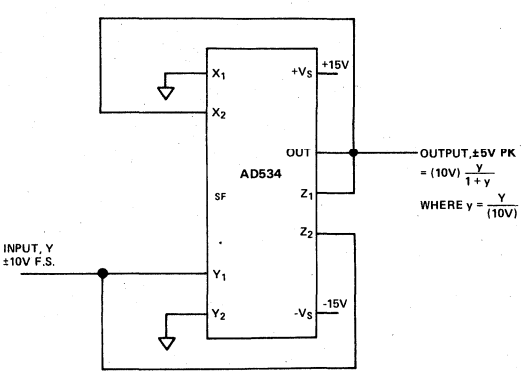
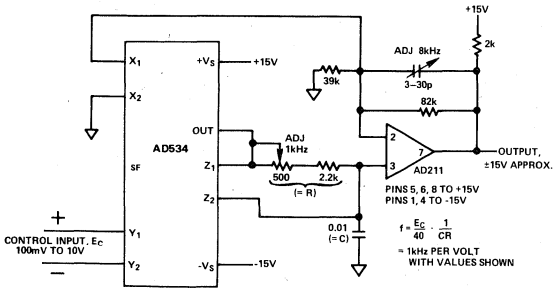


Figure 12. Bridge-Linearization Function



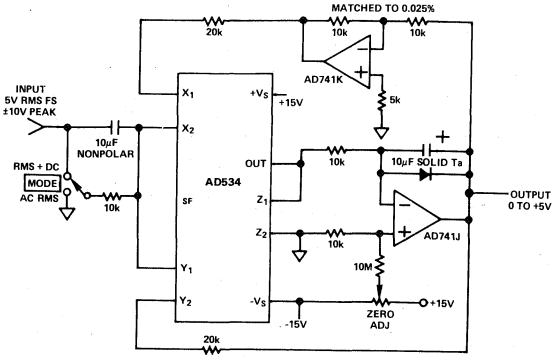
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE).

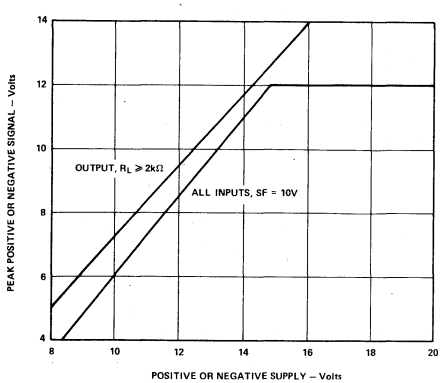
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

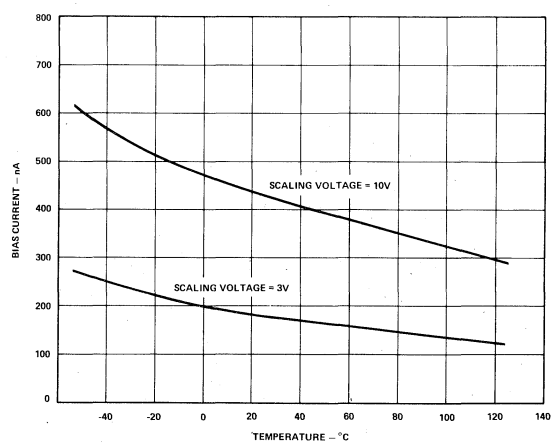
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

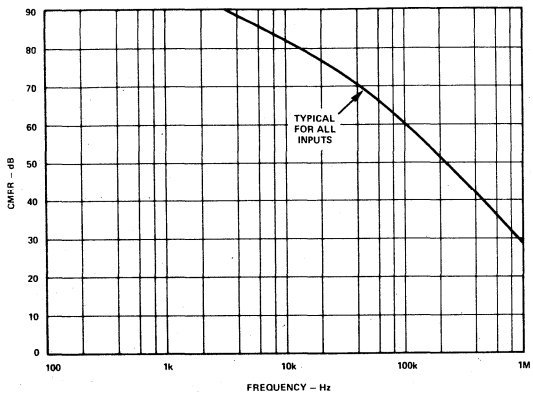
Typical Performance Curves (typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



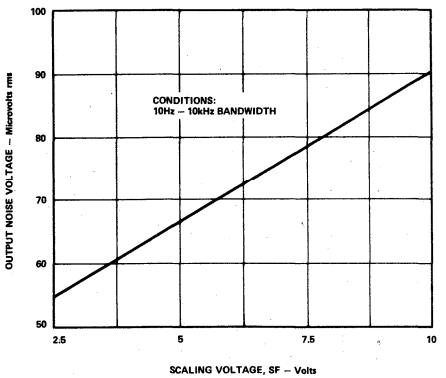
Curve 1. Input/Output Signal Range Vs. Supply Voltages



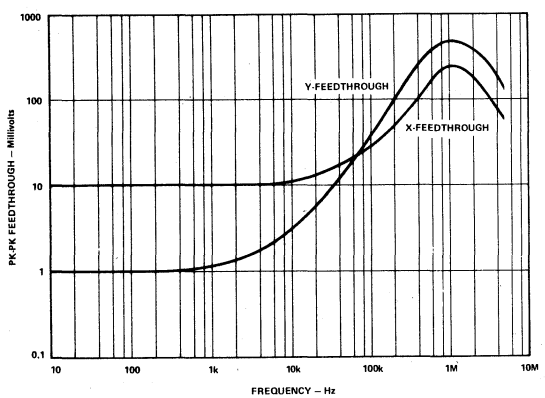
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



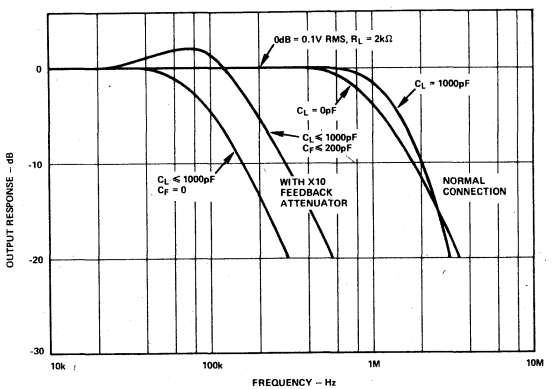
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



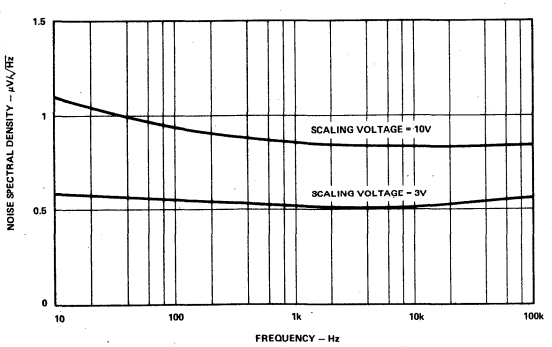
Curve 6. Wideband Noise Vs. Scaling Voltage



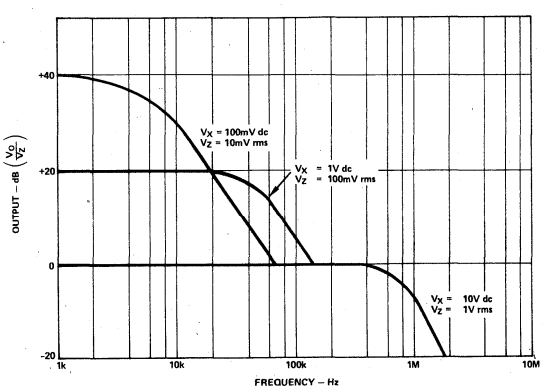
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response Vs. Divider Denominator Input Voltage

ANALOG DEVICES

Internally Trimmed Integrated Circuit Divider

AD535

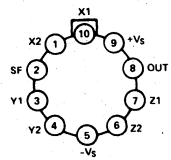
FEATURES

Pretrimmed to ±0.5% max Error, 10:1 Denominator Range (AD535K)
±2.0% max Error, 50:1 Denominator Range (AD535K)
All Inputs (X, Y and Z) Differential

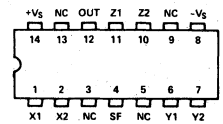
APPLICATIONS

General Analog Signal Processing
Differential Ratio and Percentage Computations
Precision AGC Loops
Square-Rooting

AD535 PIN CONFIGURATIONS



TO-100
(TOP VIEW)



TO-116
(TOP VIEW)

PRODUCT DESCRIPTION

The AD535 is a monolithic laser-trimmed two-quadrant divider having performance specifications previously found only in expensive hybrid or modular products. A maximum divider error of ±0.5% is guaranteed for the AD535K without any external trimming over a denominator range of 10:1; ±2.0% max error over a range of 50:1. A maximum error of ±1% over the 50:1 denominator range is guaranteed with the addition of two external trims. The AD535 is the first divider to offer fully differential, high impedance operation on all inputs, including the z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00; by means of an external resistor, this can be reduced by any amount down to 3.

The extraordinary versatility and performance of the AD535 recommend it as the first choice in many divider and computational applications. Typical uses include square-rooting, ratio computation, "pin-cushion" correction and AGC loops. The device is packaged in a hermetically sealed, 10-pin TO-100 can or 14-pin TO-116 DIP and made available in a ±1% max error version (J) and a ±0.5% max error version (K). Both versions are specified for operation over the 0 to +70°C temperature range.

PRODUCT HIGHLIGHTS

1. Laser trimming at the wafer stage enables the AD535 to provide high accuracies without the addition of external trims (±0.5% max error over a 10:1 denominator range for the AD535K).
2. Improved accuracies over a wider denominator range are possible with only two external trims (±0.5% max error over a 20:1 denominator range for the AD535K).
3. Differential inputs on the X, Y and Z input terminals enhance the AD535's versatility as a generalized analog computational circuit.
4. Monolithic construction permits low cost and, at the same time, increased reliability.

SPECIFICATIONS (V_S = ±15V, $R_L \geq 2k\Omega$, T_A = +25°C unless otherwise stated)

PARAMETER	CONDITIONS	AD535J	AD535K
TRANSFER FUNCTION	Figure 2	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*
TOTAL ERROR[1]	No External Trims, Figure 2		
	$1V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	1.0% max	0.5% max
	$0.2V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	5.0% max	2.0% max
	With External Trims, Figure 5		
	$0.5V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	1.0% max	0.5% max
	$0.2V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	2.0% max	1.0% max
TEMPERATURE COEFFICIENT	$1V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	0.01%/°C typ	*
	$0.5V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	0.02%/°C typ	*
	$0.2V \leq X \leq 10V$, $Z \leq \lvert X \rvert$	0.05%/°C typ	*
SUPPLY RELATED	$1V \leq X \leq 10V$	0.1%/V typ	*
Error	$0.5V \leq X \leq 10V$	0.2%/V typ	*
V_S = ±14V to ±16V	$0.2V \leq X \leq 10V$	0.5%/V typ	*
SQUARE ROOTER	No External Trims, Figure 11		
TOTAL ERROR[1]	$1V \leq Z \leq 10V$	0.4% typ	*
	$0.2V \leq Z \leq 10V$	0.7% typ	*
NOISE[2]	X = 0.2V, f = 10Hz to 10kHz	4.5mV rms typ	*
BANDWIDTH	X = 0.2V	20kHz typ	*
INPUT AMPLIFIERS[3]			
CMRR	f = 50Hz, 20V p-p	60dB min	*
Bias Current		2.0μA max	*
Offset Current		0.1μA typ	*
Differential Resistance		10MΩ typ	*
OUTPUT AMPLIFIER[3]			
Open-Loop Gain	f = 50Hz	70dB typ	*
Small Signal Gain-Bandwidth	V_{OUT} = 0.1V rms	1MHz typ	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz typ	*
Output Voltage Swing	T_{min} to T_{max}	±11V min	*
Slew Rate	V_{OUT} = 20V p-p	20V/μs typ	*
Settling Time	V_{OUT} = 20V ±1%	2μs typ	*
Output Impedance	Unity Gain, f ≤ 1kHz	0.1Ω typ	*
Wide-band Noise	f = 10Hz to 5MHz	1mV rms typ	*
	f = 10Hz to 10kHz	90μV rms typ	*
OUTPUT SHORT CURRENT	T_{min} to T_{max}, R_1 = 0	30mA	*
POWER SUPPLIES			
Rated Performance		±15V	*
Operating		±8V min, ±18V max	*
Supply Current	Quiescent	6mA max	*
PACKAGE OPTIONS[4]			
H: TO-100		AD535JH	AD535KH
D: TO-116 Style (D14A)		AD535JD	AD535KD

NOTES
*Specifications same as AD535J.
[1] Figures are given as a percent of full scale (i.e. 1.0% = 100mV).
[2] Noise may be reduced as shown in Figure 14.
[3] See Figure 1 for definition of section.
[4] See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	500mW
Output Short-Circuit to Ground	Indefinite
Input Voltages, X_1, X_2, Y_1, Y_2, Z_1, Z_2	$\pm V_S$
Rated Operating Temp Range	0 to +70°C
Storage Temp Range	-65°C to +150°C
Lead Temp, 60s soldering	+300°C

FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD535. Inputs are converted to differential currents by three identical voltage to current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique with an internal scaling voltage.

The difference between XY/SF and Z is applied to the high gain output amplifier. The transfer function can then be expressed...

$$V_{OUT} = A\left[\frac{(X_1 - X_2)(Y_1 - V_{OUT})}{SF} - (Z_1 - Z_2)\right]$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite and SF will be 10V. Dividing both sides of the equation by A and solving the V_{OUT}, we get...

$$V_{OUT} = 10V\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$$

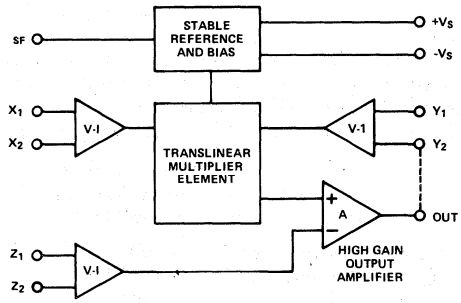


Figure 1. AD535 Functional Block Diagram

SOURCES OF ERROR

Divider error is specified as a percent of full scale (i.e. 10.00V) and consists primarily of the effects of X, Y and Z offsets and scale factor (which are trimmable) as shown in the generalized equation....

$$V_{OUT} = (SF + \Delta SF)\left[\frac{(Z_2 - Z_1) + Z_{OS}}{(X_1 - X_2) + X_{OS}}\right] + Y_1 + Y_{OS}$$

Note especially that divider error is inversely proportional to X, that is, the error increases rapidly with decreasing denominator values. Hence, the AD535 divider error is specified over several denominator ranges on previous page. (See also Figure 12, AD535 Total Error as a function of denominator values.)

Overall accuracy of the AD535 can be significantly improved by nulling out X and Z offset as described in the applications sections. Figure 13 illustrates a factor of 2 improvement in accuracy with the addition of these external trims. The remaining errors stem primarily from scale factor error and Y offsets which can be trimmed out as shown in Figure 6.

Figure 14 illustrates the bandwidth and noise relationships versus denominator voltage. Whereas noise increases with decreasing denominator, bandwidth decreases, the net result given by the expression...

$$En_{OUT}\ (\text{wideband}) = \frac{1.26}{\sqrt{\left(\frac{X}{10}\right)}}\ \text{mV rms}$$

External filtering can be added to limit output voltage noise even further. In this case...

$$En_{OUT}\ (\text{B.W. externally limited}) = \frac{0.9\sqrt{f}}{\left(\frac{X}{10}\right)}\ \text{mV rms}$$

where f = bandwidth in MHz of an external filter whose bandwidth is less than the noise bandwidth of the AD535. Table I provides calculated values of the typical output voltage noise, both filtered and unfiltered for several denominator values.

X	Noise 10Hz to 5MHz	Noise Limited by External Filtering 10Hz to 10kHz
0.2V	8.9mV rms	4.5mV rms
0.5V	5.6mV rms	1.8mV rms
1V	4.0mV rms	0.9mV rms
10V	1.3mV rms	0.09mV rms

Table I. AD535 Calculated Voltage Noise

APPLICATIONS

Figure 2 shows the standard divider connection without external trims. The denominator X, is restricted to positive values in this configuration. X, Y and Z inputs are differential with high (80dB typical) CMRR permitting the application of differential signals on X and Z (see Figure 3).

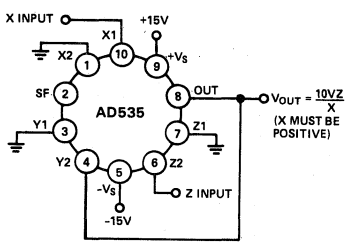


Figure 2. Divider Without External Trims

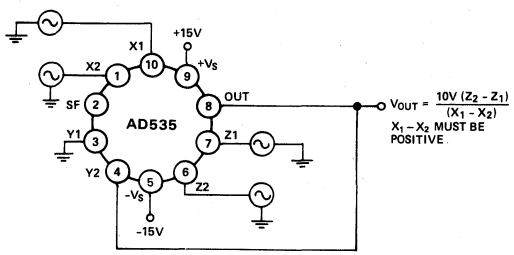


Figure 3. Differential Divider Connection

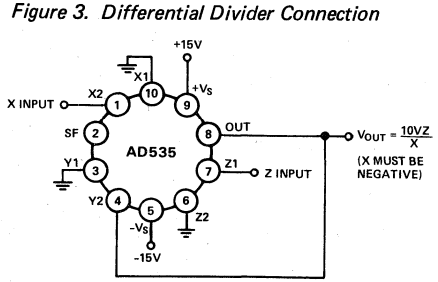


Figure 4. Divider Connection for Negative X Inputs

Negative denominator inputs are handled as shown in Figure 4. Note that in either configuration, operation is limited to two quadrants (i.e. Z is bipolar, X is unipolar).

A factor of two improvements in accuracy is possible by trimming the X and Z offsets as illustrated in Figure 5. To trim, set X to the smallest denominator value for which accurate computation is required (i.e., X = 0.2V). With Z = 0, adjust the Z_O trim for V_{OUT} = 0. Next, adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V). Finally, readjust Z_O for the best compromise at Z = +X, Z = -X and Z = O. The remaining error (Figure 13) consists primarily of scale factor error, output offset and an irreducible nonlinearity component.

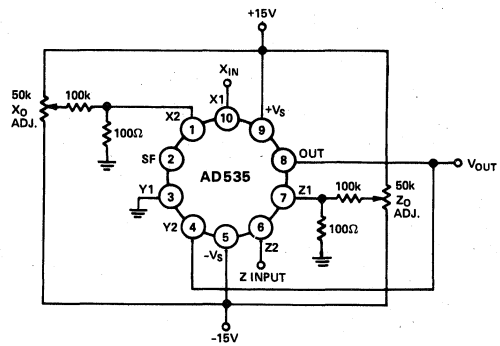


Figure 5. Precision Divider Using Two Trims

In certain applications, the user may elect to adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} ±25% using the potentiometer. Note that the peak signal is always limited to 1.25 SF (i.e. ±5V for SF = 4).

The scale factor may also be adjusted using a feedback attenuator between V_{OUT} and Y2 as indicated in Figure 6. The input signal range is unaffected using this scheme.

Scale factor and output offset error can be minimized utilizing the four trim circuit of Figure 6. Adjustment is as follows:

1. Apply X = +0.2V (or the smallest required denominator value), Z = 0 and adjust Z_O for V_{OUT} = 0.
2. Apply X = 0.2V. Then adjust the X_O trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V.)
3. Apply X = +10V, Z = 0 and adjust Y_O for V_{OUT} = 0.
4. Apply X = +10V. Then adjust the scale factor (SF) trim for the best compromise when Z = +X (V_{OUT} = +10V) and Z = -X (V_{OUT} = -10V).
5. Repeat steps 1 and 2.
6. Apply X = 0.2V. Then adjust the Z trim for the best compromise when Z = X (V_{OUT} = +10V), Z = 0 (V_{OUT} = 0) and Z = -X (V_{OUT} = -10V).

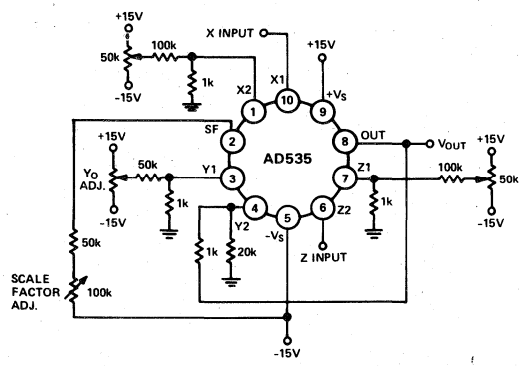


Figure 6. Precision Divider with Four External Adjustments

These trim adjustments can be made either by using two calibrated voltage sources and a DVM, or by using a differential scope, a low frequency generator, a voltage source and a precision attenuator. As shown in Figure 7, the differential scope subtracts the expected ideal output and thus displays only errors. Set the attenuation to $\frac{X}{10V}$.

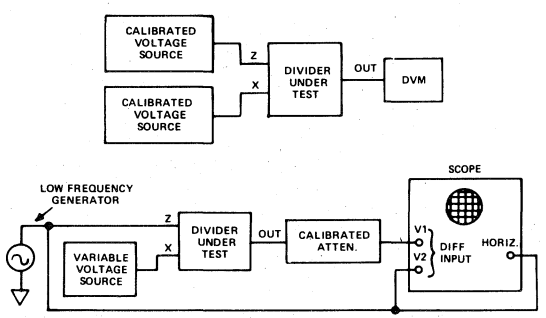


Figure 7. Alternate Trim Adjustment Set-Up

PIN-CUSHION CORRECTION

A pin-cushion corrector eliminates the distortion caused by flat screen CRT tubes. The correction equations are:

$$V_{OH} = \frac{V_{IH}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

and

$$V_{OV} = \frac{V_{IV}}{\sqrt{V_{IH}^2 + V_{IV}^2 + L^2}}$$

where: V_{OH} and V_{OV} are the horizontal and vertical output signals, respectively.

V_{IH} and V_{IV} are the horizontal and vertical input signals, respectively.

L is the length of the CRT tube.

In typical applications L (expressed in voltage) is roughly equal to full scale V_{IH} or V_{IV}. The result is that the expression, $\sqrt{(V_{IH}^2 + V_{IV}^2 + L^2)}$, varies less than 2:1 over the full range of values of V_{IH} and V_{IV}.

Major sources of divider error associated with small denominator values can thereby the minimized.

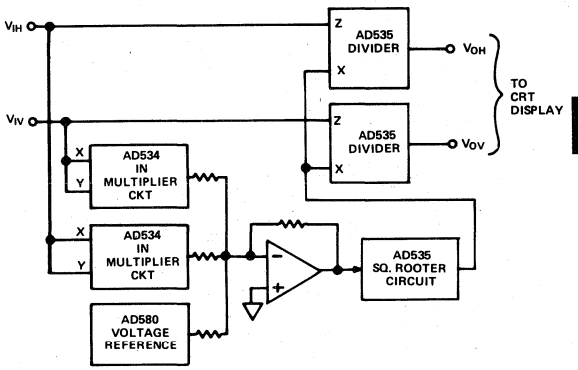


Figure 8. Pin-Cushion Corrector

Figure 9 shows an AGC loop using an AD535 divider. The AD535 lends itself naturally in this application since it is configured to provide gain rather than loss. Overall gain varies from 1 to ∞ as the denominator is servoed to maintain V_{OUT} at a constant level.

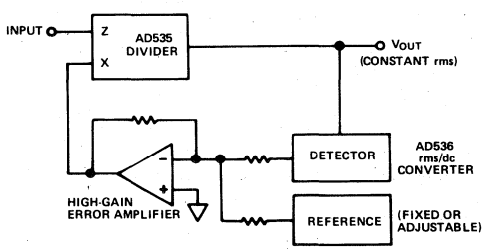


Figure 9. AGC Loop Using the AD536 rms/dc Converter as a Detector

Figure 10 shows a method for obtaining the time average as defined by:

$$\overline{X} = \frac{1}{T}\int_0^T X\,dt$$

where T is the time interval over which the average is to be taken. Conventional techniques typically provide only a crude approximation to the true time average, and furthermore, require a fixed time interval before the average can be taken. In Figure 10, the AD535 is used to divide the integrator output by the ramp generator output. Since the ramp is proportional to time, the integrator is divided by the time interval, thus allowing continuous, true time processing of signals over intervals varying by as much as 50:1.

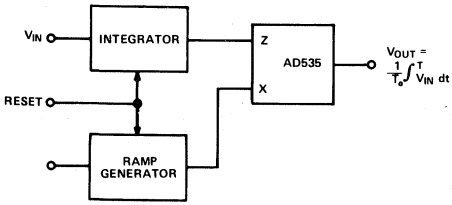


Figure 10. Time Average Computation Circuit

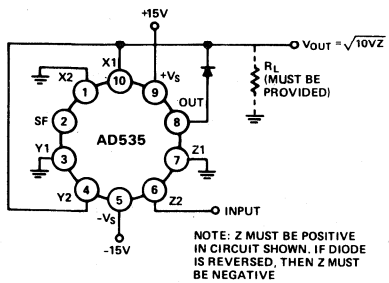


Figure 11. Square Rooter

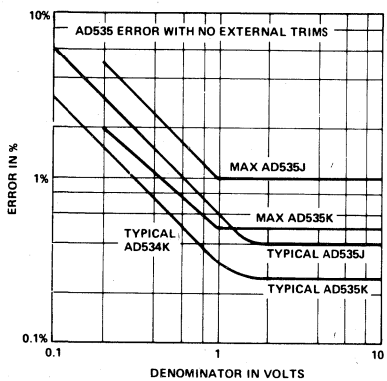


Figure 12. AD535 Error with No External Trims

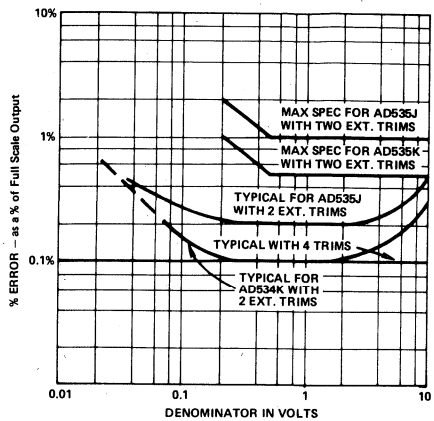


Figure 13. Errors with External Trims at 25°C

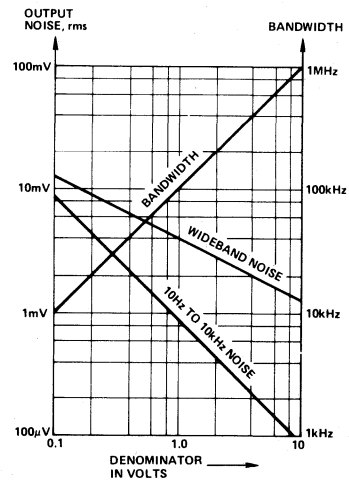


Figure 14. -3dB Bandwidth and Noise vs. Denominator

ANALOG DEVICES

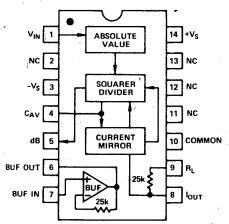
Integrated Circuit True rms-to-dc Converter

AD536A

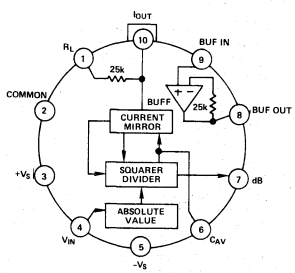
FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 300kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- -55°C to +125°C Operation (AD536AS)
- Low Cost

AD536A FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW



TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the -55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD536AJ			AD536AK			AD536AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 1)			**±5 ±0.5**			**±2 ±0.2**			**±5 ±0.5**	mV ± % of Reading
vs. Temperature, T_{min} to +70°C			±0.1 ±0.01			±0.05 ±0.005			**±0.1 ±0.005**	mV ± % of Reading
+70°C to +125°C									**±0.3 ±0.005**	mV ± % of Reading
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading
vs. Reversal Error		±0.2			±0.1			±0.2		% of Reading
Total Error, External Trim[1] (Fig. 2)		±3 ±0.3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR vs CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1.0			−1.0			−1.0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
10mV<V_{IN}≤100mV		6			6			6		kHz
100mV<V_{IN}≤1V		40			40			40		kHz
1V<V_{IN}≤7V		100			100			100		kHz
±3dB Bandwidth										
10mV<V_{IN}≤100mV		50			50			50		kHz
100mV<V_{IN}≤1V		300			300			300		kHz
1V<V_{IN}≤7V		2			2			2		MHz
AVERAGING TIME CONSTANT (Fig. 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15V Supply		±20			±20			±20		V Peak
Signal Range, ±5V Supply		±5			±5			±5		V Peak
Safe Input, All Supply Voltages		±25			±25			±25		V
Input Resistance	13.33	16.7	20.87	13.33	16.7	20.87	13.33	16.7	20.87	kΩ
Input Offset Voltage			±2			±1			±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage		±1	±2		±0.5	±1			±2	mV
vs. Temperature		±0.1			±0.1				±0.2	mV/°C
vs. Supply Voltage		±0.1			±0.1			±0.2		mV/V
Voltage Swing, ±15V Supplies	**±11**			**±11**			**±11**			V
±5V Supply	±2			±2			±2			V
Output Current	(+5mA,			(+5mA,			(+5mA,			
	−130μA)			−130μA)			−130μA)			V
Short Circuit Current		20			20			20		mA
Resistance			0.5			0.5			0.5	Ω
dB OUTPUT (Fig. 13)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	±0.6		±0.2	±0.3		±0.5		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see										
Fig. 13 for Temperature Compensation)		−0.3			−0.3			−0.35		% of Reading
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{REF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±20			±20			±20		%
Output Resistance		10^8			10^8			10^8		Ω
Voltance Compliance		$-V_S$ to ($+V_S$			$-V_S$ to ($+V_S$			$-V_S$ to ($+V_S$		
		−2.5V)			−2.5)			−2.5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$		$+V_S$ −2.5V	$-V_S$		$+V_S$ −2.5V	$-V_S$		$+V_S$ −2.5V	V
Input Offset Voltage, R_S = 25k			**±4**			**±4**			**±4**	mV
Input Current		60	300		60	300		60	300	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA,			(+5mA,			(+5mA,			
	−130μA)			−130μA)			−130μA)			V
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance										
Dual Supply	±3.0		±18	±3.0		±18	±3.0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S 5V to 36V, T_{min} to T_{max}		1.2	**2**		1.2	**2**		1.2	**2**	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−55		+150	−55		+150	−55		+150	°C
PACKAGE OPTIONS[5]										
Ceramic DIP (D14A)		AD536AJD			AD536AKD			AD536ASD		
Metal Can (TO-100)		AD536AJH			AD536AKH			AD536ASH		

NOTES

[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced.

[2]Error vs. crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs.

[3]Input voltages are expressed in volts rms, and error is percent of reading.

[4]With 2k external pulldown resistor.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 14. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

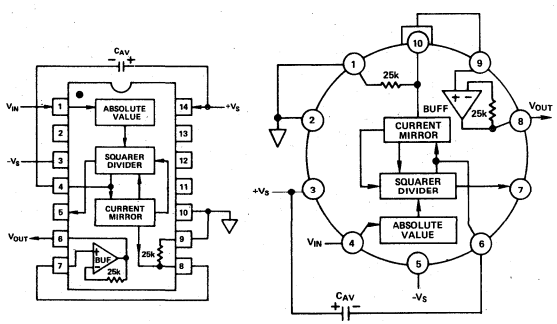


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 249Ω in series with the internal 25kΩ resistor. This will cause a 1% increase in scale factor, which is trimmed out by using R_1 as shown.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

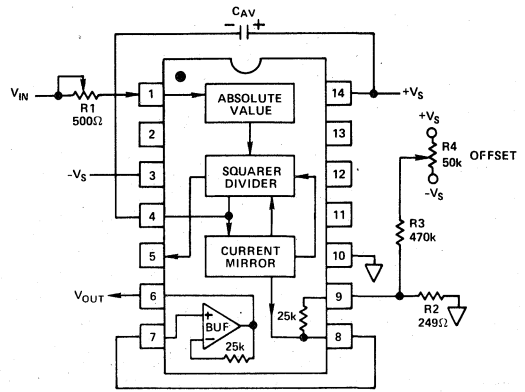


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 14. The load resistor, R_L, is necessary to provide output sink current.

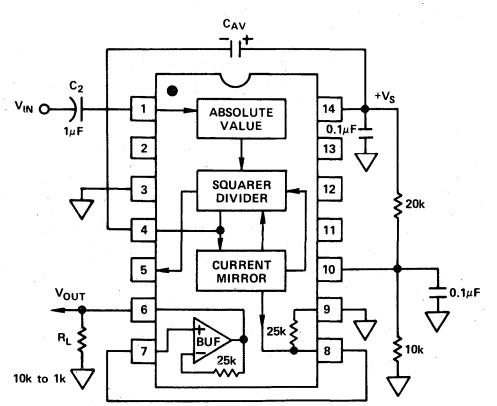


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

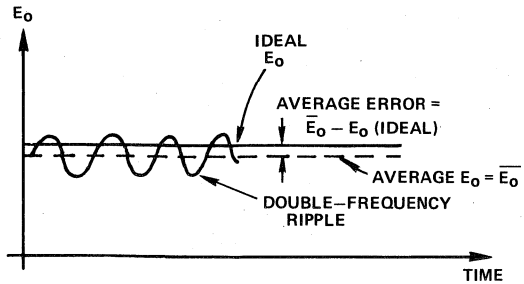


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

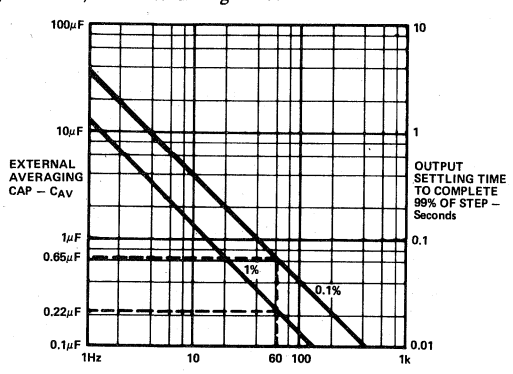


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

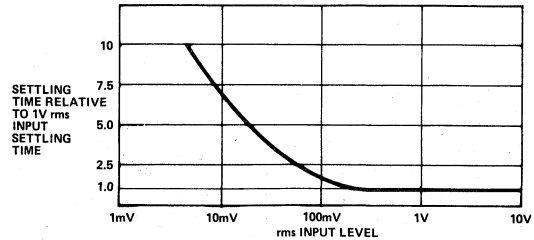


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

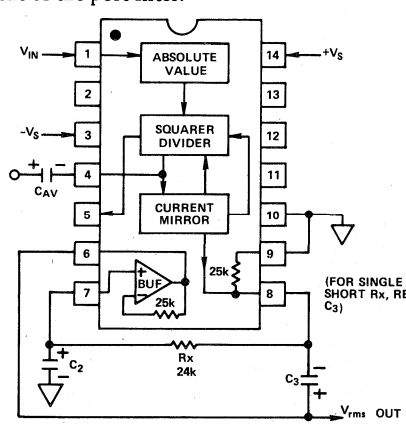


Figure 7. 2 Pole "Post" Filter

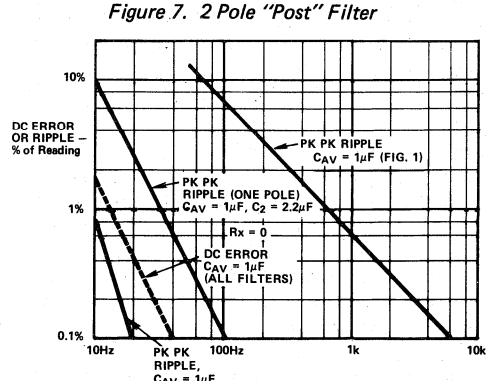


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

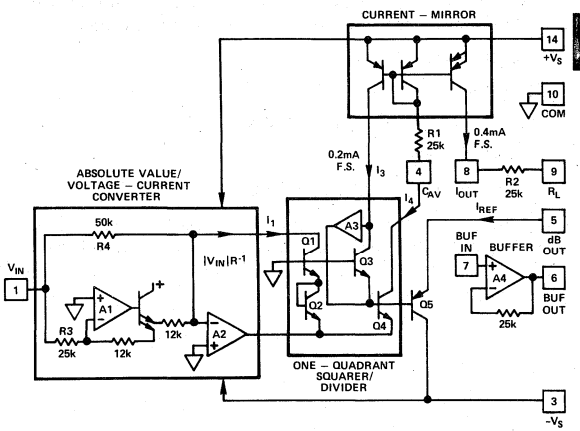


Figure 9. Simplified Schematic

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A, which is not available in any other computing rms circuit, is the logarithmic or decibel output. The internal circuit which computes dB is very accurate and works well over a 60dB range. The connection for dB measurements is shown in Figure 10. The user selects the 0dB level by setting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor, R_3, is available from Tel Labs, Londonderry, NH, type number Q-81. The linear rms output is available at pin 8 with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc
4. Adjust R_2 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_2 for the proper gain automatically gives the correct temperature compensation.

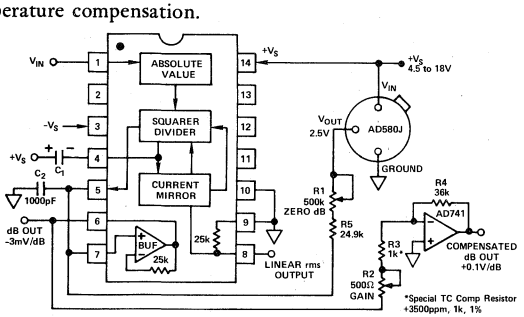


Figure 10. dB Connection

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 100kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 6kHz.

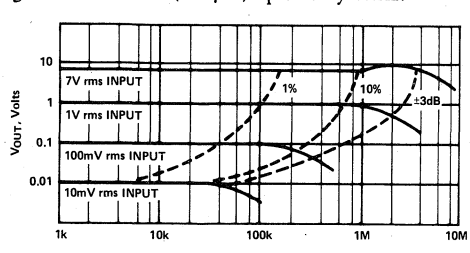


Figure 11. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 12 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

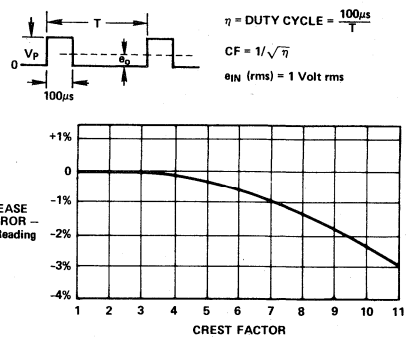


Figure 12. Error vs. Crest Factor

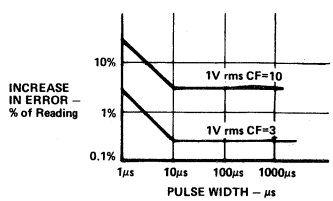


Figure 13. AD536A Error vs. Pulse Width Rectangular Pulse

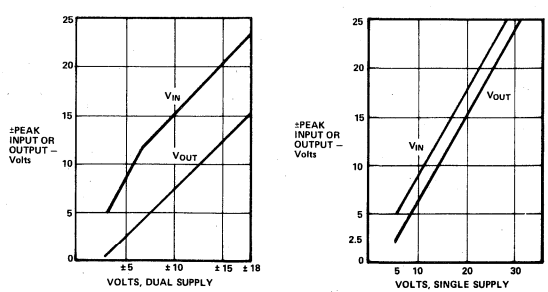


Figure 14. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

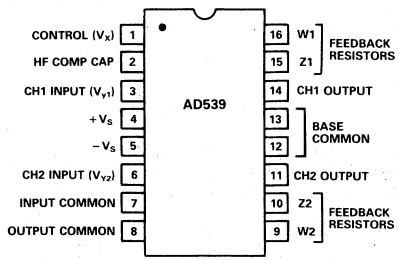
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
- Two Quadrant Multiplication/Division
- Two Independent Signal Channels
- Signal Bandwidth of 60MHz (I_{OUT})
- Linear Control-Bandwidth of 5MHz
- Fully-Calibrated, Monolithic Circuit

APPLICATIONS
- Precise AGC and VCA Systems
- Voltage-Controlled Filters
- Video-Signal Processing
- High-Speed Analog Division
- Automatic Signal-Leveling
- Square-Law Gain/Loss Control

AD539 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage reference and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps in conjunction with the on-chip scaling resistors, accurate multiplication and large output voltages can be achieved, but with a reduction in bandwidth typically to 25MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. All versions are packaged in 16-pin DIPs.

DUAL SIGNAL CHANNELS

The signal voltages inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, +3.2V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

SPECIFICATIONS ($@ T_A = 25°C, V_S = \pm 5V$, unless otherwise specified)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS	Reference Figure 6a										
Minimal Configuration											
Bandwidth, −3dB	$R_L = 50\Omega, C_C = 0.01\mu F$	30	60		30	60		30	60		MHz
Maximum Output	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		−10			−10			210		dBm
Feedthrough, f<1MHz	$V_X = 0, V_{Yac} = 1.5V$ rms		−75			−75			−75		dBm
f=20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
$-1V < V_{Ydc} < +1V$	f=3.58MHz, $V_X = +3V$,		±0.2			±0.2			±0.2		Degrees
$-2V < V_{Ydc} < +2V$	$V_{Yac} = 100mV$		±0.5			±0.5			±0.5		Degrees
Group Delay	Reference Figure 2										
Bandwidth, −3dB (AD509)	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		6			6			6		MHz
Maximum Output	$V_X = +3V, V_{Yac} = 1.5V$ rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	$V_X = 0, V_{Yac} = 1.5V$ rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	$V_{Y1} = 1V$ rms, $V_{Y2} = 0$										
	$V_X = +3V$, f<100kHz		−40			−40			−40		dB
Noise, 10Hz to 1MHz	$V_X = +1.5V, V_Y = 0$, Figure 2		200			200			200		$nV/\sqrt{Hz}$
THD + Noise, $V_X = +1V$,	f=10kHz, $V_{Yac} = 1V$ rms		0.02			0.02			0.02		%
$V_Y = +3V$	f=10kHz, $V_{Yac} = 1V$ rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	$+0.1V < V_X < +3V, V_{Yac} = 1V$ rms		25			25			25		MHz
Maximum Output Feedthrough, $V_X = +3V$	$V_{Yac} = 1.5V$ rms, f=3MHz		2.25			2.25			2.25		V rms
$V_X = +0$	$V_{Yac} = 1.0V$ rms, f=3MHz		14			14			14		mV rms
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	$C_C = 3000pF, V_X dc = +1.5V$,										
	$V_X ac = 100mV$ rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S > 7V$	±4.2			±4.2			±4.2			V
Input Resistance			400			400			400		kΩ
Bias Current			10	**30**		10	**20**		10	**30**	μA
Offset Voltage	$V_X = +3V, V_Y = 0$		5	**20**		5	**10**		5	**20**	mV
(T_{min} to T_{max})			10		5				15	35	mV
Power Supply Sensitivity	$V_X = +3V, V_Y = 0$		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		+3.2			+3.2			+3.2			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	4		1	2		1	4	mV
(T_{min} to T_{max})			3			2			2	5	mV
Power Supply Sensitivity			30			30			30		μV/V
Decibel Gain	(Figure 2)		20			20			20		$\log_{10}(V_X)$
Absolute Gain Error	$V_X = +0.1V$ to $+3.0V$		0.2	**0.4**		0.1	**0.2**		0.2	**0.4**	dB
(T_{min} to T_{max})			0.3			0.15			0.25	0.5	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	$V_X = +3V, V_Y = \pm 2V$		±1			±1			±1		mA
Peak Output Current	$V_X = +3.3V, V_Y = \pm 5V$	±2	±2.8		±2	±2.8		±2	±2.8		mA
Output Offset Current	$V_X = 0, V_Y = 0$		0.2	2		0.2	2		0.2	2	μA
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,											
Either Channel			$V_W = -V_X \cdot V_Y / V_Q$			$V_W = -V_X \cdot V_Y / V_Q$			$V_W = -V_X \cdot V_Y / V_Q$		
Multiplier Scaling Voltage, V_Q			1.0			1.0			1.0		V
Accuracy			0.5	**2**		0.5	**1**		0.5	**2**	%
(T_{min} to T_{max})			1			0.5			1.0	3	%
Power Supply Sensitivity			0.03%			0.03			0.03		%/V
Total Multiplication Error[3]	$V_X <= +3V, -2V < V_Y < 2V$		0.6	**2.5**		0.6	**1.5**		2.5	**4**	% FSR
T_{min} to T_{max}			2			1			1		%
Control Feedthrough	$V_X = 0$ to $+3V, V_Y = 0$		15	**60**		15	**30**		15	**60**	mV
T_{min} to T_{max}			30			15			60	120	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°
POWER SUPPLIES											
Operational Range		±4.5		±16.5	±4.5		±16.5	±4.5		±16.5	V
Current Consumption											
$+V_S$			8.5	**10.2**		8.5	**10.2**		8.5	**10.2**	mA
$-V_S$			18.5	**22.2**		18.5	**22.2**		18.5	**22.2**	mA
PACKAGE OPTION[4]											
Ceramic DIP: (D16A)			AD539JD			AD539KD			AD539SD		

NOTES

[1]Resistance value and absolute current outputs subject to 20% tolerance.

[2]Spec assumes the external op amp is trimmed for negligible input offset.

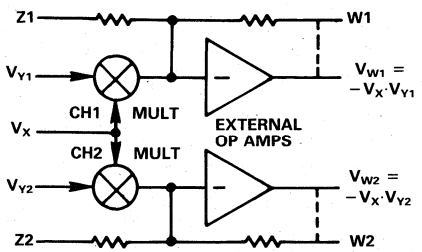
[3]Includes all errors.

[4]See Section 19 for package outline information

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AD539 FUNCTIONAL BLOCK DIAGRAM



CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

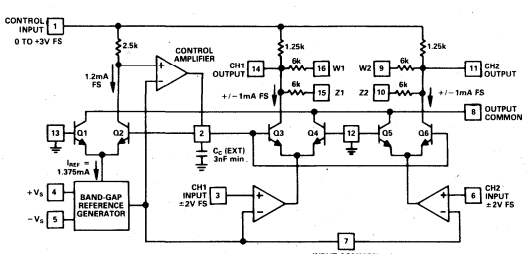


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the ouput. The bias component absorbed by the 1.25k resistors also connected to V_X, and resulting the signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above +V_S; the minimum value is 2.5V above −V_S. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_Q$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_Q are expressed in a consistent unit, usually volts. In this case, V_Q is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_Q allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to half the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y/2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y/V_Q'$$

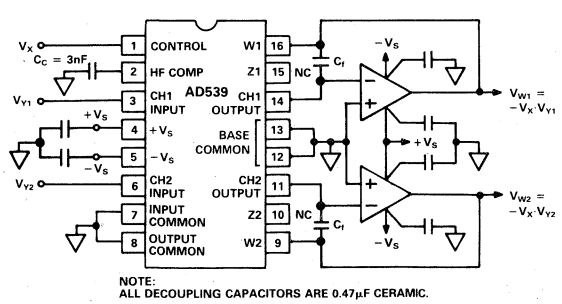
where the effective scaling voltage, V_Q' can be calculated for each channel using the formula $V_Q' = V_Q(5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when $R_L = 100\Omega$, $V_Q' = 67.5V$. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_Q' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of $V_X = +3V$, $V_Y = \pm 2V$ the full-scale outputs are $\pm 6V$. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least $\pm 8V$ are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of $+3.2V$ and $\pm 4.2V$ respectively, when the peak output is $\pm 13.4V$. This requires operating the op amps at supplies of $\pm 15V$. Under these conditions it is advisable to reduce the supplies to the AD539 to $\pm 7.5V$ to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from $\pm 15V$ supplies.



NOTE:
ALL DECOUPLING CAPACITORS ARE 0.47μF CERAMIC.

Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at $V_X = +3.162V$, 0dB at $V_X = +1V$, $-20dB$ at $V_X = +0.1V$, and so on. In many ac applications the output offset voltage (for $V_X = 0$ or $V_Y = 0$) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a $\pm 1mV$ offset uncertainty will cause the nominal 40dB attenuation at $V_X = +0.01V$ to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of $\pm 2mV$ for the AD539K and $\pm 4mV$ for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

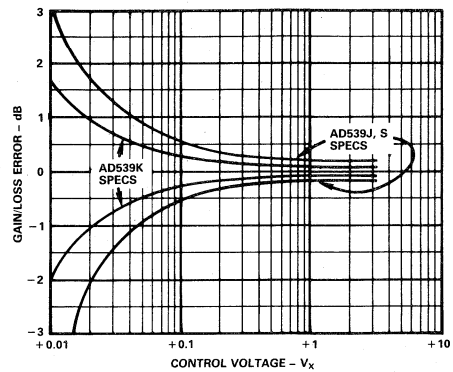


Figure 3a. Maximum ac Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with $V_Y = 0.5$ and 1.5V rms.

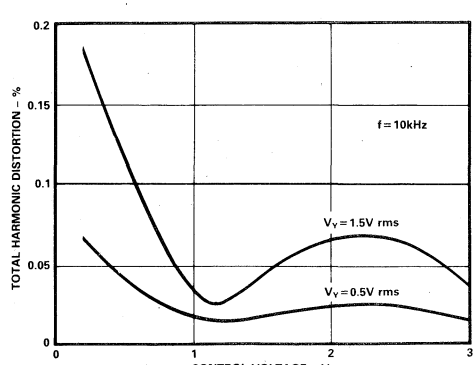


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at $\pm 3V$ FS ($\pm 6.75V$ pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is $\pm 12V$. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to $+10V$) control voltage. A disadvantage of this scheme is the need to

adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. The AD509 is a good choice for many applications since it is inexpensive, has good slewing properties and can provide about 6MHz of bandwidth in conjunction with the AD539. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

Figure 4a shows the response of the configuration of Figure 2 using AD509 op amps, with the small capacitor C_F adjusted for 1dB peaking at $V_X = +1V$. The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS). For these curves, V_Y is 1V rms; other conditions are listed in Table I. The −3dB bandwidth is essentially constant at 6MHz for $V_X = +0.01V$ to $V_X = +1V$. At $V_X = +3.162V$ (chosen to result in 10dB gain) the apparent slight loss of bandwidth is due to the onset of slew-rate limitations

	AD544	AD509	ADLH0032
Op Amp Supply Voltages	±15V	±10V	±10V
Op Amp Compensation Cap.	None	None	1-5pF (Pins 2, 3)
Feedback Capacitor, C_F	None	2-5pF	1-4pF
−3dB Bandwidth, $V_X = +1V$	400kHz	6MHz	25MHz
Load Capacitance	<1nF	<100pF	<100pF
HF Feedthrough, $V_X = -0.01V$, f = 5MHz	–	−75dB	−70dB
rms Output Noise,			
$V_X = +1V$, BW 10Hz-10kHz	50μV	50μV	30μV
$V_X = +1V$, BW 10Hz-5MHz	220μV	550μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

Table I. Summary of Operating Conditions and Performance for Standard Multiplier Connections

(peak output is then ±4.5V). The corresponding pulse response is shown in Figure 4b for a signal input V_Y of ±1V and two values of V_X (+0.1V and +3V).

For wide-band applications a hybrid op amp can be used. Figure 5a shows the HF response using the ADLH0032, with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at $V_X = +1V$; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at $V_X = +0.01V$. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably

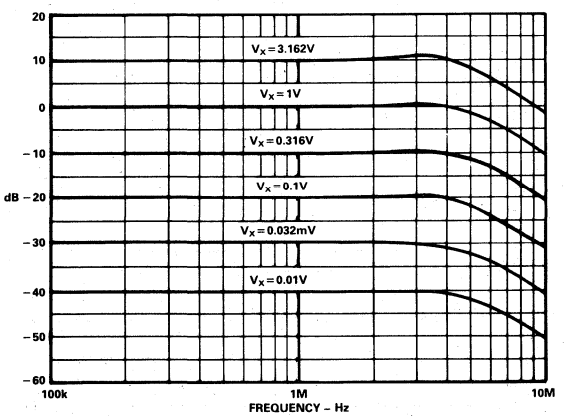


Figure 4a. Response in Standard Configuration Using AD509 Output Op Amp

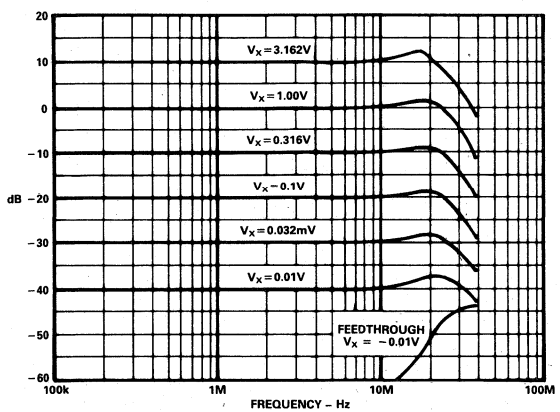
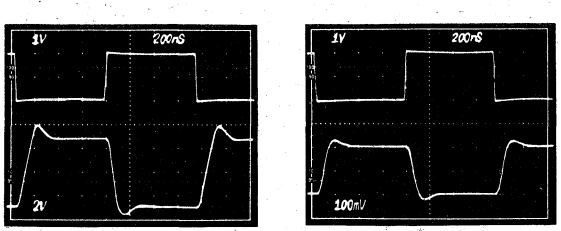
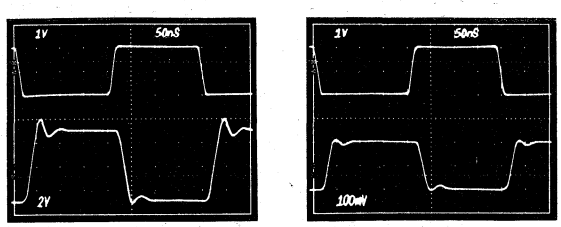


Figure 5a. Multiplier HF Response Using ADLH0032 Op Amps



$V_X = +3V$ $V_X = +0.1V$

Figure 4b. Multiplier Pulse Response Using AD509 Op Amps



$V_X = +3V$ $V_X = +0.1V$

Figure 5b. Multiplier Pulse Response Using ADLH0032 Op Amps

zero. Measurements show that the feedthrough can be held to −90dB relative to full output at low frequencies and to −60dB up to 20MHz with careful in board layout. The corresponding pulse response is shown in Figure 5b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk, into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 6a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

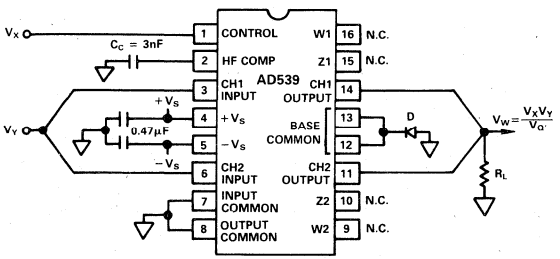


Figure 6a. Minimal Single-Channel Multiplier

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV	±134mV	±172mV	±242mV	±612mV	±1V
	65.5mV rms	94.7mV rms	122mV rms	171mV rms	433mV rms	*
FS Output-Power in Load	0.086mW	0.12mW	0.15mW	0.195mW	0.312mW	–
	−10.5dBm	−9.2dBm	−8.3dBm	−7.1dBm	−5.05dBm	–
Pk Output Voltage	±210mV	±300mV	±388mV	±544mV	±1V	±1V
	148mV rms	212mV rms	274mV rms	385mV rms	*	*
Pk Output-Power in Load	0.44mW	0.6mW	0.75mW	1mW	±1V	±1V
	−7dBm	−4.4dBm	−2.5dBm	0dBm	*	*
Effective Scaling Voltage, V_Q'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance.

Table II. Summary of Performance for Minimal Configuration

Figure 6b shows the HF response in this configuration with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response. In many applications *phase linearity* over frequency is important. Figure 6c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 6d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough

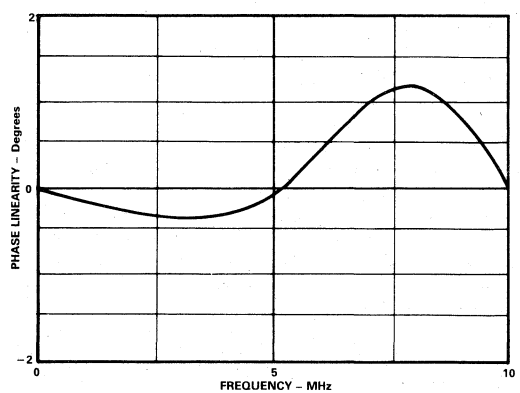


Figure 6c. Phase Linearity Error in Minimal Configuration

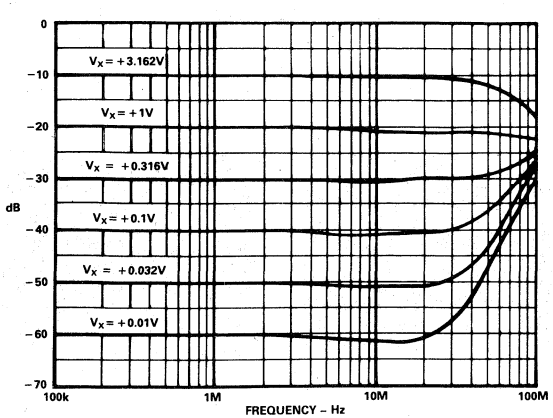


Figure 6b. HF Response in Minimal Configuration

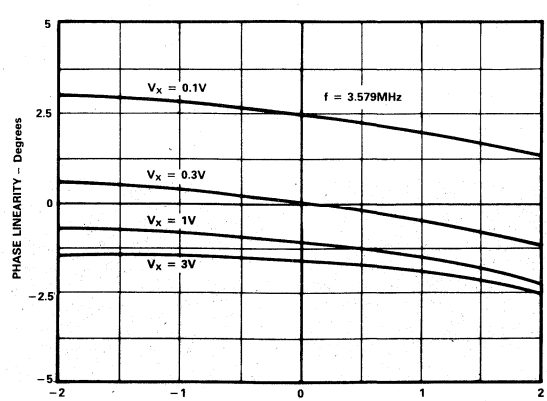


Figure 6d. Differential Phase Linearity in Minimal Configuration for a Typical Device

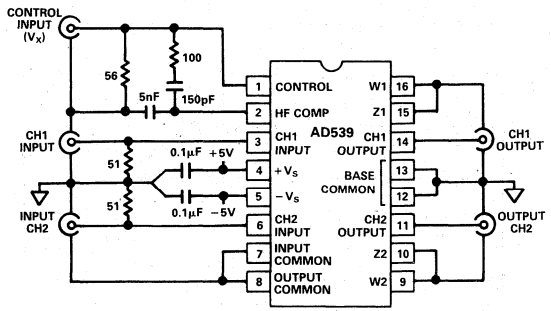


Figure 7a. High-Speed Differential Configuration

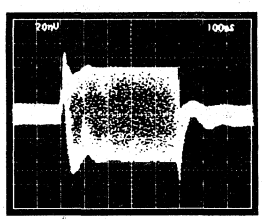


Figure 7b. Control Feedthrough One Channel of Figure 7a

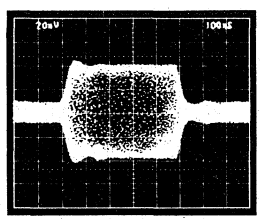


Figure 7c. Control Feedthrough Differential Mode, Figure 7a

is virtually eliminated. Figure 7a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal response time. The control feedthrough glitch is shown in Figure 7b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 7c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 8a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω. They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 8b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins

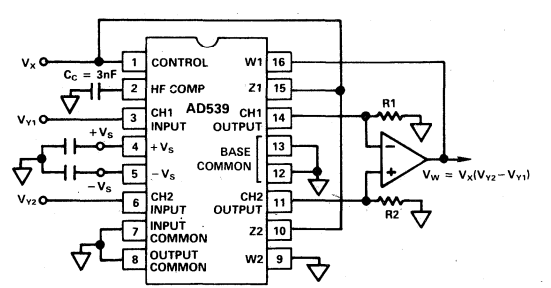


Figure 8a. Low-Distortion Differential Configuration

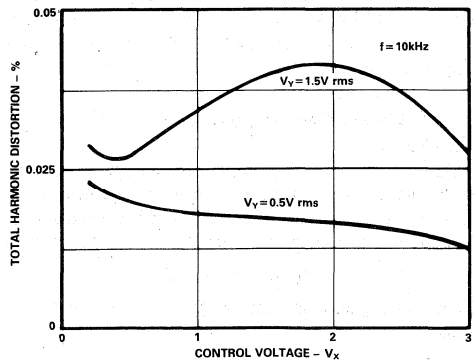


Figure 8b. Distortion in Differential Mode Using ADLH0032

10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

Square-Law Voltage Controlled Amplifier

The signal channels of the AD539 can be cascaded to achieve a

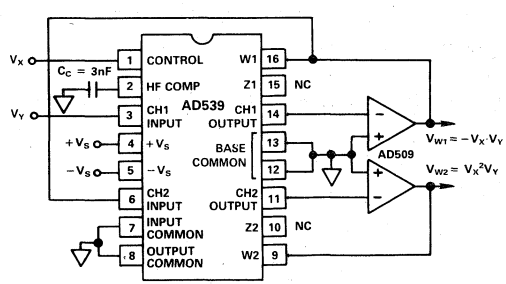


Figure 9a. Square-Law, Voltage-Controlled Amplifier

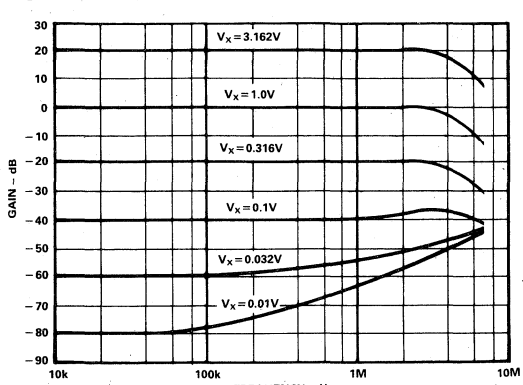


Figure 9b. HF Response of Square-Law Amplifier

much wider gain range with a square-law control characteristic. Figure 9a shows the connections and Figure 9b is the measured HF response using AD509 op amps with no additional HF compensation. Note that the gain varies from -80dB for $V_X = +0.01$V to $+20$dB at $V_X = +3.162$V, which is a 100dB control range. Since V_X is never very small, the gain or loss is well-defined over the entire range.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_Q V_W / V_X$$

Recalling that the nominal value of V_Q is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1$V and a gain of 40dB when $V_X =$

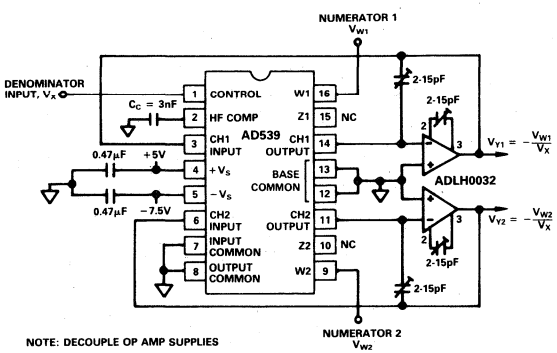


Figure 10a. Two-Channel Divider with 1V Scaling

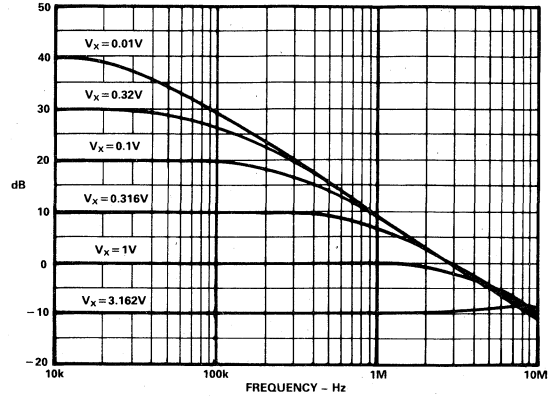


Figure 10b. HF Response of Figure 10a Divider

$+0.01$V. The output swing is limited to ± 2V nominal full-scale and ± 4.2V peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162$V), it follows that the maximum input to V_W should be ± 6.3V (4.4V rms) for low distortion applications, and no more than ± 13.4V (9.5V rms) to avoid clipping. Note that offset adjustment will be needed for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$ or 600 at $V_X = +0.01$V.

The gain-magnitude response for this configuration using the ADLH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7$pF is shown in Figure 10b. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162$V, 4.5MHz at $V_X = +1$V, 350kHz at $V_X = +0.1$V and 35kHz at $V_X = +0.01$V. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed.

ANALOG DEVICES

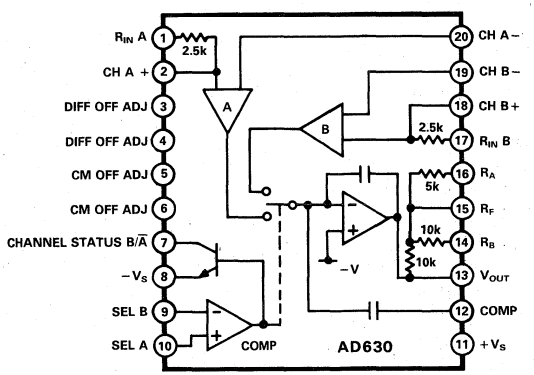
Balanced Modulator/Demodulator

AD630

FEATURES

Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth

AD630 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630J Min	AD630J Typ	AD630J Max	AD630K Min	AD630K Typ	AD630K Max	Units
GAIN							
Open Loop Gain	**90**	110		**100**	120		dB
±1, ±2 Closed Loop Gain Error		0.1				**0.05**	%
Closed Loop Gain Match		0.1				**0.05**	%
Closed Loop Gain Drift		2			2		ppm°C
CHANNEL INPUTS							
V_{IN} Operational Limit[1]		$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$		Volts
Input Offset Voltage			**500**			**100**	µV
Input Offset Voltage							
T_{min} to T_{max}			**800**			**160**	µV
Input Bias Current		100	**300**		100	**300**	nA
Input Offset Current		10	**50**		10	**50**	nA
Channel Separation @ 10kHz		100			100		dB
COMPARATOR							
V_{IN} Operational Limit[1]		$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$		Volts
Switching Window			**±1.5**			**±1.5**	mV
Switching Window							
T_{min} to T_{max}			**±2.0**			**±2.0**	mV
Input Bias Current		100	**300**		100	**300**	nA
Response Time (−5mV to +5mV step)		200			200		ns
Channel Status							
I_{SINK} @ $V_{OL} \mp -V_S + 0.4V$[2]	**1.6**			**1.6**			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE							
Unity Gain Bandwidth		2			2		MHz
Slew Rate[3]		45			45		V/µs
Settling Time to 0.1% (20V step)		3			3		µs
OPERATING CHARACTERISTICS							
Common-Mode Rejection	**85**	105		**90**	110		dB
Power Supply Rejection	**90**	110		**90**	110		dB
Supply Voltage Range	**±5**		±16.5	**±5**		±16.5	Volts
Supply Current		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ							
T_{min} to T_{max}	**±10**			**±10**			Volts
Output Short Circuit Current		25			25		mA
TEMPERATURE RANGES							
Rated Performance – N Package	0		+70	0		+70	°C
D Package		N/A			N/A		°C
PACKAGE OPTIONS[4]							
Plastic DIP – (N20A)		AD630JN			AD630KN		
Ceramic DIP – (D20A)		–			–		

NOTES

[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.

[2] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.

[3] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.

[4] See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (@ +25°C and $\pm V_S = \pm 15V$ unless otherwise specified)

Model	AD630A			AD630B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage										
T_{min} to T_{max}			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window										
T_{min} to T_{max}			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[2]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[3]		45			45			45		V/µs
Settling Time to 0.1% (20V step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ $R_L = 2k\Omega$										
T_{min} to T_{max}	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package		N/A			N/A			N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C
PACKAGE OPTIONS[4]										
Plastic DIP – (N20A)		–			–			–		
Ceramic DIP – (D20A)		AD630AD			AD630BD			AD630SD		

NOTES
[1]If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.
[2] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.
[3] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.
[4]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature, Ceramic Package	−65°C to +150°C
Storage Temperature, Plastic Package	−55°C to +125°C
Lead Temperature, 10 sec. Soldering	+300°C
Max Junction Temperature	+150°C

Typical Performance Characteristics

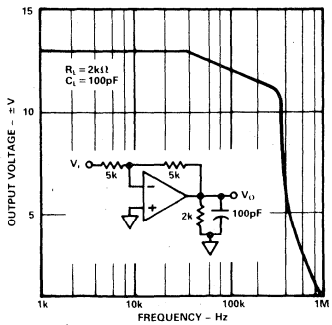


Figure 1. Output Voltage vs. Frequency

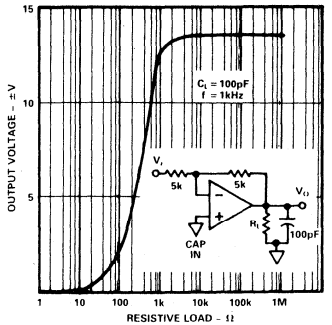


Figure 2. Output Voltage vs. Resistive Load

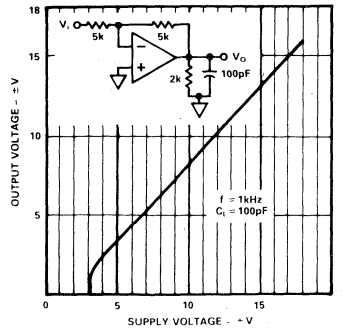


Figure 3. Output Voltage Swing vs. Supply Voltage

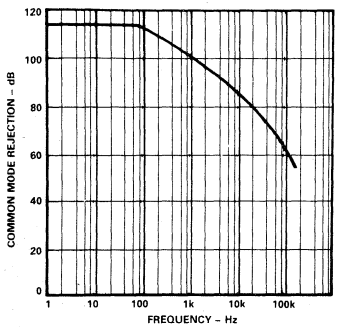


Figure 4. Common Mode Rejection vs. Frequency

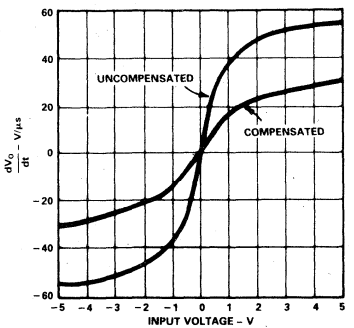


Figure 5. $\frac{dV_O}{dt}$ vs. Input Voltage

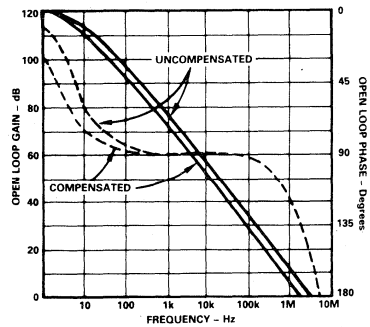
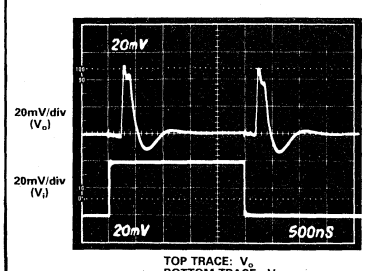
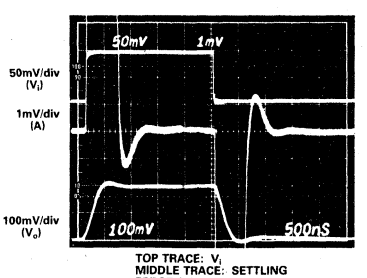
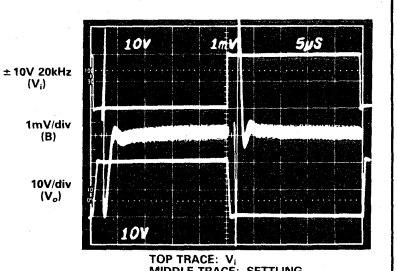


Figure 6. Gain and Phase vs. Frequency







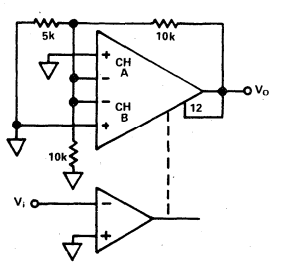


Figure 7. Channel-to-Channel Switching Characteristic

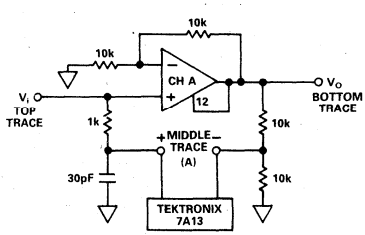


Figure 8. Small Signal Noninverting Step Response

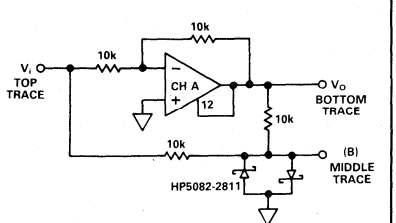


Figure 9. Large Signal Inverting Step Response

TWO WAYS TO LOOK AT THE AD630

Figure 10 is a functional block diagram of the AD630 which also shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 11. In this diagram, the individual A and B channel pre-amps, the switch, and the integrator-output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

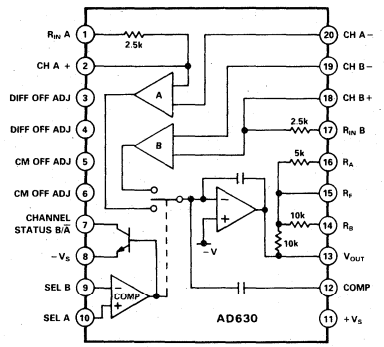


Figure 10. Functional Block Diagram

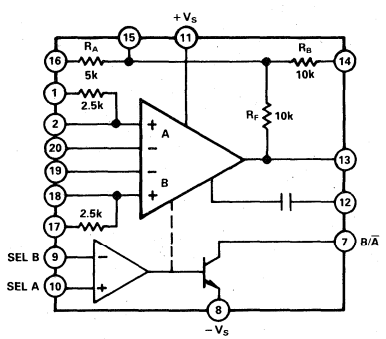


Figure 11. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be more easy to recognize as two fixed gain stages which may be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes Laser-Wafer-Trimmed thin-film feedback resistors on the monolithic chip. The configuration shown below yields a gain of ± 2 and can be easily changed to ± 1 by shifting R_B from its ground connection to the output.

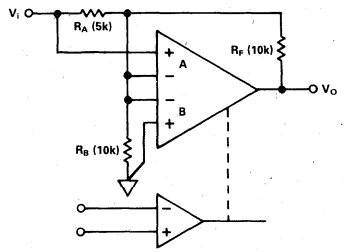


Figure 12. AD630 Symmetric Gain (± 2)

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The de-selected input is off and has negligible effect on the operation.

When channel B is selected, the resistors R_A and R_F are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 13. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, input B will be de-selected and A will be selected. The new equivalent circuit will be the noninverting gain configuration shown below. In this case R_A will appear across the op-amp input terminals, but since the amplifier drives this difference voltage to zero the closed loop gain is unaffected.

The two closed loop gain magnitudes will be equal when $R_F/R_A = 1 + R_F/R_B$, which will result from making R_A equal to $R_F R_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5k and the two 10k resistors on the AD630 chip can be used to make a gain of two as shown here. By paralleling the 10k resistors to make R_F equal 5k and omitting R_B the circuit can be programmed for a gain of ± 1 (as shown in Figure 19a). These and other configurations using the on chip resistors present the inverting inputs with a 2.5k source impedance. The more complete AD630 diagrams show 2.5k resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

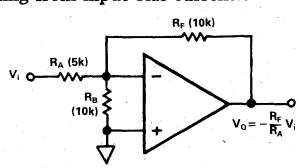


Figure 13. Inverting Gain Configuration

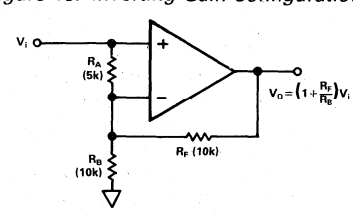


Figure 14. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 15. It has been subdivided into three major sections, the comparator, the two input stages and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5mV in magnitude

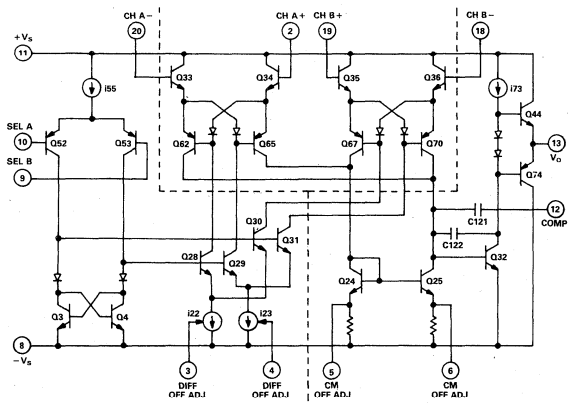


Figure 15. AD630 Simplified Schematic

applied to the comparator inputs will completely select one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls causing it to become active. The deselected cell blocks the bias to its input stage which, as a consequence, remains off.

The structure of the transconductance stages is such that they present a high impedance at their input terminals and draw no bias current when deselected. The deselected input does not interfere with the operation of the selected input insuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasi-hyperbolic-sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage will drive the output integrator, and hence, the faster the output signal will move. This feature helps insure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror-load (Q24 and Q25), an integrator-voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Since the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ± 1 and ± 2 which the self-contained applications resistors provide. The AD630 can be readily programmed with 3 external resistors over a wide range of positive and negative gain by selecting R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequently R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_B R_F/(R_B + R_F)$. That is, R_A should equal the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes will match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. Essentially the same considerations apply to the AD630 as to conventional op-amp feedback circuits. Virtually any function which can be realized with simple non-inverting "L network" feedback can be used with the AD630. A common arrangement is shown in Figure 16. The low frequency gain of this circuit is 10. The response will have a pole (–3dB) at a frequency $f \simeq 1/(2\pi 100k\Omega C)$ and a zero (3dB from the high frequency asymptote) at about 10 times this frequency. The 2k resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal will be transmitted at unity gain

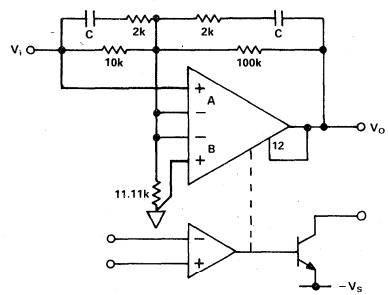


Figure 16. AD630 with External Feedback

while the low frequency components will be amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal will contain the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If gain is switched when the input signal is not zero, as it is in many practical cases, a transient will be delivered to the circuitry driving the AD630. In most applications, this will require the AD630 circuit to be driven by a low impedance source which remains "stiff " at high frequencies. Generally this will be a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ±2 applications the noise gain which must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop will be on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew-rate for closed-loop gains of |2| and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin will be reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response will not be optimum. For these applications, the self-contained compensation capacitor may be added by connecting pin 12 to pin 13. This connection reduces the closed loop bandwidth somewhat, and improves the phase margin.

For intermediate conditions, such as gain of ±1 where loop attenuation is 2, use of the compensation should be determined by whether bandwidth or settling response must be optimized. The optional compensation should also be used when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pre-trimmed so that external trimming will only be required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With system input tied to 0V, and a switching or carrier waveform applied to the comparator, a low level square wave will appear at the output. The differential offset adjustment pot can be used to null the amplitude of this square wave (pins 3 and 4). The common mode offset adjustment can be used to zero the residual dc output voltage (pins 5 and 6). These functions should be implemented using 10k trim pots with wipers connected directly to pin 8 as shown in Figures 19a and 19b.

CHANNEL STATUS OUTPUT

The channel status output, pin 7, is an open collector output referenced to $-V_S$ which can be used to indicate which of the two input channels is active. The output will be active (pulled low) when channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 17 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

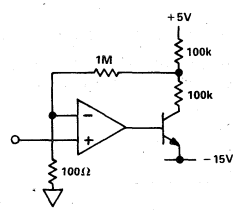


Figure 17. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 18. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

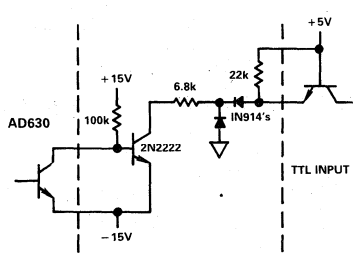


Figure 18. Channel Status – TTL Interface

APPLICATIONS:
BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ±1 and ±2. The ±1 arrangement is shown in Figure 19a and the ±2 arrangement is shown in Figure 19b. These cases differ only in the connection of the 10k feedback resistor (pin 14) and the compensation capacitor (pin 12). Note the use of the 2.5kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ±1 gain case. Figure 20 demonstrates the performance of the AD630 when used to modulate a 100kHz square wave carrier with a 10kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels, and a reference (or carrier) input applied to the comparator.

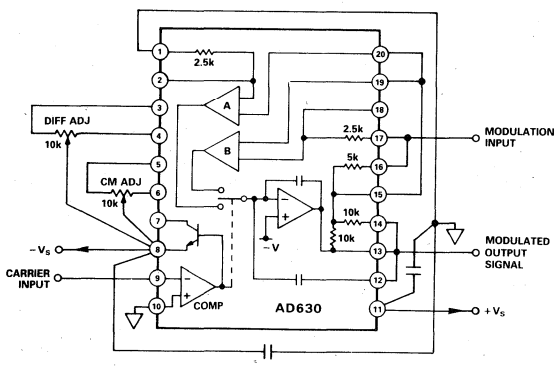


Figure 19a. AD630 Configured as a Gain-of-One Balanced Modulator

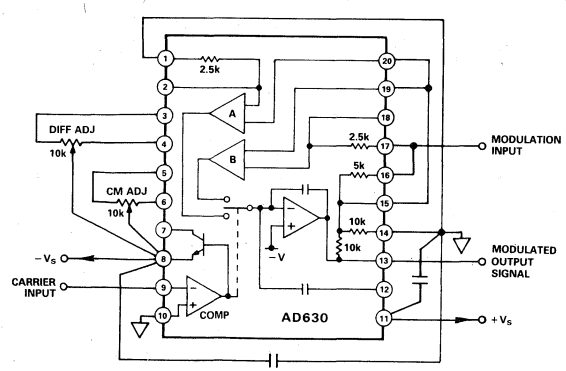


Figure 19b. AD630 Configured as a Gain-of-Two Balanced Modulator

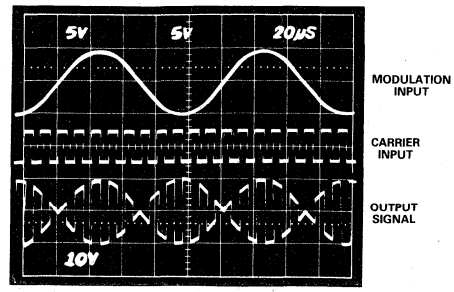


Figure 20. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described above will also act as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances will be the baseband modulation signal. Higher order carrier components will also be present which can be removed with a low-pass filter. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figures 19a and 19b can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low pass filtering) will be proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, then the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output will be zero.

PRECISION RECTIFIER-ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 will act as a precision rectifier. The high frequency performance will be superior to that which can be achieved with diode feedback and op amps. There are no diode drops which the op amp must "leap over" with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A Linear Variable Differential Transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 21 shows an accurate synchronous demodulation system which can be used to produce a dc voltage which corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second order effect.

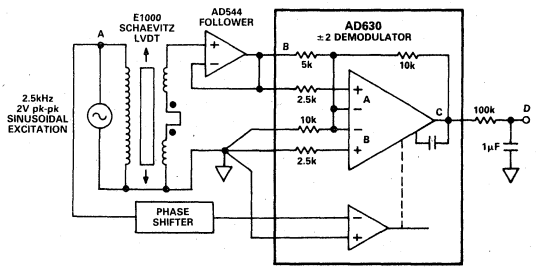


Figure 21. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

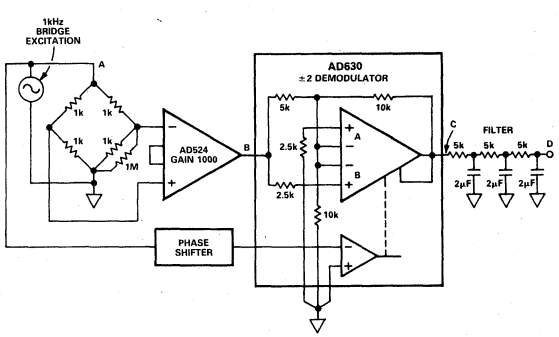


Figure 22. AC Bridge System

Figure 22 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper-middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 3.2mV change in the low pass filtered dc output, well above the RTO drifts and noise.

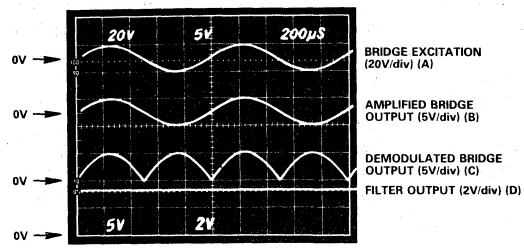


Figure 23. AC Bridge Waveforms

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique which is used to separate a small, narrow band signal from interfering noise. The lock-in amplifier acts as a detector and narrow band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 24. Figure 25 is an oscilloscope photo showing the recovery of a signal modulated at 400Hz from a noise signal approximately 100,000 times larger; a dynamic range of 100dB.

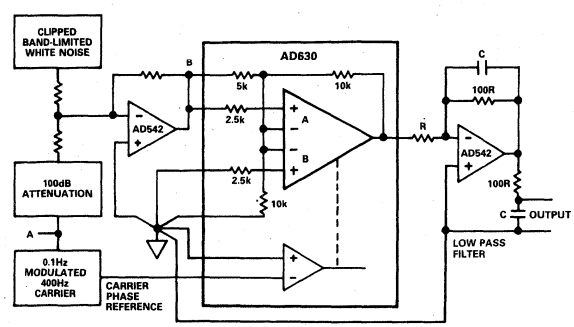


Figure 24. Lock-In Amplifier

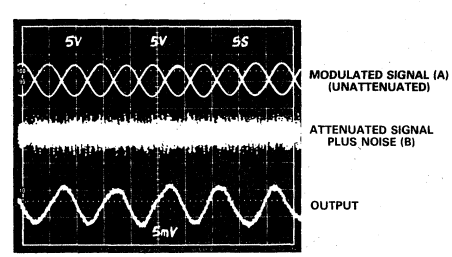


Figure 25. Lock-In Amplifier Wave Forms

The test signal is produced by modulating a 400Hz carrier with a 0.1Hz sine wave. The signals produced, for example, by chopped radiation (IR, optical, etc.) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 19b and is shown in the upper trace of Figure 25. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited clipped white noise. Figure 25 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 25.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low pass output filter will aid in rejecting wider bandwidth interference.

ANALOG DEVICES

Internally Trimmed Precision I.C. Multiplier

AD632

PRELIMINARY TECHNICAL DATA

FEATURES

- **Pretrimmed to ±0.5% Max 4-Quadrant Error**
- **All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function**
- **Scale-Factor Adjustable to Provide up to X10 Gain**
- **Low Noise Design: 90μV rms, 10Hz-10kHz**
- **Low Cost, Monolithic Construction**
- **Excellent Long Term Stability**

APPLICATIONS

- **High Quality Analog Signal Processing**
- **Differential Ratio and Percentage Computations**
- **Algebraic and Trigonometric Function Synthesis**
- **Accurate Voltage Controlled Oscillators and Filters**

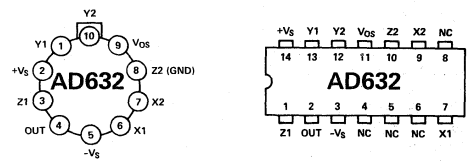
PRODUCT DESCRIPTION

The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin for pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90μV rms.

AD632 PIN CONFIGURATION



PRODUCT HIGHLIGHTS

Guaranteed Performance Over Temperature: The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively at +25°C and are rated for operation from –25°C to +85°C. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of –55°C to +125°C.

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$ unless otherwise noted)

Model	AD632A			AD632B			AD632S			AD632T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)+Z_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Y_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Z_2}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)+Y_2}{10V}$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±1.0**			**±0.5**	%
T_A = min to max			**±1.5**			**±1.0**			**±2.0**			**±1.0**	%
Total Error vs Temperature			±0.02			±0.01			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		±0.02						±0.2				±0.005	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.08	±0.5		±0.8	±0.25		±0.08	±0.5		±0.08	±0.25	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.01			±0.1	±0.1		±0.01			±0.01	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.15	±0.3		±0.05	±0.15		±0.15	±0.3		±0.15	±0.15	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01	±0.1		±0.01	±0.1		±0.01	±0.1		±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift		200	400		200	400			**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2			2		µs
NOISE													
Noise Spectral-Density SF = 10V		0.08			0.08			0.08			0.08		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.04			0.04			0.04			0.04		$\mu V/\sqrt{Hz}$
Wideband Noise A = 10Hz to 5MHz		1.0			1.0			1.0			1.0		µV/rms
P = 10Hz to 10kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]													
Signal Voltage Range (Diff. or CM		±10			±10			±10			±10		V
Operating Diff.)		±12			±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200	400		100	200			500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dB
Bias Current		0.8	**2**		0.8	**2**		0.8	**2**		0.8	2	µA
Offset Current		0.1			0.1			0.1			0.1		µA
Differential Resistance		10			10			10			10		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$\frac{10V(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
($X-10V, -10V \leq Z \leq +10V$)		±0.75			±0.35			±0.75			±0.35		%
($X-1V, -1V \leq Z \leq +1V$)		±2.0			±1.0			±2.0			±1.0		%
($0.10V \leq X \leq 10V, -10V \leq Z \leq 10V$													
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$			$\frac{(X_1-X_2)^2}{(10V)}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[6] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	**±8**		**±20**	**±8**		**±20**	**±8**		**±22**	**±8**		**±22**	V
Supply Current													
Quiescent		4	**6**		4	6		4	**6**		4	6	mA

NOTES

[1]Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).

[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3V.

[5]See functional block diagram for definition of sections.

[6]With external Z-offset adjustment, $Z \leq \pm X$.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

	AD632A, B	AD632S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD632A

PACKAGE OPTIONS[1]

AD632AD: TO-116 – (D14A)
AD632AH: TO-100
AD632BD: TO-116 – (D14A)
AD632BH: TO-100
AD632SD: TO-116 – (D14A)
AD632SH: TO-100
AD632TD: TO-116 – (D14A)
AD632TH: TO-100

NOTE
[1] See Section 19 for package outline information.

6

Typical Performance Curves

(typical at +25°C with $\pm V_S$ = 15V)

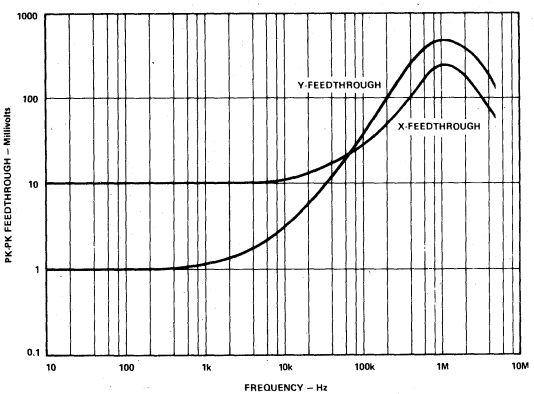


Figure 1. AC Feedthrough vs. Frequency

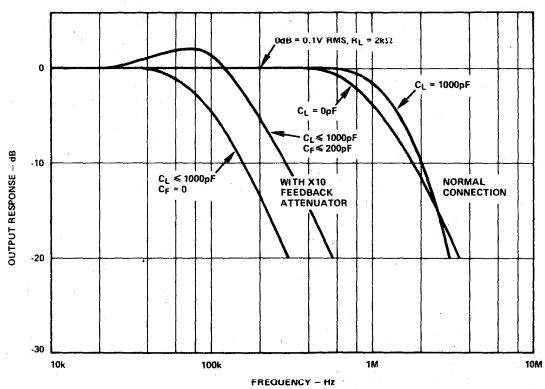


Figure 2. Frequency Response as a Multiplier

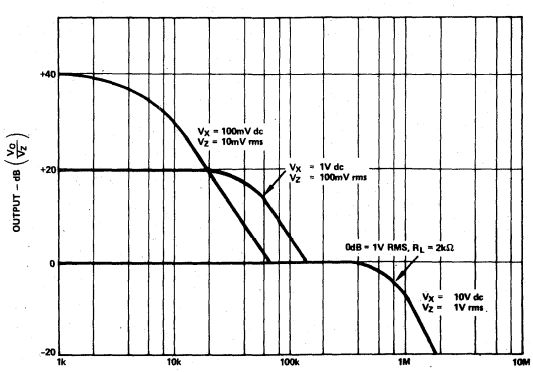


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

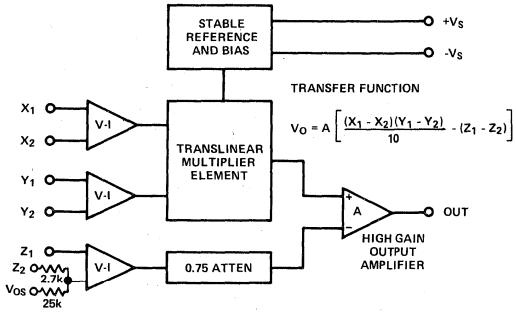


Figure 4. AD632 Functional Block Diagram

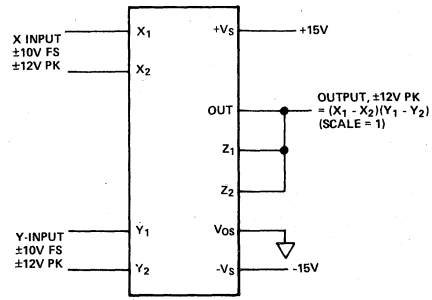


Figure 6. Connections for Scale-Factor of Unity

OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

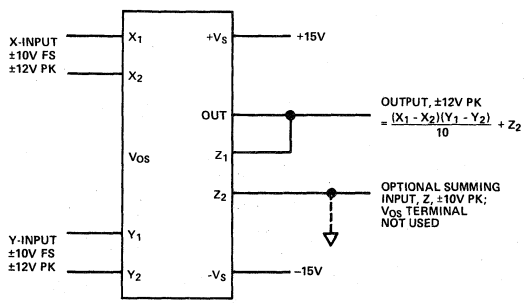


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The Z_2 terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z_1 terminal where they are amplified by −10 or to the common ground connection where they are amplified by −1. Input signals may also be applied to the lower end of the 2.7kΩ resistor, giving a gain of +9.

OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

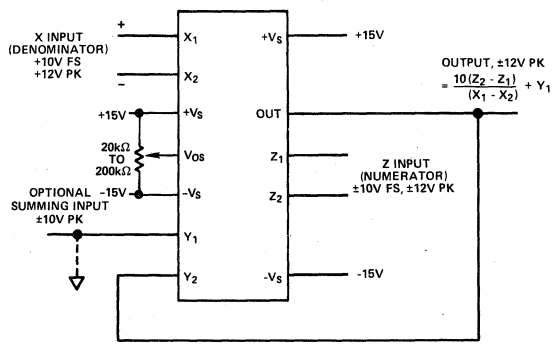


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10V to 1V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

*See the AD535 Data Sheet for more details.

ANALOG DEVICES

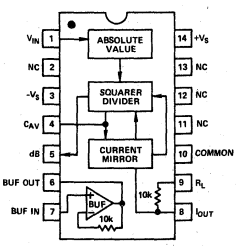
Low Level True rms-to-dc Converter

AD636

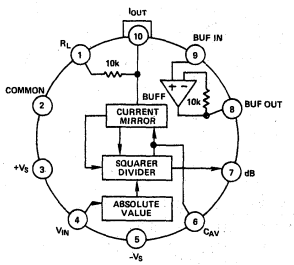
FEATURES

- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.5% max Error (AD636K)
  - 1.0% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit

AD636 FUNCTIONAL BLOCK DIAGRAMS



TO-116
TOP VIEW



TO-100
TOP VIEW

PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±12V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal), and full scale accuracy. Thus no external trims are required to achieve full rated accuracy.

The AD636 is available in two accuracy grades; the AD636J has a total error of ±0.5mV ±1.0% of reading, and the AD636K is accurate within ±0.2mV ±0.5% of reading. Both versions are specified for the 0 to 70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10 pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±12V sources. A standard 9V battery will provide several hundred hours of continuous operation.

SPECIFICATIONS (typical @ +25°C, $+V_S$ = +3V, $-V_S$ = -5V, unless otherwise specified)

Model	AD636J	AD636K
TRANSFER EQUATION	$V_{OUT} = \sqrt{\text{avg. } (V_{IN})^2}$	*
CONVERSION ACCURACY		
Total Error, Internal Trim[1,2]	±0.5mV ±1.0% of Reading, max	±0.2mV ±0.5% of Reading, max
vs. Temperature, 0 to +70°C	±(0.1mV ±0.01% of Reading)/°C max	±(0.1mV ±0.005% of Reading)/°C max
vs. Supply Voltage	±(0.1mV ±0.01% of Reading)/V	*
dc Reversal Error	±0.2% of Reading	±0.1% of Reading
Total Error, External Trim[1]	±0.3mV ±0.3% of Reading	±0.1mV ±0.2% of Reading
ERROR vs. CREST FACTOR[3]		
Crest Factor 1 to 2	Specified Accuracy	*
Crest Factor = 3	-0.2%	*
Crest Factor = 6	-0.5%	*
FREQUENCY RESPONSE[2,4]		
Bandwidth for 1% Additional Error (0.2dB)		
V_{IN} = 10mV	12kHz	*
V_{IN} = 100mV	80kHz	*
V_{IN} = 200mV	130kHz	*
±3dB Bandwidth		
V_{IN} = 10mV	80kHz	*
V_{IN} = 100mV	800kHz	*
V_{IN} = 200mV	1.3MHz	*
AVERAGING TIME CONSTANT	25ms/μF	*
INPUT CHARACTERISTICS		
Signal Range		
+3, -5V Supply	±2.8V Peak	*
±2.5V Supply	±2V Peak	*
±5V Supply	±5V Peak	*
Safe Input, All Supply Voltage	±12V max	*
Input Resistance	6.7kΩ ±20%	*
Input Offset Voltage	0.5mV max	0.2mV max
OUTPUT CHARACTERISTICS[2]		
Offset Voltage	0.5mV max	0.2mV max
vs. Temperature	±10μV/°C	*
vs. Supply	±0.1mV/V	*
Voltage Swing		
+3, -5V Supply	0 to 1V typ (0.3V min)	*
±5V Supply	0 to 1.4V typ (0.3V min)	*
Output Impedance	10kΩ ±20% typ	*
dB OUTPUT		
Error, $7mV \leq V_{IN} \leq 300mV$ rms	±0.5dB max	±0.2dB max
Scale Factor	-3mV/dB	*
Scale Factor Temperature Coefficient	+0.3%/°C(-0.03dB/°C)	*
I_{REF} for 0dB = 0.1V rms	4μA (2μA min, 8μA max)	*
I_{REF} Range	1μA to 50μA	*
I_{OUT} TERMINAL		
I_{OUT} Scale Factor	100μA/V rms	*
I_{OUT} Scale Factor Tolerance	±20%	*
Output Resistance	10^8 Ω	*
Voltage Compliance	$-V_S$ to ($+V_S$ -2V)	*
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to ($+V_S$ -2V) min	*
Input Offset Voltage, R_S = 10k	2mV max	1mV max
Input Current	100nA typ (300nA max)	*
Input Resistance	10^8 Ω	*
Output Current	(+5mA, -130μA) min	*
Short Circuit Current	20mA	*
Small Signal Bandwidth	1MHz	*
Slew Rate[5]	5V/μs	*
POWER SUPPLY		
Voltage, Rated Performance	+3, -5V	*
Dual Supply	+2/-2.5V to ±12V	*
Single Supply	+5V to +24V	*
Quiescent Current[6]	800μA (1mA max)	*
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Storage	-55°C to +150°C	*
PACKAGE OPTIONS[7]		
"H" Package: TO-100	AD636JH	AD636KH
"D" Package: TO-116 Style D14A	AD636JD	AD636KD

NOTES
[1] Accuracy is specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels.
[2] Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.
[3] Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.
[4] Input voltages are expressed in volts rms.
[5] With 10kΩ pull-down resistor from pin 6 (BUF OUT) to $-V_S$.
[6] With BUF input tied to $-V_S$.
[7] See Section 19 for package outline information.
*Specifications same as AD636J.

Specifications subject to change without notice.

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100μA per volt rms input, positive out.

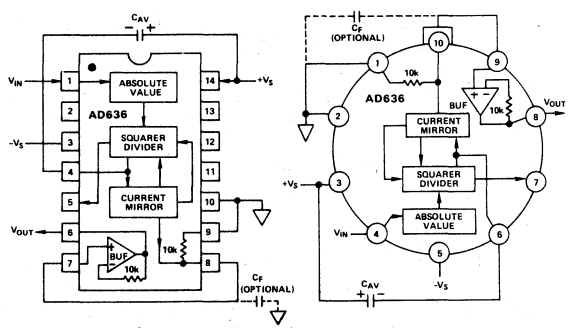


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

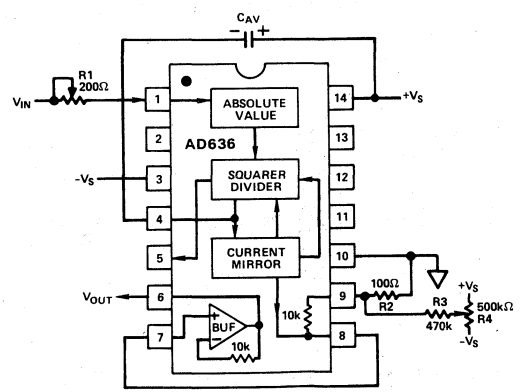


Figure 2. Optional External Gain and Output Offset Trims

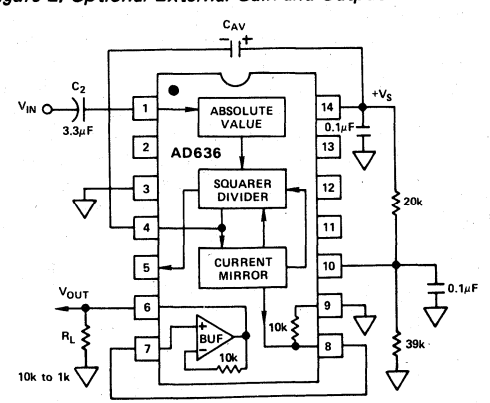


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by an average (or dc) error and some amount of ripple, as demonstrated in Figure 4.

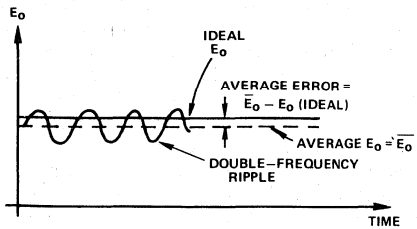


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield 1% or 0.1% dc error above a given frequency. For example, if a 60Hz waveform is to be measured with a dc error of less than 0.1%, C_{AV} must be greater than 0.65μF. If a 1% error can be tolerated, the minimum value of C_{AV} is 0.22μF.

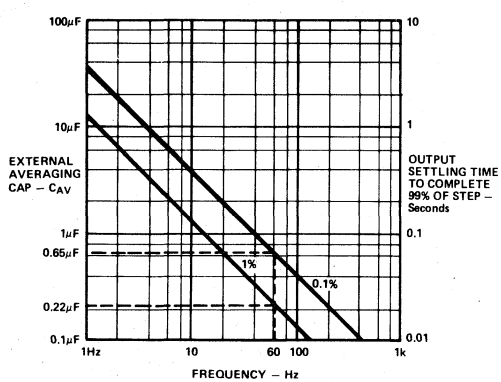


Figure 5. Lower Frequency for Stated % of Reading Error and Settling Time for Circuit Shown in Figure 1

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

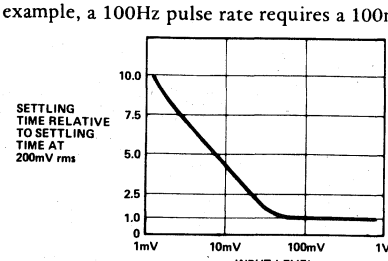


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and settling time is 100 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 4.7μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

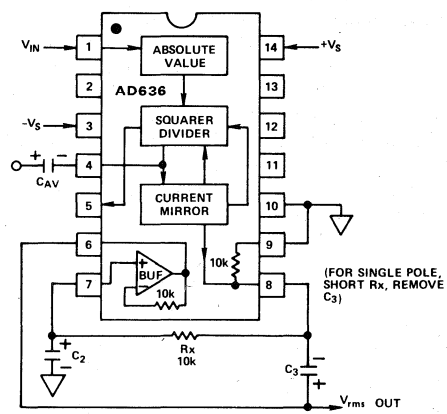


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

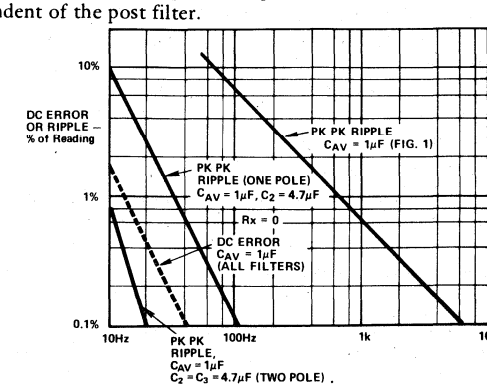


Figure 8. Performance Features of Various Filter Types

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN} \text{ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

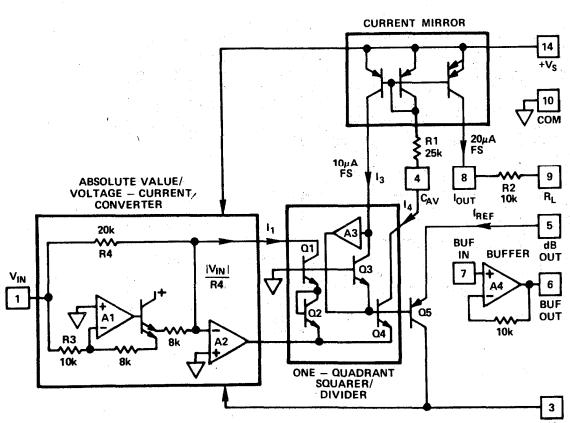


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

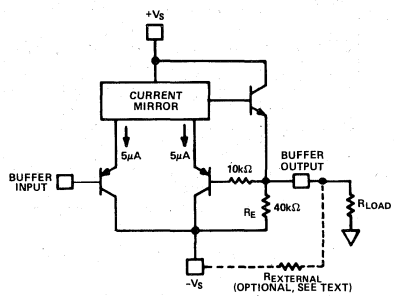


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S = -5V$.

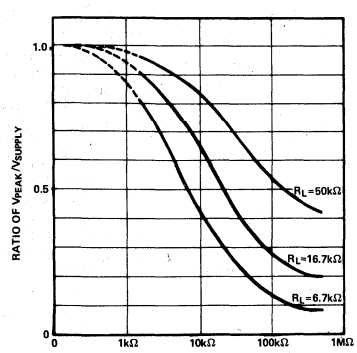


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 200kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 12kHz.

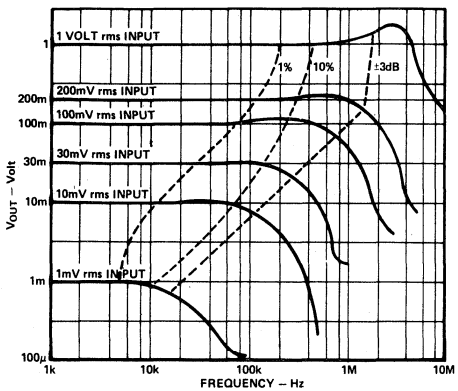


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

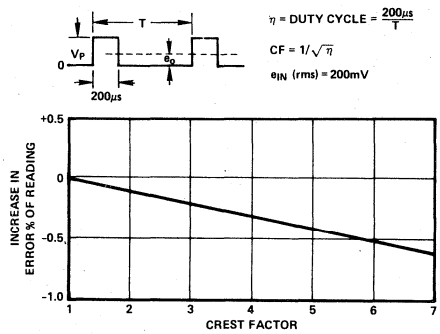


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

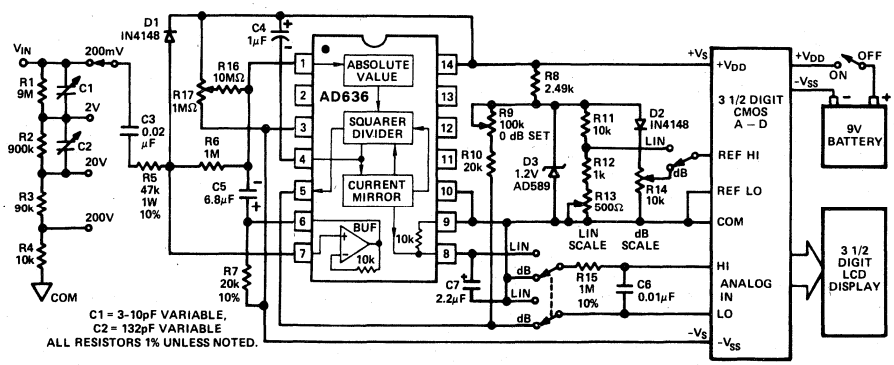


Figure 14. 3 1/2 Digit True rms ac Voltmeter

High Precision Wideband rms-to-dc Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Max Error to Crest Factor of 3**

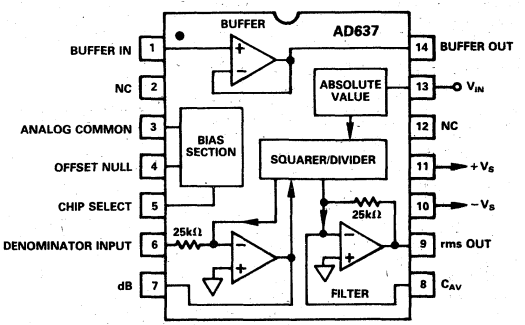
Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (−60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiesent Current Reduction from 2.2mA to 350μA**

AD637 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 2V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C temperature range. All versions are available in ceramic 14-lead DIP packages.

PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD637AJ			AD637AK			AD637AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig. 2)[1]			**±1 ±0.5**			**±0.5±0.2**			**±1 ±0.5**	mV ± % of Reading
T_{min} to T_{max}			**±3.0 ±0.6**			**±2.0 ±0.3**			**±6 ±0.7**	mV ± % of Reading
vs. Supply +		30	**150**		30	**150**		30	**150**	µ/V
vs. Supply −		100	**300**		100	**300**		100	**300**	µ/V
dc Reversal Error			**0.25**			**0.1**			**0.25**	% of Reading
Nonlinearity 2V Full Scale[2]			**0.04**			**0.02**			**0.04**	% of FSR
Nonlinearity 7V Full Scale			**0.05**			**0.05**			**0.05**	% of FSR
Total Error, External Trim		±0.5 ±0.1			±0.25 ±0.05			±0.5 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0.1			±0.1			±0.1		% of Reading
Crest Factor = 10		±1.0			±1.0			±1.0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF CAV
INPUT CHARACTERISTICS										
Signal Range, ±15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ±5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Non-Destructive										
Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance		8			8			8		kΩ
Input Offset Voltage			**±0.5**			**±0.2**			**±0.5**	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0.1dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		97			200			200		kHz
= 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs. Temperature		±0.05			±0.05			±0.05		mV/°C
Voltage Swing, ±15V Supply,										
2kΩ Load	**0 to +13.5**			**0 to +13.5**			**0 to +13.5**			V
Voltage Swing, ±5V Supply,										
2kΩLoad	0 to +2			0 to +2			0 to +2			V
Output Current	5			5			5			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0.5			0.5			0.5		Ω
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±1			±1			±1		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC		−0.3			−0.3			−0.3		% of Reading/°C
I_{REF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	µA
I_{REF} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2.5V)			V
Input Offset Voltage		±0.8	**±2**		±0.8	**±1**		±0.8	**±2**	mV
Input Current		±2	**±10**		±2	**±5**		±2	**±10**	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130µA)			(+5mA, −130µA)			(+5mA, −130µA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to 2			0 to 2			0 to 2		V
Input Impedance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage			**±0.5**			**±0.5**			**±0.5**	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level	Open or $+2.4V<V_C<+V_S$			Open or $+2.4V<V_C<+V_S$			Open or $+2.4V<V_C<+V_S$			
rms "OFF" Level	$V_C<+0.2V$			$V_C<+0.2V$			$V_C<+0.2V$			
I_{OUT} of Chip Select										
CS "LOW"	10			10			10			µA
CS "HIGH"	Zero			Zero			Zero			
On Time	$10\mu s + ((25k\Omega) \times C_{AV})$			$10\mu s + ((25k\Omega) \times C_{AV})$			$10\mu s + ((25k\Omega) \times C_{AV})$			
Off Time	$10\mu s + ((25k\Omega) \times C_{AV})$			$10\mu s + ((25k\Omega) \times C_{AV})$			$10\mu s + ((25k\Omega) \times C_{AV})$			

Model	AD637AJ			AD637AK			AD637AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	mA

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 1.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms.
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Package[1]
AD637JD	0 to +70°C	Ceramic DIP (D14A)
AD637KD	0 to +70°C	Ceramic DIP (D14A)
AD637SD	−55°C to +125°C	Ceramic DIP (D14A)

NOTE
[1]See Section 19 for package outline information.

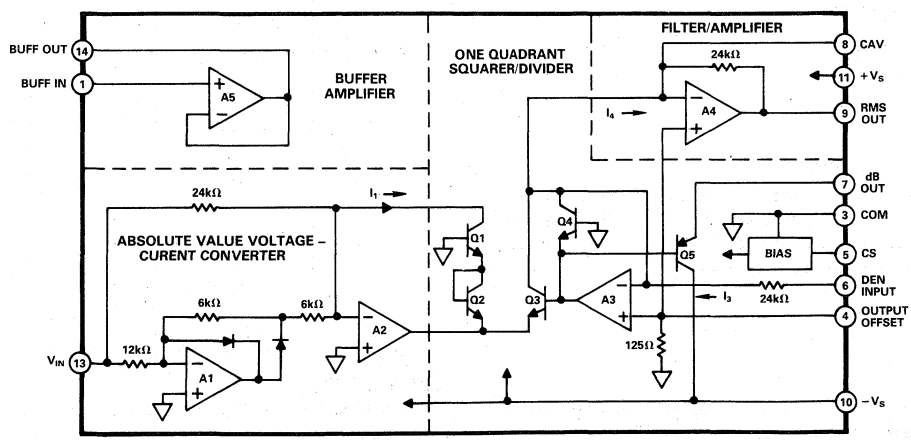


Figure 1. Simplified Schematic

FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ rms = Avg\left[\frac{V_{IN}^2}{V\ rms}\right]$$

Figure 1 is a simplified schematic of the AD637, it is subdivided into four major sections; absolute value circuit (active rectifier), square/divider, filter circuit and buffer amplifier. The input voltage V_{IN} which can be ac or dc is converted to a unipolar current I1 by the active rectifier A1, A2. I1 drives one input of the squarer divider which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider, I4 drives A4 which forms a low pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal than A4s output will be proportional to the average of I4. The output of this filter amplifier is used by A3 to provide the denominator current I3 which equals Avg. I4 and is returned to the squarer/divider to complete the implicit rms computation.

$$I_4 = Avg\left[\frac{I_1^2}{I_4}\right] = I_1\ rms$$

and

$$V_{OUT} = V_{IN}\ rms$$

If the averaging capacitor is omitted the AD637 will compute the absolute value of the input signal. A nominal 100pF capacitor should be used to insure stability. The circuit operates identically to that of the rms configuration except that I3 is now equal to I4 giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to pin 6. The circuit operates identically to the rms case except that I3 is now proportional to V_{REF}. Thus:

$$I_4 = Avg\ \frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

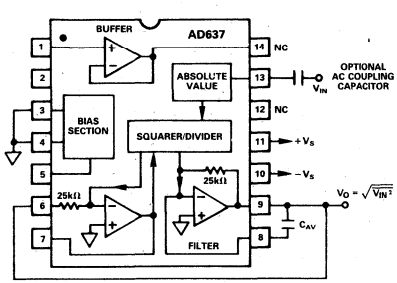


Figure 2. Standard rms Connection

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor will be present at low frequencies. For example, if the filter capacitor C_{AV}, is 4μF this error will be 0.1% at 10Hz and decreases to 1% at 3Hz. If it is desired to measure only ac signals the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

The performance of the AD637 is tolerant of minor variations in the power supply voltages, however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1μF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. The output of the AD637 is capable of driving 5mA into a 2kΩ load without degrading the accuracy of the device.

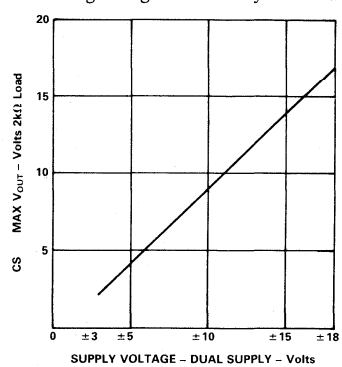


Figure 3. AD637 max V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature which allows the user to decrease the quiescent current of the device from 2.2mA to 350μA. This is done by driving the CS, pin 5, to below 0.2V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, pin 5 should be tied high or left floating.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal, V_{IN} and adjust R1 to give 0V output from pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input to V_{IN}, using either a dc or a calibrated ac signal, trim R3 to give the correct output at pin 9, i.e., 1V dc should give 1.000V dc output. Of course, a 2V peak-to-peak sine wave should give 0.707V dc output. Remaining errors are due to the nonlinearity.

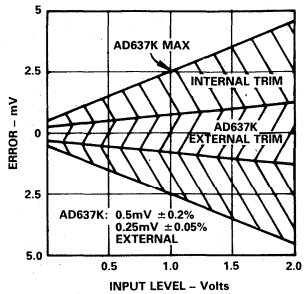


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

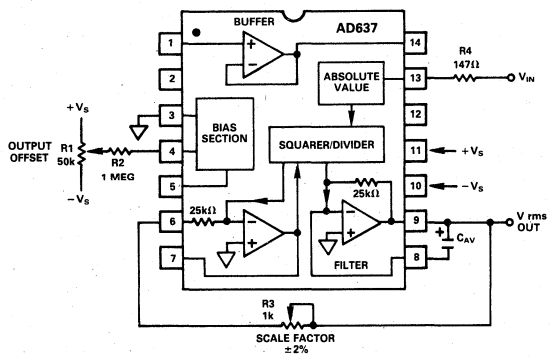


Figure 5. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f, and the averaging time constant τ (τ: 25ms/μF of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

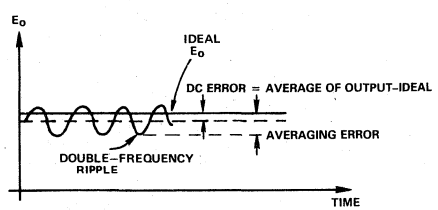


Figure 6. Typical Output Waveform for a Sinusoidal Input

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3\tau f} \text{ in \% of reading where } (\tau > 1/f)$$

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4\tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and will not be affected by post filtering.

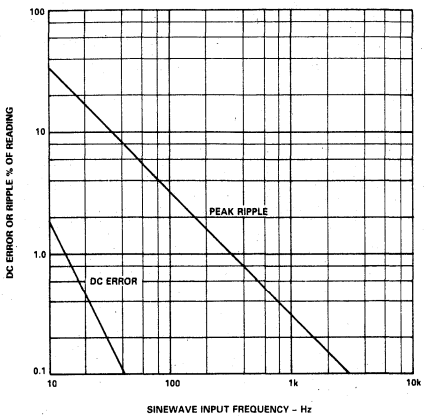


Figure 7. Comparison of Percent dc Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard rms Connection with a 1μF C_{AV}

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115ms/μF of averaging capacitance). A preferrable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

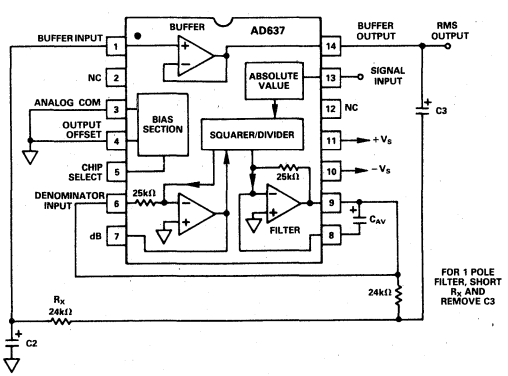


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of C_{AV} and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50Hz. As an example, by using a 1μF averaging capacitor and a 3.3μF filter capacitor the ripple for a 60Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of C_{AV} and C_2, the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

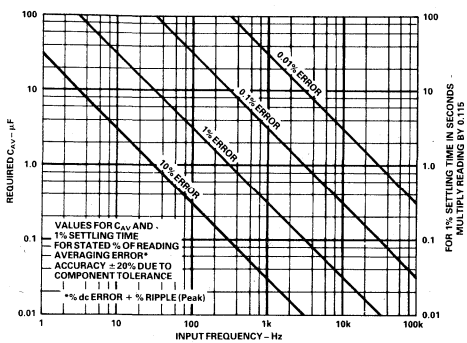


Figure 9a.

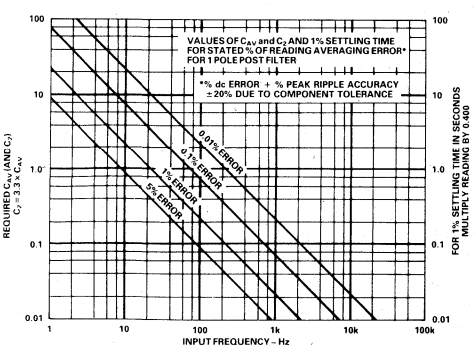


Figure 9b.

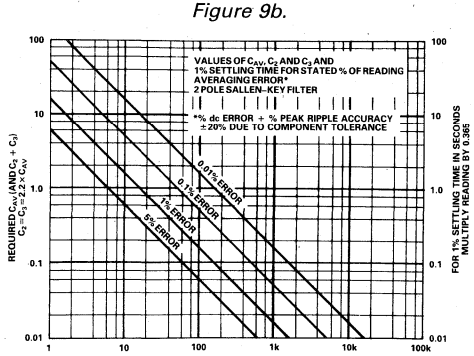


Figure 9c.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60Hz input signals. These capacitor values can be directly scaled for frequencies other than 60Hz, i.e., for 30Hz double these values, for 120Hz they are halved.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error@ 60Hz with T = 16.6ms		1% Settling Time
				Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	Symmetrical Sine Wave	1/2T	1/2T	0.47μF	1.5μF	181ms
B	Sine Wave with dc Offset	T	T	0.82μF	2.7μF	325ms
C	Pulse Train Waveform	T, T_2	$10(T - T_2)$	6.8μF	22μF	2.67sec
D		T, T_2	$10(T - 2T_2)$	5.6μF	18μF	2.17sec

Table I. Practical Values of C_{AV} and C2 for Various Input Waveforms

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of C_{AV}, C_2 and C_3 for the desired level of ripple and settling time.

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10% and ±3dB of additional error. For example, note that for 1% additional error with a 2V rms input the highest frequency allowable is 200kHz. A 200mV signal can be measured with 1% error at signal frequencies up to 100kHz.

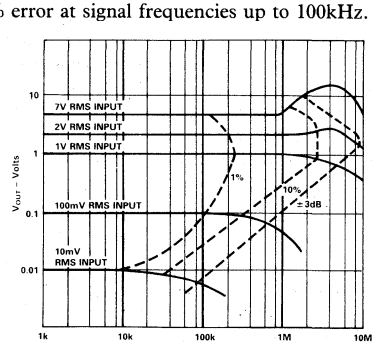


Figure 10. Frequency Response

To take full advantage of the wide bandwidth of the AD637 care must be taken in the selection of the input buffer amplifier. To insure that the input signal is accurately presented to the converter, the input buffer must have a −3dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1V rms 5MHz sine-wave input signal is 44V/μs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier as

some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD381 is recommended as a precision input buffer.

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤ 2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

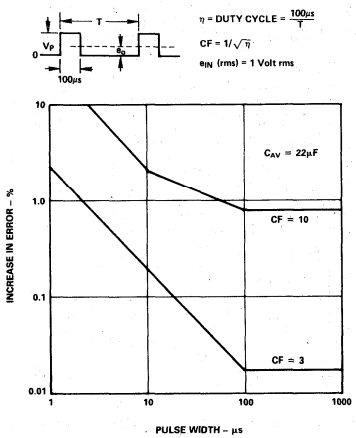


Figure 11. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

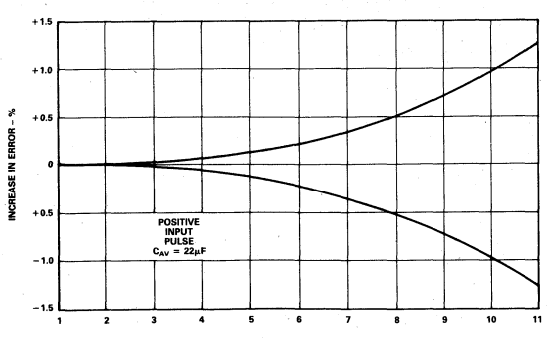


Figure 12. Additonal Error vs. Crest Factor

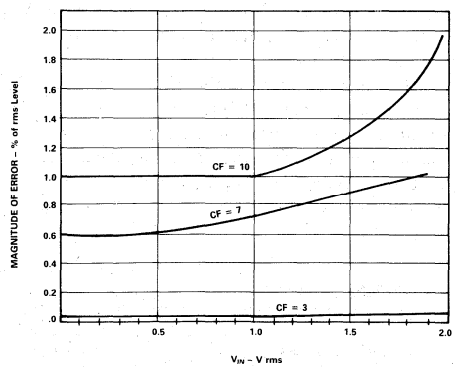


Figure 13. Error vs. rms Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic or decibel output. The internal circuit which computes dB works well over a 60dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0dB level by setting R1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the 0.3%/°C temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londenderry, New Hampshire (model Q-81) and from Precision Resistor Inc., Hillside, N.J. (model PT146).

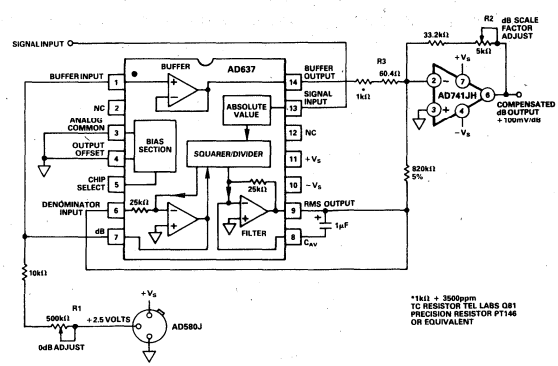


Figure 14. dB Connection

dB CALIBRATION

1. Set V_{IN} = 1.00V dc
2. Adjust R1 for 0dB out = 0.00V
3. Set V_{IN} = 0.1V dc
4. Adjust R2 for dB out = 2.00V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. The circuit shown in Figure 15 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5ms/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two pole Sallen-Key filter shown in the diagram be used to obtain a low ripple level and minimize the value of the averaging capacitor.

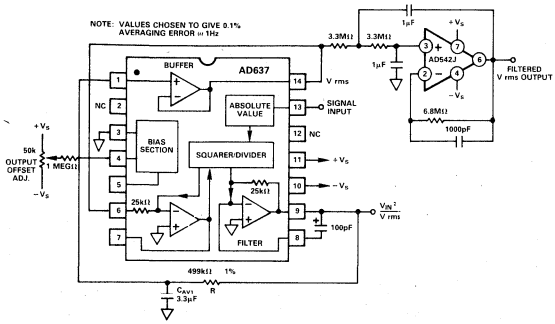


Figure 15. AD637 as a Low Frequency rms Converter

If the frequency of interest is below 1Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done it is suggested that a low input current, low offset voltage amplifier like the AD542 be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s as shown in Figure 16. Here the averaging capacitors are omitted (nominal 100pF capacitors are used to insure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

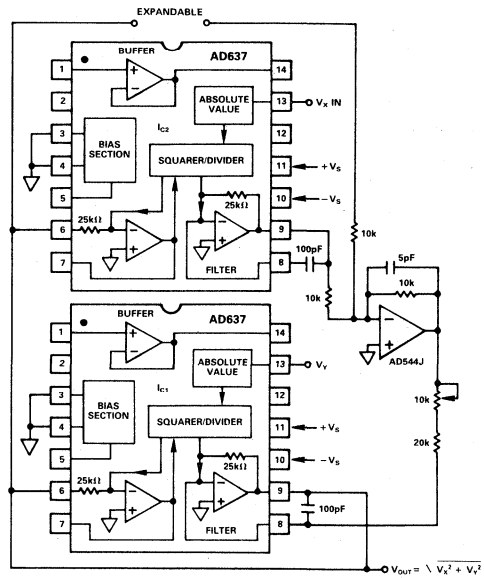


Figure 16. AD637 Vector Sum Configuration

This concept can be expanded to include additional terms by feeding the signal from pin 9 of each additional AD637 through a 10kΩ resistor to the summing junction of the AD544, and tying all of the denominator inputs (pin 6) together.

If C_{AV} is added to IC1 in this configuration the output is $\sqrt{V_X^2 + V_Y^2}$ If the averaging capacitor is included on both IC1 and IC2 the output will be $\sqrt{\overline{V_X^2} + \overline{V_Y^2}}$

This circuit has a dynamic range of 10V to 10mV and is limited only by the 0.5mV offset voltage of the AD637. The useful bandwidth is 100kHz.

Voltage References

Contents

Selection Guide
Voltage References

		AD589	AD580	AD1403	AD581	AD584	AD2700	AD2710
Output Voltage Range	1.235V	•				•		
	2.5V		•	•		•		
	5.0V					•		
	7.5V					•		
	+10.00V				•	•	•	•
	-10.00V						•	
	±10.00V						•	•
Output Voltage Tolerance	⩽±0.4%		•	•	•	•	•	•
	⩽±0.05%				•	•	•	•
	⩽±0.025%						•	•
	⩽±0.012%							•
Temperature Stability	⩽25ppm/°C	•	•	•	•	•	•	•
	⩽10ppm/°C		•		•	•	•	•
	⩽5ppm/°C				•	•	•	•
	⩽1ppm/°C							•
Temperature Range	0 to +70°C	•	•	•	•	•	•	•
	-25°C to +85°C						•	
	-55°C to +125°C	•	•		•	•		
Package Style	Hermetic Package	•	•		•	•	•	•
	Plastic Package			•				
Dice Available		•	•		•	•		
Volume I Page		7-25	7-5	7-29	7-9	7-17	7-33	7-37

Orientation
Voltage References

A voltage reference is used to provide an accurately known voltage which can be utilized in a circuit or system. For example, measurement systems rely on precision references in order to establish a basis for absolute measurement accuracy. Any reference inaccuracy will undermine the accuracy of the overall system. Thus, ideal references are characterized by accurately set (and traceable to recognized fundamental standards) constant output voltage, independent of temperature, load changes, input voltage variation, and time.

Types of References

The majority of available IC reference circuits use the bandgap principle: the V_{BE} of any silicon transistor has a negative tempco of about 2mV/°C, which can be extrapolated to approximately 1.2 volts at absolute zero (the *bandgap* voltage of silicon). Since identical transistors operating at constant current densities will have predictably different temperature coefficients of base-emitter voltage, it is possible to arrange circuit elements so as to null out the temperature coefficients associated with the two phenomena and produce a constant voltage (usually 1.2 volts). This temperature-invariant voltage can be amplified and buffered to produce a standard voltage value, such as 2.5V or 10.0V. The bandgap types catalogued here include the AD1403 and the AD580 (2.5V), the AD581 (10.0V), and the multi-output AD584 (2.5, 5.0, 7.5, and/or 10.0V).

Another popular form of reference circuit uses a selected low-drift Zener diode, followed by a buffer-amplifier-and-precision-gain stage to provide a standard output voltage. The AD2710, AD2712 families provide +10V and ±10V (dual output) using this technique. Laser-trimmed thin-film resistors are essential to secure ±1mV accuracy and ±1ppm/°C max drift in these hybrid devices.

The AD589 family are two-terminal 1.2V bandgap ICs used like Zener diodes. They are ideally suited to battery-powered instruments or portable equipment where low power consumption (and often low supply voltages) are essential. Power requirements as low as 60μW, combined with low temperature drift, provide precision performance at low cost.

Definitions of Specifications

Line regulation. The change in output voltage due to a specified change in input voltage. It is usually expressed in percent per volt or microvolts per volt of input change.

Load regulation. The change in output voltage for a specified change in load current. It is generally expressed in microvolts per milliampere, or ohms of dc output resistance. This specification includes the effect of self-heating due to increased power dissipation at higher load currents.

Output voltage tolerance. The deviation from the nominal output voltage at 25°C and specified input voltage as measured by a device traceable to a recognized fundamental voltage standard.

Output voltage change with temperature. The change in output voltage from the value at 25°C ambient; it is independent of variations in the other operating conditions. Analog Devices specifies both an error band and an equivalent temperature coefficient (in ppm/°C) for most references. The error band (e.g., ±5mV, −55°C to +125°C), is defined graphically in terms of a box (voltage vertically, temperature horizontally) whose diagonals extend from 25°C to T_{max} and 25°C to T_{min}, with a slope equal to the stated temperature coefficient. Thus, the total absolute error for a particular reference over its specified temperature range is equal to the output voltage tolerance at 25°C plus the error band.

Turn-on settling time. The time, from a cold start, for the reference output to settle within a specified error band. This definition relates only to the electrical turn-on of the chip, and does not include thermal settling time, which depends on the package, heat-sinking, and load-current change.

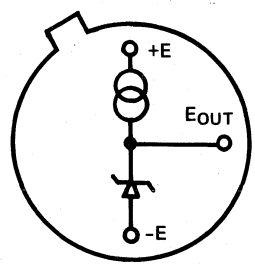
High Precision 2.5 Volt IC Reference

AD580*

FEATURES

- Laser Trimmed to Higher Accuracy: 2.500V ±0.4%, Improved from ±1.0% (AD580M)
- 3-Terminal Device: Voltage In/Voltage Out
- Excellent Temperature Stability: 10ppm/°C (AD580M, U)
- Excellent Long Term Stability: 250μV (25μV/Month)
- Low Quiescent Current: 1.5mA max
- Small, Hermetic IC Package: TO-52 Can

AD580 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD580 is an improved three-terminal, low cost, temperature compensated, bandgap voltage reference which provides a fixed 2.5V output for inputs between 4.5V and 30V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provide the AD580 with an improved initial tolerance of ±0.4%, a temperature stability of better than 10ppm/°C and long term stability of better than 250μV. In addition, the low quiescent current drain of 1.5mA max offers a clear advantage over classical zener techniques.

The AD580 is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD580 allows operation with 5 volt logic supplies making the AD580 ideal for digital panel meter applications or whenever only a single logic power supply is available.

The AD580J, K, L and M are specified for operation over the 0 to +70°C temperature range; the AD580S, T and U are specified for operation over the extended temperature range of −55°C to +125°C.

*Covered by Patent Nos. 3,887,863; RE30,586.

PRODUCT HIGHLIGHTS

1. Laser-trimming the thin-film resistors has reduced the AD580 output error. For example, AD580L output tolerance is now ±10mV, improved from ±50mV.
2. The three-terminal voltage in/voltage out operation of the AD580 provides regulated output voltage without any external components.
3. The AD580 provides a stable 2.5V output voltage for input voltages between 4.5V and 30V. The capability to provide a stable output voltage using a 5-volt input makes the AD580 an ideal choice for systems that contain a single logic power supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD580 with temperature stabilities to 10ppm/°C and long term stability better than 250μV.
5. The low quiescent current drain of the AD580 makes it ideal for CMOS and other low power applications.

SPECIFICATIONS (@ E_{IN} and 25°C)

Model	AD580J Min	AD580J Typ	AD580J Max	AD580K Min	AD580K Typ	AD580K Max	AD580L Min	AD580L Typ	AD580L Max	AD580M Min	AD580M Typ	AD580M Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±75			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE													
T_{min} to T_{max}			15			7			4.3			1.75	mV
			85			40			25			10	ppm/°C
LINE REGULATION													
$7V \leq V_{IN} \leq 30V$		1.5	6		1.5	4			2			2	mV
$4.5V \leq V_{IN} \leq 7V$		0.3	3		0.3	2			1			1	mV
LOAD REGULATION													
ΔI = 10mA			10			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		60			60			60			60		μV (p-p)
STABILITY													
Long Term		250			250			250			250		μV
Per Month		25			25			25			25		μV
TEMPERATURE PERFORMANCE													
Specified	0		+70	0		+70	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	−65		+175	−65		+175	°C
PACKAGE OPTION[1] – TO-52	AD580JH			AD580KH			AD580LH			AD580MH			

Model	AD580S Min	AD580S Typ	AD580S Max	AD580T Min	AD580T Typ	AD580T Max	AD580U Min	AD580U Typ	AD580U Max	Units
OUTPUT VOLTAGE TOLERANCE (Error from Nominal 2.500 Volt Output)			±25			±10			±10	mV
OUTPUT VOLTAGE CHANGE										
T_{min} to T_{max}			25			11			4.5	mV
			55			25			10	ppm/°C
LINE REGULATION										
$7V \leq V_{IN} \leq 30V$		1.5	6			2			2	mV
$4.5V \leq V_{IN} \leq 7V$		0.3	3			1			1	mV
LOAD REGULATION										
ΔI = 10mA			10			10			10	mV
QUIESCENT CURRENT		1.0	1.5		1.0	1.5		1.0	1.5	mA
NOISE (0.1Hz to 10Hz)		60			60			60		μV (p-p)
STABILITY										
Long Term		250			250			250		μV
Per Month		25			25			25		μV
TEMPERATURE PERFORMANCE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−55		+150	−55		+150	−55		+150	°C
Storage	−65		+175	−65		+175	−65		+175	°C
ABSOLUTE MAXIMUM RATINGS										
Input Voltage	40V									
Power Dissipation @ + 25°C										
Ambient Temperature	350mW									
Derate above + 25°C	2.8mW/°C									
Lead Temperature (Soldering, 10 sec)	300°C									
Thermal Resistance										
Junction-to-Case	100°C/W									
Junction-to-Ambient	360°C/W									
PACKAGE OPTION[1] – TO-52	AD580SH			AD580TH			AD580UH			

NOTES

[1]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

THEORY OF OPERATION

Most precision IC references use complex multichip hybrid designs based on expensive temperature-compensated zener diodes. Others are monolithic with on-chip zener diodes; these often require more than one power supply and, with the zener breakdown occuring near 6.3 volts, will not operate from a low voltage logic supply.

The AD580 family (AD580, AD581, AD584, AD589) uses the "bandgap" concept to produce a stable, low-temperature-coefficient voltage reference suitable for high accuracy data-acquisition components and systems. The device makes use of the underlying physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a -2mV/°C temperature coefficient, unsuitable for use directly as a low TC reference; however, extrapolation of the temperature characteristic of any one of these devices to absolute zero (with emitter current proportional to absolute temperature) reveals that it will go to a V_{BE} of 1.205 volts 0K, as shown in Figure 1. Thus, if a voltage could be developed with an opposing temperature coefficient to sum with V_{BE} to total 1.205 volts, a zero-TC reference would result and operation from a single, low-voltage supply would be possible. The AD580 circuit provides such a compensating voltage, V_1 in Figure 2, by driving two transistors at different current densities and amplifying the resulting V_{BE} difference (ΔV_{BE} – which now has a positive TC); the sum (V_Z) is then buffered and amplified up to 2.5 volts to provide a usable reference-voltage output. Figure 3 is the schematic diagram of the AD580.

The AD580 operates as a three-terminal reference, that means that no additional components are required for biasing or current setting. The connection diagram, Figure 4 is quite simple.

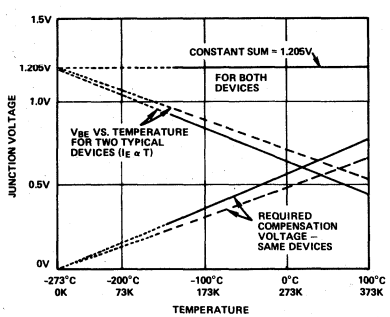


Figure 1. Extrapolated Variation of Base-Emitter Voltage with Temperature ($I_E \alpha T$), and Required Compensation, Shown for Two Different Devices

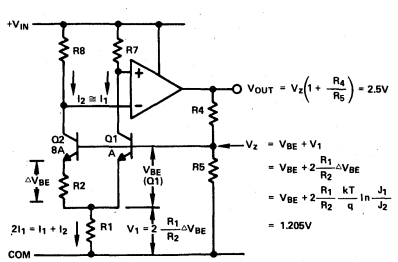


Figure 2. Basic Bandgap-Reference Regulator Circuit

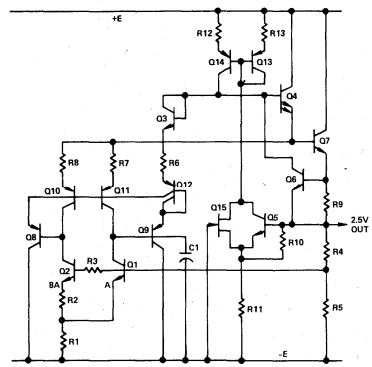


Figure 3. AD580 Schematic Diagram

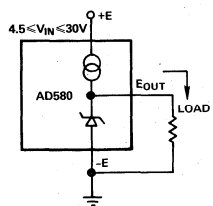


Figure 4. AD580 Connection Diagram

VOLTAGE VARIATION VS. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consistent Voltage vs. Temperature performance of a typical AD580 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

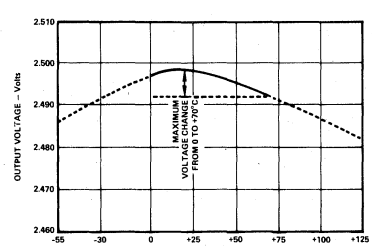


Figure 5. Typical AD580K Output Voltage vs. Temperature

The AD580M guarantees a maximum deviation of 1.75mV over the 0 to +70°C temperature range. This can be shown to be equivalent to 10ppm/°C average maximum; i.e. . .

$$\frac{1.75\text{mV max}}{70^\circ\text{C}} \times \frac{1}{2.5\text{V}} = 10\text{ppm}/^\circ\text{C max average}$$

The AD580 typically exhibits a variation of 1.5mV over the power supply range of 7 to 30 volts. Figure 6 is a plot of AD580 line rejection versus frequency.

NOISE PERFORMANCE

Figure 7 represents the peak-to-peak noise of the AD580 from 1Hz (3dB point) to a 3dB high end shown on the horizontal axis. Peak-to-peak noise from 1Hz to 1MHz is approximately 600μV.

THE AD580 AS A CURRENT LIMITER

The AD580 represents an excellent alternative to current limiter diodes which require factory-selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD580 approach is not limited to a specially selected factory set current limit; it can be programmed from 1 to 10mA with the insertion of a single external resistor. The approximate temperature coefficient of current limit for the AD580 used in this mode is 0.13%/°C for I_{LIM} = 1mA and 0.01%/°C for I_{LIM} = 13mA (see Figure 9). Figure 8 displays the high output impedance of the AD580 used as a current limiter for I_{LIM} = 1, 2, 3, 4, 5mA.

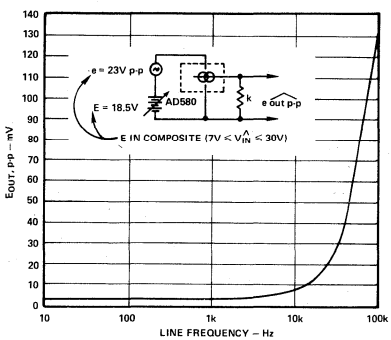


Figure 6. AD580 Line Rejection Plot

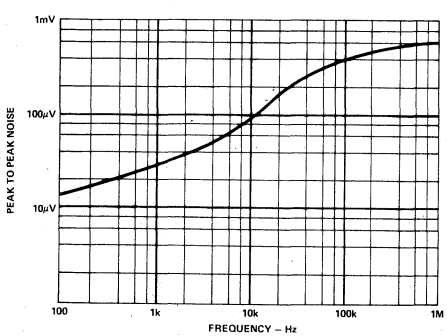


Figure 7. Peak-to-Peak Output Noise vs. Frequency

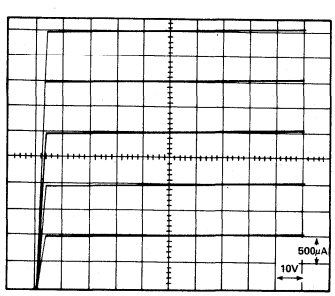


Figure 8. Input Current vs. Input Voltage (Integral Loads)

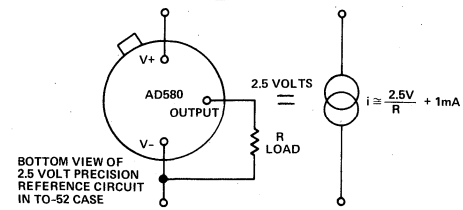


Figure 9. A Two-Component Precision Current Limiter

THE AD580 AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD580 has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

Figure 10 shows the AD580 used as a reference for the AD7542 12-bit CMOS DAC with complete microprocessor interface. The AD580 and the AD7542 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7542 includes three 4-bit data registers, a 12-bit DAC register, and address decoding logic; it may thus be interfaced directly to a 4-, 8- or 16-bit data bus. Only 8mA of quiescent current from the single +5 volt supply is required to operate the AD7542 which is packaged in a small 16-pin DIP. The AD544 output amplifier is also low power, requiring only 2.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7542KN without user trims and it typically settles to ±1/2 LSB in less than 3μs. It will provide the 0 to −2.5 volt output swing from ±5 volt supplies.

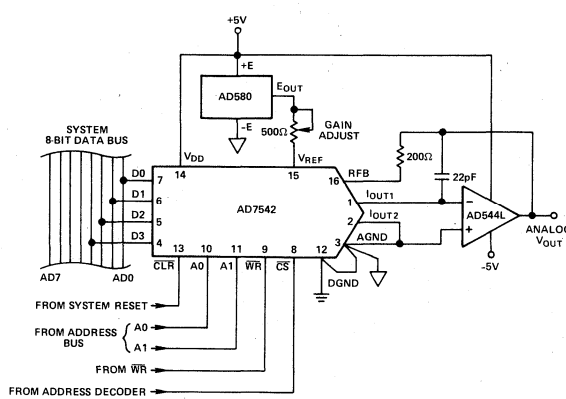


Figure 10. Low Power, Low Voltage Reference for the AD7542 Microprocessor-Compatible 12-Bit DAC

ANALOG DEVICES

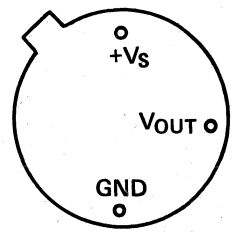
High Precision 10 Volt IC Reference

AD581*

FEATURES

- Laser-Trimmed to High Accuracy:
  - 10.000 Volts ±5mV (L and U)
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (L)
  - 10ppm/°C max, -55°C to +125°C (U)
- Excellent Long-Term Stability:
  - 25ppm/1000 hrs. (Non-Cumulative)
- Negative 10 Volt Reference Capability
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability
- 3-Terminal TO-5 Package

AD581 PIN CONFIGURATION



TO-5
BOTTOM VIEW

PRODUCT DESCRIPTION

The AD581 is a three-terminal, temperature compensated, monolithic band-gap voltage reference which provides a precise 10.00 volt output from an unregulated input level from 12 to 30 volts. Laser Wafer Trimming (LWT) is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in high precision performance previously available only in expensive hybrids or oven-regulated modules. The 5mV initial error tolerance and 5ppm/°C guaranteed temperature coefficient of the AD581L represent the best performance combination available in a monolithic voltage reference.

The band-gap circuit design used in the AD581 offers several advantages over classical zener breakdown diode techniques. Most important, no external components are required to achieve full accuracy and stability of significance to low power systems. In addition, total supply current to the device, including the output buffer amplifier (which can supply up to 10mA) is typically 750μA. The long-term stability of the band-gap design is equivalent or superior to selected zener reference diodes.

The AD581 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD581J, K, and L are specified for operation from 0 to +70°C; the AD581S, T, and U are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed three-terminal TO-5 metal can.

PRODUCT HIGHLIGHTS

1. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD581L has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C, while the AD581U guarantees ±15mV maximum total error without external trims from -55°C to +125°C.
2. Since the laser trimming is done on the wafer prior to separation into individual chips, the AD581 will be extremely valuable to hybrid designers for its ease of use, lack of required external trims, and inherent high performance.
3. The AD581 can also be operated in a two-terminal "Zener" mode to provide a precision negative 10 volt reference with just one external resistor to the unregulated supply. The performance in this mode is nearly equal to that of the standard three-terminal configuration.
4. Advanced circuit design using the band-gap concept allows the AD581 to give full performance with an unregulated input voltage down to 13 volts. With an external resistor, the device will operate with a supply as low as 11.4 volts.

*Covered by Patent Nos. 3,887,863; RE 30,586

SPECIFICATIONS (@ V_{IN} = +15V and 25°C)

Model	AD581J			AD581K			AD581L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±13.5**			**±6.75**			**±2.25**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			5	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			µA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Specified	0		+70	0		+70	0		+70	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE: TO-5[2]	AD581JH			AD581KH			AD581LH			

NOTES

[1]See Figure 6.

[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD581S			AD581T			AD581U			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE (Error from nominal 10,000V output)			**±30**			**±10**			±5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C			**±30**			**±15**			**±10**	mV
Value, T_{min} to T_{max} (Temperature Coefficient)			30			15			10	ppm/°C
LINE REGULATION										
$15V \leq V_{IN} \leq 30V$			**3.0**			**3.0**			**3.0**	mV
			(0.002)			(0.002)			(0.002)	%/V
$13V \leq V_{IN} \leq 15V$			**1.0**			**1.0**			**1.0**	mV
			(0.005)			(0.005)			(0.005)	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$		200	**500**		200	**500**		200	**500**	µV/mA
QUIESCENT CURRENT		0.75	**1.0**		0.75	**1.0**		0.75	**1.0**	mA
TURN-ON SETTLING TIME TO 0.1%[1]		200			200			200		µs
NOISE (0.1 to 10Hz)		50			50			50		µV/p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 hrs.
SHORT CIRCUIT CURRENT		30			30			30		mA
OUTPUT CURRENT										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	200			200			200			µA
Sink −55°C to +85°C	5			5			5			mA
TEMPERATURE RANGE										
Specified	−55		+125	−55		+125	−55		+125	°C
Operating	−65		+150	−65		+150	−65		+150	°C
PACKAGE: TO-5[2]	AD581SH			AD581TH			AD581UH			

NOTES
[1]See Figure 6.
[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD581

APPLYING THE AD581

The AD581 is easy to use in virtually all precision reference applications. The three terminals are simply primary supply, ground, and output, with the case grounded. No external components are required even for high precision applications; the degree of desired absolute accuracy is achieved simply by selecting the required device grade. The AD581 requires less than 1mA quiescent current from an operating supply range of 12 to 30 volts.

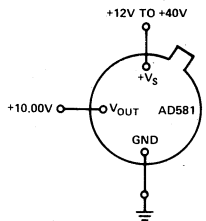
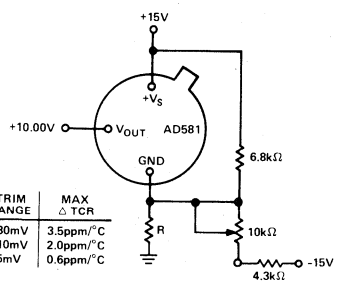


Figure 1. AD581 Pin Configuration (Top View)

An external fine trim may be desired to set the output level to exactly 10.000 volts within less than a millivolt (calibrated to a main system reference). System calibration may also require a reference slightly different from 10.00 volts. In either case, the optional trim circuit shown in Figure 2 can offset the output by up to ±30 millivolts (with the 22Ω resistor), if needed, with minimal effect on other device characteristics.



R	TRIM RANGE	MAX △ TCR
22Ω	±30mV	3.5ppm/°C
12Ω	±10mV	2.0ppm/°C
3.9Ω	±5mV	0.6ppm/°C

Figure 2. Optional Fine Trim Configuration

ABSOLUTE MAXIMUM RATING

Input Voltage V_{IN} to Ground 40V
Power Dissipation @ +25°C 600mW
Operating Junction Temperature Range . . . . -55°C to +150°C
Lead Temperature
Soldering, 10sec . . . . . 300°C
Thermal Resistance
Junction-to-Ambient . . . . . 150°C/W

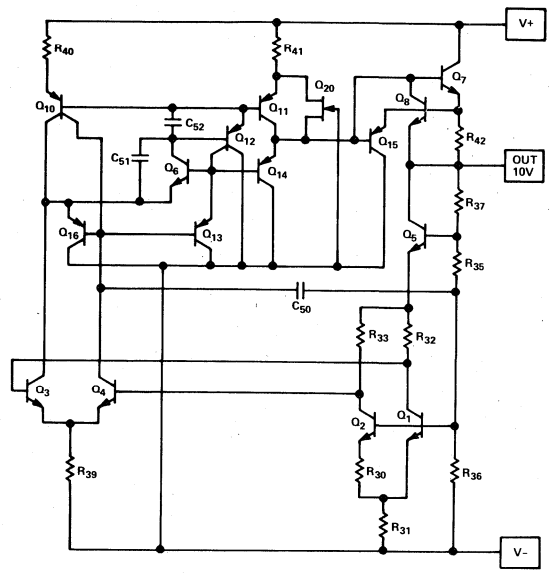
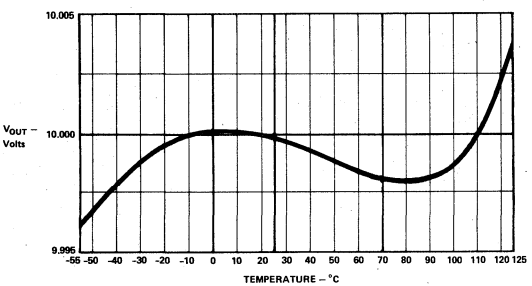


Figure 3. Simplified Schematic

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD581 consistently follows the S-curve shown in Figure 4. Five-point measurement of each device guarantees the error band over the -55°C to +125°C range; three-point measurement guarantees the error band from 0 to +70°C.

The error band which is guaranteed with the AD581 is the maximum deviation from the initial value at +25°C; this error band is of more use to a designer than one which simply guarantees the maximum total change over the entire range (i.e., in the latter definition, all of the changes could occur in the positive direction). Thus, with a given grade of the AD581, the designer can easily determine the maximum total error from initial tolerance plus temperature variation (e.g., for the AD581T, the initial tolerance is ±10mV, the temperature error band is ±15mV, thus the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C).



OUTPUT CURRENT CHARACTERISTICS

The AD581 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device are shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

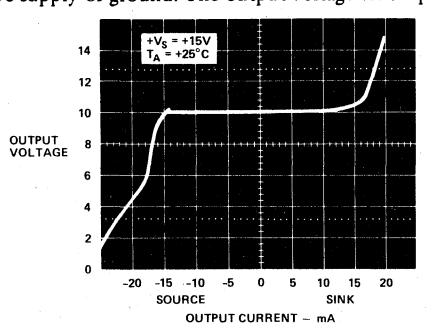


Figure 5. AD581 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD581. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

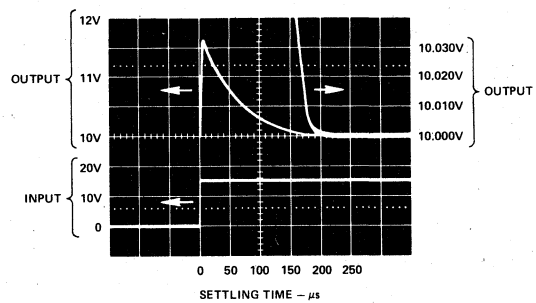


Figure 6. Output Settling Characteristic

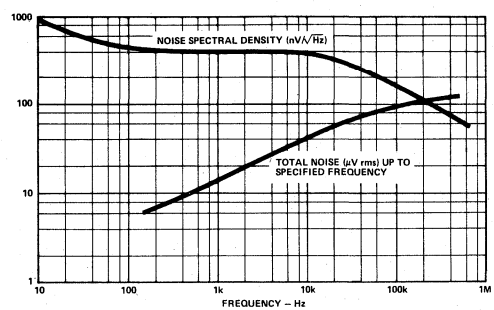


Figure 7. Spectral Noise Density and Total rms Noise vs. Frequency

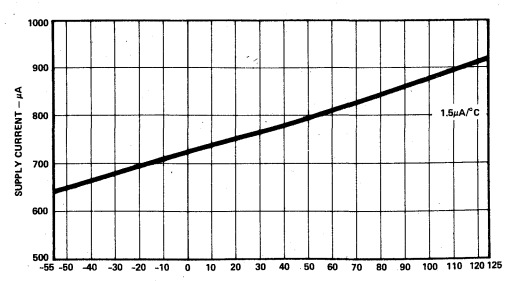


Figure 8. Quiescent Current vs. Temperature

PRECISION HIGH CURRENT SUPPLY

The AD581 can be easily connected with power pnp or power darlington pnp devices to provide much greater output current capability. The circuit shown in Figure 9 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

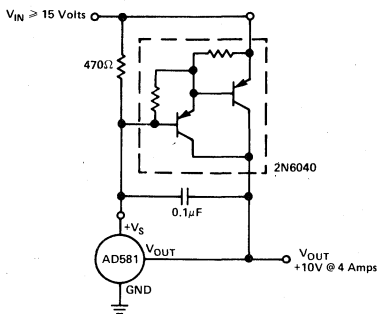


Figure 9. High Current Precision Supply

CONNECTION FOR REDUCED PRIMARY SUPPLY

While line regulation is specified down to 13 volts, the typical AD581 will work as specified down to 12 volts or below. The current sink capability allows even lower supply voltage capability such as operation from 12V ±5% as shown in Figure 10. The 560Ω resistor reduces the current supplied by the AD581 to a manageable level at full 5mA load. Note that other bandgap references, without current sink capability, may be damaged by use in this circuit configuration.

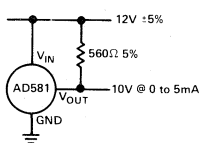


Figure 10. 12-Volt Supply Connection

THE AD581 AS A CURRENT LIMITER

The AD581 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. This approach often results in temperature coefficients of 1%/°C. The AD581 approach is not limited to a defined set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor. Of course, the minimum voltage required to drive the connection is 13 volts. The AD580, which is a 2.5 volt reference, can be used in this type of circuit with compliance voltage down to 4.5 volts.

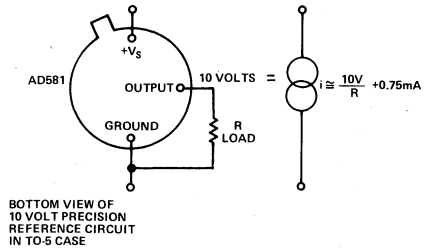


Figure 11. A Two-Component Precision Current Limiter

NEGATIVE 10-VOLT REFERENCE

The AD581 can also be used in a two-terminal "zener" mode to provide a precision -10.00 volt reference. As shown in Figure 12, the V_{IN} and V_{OUT} terminals are connected together to the high supply (in this case, ground). The ground pin is connected through a resistor to the negative supply. The output is now taken from the ground pin instead of V_{OUT}. With 1mA flowing through the AD581 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2 ohms. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD581 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD581 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 10.5 volts. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD581 always remains within its regulating range of 1 to 5mA.

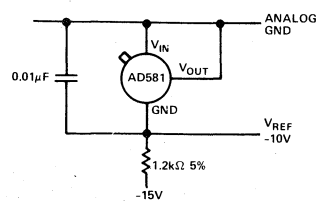


Figure 12. Two-Terminal -10 Volt Reference

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD581 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up, as shown in Figure 13, the +10 volt reference is inverted by the amplifier/DAC configuration to produce a 0 to −10 volt range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. If a 0 to +10 volt full scale range is desired, the AD581 can be connected to the CMOS DAC in its −10 volt "zener" mode, as shown in Figure 12 (the $-10V_{REF}$ output is connected directly to the $V_{REF\ IN}$ of the CMOS DAC). The AD581 will normally be used in the −10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 14. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

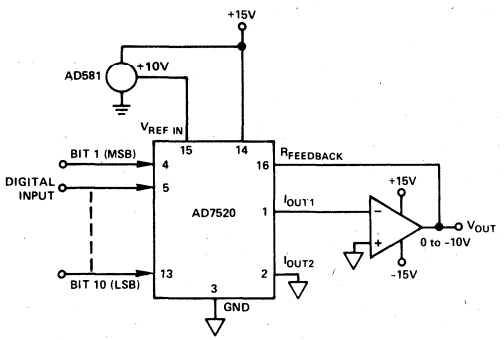


Figure 13. Low Power 10-Bit CMOS DAC Application

PRECISION 12-BIT D/A CONVERTER REFERENCE

The AD562, like most D/A converters, is designed to operate with a +10 volt reference element. In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD581L (at 5ppm/°C) as the 10 volt reference guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C.

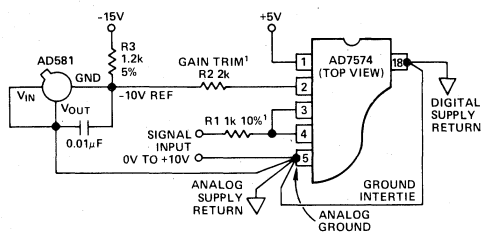


Figure 14. AD581 as Negative 10-Volt Reference for CMOS ADC

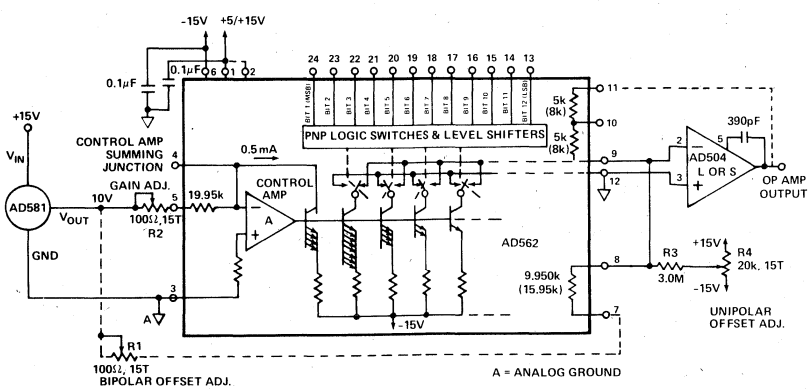


Figure 15. Precision 12-Bit D/A Converter

ANALOG DEVICES

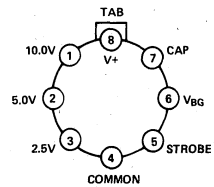
Pin Programmable Precision Voltage Reference

AD584*

FEATURES

- Four Programmable Output Voltages:
  - 10.000V, 7.500V, 5.000V, 2.500V
- Laser-Trimmed to High Accuracies
- No External Components Required
- Trimmed Temperature Coefficient:
  - 5ppm/°C max, 0 to +70°C (AD584LH)
  - 15ppm/°C max, -55°C to +125°C (AD584TH)
- Zero Output Strobe Terminal Provided
- Two Terminal Negative Reference Capability (5V & Above)
- Output Sources or Sinks Current
- Low Quiescent Current: 1.0mA max
- 10mA Current Output Capability

AD584 PIN CONFIGURATION



TO-99
TOP VIEW

PRODUCT DESCRIPTION

The AD584 is an eight-terminal precision voltage reference offering pin-programmable selection of four popular output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other output voltages, above, below or between the four standard outputs, are available by the addition of external resistors. Input voltage may vary between 4.5 and 30 volts.

Laser Wafer Trimming (LWT) is used to adjust the pin-programmable output levels and temperature coefficients, resulting in the most flexible high precision voltage reference available in monolithic form.

In addition to the programmable output voltages, the AD584 offers a unique strobe terminal which permits the device to be turned on or off. When the AD584 is used as a power supply reference, the supply can be switched off with a single, low-power signal. In the "off" state the current drain by the AD584 is reduced to about 100μA. In the "on" state the total supply current is typically 750μA including the output buffer amplifier.

The AD584 is recommended for use as a reference for 8-, 10- or 12-bit D/A converters which require an external precision reference. The device is also ideal for all types of A/D converters of up to 14 bit accuracy, either successive approximation or integrating designs, and in general can offer better performance than that provided by standard self-contained references.

The AD584J, K, and L are specified for operation from 0 to +70°C; the AD584S and T are specified for the -55°C to +125°C range. All grades are packaged in a hermetically-sealed eight-terminal TO-99 metal can.

*Covered by U.S. Patent No. 3,887,863; RE 30,586

PRODUCT HIGHLIGHTS

1. The flexibility of the AD584 eliminates the need to design-in and inventory several different voltage references. Furthermore one AD584 can serve as several references simultaneously when buffered properly.
2. Laser trimming of both initial accuracy and temperature coefficient results in very low errors over temperature without the use of external components. The AD584LH has a maximum deviation from 10.000 volts of ±7.25mV from 0 to +70°C.
3. The AD584 can be operated in a two-terminal "Zener" mode at 5 volts output and above. By connecting the input and the output, the AD584 can be used in this "Zener" configuration as a negative reference.
4. The output of the AD584 is configured to sink or source currents. This means that small reverse currents can be tolerated in circuits using the AD584 without damage to the reference and without disturbing the output voltage (10V, 7.5V and 5V outputs).

SPECIFICATIONS (@ V_{IN} = 15V and 25°C)

Model	AD584J			AD584K			AD584L			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE										
Maximum Error[1] for Nominal										
Outputs of:										
10.000V			±30			±10			±5	mV
7.500V			±20			±8			±4	mV
5.000V			±15			±6			±3	mV
2.500V			±7.5			±3.5			±2.5	mV
OUTPUT VOLTAGE CHANGE										
Maximum Deviation from +25°C										
Value, T_{min} to T_{max}[2]										
10.000, 7.500, 5.000V Outputs			30			15			5	ppm/°C
2.500V Output			30			15			10	ppm/°C
Differential Temperature										
Coefficients Between Outputs		5			3			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200			200		µs
NOISE										
(0.1 to 10Hz)		50			50			50		µV p-p
LONG-TERM STABILITY		25			25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30			30		mA
LINE REGULATION (No Load)										
$15V \leq V_{IN} \leq 30V$			0.002			0.002			0.002	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			0.005			0.005			0.005	%/V
LOAD REGULATION										
$0 \leq I_{OUT} \leq 5mA$, All Outputs		20	50		20	50		20	50	ppm/mA
OUTPUT CURRENT										
$V_{IN} \geq V_{OUT} + 2.5V$										
Source @ +25°C	10			10			10			mA
Source T_{min} to T_{max}	5			5			5			mA
Sink T_{min} to T_{max}	5			5			5			mA
Sink −55°C to +85°C	–			–			–			mA
TEMPERATURE RANGE										
Operating	0		+70	0		+70	0		+70	°C
Storage	−65		+175	−65		+175	−65		+175	°C
PACKAGE (H08A)[3]	AD584JH			AD584KH			AD584LH			

NOTES
[1]At Pin 1.
[2]Calculated as average over the operating temperature range.
[3]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD584S			AD584T			Units
	Min	Typ	Max	Min	Typ	Max	
OUTPUT VOLTAGE TOLERANCE							
Maximum Error[1] for Nominal Outputs of:							
10.000V			±30			±10	mV
7.500V			±20			±8	mV
5.000V			±15			±6	mV
2.500V			±7.5			±3.5	mV
OUTPUT VOLTAGE CHANGE							
Maximum Deviation from +25°C Value, T_{min} to T_{max}[2]							
10.000, 7.500, 5.000V Outputs			30			15	ppm/°C
2.500V Output			30			20	ppm/°C
Differential Temperature Coefficients Between Outputs		5			3		ppm/°C
QUIESCENT CURRENT		0.75	1.0		0.75	1.0	mA
Temperature Variation		1.5			1.5		µA/°C
TURN-ON SETTLING TIME TO 0.1%		200			200		µs
NOISE (0.1 to 10Hz)		50			50		µV p-p
LONG-TERM STABILITY		25			25		ppm/1000 Hrs.
SHORT-CIRCUIT CURRENT		30			30		mA
LINE REGULATION (No Load)							
$15V \leq V_{IN} \leq 30V$			0.002			0.002	%/V
$(V_{OUT} + 2.5V) \leq V_{IN} \leq 15V$			0.005			0.005	%/V
LOAD REGULATION $0 \leq I_{OUT} \leq 5mA$, All Outputs		20	50		20	50	ppm/mA
OUTPUT CURRENT $V_{IN} \geq V_{OUT} + 2.5V$							
Source @ +25°C	10			10			mA
Source T_{min} to T_{max}	5			5			mA
Sink T_{min} to T_{max}	200			200			mA
Sink −55°C to +85°C	5			5			mA
TEMPERATURE RANGE							
Operating	−55		+125	−55		+125	°C
Storage	−65		+175	−65		+175	°C
PACKAGE (H08A)[3]	AD584SH			AD584TH			
ABSOLUTE MAX RATINGS							
Input Voltage V_{IN} to Ground	40V						
Power Dissipation @ +25°C	600mW						
Operating Junction Temp. Range	−55°C to +125°C						
Lead Temperature Soldering, 10sec)	300°C						
Thermal Resistance Junction-to-Ambient	150°C/Watt						

NOTES
[1]At Pin 1
[2]Calculated as average over the operating temperature range.
[3]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Applying the AD584

APPLYING THE AD584

With power applied to pins 8 and 4 and all other pins open the AD584 will produce a buffered nominal 10.0V output between pins 1 and 4 (see Figure 1). The stabilized output voltage may be reduced to 7.5V, 5.0V or 2.5V by connecting the programming pins as follows:

OUTPUT VOLTAGE	PIN PROGRAMMING
7.5V	Join the 2.5V and 5.0V pins (2) and (3).
5.0V	Connect the 5.0V pin (2) to the output pin (1).
2.5V	Connect the 2.5V pin (3) to the output pin (1).

The options shown above are available without the use of any additional components. Multiple outputs using only one AD584, are also possible by simply buffering each voltage programming pin with a unity-gain noninverting op amp.

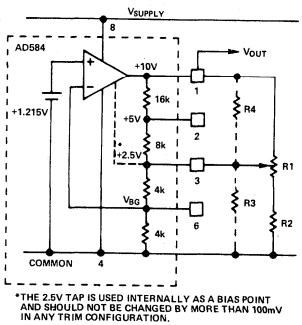


Figure 1. Variable Output Options

The AD584 can also be programmed over a wide range of output voltages, including voltages greater than 10V, by the addition of one or more external resistors. Figure 1 illustrates the general adjustment procedure, with approximate values given for the internal resistors of the AD584. The AD584 may be modeled as an op amp with a noninverting feedback connection, driven by a high stability 1.215 volt bandgap reference (see Figure 3 for schematic).

When the feedback ratio is adjusted with external resistors, the output amplifier can be made to multiply the reference voltage by almost any convenient amount, making popular outputs of 10.24V, 5.12V, 2.56V or 6.3V easy to obtain. The most general adjustment (which gives the greatest range and poorest resolution) uses R1 and R2 alone (see Figure 1). As R1 is adjusted to its upper limit the 2.5V pin 3 will be connected to the output, which will reduce to 2.5V. As R1 is adjusted to its lower limit, the output voltage will rise to a value limited by R2. For example, if R2 is about 6kΩ, the upper limit of the output range will be about 20V even for large values of R1. R2 should not be omitted; its value should be chosen to limit the output to a value which can be tolerated by the load circuits. If R2 is zero, adjusting R1 to its lower limit will result in a loss of control over the output voltage. If precision voltages are required to be set at levels other than the standard outputs, the 20% absolute tolerance in the internal resistor ladder must be accounted for.

Alternatively, the output voltage can be raised by loading the 2.5V tap with R3 alone. The output voltage can be lowered by connecting R4 alone. Either of these resistors can be a fixed resistor selected by test or an adjustable resistor. In all cases the resistors should have a low temperature coefficient to match the AD584 internal resistors, which have a negative T.C. less than 60ppm/°C. If both R3 and R4 are used, these resistors should have matched temperature coefficients.

When only small adjustments or trims are required, the circuit of Figure 2 offers better resolution over a limited trim range. The circuit can be programmed to 5.0V, 7.5V or 10V and adjusted by means of R1 over a range of about ±200mV. To trim the 2.5V output option, R2 (Figure 2) can be reconnected to the bandgap reference (pin 6). In this configuration, the adjustment should be limited to ±100mV in order to avoid affecting the performance of the AD584.

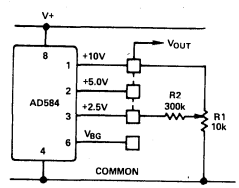


Figure 2. Output Trimming

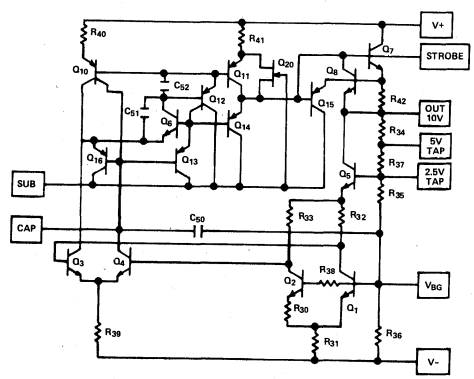


Figure 3. Schematic Diagram

PERFORMANCE OVER TEMPERATURE

Each AD584 is tested at five temperatures over the -55°C to +125°C range to ensure that each device falls within the Maximum Error Band (see Figure 4) specified for a particular grade (i.e., S and T grades); three-point measurement guarantees performance within the error band from 0 to +70°C (i.e., J, K, or L grades). The error band guaranteed for the AD584 is the maximum deviation from the initial value at +25°C. Thus, given the grade of the AD584, the designer can easily determine the maximum total error from initial tolerance plus temperature variation. For example, for the AD584T, the initial tolerance is ±10mV and the error band is ±15mV. Hence, the unit is guaranteed to be 10.000 volts ±25mV from -55°C to +125°C.

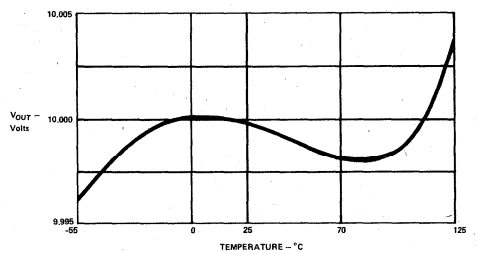


Figure 4. Typical Temperature Characteristic

OUTPUT CURRENT CHARACTERISTICS

The AD584 has the capability to either source or sink current and provide good load regulation in either direction, although it has better characteristics in the source mode (positive current into the load). The circuit is protected for shorts to either positive supply or ground. The output voltage vs. output current characteristics of the device is shown in Figure 5. Source current is displayed as negative current in the figure; sink current is positive. Note that the short circuit current (i.e., zero volts output) is about 28mA; when shorted to +15 volts, the sink current goes to about 20mA.

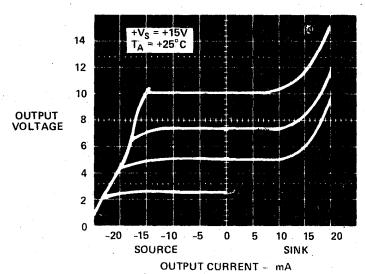


Figure 5. AD584 Output Voltage vs. Sink and Source Current

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 6 displays the turn-on characteristic of the AD584. Figure 6a is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 180μs, and there is no long thermal tail appearing after the point.

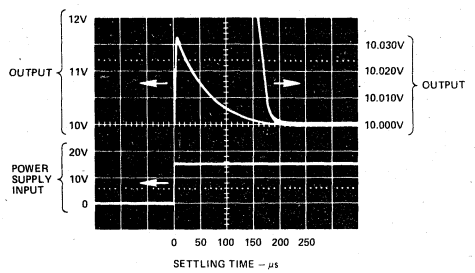


Figure 6. Output Settling Characteristic

NOISE FILTERING

The bandwidth of the output amplifier in the AD584 can be reduced to filter the output noise. A capacitor ranging between 0.01μF and 0.1μF connected between the Cap and V_{BG} terminals will further reduce the wideband and feedthrough noise in the output of the AD584, as shown in Figure 8.

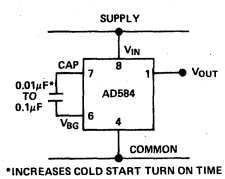


Figure 7. Additional Noise Filtering with an External Capacitor

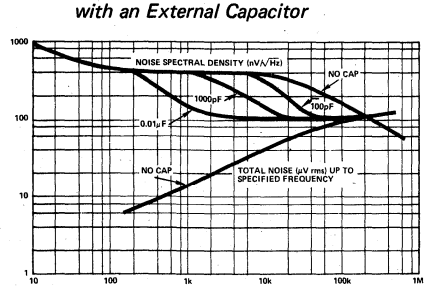


Figure 8. Spectral Noise Density and Total rms Noise vs. Frequency

Applications of the AD584

USING THE STROBE TERMINAL

The AD584 has a strobe input which can be used to zero the output. This unique feature permits a variety of new applications in signal and power conditioning circuits.

Figure 9 illustrates the strobe connection. A simple NPN switch can be used to translate a TTL logic signal into a strobe of the output. The AD584 operates normally when there is no current drawn from pin 5. Bringing this terminal low, to less than 200mV, will allow the output voltage to go to zero. In this mode the AD584 should not be required to source or sink current (unless a 0.7V residual output is permissible). If the AD584 is required to sink a transient current while strobed off, the strobe terminal input current should be limited by a 100Ω resistor as shown in Figure 9.

The strobe terminal will tolerate up to 5μA leakage and its driver should be capable of sinking 500μA continuous. A low leakage open collector gate can be used to drive the strobe terminal directly, provided the gate can withstand the AD584 output voltage plus one volt.

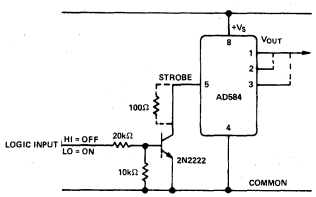


Figure 9. Use of the Strobe Terminal

PRECISION HIGH CURRENT SUPPLY

The AD584 can be easily connected to a power PNP or power Darlington PNP device to provide much greater output current capability. The circuit shown in Figure 10 delivers a precision 10 volt output with up to 4 amperes supplied to the load. The 0.1μF capacitor is required only if the load has a significant capacitive component. If the load is purely resistive, improved high frequency supply rejection results from removing the capacitor.

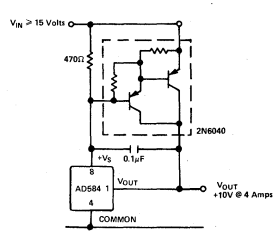


Figure 10. High Current Precision Supply

The AD584 can also use an NPN or Darlington NPN transistor to boost its output current. Simply connect the 10V output terminal of the AD584 to the base of the NPN booster and take the output from the booster emitter as shown in Figure 11. The 5.0V or 2.5V pin must connect to the actual output in this configuration. Variable or adjustable outputs (as shown in Figures 1 and 2) may be combined with +5.0V connection to obtain outputs above +5.0V.

THE AD584 AS A CURRENT LIMITER

The AD584 represents an alternative to current limiter diodes which require factory selection to achieve a desired current. Use of current limiting diodes often results in temperature coefficients of 1%/°C. Use of the AD584 in this mode is not limited to a set current limit; it can be programmed from 0.75 to 5mA with the insertion of a single external resistor (see Figure 12). Of course, the minimum voltage required to drive the connection is 5 volts.

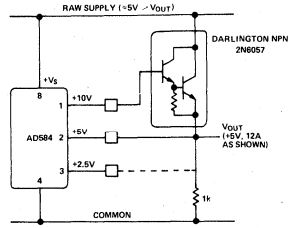


Figure 11. NPN Output Current Booster

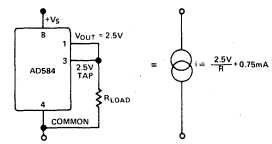


Figure 12. A Two-Component Precision Current Limiter

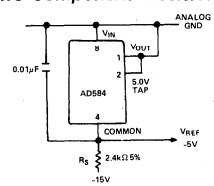


Figure 13. Two-Terminal -5 Volt Reference

NEGATIVE REFERENCE VOLTAGES FROM AN AD584

The AD584 can also be used in a two-terminal "zener" mode to provide a precision -10, -7.5 or -5.0 volt reference. As shown in Figure 13, the V_{IN} and V_{OUT} terminals are connected together to the positive supply (in this case, ground). The AD584 common pin is connected through a resistor to the negative supply. The output is now taken from the common pin instead of V_{OUT}. With 1mA flowing through the AD584 in this mode, a typical unit will show a 2mV increase in output level over that produced in the three-terminal mode. Note also that the effective output impedance in this connection increases from 0.2Ω typical to 2Ω. It is essential to arrange the output load and the supply resistor, R_S, so that the net current through the AD584 is always between 1 and 5mA. The temperature characteristics and long-term stability of the device will be essentially the same as that of a unit used in the standard three-terminal mode. The operating temperature range is limited to -55°C to +85°C.

The AD584 can also be used in a two-terminal mode to develop a positive reference. V_{IN} and V_{OUT} are tied together and to the positive supply through an appropriate supply resistor. The performance characteristics will be similar to those of the negative two-terminal connection. The only advantage of this connection over the standard three-terminal connection is that a lower primary supply can be used, as low as 0.5 volts above the desired output voltage. This type of operation will require considerable attention to load and primary supply regulation to be sure the AD584 always remains within its regulating range of 1 to 5mA.

10 VOLT REFERENCE WITH MULTIPLYING CMOS D/A OR A/D CONVERTERS

The AD584 is ideal for application with the entire AD7520 series of 10- and 12-bit multiplying CMOS D/A converters, especially for low power applications. It is equally suitable for the AD7574 8-bit A/D converter. In the standard hook-up as shown in Figure 14, the standard output voltages are inverted by the amplifier/DAC configuration to produce converted voltage ranges. For example, a +10V reference produces a 0 to -10V range. If an AD308 amplifier is used, total quiescent supply current will typically be 2mA. The AD584 will normally be used in the -10 volt mode with the AD7574 to give a 0 to +10 volt ADC range. This is shown in Figure 16. Bipolar output applications and other operating details can be found in the data sheets for the CMOS products.

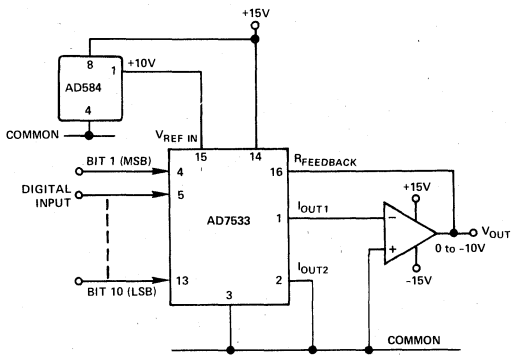
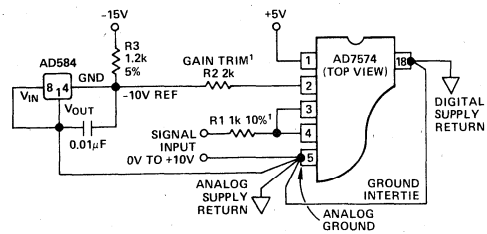


Figure 14. Low Power 10-Bit CMOS DAC Application

PRECISION D/A CONVERTER REFERENCE

The AD562, like many D/A converters, is designed to operate with a +10 volt reference element (Figure 15). In the AD562, this 10 volt reference voltage is converted into a reference current of approximately 0.5mA via the internal 19.95kΩ resistor (in series with the external 100Ω trimmer). The gain temperature coefficient of the AD562 is primarily governed by the temperature tracking of the 19.95kΩ resistor and the 5k/10k span resistors; this gain T.C. is guaranteed to 3ppm/°C. Thus, using the AD584L (at 5ppm/°C) as the 10 volt reference



NOTE 1: R1 AND R2 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED

Figure 16. AD584 as Negative 10 Volt Reference for CMOS ADC

guarantees a maximum full scale temperature coefficient of 8ppm/°C over the commercial range. The 10 volt reference also supplies the normal 1mA bipolar offset current through the 9.95k bipolar offset resistor. The bipolar offset T.C. thus depends only on the T.C. matching of the bipolar offset resistor to the input reference resistor and is guaranteed to 3ppm/°C. Figure 17 demonstrates the flexibility of the AD584 applied to another popular D/A configuration.

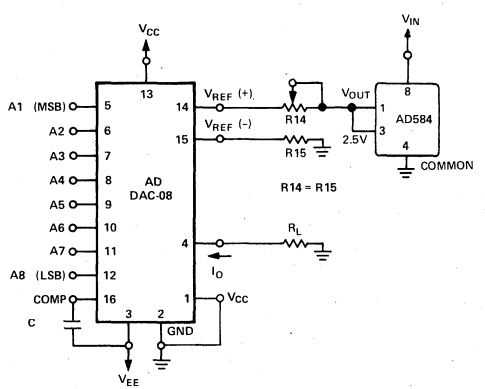


Figure 17. Current Output 8-Bit D/A

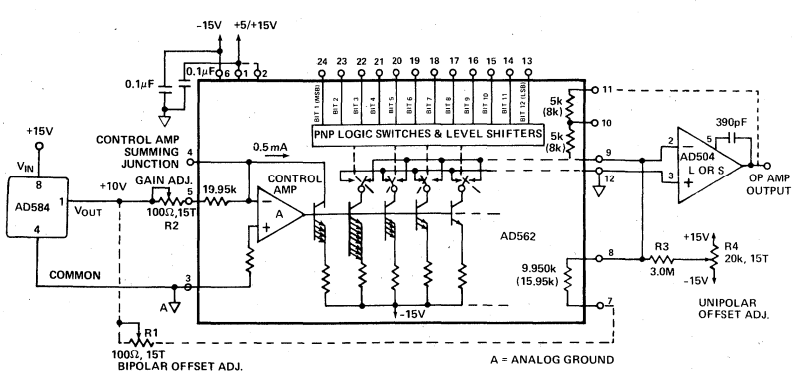


Figure 15. Precision 12-Bit D/A Converter

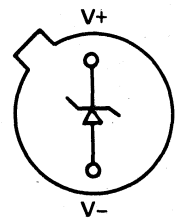
Two-Terminal IC 1.2 Volt Reference

AD589

FEATURES

Superior Replacement for Other 1.2V References
Wide Operating Range: 50μA to 5mA
Low Power: 60μW Total P_D at 50μA
Low Temperature Coefficient:
10ppm/°C max, 0 to +70°C (AD589M)
25ppm/°C max, -55°C to +125°C (AD589U)
Two Terminal "Zener" Operation
Low Output Impedance: 0.6Ω
No Frequency Compensation Required
Low Cost

AD589 FUNCTIONAL BLOCK DIAGRAM



BOTTOM VIEW

7

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589 is available in seven versions. The AD589J, K, L and M grades are specified for 0 to +70°C operation, while the S, T and U grades are rated for the full -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD589 is a two-terminal device which delivers a a constant reference voltage for a wide range of input current.
2. Output impedance of 0.6Ω and temperature coefficients as low as 10ppm/°C insure stable output voltage over a wide range of operating conditions.
3. The AD589 can be operated as a positive or negative reference. "Floating" operation is also possible.
4. The AD589 will operate with total current as low as 50μA (60μW total power dissipation), ideal for battery powered instrument applications.
5. The AD589 is an exact replacement for other 1.2V references, offering superior temperature performance and reduced sensitivity to capacitive loading.

SPECIFICATIONS (typical @ I_{IN} = 500μA and T_A = 25°C unless otherwise noted)

Model	AD589JH	AD589KH	AD589LH	AD589MH	AD589SH	AD589TH	AD589UH
ABSOLUTE MAXIMUM RATINGS							
Current	10mA	*	*	*	*	*	*
Reverse Current	10mA	*	*	*	*	*	*
Power Dissipation[1]	125mW	*	*	*	*	*	*
Storage Temperature Range	−65°C to +175°C	*	*	*	*	*	*
Operating Junction Temperature Range	−55°C to +150°C	*	*	*	*	*	*
Lead Temperature (Soldering, 10sec)	300°C	*	*	*	*	*	*
Operating Temperature Range	0 to +70°C	*	*	*	−55°C to +125°C	**	**
OUTPUT VOLTAGE, T_a = 25°C	1.200V min	*	*	*	*	*	*
	1.235V typ	*	*	*	*	*	*
	1.250V max	*	*	*	*	*	*
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA − 5mA)	5mV max	*	*	*	*	*	*
DYNAMIC OUTPUT IMPEDANCE	0.6Ω typ	*	*	*	*	*	*
	2Ω max	*	*	*	*	*	*
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5μV	*	*	*	*	*	*
TEMPERATURE COEFFICIENT[2] − ppm/°C	100 max	50 max	25 max	10 max	100 max	50 max	25 max
TURN-ON SETTLING TIME TO 0.1%	25μs	*	*	*	*	*	*
OPERATING CURRENT[3]	50μA min	*	*	*	*	*	*
	5mA max	*	*	*	*	*	*
PACKAGE STYLE:[4] H2A	H	*	*	*	*	*	*

NOTES
[1] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and $\theta_{JA} = 400°C/W$.
[2] See following page for explanation of temperature coefficient measurement method.
[3] Optimum performance is obtained at currents below 500μA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.
[4] See Section 19 for package outline information.

*Specifications same as AD589J.
**Specifications same as AD589S.
Specifications subject to change without notice.

VOLTAGE VARIATION vs. TEMPERATURE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references have been characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of nonlinearities in temperature characteristics, which originated in standard zener references (such as "S" type characteristics) most manufacturers have begun to use a maximum limit error band approach to specify devices. This technique involves measurement of the output at 3, 5 or more different temperatures to guarantee that the output voltage will fall within the given error band. The temperature characteristic of the AD589 consistently follows the curve shown in Figure 1. Three-point measurement guarantees the error band over the specified temperature range. The temperature coefficients specified on page 2 represent the slopes of the diagonals of the error band from +25°C to T_{min} and +25°C to T_{max}.

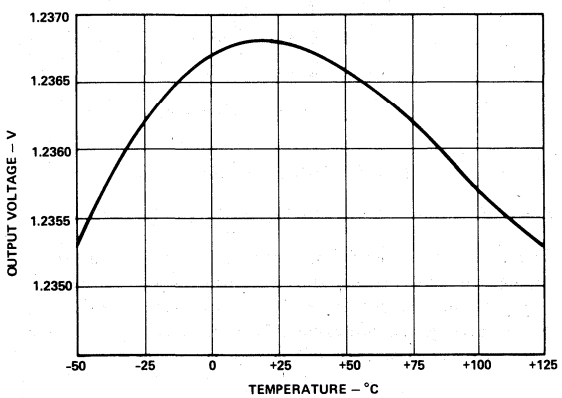


Figure 1. Typical AD589 Temperature Characteristics

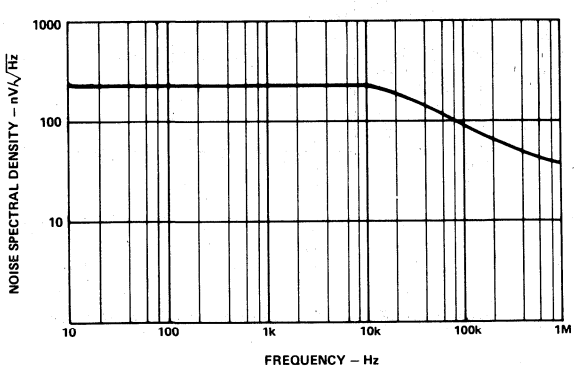


Figure 2. Noise Spectral Density

DYNAMIC PERFORMANCE

Many low power instrument manufacturers are becoming increasingly concerned with the turn-on characteristics of the components being used in their systems. Fast turn-on components often enable the end user to keep power off when not needed, and yet respond quickly when the power is turned on for operation. Figure 3 displays the turn-on characteristic of the AD589. This characteristic is generated from cold-start operation and represents the true turn-on waveform after an extended period with the supplies off. The figure shows both the coarse and fine transient characteristics of the device; the total settling time to within ±1 millivolt is about 25μs, and there is no long thermal tail appearing after that point.

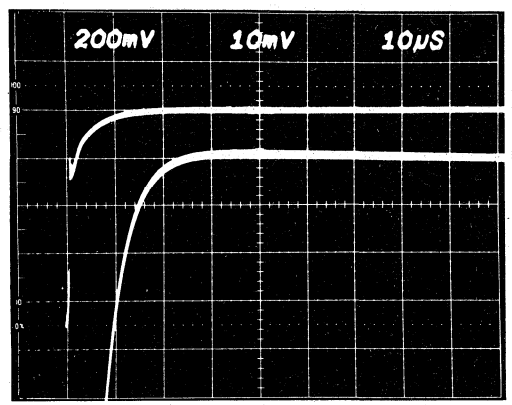


Figure 3. Output Settling Characteristics

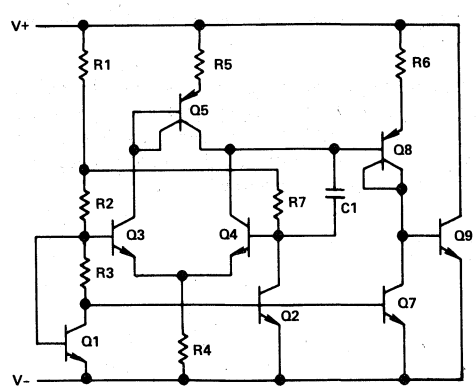


Figure 4. Schematic Diagram

APPLICATION INFORMATION

The AD589 functions as a two-terminal shunt-type regulator. It provides a constant 1.23V output for a wide range of input current from 50μA to 5mA. Figure 5 shows the simplest configuration for an output voltage of 1.2V or less. Note that no frequency compensation is required. If additional filtering is desired for ultra low noise applications, minimum recommended capacitance is 1000pF.

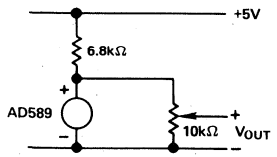


Figure 5. Basic Configuration for 1.2V or Less

The AD589 can also be used as a building block to generate other values of reference voltage. Figure 6 shows a circuit which produces a buffered 10V output. Total supply current for this circuit is approximately 2mA.

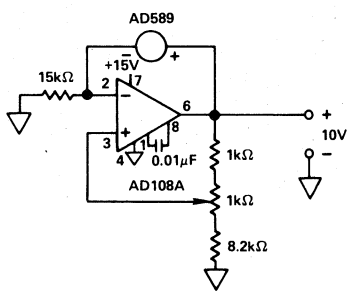
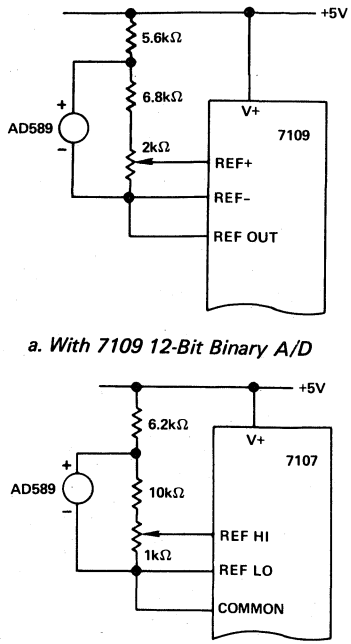


Figure 6. Single-Supply Buffered 10V Reference

The low power operation of the AD589 makes it ideal for use in battery operated portable equipment. It is especially useful as a reference for CMOS analog-to-digital converters. Figure 7 shows the AD589 used in conjunction with two popular integrating type CMOS A/D converters.



a. With 7109 12-Bit Binary A/D

b. With 7107 Panel Meter A/D

Figure 7. AD589 Used as Reference for CMOS A/D Converters

The AD589 also is useful as a reference for CMOS multiplying DACs such as the AD7533. These DACs require a negative reference voltage in order to provide a positive output range. Figure 8 shows the AD589 used to supply an equivalent -1.0V reference to an AD7533.

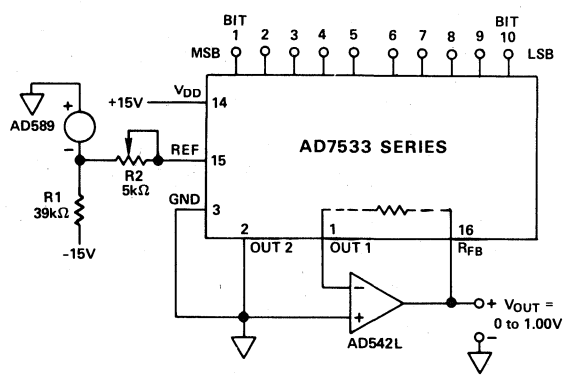


Figure 8. AD589 as Reference for 10-Bit CMOS DAC

ANALOG DEVICES

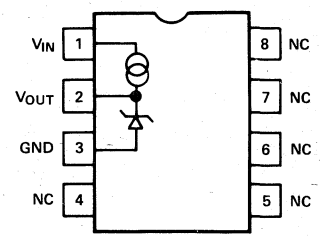
Low Cost, Precision 2.5 Volt IC Reference

AD1403/AD1403A*

FEATURES

Improved, Lower Cost, Replacements for Standard 1403, 1403A
3-Terminal Device: Voltage In/Voltage Out
Laser Trimmed to High Accuracy: 2.500V ±10mV (AD1403A)
Excellent Temperature Stability: 25ppm/°C (AD1403A)
Low Quiescent Current: 1.5mA max
10mA Current Output Capability
Convenient MINI-DIP Package

AD1403/AD1403A
FUNCTIONAL BLOCK DIAGRAM



8-PIN MINI-DIP

7

PRODUCT DESCRIPTION

The AD1403 and AD1403A are improved three-terminal, low cost, temperature compensated, bandgap voltage references that provide a fixed 2.5V output voltage for inputs between 4.5V and 40V. A unique combination of advanced circuit design and laser-wafer-trimmed thin-film resistors provides the AD1403/AD1403A with an initial tolerance of ±10mV and a temperature stability of better than 25ppm/°C. In addition, the low quiescent current drain of 1.5mA (max) offers a clear advantage over classical zener techniques.

The AD1403 or AD1403A is recommended as a stable reference for all 8-, 10- and 12-bit D-to-A converters that require an external reference. In addition, the wide input range of the AD1403/AD1403A allows operation with 5 volt logic supplies, making these devices ideal for digital panel meter applications and when only a single logic supply is available.

The AD1403 and AD1403A are specified for operation over the 0 to +70°C temperature range. The AD580 series of 2.5 volt precision IC references is recommended for applications where operation over the −55°C to +125°C range is required.

*Covered by Patent Numbers: 3,887,863; RE30,586.

PRODUCT HIGHLIGHTS

1. The AD1403A offers improved initial tolerance over the industry-standard 1403A: ±10mV versus ±25mV at a lower cost.
2. The three-terminal voltage in/voltage out operation of the AD1403/AD1403A provides a regulated output voltage without any external components.
3. The AD1403/AD1403A provides a stable 2.5V output voltage for input voltages between 4.5V and 40V making these devices ideal for systems that contain a single logic supply.
4. Thin film resistor technology and tightly controlled bipolar processing provide the AD1403A with temperature stabilities of 25ppm/°C.
5. The low 1.5mA maximum quiescent current drain of the AD1403 and AD1403A makes them ideal for CMOS and other low power applications.

SPECIFICATIONS (V_{IN} = 15V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0mA)	V_O				
AD1403		2.475	2.500	2.525	V
AD1403A		2.490	2.500	2.510	
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
AD1403		–	10	40	
AD1403A		–	10	25	
Output Voltage Change, 0 to +70°C	ΔV_O				mV
AD1403		–	–	7.0	
AD1403A		–	–	4.4	
Line Regulation	Reg_{in}				mV
(15V≤V_{IN}≤40V)		–	1.2	4.5	
(4.5≤V_{IN}≤15V)		–	0.6	3.0	
Load Regulation ($0mA<I_O<10mA$)	Reg_{load}	–	–	10	mV
Quiescent Current (I_O = 0mA)	I_I	–	1.2	1.5	mA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	40	V
Storage Temperature	T_{STG}	-25 to 100	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C

Specifications subject to change without notice.

ORDERING INFORMATION

Device	Initial Tolerance	Package[1]
AD1403N	±25mV	N8A
AD1403AN	±10mV	N8A

NOTE
[1] See Section 19 for package outline information.

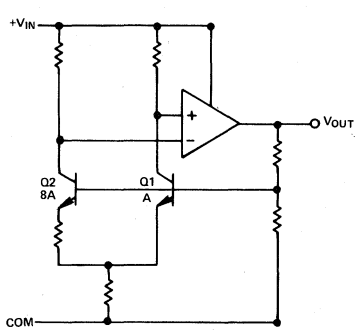


Figure 1. AD1043/AD1403A Functional Diagram

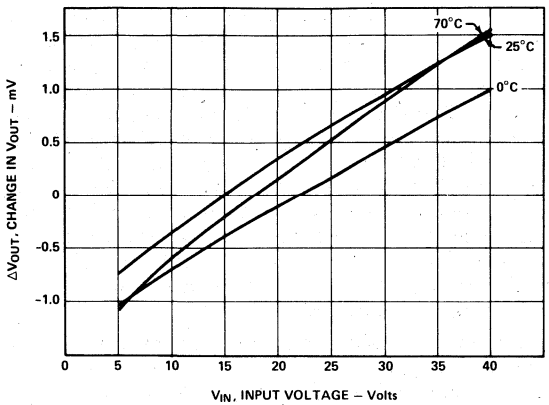


Figure 2. Typical Change in V_{OUT} vs. V_{IN} (Normalized to V_{OUT} @ V_{IN} = 15V @ T_C = 25°C)

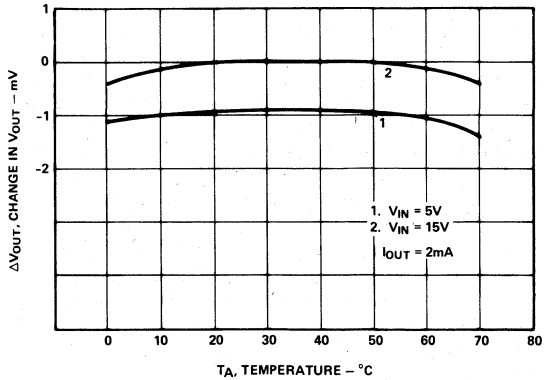


Figure 5. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V)

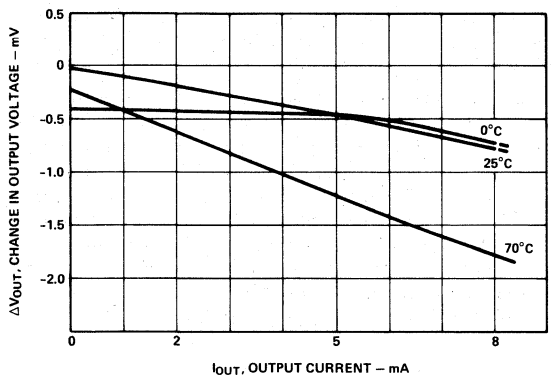


Figure 3. Change in Output Voltage vs. Load Current (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

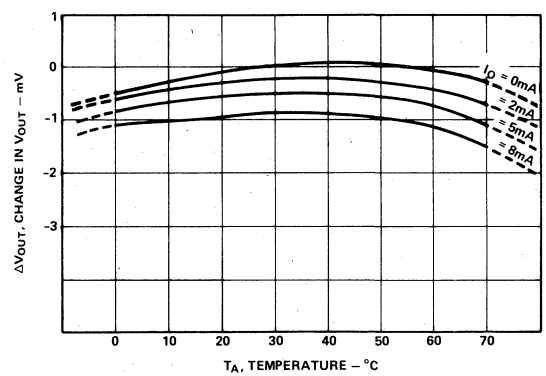


Figure 6. Change in V_{OUT} vs. Temperature (Normalized to V_{OUT} @ V_{IN} = 15V, I_{OUT} = 0mA)

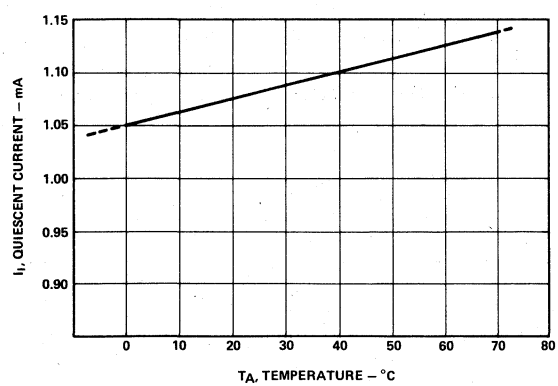


Figure 4. Quiescent Current vs. Temperature (V_{IN} = 15V, I_{OUT} = 0mA)

Applying the AD1403/AD1403A

VOLTAGE VARIATION VS. TEMPERATURE AND LINE

Some confusion exists in the area of defining and specifying reference voltage error over temperature. Historically, references are characterized using a maximum deviation per degree Centigrade; i.e., 10ppm/°C. However, because of the inconsistent nonlinearities in zener references (butterfly or "S" type characteristics), most manufacturers use a maximum limit error band approach to characterize their references. This technique measures the output voltage at 3 to 5 different temperatures and guarantees that the output voltage deviation will fall within the guaranteed error band at these discrete temperatures. This approach, of course, makes no mention or guarantee of performance at any other temperature within the operating temperature range of the device.

The consisten Voltage vs. Temperature performance of a typical AD1403 is shown in Figure 5. Note that the characteristic is quasi-parabolic, not the possible "S" type characteristics of classical zener references. This parabolic characteristic permits a maximum output deviation specification over the device's full operating temperature range, rather than just at 3 to 5 discrete temperatures.

The AD1403 exhibits a worst-case shift of 7.5mV over the entire range of operating input voltage, 4.5 volts to 40 volts. Typically, the shift is less than 1mV as shown in Figure 2.

THE AD1403A AS A LOW POWER, LOW VOLTAGE PRECISION REFERENCE FOR DATA CONVERTERS

The AD1403A has a number of features that make it ideally suited for use with A/D and D/A data converters used in complex microprocessor-based systems. The calibrated 2.500 volt output minimizes user trim requirements and allows operation from a single low voltage supply. Low power consumption (1.5mA quiescent current) is commensurate with that of CMOS-type devices, while the low cost and small package complements the decreasing cost and size of the latest converters.

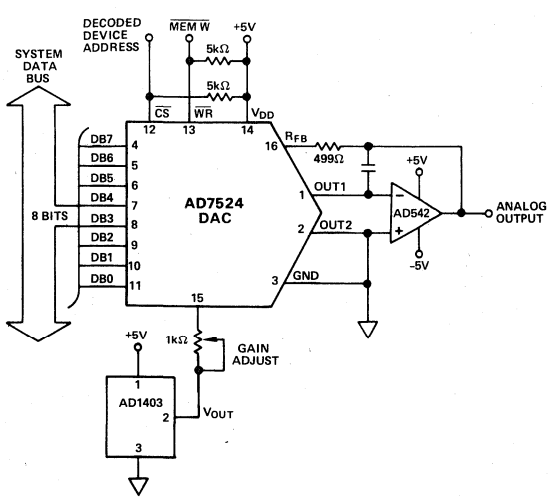


Figure 7. Low Power, Low Voltage Reference for the AD7524 Microprocessor-Compatible 8-Bit DAC

Figure 7 shows the AD1403A used as a reference for the AD7524 low-cost 8-bit CMOS DAC with complete microprocessor interface. The AD1403A and the AD7524 are specified to operate from a single 5 volt supply; this eliminates the need to provide a +15 volt power supply for the sole purpose of operating a reference. The AD7524 includes an 8-bit data register, and address decoding logic; it may thus be interfaced directly to an 8- or 16-bit data bus. Only 300μA of quiescent current from the single +5 volt supply is required to operate the AD7524 which is packaged in a small 16 pin DIP. The AD542 output amplifier is also low power, requiring only 1.5mA quiescent current. Its laser-trimmed offset voltage preserves the ±1/2LSB linearity of the AD7524KN without user trims and it typically settles to ±1/2LSB in less than 5 microseconds. It will provide the 0 volt to -2.5 volt output swing from ±5 volt supplies.

THE AD1403 AS A PRECISION PROGRAMMABLE CURRENT SOURCE

The AD1403 is an excellent building block for precision current sources. Its wide range of operating voltages, 4.5V to 40V, along with excellent line regulation over that range (7.5mV) result in high insensitivity to varying load impedances. The low quiescent current (I_I) of 1.5mA (max) and the maximum specified maximum load current of 10mA allows the user to program current to any value between 1.5mA and 10mA.

Figure 8a shows the AD1403 connected as a current source. Total current is equal to the quiescent current plus the load current. Most of the temperature coefficient comes from the quiescent current term I_I, which has a typical TC of 0.13%/°C (1300ppm/°C). The load voltage (and hence current) TC is much lower at ±40ppm/°C max (AD1403). Therefore, the overall temperature coefficient decreases rapidly as the load current is increased. Figure 8b shows the typical temperature coefficient for currents between 1.5mA and 10mA. Use of an AD1403A will improve the TC appreciably.

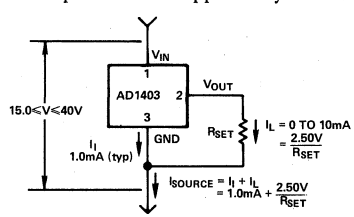


Figure 8a. The AD1403 as a Precision Programmable Current Source.

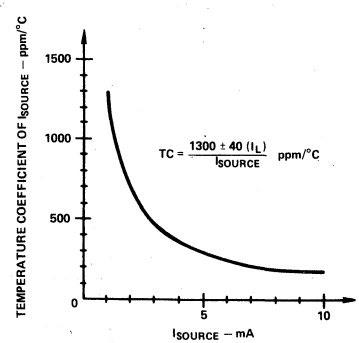


Figure 8b. Typical Temperature Coefficient of Current Source

ANALOG DEVICES

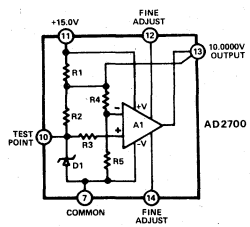
±10 Volt Precision Reference Series

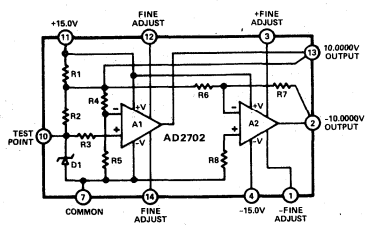
AD2700, AD2701, AD2702

FEATURES

Very High Accuracy: 10.000 Volts ±2.5mV (L and U)
Low Temperature Coefficient: 3ppm/°C
Performance Guaranteed -55°C to +125°C
10mA Output Current Capability
Low Noise
Short Circuit Protected

AD2700 SERIES FUNCTIONAL BLOCK DIAGRAMS





14-PIN DIP

PRODUCT DESCRIPTION

The AD2700 family of precision 10 volt references offer the user excellent accuracy and stability at a moderate price by combining the recognized advantages of thin film technology and active laser trimming. The low temperature drift (3ppm/°C) achieved with these technologies can be matched only by the use of ovens, chip heaters for temperature regulation, or with hand selected components and manual trimming. In addition, temperature-regulated devices are guaranteed only up to +85°C operation, whereas the U- and S-grade devices in the AD2700 family are guaranteed to +125°C.

The AD2700 is a +10 volt reference which is designed to interface with high accuracy bipolar D/A converters of 10 and 12 bit resolution. The 10mA output drive capability also makes the AD2700 ideal for use as a general positive system reference.

The AD2701 is a negative 10 volt reference especially designed to interface with CMOS D/A and A/D converters, as shown in the applications. For systems requiring a dual tracking reference, the AD2702 offers both positive and negative precision 10 volt outputs in a single package. Both are often used with 52XX Series 12-bit A/D converters which require -10V external references for high accuracy over wide temperature ranges.

All three devices are offered in "J" and "L" grades for operation from -25°C to +85°C and "S" and "U" grades for the -55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature performance results in very high accuracy over the temperature range without external components. The AD2700/01/02 LD grades have a maximum output voltage error at 25°C of ±2.5mV with no external adjustments.
2. The performance of the AD2700 series is achieved by a well-characterized design and precise control over the manufacturing process.
3. The AD2700 series is well suited for a broad range of applications requiring an accurate, stable reference source such as high resolution data converters (12 or 14 bits), test and measurement systems and calibration standards.

Model	Output
AD2700	+10.000V
AD2701	-10.000V
AD2702	±10.000V

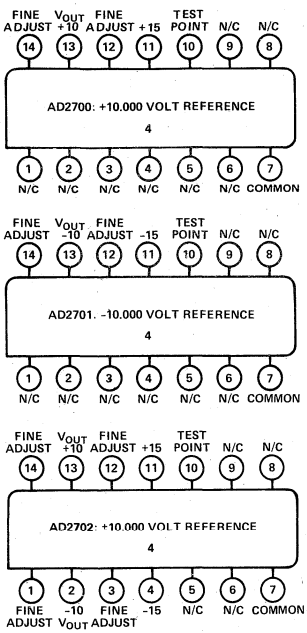
SPECIFICATIONS (maximum or minimum @ E_{IN} ±15V @ +25°C, R_L = 2kΩ unless otherwise noted)

MODEL	JD	LD	SD	UD
ABSOLUTE MAX RATINGS				
Input Voltage (for applicable supply)	±20V	*	*	*
Power Dissipation @ +25°C – AD2700, 01	300mW	*	*	*
– AD2702	450mW	*	*	*
Operating Temperature Range	-25°C to +85°C	*	-55°C to +125°C	***
Storage Temperature Range	-65°C to +150°C	*	*	*
Lead Temperature (soldering, 10s)	+300°C	*	*	*
Short Circuit Protection (to GND)	Continuous	*	*	*
OUTPUT VOLTAGE ERROR @ +25°C				
AD2700 10.000V	±0.005V	±0.0025V	*	**
AD2701 -10.000V	±0.005V	±0.0025V	*	**
AD2702 ±10.000V	±0.005V	±0.0025V	*	**
OUTPUT CURRENT[1] – @ +25°C	±10mA	*	*	*
(V_{IN} = ±13 to ±18V) over op. temp. range	±5mA	+5mA, -2mA	**	**
OUTPUT VOLTAGE ERROR – AD2700,01	10ppm/°C	3ppm/°C	**	**
(T_{min} to T_{max})[2]	±11.0mV	±4.3mV	±8mV	±5.5mV
AD2702	10ppm/°C	5ppm/°C	**	3ppm/°C
	±11.0mV	±5.5mV	±10.0mV	±5.5mV
LINE REGULATION				
V_{IN} = ±13.5 to ±16.5V	300μV/V	*	*	*
LOAD REGULATION				
0 to ±10mA	50μV/mA	*	*	*
OUTPUT RESISTANCE	0.05Ω	*	*	*
INPUT VOLTAGE, OPERATING	±13V to ±18V	*	*	*
QUIESCENT CURRENT – AD2700, 01	±14mA	*	*	*
– AD2702	+17mA, -4mA	*	*	*
NOISE				
(0.1 to 10Hz)	50μV p-p typ	*	*	*
LONG TERM STABILITY (@ +55°C)	100ppm/1000 Hrs. (typ)	*	*	*
OFFSET ADJUST RANGE				
(See Diagrams)	±20mV (min)	*	*	*
OFFSET ADJUST TEMP DRIFT EFFECT	±4μV/°C per mV of Adjust (typ)	*	*	*
PACKAGE[3,4]	HY14B	HY14B	HY14D	HY14D

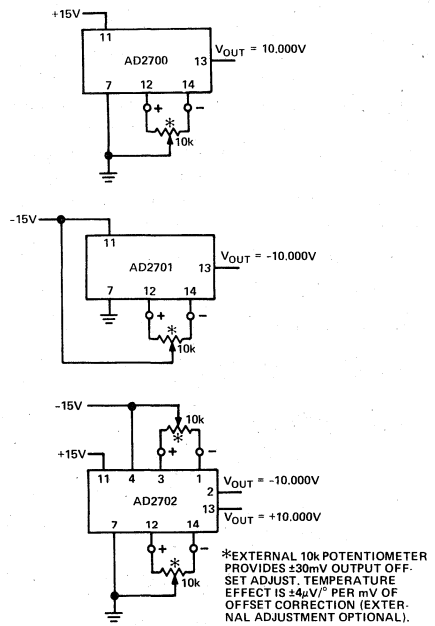
NOTES
*Same as "JD" grade performance.
**Same as "LD" grade performance.
***Same as "SD" grade performance.

[1] Specified with resistive load to common.
[2] Output voltage error as a function of temperature is determined using the box method. Each unit is tested at T_{min}, T_{max} and +25°C. At each temperature V_{OUT} must fall within the rectangular area bounded by the minimum and maximum temperature and whose maximum V_{OUT} value is equal to V_{OUT} nominal plus or minus the maximum +25°C error plus the maximum drift error from +25°C. The box limits are noted below the drift values used to calculate the box.
[3] Analog Devices reserves the right to ship metal packages in lieu of the standard ceramic packages for J and L grade parts.
[4] See Section 19 for package outline information.

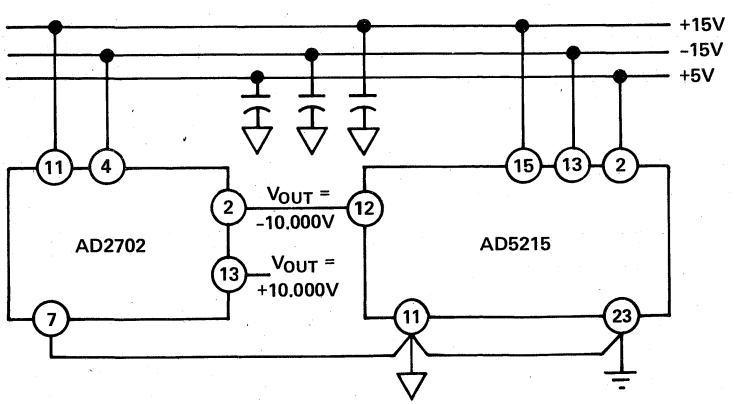
Specifications subject to change without notice.



Pin Designations



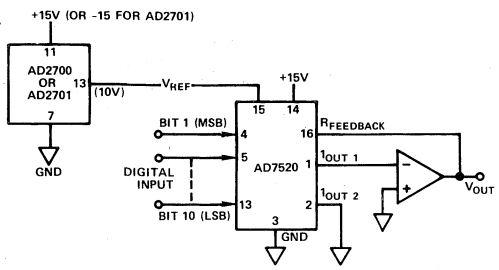
Fine Trim Connections



Using AD2702 Reference with the Fast, High Accuracy AD5215 – 12-Bit ADC

USING AD2700 REFERENCE WITH THE AD7520 AND AN IC AMPLIFIER TO BUILD A DAC

The AD2700 series is ideal for use with the AD7520 series of CMOS D/A converters. A CMOS converter in a unipolar application as shown below performs an inversion of the voltage reference input. Thus, use of the +10 volt AD2700 reference will result in a 0 to -10 volt output range. Alternatively, using the -10 volt AD2701 will result in a 0 to +10 volt range. Two operational amplifiers are used to give a bipolar output range of -10 volt to +10 volt, as shown in the lower figure. Either the AD2700 or AD2701 can be used, depending on the transfer code characteristic desired. For more detailed applications information, refer to the AD7520 Data Sheet.

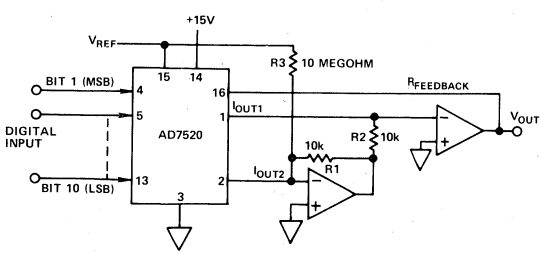


Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation



Bipolar Operation (4-Quadrant Multiplication)

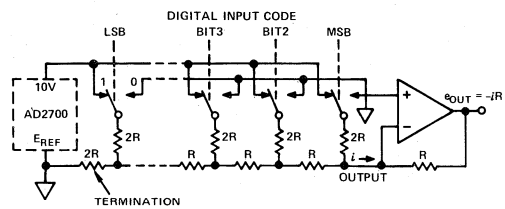
DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\ (1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\ (2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}\ (2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}\ (1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

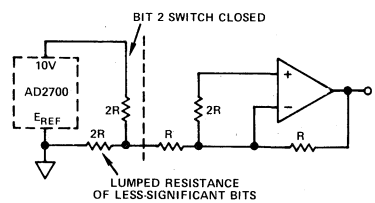
Table II. Code Table — Bipolar (Offset Binary) Operation

USING THE AD2700 VOLTAGE REFERENCE WITH D/A CONVERTER

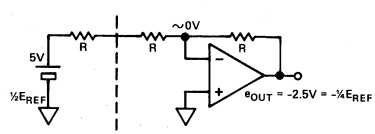
An AD2700 Voltage Reference can be used with an inverting operational amplifier and an R-2R ladder network. If all bits but the MSB are off (i.e., grounded), the output voltage is $(-R/2R)E_{REF}$. If all bits but Bit 2 are off, it can be shown that the output voltage is $\frac{1}{2}(-R/2R)E_{REF} = \frac{1}{4}E_{REF}$: The lumped resistance of all the less-significant-bit circuitry (to the left of Bit 2) is 2R; the Thevenin equivalent looking back from the MSB towards Bit 2 is the generator, $E_{REF}/2$, and the series resistance 2R; since the grounded MSB series resistance, 2R, has virtually no influence — because the amplifier summing point is at virtual ground — the output voltage is therefore $-E_{REF}/4$. The same line of thinking can be employed to show that the nth bit produces an increment of output equal to 2^{-n} E_{REF}.



a. Basic Circuit



b. Example: Contribution of Bit 2; All Other Bits "0"



c. Simplified Equivalent of Circuit (b.)

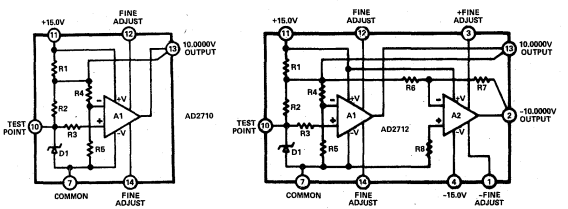
±10.000 Volt Ultra High Precision Reference Series

AD2710, AD2712

FEATURES

- **Laser Trimmed to High Accuracy: 10.000V ± 1.0mV**
- **Low Temperature Coefficient: 1ppm/°C (L Grade)**
- **Excellent Long Term Stability: 25ppm/1000hrs.**
- **5mA Output Current Capability**
- **Low Noise: 30μV p-p**
- **Short Circuit Protected**
- **No Heater Utilized**
- **Small Size (Standard 14-Pin DIP Package)**

AD2710, AD2712 FUNCTIONAL BLOCK DIAGRAMS



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PRODUCT DESCRIPTION

The AD2710 and AD2712 are temperature-compensated, hybrid voltage references which provide precise 10.000V output from an unregulated input level from 13.5 to 16.5 volts. Active laser trimming is used to trim both the initial error at +25°C as well as the temperature coefficient, which results in ultra high precision performance previously available only in oven-regulated modules. The 1.0mV maximum initial error and 1ppm/°C guaranteed maximum temperature coefficient of the AD2710L and AD2712L represent the best performance combination available without using ovens or heated substrates for temperature regulation.

The AD2710 series of precision 10.000 volt references offer the user unequalled accuracy and stability with performance guaranteed over the 0 to +70°C temperature range. The devices combine the recognized advantages of thin film technology and active laser trimming with a unique integrated ceramic package design to provide an excellent reference for use in applications requiring high accuracy and stability.

The AD2710 is recommended for use as a reference for 10-, 12- and 14-bit D/A converters which require an external reference. The device is also suitable for many types of high resolution A/D converters, either successive approximation or integrating designs. The 5mA output drive capability of the device also makes the AD2710 ideal for use as a master system reference.

For systems requiring a dual tracking reference, the AD2712 offers both positive and negative outputs in a single package. All units are packaged in an integrated ceramic 14-pin side-brazed package offering superior reliability over other package designs.

PRODUCT HIGHLIGHTS

1. Active laser trimming of both initial accuracy and temperature coefficient results in very high accuracy over the temperature range without the use of external components. AD2710 has a maximum deviation from 10.000 volts of ±1.00mV at 25°C with no external adjustments.
2. The AD2710 and AD2712 are well suited for a broad range of applications requiring an accurate, stable reference source such as data converters, test and measurement systems and calibration standards.
3. The performance of the AD2710 series is achieved by a well-characterized design and close control over the manufacturing process. This eliminates the need for temperature-controlled ovens to provide stability.
4. The advanced multilayer integrated ceramic package results in superior electrical performance as well as inherent high reliability.

SPECIFICATIONS (typical @ V_S ±15V after a 5 minute warm-up at +25°C, no load condition unless otherwise specified)

Model		AD2710KN	AD2710LN	AD2712KN	AD2712LN
ABSOLUTE MAXIMUM RATINGS					
Input Voltage (for applicable supply)		±18V	*	*	*
Power Dissipation @ +25°C		300mW	*	450mW	**
Operating Temperature Range		0 to +70°C	*	*	*
Storage Temperature Range		−55°C to +100°C	*	*	*
Lead Temperature (soldering, 20s)		+260°C	*	*	*
Short Circuit Protection (to GND)		Continuous	*	*	*
OUTPUT VOLTAGE ERROR[1]					
+25°C		±1.0mV max	*	*	*
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT[2]					
+10V Output	+25°C to +70°C	±2ppm/°C max	±1ppm/°C max	±2ppm/°C max	±1ppm/°C max
	0 to +25°C	±5ppm/°C max	*[3]	*	*[3]
−10V Output[4]	+25°C to +70°C	Not Applicable	Not Applicable	±3ppm/°C max	±2ppm/°C max
	0 to +25°C	Not Applicable	Not Applicable	±5ppm/°C max	**
LINE REGULATION					
V_S = ±13.5 to ±16.5[5]		125μV/V(200μV/V max)	*	*	*
OUTPUT CURRENT		10mA	*	*	*
LOAD REGULATION					
I_O = 0 to ±5mA		50μV/mA(100μV/mA max)	*	*	*
OUTPUT RESISTANCE		0.05Ω	*	*	*
INPUT VOLTAGE[5]					
Operating Range		±13V to ±18V	*	*	*
Specified Performance		±13.5V to ±16.5V	*	*	*
QUIESCENT SUPPLY CURRENT					
V_S+		9mA(14mA max)	*	12mA (16mA max)	**
V_S−[5]		Not Applicable	Not Applicable	2mA (4mA max)	**
NOISE					
0.1 to 10Hz		30μV p-p	*	*	*
LONG TERM STABILITY					
T_A = +25°C		25ppm/1000 Hours	*	*	*
EXTERNAL TRIM RANGE[6]		±10mV	*	*	*
PACKAGE OPTION[7]		HY14B	*	*	*

NOTES
*Same as AD2710KN. **Same as AD2712KN performance.
[1] Specifications apply to both outputs of the AD2712.
[2] Refer to next page for definition of temperature-related error specifications.
[3] The AD2710LN and AD2712LN outputs are guaranteed for a maximum ±2ppm/°C temperature coefficient over the +15°C to +25°C temperature range. Refer to Figure 1.
[4] The +10V and −10V outputs of the AD2712 typically track within ±1ppm/°C over the specified temperature range.
[5] Negative power supply not required for AD2710.
[6] Use of the output trim will change the temperature coefficient approximately 0.3ppm/°C for each millivolt of adjustment.
[7] See Section 19 for package outline information.
Specifications subject to change without notice.

UNDERSTANDING THE SPECIFICATIONS

The AD2710 and AD2712 precision references are designed for applications requiring both the lowest possible initial error at room temperature and the lowest possible temperature drift. The specification for initial error is relatively straight-forward, and is the absolute error from exactly 10.000V. The specification for temperature drift, however, must be explained.

Various methods have been used to specify the temperature drift of voltage references, including the "butterfly", "box", and "modified-box" (or total error) methods. The AD2710 and AD2712 are specified with the "butterfly" method.

Using three or more temperatures provides the user with a tighter drift specification, eliminating possible mid-range excursions. The AD2710 and AD2712 have been designed and characterized as having a smooth drift curve with a virtually straight segment from +25°C to +70°C. The typical curve as shown is concave downward and gradually increases slope near 0°C.

As can be seen from Figure 1, the AD2710L and AD2712L +10V outputs will exhibit a maximum temperature coefficient of ±1ppm/°C (±2ppm/°C for "K" grade) from +25°C to +70°C. Over the short range between +15°C and +25°C, the AD2710L and AD2712L +10V outputs have a maximum drift of only ±2ppm/°C and a maximum drift of ±5ppm/°C from 0 to +15°C. The negative output of the AD2712L has a similar temperature coefficient characteristic with a maximum slope of ±2ppm/°C from +25°C to +70°C. This limit continues from +25°C to +15°C and then increases to a ±5ppm/°C maximum slope from +15°C and 0°C. Every unit is 100 percent tested and guaranteed to meet these specifications over the full 0 to +70°C temperature range.

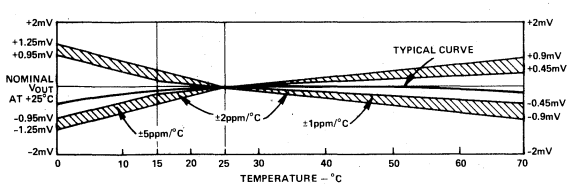


Figure 1. Maximum Change from +10V Output from +25°C Value vs. Temperature

All grades of the AD2710 and AD2712 are tested after a five minute warm-up period. This warm-up allows the entire circuit to attain thermal equilibrium. The warm-up drift is approximately 500 microvolts and is completely settled approximately three minutes after turn-on. Figure 2 shows the typical warm-up characteristics of the AD2710.

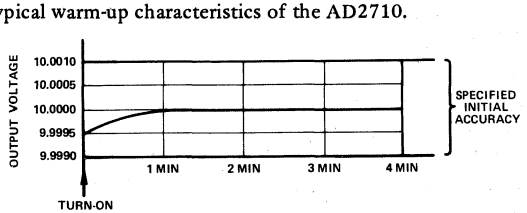


Figure 2. AD2710 Typical Warm-Up Drift

USING THE AD2710 AS A DAC REFERENCE

Digital-to-analog converters require a reference to establish the full scale output range. It is this reference which will ultimately determine the absolute accuracy of the converter. While many converters include internal reference sources, better overall performance can be obtained if a higher precision external reference is used.

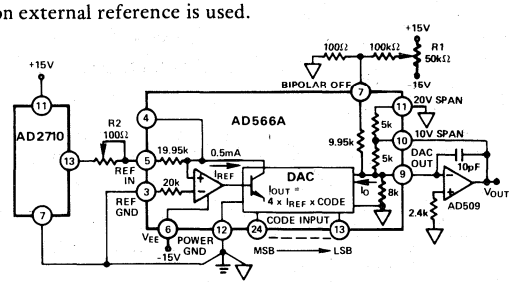


Figure 3. Low Drift 12-Bit D/A Converter

Figure 3 shows the AD2710 used with the AD566A high-speed 12-bit DAC. The AD566AKD is laser trimmed for ±1/4LSB maximum nonlinearity, and exhibits a gain temperature coefficient of 3ppm/°C. Use of the AD2710LN reference will result in a worst case total gain temperature coefficient of 4ppm/°C. After initial calibration of the DAC scale factor at room temperature, 12-bit absolute accuracy can be maintained over the +15°C to +70°C temperature range. The high output current capability of the AD2710 allows it to serve as a reference for up to 10 such converters in a system.

The resolution of the AD566A can be extended as shown in Figure 3 by summing the output of another DAC. In this example, an AD559 is used to provide 4 additional bits. Since the AD559 is driven from the same AD2710 reference as the AD566A which provides the higher-order bits, and uses a similar internal thin-film resistor ladder, it will exhibit first-order temperature tracking. While this circuit provides 16-bits of resolution, it is only as accurate as the AD566A used for the most significant bits. Use of an AD566AKD will typically achieve ±0.003% accuracy (±1/2LSB at 14 bits).

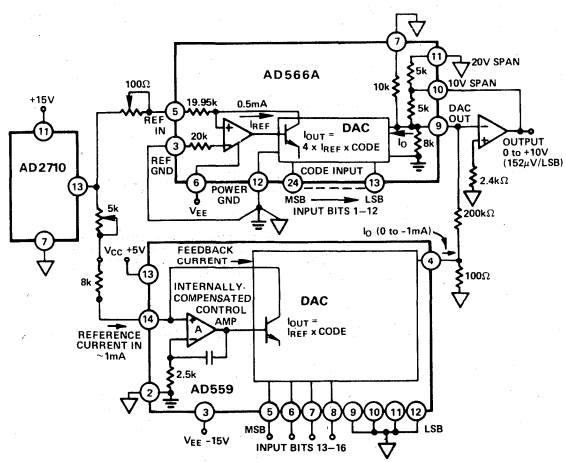
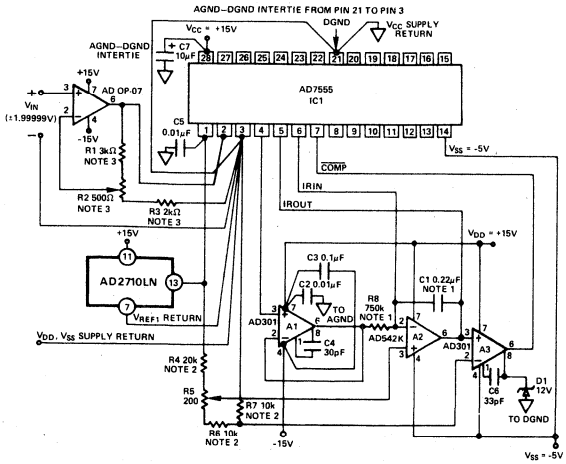


Figure 4. 16-Bit Binary DAC with AD2710 Reference

HIGH RESOLUTION ANALOG-TO-DIGITAL CONVERSION

The AD2710 is well-suited to both system and instrument-level analog-to-digital converter reference requirements. The excellent absolute accuracy and low temperature drift allow low-cost measurement systems to offer high levels of performance.

The AD7555 is a 4½/5½ digit ADC subsystem which uses the quad-slope conversion technique to achieve high accuracy at low cost. This patented conversion process performs automatic correction for offsets and other errors in the analog circuitry as a part of each conversion. Total scale factor drift 1.2ppm/°C is possible using the AD2710L reference and medium-precision external amplifiers. This represents a full scale drift of less than ±10 counts in ±200,000 from +15°C to +45°C. Less than 1 count of drift will occur in the 4 1/2 digit mode.



NOTES:
1. R8 C1 VALUES SHOWN ARE FOR 5 1/2 DIGIT MODE. FOR 4 1/2 DIGIT MODE R_8 = 360k, C_1 = 0.22µF. SUITABLE CAPACITORS AVAILABLE FROM COMPONENT RESEARCH CO. INC., 1655 26th STREET, SANTA MONICA, CA. 90404. (STOCK NUMBER FOR 0.22µF CAPACITOR IS D11B224KXW).
2. R4, R6, R7 1% TOLERANCE
3. R1, R3 SHOULD TRACK WITHIN 0.5ppm/°C. EITHER BULK METAL OR WIRE-WOUND RESISTORS (OR A THIN-FILM NETWORK) SHOULD BE USED. R2 SHOULD BE A LOW-TC TYPE POTENTIOMETER OR A SELECTED LOW DRIFT FIXED RESISTOR.

Figure 5. High Accuracy Low Drift A/D Converter

The AD7555 was designed for use with a 4.096V reference, which produces a ±2 volt input range. When the AD2710 is used, the input range is increased to ±4.88281V (24.4µV/count). The new scaling can be handled either by using a precision gain stage before the AD7555 analog input as shown or by using a microprocessor to digitally correct the scale. The actual input signal value can be computed by multiplying the count produced by the AD7555 by V_{REF1} (10 volts in this case), and dividing the result by 409600. Details of the digital circuitry of the AD7555 can be found on the AD7555 data sheet.

It should be noted that when the AD7555 is used with the AD2710 10 volt reference, it is necessary to use a V_{CC} greater than 10 volts. Thus the digital inputs and outputs of the ADC will be compatible with CMOS logic levels.

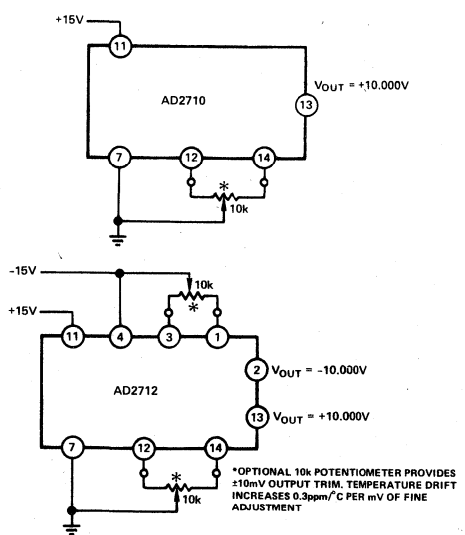


Figure 6. Optional Fine Trim Connections

CMOS Monolithic DC-DC Voltage Converter & Reference

AD7560

PRELIMINARY TECHNICAL DATA

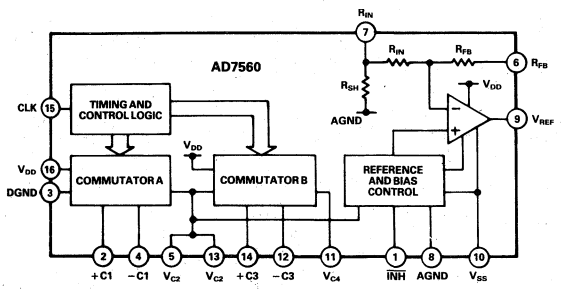
FEATURES

- Efficient Series Stacked dc/dc Converters Which Provide Multiple Outputs From a Single +5V Supply (−5V, −10V, −15V, +10V, +15V)
- On-Chip −10V Reference Voltage Output
- High Reference Voltage Power Supply Rejection
- Minimum Circuit Requires Only Two Low Cost Capacitors

APPLICATIONS

- Negative Reference Voltage Generation for Data Acquisition Systems, from a Single +5V Supply
- Op-Amp Supply Generation; ±5V, ±15V
- Low Power, High Efficiency Voltage Converter for Battery Operation

AD7560 FUNCTIONAL BLOCK DIAGRAM



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GENERAL DESCRIPTION

The AD7560 is a monolithic CMOS voltage converter plus voltage reference circuit. It performs both voltage inversion and subsequent voltage multiplication of the incoming positive supply voltage. It contains two converter circuits, A and B, in series to provide two negative output voltages of approximately $-V_{DD}$ and $-3V_{DD}$ from the $+V_{DD}$ input. The unregulated $-3V_{DD}$ output from converter B is used to generate an internal reference voltage of −5V. This is buffered and amplified to provide a temperature compensated −10V output (V_{REF}, pin 9) which can sink over 1.0mA. In applications where the reference output is not required this section can be powered down via the reference inhibit input $\overline{INH}$, pin 1.

An on-chip oscillator is provided to drive the converters. The oscillator frequency is determined by the addition of an external capacitor. Additionally, if converter synchronization to an external clock source is required, the clock input can be driven directly from a 5V CMOS compatible clock source.

ORDERING INFORMATION

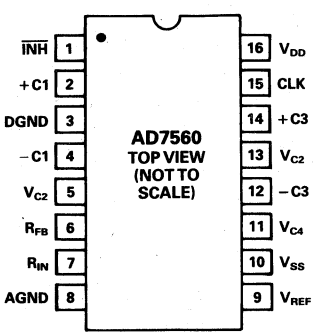
Reference Voltage Accuracy (T_{min} to T_{max})	Reference Voltage T.C. (max)	Temperature Range & Package[1] −25°C to +70°C Plastic
±500mV	±200ppm/°C	AD7560JN

NOTE
[1]Plastic DIP Package – N16B
See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The AD7560 produces multiple output voltages with a minimum number of external components, e.g., basic configurations require only two or four low cost general purpose electrolytic capacitors.
2. A −10V voltage reference output which can be powered down if not required.
3. The 5V CMOS compatible clock input can be driven from an external clock source (for synchronization) or can be made to oscillate with the addition of an external capacitor.
4. All outputs are short-circuit proof and latch-up free.

PIN CONFIGURATION



SPECIFICATIONS

(V_{DD} = +5V[1], F_{CLK} = 6kHz external clock, 0 ≤ I_{REF} ≤1mA (see test circuits, Figures 1 & 2). All specifications T_{min} to T_{max}[2] unless otherwise noted)

Parameter	$\overline{INH}$ = 0V[3]	$\overline{INH}$ = V_{DD}[4]	Units	Conditions/Comments
CONVERTER A, V_{C2} (Pins 5 & 13)				
Voltage Conversion Factor, α_A				
T_A = +25°C	0.90	0.68	min	$I_{C2} = I_{C4}$ = 0mA
	0.95	0.80	typ	
T_{MIN}, T_{MAX}	0.85	0.65	min	
	0.90	0.75	typ	
V_{C2} Output Source Resistance				
T_A = +25°C	160	N.A.	Ω max	I_{C2} = 5mA, I_{C4} = 0mA, I_{REF} = N.A. (Not Applicable)
	120	N.A.	Ω typ	
T_{MIN}, T_{MAX}	200	N.A.	Ω max	
T_A = +25°C	N.A.	160	Ω max	I_{C2} = 1mA, I_{C4} = 0mA, 0≤I_{REF} ≤0.25mA
	N.A.	120	Ω typ	
T_{MIN}, T_{MAX}	N.A.	200	Ω max	
V_{C2} Short Circuit Current	30	30	mA typ	Short Circuit to DGND
CONVERTER B, V_{C4} (Pin 11)				
Voltage Conversion Factor, α_B				
T_A = +25°C	2.80	2.35	min	$I_{C2} = I_{C4}$ = 0mA
	2.90	2.45	typ	
T_{MIN}, T_{MAX}	2.75	2.30	min	
	2.85	2.35	typ	
V_{C4} Output Source Resistance				
T_A = +25°C	900	N.A.	Ω max	I_{C2} = 0mA, I_{C4} = 2.5mA, I_{REF} = N.A.
	750	N.A.	Ω typ	
T_{MIN}, T_{MAX}	1200	N.A.	Ω max	
T_A = +25°C	N.A.	900	Ω max	I_{C2} = 0mA, I_{C4} = 0.25mA, 0≤I_{REF} ≤0.25mA
	N.A.	750	Ω typ	
T_{MIN}, T_{MAX}	N.A.	1200	Ω max	
V_{C4} Short Circuit Current	20	20	mA typ	Short Circuit to DGND
VOLTAGE REFERENCE[5], V_{REF} (Pin 9)				
Reference Voltage Output	N.A.	−10.00	V	
Reference Voltage Accuracy	N.A.	±500	mV max	
Reference Temperature Coefficient[6]	N.A.	±200	ppm/°C max	
Reference Voltage Drift	N.A.	±60	mV typ	1,000 hours, +70°C
Reference Sink Current, I_{REF}	N.A.	1.0	mA min	
		1.5	mA typ	
Reference Output Resistance	–	3	Ω max	
	20	1	kΩ typ	
Reference Short Circuit Current	0.4	5	mA max	Short Circuit to AGND
Power Supply Rejection				
V_{REF}/V_{DD}	N.A.	±12	mV/V max	
		±6	mV/V typ	
Buffer Amplifier Resistor Values				
R_{IN} and R_{FB}	30/50/75	30/50/75	kΩ min/typ/max	
Input Shunt Resistance, R_{SH}	75	75	kΩ typ	R_{SH} is Approximately 1.5R_{FB}
DIGITAL INPUTS				
INH (Pin 1)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±10	±10	µA max	V_{IN} = 0V or V_{DD}
C_{IN} Input Capacitance[7]	7	7	pF max	
CLK (Pin 15)				
V_{IH} Input High Voltage	+3.0	+3.0	V min	
V_{IL} Input Low Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	±25	±25	µA max	V_{IN} = 0V or V_{DD}
	±15	±15	µA typ	
POWER REQUIREMENTS				
Power Supply Current, I_{DD}	6	22	mA max	$I_{C2} = I_{C4}$ = 0mA
	3	15	mA typ	
	16	N.A.	mA max	I_{C2} = 0mA, I_{C4} = 2.5mA
	12	N.A.	mA typ	
V_{DD} Operating Range	+4.5/+5.5	+4.75/+5.5	V	Specifications not guaranteed outside V_{DD} = +5V ±5%
	+4.5/+7.5	+4.75/+7.5	V	Degraded performance over this range. External limit resistors required. See Figure 15.

NOTES

[1]V_{DD} = +5V ±5%.

[2]Temperature range of AD7560JN is −25°C to +70°C.

[3]See test circuit, Figure 1.

[4]See test circuit, Figure 2.

[5]To meet this voltage reference specification (T_{min} to T_{max}) external loading on V_{C2} (pins 5 & 13) and V_{C4} (pin 11) should be restricted to satisfy conditions $|V_{C4}| \geq |V_{REF}| + 0.5V$. Refer to Figures 4 and 9.

[6]Using internal resistors R_{FB} and R_{IN}.

[7]Guaranteed by design, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND	−0.3V, +8V
V_{DD} to V_{C2}	−0.3V, +16V
V_{DD} to V_{C4}	−0.3V, +32V
V_{DD} to V_{SS}	−0.3V, +32V
V_{C2}, −C1, (DGND = 0V)	V_{DD}, −8V
V_{C4}, −C3, (DGND = 0V)	V_{DD}, −24V
+C1 (DGND = 0V)	−0.3V, V_{DD}
+C3 (DGND = 0V)	V_{C2}, V_{DD}
AGND to DGND	V_{SS}, V_{DD}
CLK, $\overline{INH}$, (DGND = 0V)	V_{DD}, −5V
V_{REF}	V_{DD}, V_{SS}
R_{IN}, R_{FB} (AGND = 0V)	±15V
I_{DD}	100mA dc
I_{REF} Short Circuit Duration to V_{DD}	Continuous
I_{C2} Short Circuit Duration to DGND	Continuous
I_{C4} Short Circuit Duration to DGND	Continuous
Operating Temperature Range, JN	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Package)	
to +50°C	450mW
Derate Above +50°C by	6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational selections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TEST CIRCUITS

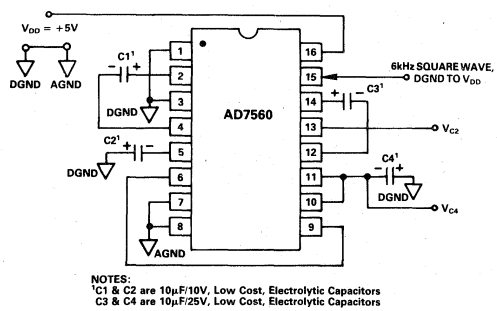


Figure 1. Test Circuit for dc-dc Converter Only, $\overline{INH}$ = 0V

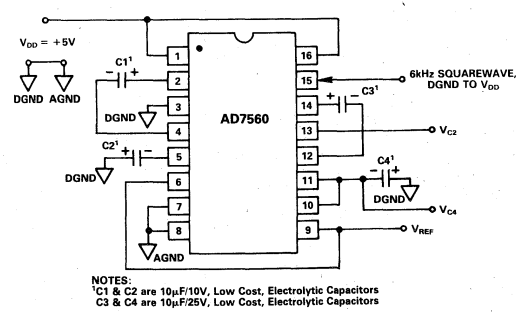


Figure 2. Test Circuit for dc/dc Converter & Voltage Reference, $\overline{INH}$ = V_{DD}

Typical Performance Characteristics

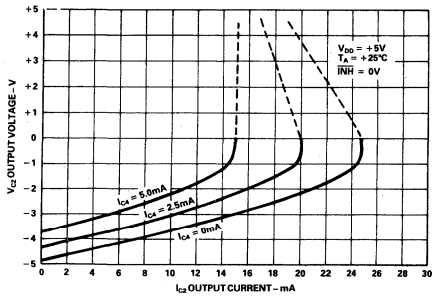


Figure 3. V_{C2} Output Voltage vs. I_{C2} Output Current for Different Values of I_{C4} (See Figure 1)

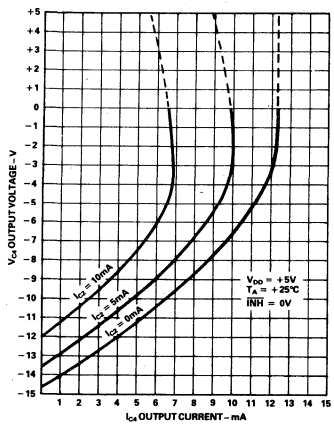


Figure 4. V_{C4} Output Voltage vs. I_{C4} Output Current for Different Values of I_{C2} (see Figure 1)

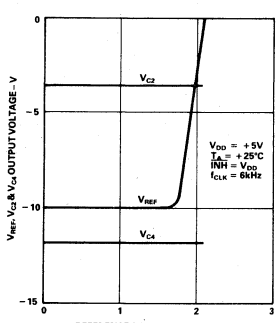


Figure 5. V_{REF}, V_{C2} and V_{C4} Output Voltage Levels vs. Reference Sink Current I_{REF} (see Figure 2)

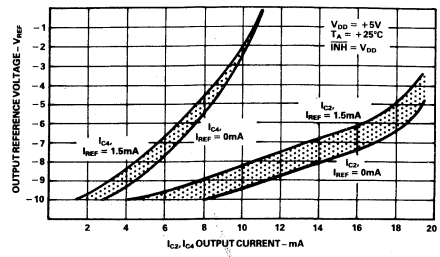


Figure 6. Output Reference Voltage V_{REF} vs. I_{C2} and I_{C4} Load Currents (see Figure 2)

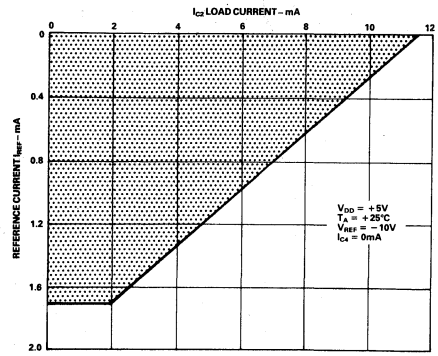


Figure 7. I_{C2} vs. I_{REF} Operating Area (Shaded) for V_{REF} = – 10V (see Figure 2)

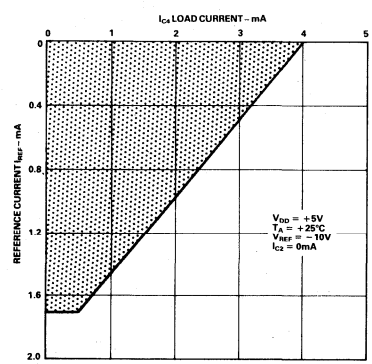


Figure 8. I_{C4} vs. I_{REF} Operating Area (Shaded) for V_{REF} = – 10V (see Figure 2)

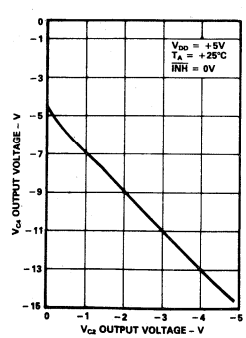


Figure 9. V_{C4} Output Voltage vs. V_{c2} Output Voltage i.e., V_{C4} Output Voltage as a Function of Current Loading on V_{C2} (see Figure 1)

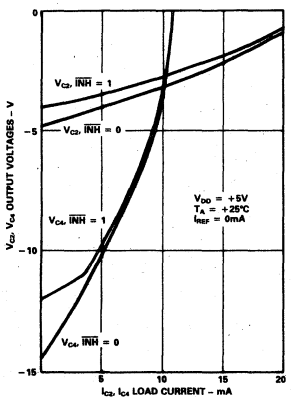


Figure 10. Effect of INHIBIT Input ($\overline{INH}$, Pin 1) on Converter Efficiency

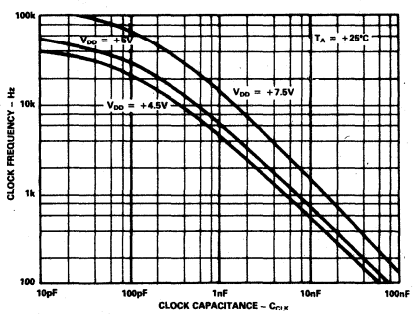


Figure 11. Typical Clock Frequency vs. Clock Capacitance

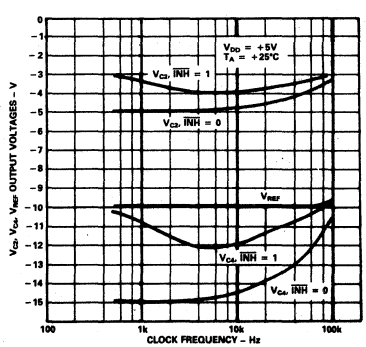


Figure 12. V_{C2}, V_{C4} and V_{REF} Output Voltages vs. Clock Frequency

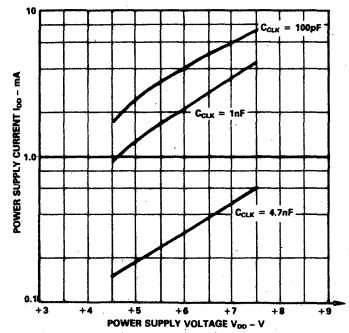


Figure 13. Power Supply Current vs. Power Supply Voltage for Different Values of C_{CLK}

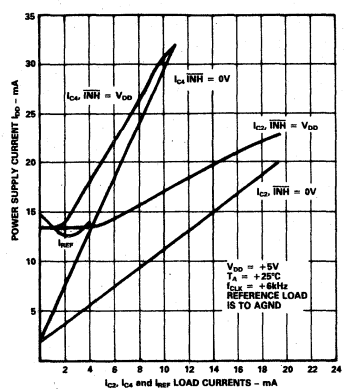


Figure 14. Power Supply Current I_{DD} vs. I_{C2}, I_{C4} and I_{REF} Load Currents

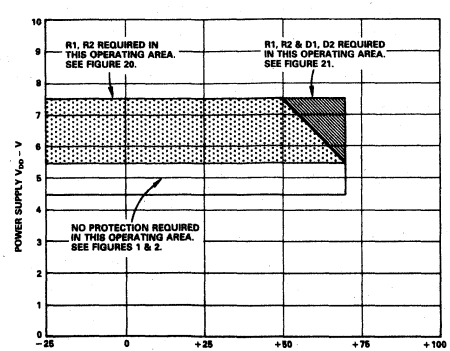


Figure 15. Operating Areas as a Function of Supply Voltage and Temperature

CIRCUIT DESCRIPTION

The AD7560 consists of two separate dc-to-dc converters which are driven in series plus a precision voltage reference with buffer amplifier. The voltage conversion circuitry of the AD7560 may best be understood by referring to Figure 16. This shows the two converters A, and B, each comprising four switches and two external capacitors.

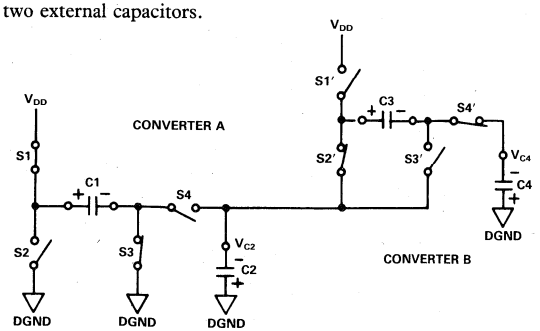


Figure 16. Converter Circuitry with External Capacitors Included

Consider initially converter A, switches S1 through S4, and capacitors C1 and C2. The oscillator and voltage-level translator sections provide the control signals to the four switches. During the charge phase, capacitor C1 is charged through S1 and S3 (S2 and S4 open) to a voltage equal to the supply voltage V_{DD}. In the pump phase, S2 and S4 are closed (S1 and S3 open) and the charge is pumped or transferred from capacitor C1 to C2. The voltage on C2 (V_{C2}, pins 5 and 13) is equal in value and opposite in polarity to $+V_{DD}$ with respect to DGND (assuming ideal switches and no load on C2). Since a finite time is required after power-on for the voltage to build up across C2 this discussion has assumed that steady state conditions have been reached.

Operation of the second converter is identical with the first except that capacitor C3 is now charged between $+V_{DD}$ and $-V_{DD}$.

This means that during the charge phase capacitor C3 will charge to $(+V_{DD}) - (-V_{DD})$ or $+2V_{DD}$. This voltage is then pumped to capacitor C4. The subsequent voltage on C4 (V_{C4}, pin 11) is ideally $3V_{DD}$ and is negative with respect to DGND. When the first converter is in the charge phase, the second is in the pump phase and vice versa. Converter timing is derived from an on-chip oscillator which can be free-running or synchronized with an externally applied clock.

Figures 3 and 4 in the Typical Performance section show output voltage vs. load current characteristics for converter A (V_{C2}) and converter B (V_{C4}) outputs respectively.

The reference portion of the AD7560 consists of an internal reference voltage circuit and an output buffer amplifier (see Figure 17). Both the reference circuit and the amplifier obtain their bias conditions from a bias controller which is powered by V_{C2} (converter A output) via an internal connection and from an externally applied negative voltage to V_{SS} (pin 10). The amplifier operating current is supplied from V_{DD} and V_{SS}. Normally the voltage output V_{C4} available on C4 (converter B output) is used as the V_{SS} supply. The reference voltage circuit, which is referenced to analog ground (AGND, pin 8), provides a stable temperature compensated -5V reference voltage at the noninverting input of the buffer amplifier A1. R_{IN} and R_{FB} are two thin film resistors with nominal value of 50kΩ each. With R_{IN} (pin 7) tied to AGND and R_{FB} (pin 6) tied to the amplifier output V_{REF} (pin 9), the amplifier provides a noninverting gain of 2 for the internal reference. The amplifier thus supplies a precision reference

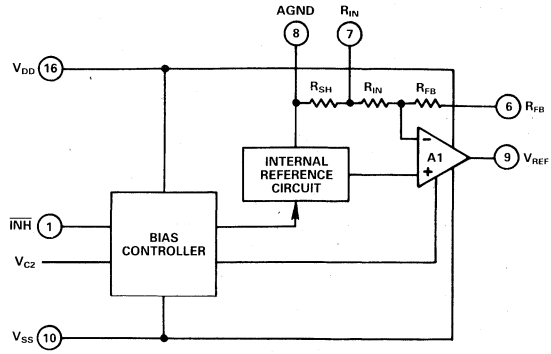


Figure 17. Reference Voltage Circuitry

voltage output of -10V with a current sink capability of over 1.0mA. The R_{IN} pin is internally tied to AGND via a shunt resistor R_{SH} which is approximately equal to 1.5 R_{FB}.

The entire reference voltage circuitry can be powered down via the INHIBIT input ($\overline{INH}$, pin 1). This reduces current loading on V_{C2} and V_{C4} and results in increased conversion efficiency of both dc-to-dc converters. See Figure 10 under Typical Performance Characteristics.

TRIM TECHNIQUES

Normal lot-to-lot variations in fabrication will produce devices whose output reference voltages will be distributed symmetrically around -10.00V. With the addition of one fixed resistor and a potentiometer it is possible to adjust every device to provide a -10.00V output (see Figure 18).

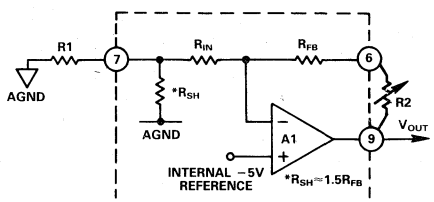


Figure 18. Trim Resistors for Reference Circuit

Trim Resistor	AD7560JN
R1 (Fixed)	10kΩ
R2 (Variable)	20kΩ

R1: thick film metal glaze, tolerance ±2%, T.C. ±100ppm/°C
R2: 20 turn cermet trimmer, tolerance ±10%, T.C. ±100ppm/°C

Table I. Recommended Trim Resistor Values

The fixed resistor R1 must be sufficiently large (when R2 = 0Ω) to ensure that the output reference voltage of any device is less than -10.00V. Potentiometer R2 is then increased from 0Ω until the reference voltage equals -10.00V. Worst case values of R1 and R2 are indicated in Table I and, therefore, represent the minimum values required which will ensure all devices can be properly trimmed.

In the absence of external gain trim components the output reference voltage is expressed as:

$$V_{REF} = -5 \times \left(1 + \frac{R_{FB}}{R_{IN}}\right) \text{Volts}$$

This reference voltage has a typical temperature coefficient (TC) of 40ppm/°C. The internal thin-film resistors R_{IN} and R_{FB} (and R_{SH}) have typical TCs of -300ppm/°C. However, their

matching and tracking is so tight as to produce no appreciable effect on the output TC.

The inclusion of external gain trim components R1 and R2 (as shown in Figure 18) modifies the overall reference performance since these external trim resistors will have different TCs from the internal thin-film resistors. The lowest values possible for R1 and R2 should be chosen in order to minimize their effect on the overall reference TC. To obtain the lowest possible reference TC the most suitable technique for reference trimming is a "select on test" approach to choosing R1 and/or R2 as opposed to potentiometer trimming.

Referring to Figure 18, if pins 6, 7 and 9 are connected together–omitting R1 and R2–amplifier A1 is configured as a unity gain buffer amplifier making the internal −5V reference available externally. However, the current loading capability of the V_{C4} output is not appreciably increased over normal −10V reference conditions.

OUTPUT VOLTAGE CALCULATION

Since the two converters (A and B), are driven in series, current loading on either of the two storage capacitors will reduce both output voltages, V_{C2} and V_{C4}, as well as the overall converter efficiency. An approximate equivalent circuit for the converter outputs is shown in Figure 19.

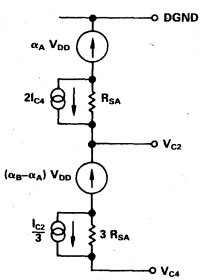


Figure 19. Equivalent Circuit for V_{C2}, V_{C4} Outputs (See Figure 1)

The output voltages using this equivalent circuit and under moderate current loads can be calculated as follows:

$$V_{C2} = -\alpha_A V_{DD} + I_{C2} R_{SA} + 2 I_{C4} R_{SA}$$

$$V_{C4} = -\alpha_B V_{DD} + 2 I_{C2} R_{SA} + 6 I_{C4} R_{SA}$$

Where: α_A is converter A conversion factor,
typically $\alpha_A = 0.95$

$$\alpha_A = \frac{|V_{C2}|}{V_{DD}}$$

α_B is converter B conversion factor,
typically $\alpha_B = 2.90$

$$\alpha_B = \frac{|V_{C4}|}{V_{DD}}$$

I_{C2} = External current load on C2

I_{C4} = External current load on C4

R_{SA} = Converter A output source resistance
$R_{SA} = 120\Omega$ typically.

If only converter B output is loaded the previous expression simplifies to:

$$V_{C4} = -\alpha_B V_{DD} + 6 I_{C4} R_{SA}$$

which is the analysis of a voltage source, $\alpha_B V_{DD}$, with an output impedance of $6R_{SA}$. Refer to the relevant current-voltage characteristics shown under Typical Performance Characteristics.

VOLTAGE CONVERSION EFFICIENCY

The efficiency of the dc-to-dc converters depends upon the switching transient losses which occur during the conversion cycles. These losses increase with increasing supply voltage V_{DD} and with increasing oscillator frequency f_{CLK}. Figure 13 shows typical power supply current I_{DD} vs. power supply voltage V_{DD} for different values of clock capacitor. The choice of values for the pump and reservoir capacitors for both converters depends primarily on the required output current loading and the peak-to-peak output voltage ripple. The AD7560 is specified with C1 = C2 = C3 = C4 = 10μF and a clock frequency of 6kHz as per the test circuit of Figure 1. The efficiency is relatively constant and optimal over a clock frequency range from 2kHz to 20kHz as indicated in Figure 12 which shows the converter output voltages as a function of clock frequency with fixed values for C1 to C4. If maximum efficiency is required at clock frequencies other than 6kHz, then the value of the pump and storage capacitors must be changed to ensure that the capacitive load impedances remain constant, i.e., if the clock frequency is reduced from 6kHz to 600Hz (a reduction of 10) then C1 to C4 values should be increased by 10 (from 10μF to 100μF). Note that the pump frequency is always one half the clock frequency at pin 15.

CLOCK FREQUENCY CONTROL

The conversion cycle time (charge and pump phases) of the dc-to-dc converters may be derived from the on-chip oscillator or else controlled by an externally applied clock signal.

1. External Clock Capacitor: When the clock input (CLK, pin 15) of the AD7560 is left open circuit, the internal oscillator runs at a typical rate of 50kHz. This frequency is lowered by connecting an external capacitor between CLK and V_{DD} or between CLK and DGND.
2. External Clock Signal: The internal oscillator can be over-ridden by an externally applied clock signal. The clock input of the AD7560 is 5V CMOS compatible and sources or sinks typically 15μA of input current. The mark/space ratio of the external clock can be highly asymmetric; minimum clock HIGH level (or LOW level) requirement is 5μs. The conversion phases change state on the negative going edge of the clock signal.

INHIBIT INPUT

As mentioned in the Circuit Description section, the reference and amplifier circuitry of the AD7560 obtains bias and operating current from the converter outputs–internally from converter A and externally (via V_{SS}) from converter B. This total current load is constant and is typically 3.5mA. Note that this 3.5mA includes any reference current that the reference amplifier sinks. In applications where the reference output voltage is not required, this current load can be reduced to negligible values by applying a logic LOW to the inhibit input ($\overline{INH}$, pin 1). The effect of the inhibit control on voltage conversion efficiency is evident from the performance characteristics as shown in Figure 10.

INTERNAL CIRCUIT PROTECTION

Referring to Figure 16, the MOS switches of both converters, S3, S4 and S3′, S4′ are N-channel devices. During normal

charge and pump cycles and also during power-up and output short circuit conditions (see following section), the voltages on the sources and drains of these output transistors vary in amplitude and polarity. To ensure optimum transistor performance (i.e., low R_{ON} and substrate reverse biased with respect to source) under any condition, their substrates must be tied to the most suitable negative potential available. To achieve this, a section of the internal control logic is devoted to sensing the voltages on the transistor sources and drains, and ensuring that their substrates are always correctly biased. This technique prevents the AD7560 from latching up during power-up and overload conditions, and also ensures optimum efficiency of both dc-to-dc converters.

OPERATION AT HIGH VOLTAGES AND ELEVATED TEMPERATURES

Under normal specified conditions, the AD7560 operates efficiently over its full temperature and supply voltage ranges. If any one of the external capacitors short circuits or if the V_{C2} or V_{C4} output is shorted to any low impedance point (e.g., V_{DD} or DGND) the AD7560 internal protection circuitry mentioned previously acts to prevent SCR action and to avoid device destruction. If the AD7560 is to operate under a combination of temperature/supply voltage conditions, as shown in the shaded areas of Figure 15, then external protection circuitry is required both to ensure device operation and, in the event of a short circuit occurring, to preclude device destruction.

Figure 20 shows the protection circuitry required when operating in the dotted area of Figure 15. Due to the inclusion of R1 in series with the V_{C2} output on pin 5, the V_{C2} output on pin 13 should not be used.

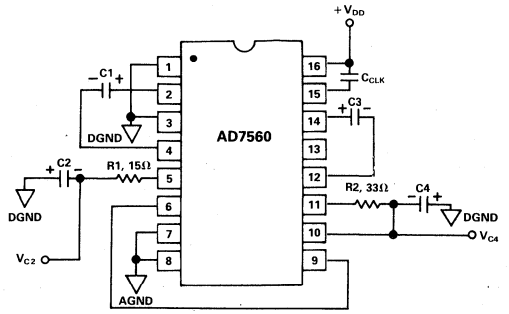


Figure 20. Location of Protection Components R1, R2 Required for Operation in Shaded Area of Figure 15

Figure 21 shows the protection circuitry required when operating in the lined area of Figure 15. Under these conditions of high temperature/high voltage, if the V_{C2} or V_{C4} output is shorted to V_{DD}, then internal parasitic transistors may be turned on leading to SCR action and possible device destruction. Diodes D1 and D2 ensure that the V_{C2} and V_{C4} outputs are never pulled higher than a diode drop above DGND. Note that these diodes will require current limiting protection via the R_{LIMIT} series resistors.

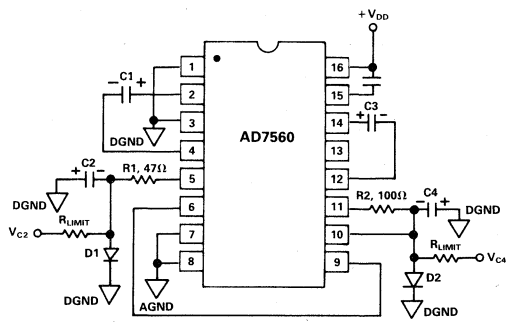


Figure 21. Location of Protection Components R1, R2 and D1, D2 Required for Operation in Lined area of Figure 15

Note that none of the above external protection is required when operating the AD7560 within specified limits of $+4.5 \leq V_{DD} \leq +5.5V$ at any temperature over its $-25°C$ to $+70°C$ range.

The AD7560 can be used in a multitude of configurations to suit different requirements and applications. Table II outlines some of these operating configurations.

Figure	Input Voltage	Nominal Output Voltages
22	+5V	−5V
23	+5V	−5V, −15V
24	+5V	−5V, −15V, −10V Reference
25	+5V	−5V, +10V
26	+5V	−5V, +15V
27	+5V	−5V, −15V, +10V
28	+5V	−5V, −15V, +15V
29	+5V	−5V, −15V, +10V, −10V Reference
30	+5V	−5V, −15V, +15V, −10V Reference

Table II. Typical AD7560 Operating Configurations

$+V_{DD}$ In, $-V_{DD}$ Out (Figure 22)
Figure 22 shows the circuitry required for single voltage conversion. C1 and C2 are standard 10μF/10V electrolytic capacitors. See Figure 3 for typical performance characteristics.

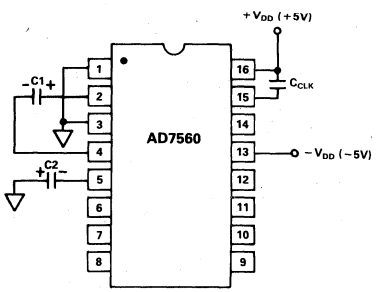


Figure 22. $+V_{DD}$ to $-V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, and $-3V_{DD}$ Out (Figure 23)
Figure 23 shows the circuitry required for voltage conversion and negative voltage multiplication. Capacitors C1 and C2 are 10μF/10V, capacitors C3 and C4 are 10μF/25V. All are standard low cost electrolytic types. Typical performance characteristics are shown in Figure 4.

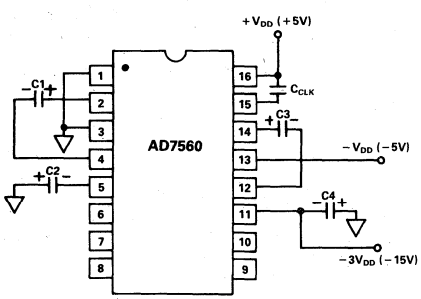


Figure 23. $+V_{DD}$ to $-V_{DD}$ and $-3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and −10V Reference Out (Figure 24)
To allow the voltage reference circuit to operate, the inhibit input ($\overline{INH}$, pin 1) is tied to V_{DD}. The feedback loop of the internal buffer amplifier is closed by tying R_{FB} (pin 6) to V_{REF} (pin 9). The amplifier input resistance R_{IN} (pin 7) is tied to AGND (pin 8) to provide a gain of +2 for the internal −5V reference (see Figure 24).

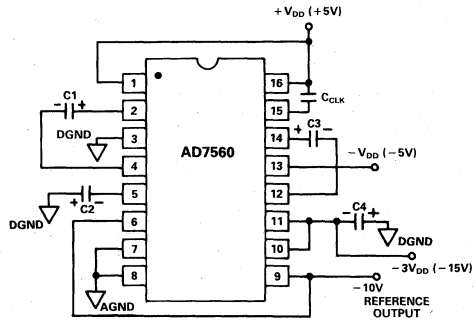


Figure 24. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and −10V Reference Output

$+V_{DD}$ In, $-V_{DD}$, $+2V_{DD}$ Out (Figure 25)
Positive voltage multiplication is possible using a diode pump scheme as shown in Figure 25. In this configuration, the input capacitor (C5) of the diode pump is switched between $+V_{DD}$ and DGND by the action of converter A. During its pump phase (pin 2 at AGND) C5 is charged to $+V_{DD} - V_F$ (where V_F is the forward diode drop of D1.) During the charge phase (pin 2 at $+V_{DD}$) the voltage on C5 plus the supply voltage is applied through D2 to capacitor C6. Thus the output voltage on C6 is $+2V_{DD} - 2V_F$.

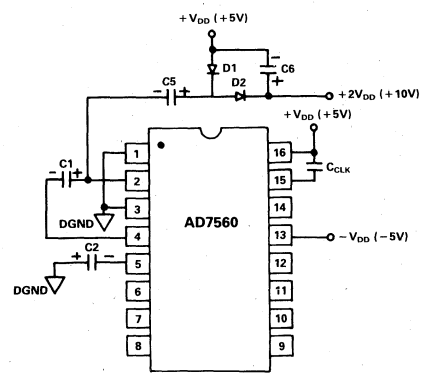


Figure 25. $+V_{DD}$ to $-V_{DD}$ and $+2V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $+3V_{DD}$ Out (Figure 26)
In this configuration, multiplication of $+V_{DD}$ to $+3V_{DD}$ is achieved by switching the input of the diode pump capacitor (C5) between $+V_{DD}$ and V_{C2}. During the pump phase of converter B capacitor C5 is charged to $+V_{DD} + V_{C2} - V_F$ (where V_F is the forward diode drop of D1). During the charge phase the voltage on C5 plus the supply voltage is applied through diode D2 to capacitor C6. The output voltage on C6 is thus $2V_{DD} + V_{C2} - 2V_F$. Capacitors C5 and C6 are 10μF/25V.

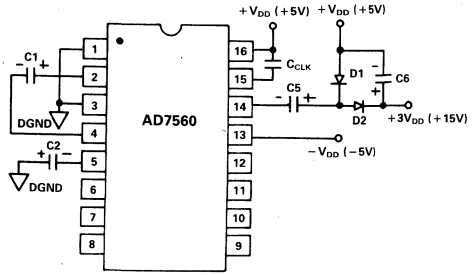


Figure 26. $+V_{DD}$ to $-V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ Out (Figure 27)
This configuration uses both converters and a diode pump. Driving the diode pump input capacitor from +C1 (pin 2) provides positive voltage doubling as explained in conjunction with Figure 25.

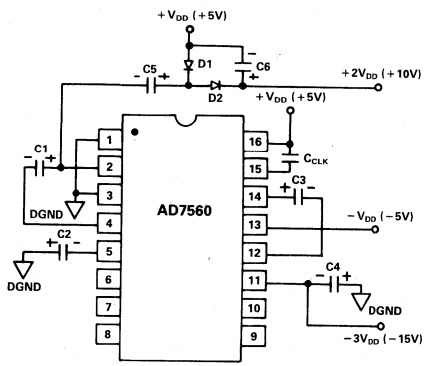


Figure 27. $+V_{DD}$ to $-V_{DD}$, $+3V_{DD}$ and $+2V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ Out (Figure 28)
This circuit is similar to Figure 27 except that the diode pump is now driven from +C3 (pin 14). This provides voltage trebling as explained in conjunction with Figure 26.

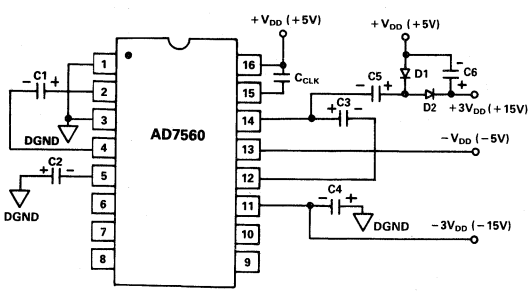


Figure 28. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+2V_{DD}$ and $-10V$ Reference Out (Figure 29)
The configuration shown in Figure 29 uses both converters, reference circuit and diode pump to provide multiple analog outputs.

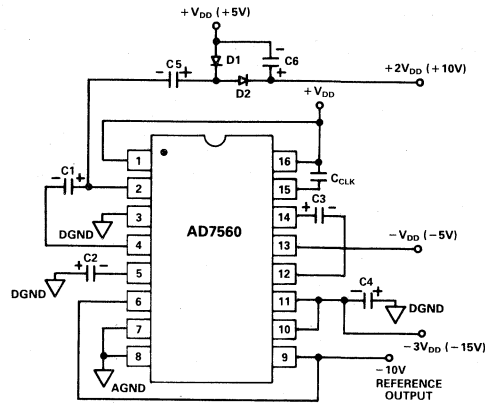


Figure 29. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+2V_{DD}$ and $-10V$ Reference Output

$+V_{DD}$ In, $-V_{DD}$, $-3V_{DD}$, $+3V_{DD}$ and $-10V$ Reference Out (Figure 30)
This circuit is similar to Figure 29 except that the diode pump is now driven from +C3 (pin 14) to provide positive voltage trebling (see Figure 30).

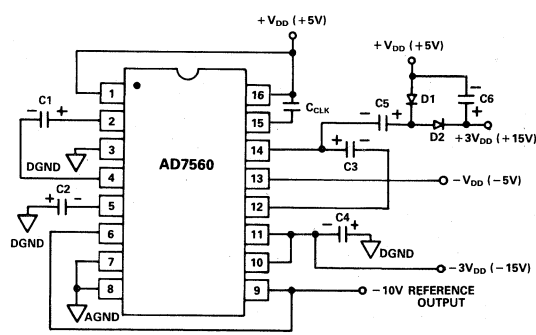


Figure 30. $+V_{DD}$ to $-V_{DD}$, $-3V_{DD}$ and $+3V_{DD}$ and $-10V$ Reference Output

INCREASING OUTPUT CURRENT CAPABILITY

It is possible to run two or more AD7560s in parallel to reduce the output resistance of both V_{C2} and V_{C4}. Figure 31 shows the circuit connections. Each converter has its own pump capacitor while the respective storage capacitors are common. The resultant output resistance of either converter A or converter B is approximately equal to that of a single device divided by the number of devices paralleled.

Each AD7560 in Figure 31 is shown with an individual clock capacitor. Thus each device runs independently at a different conversion frequency leading to increased noise in the reference voltage output. To reduce the generated noise to a minimum drive all CLK inputs in parallel from a common clock signal.

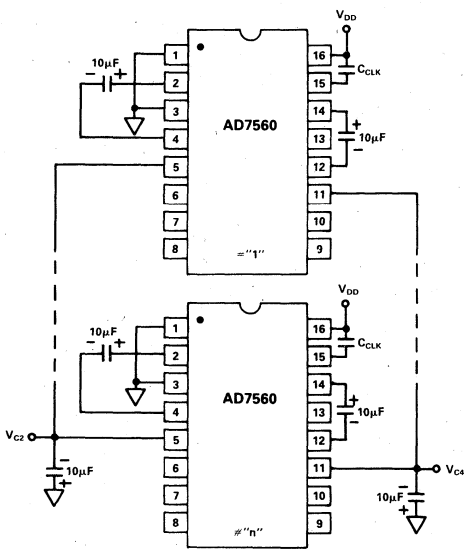


Figure 31. Paralleling Devices to Increase Output Current Capability

The reference voltage output can also benefit from the paralleling of devices. Figure 32 shows how the final AD7560 (e.g., device ≠ "n" in Figure 31) should be connected to boost the available reference current. For example, with two devices in parallel the typical reference current is increased to over 5mA.

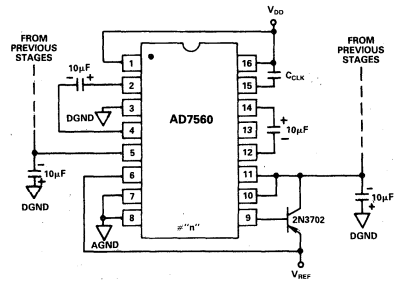


Figure 32. Reference Current Boosting

Note that this reference current boosting technique may also be used with existing −12V to −15V power supplies. Using the single general purpose PNP transistor as indicated in Figure 32 and an existing −12V power supply, one AD7560 can control up to 200mA of reference current (see Figure 33).

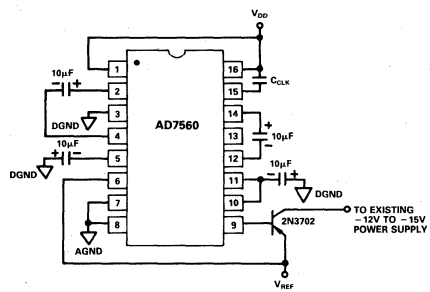


Figure 33. Reference Current Boosting Using Existing −12V to −15V Power Supply

Temperature Measurement Components

Contents

•New product since publication of *1982–1983 Databook Update.*

8

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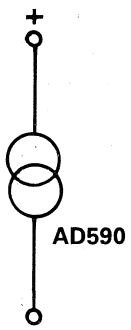
Temperature Measurement Components
Temperature Transducers



AD590

Page
Vol. I
8–15

Linear Current Output: 1μA/K
Wide Range: −55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case

AD592

Vol. I
8–23

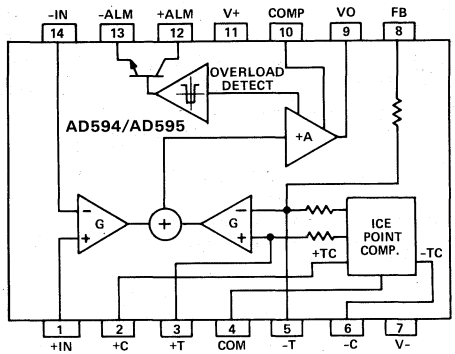
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.2°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output Signal: 1μA/°C
Two Terminal Monolithic IC: Temperature In/Current Out
Minimal Self-Heating Errors
Low Cost Plastic Package

AC2626

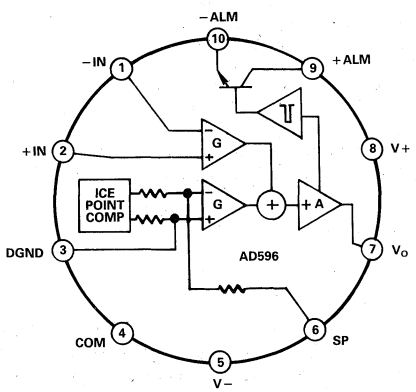
Vol. II
9–13

Linear Current Output: 1μA/K
Wide Range: −55°C to +150°C
Laser Trimmed Sensor (AD590) to ±0.5°C Calibration Accuracy (AC2626M)
Excellent Linearity: ±0.3°C Over Full Range (AC2626M)
6 Inch or 4 Inch Standard, Stainless Steel Sheath
3/16 Inch in Outside Diameter
3 Feet Teflon Coated Lead Wire
Wide Power Supply Range +4V to +30V
Fast Response: 2 Seconds (In Stirred Water)
Sensor Isolated from Sheath

Temperature Transducer Signal Conditioners



AD594/AD595



AD596

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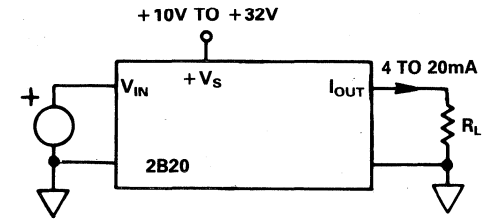
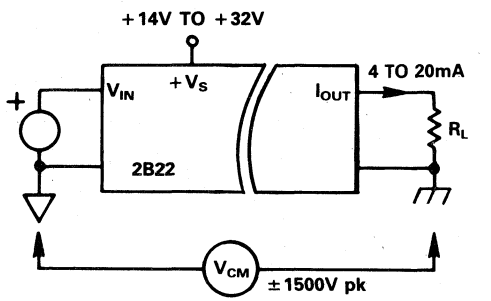
Voltage-to-Current Converters



2B20

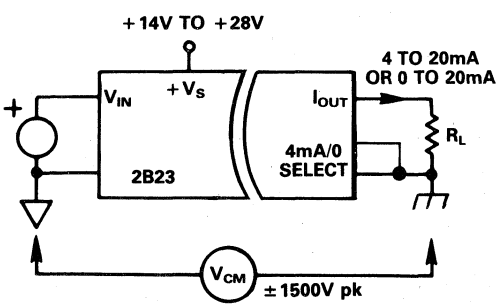
Page

Complete, No External Components Needed — Vol. II
Small Size: 1.1″ × 1.1″ × 0.4″ Module — 9–15
Input: 0 to +10V; Output: 4 to 20mA
Low Drift: 0.005%/°C max; Nonlinearity: 0.005% max (2B20B)
Wide Temperature Range: −25°C to +85°C
Single Supply: +10V to +32V
Meets ISA Std. 50.1 for Type 3, Class L and U, Nonisolated Current Loop Transmitters



2B22

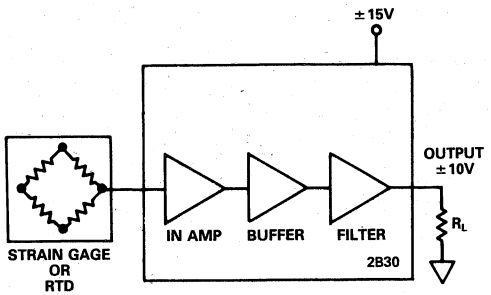
Wide Input Range: 0 to +1V to 0 to +10V — Vol. II
Standard Output Range: 4 to 20mA — 9–19
High CMV Input/Output Isolation: 1500V dc Continuous
Low Nonlinearity: 0.05% max, 2B22L
Low Span Drift: 0.005%/°C max, 2B22L
Single Supply: +14V to +32V
Meets IEEE Std. 472: Transient Protection (SWC)
Meets ISA Std. 50.1: Isolated Current Loop Transmitters



2B23

Wide Input Range, Resistor Programmable — Vol. II
Pin Programmable Output: 4 to 20mA or 0 to 20mA — 9–23
High CMV Input/Output Isolation: ±1500V pk Continuous
Low Nonlinearity: ±0.05% max (2B23K)
Low Span Drift: ±0.005%/°C max (2B23K)
Single Supply Operation: +14V to +28V
Small Size: 1.8″ × 2.4″ × 0.6″
Meets IEEE Std. 472: Transient Protection (SWC)
Meets ISA ST. 50.1: Isolated Current Loop Transmitters

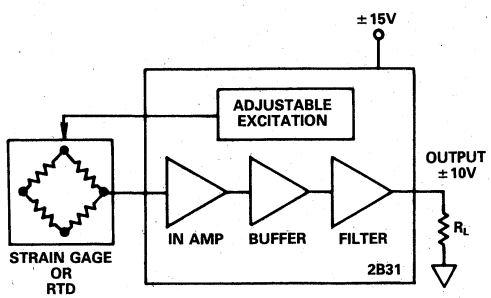
Transducer Signal Conditioners



2B30

Page
Vol. II
9-29

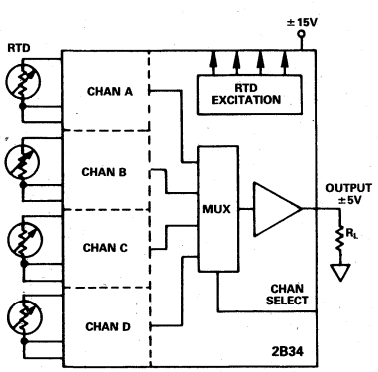
Complete Signal Conditioning Function
Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
Wide Gain Range: 1 to 2000V/V
Low Nonlinearity: 0.0025% max ("L")
High CMR: 140dB min (60Hz, G = 1000V/V)
Input Protected to 130V rms
Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)



2B31

Vol. II
9-29

Complete Signal Conditioning Function
Low Drift: 0.5μV/°C max ("L"); Low Noise: 1μV p-p max
Wide Gain Range: 1 to 2000V/V
Low Nonlinearity: 0.0025% max ("L")
High CMR: 140dB min (60Hz, G = 1000V/V)
Input Protected to 130V rms
Adjustable Low Pass Filter: 60dB/Decade Roll-Off (from 2Hz)
Programmable Transducer Excitation: Voltage (4V to 15V @ 100mA) or Current (100μA to 10mA)



2B34

Vol. II
9-35

Low Input Offset Drift: ±1.0μV/°C
Low Gain Drift: ±25ppm/°C
Low Nonlinearity: ±0.01% max (±0.005% typ)
Differential Input Protection: ±130V rms
Channel Multiplexing: 3000 chan/sec Scanning Speed
Solid State Reliability
Internal RTD Excitation/Lead Wire Compensation

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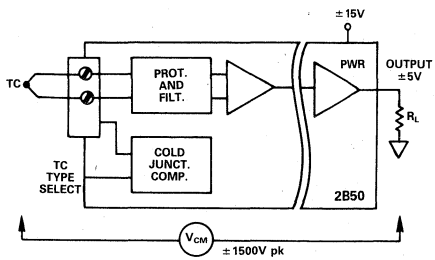
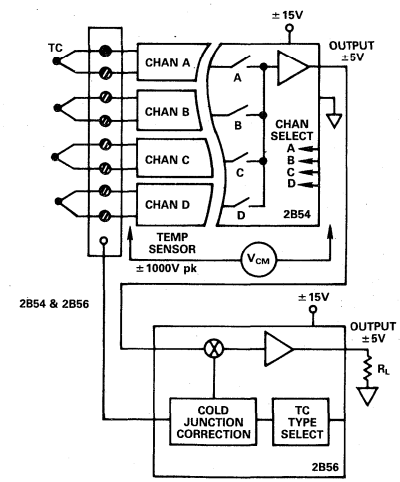
Temperature Measurement Components
Isolated Transducer Signal Conditioners



2B50

Page

- Accepts J, K, T, E, R, S or B Thermocouple Types — Vol. II 9-41
- Internally Provided Cold Junction Compensation
- High CMV Isolation: ±1500V pk
- High CMR: 160dB min @ 60Hz
- Low Drift: ±1μV/°C max (2B50B)
- High Linearity: ±0.01% max (2B50B)
- Input Protection and Filtering
- Screw Terminal Input Connections

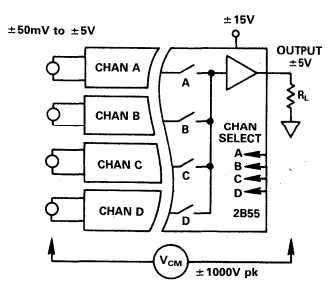


2B54

- Low Cost — Vol. II 9-47
- Wide Input Span Range: ±5mV to ±100mV
- 12-Bit Systems Compatible
- High CMV Isolation: ±1000V dc; CMR = 156dB min @ 60Hz
- Low Input Offset Voltage Drift: ±1μV/°C max (2B54B)
- Low Gain Drift: ±25ppm/°C max (2B54B)
- Low Nonlinearity: ±0.02% max (±0.012% typ)
- Normal Mode Input Protection (130V rms) and Filtering
- Channel Multiplexing: 400 chan/sec Scanning Speed
- Solid State Reliability

2B56

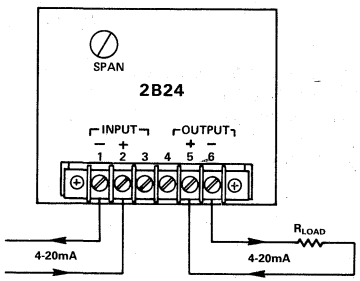
- Universal Thermocouple Compensation — Vol. II 9-53
  - Internally Provided: Types J, K, T
  - User Configurable: Types E, R, S, B
- Digitally Programmable
- High Accuracy: ±0.8°C max over +5°C to +45°C
- High Ambient Rejection: 50 to 1 min
- Low Cost
- Small Size: 1.5″ × 2″ × 0.4″



2B55

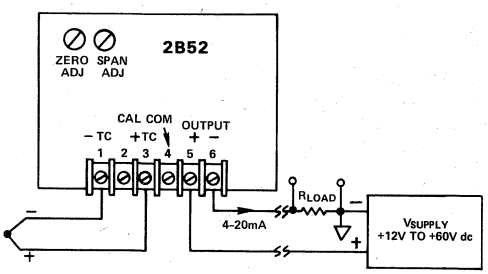
- Low Cost — Vol. II 9-47
- Wide Input Span Range: ±50mV to ±5V
- 12-Bit Systems Compatible
- High CMV Isolation: ±1000V dc; CMR = 145dB min @ 60Hz
- Low Input Offset Voltage Drift: ±5μV/°C max
- Low Gain Drift: ±25ppm/°C max
- Low Nonlinearity: ±0.02% max (G = 1 to 100)
- Normal Mode Input Protection (130V rms) and Filtering
- Channel Multiplexing: 400 chan/sec Scanning Speed
- Solid State Reliability

Two-Wire Transmitters



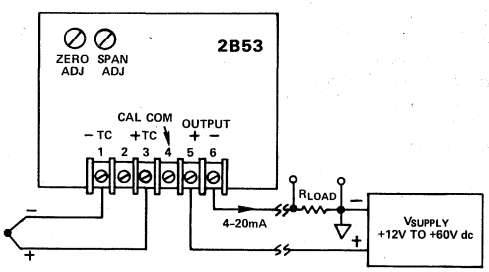
2B24

Self-Powered
Wide Input Range: 1-50mA (2B24B)
High CMV Isolation: ±1500V pk; CMR: 120dB
High Accuracy: ±0.1%
RFI/EMI Immunity
Low Cost



2B52

Accepts Type J, K or T Thermocouple Inputs
Compatible with Standard 4-20mA Loops
High Accuracy: ±0.1%
High CMV Isolation: 600V rms; CMR = 160dB
High Noise Rejection and RFI Immunity
Internal Cold Junction Compensation
Open Thermocouple Detection
Millivolt Signal Transmission
Low Cost
FM Approved



2B53

Accepts Type J, K or T Thermocouple Inputs
Compatible with Standard 4-20mA Loops
High Accuracy: ±0.1%
High Noise Rejection and RFI Immunity
Internal Cold Junction Compensation
Open Thermocouple Detection
Millivolt Signal Transmission
Low Cost

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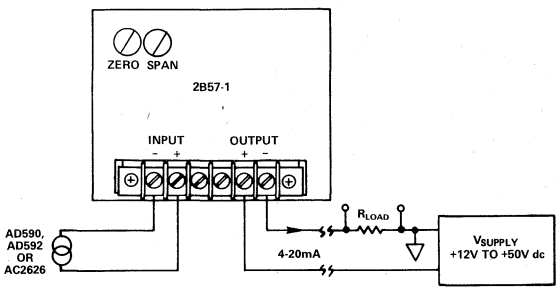
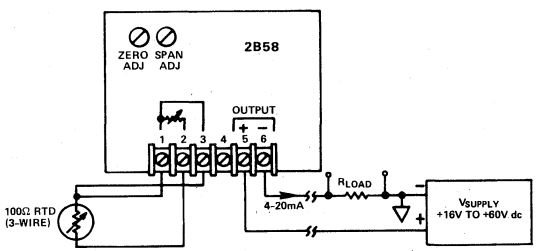
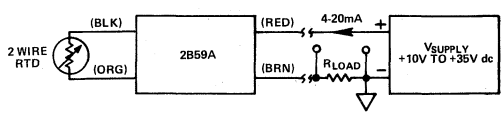


2B57

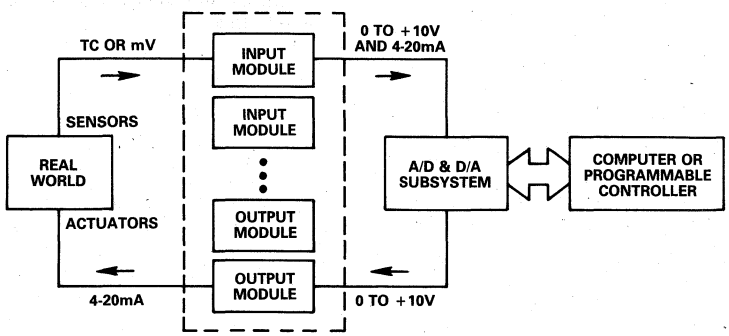


2B58



2B59

3B Series Signal Conditioning I/O Subsystems



Input Module Selection

Input Type/Span	Voltage Output	Current Output	Nonisolated Modules	Isolated Modules
dc, ± 10mV, ± 50mV, ± 100mV	± 10V	4-20mA/0-20mA	3B10	3B30
dc, ± 1V, ± 5V	± 10V	4-20mA/0-20mA	3B10	3B31
dc, ± 10V	± 10V	4-20mA/0-20mA	3B11	3B31
dc, 4-20mA, 0-20mA	0 to + 10V	4-20mA/0-20mA	3B12	3B32
Thermocouple Types J, K, T, E, R, S, B	0 to + 10V	4-20mA/0-20mA		3B37
100Ω Platinum RTD, 2-, 3-, 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B14	3B34
100Ω Platinum RTD, Kelvin 4-Wire $\alpha = 0.00385$ (linearized)	0 to + 10V	4-20mA/0-20mA	3B15	
Strain Gage ± 30mV, ± 100mV	± 10V	4-20mA/0-20mA	3B16	
AD590/AD592/AC2626 Solid State Temperature Transducer	0 to + 10V	4-20mA/0-20mA	3B13	
Wideband Strain Gage	± 10V	4-20mA/0-20mA	3B18	
Wideband mV, V	± 10V	4-20mA/0-20mA		3B40/1
AC Input	0 to + 10V	4-20mA/0-20mA		3B42/3/4
Frequency Input	0 to + 10V	4-20mA/0-20mA		3B45/6

Output Module Selection

Input Type/Span	Current Output	Nonisolated Modules	Isolated Modules
0 to + 10V, ± 10V	4-20mA/0-20mA	3B19	3B39

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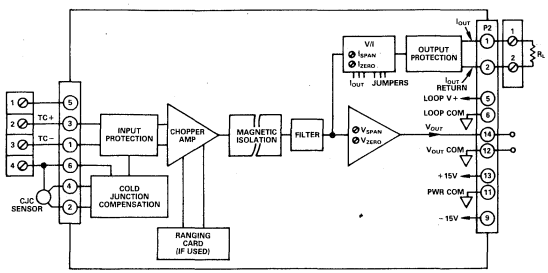
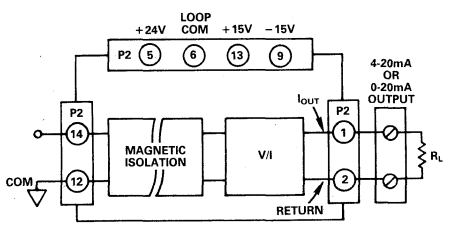
3B Series Signal Conditioning I/O Subsystems





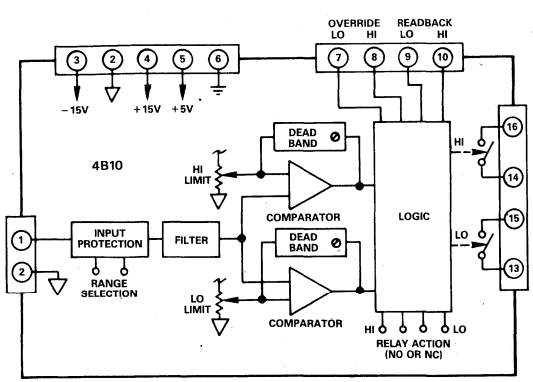
Input Modules

	Page
Wide Variety of Sensor Inputs: Thermocouples, RTD's, Strain Gages, AD590/AD592/AC2626	Vol. II 9–65
Dual High Level Outputs Voltage: 0 to +10V or ±10V Current: 4-20mA/0-20mA	
Mix and Match Input Capability Sensor Signals, mV, V, 4-20mA, 0-20mA	
High Accuracy: ±0.1%	
High Noise Rejection and RFI/EMI Immunity	
Reliable Transformer Isolation: ±1500V CMV	
Meets IEEE-STD 472: Transient Protection (SWC)	
Input Protection: 130V or 220V rms Continuous	

Output Modules

High Level Voltage Input: (0 to +10V, ±10V)	Vol. II 9–65
Process Current Output: (4-20mA/0-20mA)	
High Accuracy: ±0.1%	
Reliable Transformer Isolation: ±1500V CMV, CMR = 90dB	
Meets IEEE-STD 472: Transient Protection (SWC)	
Output Protection: 130V or 220V rms Continuous	

4B Series Alarm Limit Subsystem



Features/Benefits

Low Cost, Completely Integrated 12-Channel Modular Alarm Limit Subsystem Selection of Alarm Limit Modules Rugged Industrial Chassis, Rack or Surface Mounted On-Board Power Supplies Available	Vol. II 9–69
Alarm Modules Accept High Level Voltage and Process Current Inputs	
Complete Alarm Function per Module High Accuracy of ±0.1% Two Set Points, Adjustable Over 100% Span Dead Band Adjustment per Set Point, Adjustable Over 0.5%–10.0% Span Alarm Types are Configurable for HI or LO Operation Two Relay Outputs Display Indicates Set Points and Process Variable LED per Set Point Provides Local Alarm Indication Input Protection High RFI/EMI Immunity	
Specifications Valid Over the 0 to +70°C Temperature Range	
Easy to Install Calibrate and Service	

Orientation
Temperature Measurement Components

The AD590 and AD592 are two-terminal integrated circuit temperature transducers which produce an output current proportional to absolute temperature. The AD590 and AD592 have a standard 1μA/K output current which is inherently linear, therefore, no linearization is required.

Attention to all the detail is the key to success in most interface criteria. The following application is provided to illustrate the problems involved in designing circuits which measure physical pheonomenon.

In this application, there is a need to measure temperatures from 0 to +100°C, to within 1.0°C, at low cost, at a remote location several hundred feet from the instrumentation. The ambient temperature in the vicinity of the instrumentation is expected to be 25°C ±15°. A number of possible transducers will operate over the specified range, but the requirement for a remote measurement suggests the use of the current-output two-wire AD590 or AD592 semiconductor temperature sensor, because the current is unaffected by voltage drops and induced voltages.

Consulting the "Accuracies of the AD590"[1] we find that the AD590J, with two external trims, would be suitable; its maximum error over the 0 to 100°C range is 0.3°. This permits an allowance of 0.7° for all other errors. If a tighter tolerance were required, it would be worthwhile to consider using the AD590M with two trims, for an error *below* 0.05°C.

Since AD590 measures absolute temperature (its nominal output is 1μA/K), the output must be offset by 273.2μA in order to read out in degrees Celsius. The output of the AD590 flows through a 1kΩ resistance, developing a voltage of 1mV/K (Figure 1). The output of an AD580 2.5-volt reference is divided down by resistors to provide a 273.2mV offset, which is subtracted from the voltage across the 1kΩ resistor by an AD521 instrumentation amplifier. The AD521 provides a gain of 10.0, so that the output range, corresponding to 0 to 100°C, is 0 to 1.00V (10mV/°C).

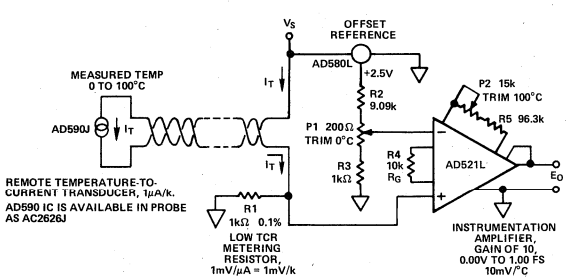


Figure 1. Thermometer Circuit

The desired system accuracy is to within 1.0°C; as noted, all errors other than that of the AD590 must contribute the equivalent of less than 0.7°. It will be helpful to assemble an error budget for the circuit, assessing the contributions of each of the elements (Table I). Errors will be expressed in degrees Celsius.

AD590 regulation. If the AD590 is excited by a voltage source of between 5 and 10V, the typical regulation is 0.2μA/V (0.2°C/V). With 1% source regulation, this contribution will be 0.01°C

AD590 linearity error. Total error for AD590J, over the 0 to 100°C range, with two trims, is 0.3°C. Those trims will be the gain and offset trims for the whole circuit, accounting for resistor and ratio errors, AD521L gain, offset and bias-current errors, AD580L voltage error, and the AD590J's calibration error 0.3°C

R1 temperature coefficient. Since R1 is responsible for the conversion of the AD590's current to voltage, high absolute accuracy is important. Consequently, we would expect to use a device having 10ppm/°C or less in this spot. For ±15°C, the maximum error is $373.2\mu A \times 10^{-5}/°C \times 15° = 0.06\mu A$ 0.06°C

(typical at 25°C and rated supply voltage unless noted otherwise)

Parameter	Condition	Specification
AD580L 2.5V VOLTAGE REFERENCE		
Output voltage	V_S = +15V	2.450V min, 2.550V max
Input voltage, operating		30V max, 7V min
Line regulation	$7V \leqslant V_{IN} \leqslant 30V$	2mV max
Temperature sensitivity	0 to 70°C	4.3mV max, 25ppm/°C, typ
Noise	0.1 to 10Hz	60μV, p-p
Stability (drift with time)	long term	250μV (0.01%)
	per month	25μV (10ppm)
AD590J 1μV/K TEMPERATURE TRANSDUCER		
Output current	Nominal at 25°C (298.2k)	298.2μA
Input voltage, operating		30V max, 4V min
Calibration error	25°C, V_S = 5V	±5°C max
Linearity error	Two trims, 0 to 100°C range	0.3°C max
Repeatability	per month	0.1°C max
Long-term drift		0.1°C max
Noise spectral density		40pA/√Hz
Power-supply rejection	$+5V \leqslant V_S \leqslant +15V$	0.2μA/V
Operating range		−55°C to +150°C
AD521L DIFFERENTIAL INSTRUMENTATION AMPLIFIER		
Gain equation (volts/volt)	Nominal	$G = R_S/R_G$
Error from equation	Untrimmed	(±0.25 - 0.004G)%
Nonlinearity	±9V output	0.1% max
Gain tempco	0 to 70°C	±(3±0.05G)ppm/°C
Voltage offset	Input	1.0mV max
	Output	100mV max
Voltage offset tempco	Input, 0 to 70°C	2μV/°C max
	Output, 0 to 70°C	75μV/°C max
Voltage offset vs. supply	Input	3μV/%
	Output, untrimmed*	0.5mV/%
Bias current	25°C	40nA max
Bias current tempco	0 to 70°C	500pA/°C
Input impedance	Common-mode	$6 \times 10^{10}\Omega \| 3.0pF$
Common-mode rejection	G = 10, dc to 60Hz, 1kΩ source unbalance	94dB min
Voltage noise	G = 10, 0.1Hz to 10Hz, p-p, RTO	225μV

*Can be reduced by trimming the output offset.

Table I. Device Specifications Pertinent to the Analysis in the Text

[1] Accuracies of the AD590 Application Note, Analog Devices.

AD580 temperature coefficient. The specified tempco for the AD580L is 25ppm/°C typical (61ppm/°C max over the range 0 to 70°C). Since operation is over a narrow range, the typical value is most useful, unless the AD580 has a critical effect on the overall error. $25 \times 10^{-6}/°C \times 273mV \times 15° = 0.1mV$ 0.10°C

Resistive divider tempco. The absolute values of R2 and R3 are of considerably less importance than their ability to track. 10ppm/°C is a reasonable value for tracking tempco. $10^{-5}/°C \times 273mV \times 15° = 0.04mV$ 0.04°C

Common-mode error. At a gain of 10, the minimum common-mode error of the AD521L amplifier is 94dB, one part in 50,000 of the common-mode voltage (273mV), or 5μV (negligible) 0.0°C

AD521 temperature coefficient. The specified input offset tempco for the AD521L is 2μV/°C max, and the output offset tempco is 75μV/°C max (7.5μV/°C, referred to the input), for a total of $9.5\mu V/°C$ R.T.I. $9.5\mu V/°C \times 15° = 143\mu V$ 0.14°C

AD521 bias-current tempco. The maximum bias-current change is $500pA/°C \times 30°$ (range) = 15nA. The equivalent offset-voltage change is $15nA \times 1k\Omega = 15\mu V$ 0.02°C

AD521 gain tempco. The circuit will be calibrated for correct output at 100°C by trimming of the gain of the AD521 at a 25°C ambient temperature. Variation of gain will cause output errors. The specified gain tempco at a gain of 10 for the AD521L is 3.5ppm/°C typical. If max is arbitrarily assumed to be ten times worse, and the resistors contribute 15ppm/°C additional, the maximum error will be $50 \times 10^{-6}/°C \times 100° \times 15° = 0.075°$ 0.075°C

AD521 nonlinearity. The 0.1% nonlinearity specification applies for a ±9V output swing; for a 1V full-scale swing, it may be reasonable to expect a tenfold improvement, or a 1mV linearity error, equivalent to 0.1°C 0.1°C

Total error (worst case) 0.84°C

This means that, once the circuit has been calibrated at 0°C and 100°C (25°C ambient), the maximum error at any combination of measured and ambient temperatures can reasonably be expected to be less than 1°C.

If the summation were root-sum-of-squares, instead of worst-case, the error would come to less than 0.4°. This suggests that the design is quite conservative, since the probability of worst-case error is low; also (with some risk), it suggests that if an AD590M were used in the same design, temperature could be measured to within 0.25°C over the range. Naturally, every precaution should be taken to avoid additional errors attributable to either Murphy's or Natural Law. Aside from errors attributable to ambient temperature variations, this simple interface will require some form of protection from extraneous signals. Shielding and grounding should follow the practice suggested earlier in this book. In addition, capacitance across R1 will help reduce the effects of any ac currents induced in the twisted pair. Power supplies must be chosen to minimize error due to sensitivity of any of the elements to power-supply voltage changes, and bypassed to minimize coupling of interference through the power-supply leads.

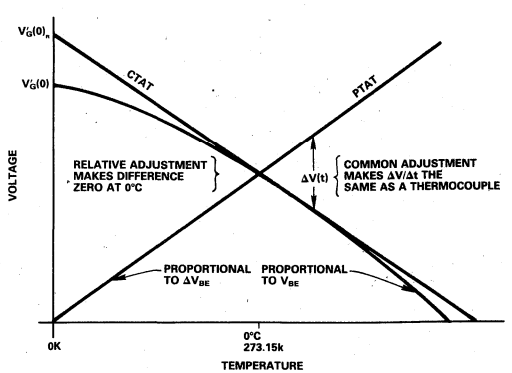
MONOLITHIC THERMOCOUPLE AMPLIFIER WITH COLD JUNCTION COMPENSATION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice-point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD596 is a low cost instrumentation amplifier and thermocouple cold junction compensator for set-point control applications. The AD596 is packaged in a rugged hermetic 10 pin TO-100 metal can and its cold junction compensation circuit is trimmed so that it will remain accurate over a wide ambient temperature range, internal architecture.

It is commonly known that the characteristics of bipolar junction transistors are temperature sensitive, and it is a usual object of linear design to suppress this sensitivity. In the case of the AD594/AD595, however, certain well behaved and repeatable temperature dependent parameters are exploited to produce the cold junction compensation voltage. When two transistors are operated at different emitter current densities, the difference in their base-emitter voltages will be *proportional to absolute temperature* or PTAT. The base-emitter voltages of a single transistor falls with rising temperature in a way that can be extrapolated to a known voltage at absolute zero. This voltage *complements* a PTAT voltage with respect to the known bandgap voltage and is referred to as CTAT.

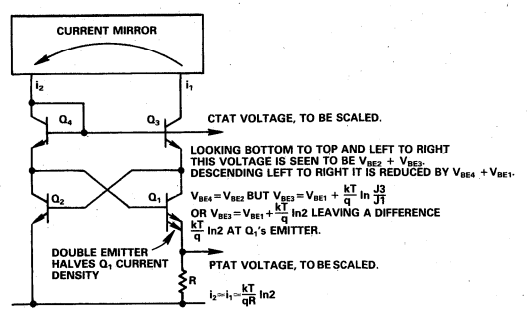
Although these two voltages are predictably related to absolute temperature, their difference can be related to Celsius temperature as shown here.



Ice-Point Compensation from the Difference of a PTAT and a CTAT Voltage

Two temperature sensitive voltages can be derived from the transistor base-emitter characteristics which can be scaled so that their difference approximates the output of an ice referenced thermocouple measuring the IC temperature. This difference is zero at zero Celsius and increases more-or-less linearly with temperature. These voltages are produced by four transistors in the AD594/AD595. A current mirror is used to force a pair of series connected transistors (Q_2, Q_4, in the figure below) to operate at the same current as another series connected pair (Q_1, Q_3). Three of these transistors are the same size and therefore operate at equal current densities. Consequently, they have the same base-emitter voltage. The fourth transistor is larger than the others so that at the same current it operates at lower current density. This implies that it has a lower base-emitter voltage. The base-emitter junctions of the four transistors connect in a loop which is completed by a resistor. Two of the voltages are connected to subtract from the others so that the net voltage across the resistor is just the difference between the base-emitter voltage of the differently sized transistors.

As noted before, this voltage will be PTAT and is scaled to the proper magnitude by a thin film network in the AD594/AD595. It is also possible to extract the sum of the two base-emitter voltages from this loop. This sum is CTAT and when properly scaled makes up the other temperature sensitive voltage for the Ice-Point Compensation.



A Cross-Connected Transistor Quad Provides CTAT Voltage in the Form of $2V_{BE}$S and PTAT Voltage from the Difference of V_{BE}S

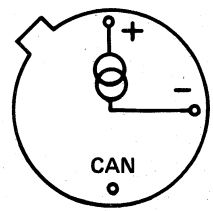
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case

AD590 FUNCTIONAL BLOCK DIAGRAM



TO-52
BOTTOM VIEW

8

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

SPECIFICATIONS (@ +25°C and V_S = 5V unless otherwise noted)

Model	AD590I			AD590J			AD590K			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS										
Forward Voltage (E+ to E−)			+44			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300			+300	°C
POWER SUPPLY										
Operating Voltage Range	+4		+30	+4		+30	+4		+30	Volts
OUTPUT										
Nominal Current Output @ +25°C (298.2K)		298.2			298.2			298.2		µA
Nominal Temperature Coefficient		1			1			1		µA/K
Calibration Error @ +25°C			**±10**			**±5.0**			**±2.5**	°C
Absolute Error (over rated performance temperature range)										
Without External Calibration Adjustment			**±20**			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±5.8**			**±3.0**			**±2.0**	°C
Nonlinearity			**±3.0**			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1			±0.1	°C
Current Noise		40			40			40		pA/$\sqrt{\text{Hz}}$
Power Supply Rejection										
+4V≤V_S≤+5V		0.5			0.5			0.5		µA/V
+5V≤V_S≤+15V		0.2			0.2			0.2		µA/V
+15V≤V_S≤+30V		0.1			0.1			0.1		µA/V
Case Isolation to Either Lead		10^{10}			10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100			100		pF
Electrical Turn-On Time		20			20			20		µs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10			10		pA
PACKAGE OPTION[5]										
"H" Package: TO-52		AD590IH			AD590JH			AD590KH		
"F" Package: Flat Pack (F2A)		AD590IF			AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.

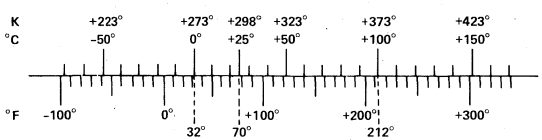
[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[4]Leakage current doubles every 10°C.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

Model	AD590L Min	AD590L Typ	AD590L Max	AD590M Min	AD590M Typ	AD590M Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±1.0**			**±0.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±3.0**			**±1.7**	°C
With +25°C Calibration Error Set to Zero			**±1.6**			**±1.0**	°C
Nonlinearity			**±0.4**			**±0.3**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{\text{Hz}}$
Power Supply Rejection							
+4V≤V_S≤+5V		0.5			0.5		μA/V
+5V≤V_S≤+15V		0.2			0.2		μA/V
+15V≤V_S≤+30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
"H" Package: TO-52		AD590LH			AD590MH		
"F" Package: Flat Pack (F2A)		AD590LF			AD590MF		

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

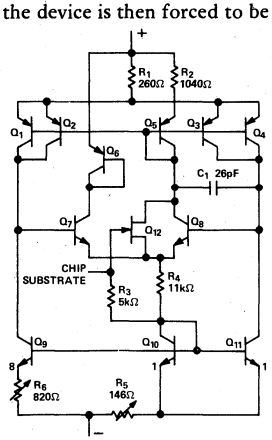


Figure 1. Schematic Diagram

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

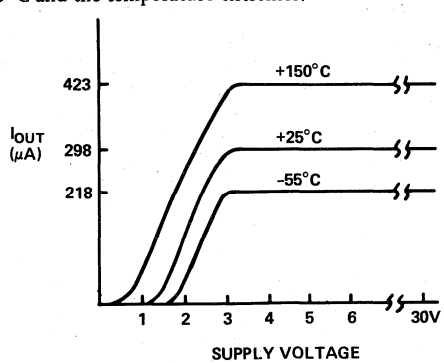


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

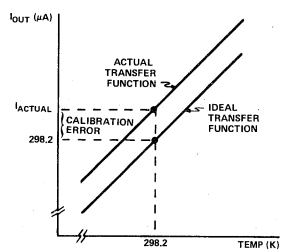


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

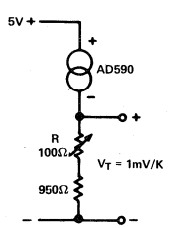


Figure 4. One Temperature Trim

[1] T(°C) = T(K) -273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

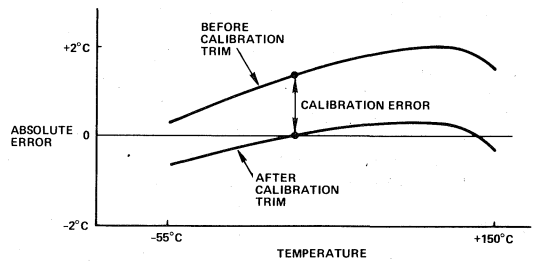


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

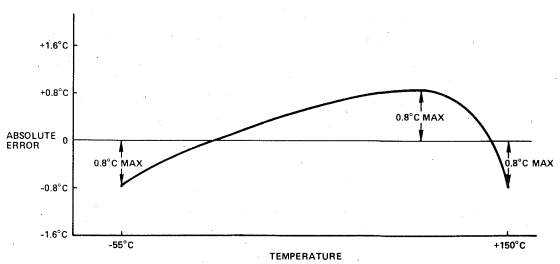


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

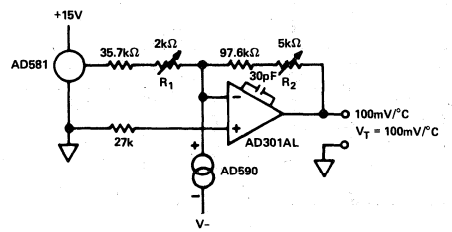


Figure 7A. Two Temperature Trim

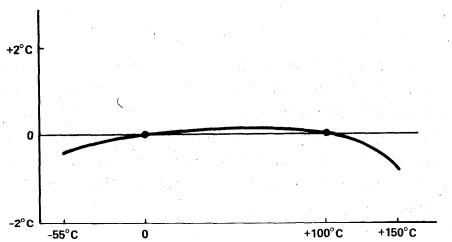


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

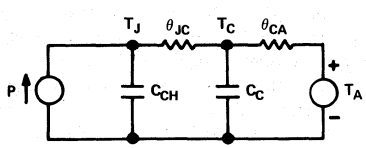


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P\,(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

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MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	—	5.0	—
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	—	108	—
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.

[2] Air velocity ≅ 9ft/sec.

[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

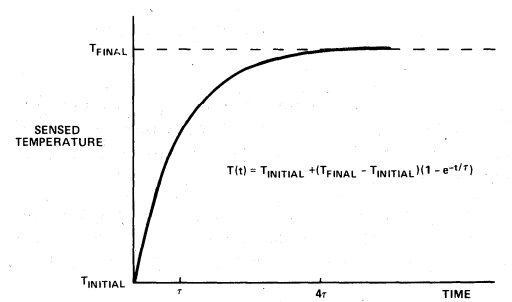


Figure 9. Time Response Curve

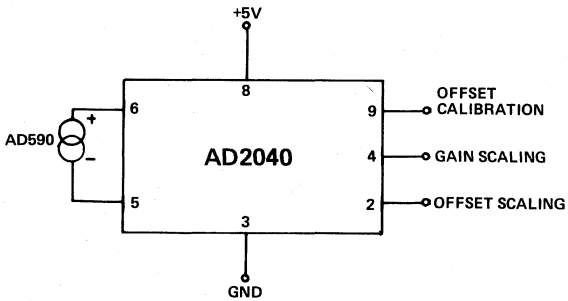


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

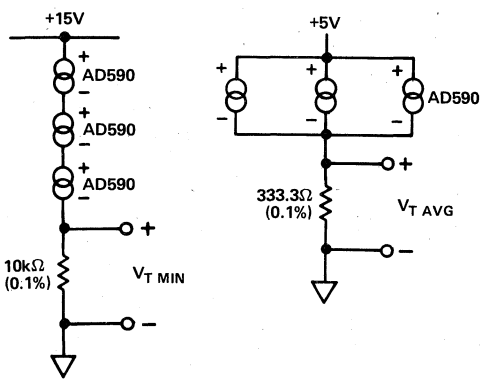


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate

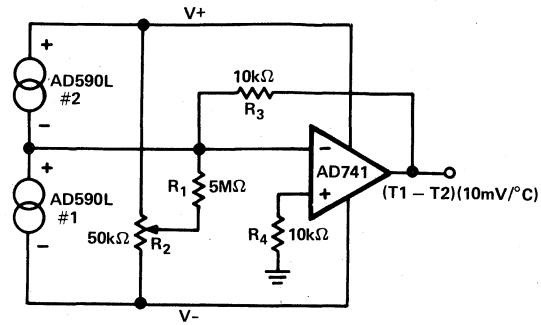


Figure 12. Differential Measurements

a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

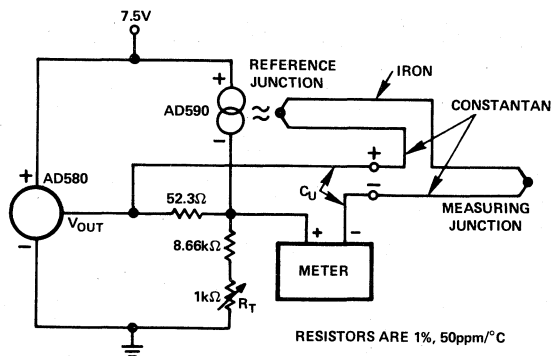


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

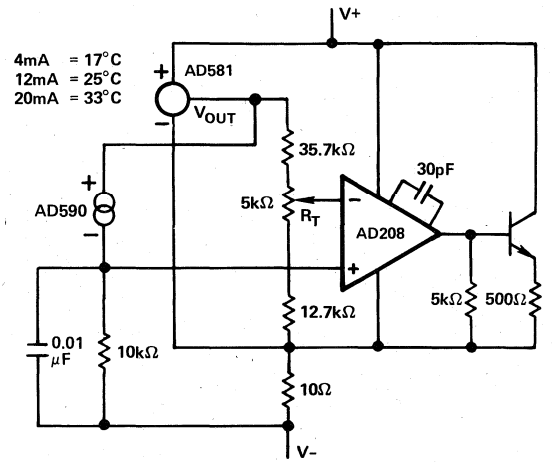


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

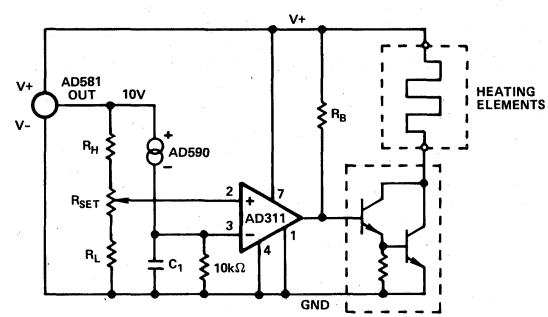


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

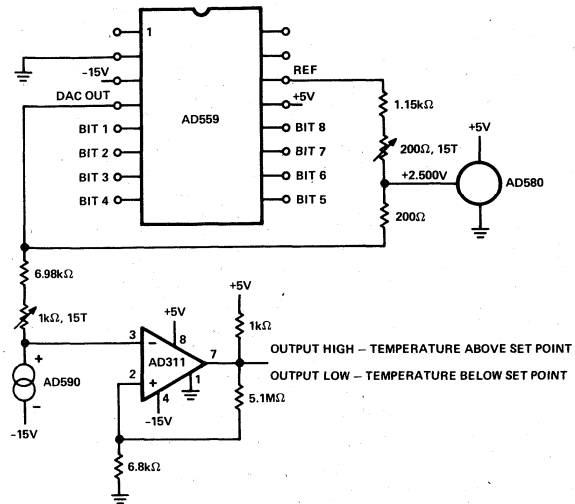


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

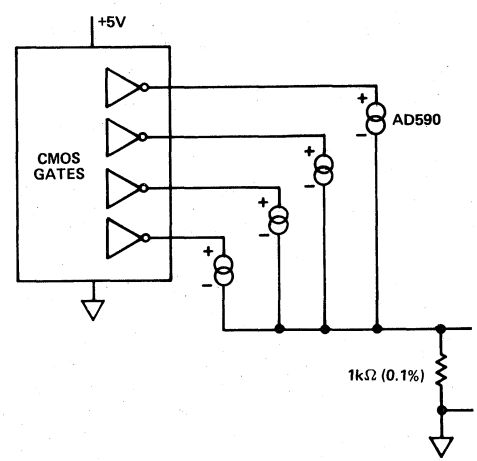


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

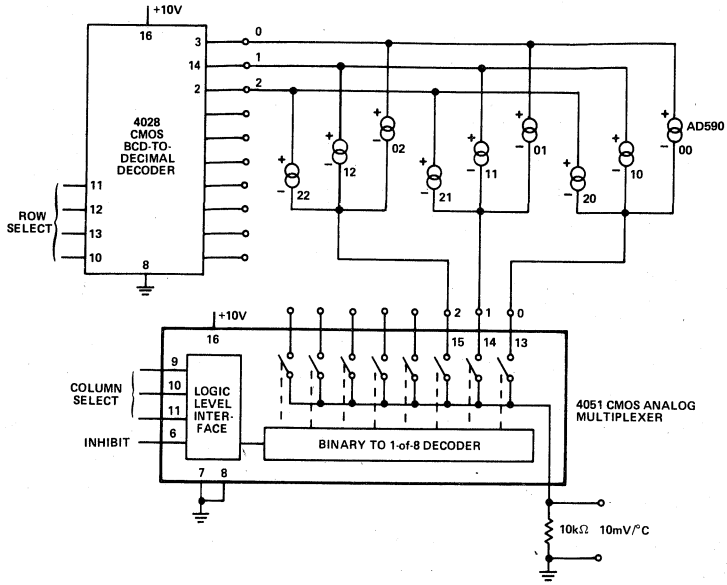


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

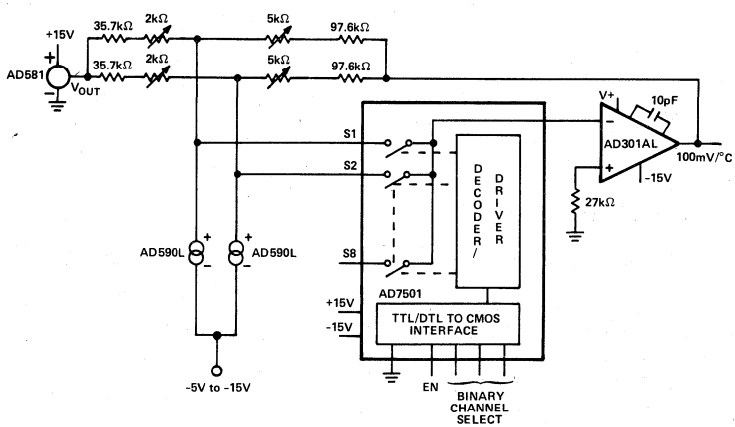


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of −55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

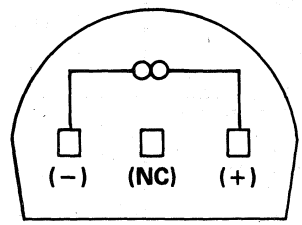
ANALOG DEVICES

Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

AD592 FUNCTIONAL BLOCK DIAGRAM



TO-92
BOTTOM VIEW

8

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

*Covered by Patent No. 4,123,698

The AD592 is available in three performance grades; the AD592AN, AD592BNand AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.

SPECIFICATIONS (typical @ 25°C, V_S = 5V, unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	**2.5**		0.7	**1.0**		0.3	**0.5**	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	**3.5**		0.9	**2.0**		0.5	**1.0**	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			**44**			**44**			**44**	V
Reverse Voltage (− to +)			**20**			**20**			**20**	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			**0.5**			**0.5**			**0.5**	C/V
+5V<V_S<+15V			**0.2**			**0.2**			**0.2**	C/V
+15V<V_S<+30V			**0.1**			**0.1**			**0.1**	C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only.

[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

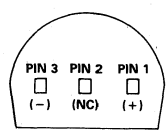
[5]Operation @125°C, error over time is noncummulative.

[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

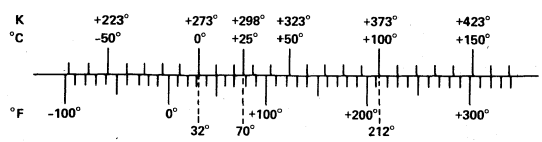
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CONNECTING DIAGRAM (BOTTOM VIEW)



*PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED

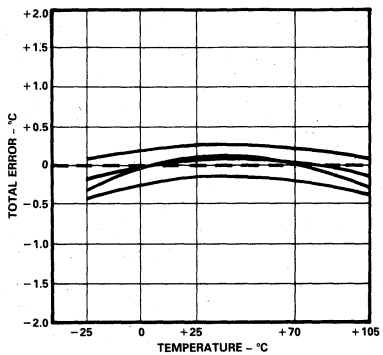


TEMPERATURE SCALE CONVERSION EQUATIONS

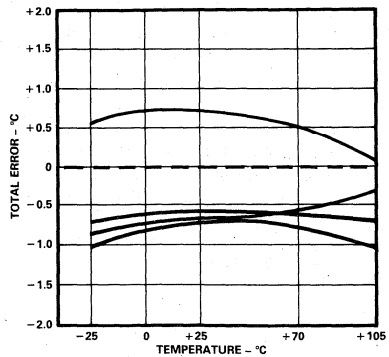
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

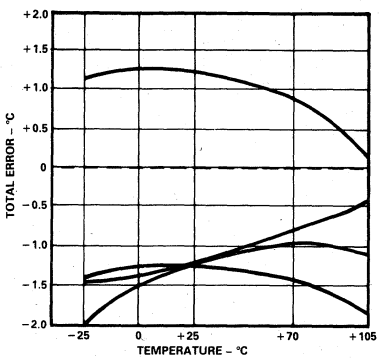
Typical @ V_S = +5V



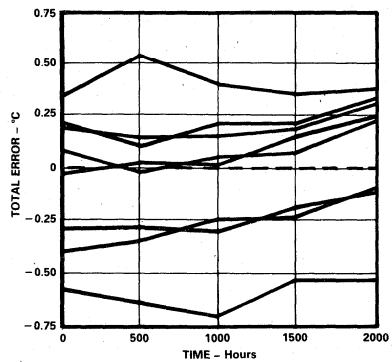
AD592CN Accuracy Over Temperature



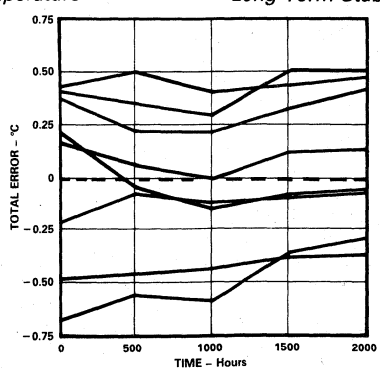
AD592BN Accuracy Over Temperature



AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity



Long-Term Stability @ 125°C

AD592 ORDERING GUIDE

Model	Package[1]	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C
AD592CN	TO-92	0.5°C	1.0°C	0.35°C
AD592BN	TO-92	1.0°C	2.0°C	0.4°C
AD592AN	TO-92	2.5°C	3.5°C	0.5°C

NOTE
[1]See Section 19 for package outline information.

THEORY OF OPERATION

The AD592 uses a fundamental property of silicon transistors to realize its temperature proportional output. If two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron are constant, the resulting voltage is directly Proportional To Absolute Temperature (PTAT). In the AD592 this difference voltage is converted to a PTAT current by low temperature coefficient thin film resistors. This PTAT current is then used to force the total output current to be proportional to degrees Kelvin. The result is a current source with an output equal to a scale factor times the temperature (K) of the sensor. A typical V-I plot of the circuit at +25°C and the temperature extremes is shown in Figure 1.

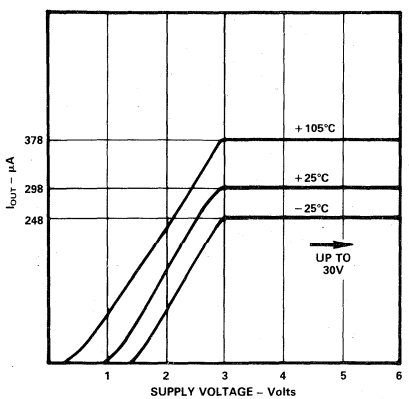


Figure 1. V–I Characteristics

Factory trimming of the scale factor to 1µA/K is accomplished at the wafer level by adjusting the AD592's temperature reading so it corresponds to the actual temperature. During laser trimming the IC is at a temperature within a few degrees of 25°C and is powered by a 5V supply. The device is then packaged and automatically temperature tested to specification.

FACTORS AFFECTING AD592 SYSTEM PRECISION

The accuracy limits given on the Specifications page for the AD592 makes it easy to apply in a variety of diverse applications. To calculate a total error budget in a given system it is important to correctly interpret the accuracy specifications, nonlinearity errors, the response of the circuit to supply voltage variations and the effect of the surrounding thermal environment. As with other electronic designs external component selection will have a major effect on accuracy.

CALIBRATION ERROR, ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Three primary limits of error are given for the AD592 such that the correct grade for any given application can easily be chosen for the overall level of accuracy required. They are the calibration accuracy at 25°C, and the error over temperature from 0 to 70°C and −25°C to +105°C. These specifications correspond to the actual error the user would see if the current output of a AD592 were converted to a voltage with a precision resistor. Note that the maximum error at room temperature, over the commercial IC temperature range, or an extended range including the boiling point of water, can be directly read from the Specifications Table. All three error limits are a combination of initial error, scale factor variation and nonlinearity deviation from the ideal 1µA/K output. Figure 2 graphically depicts the guaranteed limits of accuracy for an AD592CN.

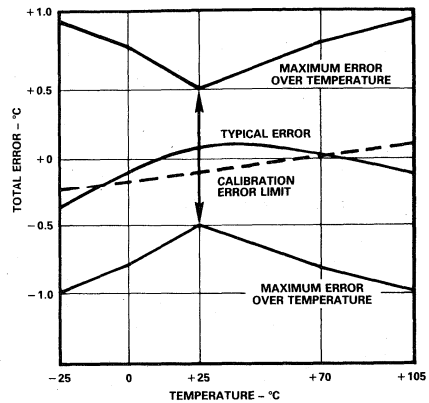


Figure 2. Error Specifications (AD592CN)

The AD592 has a highly linear output in comparison to older technology sensors (i.e., thermistors, RTDs and thermocouples), thus a nonlinearity error specification is separated from the absolute accuracy given over temperature. As a maximum deviation from a best-fit straight line this specification represents the only error which cannot be trimmed out. Figure 3 is a plot of typical AD592CN nonlinearity over the full rated temperature range.

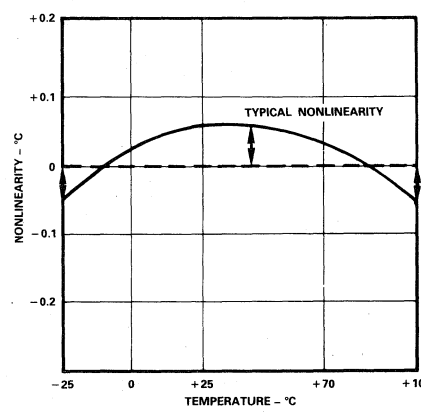


Figure 3. Nonlinearity Error (AD592CN)

TRIMMING FOR HIGHER ACCURACY

Calibration error at 25°C can be removed with a single temperature trim. Figure 4 shows how to adjust the AD592's scale factor in the basic voltage output circuit.

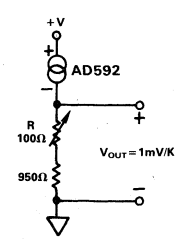


Figure 4. Basic Voltage Output (Single Temperature Trim)

To trim the circuit the temperature must be measured by a reference sensor and the value of R should be adjusted so the output (V_{OUT}) corresponds to 1mV/K. Note that the trim procedure should be implemented as close as possible to the temperature highest accuracy is desired for. In most applications if a single temperature trim is desired it can be implemented where the AD592 current-to-output voltage conversion takes place (e.g., output resistor, offset to an op amp). Figure 5 illustrates the effect on total error when using this technique.

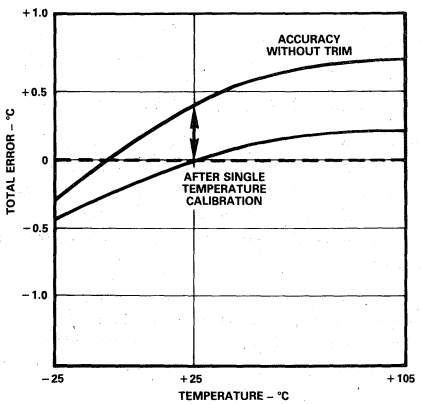


Figure 5. Effect of Scale Factor Trim on Accuracy

If greater accuracy is desired, initial calibration and scale factor errors can be removed by using the AD592 in the circuit of Figure 6.

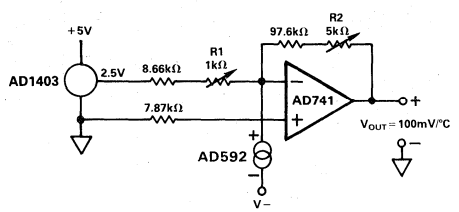


Figure 6. Two Temperature Trim Circuit

With the transducer at 0°C adjustment of R1 for a 0V output nulls the initial calibration error and shifts the output from K to °C. Tweaking the gain of the circuit at an elevated temperature by adjusting R2 trims out scale factor error. The only error remaining over the temperature range being trimmed for is nonlinearity. A typical plot of two trim accuracy is given in Figure 7.

SUPPLY VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection characteristics of the AD592 minimizes errors due to voltage irregularity, ripple and noise. If a supply is used other than 5V (used in factory trimming), the power supply error can be removed with a single temperature trim. The PTAT nature of the AD592 will remain unchanged. The general insensitivity of the output allows the use of lower cost unregulated supplies and means that a series resistance of several hundred ohms (e.g., CMOS multiplexer, meter coil resistance) will not degrade the overall performance.

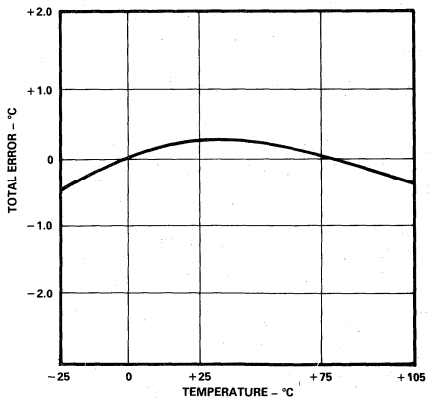


Figure 7. Typical Two Trim Accuracy

The thermal environment in which the AD592 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption level of the circuit and the thermal resistance between the chip and the ambient environment (θ_{JA}). Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. In typical free air applications at 25°C with a 5V supply the magnitude of the error is 0.2°C or less. A common clip-on heat sink will reduce the error by 25% or more in critical high temperature, large supply voltage situations.

Medium	**θ_{JA} (°C/watt)**	**τ (sec)***
Still Air		
Without Heat Sink	175	60
With Heat Sink	130	55
Moving Air		
Without Heat Sink	60	12
With Heat Sink	40	10
Fluorinert Liquid	35	5
Aluminum Block**	30	2.4

*τ is an average of five time constants (99.3% of final value). In cases where the thermal response is not a simple exponential function, the actual thermal response may be better than indicated.
**With thermal grease.

Table I. Thermal Characteristics

Response of the AD592 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 8 shows typical response time plots for several media of interest.

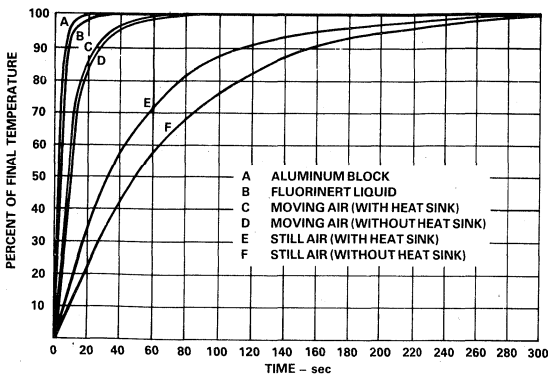


Figure 8. Thermal Response Curves

The time constant, τ, is dependent on θ_{JA} and the thermal capacities of the chip and the package. Table I lists the effective τ (time to reach 63.2% of the final value) for several different media. Copper printed circuit board connections where neglected in the analysis, however, they will sink or conduct heat directly through the AD592's solder dipped Kovar leads. When faster response is required a thermally conductive grease or glue between the AD592 and the surface temperature being measured should be used. In free air applications a clip-on heat sink will decrease output stabilization time by 10–20%.

MOUNTING CONSIDERATIONS

If the AD592 is thermally attached and properly protected, it can be used in any temperature measuring situation where the maximum range of temperatures encountered is between −25°C and +105°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be safeguarded against when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended under typical mounting conditions. In wet or corrosive environments any electrically isolated metal or ceramic well can be used to shield the AD592. Condensation at cold temperatures can cause leakage current related errors and should be avoided by sealing the device in nonconductive epoxy paint or dips.

APPLICATIONS

Connecting several AD592 devices in parallel adds the currents through them and produces a reading proportional to the average temperature. Series AD592s will indicate the lowest temperature

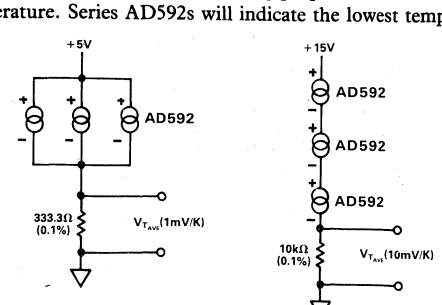


Figure 9. Average and Minimum Temperature Connections

because the coldest device limits the series current flowing through the sensors. Both of these circuits are depicted in Figure 9.

The circuit of Figure 10 demonstrates a method in which a voltage output can be derived in a differential temperature measurement.

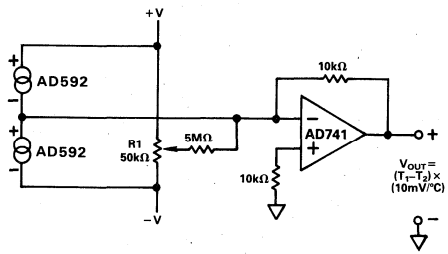


Figure 10. Differential Measurements

R1 can be used to trim out the inherent offset between the two devices. By increasing the gain resistor (10kΩ) temperature measurements can be made with higher resolution. If the magnitude of V+ and V− is not the same, the difference in power consumption between the two devices can cause a differential self-heating error.

Cold junction compensation (CJC) used in thermocouple signal conditioning can be implemented using an AD592 in the circuit configuration of Figure 11. Expensive simulated ice baths or hard to trim, inaccurate bridge circuits are no longer required.

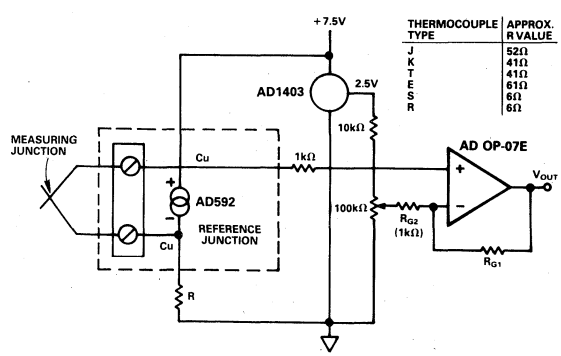


Figure 11. Thermocouple Cold Junction Compensation

The circuit shown can be optimized for any ambient temperature range or thermocouple type by simply selecting the correct value for the scaling resistor – R. The AD592 output (1μA/K) times R should approximate the line best fit to the thermocouple curve (slope in V/°C) over the most likely ambient temperature range. Additionally, the output sensitivity can be chosen by selecting the resistors R_{G1} and R_{G2} for the desired noninverting gain. The offset adjustment shown simply references the AD592 to °C. Note that the TC's of the reference and the resistors are the primary contributors to error. Temperature rejection of 40 to 1 can be easily achieved using the above technique.

Although the AD592 offers a noise immune current output, it is not compatible with process control/industrial automation current loop standards. Figure 12 is an example of a temperature to 4-20mA transmitter for use with 40V, 1kΩ systems.

In this circuit the 1μA/K output of the AD592 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. Rt is trimmed for proper reading at an

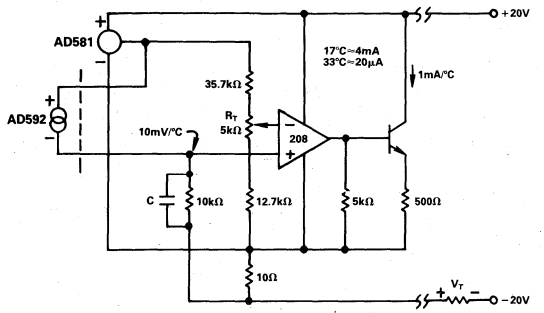


Figure 12. Temperature to 4–20mA Current Transmitter

intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD592 may be chosen.

Reading temperature with an AD592 in a microprocessor based system can be implemented with the circuit shown in Figure 13.

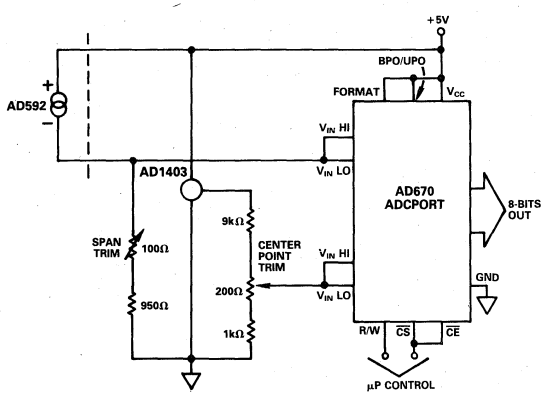


Figure 13. Temperature to Digital Output

By using a differential input A/D converter and choosing the current to voltage conversion resistor correctly any range of temperatures (up to the 130°C span the AD592 is rated for) centered at any point can be measured using a minimal number of components. In this configuration the system will resolve up to 1°C.

A variable temperature controlling thermostat can easily be built using the AD592 in the circuit of Figure 14.

R_{HIGH} and R_{LOW} determine the limits of temperature controlled by the potentiometer R_{SET}. The circuit shown operates over the full temperature range (−25°C to +105°C) the AD592 is rated for. The reference maintains a constant set point voltage and insures that approximately 7V appears across the sensor. If it is necessary to guardband for extraneous noise hysteresis can be added by tying a resistor from the output to the ungrounded end of R_{LOW}.

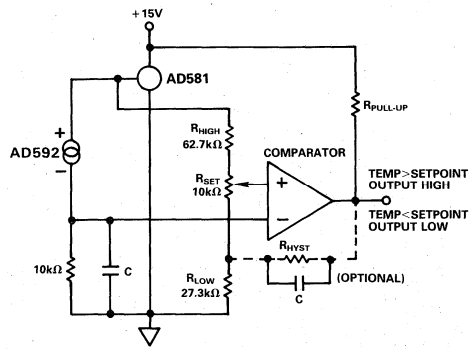


Figure 14. Variable Temperature Thermostat

Multiple remote temperatures can be measured using several AD592s with a CMOS multiplexer or a series of 5V logic gates because of the device's current-mode output and supply-voltage compliance range. The on-resistance of a FET switch or output impedance of a gate will not effect the accuracy, as long as 4V is maintained across the transducer. MUXs and logic driving circuits should be chosen to minimize leakage current related errors. Figure 15 illustrates a locally controlled MUX switching the signal current from several remote AD592s. CMOS or TTL gates can also be used to switch the AD592 supply voltages, with the multiplexed signal being transmitted over a single twisted pair to the load.

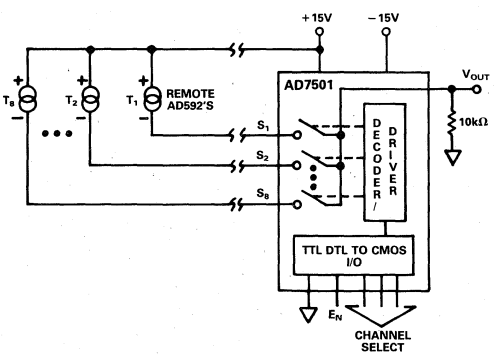


Figure 15. Remote Temperature Multiplexing

To minimize the number of MUXs required when a large number of AD592s are being used, the circuit can be configured in a matrix. That is, a decoder can be used to switch the supply voltage to a column of AD592s while a MUX is used to control which row of sensors are being measured. The maximum number of AD592s which can be used is the product of the number of channels of the decoder and MUX.

An example circuit controlling 80 AD592s is shown in Figure 16. A 7-bit digital word is all that is required to select one of the sensors. The enable input of the multiplexer turns all the sensors off for minimum dissipation while idling.

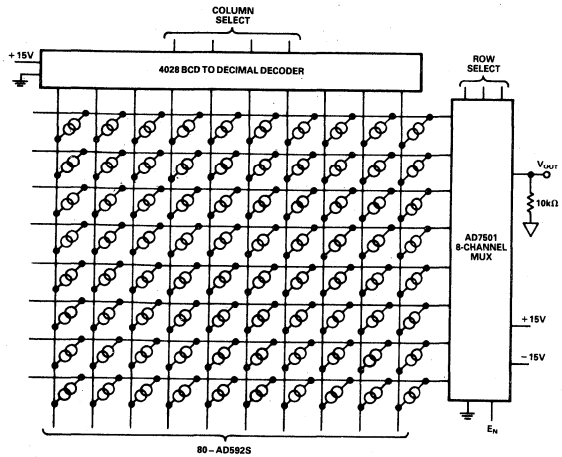
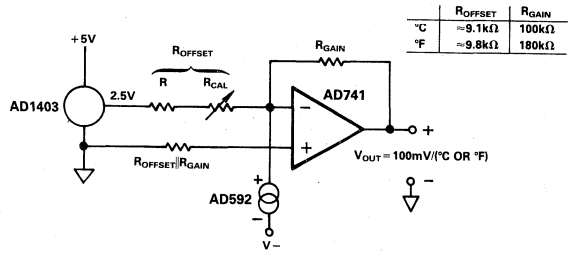


Figure 16. Matrix Multiplexer

To convert the AD592 output to °C or °F a single inexpensive reference and op amp can be used as shown in Figure 17. Although this circuit is similar to the two temperature trim circuit shown in Figure 6, two important differences exist. First, the gain resistor is fixed alleviating the need for an elevated temperature trim. Acceptable accuracy can be achieved by choosing an inexpensive resistor with the correct tolerance. Second, the AD592 calibration error can be trimmed out at a known convenient temperature (i.e., room temperature) with a single pot adjustment. This step is independent of the gain selection.



	R_{OFFSET}	R_{GAIN}
°C	≈9.1kΩ	100kΩ
°F	≈9.8kΩ	180kΩ

Figure 17. Celsius or Fahrenheit Thermometer

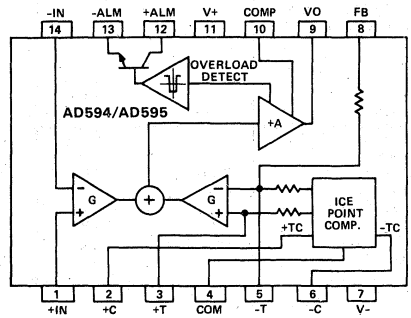
Monolithic Thermocouple Amplifier with Cold Junction Compensation

AD594*/AD595*

FEATURES

- **Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples**
- **Can Be Used with Type T Thermocouple Inputs**
- **Low Impedance Voltage Output: 10mV/°C**
- **Built-In Ice Point Compensation**
- **Wide Power Supply Range: +5V to ±15V**
- **Low Power: <1mW typical**
- **Thermocouple Failure Alarm**
- **Laser Wafer Trimmed to 1°C Calibration Accuracy**
- **Set-Point Mode Operation**
- **Self-Contained Celsius Thermometer Operation**
- **High Impedance Differential Input**

AD594/AD595 BLOCK DIAGRAM



8

PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a Thermocouple Failure Alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in a 14-pin, hermetically sealed, side-brazed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

*Protected by U.S. Patent No. 4,029,974.

SPECIFICATIONS (@ +25°C and V_S = 5V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A			AD594C			AD595A			AD595C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0 to +50°C)													
Calibration Error at +25°C[1]			±3			±1			±3			±1	°C
Stability vs. Temperature[2]			±0.05			±0.025			±0.05			±0.025	°C/°C
Gain Error			±1.5			±0.75			±1.5			±0.75	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		193.4			193.4			247.3			247.3		
Input Offset Voltage	(Temperature in °C) × 51.70μV/°C			(Temperature in °C) × 51.70μV/°C			(Temperature in °C) × 44.44μV/°C			(Temperature in °C) × 44.44μV/°C			μV
Input Bias Current		0.1			0.1			0.1			0.1		μA
Differential Input Range	−10		+50				−10		+50	−10		+50	mV
Common Mode Range	**−4 to ($-V_S-0.15$)**		**$+V_S$**	**−4 to ($-V_S-0.15$)**		**$+V_S$**	**−4 to ($-V_S-0.15$)**		**$+V_S$**	**−4 to ($-V_S-0.15$)**		**$+V_S$**	Volts
Common Mode Sensitivity–RTO			**10**			**10**			**10**			**10**	mV/V
Power Supply Sensitivity–RTO			**10**			**10**			**10**			**10**	mV/V
Output Voltage Range													
Dual Supplies	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	Volts
Single Supply	0		$+V_S-2$	0		$+V_S-2$	0		$+V_S+2$	0		$+V_S-2$	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2mA		0.3			0.3			0.3			0.3		Volts
Leakage Current			±1			±1			±1			±1	μA max
Operating Voltage at −ALM			$+V_S-4$			$+V_S-4$			$+V_S-4$			$+V_S-4$	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance	$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			Volts
Operating	$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	μA
$-V_S$		100			100			100			100		μA
PACKAGE OPTION[5] (D14A)	AD594AD			AD594CD			AD595AD			AD595CD			

NOTES

[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7μV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7mV at 0°C.

[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.

[3]Pin 8 shorted to pin 9.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Model	Maximum Cal. Error
AD594AD	±3°C
AD594CD	±1°C
AD595AD	±3°C
AD595CD	±1°C

Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV	Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV
− 200	− 7.890	−1523	− 5.891	−1454	500	27.388	5300	20.640	5107
− 180	− 7.402	−1428	− 5.550	−1370	520	28.511	5517	21.493	5318
− 160	− 6.821	−1316	− 5.141	−1269	540	29.642	5736	22.346	5529
− 140	− 6.159	−1188	− 4.669	−1152	560	30.782	5956	23.198	5740
− 120	− 5.426	−1046	− 4.138	−1021	580	31.933	6179	24.050	5950
− 100	− 4.632	− 893	− 3.553	− 876	600	33.096	6404	24.902	6161
− 80	− 3.785	− 729	− 2.920	− 719	620	34.273	6632	25.751	6371
− 60	− 2.892	− 556	− 2.243	− 552	640	35.464	6862	26.599	6581
− 40	− 1.960	− 376	− 1.527	− 375	660	36.671	7095	27.445	6790
− 20	− .995	− 189	− .777	− 189	680	37.893	7332	28.288	6998
− 10	− .501	− 94	− .392	− 94	700	39.130	7571	28.128	7206
0	0	3.1	0	2.7	720	40.382	7813	29.965	7413
10	.507	101	.397	101	740	41.647	8058	30.799	7619
20	1.019	200	.798	200	750	42.283	8181	31.214	7722
25	1.277	250	1.000	250	760	–	–	31.629	7825
30	1.536	300	1.203	300	780	–	–	32.455	8029
40	2.058	401	1.611	401	800	–	–	33.277	8232
50	2.585	503	2.022	503	820	–	–	34.095	8434
60	3.115	606	2.436	605	840	–	–	34.909	8636
80	4.186	813	3.266	810	860	–	–	35.718	8836
100	5.268	1022	4.095	1015	880	–	–	36.524	9035
120	6.359	1233	4.919	1219	900	–	–	37.325	9233
140	7.457	1445	5.733	1420	920	–	–	38.122	9430
160	8.560	1659	6.539	1620	940	–	–	38.915	9626
180	9.667	1873	7.338	1817	960	–	–	39.703	9821
200	10.777	2087	8.137	2015	980	–	–	40.488	10015
220	11.887	2302	8.938	2213	1000	–	–	41.269	10209
240	12.998	2517	9.745	2413	1020	–	–	42.045	10400
260	14.108	2732	10.560	2614	1040	–	–	42.817	10591
280	15.217	2946	11.381	2817	1060	–	–	43.585	10781
300	16.325	3160	12.207	3022	1080	–	–	44.349	10970
320	17.432	3374	13.039	3327	1100	–	–	45.108	11158
340	18.537	3588	13.874	3434	1120	–	–	45.863	11345
360	19.640	3801	14.712	3641	1140	–	–	46.612	11530
380	20.743	4015	15.552	3849	1160	–	–	47.356	11714
400	21.846	4228	16.395	4057	1180	–	–	48.095	11897
420	22.949	4441	17.241	4266	1200	–	–	48.828	12078
440	24.054	4655	18.088	4476	1220	–	–	49.555	12258
460	25.161	4869	18.938	4686	1240	–	–	50.276	12436
480	26.272	5084	19.788	4896	1250	–	–	50.633	12524

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +25°C, V_S = −5V, +15V)

INTERPRETING AD594/AD595 OUTPUT VOLTAGES

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD594/AD595 is gain trimmed to match the transfer characteristic of J and K type thermocouples at 25°C. For a type J output in this temperature range the TC is 51.70μV/°C, while for a type K it is 40.44μV/°C. The resulting gain for the AD594 is 193.4 (10mV/°C divided by 51.7μV/°C) and for the AD595 is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 16μV for the AD594 and 11μV for the AD595. This offset arises because the AD594/AD595 is trimmed for a 250mV output while applying a 25°C thermocouple input.

Because a thermocouple output voltage is nonlinear with respect to temperature, and the AD594/AD595 linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD594 output = (Type J Voltage + 16μV) × 193.4

AD595 output = (Type K Voltage + 11μV) × 247.3

or conversely:

Type J voltage = (AD594 output / 193.4) − 16μV

Type K voltage = (AD595 output / 247.3) − 11μV

Table I above lists the ideal AD594/AD595 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and ANSI thermocouple voltage tables referred to zero degrees Celsius. Due to a slight variation in alloy content between ANSI type J and DIN FE–CUNI thermocouples Table I should not be used in conjunction with European standard thermocouples. Instead the transfer function given previously and a DIN thermocouple table should be used. ANSI type K and DIN NICR–NI thermocouples are composed of identical alloys and exhibit similar behavior. The upper temperature limits in Table I are those recommended for type J and type K thermocouples by the majority of vendors.

SINGLE AND DUAL SUPPLY CONNECTIONS

The AD594/AD595 is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 1 will provide a direct output from a type J thermocouple (AD594) or type K thermocouple (AD595) measuring from 0 to +300°C.

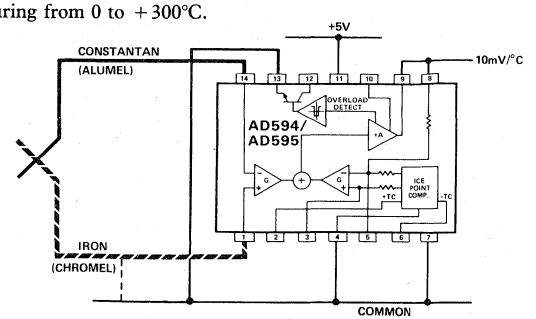


Figure 1. Basic Connection, Single Supply Operation

Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimized at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V− connection at pin 7 strapped to power and signal common at pin 4. The thermocouple wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or −V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

By using a wider ranging dual supply, as shown in Figure 2, the AD594/AD595 can be interfaced to thermocouples measuring both negative and extended positive temperatures.

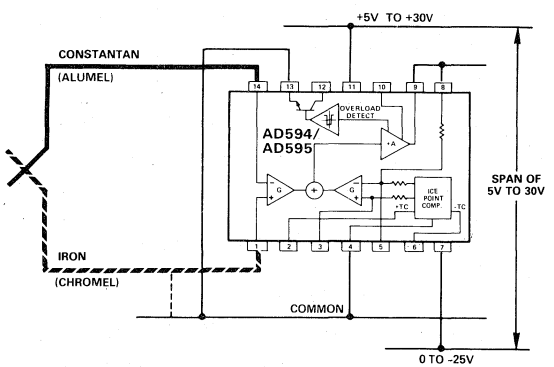


Figure 2. Dual Supply Operation

With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the 750°C temperature limit recommended for type J thermocouples (AD594) and the 1250°C for type K thermocouples (AD595).

Common-mode voltages on the thermocouple inputs must remain within the common-mode range of the AD594/AD595, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are recommended. A resistor may be needed in this connection to assure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

THERMOCOUPLE CONNECTIONS

The isothermal terminating connections of a pair of themocouple wires forms an effective reference junction. This junction must be kept at the same temperature as the AD594/AD595 for the internal cold junction compensation to be effective.

A method that provides for thermal equilibrium is the printed circuit board connection layout illustrated in Figure 3.

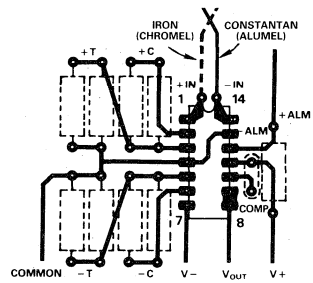


Figure 3. PCB Connections

Here the AD594/AD595 package temperature and circuit board are thermally contacted in the copper printed circuit board tracks under pins 1 and 14. The reference junction is now composed of a copper-constantan (or copper-alumel) connection and copper-iron (or copper-chromel) connection, both of which are at the same temperature as the AD594/AD595.

The printed circuit board layout shown also provides for placement of optional alarm load resistors, recalibration resistors and a compensation capacitor to limit bandwidth.

To ensure secure bonding the thermocouple wire should be cleaned to remove oxidation prior to soldering. Noncorrosive rosin flux is effective with iron, constantan, chromel and alumel and the following solders: 95% tin-5% antimony, 95% tin-5% silver or 90% tin-10% lead.

FUNCTIONAL DESCRIPTION

The AD594 behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in Figure 4.

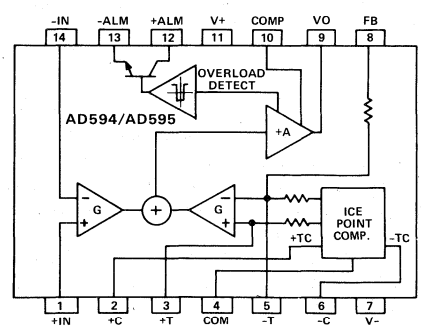


Figure 4. AD594/AD595 Block Diagram

In normal operation the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are amplified by gain G of the differential amplifier and are then further amplified by gain A in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes

the feedback to be driven to reduce this difference signal to a small value. The two differential amplifiers are made to match and have identical gains, G. As a result, the feedback signal that must be applied to the right-hand differential amplifier will precisely match the thermocouple input signal when the difference signal has been reduced to zero. The feedback network is trimmed so that the effective gain to the output, at pins 8 and 9, results in a voltage of 10mV/°C of thermocouple excitation.

In addition to the feedback signal, a cold junction compensation voltage is applied to the right-hand differential amplifier. The compensation is a differential voltage proportional to the Celsius temperature of the AD594/AD595. This signal disturbs the differential input so that the amplifier output must adjust to restore the input to equal the applied thermocouple voltage.

The compensation is applied through the gain scaling resistors so that its effect on the main output is also 10mV/°C. As a result, the compensation voltage adds to the effect of the thermocouple voltage a signal directly proportional to the difference between 0°C and the AD594/AD595 temperature. If the thermocouple reference junction is maintained at the AD594/AD595 temperature, the output of the AD594/AD595 will correspond to the reading that would have been obtained from amplification of a signal from a thermocouple referenced to an ice bath.

The AD594/AD595 also includes an input open circuit detector that switches on an alarm transistor. This transistor is actually a current-limited output buffer, but can be used up to the limit as a switch transistor for either pull-up or pull-down operation of external alarms.

The ice point compensation network has voltages available with positive and negative temperature coefficients. These voltages may be used with external resistors to modify the ice point compensation and recalibrate the AD594/AD595 as described in the next column.

The feedback resistor is separately pinned out so that its value can be padded with a series resistor, or replaced with an external resistor between pins 5 and 9. External availability of the feedback resistor allows gain to be adjusted, and also permits the AD594/AD595 to operate in a switching mode for set-point operation.

CAUTIONS:

The temperature compensation terminals (+C and −C) at pins 2 and 6 are provided to supply small calibration currents only. The AD594/AD595 may be permanently damaged if they are grounded or connected to a low impedance.

The AD594/AD595 is internally frequency compensated for feedback ratios (corresponding to normal signal gain) of 75 or more. If a lower gain is desired, additional frequency compensation should be added in the form of a 300pF capacitor from pin 10 to the output at pin 9. As shown in Figure 5 an additional 0.01μF capacitor between pins 10 and 11 is recommended.

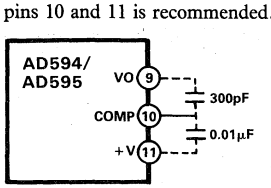


Figure 5. Low Gain Frequency Compensation

RECALIBRATION PRINCIPLES AND LIMITATIONS

The ice point compensation network of the AD594/AD595 produces a differential signal which is zero at 0°C and corresponds to the output of an ice referenced thermocouple at the temperature of the chip. The positive TC output of the circuit is proportional to Kelvin temperature and appears as a voltage at +T. It is possible to decrease this signal by loading it with a resistor from +T to COM, or increase it with a pull-up resistor from +T to the larger positive TC voltage at +C. Note that adjustments to +T should be made by measuring the voltage which tracks it at −T. To avoid destabilizing the feedback amplifier the measuring instrument should be isolated by a few thousand ohms in series with the lead connected to −T.

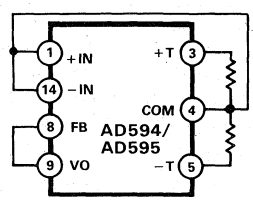


Figure 6. Decreased Sensitivity Adjustment

Changing the positive TC half of the differential output of the compensation scheme shifts the zero point away from 0°C. The zero can be restored by adjusting the current flow into the negative input of the feedback amplifier, the −T pin. A current into this terminal can be produced with a resistor between −C and −T to balance an increase in +T, or a resistor from −T to COM to offset a decrease in +T.

If the compensation is adjusted substantially to accommodate a different thermocouple type, its effect on the final output voltage will increase or decrease in proportion. To restore the nominal output to 10mV/°C the gain may be adjusted to match the new compensation and thermocouple input characteristics. When reducing the compensation the resistance between −T and COM automatically increases the gain to within 0.5% of the correct value. If a smaller gain is required, however, the nominal 47kΩ internal feedback resistor can be paralleled or replaced with an external resistor.

Fine calibration adjustments will require temperature response measurements of individual devices to assure accuracy. Major reconfigurations for other thermocouple types can be achieved without seriously compromising initial calibration accuracy, so long as the procedure is done at a fixed temperature using the factory calibration as a reference. It should be noted that intermediate recalibration conditions may require the use of a negative supply. An example using a type E thermocouple and an AD594 is given on the next page.

EXAMPLE: TYPE E RECALIBRATION – AD594/AD595

Both the AD594 and AD595 can be configured to condition the output of a type E (chromel-constantan) thermocouple. Temperature characteristics of type E thermocouples differ less from type J, than from type K, therefore the AD594 is preferred for recalibration.

While maintaining the device at a constant temperature follow the recalibration steps given here. First, measure the device temperature by tying both inputs to common (or a selected common mode potential) and connecting FB to V_O. The AD594 is now in the stand alone Celsius thermometer mode. For this example assume the ambient is 24°C and the initial output V_O is 240mV. Check the output at V_O to verify that it corresponds to the temperature of the device.

Next, measure the voltage −T at pin 5 with a high impedance DVM (capacitance should be isolated by a few thousand ohms of resistance at the measured terminals). At 24°C the −T voltage will be about 8.3mV. To adjust the compensation of an AD594 to a type E thermocouple a resistor, R1, should be connected between +T and +C, pins 2 and 3, to raise the voltage at −T by the ratio of thermocouple sensitivities. The ratio for converting a type J device to a type E characteristic is:

$$r\ (AD594) = (60.9\mu V/°C)/(51.7\mu V/°C) = 1.18$$

Thus, multiply the initial voltage measured at −T by r and experimentally determine the R1 value required to raise −T to that level. For the example the new −T voltage should be about 9.8mV. The resistance value should be approximately 1.8kΩ.

The zero differential point must now be shifted back to 0°C. This is accomplished by multiplying the original output voltage V_O by r and adjusting the measured output voltage to this value by experimentally adding a resistor, R2, between −C and −T, pins 5 and 6. The target output value in this case should be about 283mV. The resistance value of R2 should be approximately 240kΩ.

Finally, the gain must be recalibrated such that the output V_O indicates the device's temperature once again. Do this by adding a third resistor, R3, between FB and −T, pins 8 and 5. V_O should now be back to the initial 240mV reading. The resistance value of R3 should be approximately 280kΩ. The final connection diagram is shown in Figure 7. An approximate verification of the effectiveness of recalibration is to measure the differential gain to the output. For type E it should be 164.2.

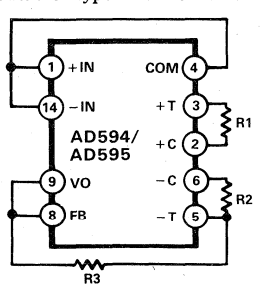


Figure 7. Type E Recalibration

When implementing a similar recalibration procedure for the AD595 the values for R1, R2, R3 and r will be approximately 650Ω, 84kΩ, 93kΩ and 1.51, respectively. Power consumption will increase by about 50% when using the AD595 with type E inputs.

Note that during this procedure it is crucial to maintain the AD594/AD595 at a stable temperature because it is used as the temperature reference. Contact with fingers or any tools not at ambient temperature will quickly produce errors. Radiational heating from a change in lighting or approach of a soldering iron must also be guarded against.

USING TYPE T THERMOCOUPLES WITH THE AD595

Because of the similarity of thermal EMFs in the 0 to 50°C range between type K and type T thermocouples, the AD595 can be directly used with both types of inputs. Within this ambient temperature range the AD595 should exhibit no more than an additional 0.2°C output calibration error when used with type T inputs. The error arises because the ice point compensator is trimmed to type K characteristics at 25°C. To calculate the AD595 output values over the recommended −200 to 350°C range for type T thermocouples, simply use the ANSI thermocouple voltages referred to 0°C and the output equation given on page 3 for the AD595. Because of the relatively large nonlinearities associated with type T thermocouples the output will deviate widely from the nominal 10mV/°C. However, cold junction compensation over the rated 0 to 50°C ambient will remain accurate.

STABILITY OVER TEMPERATURE

Each AD594/AD595 is tested for error over temperature with the measuring thermocouple at 0°C. The combined effects of cold junction compensation error, amplifier offset drift and gain error determine the stability of the AD594/AD595 output over the rated ambient temperature range. Figure 8 shows an AD594/AD595 drift error envelope. The slope of this figure has units of °C/°C.

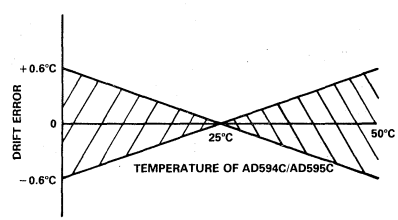


Figure 8. Drift Error vs. Temperature

THERMAL ENVIRONMENT EFFECTS

The inherent low power dissipation of the AD594/AD595 and the low thermal resistance of the package make self-heating errors almost negligible. For example, in still air the chip to ambient thermal resistance is about 80°C/watt. At the nominal dissipation of 800μW the self-heating in free air is less than 0.065°C. Submerged in fluorinert liquid (unstirred) the thermal resistance is about 40°C/watt, resulting in a self-heating error of about 0.032°C.

SET-POINT CONTROLLER

The AD594/AD595 can readily be connected as a set-point controller as shown in Figure 9.

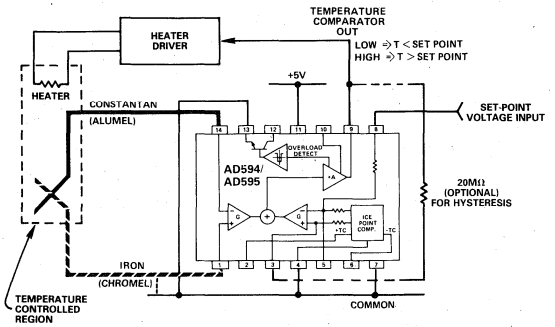


Figure 9. Set-Point Controller

The thermocouple is used to sense the unknown temperature and provide a thermal EMF to the input of the AD594/AD595. The signal is cold junction compensated, amplified to 10mV/°C and compared to an external set-point voltage applied by the user to the feedback at pin 8. Table I lists the correspondence between set-point voltage and temperature, accounting for the nonlinearity of the measurement thermocouple. If the set-point temperature range is within the operating range (−55°C to +125°C) of the AD594/AD595, the chip can be used as the transducer for the circuit by shorting the inputs together and utilizing the nominal calibration of 10mV/°C. This is the centigrade thermometer configuration as shown in Figure 13.

In operation if the set-point voltage is above the voltage corresponding to the temperature being measured the output swings low to approximately zero volts. Conversely, when the temperature rises above the set-point voltage the output switches to the positive limit of about 4 volts with a +5V supply. Figure 9 shows the set-point comparator configuration complete with a heater element driver circuit being controlled by the AD594/AD595 toggled output. Hysteresis can be introduced by injecting a current into the positive input of the feedback amplifier when the output is toggled high. With an AD594 about 200nA into the +T terminal provides 1°C of hysteresis. When using a single 5V supply with an AD594, a 20MΩ resistor from V_O to +T will supply the 200nA of current when the output is forced high (about 4V). To widen the hysteresis band decrease the resistance connected from V_O to +T.

ALARM CIRCUIT

In all applications of the AD594/AD595 the −ALM connection, pin 13, should be constrained so that it is not more positive than (V+) − 4V. This can be most easily achieved by connecting pin 13 to either common at pin 4 or V− at pin 7. For most applications that use the alarm signal, pin 13 will be grounded and the signal will be taken from +ALM on pin 12. A typical application is shown in Figure 10.

In this configuration the alarm transistor will be off in normal operation and the 20k pull up will cause the +ALM output on pin 12 to go high. If one or both of the thermocouple leads are interrupted, the +ALM pin will be driven low. As shown in Figure 10 this signal is compatible with the input of a TTL gate which can be used as a buffer and/or inverter.

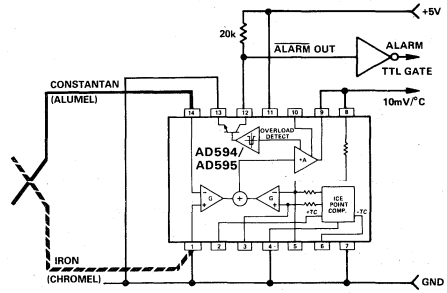


Figure 10. Using the Alarm to Drive a TTL Gate ("Grounded" Emitter Configuration)

Since the alarm is a high level output it may be used to directly drive an LED or other indicator as shown in Figure 11.

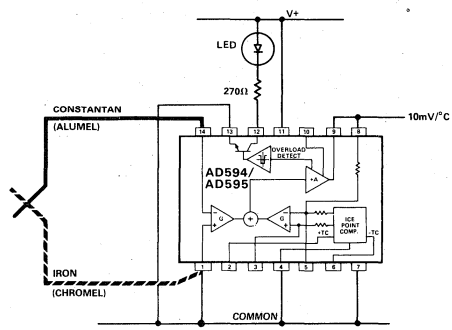


Figure 11. Alarm Directly Drives LED

A 270Ω series resistor will limit current in the LED to 10mA, but may be omitted since the alarm output transistor is current limited at about 20mA. The transistor, however, will operate in a high dissipation mode and the temperature of the circuit will rise well above ambient. Note that the cold junction compensation will be affected whenever the alarm circuit is activated. The time required for the chip to return to ambient temperature will depend on the power dissipation of the alarm circuit, the nature of the thermal path to the environment and the alarm duration.

The alarm can be used with both single and dual supplies. It can be operated above or below ground. The collector and emitter of the output transistor can be used in any normal switch configuration. As an example a negative referenced load can be driven from −ALM as shown in Figure 12.

The collector (+ALM) should not be allowed to become more positive than (V−) +36V, however, it may be permitted to be more positive than V+. The emitter voltage (−ALM) should be constrained so that it does not become more positive than 4 volts below the V+ applied to the circuit.

Additionally, the AD594/AD595 can be configured to produce an extreme upscale or downscale output in applications where an extra signal line for an alarm is inappropriate. By tying either of the thermocouple inputs to common most runaway control conditions can be automatically avoided. A +IN to common connection creates a downscale output if the thermocouple opens, while connecting −IN to common provides an upscale output.

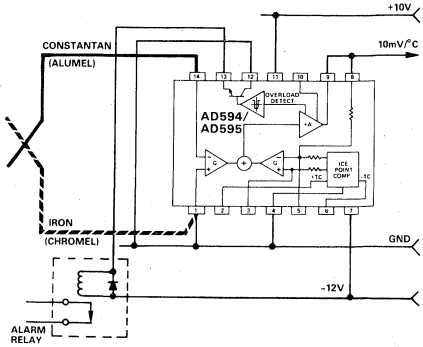


Figure 12. –ALM Driving A Negative Referenced Load

CELSIUS THERMOMETER

The AD594/AD595 may be configured as a stand-alone celsius thermometer as shown in Figure 13.

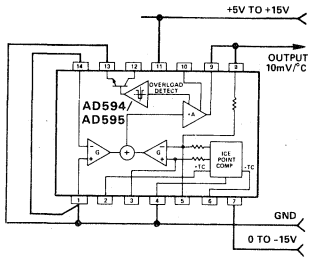


Figure 13. AD594/AD595 as a Stand-Alone Celsius Thermometer

Simply omit the thermocouple and connect the inputs (pins 1 and 14) to common. The output now will reflect the compensation voltage and hence will indicate the AD594/AD595 temperature with a scale factor of 10mV/°C. In this three terminal, voltage output, temperature sensing mode, the AD594/AD595 will operate over the full military −55°C to +125°C temperature range.

THERMOCOUPLE BASICS

Thermocouples are economical and rugged; they have reasonably good long-term stability. Because of their small size, they respond quickly and are good choices where fast response is important. They function over temperature ranges from cryogenics to jet-engine exhaust and have reasonable linearity and accuracy.

Because the number of free electrons in a piece of metal depends on both temperature and composition of the metal, two pieces of dissimilar metal in isothermal contact will exhibit a potential difference that is a repeatable function of temperature, as shown in Figure 14. The resulting voltage depends on the temperatures, T1 and T2, in a repeatable way.

Since the thermocouple is basically a differential rather than absolute measuring device, a known reference temperature is required for one of the junctions if the temperature of the other is to be inferred from the output voltage. Thermocouples made of specially selected materials have been exhaustively characterized in terms of voltage versus temperature compared to primary temperature standards. Most notably the water-ice point of 0°C is used for tables of standard thermocouple performance.

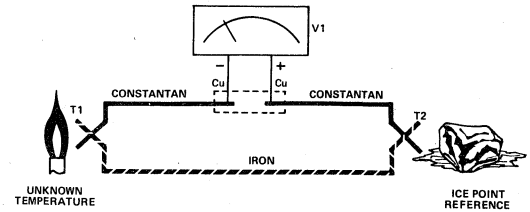


Figure 14. Thermocouple Voltage with 0°C Reference

An alternative measurement technique, illustrated in Figure 15, is used in most practical applications where accuracy requirements do not warrant maintenance of primary standards. The reference junction temperature is allowed to change with the environment

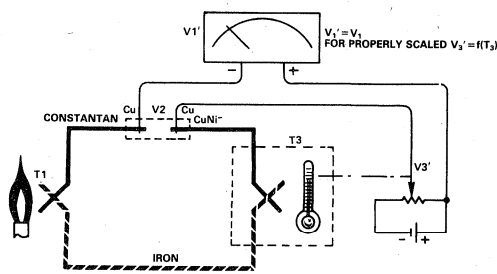


Figure 15. Substitution of Measured Reference Temperature for Ice Point Reference

of the measurement system, but it is carefully measured by some type of absolute thermometer. A measurement of the thermocouple voltage combined with a knowledge of the reference temperature can be used to calculate the measurement junction temperature. Usual practice, however, is to use a convenient thermoelectric method to measure the reference temperature and to arrange its output voltage so that it corresponds to a thermocouple referred to 0°C. This voltage is simply added to the thermocouple voltage and the sum then corresponds to the standard voltage tabulated for an ice-point referenced thermocouple.

The temperature sensitivity of silicon integrated circuit transistors is quite predictable and repeatable. This sensitivity is exploited in the AD594/AD595 to produce a temperature related voltage to compensate the reference or "cold" junction of a thermocouple as shown in Figure 16.

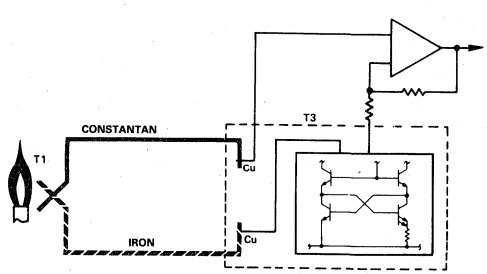


Figure 16. Connecting Isothermal Junctions

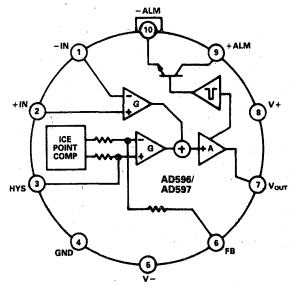
Since the compensation is at the reference junction temperature, it is often convenient to form the reference "junction" by connecting directly to the circuit wiring. So long as these connections and the compensation are at the same temperature no error will result.

Thermocouple Conditioner and Set-Point Controller

AD596*/AD597*

FEATURES
- **Low Cost**
- **Operates with Type J (AD596) or Type K (AD597) Thermocouples**
- **Built-In Ice Point Compensation**
- **Temperature Proportional Operation – 10mV/°C**
- **Temperature Set-Point Operation – ON/OFF**
- **Programmable Switching Hysteresis**
- **High Impedance Differential Input**

AD596/AD597 FUNCTIONAL BLOCK DIAGRAM



8

PRODUCT DESCRIPTION

The AD596/AD597 is a monolithic temperature set-point controller which has been optimized for use at elevated temperatures such as those found in oven control applications. The device cold junction compensates and amplifies a type J or K thermocouple input to derive an internal signal proportional to temperature. The internal signal is then compared with an externally applied set-point voltage to yield a low impedance switched output voltage. Dead-Band or switching hysteresis can be programmed using a single external resistor. Alternately, the AD596/AD597 can be configured to provide a voltage output (10mV/°C) directly from a type J or K thermocouple signal. It can also be used as a stand-alone voltage output temperature sensor.

The AD596/AD597 can be powered with a single supply from +5V to +30V, or dual supplies up to a total span of 36V. Typical quiescent supply current is 160μA which minimizes self-heating errors.

The AD596/AD597 includes a thermocouple failure alarm that indicates an open thermocouple lead when operated in the temperature proportional measurement mode. The alarm output has a flexible format which can be used to drive relays, LEDs or TTL logic.

The device is packaged in a reliability qualified, cost effective 10-pin metal can and is trimmed to operate over an ambient temperature range from +25°C to +100°C. Operation over an extended ambient temperature range is possible with slightly reduced accuracy. The AD596 will amplify thermocouple signals covering the entire −200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate −200°C to +1250°C type K inputs.

The AD596/AD597 has a calibration accuracy of ±4°C at an ambient temperature of 60°C and an ambient temperature stability specification of 0.05°C/°C from +25°C to +100°C. If higher accuracy, or a lower ambient operating temperature is required, either the AD594 (J thermocouple) or AD595 (K thermocouple) should be considered.

PRODUCT HIGHLIGHTS

1. The AD596/AD597 provides cold junction compensation and a high gain amplifier which can be used as a set-point comparator.
2. The input stage of the AD596/AD597 is a high quality instrumentation amplifier that allows the thermocouple to float over most of the supply voltage range.
3. Linearization not required for thermocouple temperatures close to 175°C (+100°C to +540°C for AD596).
4. Cold junction compensation is optimized for ambient temperatures ranging from +25°C to +100°C.
5. In the stand-alone mode, the AD596/AD597 produces an output voltage that indicates its own temperature.

***Protected by U.S. Patent No. 4,029,974.**

SPECIFICATIONS (@ +60°C and V_S = 5V, Type J (AD596), Type K (AD597) Thermocouple, unless otherwise noted)

Model	AD596			AD597			Units
	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS							
$+V_S$ to $-V_S$			36			36	Volts
Common-Mode Input Voltage	$(-V_S-0.15)$		$+V_S$	$(-V_S-0.15)$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages							
+ALM	$-V_S$		$(-V_S+36)$	$-V_S$		$(-V_S+36)$	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			
TEMPERATURE MEASUREMENT							
(Specified Temperature Range							
+25°C to +100°C)							
Calibration Error with 175°C Thermocouple[1]	**−4**		+4	**−4**		**+4**	°C
Stability vs. Temperature[2]			±0.05			±0.05	°C/°C
Gain Error	**−1.5**		+1.5	**−1.5**		**+1.5**	%
Nominal Transfer Function		10			10		mV/°C
AMPLIFIER CHARACTERISTICS							
Closed Loop Gain[3]		180.6			245.5		
Input Offset Voltage		°C × 53.21 + 236			°C × 41.27 − 37		µV
Input Bias Current		0.1			0.1		µA
Differential Input Range	−10		+50	−10		+50	mV
Common Mode Range	$(-V_S-0.15)$		$(+V_S-4)$	$(-V_S-0.15)$		$(+V_S-4)$	Volts
Common Mode Sensitivity – RTO			**10**			10	mV/V
Power Supply Sensitivity – RTO			**10**			10	mV/V
Output Voltage Range							
Dual Supplies	$(-V_S+2.5)$		$(+V_S-2)$	$(-V_S+2.5)$		$(+V_S-2)$	Volts
Single Supply	**0**		$(+V_S+2)$	**0**		$(+V_S-2)$	Volts
Usable Output Current[4]	±5			±5			mA
3dB Bandwidth		15			15		kHz
ALARM CHARACTERISTICS							
$V_{CE(SAT)}$ at 2mA		0.3			0.3		Volts
Leakage Current			±1			**±1**	µA
Operating Voltage at −ALM			$(+V_S-4)$			$(+V_S-4)$	Volts
Short Circuit Current		20			20		mA
POWER REQUIREMENTS							
Operating		$(+V_S$ to $-V_S) \leq 30$			$(+V_S$ to $-V_S) \leq 30$		Volts
Quiescent Current							
$+V_S$		160	**300**		160	**300**	µA
$-V_S$		160			160		µA
PACKAGE OPTION[5]							
TO-100		AD596AH			AD597AH		

NOTES

[1]Calibrated for minimum error at a device temperature of 60°C and a thermocouple temperature of 175°C using a thermocouple sensitivity of 55.38µV/°C for AD596 and 40.74µV/°C for the AD597. With the thermocouple at 0°C, the AD596 will normally read 54mV due to thermocouple nonlinearity.

[2]Defined as the slope of the line connecting the AD596/AD597 CJC errors measured at 25°C and 100°C ambient temperature.

[3]Pin 6 shorted to pin 7.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV	Thermocouple Temperature °C	Type J Voltage mV	AD596 Output mV	Type K Voltage mV	AD597 Output mV
− 200	− 7.890	−1370	− 5.891	−1446	500	27.388	5000	20.640	5066
− 180	− 7.402	−1282	− 5.550	−1362	520	28.511	5203	21.493	5276
− 160	− 6.821	−1177	− 5.141	−1262	540	29.642	5407	22.346	5485
− 140	− 6.159	−1058	− 4.669	−1146	560	30.782	5613	23.198	5694
− 120	− 5.426	− 925	− 4.138	−1016	580	31.933	5821	24.050	5903
− 100	− 4.632	− 782	− 3.553	− 872	600	33.096	6031	24.902	6112
− 80	− 3.785	− 629	− 2.920	− 717	620	34.273	6243	25.751	6321
− 60	− 2.892	− 468	− 2.243	− 551	640	35.464	6458	26.599	6529
− 40	− 1.960	− 299	− 1.527	− 375	660	36.671	6676	27.445	6737
− 20	− .995	− 125	− .777	− 191	680	37.893	6897	28.288	6944
− 10	− .501	− 36	− .392	− 96	700	39.130	7120	29.128	7150
0	0	54	0	0	720	40.382	7346	29.965	7355
10	.507	146	.397	97	740	41.647	7575	30.799	7560
20	1.019	238	.798	196	750	42.283	7689	31.214	7662
25	1.277	285	1.000	245	760	–	–	31.629	7764
30	1.536	332	1.203	295	780	–	–	32.455	7966
40	2.058	426	1.611	395	800	–	–	33.277	8168
50	2.585	521	2.022	496	820	–	–	34.095	8369
60	3.115	617	2.436	598	840	–	–	34.909	8569
80	4.186	810	3.266	802	860	–	–	35.718	8767
100	5.268	1006	4.095	1005	880	–	–	36.524	8965
120	6.359	1203	4.919	1207	900	–	–	37.325	9162
140	7.457	1401	5.733	1407	920	–	–	38.122	9357
160	8.560	1600	6.539	1605	940	–	–	38.915	9552
180	9.667	1800	7.338	1801	960	–	–	39.703	9745
200	10.777	2000	8.137	1997	980	–	–	40.488	9938
220	11.887	2201	8.938	2194	1000	–	–	41.269	10130
240	12.998	2401	9.745	2392	1020	–	–	42.045	10320
260	14.108	2602	10.560	2592	1040	–	–	42.817	10510
280	15.217	2802	11.381	2794	1060	–	–	43.585	10698
300	16.325	3002	12.207	2996	1080	–	–	44.439	10908
320	17.432	3202	13.039	3201	1100	–	–	45.108	11072
340	18.537	3402	13.874	3406	1120	–	–	45.863	11258
360	19.640	3601	14.712	3611	1140	–	–	46.612	11441
380	20.743	3800	15.552	3817	1160	–	–	47.356	11624
400	21.846	3999	16.395	4024	1180	–	–	48.095	11805
420	22.949	4198	17.241	4232	1200	–	–	48.828	11985
440	24.054	4398	18.088	4440	1220	–	–	49.555	12164
460	25.161	4598	18.938	4649	1240	–	–	50.276	12341
480	26.272	4798	19.788	4857	1250	–	–	50.633	12428

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +60°C, V_S = −5V, +15V)

TEMPERATURE PROPORTIONAL OUTPUT MODE

The AD596/AD597 can be used to generate a temperature proportional output of 10mV/°C when operated with J and K type thermocouples as shown in Figure 1. Thermocouples produce low level output voltages which are a function of both the temperature being measured and the reference or cold junction temperature at the measuring end. The AD596/AD597 compensates for the cold junction temperature and amplifies the thermocouple signal to produce a high level 10mV/°C voltage output which is a function only of the temperature being measured. The temperature stability of the part indicates the sensitivity of the output voltage to changes in ambient or device temperatures. This is typically 0.02°C/°C over the +25°C to +100°C recommended ambient temperature range. The parts will operate over the extended ambient temperature ranges from −55°C to +125°C, but thermocouple nonlinearity at the reference junction will degrade the temperature stability over this extended range. Table I is a list of ideal AD596/AD597 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples with package and reference junction at 60°C. As

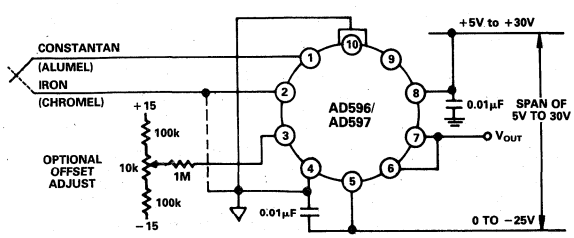


Figure 1. Temperature Proportional Output Connection

is normally the case, these outputs are subject to calibration and temperature sensitivity errors. These tables are derived using the ideal transfer functions:

AD596 output = (Type J voltage +301.5µV) × 180.57
AD597 output = (Type K voltage) × 245.46

The offsets and gains of these devices have been laser trimmed to closely approximate thermocouple characteristics over measurement temperature ranges centered around 175°C with the

AD596/AD597 at an ambient temperature between 25°C and 100°C. This eliminates the need for additional gain or offset adjustments to make the output voltage read:

$$V_{OUT} = 10mV/°C \times (\text{thermocouple temperature in °C})$$
(within specified tolerances).

Excluding calibration errors, the above transfer function is accurate to within 1°C from +80°C to +550°C for the AD596 and −20°C to +350°C for the AD597. The different temperature ranges are due to the differences in J and K type thermocouple curves.

European DIN FE-CuNi thermocouple vary slightly from ANSI type J thermocouples. Table I does not apply when these types of thermocouples are used. The transfer functions given previously and a thermocouple table should be used instead.

Figure 1 shows an optional trimming network which can be used to change the device's offset voltage. Injecting or sinking 200nA from Pin 3 will offset the output aproximately 10mV (1°C).

The AD596/AD597 can operate from a single supply from 5V to 36V or from split supplies totalling 36V or less as shown. Since the output can only swing to within 2V of the positive supply, the usable measurement temperature range will be restricted when positive supplies less than 15V for the AD597 and 10V for the AD596 are used. If the AD596/AD597 is to be used to indicate negative Celsius temperatures, then a negative supply is required.

Common-mode voltages on the thermocouple inputs must remain within the common-mode voltage range of the AD596/AD597, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connection shown in Figure 1 must be made to one of the thermocouple inputs. A resistor up to 1kΩ can be used in this connection to provide a current return path for the input bias current. If there is no return path for the bias currents, the input stage will saturate, causing erroneous output voltages.

In this configuration, the AD596/AD597 has circuitry which detects the presence of an open thermocouple. If the thermocouple loop becomes open, one or both of the inputs to the device will be deprived of bias current causing the output to saturate. It is this saturation which is detected internally and used to activate the alarm circuitry. The output of this feature has a flexible format which can be used to source or sink up to 20mA of current. The collector (+ALM) should not be allowed to become more positive than ($-V_S$ +36V), however, it may be permitted to be more positive than $+V_S$. The emitter voltage (−ALM) should be constrained such that it does not become more positive than 4V below $+V_S$. If the alarm feature is not used, this pin should be connected to Pins 4 or 5 as shown in Figure 1.

SET-POINT CONTROL MODE

The AD596/AD597 can be connected as a set-point controller as shown in Figure 2. The thermocouple voltage is cold junction compensated, amplified, and compared to an external set-point voltage. The relationship between set-point voltage and temperature is given in Table I. If the temperature to be controlled is within the operating range (−55°C to +125°C) of the device, it can monitor its own temperature by shorting the inputs to ground. The set-point voltage with the thermocouple inputs grounded is given by the expressions:

AD596 Set-Point Voltage = °C × 9.6mV/°C +42mV
AD597 Set-Point Voltage = °C × 10.1mV/°C −9.1mV

The input impedance of the set-point pin of the AD596/AD597 is approximately 50kΩ. The temperature coefficient of this resistance is ±15ppm/°C. Therefore, the 100ppm/°C 5kΩ pot

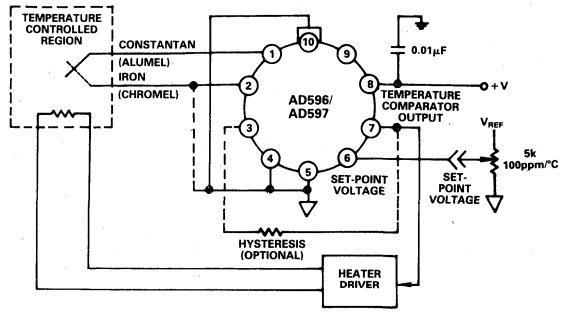


Figure 2. Set-Point Control Mode

shown in Figure 2 will only introduce an additional ±1°C degradation of temperature stability over the +25°C to +100°C ambient temperature range.

Switching hysteresis is often used in set-point systems of this type to provide noise immunity and increase system reliability. By reducing the frequency of on-off cycling, mechanical component wear is reduced leading to enhanced system reliability. This can easily be implemented with a single external resistor between Pins 7 and 3 of the AD596/AD597. Each 200nA of current injected into Pin 3 when the output switches will cause about 1°C of hysteresis.

In the set-point configuration, the AD596/AD597 output is saturated at all times, so the alarm transistor will be ON regardless of whether there is an open circuit or not. However, −ALM must be tied to a voltage below ($+V_S$ −4V) for proper operation of the rest of the circuit.

STAND-ALONE TEMPERATURE TRANSDUCER

The AD596/AD597 may be configured as a stand-alone Celsius thermometer as shown in Figure 3.

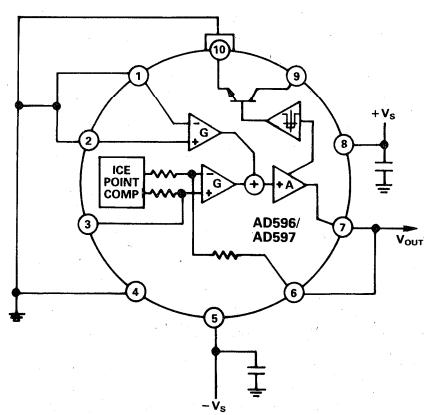


Figure 3. Stand-Alone Temperature Transducer Temperature Proportional Output Connection

Simply omit the thermocouple and connect the inputs (Pins 1 and 2) to common. The output will now reflect the compensation voltage and hence will indicate the AD596/AD597 temperature. In this three terminal, voltage output, temperature sensing mode, the AD596/AD597 will operate over the full extended −55°C to +125°C temperature range. The output scaling will be 9.6mV per °C with the AD596 and 10.1mV per °C with the AD597. Additionally there will be a 42mV offset with the AD596 causing it to read slightly high when used in this mode.

THERMOCOUPLE CONNECTIONS

The connection of the thermocouple wire and the normal wire or printed circuit board traces going to the AD596/AD597 forms an effective reference junction as shown in Figure 4. This junction must be kept at the same temperature as the AD596/AD597 for the internal cold junction compensation to work properly. Unless the AD596/AD597 is in a thermally stable enclosure, the thermocouple leads should be brought in directly to Pins 1 and 2.

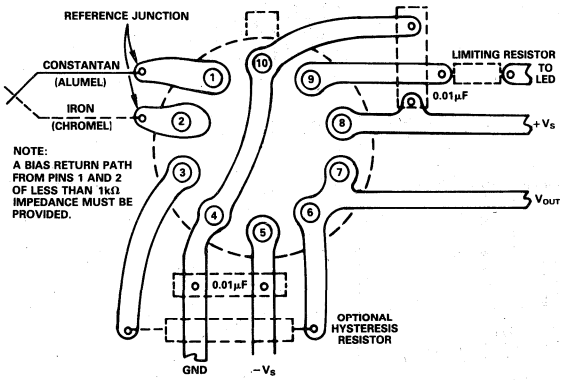


Figure 4. PCB Connections

To ensure secure bonding, the thermocouple wire should be cleaned to remove oxidization prior to soldering. Noncorrosive resin flux is effective with iron, constantan, chromel, and alumel, and the following solders: 95% tin–5% silver, or 90% tin–10% lead.

SINGLE AND DUAL SUPPLY CONNECTIONS

In the single supply configuration as used in the set-point controller of Figure 2, any convenient voltage from +5V to +36V may be used, with self-heating errors being minimized at lower supply levels. In this configuration, the $-V_S$ connection at Pin 5 is tied to ground. Temperatures below zero can be accommodated in the single supply set-point mode, but not in the single supply temperature measuring mode (Figure 1 reconnected for single supply). Temperatures below zero can only be indicated by a negative output voltage, which is impossible in the single supply mode.

Common-mode voltages on the thermocouple inputs must remain below the positive supply, and not more than 0.15V more negative than the minus supply. In addition, a return path for the input bias currents must be provided. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are mandatory.

STABILITY OVER TEMPERATURE

The AD596/AD597 is specified for a maximum error of ±4°C at an ambient temperature of 60°C and a measuring junction temperature at 175°C. The ambient temperature stability is specified to be a maximum of 0.05°C/°C. In other words, for every degree change in the ambient temperature, the output will change no more than 0.05 degree. So, at 25°C the maximum deviation from the temperature-voltage characteristic of Table I is ±5.75°C, and at 100°C it is ±6°C maximum. If the offset error of ±4°C is removed with a single offset adjustment, these errors will be be reduced to ±1.75°C and a ±2°C max. The optional trim circuit shown in Figure 1 demonstrates how the ambient offset error can be adjusted to zero.

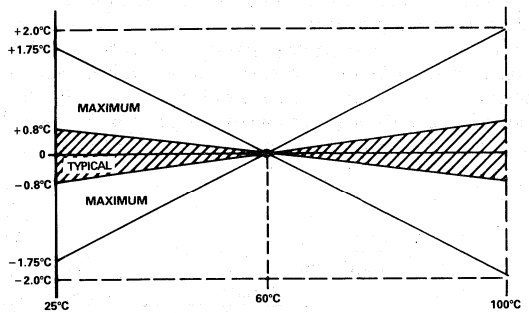


Figure 5. Drift Error vs. Temperature

THERMAL ENVIRONMENTAL EFFECTS

The inherent low power dissipation of the AD596/AD597 keeps self-heating errors to a minimum. However, device output is capable of delivering ±5mA to an external load and the alarm circuitry can supply up to 20mA. Since the typical junction to ambient thermal resistance in free air is 150°C/W, significant temperature difference between the package pins (where the reference junction is located) and the chip (where the cold junction temperature is measured and then compensated) can exist when the device is operated in a high dissipation mode. These temperature differences will result in a direct error at the output. In the temperature proportional mode, the alarm feature will only activate in the event of an open thermocouple or system transient which causes the device output to saturate. Self-Heating errors will not effect the operation of the alarm but two cases do need to be considered. First, after a fault is corrected and the alarm is reset, the AD596/AD597 must be allowed to cool before readings can again be accurate. This can take 5 minutes or more depending upon the thermal environment seen by the device. Second, the junction temperature of the part should not be allowed to exceed 150°C. If the alarm circuit of the AD596/AD597 is made to source or sink 20mA with 30V across it, the junction temperature will be 90°C above ambient causing the die temperature to exceed 150°C when ambient is above 60°C. In this case, either the load must be reduced, or a heat sink used to lower the thermal resistance.

TEMPERATURE READOUT AND CONTROL

Figure 6 shows a complete temperature indication and control system based on the AD596/AD597. Here the AD596/AD597 is being used as a closed-loop thermocouple signal conditioner and an external op-amp is used to implement set point. This has two important advantages. It provides a high level (10mV/°C) output for the A/D panel meter and also preserves the alarm function for open thermocouples.

The A/D panel meter can easily be offset and scaled as shown to read directly in degrees Fahrenheit. If a two temperature calibration scheme is used, the dominant residual errors will arise from two sources; the ambient temperature rejection (typically ±2°C over a 25°C to 100°C range) and thermocouple nonlinearity typical +1°C from 80°C to 550°C for type J and +1°C from −20°C to 350°C for type K.

An external voltage reference is used both to increase the stability of the A/D converter and supply a stable reference for the set-point voltage.

A traditional requirement for the design of set-point control thermocouple systems has been to configure the system such that the appropriate action is taken in the event of an open thermocouple. The open thermocouple alarm pin with its flexible current-limited output format supports this function when the part operates in the temperature proportional mode. In addition, if the thermocouple is not remotely grounded, it is possible to program the device for either a positive or negative full scale output in the event of an open thermocouple. This is done by connecting the bias return resistor directly to Pin 1 if a high output voltage is desired to indicate a fault condition. Alternately, if the bias return is provided on the thermocouple lead connected to Pin 2, an open circuit will result in an output low reading Figure 6 shows the ground return connected to Pin 1 so that if the thermocouple fails, the heater will remain off. At the same time, the alarm circuit lights the LED signalling the need to service the thermocouple. Grounding Pin 2 would lead to low output voltage saturation, and in this circuit would result in a potentially dangerous thermal runaway under fault conditions.

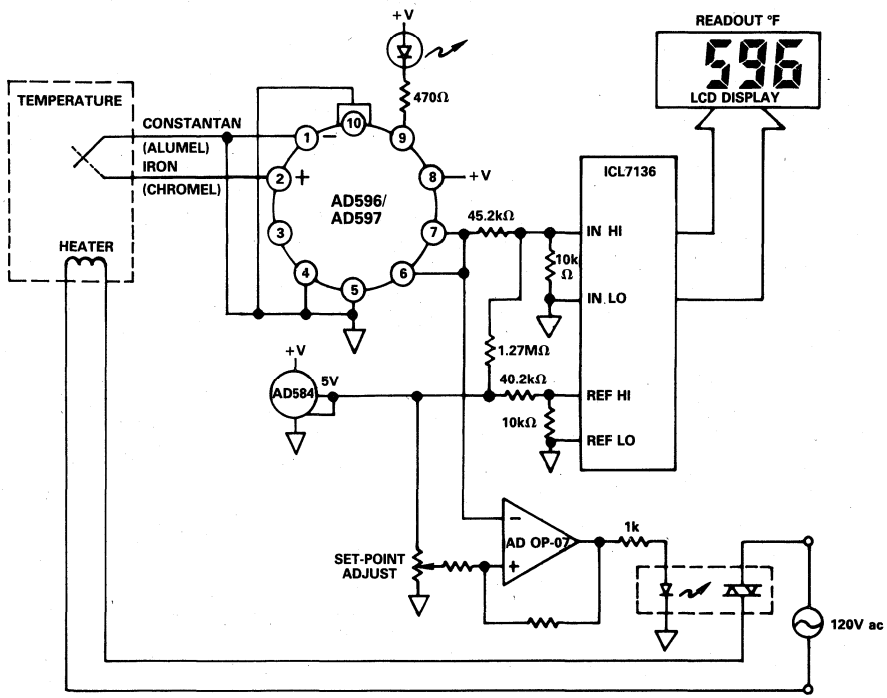


Figure 6. Temperature Measurement and Control

Digital-to-Analog Converters

Contents

•New product since publication of *1982–1983 Databook Update.*

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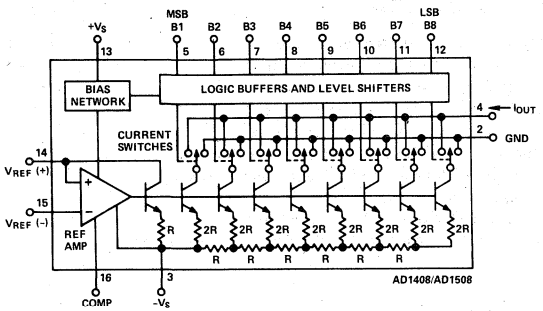
Digital-to-Analog Converters

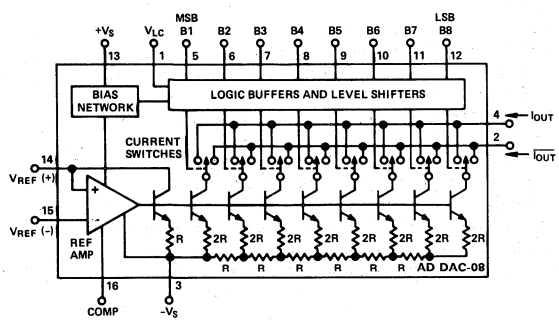
General Purpose 8-Bit D/A Converters



AD1408/AD1508

Page
Vol. I
9-265

- Improved Replacement for Industry Standard 1408/1508
- Improved Settling Time: 250ns typ
- Improved Linearity: ±0.1% Accuracy Guaranteed Over Temperature Range (−9 Grade)
- High Output Voltage Compliance: +0.5V to −5.0V
- Low Power Consumption: 157mW typ
- High Speed 2-Quadrant Multiplying Input: 4.0mA/μs Slew Rate
- Single Chip Monolithic Construction
- Hermetic 16-Pin Ceramic DIP



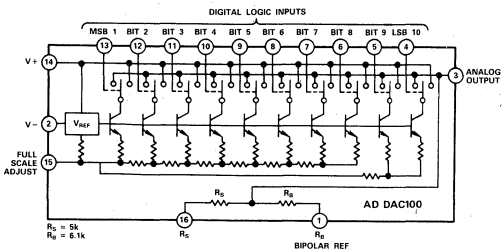
AD DAC-08

Vol. I
9-89

- Exact Replacement for Industry Standard DAC-08
- Fast (85ns typical) Settling Time
- Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
- Wide Output Voltage Compliance: −10V to +18V
- Single Chip Monolithic Construction
- 16-Pin Ceramic DIP Packaging

Selection Guide
Digital-to-Analog Converters

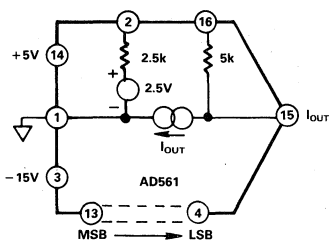
General Purpose 10-Bit D/A Converters



AD DAC-100

Page

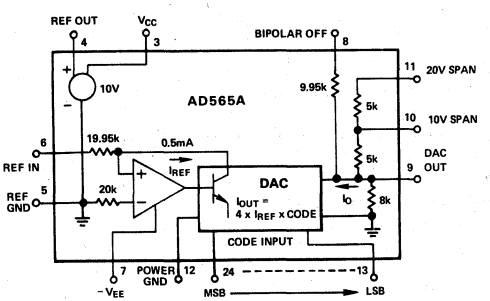
Complete Current Output Converter Vol. I
High Stability Buried Zener Reference 9-287
Single Chip Monolithic Construction
Wide Supply Range ±6V to ±18V
Trimmed Output Application Resistors
Fast Settling – 225ns (8 Bits), 375ns (10 Bits)
Guaranteed Monotonicity Over Full Operating Temperature Range
TTL and DTL Compatible Logic Inputs
Hermeticaly-Sealed 16-Pin Ceramic DIP (All Grades)



AD561

Complete Current Output Converter Vol. I
High Stability Buried Zener Reference 9-43
Laser Trimmed to High Accuracy (1/4 LSB Max Error, AD561K, T)
Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
Fast Settling – 250ns to 1/2LSB
Guaranteed Monotonicity Over Full Operating Temperature Range
TTL/DDT and CMOS Compatible (Positive True Logic)
Single Chip Monolithic Construction
Hermetically-Sealed Ceramic DIP (All Grades)

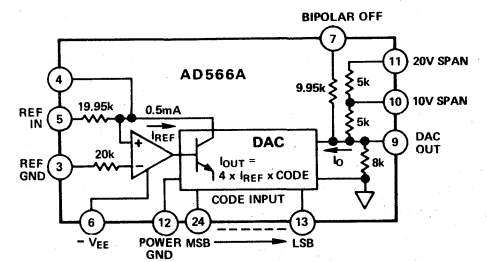
General Purpose 12-Bit D/A Converters



AD565A

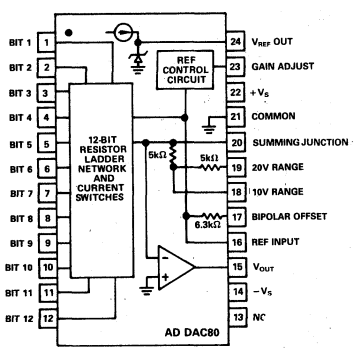
Page

- Single Chip Construction — Vol. I
- Very High Speed: Settles to 1/2LSB in 250ns max — 9-57
  Full Scale Switching Time: 30ns
- High Stability Buried Zener Reference On Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD565AK, T)
- Guaranteed for Operation with ±12V Supplies
- Low Power: 225mW Including Reference
- Pin-Out Compatible with AD563, AD565



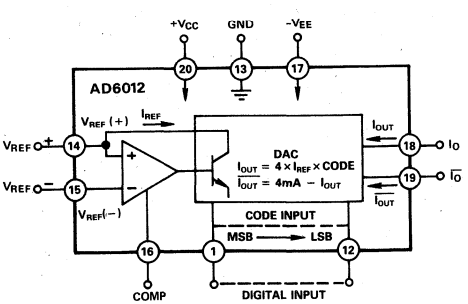
AD566A

- Single Chip Construction — Vol. I
- Very High Speed: Settles to 1/2LSB in 350ns max — 9-65
  Full Scale Switching Time: 30ns
- Guaranteed for Operation with −12V Supply
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD566AK, T)
- Low Power: 180mW
- Pin-Out Compatible with AD562, AD566



AD DAC80 SERIES

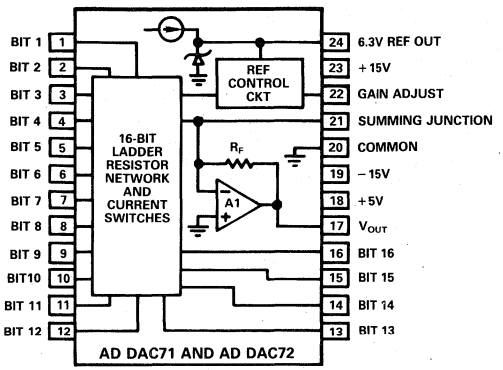
- Single Chip Construction — Vol. I
- On-Board Output Amplifier — 9-277
- Low Power Dissipation: 300mW
- Monotonicity Guaranteed Over Temperature
- Guaranteed for Operation with ±12V Supplies
- Improved Replacement for Standard DAC80
- High Stability, High Current Output Buried Zener Reference
- Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity
- Low Cost Plastic Packaging
- Current Out Models and Voltage Output Models Available



AD6012

- 1/2LSB max Differential Linearity Error Over Temperature — Vol. I 9-97
- 250ns Typical Settling Time
- Full Scale Current 4mA
- High Speed Multiplying Capability
- TTL/CMOS/ECL/HTL Compatible
- High Output Compliance: −5V to +10V
- Complementary Current Outputs
- Low Power Consumption: 230mW

Selection Guide
Digital-to-Analog Converters
High Resolution D/A Converters



AD DAC71/AD DAC72

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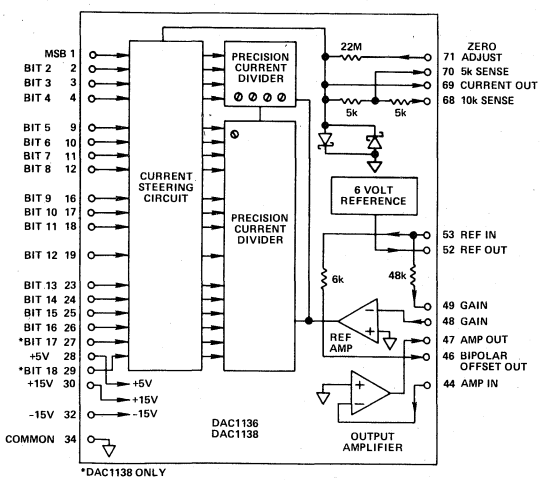
16-Bit Resolution Vol. I
±0.003% Maximum Nonlinearity 9–271
Low Gain Drift ±7ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC71H, AD DAC72C)
−25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source

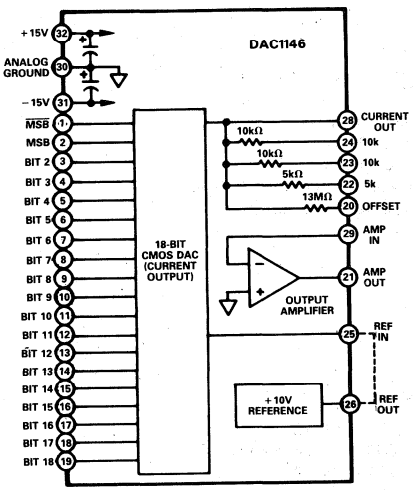


DAC1136

16-Bit Resolution and Accuracy Vol. II
Low Cost 10–27
Nonlinearity 1/2LSB
Settling to 1/2LSB (0.0008%) in 6μs

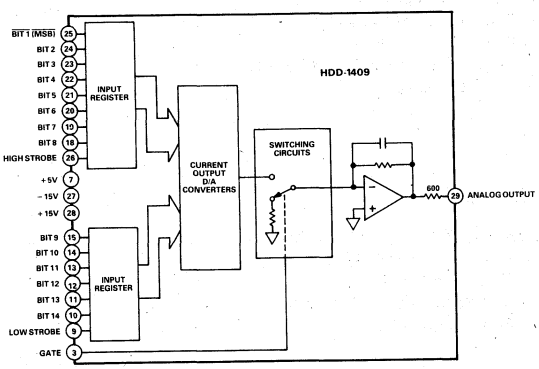
DAC1138

18-Bit Resolution and Accuracy (38μV, 1 Part in 62,144) Vol. II
Integral Nonlinearity 1/2LSB 10–27
Differential Nonlinearity 1/2LSB
Settling to 1/2LSB (0.002%) in 10μs
Hermetically-Sealed Semiconductors



DAC1146

	Page
Low Cost, High Accuracy 18-Bit D/A Converter	Vol. II
Integral Nonlinearity: ±0.00076% FSR max	10-35
Differential Nonlinearity: ±0.00076% FSR max	
Low Differential Nonlinearity T.C.: ±1ppm/°C max	
Wide Power Supply Operation: ±11.5V to ±16V	
Fast Settling: 6µs to ±0.00076% FSR	
Small Size 2" × 2" × 0.4"	



HDD-1409

14-Bit Resolution
200kHz Word Rates
RZ Gated Output
32-Pin DIP

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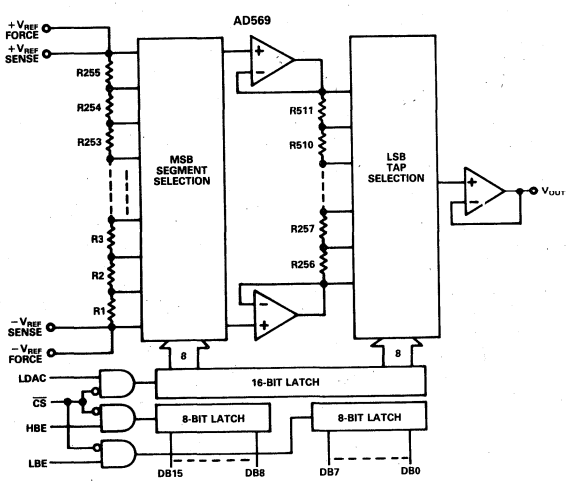
Digital Signal Processing	
PCM Systems	
Digital Audio	



AD569

Guaranteed 16-Bit Monotonicity
Voltage Output, 6µs Settling Time
Monolithic BIMOS Construction
±0.02% Nonlinearity
8- and 16-Bit Bus Compatible
6µs Settling Time
Low Drift
Low Power: 150mW
Low Cost

Vol. I
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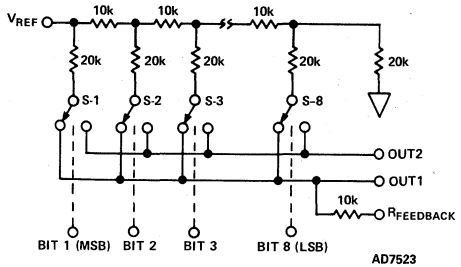
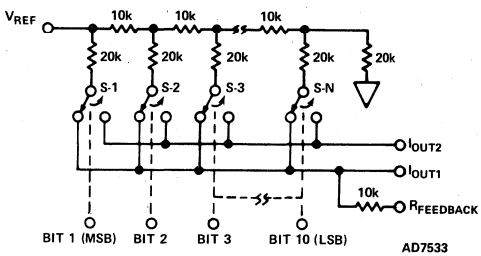
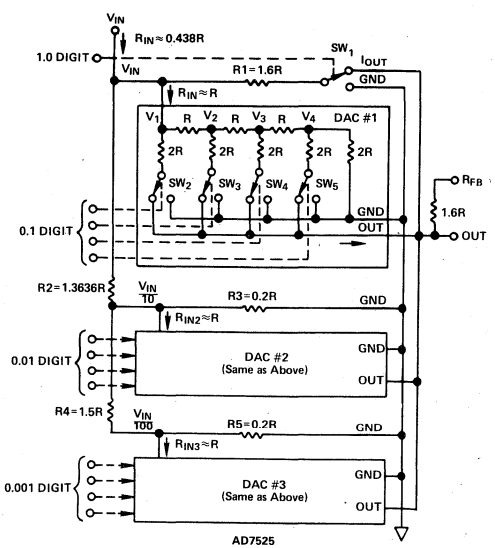
Selection Guide
Digital-to-Analog Converters
CMOS Multiplying D/A Converters



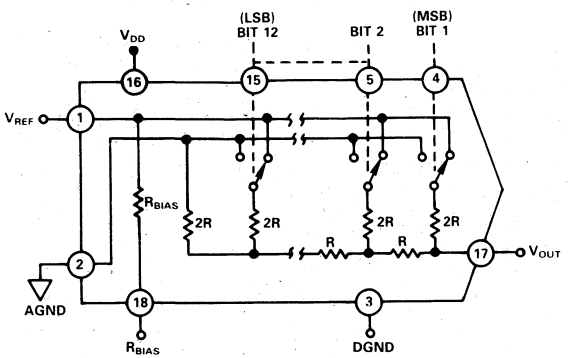
AD7523



AD7533



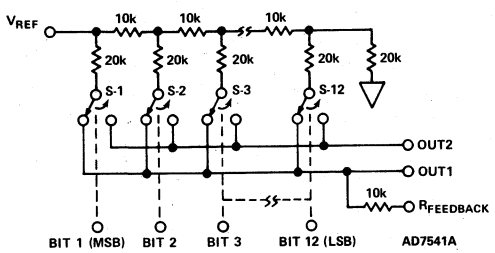
AD7525



AD7240

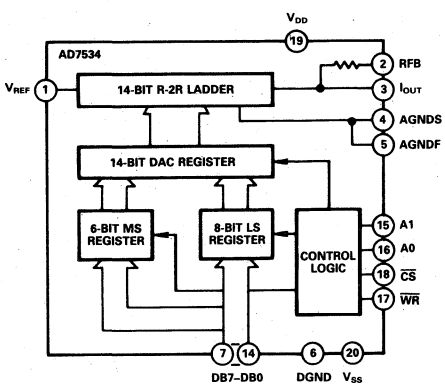
Page

- 12 Bits of Resolution — Vol. I
- Fast Voltage Settling Time: 550ns to 0.01% — 9-145
- Total Unadjusted Error: 1LSB max
- Single Supply Operation
- Latch-Up Proof (No Protection Schottky Required)
- Superb Differential Nonlinearity: 1/2LSB max Over Temperature
- Low Power Dissipation: 30mW



AD7541A

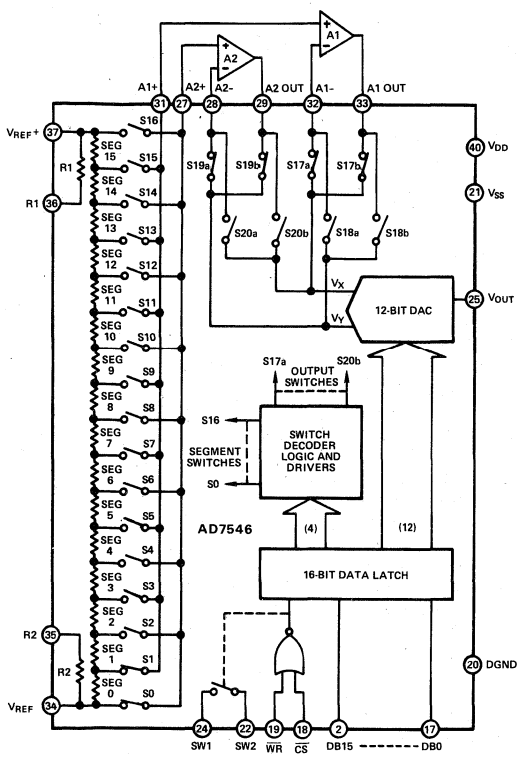
- 12 Bits of Resolution — Vol. I
- Improved Version of AD7541 — 9-209
- Full Four Quadrant Multiplication
- 12-Bit Linearity (End-Point)
- ±1LSB Gain Error
- All Parts Guaranteed Monotonic
- TTL/CMOS Compatible
- Protection Schottky not Required
- Low Logic Input Leakage



AD7534

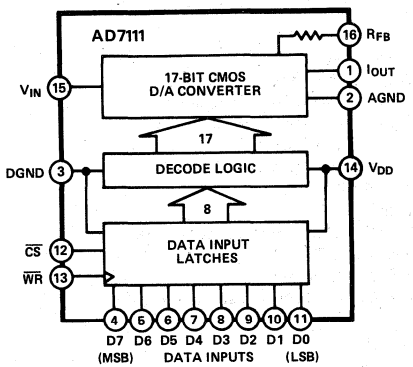
- 14 Bits of Resolution — Vol. I
- Full 4-Quadrnat Multiplication — 9-201
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0ppm/°C typ
- Small 20-Pin Package
- Low Output Leakage (<20nA) over the Full Temperature Range
- All Grades 14-Bit Monotonic over the Full Temperature Range

Selection Guide
Digital-to-Analog Converters
CMOS Multiplying D/A Converters



AD7546

Log D/A Converters

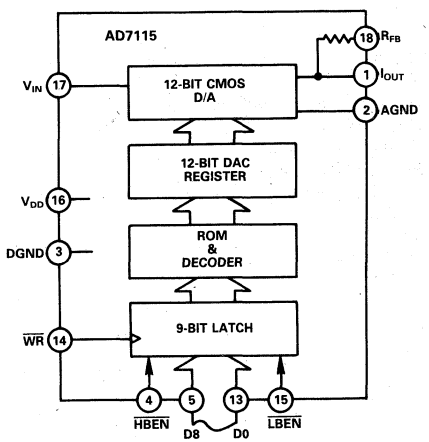


AD7111

Page
Vol. I
9-109

Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

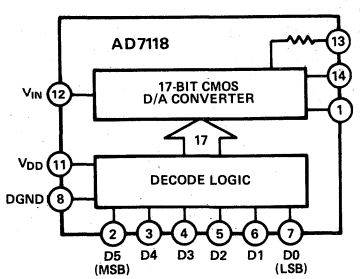
APPLICATIONS
Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators



AD7115

Vol. I
9-115

Dynamic Range: 0 to 19.9dB Plus Full Muting
Resolution: 0.1dB
2 1/2 Digit BCD Input Coding
On-Chip Data Latches
Full ±25V Input Range
Low Distortion and Noise
Latch-Up Free (No Protection Schottky Required)
TTL Compatible

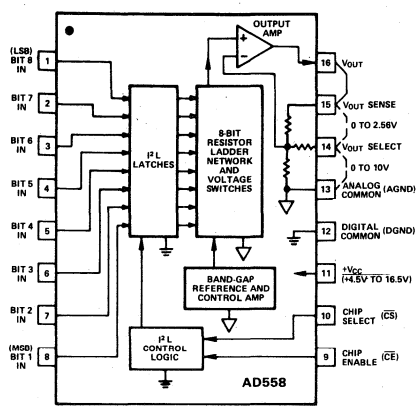


AD7118

Vol. I
9-123

Dynamic Range 85.5dB
Resolution 1.5dB
Full ±25V Input Range Multiplying DAC
Extended Temperature Range −55°C to +125°C
Low Distortion
Low Power Consumption
Latch-Proof Operation (Schottky Diodes Not Required)

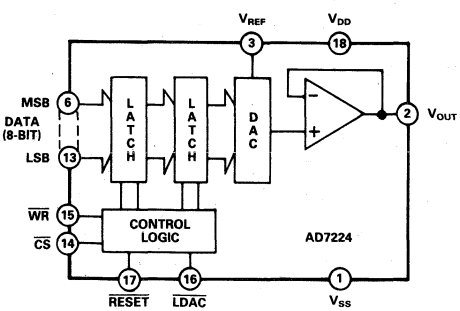
Selection Guide
Digital-to-Analog Converters
8-Bit μP-Compatible D/A Converters



AD558

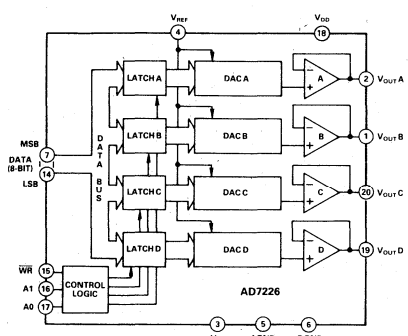
Page

- Complete 8-Bit DAC — Vol. I 9-35
- Voltage Output – 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1μs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP Package
- Single Laser-Wafer-Trimmed Chip for Hybrids



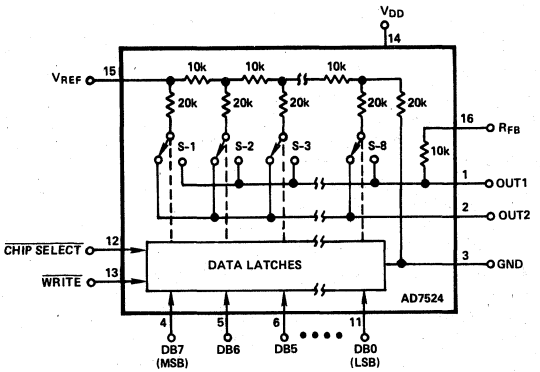
AD7224

- 8-Bit DAC with Output Amplifier — Vol. I 9-129
- Full Double Buffering
- Microprocessor Compatible
- Single Supply Operation
- Multiplying Capability
- No User Trims
- Low Power
- 0.3" Wide 18-Pin DIP



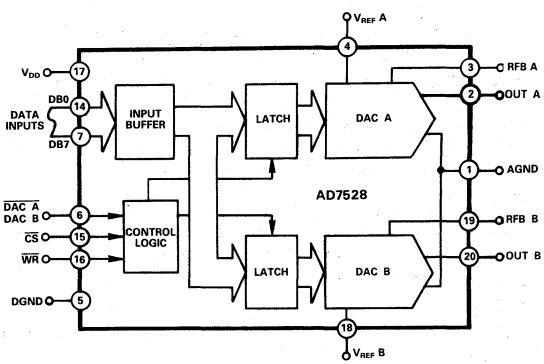
AD7226

- Four 8-Bit DACs with Output Amplifiers — Vol. I 9-133
- 0.3" Wide, 20-Pin DIP
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trims
- Single Supply Operation Possible



AD7524

- Microprocessor Compatible (6800, 8085, Z80, Etc.)
- TTL/CMOS Compatible Inputs
- On-Chip Data Latches
- End Point Linearity
- Low Power Consumption
- Monotonicity Guaranteed (Full Temperature Range)
- Latch-Free (No Protection Schottky Required)

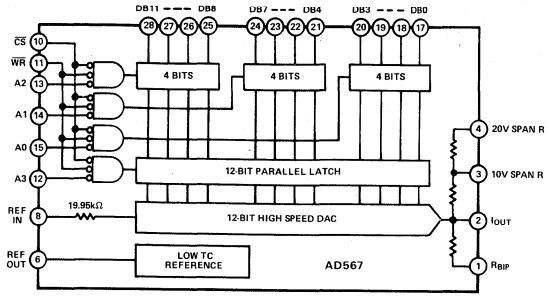


AD7528

- Dual D/A Converter
- On-Chip Latches for Both DACs
- +5V to +15V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch-Free (Protection Schottkys Not Required)

Selection Guide
Digital-to-Analog Converters

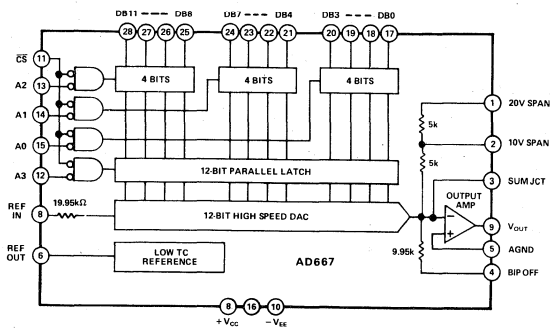
12-Bit µP-Compatible D/A Converters



AD567

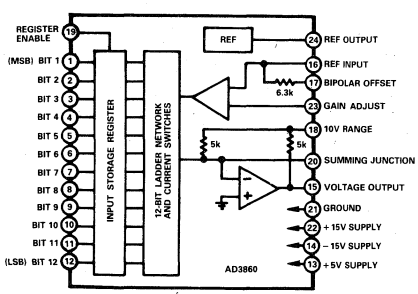
Page

- Single Chip Construction — Vol. I
- Double-Buffered Latch for 8-Bit µP Compatibility — 9–73
- Fast Settling Time: 500ns max to ±1/2LSB
- High Stability Buried Zener Reference on Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K, T)
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs



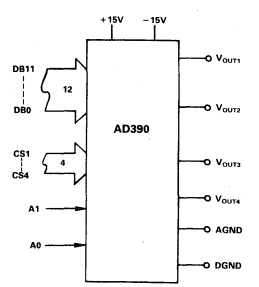
AD667

- Voltage Output — Vol. I
- Single Chip Construction — 9–83
- Double-Buffered Latch for 8-Bit µP-Compatibility
- Fast Settling Time: 5ns max to ±1/2LSB
- High Stability Buried Zener Reference On Chip
- Monotonicity Guaranteed Over Temperature
- Linearity Guaranteed Over Temperature: 1/2LSB max (AD667K, T)
- Guaranteed for Operation with ±12V or ±15V Supplies
- Low Power: 300mW Including Reference
- TTL/5V CMOS Compatible Logic Inputs



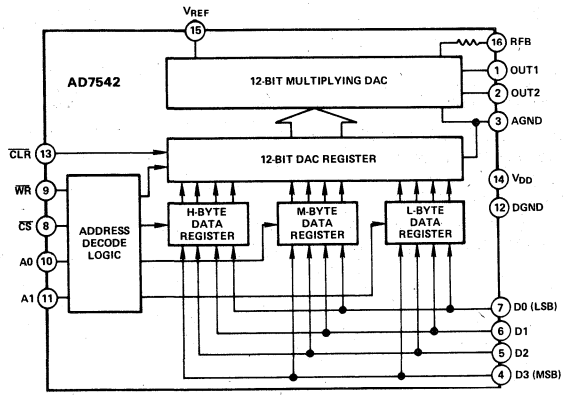
AD3860

- Nonlinearity: ±1/2LSB T_{min} to T_{max} — Vol. I
- 12-Bit Input Register — 9–93
- Small Size: 24-Pin DIP
- Fast Settling: 5µs to ±0.01%
- Internal Reference
- Internal Output Amplifier



AD390

- Four Complete 12-Bit DACs in One IC Package — Vol. I
- Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T) — 9–27
- Factory-Trimmed Gain and Offset
- Buffered Voltage Output
- Monotonicity Guaranteed Over Full Temperature Range
- Double-Buffered Data Latches
- Includes Reference and Buffer
- Fast Settling: 8µs max to ±1/2LSB

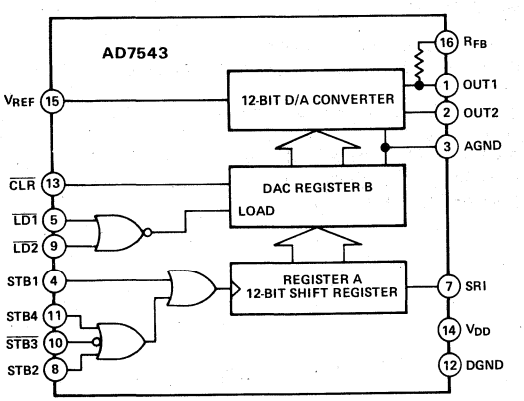


AD7542

Page

Vol. I
9-215

Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
Microprocessor Compatible
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough
Low Power Dissipation: 40mW max
Small Size: 16-Pin DIP



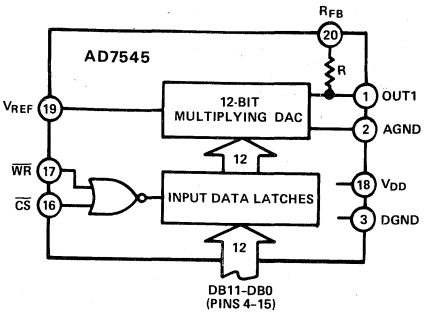
AD7543

Vol. I
9-223

Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
Serial Load on Positive or Negative Strobe
Asynchronous CLEAR Input for Initialization
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough: 1LSB max @ 10kHz
Requires no Schottky Diode Output Protection
Low Power Dissipation: 40mW max
+5V Supply
Small Size: 16-Pin DIP

Selection Guide
Digital-to-Analog Converters

12-Bit µP-Compatible D/A Converters

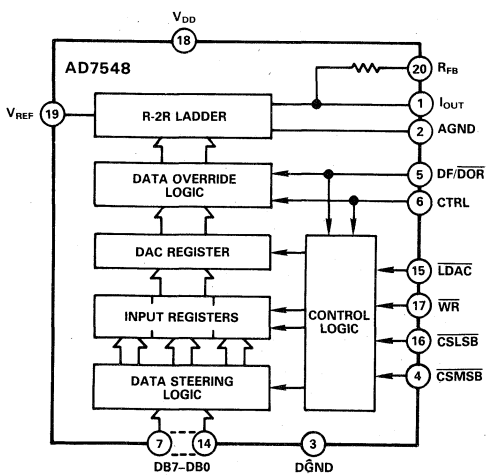


Page

AD7545

Vol. I
9–231

Low Gain T.C.: 2ppm/°C typ
Fast TTL Compatible Data Latches
Single +5V to +15V Supply
Small 20-Pin 0.3″ DIP
Latch Free (Schottky Protection Diode Not Required)
Ideal for Battery Operated Equipment

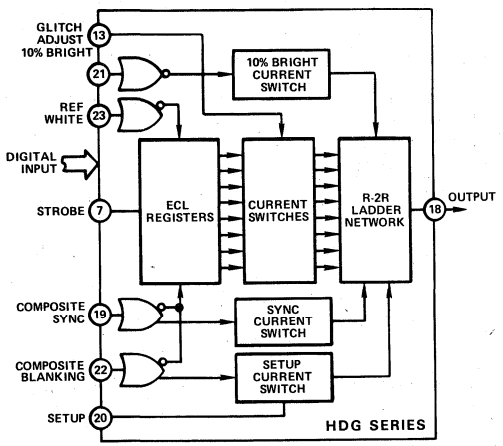


AD7548

Vol. I
9–247

8-Bit Bus Compatible 12-Bit DAC
All Grades 12-Bit Monotonic Over Full Temperature Ranges
Operation Specified at +5V, +12V or +15V Power Supply
Low Gain Drift of 5ppm/°C Maximum
Full 4-Quadrant Multiplication
Small 20-Pin Package

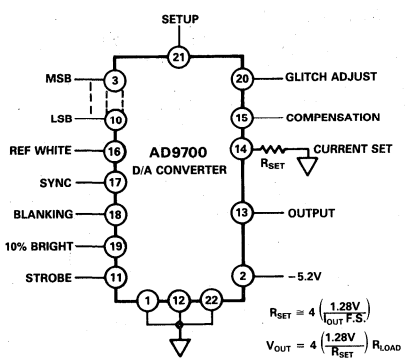
Video Display D/A Converters



HDG SERIES

Page

- Ultra Fast 7ns Settling Time to 0.4% (8ns max) — Vol. I 9-309
- Low 50 pV-s max Glitch Energy
- Operates from Single −5.2V Power Supply
- Complete Composite Inputs
- Designed for General Output Compatibility with EIA Standard RS-170 and RS-343, Including 10% Brightness
- HDG-0805
  - Resolution: 8 Bits
  - % of Gray: 0.4%
  - Settling Time: 8ns
- HDG-0605
  - Resolution: 6 Bits
  - % of Gray: 1.6%
  - Settling Time: 6ns
- HDG-0405
  - Resolution: 4 Bits
  - % of Gray: 6.4%
  - Settling Time: 4ns



AD9700

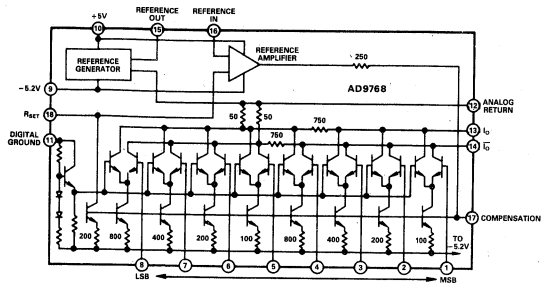
Vol. I 9-259

- Update Rates to 125MHz
- 2ns Rise Time
- On-Chip Reference Voltage
- Single −5.2V Power Supply
- Complete Composite Inputs

APPLICATIONS

- Raster Scan Displays
- Color Graphics
- Automated Test Equipment
- TV Video Reconstruction

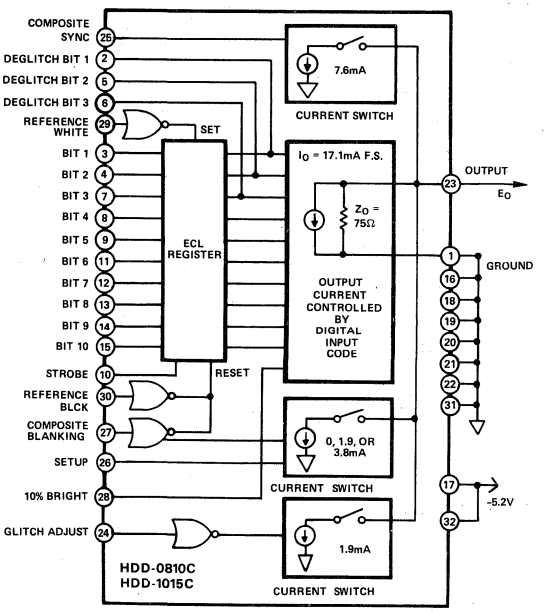
Selection Guide
Digital-to-Analog Converters
Video Display D/A Converters



AD9768

Page
Vol. I
9-261

8 Bits of Resolution
5ns Settling Time
100MHz Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

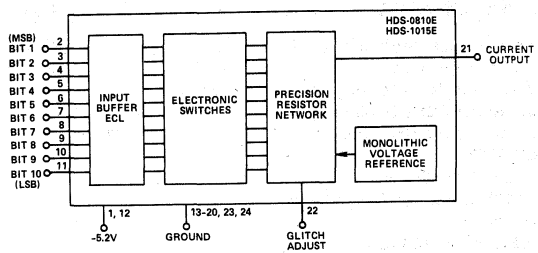


HDD SERIES

Vol. I
9-295

HDD-0810 – 8 Bits of Resolution
HDD-1015 – 10 Bits of Resolution
Ultra Fast 10ns Settling Time to 0.2% (HDD-0810)
15ns Settling Time to 0.1% (HDD-1015)
Internal Monolithic Reference
Low 200pV-s Glitch Energy
Single −5.2V Power Supply
Designed for General Output Compatibility with EIA Standards RS-170 and RS-343, Including 10% Brightness
Complete Composite Inputs (HDD-0810C, HDD-1015C)

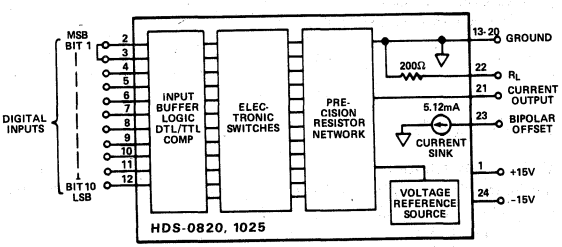
Video Speed Current Output D/A Converters



HDS-0810E/HDS-1015E

Page
Vol. I
9-321

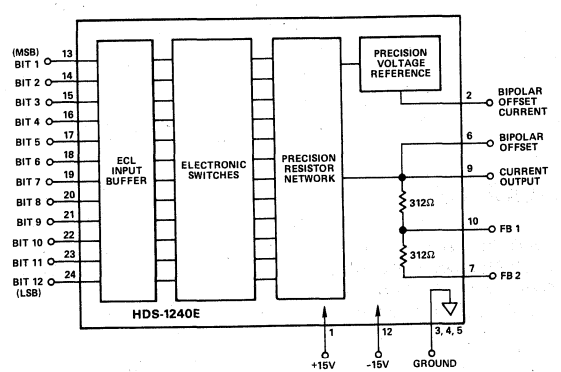
HDS-0810E: 8 Bits
HDS-1015E: 10 Bits
ECL Inputs
Settling Time to 10ns
Low Glitch Energy – 200pV-s
100MHz Update Rates
Low Power <1 Watt



HDS-0820/HDS-1025

Vol. I
9-317

HDS-0820: 8 Bits
HDS-1025: 10 Bits
25ns Current Settling to 0.1%
10mA Current Out
Guaranteed Monotonicity Over Temperature
No External Parts Required
Reliable Hybrid Construction



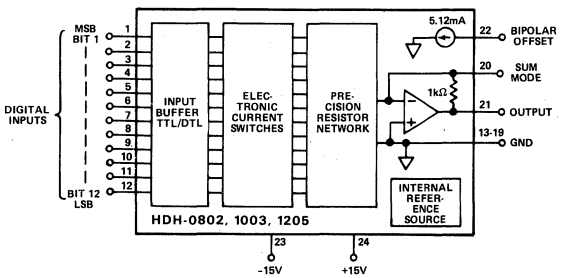
HDS-1240E

Vol. I
9-323

12 Bits of Resolution
12-Bit Settling Time to 40ns
Low Glitch Energy
ECL Compatible
Replacement for ADH-030, DA-4000, DAC397

Selection Guide
Digital-to-Analog Converters

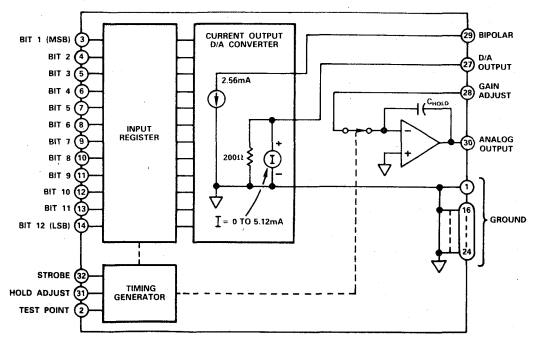
Video Speed Voltage Output D/A Converters



HDH SERIES

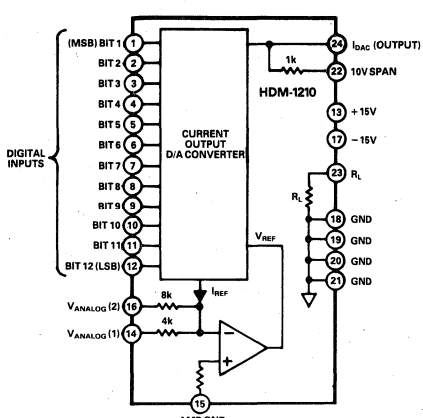
Page

200ns Voltage Settling to 0.1% Vol. I
10mA Current Out 9-317
Guaranteed Monotonicity Over Temperature
No External Parts Required
Reliable Hybrid Construction
HDH-0802
Resolution: 8 Bits
Settling Time: 200ns to 0.4%
HDH-1003
Resolution: 10 Bits
Settling Time: 300ns to 0.1%
HDH-1205
Resolution: 12 Bits
Settling Time: 500ns to 0.125%



HDD-1206

12 Bits of Resolution Vol. I
Registers, D/A, Amplifier in Single Hybrid 9-301
Deglitched Voltage Output
6MHz Update Rate



HDM-1210

Small Size: 24-Pin DIP Vol. I
12-Bit Multiplying Accuracy 9-315
Good Drive: 10.24mA
Highest Speed Available

Orientation
Digital-to-Analog Converters

FACTORS IN CHOOSING A D/A CONVERTER

In the current issue of this two-volume catalog, there are listed some 62 different families of digital-to-analog converters (DACs). If one were to consider all the variations, there would be more than 260 types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, and performance. Complete information on converters may be found in the 250-page book, ANALOG-DIGITAL CONVERSION NOTES, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood MA 02062.

FUNCTIONAL CHARACTERISTICS

The basic structure of all conventional D/A converters involves a network of precision resistors, a set of switches, and some form of level-shifting to adapt the switch drives to the specified logic levels. In addition, the device may contain output-conditioning circuitry, an output amplifier, a reference amplifier, an on-board reference, on-board buffer-registers (single- or dual-rank), configuration conditioning, and even high-voltage isolation.

Basic DAC

This form, which supplies a current, and consequently a small voltage across its internal impedance or an external low-impedance load, is used principally for high speed, for example, the 10ns HDS-0810E. Basic current-output DACs, such as AD566A, are inherently fast, but additional elements (such as an output op amp), furnished by the user to meet overall system specs, slow down the conversion. Some popular CMOS IC devices, such as the AD7523 and the AD7533, are quite simple (and correspondingly low in cost), but they usually require a buffering op amp.

While the basic DAC function is almost always linear, there are exceptions. For example, the AD7111 LOGDAC, which has linear two-quadrant analog response, has a digitally controlled exponential gain function, i.e., 0.375dB per bit; thus its gain at the input code 10000000 (binary 128) is -48dB (48 X 0.375), and the analog output swing for 10V p-p input is 0.04V p-p V_{IN} to $\exp -\left[\frac{0.375N}{20}\right]$.

Output Conditioning

The analog quantity that is the "output" of a DAC, representing the input digital data, may be a "gain" (multiplying DAC), a current, and/or a voltage. In order to obtain a substantial voltage output at low impedance, an op amp is required. It is generally provided on-board in modular and hybrid DACs (and in the monolithic AD558), but there are many ICs and other types that permit the user to choose an external op amp that will meet the particular needs of the application in stability, speed, and cost.

Almost all types of DACs provide one or more feedback resistors; they are matched to, and thermally track, resistances in the network, so that an external op amp, if used, will not require an external feedback resistor that might introduce tracking errors. If more than one feedback resistor is provided, a choice of analog output voltage ranges becomes available, e.g., 0–5V full-scale or 0–10V full-scale. If bipolar output-voltage ranges are specified, a bipolar-offset resistor is provided to subtract a half-scale value from the current flowing through the op amp summing point; it is usually derived from the DAC's reference (or analog) input to avoid additional tracking error. Multiplying DACs use an internal or external op amp for bipolar offset.

In order to avoid difficulties, the user must pay especial attention to the specified output polarity, its relationship to the reference (if external) and to the input digital code. This can be especially tricky if the output is bipolar and the input requires a complementary (negative-true) digital coding. Another such case is where a current-output DAC, specified for a particular output-voltage polarity when used with an inverting op amp, is used in a mode that develops an output voltage passively (without the op amp) across an external resistive load. In addition to polarity, in this case, the user should be aware of the output-compliance constraint and the specified resistive component of output impedance.

Reference Input

The reference may be specified as external or internal, fixed or variable, single-polarity or bipolar. If internal, it may be permanently connected (as in the AD561) or optionally connectible (as in the AD565A). If the DAC is a 4-quadrant multiplying type, the reference (or "analog input") is external, variable, and bipolar (e.g., AD7533, 7541, etc.) The user should check a converter's specifications to determine whether the full-scale accuracy specifications are overall or subdivided into a converter-gain spec and a reference spec.

Digital Data

There are a number of ways in which converters differ in regard to the input data: First, the *coding* must be appropriate (binary, offset-binary, two's-complement, BCD, arbitrary, etc.), and its sense should be understood (positive-true, negative-true). The *resolution* (number of bits) must be sufficient; in addition, the specifications must be checked to ascertain that the 2^n distinct binary input codes will not only be accepted, but that also they will (if necessary) correspond to 2^n output values in a monotonic progression at any temperature in the operating range, with sufficient accuracy. The *data levels* accepted by the converter must be checked (TTL, ECL, low-voltage CMOS, high-voltage CMOS), as must the input loading imposed by the converter, and the supply conditions under which the converter will respond to the data. Check the data notation (is the MSB Bit 1 or Bit (n-1)?)—misinterpretation can lead to connecting the data bits in backward order.

If *buffer registers* are desired, the converter should have an appropriate buffer configuration (for example, the AD558 and AD7226 have a set of TTL buffers', the AD667 and AD7548 have two ranks of buffering).

Controls

If the DAC has external digital controls—for example, register strobes— their drive levels, digital sense (true or false), loading, and timing must be considered. The function and use of con-

figuration controls (where present), such as serial/parallel, short-cycle, or chip-select decoding should be understood, and the appropriate ways of disabling them when not needed should be employed.

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog output signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specs should be employed. Any recommended external protection circuitry (e.g., Schottky diodes, to ensure that V_{CC} is never more than 0.4V above V_{DD} in the AD7522) should be planned for. In many cases separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between the grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

SPECIFICATIONS AND TERMS

Definitions of the performance specifications, and related information, are provided on the next few pages, in alphabetical order.

Accuracy, Absolute
Error of a D/A converter is the difference between the actual analog output and the output that is expected when a given digital code is applied to the converter. Sources of error include gain (calibration) error, zero error, linearity errors, and noise. Error is usually commensurate with resolution, i.e., less than $2^{-(n+1)}$, or "½ LSB" of full scale. However, accuracy may be much better than resolution in some applications; for example, a 4-bit reference supply having only 16 discrete digitally chosen levels would have a resolution of 1/16, but it might have an accuracy to within 0.01% of each ideal value.

Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

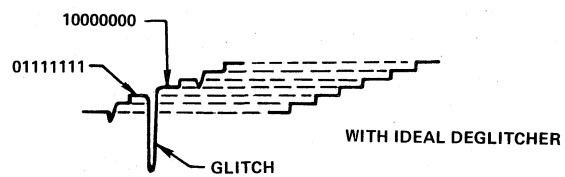
Accuracy, Relative
Relative accuracy error, expressed in %, ppm, or fractions of 1 LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristics) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated. Since the discrete analog output values corresponding to the digital input values ideally lie on a straight line, the relative-accuracy error of a linear DAC can be interpreted as a measure of nonlinearity (see *Linearity*).

Compliance-Voltage Range
For a current-output DAC, the maximum range of (output) terminal voltage for which the device will provide the specified current-output characteristics.

Common-Mode Rejection (CMR)
The ability of an amplifier to reject the effect of voltage applied to both input terminals simultaneously. Usually a logarithmic expression representing a "common-mode rejection ratio" e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 10^6:1 means that a 1V common-mode voltage passes through the device as though it were a differential input signal of 1 microvolt.

Common-Mode Voltage
An undesirable signal picked up in a circuit by both wires making up the circuit, with reference to an arbitrary "ground." Amplifiers differ in their ability to amplify a desired signal accurately in the presence of a common-mode voltage.

Deglitcher
As the input code to a DAC is increased or decreased by small changes, it passes through what is known as major and minor transitions. The most major transition is at half-scale, when the DAC switches around the MSB, and all switches change state, i.e., 01111111 to 10000000. If, at major transitions, the switches are faster (or slower) to switch off than on, this means that, for a short time, the D/A will give a zero (or full-scale) output, and then return to the required 1 LSB above the previous reading. Such large transient spikes which differ widely in amplitude and are extremely difficult to filter out, are commonly known as "glitches", hence, a deglitcher is a device which removes these glitches or reduces them to a set of small, uniform pulses. It normally consists of a fast sample-hold circuit, which holds the output constant until the switches reach equilibrium. Glitch energy is smallest in fast-switching DACs driven by fast logic gates that have little time-skew between 0-1 and 1-0 transitions.



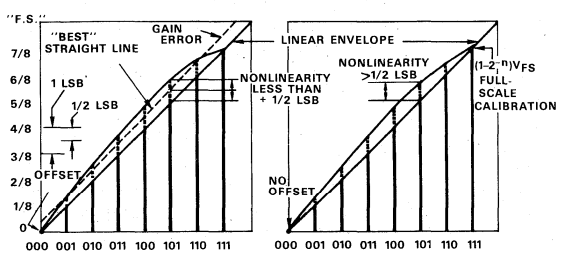
Feedthrough
Undesirable signal coupling around switches or other devices that are supposed to be turned off or provide isolation, e,g,. *feedthrough error* in a multiplying DAC. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

Four-Quadrant
In a multiplying DAC, "four quadrant" refers to the fact that both the reference signal and the number represented by the digital input may be of either positive or negative polarity. A four-quadrant multiplier is expected to obey the rules of multiplication for algebraic sign.

Gain
The "gain" of a converter is that analog scale-factor setting that provides the nominal conversion relationship, e.g., 10V span for a full-scale code change, in a fixed-reference converter. For fixed-reference converters where the use of the internal reference is optional, the converter gain and the reference may be specified separately. Gain- and zero-adjustment are discussed under *Zero*.

Least-Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the LSB is that bit that carries the smallest value, or weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost digit is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest analog change that can be resolved by an n-bit converter.

Linearity
Linearity error of a converter (also, *integral nonlinearity*, see *Linearity, Differential*), expressed in % or ppm of full-scale range, or (sub)multiples of 1 LSB, is a deviation of the analog values, in a plot of the measured conversion relationship, from a straight line. The straight line can be either a "best straight line", determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristics from this straight line; or it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated (sometimes referred to as "end-point" linearity). End-point linearity error is similar to *relative-accuracy* error.



a. ½LSB Nonlinearity Achieved By Arbitrary Location of "Best Straight Line".

b. Nonlinearity Reference is Straight Line Through End Points. Nonlinearity >½LSB for Curve of a.

Comparison of Linearity Criteria for 3-Bit D/A Converter. Straight Line Through End Points is Easier to Measure, Gives More-Conservative Specification.

For multiplying D/A converters, the *analog* linearity error, at a specified digital code, is defined in the same way as for multipliers, i.e., by deviation from a "best straight line" through the plot of the analog output-input response.

Linearity, Differential
Any two adjacent digital codes should result in measured output values that are exactly 1 LSB apart (2^{-n} of full scale for an n-bit converter). Any deviation of the measured "step" from the ideal difference is called *differential nonlinearity*, expressed in (sub)multiples of 1 LSB. It is an important specification, because a differential linearity error greater than 1 LSB can lead to non-monotonic response in a D/A converter and missed codes in an A/D converter (see *Differential Linearity* in the A/D converter section for an illustration).

Monotonic
A DAC is said to be monotonic if the output either increases or remains constant as the digital input increases, with the result that the output will always be a single-valued function of the input. The specification "monotonic" (over a given temperature range) is sometimes substituted for a *differential nonlinearity* specification, since differential nonlinearity less than 1 LSB is a sufficient condition for monotonic behavior.

Most-Significant Bit (MSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the MSB is that digit (or bit) that carries the largest value of weight. For example, in the natural-binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the leftmost "1" is the MSB, with a weight of 2^{n-1}, or 8 LSBs. Its analog weight, relative to a DAC's full-scale span, is ½. In bipolar DACs, the MSB indicates the polarity of the number represented by the rest of the bits.

Multiplying DAC
A multiplying DAC differs from a fixed-reference DAC in being designed to operate with varying (or ac) reference signals. The output signal of such a DAC is proportional to the product of the "reference" (i.e., analog input) voltage and the fractional equivalent of the digital input number (see also *four-quadrant*).

Noise, Peak and rms
Internally generated random noise is not a major factor in D/A converters, except at extreme resolutions (e.g., DAC1138) and dynamic ranges (AD7111). Random noise is characterized by rms specifications for a given bandwidth, or as a spectral density (current or voltage per root hertz); if the distribution is Gaussian, the probability of peak-to-peak values exceeding 7x the rms value is less than 0.1%.

Of much greater importance in DACs is interference in the form of high-amplitude low-energy (hence low-rms) spikes appearing at the DAC's output, caused by coupling of digital signals in a surprising variety of ways; they include coupling via stray capacitance, via power supplies, via inadequate ground systems, via feedthrough, and by glitch-generation. Their presence underscores the necessity for maximum application of the designer's art, including layout, shielding, guarding, grounding, bypassing, and deglitching.

Offset
For almost all bipolar converters (e.g., ±10-volt output), instead of actually generating negative currents to correspond to negative numbers, a unipolar DAC is used, and the output is offset by half full scale (1 MSB). For best results, this offset voltage or current is derived from the same reference supply that determines the gain of the converter.

This makes the zero point of the converter independent of thermal drift of the reference, because the ½ scale offset cancels the weight of the MSB at zero, independently of the amplitude of both.

Power-Supply Sensitivity
The sensitivity of a converter to changes in the power-supply voltages is normally expressed in terms of percent-of-full-scale change in analog output value (or fractions of 1 LSB) for a 1% dc change in the power supply, e.g., $0.05\%/\%\Delta V_S$). Power supply sensitivity may also be expressed in relation to a specified dc shift of supply voltage. A converter may be considered "good" if the change in reading at full scale does not exceed ±½ LSB for a 3% change in power supply. Even better specs are necessary for converters designed for battery operation.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit processing. All analog values within a given range of output (of a DAC) are represented by the same digital code, usually assigned to the nominal midrange value. For applications in which an analog continuum is to be restored, there is an inherent quantization uncertainty of ±½ LSB, due to limited resolution, in addition to the actual conversion errors. For applications in which discrete output levels are desired (e.g., digitally controlled power supplies or digitally controlled gains), this consideration is not relevant.

Resolution
An n-bit binary converter should be able to provide 2^n distinct and different analog output values corresponding to the set of n-bit binary words. A converter that satisfies this criterion is said to have a *resolution* of n bits. The smallest output change that can be resolved by a linear DAC is 2^{-n} of the full-scale span. However, a nonlinear device, such as the AD7111 LOGDAC has a logarithmic gain resolution of 0.375/88.5dB = 1:256dB, which corresponds to a gain increment of 4.25%/step, or 26,600:1.

Settling Time
The time required, following a prescribed data change, for the output of a DAC to reach and remain within a given fraction (usually ±½ LSB) of the final value. Typical prescribed changes are full-scale, 1 MSB, and 1 LSB at a major carry. Settling time of current-output DACs is quite fast. The major share of settling time of a voltage-output DAC is usually contributed by the settling time of the output op-amp circuit.

Slew Rate (or Slewing Rate)
Slew rate of a device or circuit is a limitation in the rate of change of output voltage, usually imposed by some basic circuit consideration, such as limited current to charge a capacitor. Amplifiers with slew rate of a few V/μs are common, and moderate in cost. Slew rates greater than about 75 volts/μs are usually seen only in more sophisticated (and expensive) devices. The output slewing speed of a voltage-output D/A converter is usually limited by the slew rate of the amplifier used at its output (if one is used).

Stability
Stability of a converter usually applies to the insensitivity of its characteristics to time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion of temperature coefficients in tables of specifications (see "Temperature Coefficient").

Staircase
A voltage or current, increasing in equal increments as a function of time and having the appearance of a staircase (in a time plot), generated by applying a pulse train to a counter, and the output of the counter to the input of a DAC.

A very simple A/D converter can be built by comparing a staircase from a DAC with the unknown analog input. When the DAC output exceeds the analog input by a fraction of 1 LSB, the count is stopped, and the code corresponding to the count is the digital output.

Switching Time
In a DAC, the switching time is the time it takes for the switch to change from one state to the other ("delay time" plus "rise time" from 10%-90%), but does not include settling time, e.g. to <½ LSB.

Temperature Coefficients
In general, temperature instabilities are expressed as %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero*.

Gain Tempco: Two factors principally affect converter gain stability with temperature.

a) In fixed-reference converters the reference source will vary with temperature. For example, the tempco of an AD581L is generally less than 5ppm/°C

b) The reference circuitry and switches may add another 3ppm/°C in good 12-bit converters (e.g. AD566K/T). High-resolution converters require much better tempcos for accuracy commensurate with the resolution.

Linearity Tempco: Sensitivity of linearity ("integral" and/or differential linearity) to temperature (in % FSR/°C or ppm FSR/°C) over the specified range. Monotonic behavior is achieved if the differential nonlinearity is less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a temperature range, and/or implied by a statement that the device is monotonic over the specified temperature range.

Offset Tempco: The temperature coefficient of the all-DAC-switches-off (minus full scale) point of a bipolar converter (in % FSR/°C or ppm FSR/°C) depends on three major factors:

a) The tempco of the reference source

b) The voltage zero-stability of the output amplifier

c) The tracking capability of the bipolar-offset resistors and the gain resistors

Unipolar Zero Tempco (in % FSR/°C or ppm FSR/°C): The temperature stability of a unipolar fixed-reference DAC is principally affected by current leakage (current-output DAC), and offset voltage and bias current of the output op-amp (voltage-output DAC).

Zero- and Gain-Adjustment Principles

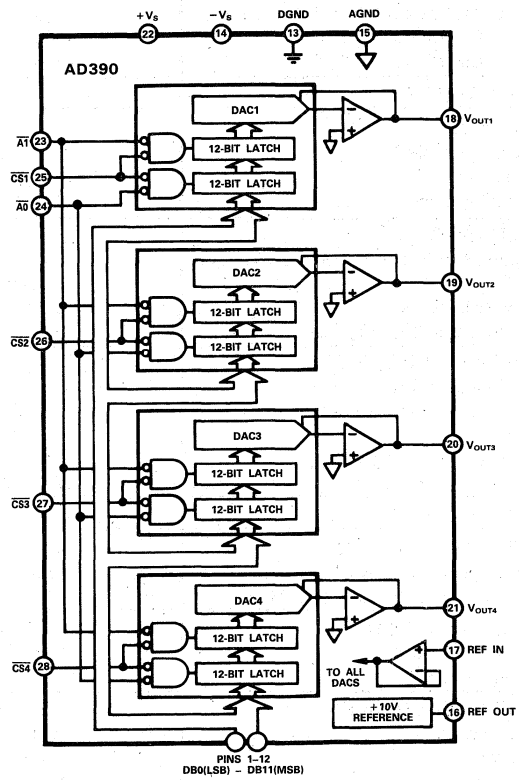
The output of a unipolar DAC is set to zero volts in the all-bits-off condition. The gain is set for F.S. $(1 - 2^{-n})$ with all bits on. The "zero" of an offset-binary bipolar DAC is set to -F.S. with all bits off, and the gain is set for +F.S. $(1 - 2^{-(n-1)})$ with all bits on. The data sheet instructions should be followed.

Quad 12-Bit Microprocessor-Compatible D/A Converter

AD390*

FEATURES
- **Four Complete 12-Bit DACs in One IC Package**
- **Linearity Error ±1/2LSB T_{min} – T_{max} (AD390K, T)**
- **Factory-Trimmed Gain and Offset**
- **Buffered Voltage Output**
- **Monotonicity Guaranteed Over Full Temperature Range**
- **Double-Buffered Data Latches**
- **Includes Reference and Buffer**
- **Fast Settling: 8μs max to ±1/2LSB**

AD390 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD390 contains four 12-bit high speed voltage-output digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit DAC chip which reduces chip count and provides high reliability. The AD390 is ideal for systems requiring digital control of many analog voltages where board space is at a premium. Such applications include automatic test equipment, process controllers, and vector-scan displays.

The AD390 is laser-trimmed to ±1/2LSB max nonlinearity (AD390KD, TD) and absolute accuracy of ±0.05 percent of full scale. The high initial accuracy is made possible by the use of thin-film scaling resistors on the monolithic DAC chips. The internal buried zener voltage reference provides excellent temperature drift characteristics (20ppm/°C) and an initial tolerance of ±0.03% maximum. The internal reference buffer allows a single common reference to be used for multiple AD390 devices in large systems.

The individual DACs are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control inputs and the $\overline{A0}$ and $\overline{A1}$ lines. These control signals permit the registers of the four DACs to be loaded sequentially and the outputs to be simultaneously updated.

The AD390 outputs are calibrated for a ±10V output range with positive-true offset binary input coding. A 0 to +10V version is available on special order.

The AD390 is packaged in a 28-lead ceramic package and is specified for operation over the 0 to +70°C and −55°C to +125°C temperature range.

***Covered by patent numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486 and other patents pending.**

PRODUCT HIGHLIGHTS

1. The AD390 offers a dramatic reduction in printed circuit board space requirements in systems using multiple DACs.
2. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
3. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 8 microseconds maximum.
4. An internal 10 volt reference is available or an external reference can be used. With an external reference, the AD390 gain TC is ±5ppm/°C maximum.
5. The proprietary monolithic DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
6. The 28-pin double-width hybrid package provides extremely high functional density. No external components or adjustments are required to provide the complete function.
7. The AD390SD and AD390TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

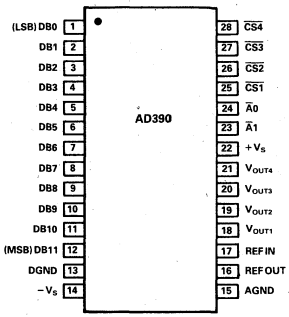
SPECIFICATIONS (T_A = +25°C, V_S = ±15V unless otherwise specified)

Model	AD390JD/SD MIN	AD390JD/SD TYP	AD390JD/SD MAX	AD390KD/TD MIN	AD390KD/TD TYP	AD390KD/TD MAX	UNITS
DATA INPUTS (Pins 1-12 and 23-28)[1]							
Except Pin 24 TTL or 5 Volt CMOS							
Input Voltage							
Bit ON (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
Bit OFF (Logic "0")			+0.8			+0.8	V
Input Current (Pin 24 is 3× Larger)							
Bit ON (Logic "1")		500	1200		500	1200	μA
Bit OFF (Logic "0")		150	400		150	400	μA
RESOLUTION			12			12	Bits
OUTPUT[2]							
Voltage Range[3]			±10			±10	V
Current			5			5	mA
Settling Time (to ±½LSB)		4	8		4	8	μs
ACCURACY							
Gain Error (w/ext. 10.000V reference)		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Linearity Error		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE DRIFT							
Gain (internal reference)			±40			±20	ppm/°C
(external reference)			±10			±5	ppm/°C
Zero			±10			±5	ppm/°C
Linearity Error $T_{min} - T_{max}$		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
CROSS TALK[5]		0.1			0.1		LSB
REFERENCE OUTPUT							
Voltage (without load)	9.997	10.000	10.003	9.997	10.000	10.003	V
Current (available for external use)	2.5	3.5		2.5	3.5		mA
REFERENCE INPUT							
Input Resistance		10^{10}			10^{10}		Ω
Voltage Range	5		11	5		11	V
POWER REQUIREMENTS							
Voltage[6]	±13.5	±15	±16.5	±13.5	±15	±16.5	V
Current							
$+V_S$		12	20		12	20	mA
$-V_S$		−75	−90		−75	−90	mA
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C
PACKAGE OPTION[7]		HY28A			HY28A		

NOTES
[1]Timing specifications appear in Table II.
[2]The AD390 outputs are guaranteed stable for load capacitances up to 300pF.
[3]±10V range is standard. A 0 to 10V version is available on special order. Consult the factory.
[4]FSR means Full Scale Range and is equal to 20V for a ±10V range.
[5]Crosstalk is defined as the change in any one output as a result of any other output being driven from −10V to +10V into a 2kΩ load.
[6]The AD390 can be used with supply voltage as low as ±11.4V, Figure 10.
[7]See Section 19 for package outline information.

Specifications subject to change without notice.

PIN CONFIGURATION
TOP VIEW



ABSOLUTE MAXIMUM RATINGS

$+V_S$ to DGND . . . . . 0 to +18V
$-V_S$ to DGND . . . . . 0 to −18V
Digital Inputs (Pins 1-12, 23-28) to DGND . . −1.0V to +7V
Ref In to DGND . . . . . $\pm V_S$
AGND to DGND . . . . . ±0.6V
Analog Outputs (Pins 16, 18-21)
. . . . . Indefinite Short to AGND or DGND
Momentary Short to $\pm V_S$

ORDERING GUIDE

Model	Temperature Range	Gain Error 25°C	Linearity Error $T_{min}-T_{max}$
AD390JD	0 to +70°C	±4LSB	±3/4LSB
AD390KD	0 to +70°C	±2LSB	±1/2LSB
AD390SD	−55°C to +125°C	±4LSB	±3/4LSB
AD390TD	−55°C to +125°C	±2LSB	±1/2LSB

Digital Circuit Details

DATA AND CONTROL SIGNAL FORMAT

The AD390 accepts 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$, $\overline{A0}$ and $\overline{A1}$ The input registers are double-buffered, allowing any register to be updated independently of the others. As detailed in Table I, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. The first rank register of a given DAC is loaded by bringing the appropriate chip select and $\overline{A0}$ both low. The second rank register of any DAC can then be loaded by bringing the appropriate chip select $\overline{A1}$ both low. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident with $\overline{A1}$ low, all four DAC outputs will be updated to the value in the corresponding first rank register. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

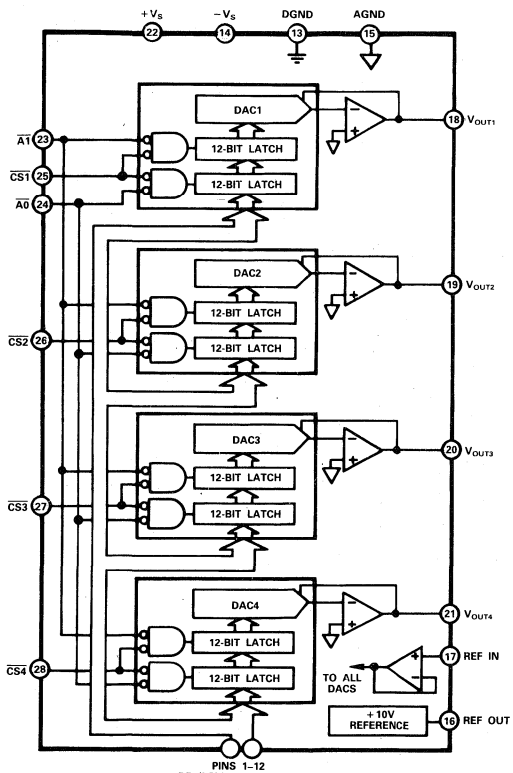


Figure 1. AD390 Functional Block Diagram

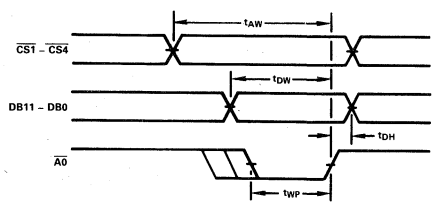
$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{A1}$	$\overline{A0}$	Operation
1	1	1	1	X	X	No Operation
X	X	X	X	1	1	No Operation
0	1	1	1	1	0	Enable 1st rank of DAC 1
1	0	1	1	1	0	Enable 1st rank of DAC 2
1	1	0	1	1	0	Enable 1st rank of DAC 3
1	1	1	0	1	0	Enable 1st rank of DAC 4
0	1	1	1	0	1	Load DAC 1 second rank from first rank
1	0	1	1	0	1	Load DAC 2 second rank from first rank
1	1	0	1	0	1	Load DAC 3 second rank from first rank
1	1	1	0	0	1	Load DAC 4 second rank from first rank
0	0	0	0	0	0	All latches transparent

Table I. AD390 Truth Table

TIMING

The AD390 control signal timing is fairly straightforward. $\overline{A0}$, $\overline{A1}$ and $\overline{CS1}$-$\overline{CS4}$ must be concurrently valid for at least 100ns for a desired operation to occur. When loading data from a bus into the first rank register, the data inputs must be stable for at least 50ns before any control signal returns high. Data can change immediately after the control signals are inactive. When loading the second rank registers from the first rank, it is possible to exercise the chip select inputs at the same time as $\overline{A1}$. DAC settling time is measured from the falling edge of whichever control signal last becomes valid.

WRITE CYCLE #1
(Load First Rank from Data Bus; $\overline{A1}$ = 1)



WRITE CYCLE #2
(Load Second Rank from First Rank; $\overline{A0}$ = 1)

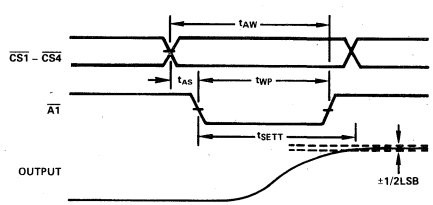


Figure 2. Timing Diagrams

Symbol	Parameter	Min	Typ	Max	Units
t_{AW}	$\overline{CS1}$-4 Valid before $\overline{A0}$ Rising Edge	100			ns
t_{WP}	$\overline{A0}$, $\overline{A1}$ Low Time	100			ns
t_{DW}	DB11-DB0 valid before $\overline{A0}$ Rising Edge	50			ns
t_{DH}	DB11-DB0 valid after $\overline{A0}$ Rising Edge	0			ns
t_{AS}	$\overline{CS1}$-4 valid before $\overline{A1}$ Low	0			ns
t_{SETT}	Output Voltage Settling Time		4	8	µs

Table II. AD390 Timing Specifications

INTERFACING THE AD390 TO MICROPROCESSORS

The AD390 control logic provides simple interface to microprocessors. The latches are fast enough to operate with even the fastest processors.

16-Bit Processors

The AD390 is a 12-bit resolution DAC system and is easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 3, the AD390 second rank registers are made transparent by hard-wiring $\overline{A1}$ low. A system $\overline{WR}$ signal is used to drive the $\overline{A0}$ control input and a 74LS138 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In this circuit, only one DAC at a time may be updated. If simultaneous update of all four DACs is required, a slightly different addressing scheme is used. The circuit shown in Figure 4 allows selection of either register of any DAC at the expense of larger memory space requirements. In this circuit, address lines A0 through A3 each select a single DAC of the four contained in the AD390. The use of a separate address line for each DAC allows several DACs to be accessed

simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address. Selection of first rank or second rank register for any DAC is done by using two additional address bits. The AD390 thus occupies a block of 64 memory word locations but offers considerable flexibility in DAC updating.

In this addressing scheme, the A5 and A4 lines divide the 64 locations into 4 blocks. When both A5 and A4 are high, no operation occurs. When A5 and A4 are both low, data written into any one of the DACs (selected by A3-A0) will immediately update that analog output. In the address block where A4 is low and A5 is high, data is written into the first rank register of the selected DAC (or DACs). When A5 is low and A4 is high, data previously written into the first rank register of the selected DAC is transferred to the second rank register, which updates the analog output. It is particularly useful to perform a $\overline{WR}$ operation with A5 low, A4 high, and A3 through A0 all low (base address plus 32) since this action will cause all four DAC outputs to be simultaneously updated to the values previously written into the first rank registers.

In both addressing schemes shown, A0 represents the least significant *word address* bit. In most 16-bit systems this will be the A1 address line. Data may reside in either the 12MSBs (left-justified) or the lower 12 bits (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

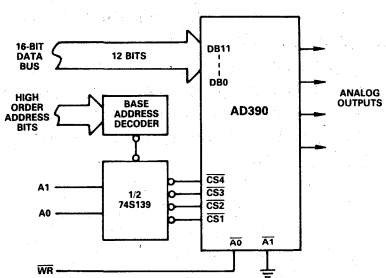


Figure 3. AD390–16-Bit Bus Interface

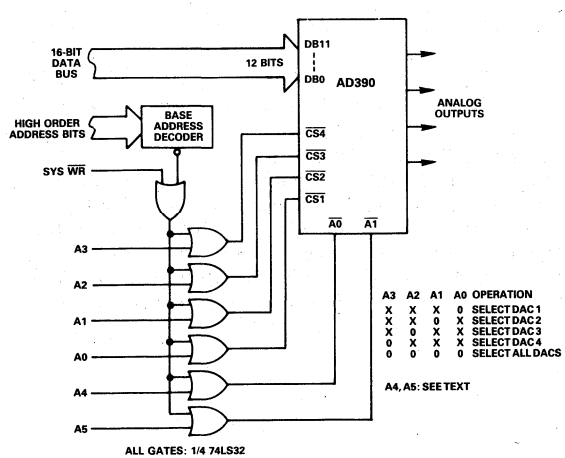
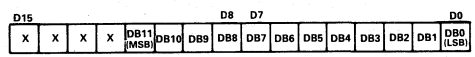


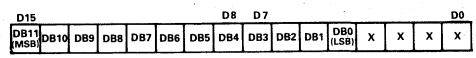
Figure 4. Alternate 16-Bit Bus Interface

8-Bit Processors

Since the AD390 is designed to accept data in 12-bit words, an external latch is required in order to interface with 8-bit buses. Thus each DAC in the AD390 occupies 2 memory locations. The choice of data format is similar to the choice in the 16-bit bus interface. The data can either be right-justified (one byte contains the 8LSBs and another the 4MSBs in the bottom half of the byte) or left-justified (where one byte contains the 8MSBs and another the 4LSBs in the top half of the byte). The addressing scheme illustrated in Figure 6 allows 12-bit data to be sent to the first rank register of any DAC in a right-justified format. The first rank register of DAC occupies two memory locations–a write to the even (A0 low) address stores the 4MSBs of the DAC data in a 74LS173 quad latch. When the 8LSBs are written to the odd address (A0 = 1), the eight bits present on the data bus and the four bits held in the 74LS173 are strobed into the first rank register of the selected DAC. Address bits A1 through A4 select the DAC to be addressed, while A6 and A5 enable either the first or second rank register (or both) as in the 16-bit interface of Figure 4.



a. Right-Justified Data ($0 \le D \le 4095$); $V_{OUT} = -10V + (4.883mV \times D)$.



b. Left-Justified Data $\left(0 \le D \le \frac{65520}{65536}\right)$; $V_{OUT} = -10V + (20V \times D)$

Figure 5. 12-Bit Data Formats for 16-Bit Bus

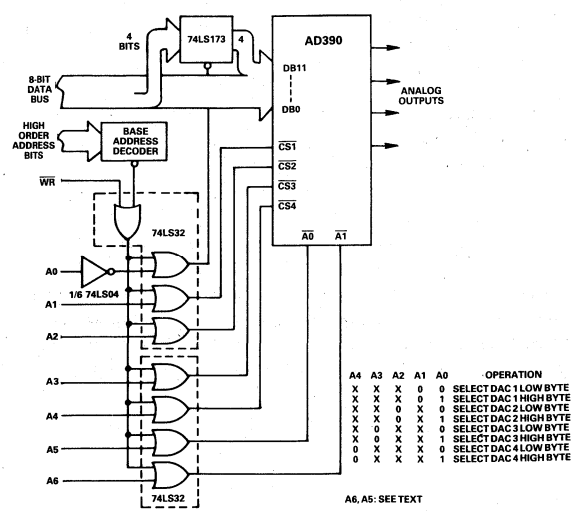


Figure 6. AD390–8-Bit Bus Interface Connections

Analog Circuit Details

REFERENCE CONNECTIONS

The AD390 is equipped with a precision internal reference voltage of 10.00 volts, trimmed to within ±3 millivolts. This reference is available for external use and can typically supply up to 3.5 milliamps of output current. In normal operation, this reference is connected to pin 17 (REF IN), which establishes the ±10 volt output scale. The internal reference is sufficiently accurate for most applications, however, if a master system reference is available, or if a range other than ±10V (±10.24V, for example) is desired, an external reference may be used. It is recommended that the reference used with the AD390 be at least 5 volts and at most 11 volts to preserve specified linearity.

Digital Input Code	Analog Output Voltage	
0000 0000 0000	−10.000V	−Full Scale
0100 0000 0000	−5.000V	−1/2 Scale
1000 0000 0000	0.000V	Zero
1000 0000 0001	+4.88mV	+1LSB
1100 0000 0000	+5.000V	+1/2 Scale
1111 1111 1111	+9.9951V	+Full Scale −1LSB

Table III. AD390 Analog Output vs. Digital Input (±V Scale)

GROUNDING RULES

The AD390 includes two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 13) and AGND (pin 15). The DGND pin is the return for the supply currents of the AD390, and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the digital circuitry which drives the AD390.

Pin 15, AGND, is the high quality analog ground connection. This pin should serve as the reference point for all analog circuitry which follows the AD390. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 15 as shown in Figure 7.

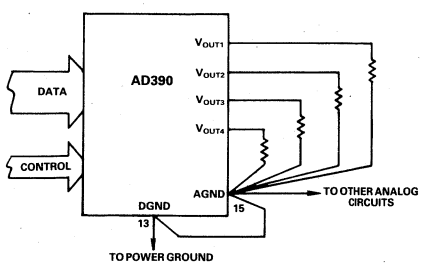


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the AD390 outputs are accurately developed between the output pin and pin 15 (AGND), delivering these signals to remote loads can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD390 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

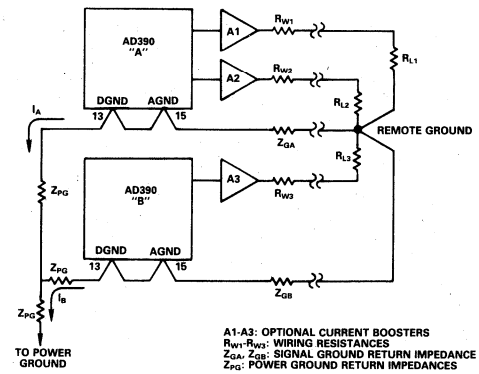


Figure 8. Grounding Errors in Multiple-AD390 Systems

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

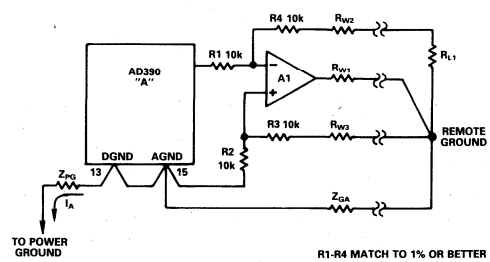


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

POWER SUPPLY DECOUPLING

The power supplies used with the AD390 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD390 supply pins and the load ground (ideally the AGND pin). If an output booster is used, its supplies should also be decoupled to the load ground.

OPERATION FROM ±12 VOLT SUPPLIES

The AD390 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB). The required 8.192V reference can be derived from a precision, low TC divider from the internal +10.000V reference. The only restriction is that the total load resistance presented to the +10.000V reference output must be at least 10kΩ for −55°C to +125°C temperature range 12 volt applications. Figure 10 shows a suggested circuit to set up a ±8.192V output range. Multiple AD390 units can share the same resistive divider-generated reference since the REF IN terminal is very high impedance.

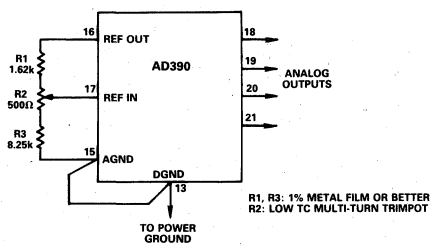


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

IMPROVING FULL-SCALE STABILITY

In large systems using multiple AD390s, it may be desirable for all devices to share a common reference. While it is possible to use the reference output for one device to provide a reference for all devices, use of an external precision reference can greatly improve system accuracy and temperature stability. The external reference should be at least +5V and at most +11V to preserve DAC linearity.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C, compared with the 10 to 20ppm/°C drift of the AD390 internal reference. The combination of the AD2710LN and AD390KD shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

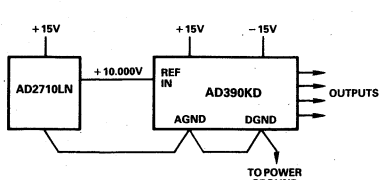
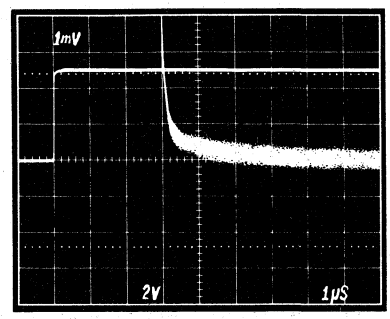


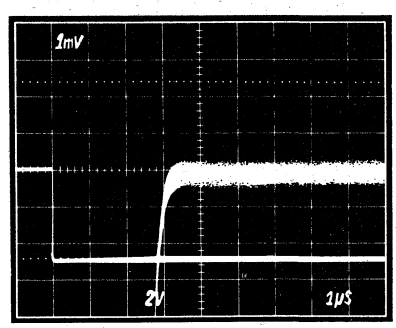
Figure 11. Low Drift AD390 Configuration

OUTPUT CURRENT BOOSTING

The output amplifiers used in the AD390 are capable of supplying a ±10 volt swing into a resistive load of 2kΩ or greater. Stability is guaranteed for load capacitance up to 300pF. Larger load capacitance may cause severe overshoot and possible oscillation. The settling characteristic of the AD390 output amplifier is shown in Figure 12.



a. All Bits OFF-to-ON



b. All Bits ON-to-OFF

Figure 12. AD390 Settling Characteristic

In many applications, including automatic test equipment, the load presented to the AD390 may be less than 2kΩ or include large capacitance. In such cases, it is advisable to use a buffer amplifier capable of delivering rated output to the most severe load anticipated. The AD382, for example, can supply ±10V into a 200Ω load and the AD3554 is suitable for load resistances down to 100Ω. In applications where errors due to output boosting must be minimized, the composite amplifier shown in Figure 13 provides excellent dc stability as well as 100mA output drive capability.

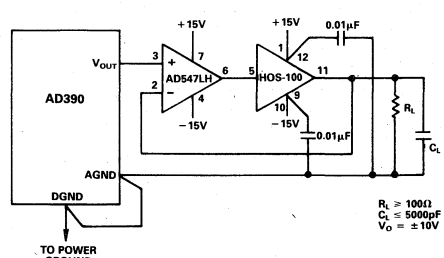


Figure 13. Composite Amplifier for Increased Output Drive

APPLICATIONS

The functional density of the AD390 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD390 in a fraction of the space which would be needed if separate DACs were used.

PROGRAMMABLE WINDOW COMPARATOR

The AD390 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD390.

In the circuit of Figure 14 two AD311 voltage comparators are used with an AD390 to test the output of a 5 volt power supply regulator. The AD390 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD390 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

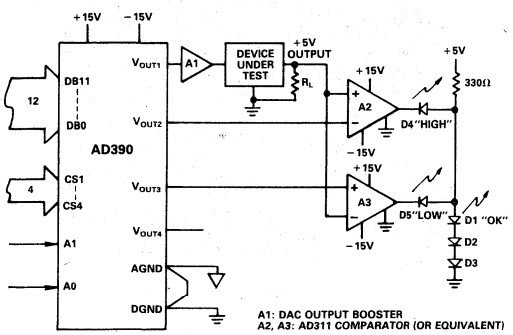


Figure 14. Programmable Window Comparator Used In Power Supply Testing

USING THE AD390 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD390 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD390 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 15. The AD311 comparator compares the unknown input voltage to one of the AD390 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 10 microseconds, resulting in 12-bit successive approximation conversion in under 120 microseconds. The benefit of the AD390 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD390 and the comparator).

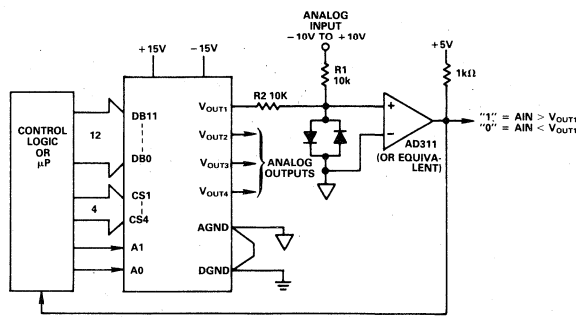


Figure 15. Using One AD390 Output for A/D Conversion

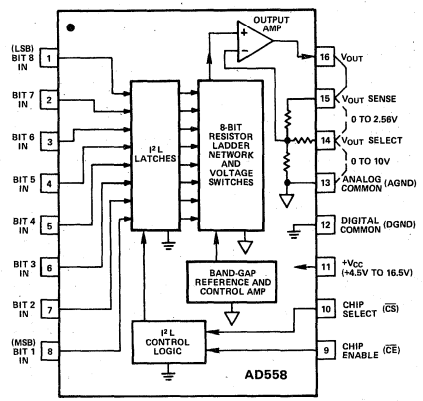
DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

AD558*

FEATURES

- Complete 8-Bit DAC
- Voltage Output — 2 Calibrated Ranges
- Internal Precision Band-Gap Reference
- Single-Supply Operation: +5V to +15V
- Full Microprocessor Interface
- Fast: 1μs Voltage Settling to ±1/2LSB
- Low Power: 75mW
- No User Trims
- Guaranteed Monotonic Over Temperature
- All Errors Specified T_{min} to T_{max}
- Small 16-Pin DIP Package
- Single Laser-Wafer-Trimmed Chip for Hybrids
- Low Cost

AD558 FUNCTIONAL BLOCK DIAGRAM



TO-116

PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for −55°C to +125°C operation.

*Covered by U.S. Patent Nos. 3,887,863; 3,685,045; 4,323,795; Patents Pending. DACPORT is a trademark of Analog Devices, Inc.

PRODUCT HIGHLIGHTS

1. The 8-bit I^2L input register and fully microprocessor-compatible control logic allow the AD558 to be directly connected to 8- or 16-bit data buses and operated with standard control signals. The latch may be disabled for direct DAC interfacing.
2. The laser-trimmed on-chip SiCr thin-film resistors are calibrated for absolute accuracy and linearity at the factory. Therefore, no user trims are necessary for full rated accuracy over the operating temperature range.
3. The inclusion of a precision low-voltage band-gap reference eliminates the need to specify and apply a separate reference source.
4. The voltage-switching structure of the AD558 DAC section along with a high-speed output amplifier and laser-trimmed resistors give the user a choice of 0V to +2.56V or 0V to +10V output ranges, selectable by pin-strapping. Circuitry is internally compensated for minimum settling time on both ranges; typically settling to ±1/2LSB for a full-scale 2.55 volt step in 800ns.
5. The AD558 is designed and specified to operate from a single +4.5V to +16.5V power supply.
6. Low digital input currents, 100μA max, minimize bus loading. Input thresholds are TTL/low voltage CMOS compatible over the entire operating V_{CC} range.

SPECIFICATIONS (@ T_A = +25°C, V_{CC} = +5V to +15V unless otherwise specified)

Model	AD558J			AD558K			AD558S			AD558T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			8			8	Bits
RELATIVE ACCURACY[1]													
0 to +70°C			±1/2			±1/4			±1/2			±1/4	LSB
−55°C to +125°C									±3/4			±3/8	LSB
OUTPUT													
Ranges[2]		0 to +2.56			0 to +2.56			0 to +2.56			0 to +2.56		V
		0 to +10			0 to +10			0 to +10			0 to +10		V
Current Source	+5			+5			+5			+5			mA
Sink		Internal Passive Pull-Down to Ground[3]			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground			Internal Passive Pull-Down to Ground		
OUTPUT SETTLING TIME[4]													
0 to 2.56 Volt Range		0.8	1.5		0.8	1.5		0.8	1.5		0.8	1.5	µs
0 to 10 Volt Range[3]		2.0	3.0		2.0	3.0		2.0	3.0		2.0	3.0	µs
FULL SCALE ACCURACY[5]													
@25°C			±1.5			±0.5			±1.5			±0.5	LSB
T_{min} to T_{max}			±2.5			±1			±2.5			±1	LSB
ZERO ERROR													
@25°C			±1			±1/2			±1			±1/2	LSB
T_{min} to T_{max}			±2			±1			±2			±1	LSB
MONOTONICITY[6]													
T_{min} to T_{max}		Guaranteed			Guaranteed			Guaranteed			Guaranteed		
DIGITAL INPUTS													
T_{min} to T_{max}													
Input Current			±100			±100			±100			100	µA
Data Inputs, Voltage													
Bit On – Logic "1"	2.0			2.0			2.0			2.0			V
Bit On – Logic "0"	0		0.8	0			0			0			V
Control Inputs, Voltage													
On – Logic "1"	2.0			2.0			2.0			2.0			V
On – Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
Input Capacitance		4			4			4			4		pF
TIMING[7]													
T_{min} to T_{max}													
t_W (Strobe Pulse Width)	150			150			150			150			ns
t_{DH} (Data Hold Time)	10			10			10			10			ns
t_{DS} (Data Set-Up Time)	200			200			200			200			ns
POWER SUPPLY													
Operating Voltage Range (V_{CC})													
2.56 Volt Range	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	+4.5		+16.5	V
10 Volt Range	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	V
Current (I_{CC})		15	25		15	25		15	25		15	25	mA
Rejection Ratio			0.03			0.03			0.03			0.03	%/%
POWER DISSIPATION, V_{CC} = 5V		75	125		75	125		75	125		75	125	mW
V_{CC} = 15V		225	375		225	375		225	375		225	375	mW
OPERATING TEMPERATURE RANGE	0		+70	0		+70	−55		+125	−55		+125	°C

NOTES
[1]Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.
[2]Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.
[3]Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.
[4]Settling time is specified for a positive-going full-scale step to ±1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.
[5]The full range output voltage for the 2.56 range is 2.55V and is guaranteed with a +5V supply, for the 10V range, it is 9.960V guaranteed with a +15V supply.
[6]A monotonic converter has a maximum differential linearity error of ±1LSB.
[7]See Figure 7.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Ground . . . . . .0V to +18V
Digital Inputs (Pins 1-10) . . . . . 0 to +7.0V
V_{OUT} . . . . . Indefinite Short to Ground
Momentary Short to V_{CC}
Power Dissipation 450mW
Storage Temperature Range
N (Plastic) Package . . . . . -25°C to +100°C
D (Ceramic) Package . . . . . -55°C to +150°C
Lead Temperature (soldering, 10 second). . . . . 300°C
Thermal Resistance
Junction to Ambient/Junction to Case
D (Ceramic) Package . . . . . 100/30°C/W
N (Plastic) Package . . . . . 140/55°C/W

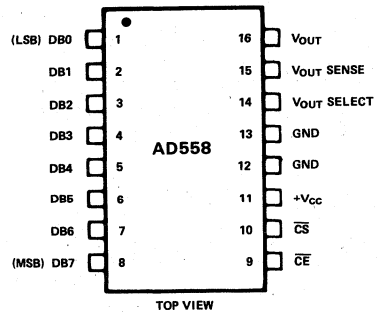


Figure 1. AD558 Pin Configuration

AD558 ORDERING GUIDE

Model	Package	Temperature	Relative Accuracy Error Max T_{min} to T_{max}	Full-Scale Error, Max T_{min} to T_{max}	Package Style[1]
AD558JN	Plastic	0 to +70°C	±1/2LSB	±2.5LSB	N16A
AD558KN	Plastic	0 to +70°C	±1/4LSB	±1LSB	N16A
AD558JD	Ceramic	0 to +70°C	±1/2LSB	±2.5LSB	D16A
AD558KD	Ceramic	0 to +70°C	±1/4LSB	±1LSB	D16A
AD558SD	Ceramic	−55°C to +125°C	±3/4LSB	±2.5LSB	D16A
AD558TD	Ceramic	−55°C to +125°C	±3/8LSB	±1LSB	D16A

[1] See Section 19 for package outline information.

CIRCUIT DESCRIPTION

The AD558 consists of four major functional blocks, fabricated on a single monolithic chip (see Figure 2). The main D to A Converter section uses eight equally-weighted laser trimmed current sources switched into a silicon-chromium thin-film R/2R resistor ladder network to give a direct but unbuffered 0mV to 400mV output range. The transistors that form the DAC switches are PNPs; this allows direct positive-voltage logic interface and a zero-based output range.

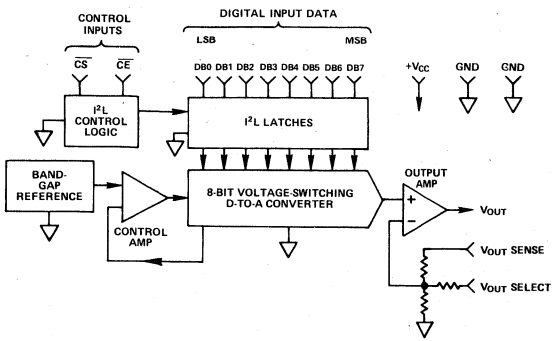


Figure 2. AD558 Functional Block Diagram

The high-speed output buffer amplifier is operated in the non-inverting mode with gain determined by the user-connections at the output range select pin. The gain-setting application resistors are thin-film laser-trimmed to match and track the DAC resistors and to assure precise initial calibration of the two output ranges, 0V to 2.56V and 0V to 10V. The amplifier output stage is an NPN transistor with passive pull-down for zero-based output capability with a single power supply.

The internal precision voltage reference is of the patented band-gap type. This design produces a reference voltage of 1.2 volts and thus, unlike 6.3 volt temperature-compensated zeners, may be operated from a single, low-voltage logic power supply. The microprocessor interface logic consists of an 8-bit data latch and control circuitry. Low-power, small geometry and high-speed are advantages of the I^2L design as applied to this section. I^2L is bipolar process compatible so that the performance of the analog sections need not be compromised to provide on-chip logic capabilities. The control logic allows the latches to be operated from a decoded microprocessor address and write signal. If the application does not involve a μP or data bus, wiring $\overline{CS}$ and $\overline{CE}$ to ground renders the latches "transparent" for direct DAC access.

Digital Input Code			Output Voltage	
Binary	**Hexadecimal**	**Decimal**	**2.56V Range**	**10.00V Range**
0000 0000	00	0	0	0
0000 0001	01	1	0.010V	0.039V
0000 0010	02	2	0.020V	0.078V
0000 1111	0F	15	0.150V	0.586V
0001 0000	10	16	0.160V	0.625V
0111 1111	7F	127	1.270V	4.961V
1000 0000	80	128	1.280V	5.000V
1100 0000	C0	192	1.920V	7.500V
1111 1111	FF	255	2.55V	9.961V

CONNECTING THE AD558

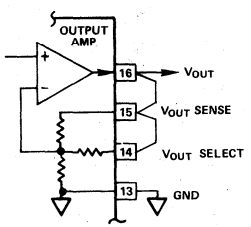
The AD558 has been configured for ease of application. All reference, output amplifier and logic connections are made internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. The only connection decision that must be made by the user is a single jumper to select output voltage range. Clean circuit-board layout is facilitated by isolating all digital bit inputs on one side of the package; analog outputs are on the opposite side.

Figure 3 shows the two alternative output range connections. The 0V to 2.56V range may be selected for use with any power supply between +4.5V and +16.5V. The 0V to 10V range requires a power supply of +11.4V to +16.5V.

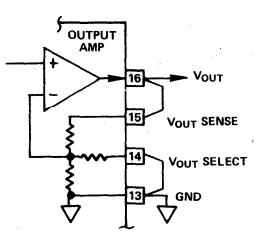
Because of its precise factory calibration, the AD558 is intended to be operated without user trims for gain and offset; therefore no provisions have been made for such user-trims. If a small increase in scale is required, however, it may be accomplished by slightly altering the effective gain of the output buffer. A resistor in series with V_{OUT} SENSE will increase the output range.

For example if a 0V to 10.24V output range is desired (40mV = 1LSB), a nominal resistance of 850Ω is required. It must be remembered that, although the internal resistors all ratio-match and track, the *absolute* tolerance of these resistors is typically ±20% and the *absolute* TC is typically −50ppm/°C (0 to −100ppm/°C). That must be considered when re-scaling is performed. Figure 4 shows the recommended circuitry for a full-scale output range of 10.24 volts. Internal resistance values shown are nominal.

NOTE: Decreasing the scale by putting a resistor in series with GND will not work properly due to the code-dependent currents in GND. Adjusting offset by injecting dc at GND is not recommended for the same reason.



a. 0V to 2.56V Output Range



b. 0V to 10V Output Range

Figure 3. Connection Diagrams

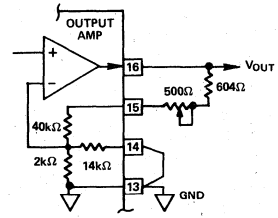


Figure 4. 10.24V Full-Scale Connection

GROUNDING AND BYPASSING*

All precision converter products require careful application of good grounding practices to maintain full rated performance. Because the AD558 is intended for application in microcomputer systems where digital noise is prevalent, special care must be taken to assure that its inherent precision is realized.

The AD558 has two ground (common) pins; this minimizes ground drops and noise in the analog signal path. Figure 5 shows how the ground connections should be made.

It is often advisable to maintain separate analog and digital grounds throughout a complete system, tying them common in one place only. If the common tie-point is remote and accidental disconnection of that one common tie-point occurs due to card removal with power on, a large differential voltage between the two commons could develop. To protect devices that interface to both digital and analog parts of the system, such as the AD558, it is recommended that common ground tie-points should be provided at *each* such device. If only one system ground can be connected directly to the AD558, it is recommended that analog common be selected.

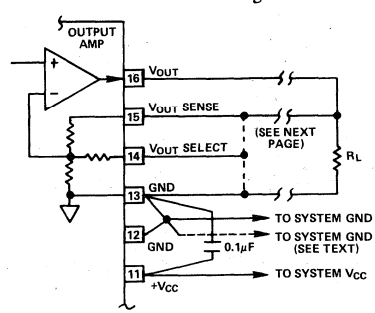


Figure 5. Recommended Grounding and Bypassing

POWER SUPPLY CONSIDERATIONS

The AD558 is designed to operate from a single positive power supply voltage. Specified performance is achieved for any supply voltage between +4.5V and +16.5V. This makes the AD558 ideal for battery-operated, portable, automotive or digital main-frame applications.

The only consideration in selecting a supply voltage is that, in order to be able to use the 0V to 10V output range, the power supply voltage must be between +11.4V and +16.5V. If, however, the 0V to 2.56V range is to be used, power consumption will be minimized by utilizing the lowest available supply voltage (above +4.5V).

*For additional insight, "An IC Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right For A Change", is available at no charge from any Analog Devices Sales Office.

TIMING AND CONTROL

The AD558 has data input latches that simplify interface to 8- and 16-bit data buses. These latches are controlled by Chip Enable ($\overline{CE}$) and Chip Select ($\overline{CS}$) inputs, pins 9 and 10 respectively. $\overline{CE}$ and $\overline{CS}$ are internally "NORed" so that the latches transmit input data to the DAC section when both $\overline{CE}$ and $\overline{CS}$ are at Logic "0". If the application does not involve a data bus, a "00" condition allows for direct operation of the DAC. When either $\overline{CE}$ or $\overline{CS}$ go to Logic "1", the input data is latched into the registers and held until both $\overline{CE}$ and $\overline{CS}$ return to "0". (Unused $\overline{CE}$ or $\overline{CS}$ inputs should be tied to ground.) The truth table is given in Table I. The logic function is also shown in Figure 6.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	∫	0	0	latching
1	∫	0	1	latching
0	0	∫	0	latching
1	0	∫	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter
∫ = Logic Threshold at Positive-Going Transition

Table I. AD558 Control Logic Truth Table

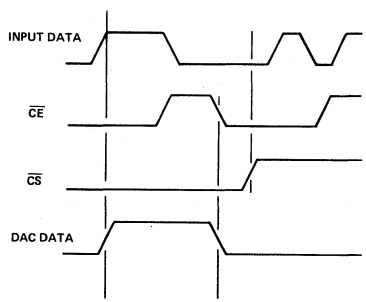
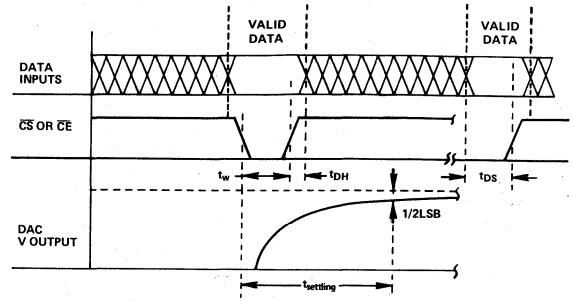


Figure 6. AD558 Control Logic Function

Figure 7 shows the timing for the data and control signals; $\overline{CE}$ and $\overline{CS}$ are identical in timing as well as in function.

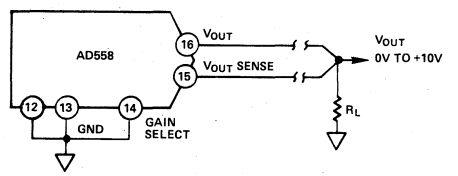


t_W = STROBE PULSE WIDTH = 150ns MIN
t_{DH} = DATA HOLD TIME = 10ns MIN
t_{DS} = DATA SETUP TIME = 200ns MIN
$t_{settling}$ = DAC OUTPUT SETTLING TIME TO ±1/2LSB

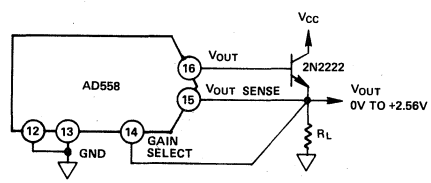
Figure 7. AD558 Timing

USE OF V_{OUT} SENSE

Separate access to the feedback resistor of the output amplifier allows additional application versatility. Figure 8 shows how I X R drops in long lines to remote loads may be cancelled by putting the drops "inside the loop". Figure 8b shows how the separate sense may be used to provide a higher output current by feeding back around a simple current booster.



a. Compensation for I x R Drops in Output Lines



b. Output Current Booster

Figure 8. Use of V_{OUT} Sense

OPTIMIZING SETTLING TIME

In order to provide single-supply operation and zero-based output voltage ranges, the AD558 output stage has a passive "pull-down" to ground. As a result, settling time for negative-going output steps may be longer than for positive-going output steps. The relative difference depends on load resistance and capacitance. If a negative power supply is available, the negative-going settling time may be improved by adding a pull-down resistor from the output to the negative supply as shown in Figure 9. The value of the resistor should be such that, at zero voltage out, current through that resistor is 0.5mA max.

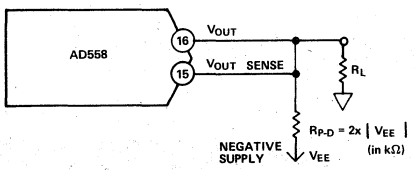


Figure 9. Improved Settling Time

BIPOLAR OUTPUT RANGES

The AD558 was designed for operation from a single power supply and is thus capable of providing only unipolar (0V to +2.56 and 0V to 10V) output ranges. If a negative supply is available, bipolar output ranges may be achieved by suitable output offsetting and scaling. Figure 10 shows how a ±1.28 volt output range may be achieved when a -5 volt power supply is available. The offset is provided by the AD589 precision 1.2 volt reference which will operate from a +5 volt supply. The AD544 output amplifier can provide the necessary ±1.28 volt output swing from ±5 volt supplies. Coding is complementary offset binary.

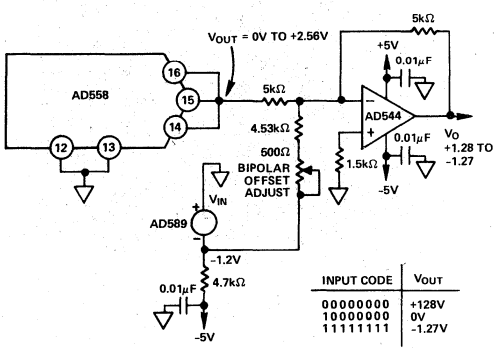
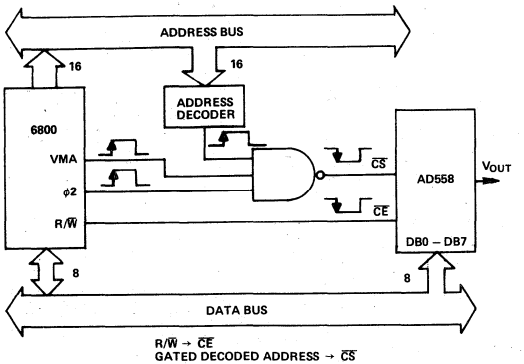


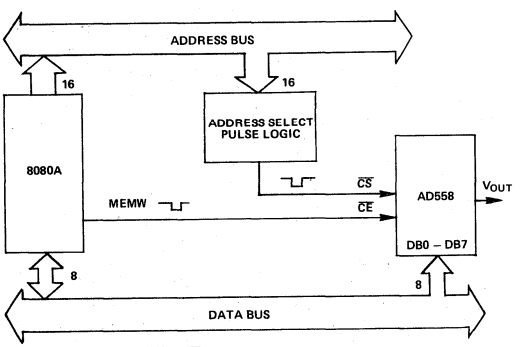
Figure 10. Bipolar Operation of AD558 from ±5V Supplies

INTERFACING THE AD558 TO MICROPROCESSOR DATA BUSES*

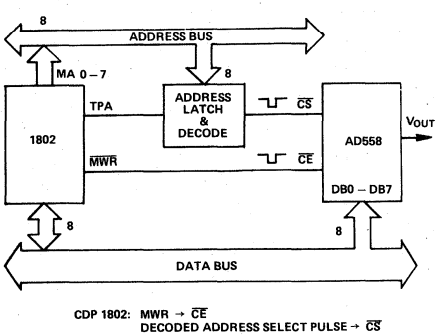
The AD558 is configured to act like a "write only" location in memory that may be made to coincide with a read only memory location or with a RAM location. The latter case allows data previously written into the DAC to be read back later via the RAM. Address decoding is partially complete for either ROM or RAM. Figure 11 shows interfaces for three popular microprocessor systems.



a. 6800/AD558 Interface



b. 8080A/AD558 Interface



c. 1802/AD558 Interface

Figure 11. Interfacing the AD558 Microprocessors

*The microprocessor-interface capabilities of the AD558 are extensive. A comprehensive application note, "Interfacing the AD558 DACPORT™ to Microprocessors" is available from any Analog Devices Sales Office upon request, free of charge.

AD558 Performance (typical @ +25°C, V_{CC} = +5V to +15V unless otherwise noted)

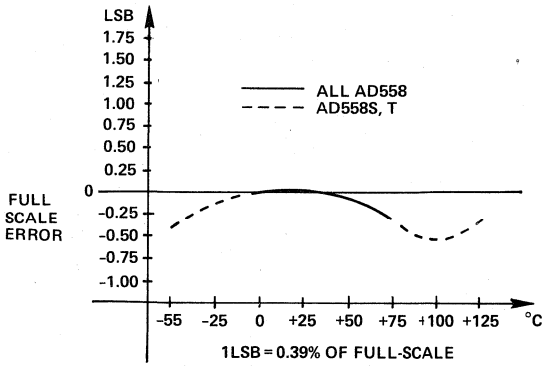


Figure 12. Full Scale Accuracy vs. Temperature Performance of AD558

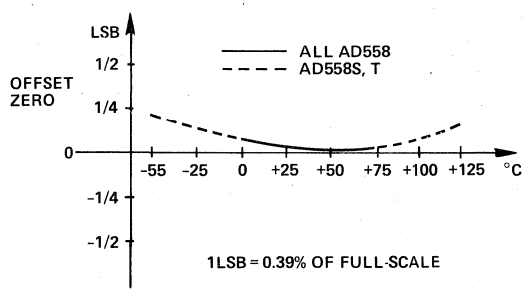


Figure 13. Zero Drift vs. Temperature Performance of AD558

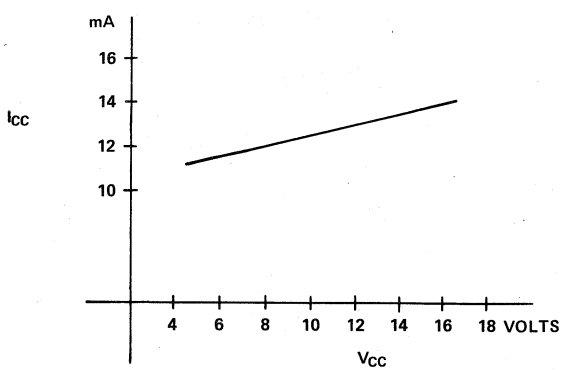


Figure 14. Quiescent Current vs. Power Supply Voltage for AD558

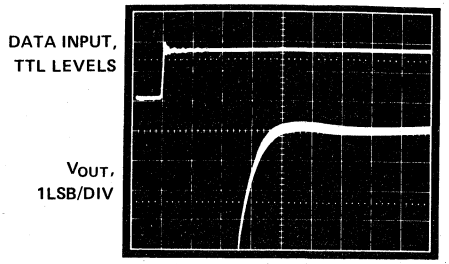


Figure 15. AD558 Settling Characteristic Detail 0V to 2.56V Output Range Full-Scale Step

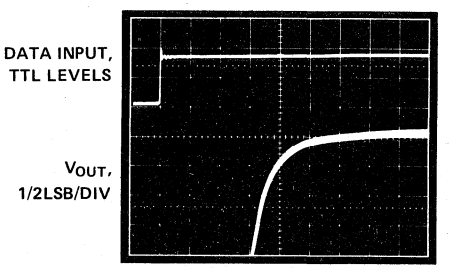


Figure 16. AD558 Settling Characteristic Detail 0V to 10V Output Range Full-Scale Step

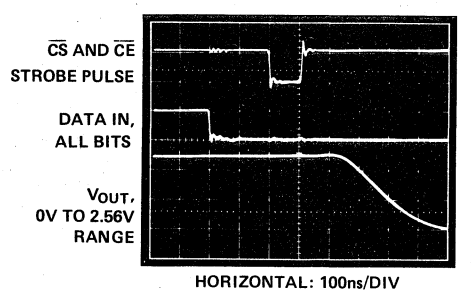


Figure 17. AD558 Logic Timing

ANALOG DEVICES

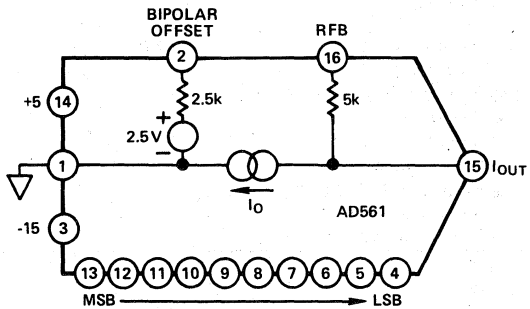
Low Cost 10-Bit Monolithic D/A Converter

AD561*

FEATURES

- Complete Current Output Converter
- High Stability Buried Zener Reference
- Laser Trimmed to High Accuracy (1/4LSB Max Error, AD561K, T)
- Trimmed Output Application Resistors for 0 to +10, ±5 Volt Ranges
- Fast Settling – 250ns to 1/2LSB
- Guaranteed Monotonicity Over Full Operating Temperature Range
- TTL/DTL and CMOS Compatible (Positive True Logic)
- Single Chip Monolithic Construction

AD561 FUNCTIONAL BLOCK DIAGRAM



TO-116

9

PRODUCT DESCRIPTION

The AD561 is an integrated circuit 10-bit digital-to-analog converter combined with a high stability voltage reference fabricated on a single monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion; they are trimmed to 0.1% accuracy, thus eliminating external trimmers in many situations.

Several important technologies combine to make the AD561 the most accurate and most stable 10-bit DAC available. The low temperature coefficient, high stability thin-film network is trimmed at the wafer level by a fine resolution laser system to 0.01% typical linearity. This results in an accuracy specification of ±1/4LSB max for the K and T versions, and 1/2LSB max for the J and S versions.

The AD561 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow custom correction of the temperature coefficient of each device. This results in a typical full-scale temperature coefficient of 15ppm/°C; the T.C. is tested and guaranteed to 30ppm/°C max for the K and T versions, 60ppm/°C max for the S, and 80ppm/°C for the J.

The AD561 is available in four performance grades. The AD561J and K are specified for use over the 0 to +70°C temperature range and are available in either a 16-pin hermetically-sealed ceramic DIP or a 16-pin molded plastic DIP. The AD561S and T grades are specified for the -55°C to +125°C range and are available in the ceramic package.

PRODUCT HIGHLIGHTS

1. Advanced monolithic processing and laser trimming at the wafer level have made the AD561 the most accurate 10-bit converter available while keeping costs consistent with large volume integrated circuit production. The AD561K and T have 1/4LSB max relative accuracy and 1/2LSB max differential nonlinearity. The low T.C. R-2R ladder guarantees that all AD561 units will be monotonic over the entire operating temperature range.
2. Digital system interfacing is simplified by the use of a positive true straight binary code. The digital input voltage threshold is a function of the positive supply level; connecting V_{CC} to the digital logic supply automatically sets the threshold to the proper level for the logic family being used. Logic sink current requirement is only 25μA.
3. The high speed current steering switches are designed to settle in less than 250ns for the worst case digital code transition. This allows construction of successive-approximation A/D converters in the 3 to 5μs range.
4. The AD561 has an output voltage compliance range from -2 to +10 volts, thus allowing direct current-to-voltage conversion with just an output resistor, omitting the op amp. The 40MΩ open collector output impedance results in negligible errors due to output leakage currents.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +5V, V_{ee} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561K MIN	AD561K TYP	AD561K MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			*			V
Bit OFF Logic "0"			+0.8			*	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			*			V
Bit OFF Logic "0"			30% V_{CC}			*	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		*	*	nA
Bit OFF Logic "0"		-5	-25		*	*	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	*	*	*	mA
Bipolar	±0.75	±1.0	±1.2	*	*	*	mA
Resistance (Exclusive of Application Resistors)		40M			*		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		*	*	% of F.S.
Capacitance		25			*		pF
Compliance Voltage	-2	-3	+10	*	*	*	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			*		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		*	*	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		*	*	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		*	*	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		*	*	ppm of F.S./%
TEMPERATURE RANGE							
Operating		0 to +70			*	*	°C
Storage ("D" Package)		-65 to +150			*	*	°C
("N" Package)		-25 to +85			*	*	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	80		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			*		V
RANGES (See Figs. 5, 6)		-5 to +5			*		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			*		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			*		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			*		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			*		% of F.S.

NOTES
*Specifications same as AD561J specs.
Specifications subject to change without notice.

MODEL	AD561S MIN	AD561S TYP	AD561S MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/4	±1/2	LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			**			V
Bit OFF Logic "0"			+0.8			**	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			**			V
Bit OFF Logic "0"			30% V_{CC}			**	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+20	+100		**	**	nA
Bit OFF Logic "0"		-25	-100		**	**	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	**	**	**	mA
Bipolar	±0.75	±1.0	±1.2	**	**	**	mA
Resistance (Exclusive of Application Resistors)		40M			**		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		**	**	% of F.S.
Capacitance		25			**		pF
Compliance Voltage	-2	-3	+10	**	**	**	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			**		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		6	10		**	**	mA
V_{EE}, -10.8V dc to -16.5V dc		11	16		**	**	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		**	**	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		**	**	ppm of F.S./%
TEMPERATURE RANGE							
Operating		-55 to +125			**	**	°C
Storage		-65 to +150			**	**	°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	10		1	5	ppm of F.S./°C
Bipolar Zero		2	20		2	10	ppm of F.S./°C
Full Scale		15	60		15	30	ppm of F.S./°C
Differential Nonlinearity		2.5			2.5		ppm of F.S./°C
MONOTONICITY		Guaranteed over full operating temp. range			Guaranteed over full operating temp. range		
PROGRAMMABLE OUTPUT		0 to +10			**		V
RANGES (See Figs. 5, 6)		-5 to +5			**		V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			**		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			**		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			**		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			**		% of F.S.

NOTES

**Specifications same as AD561S specs.

Specifications subject to change without notice.

THE AD561 OFFERS TRUE 10-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD561 is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T versions − 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD561 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 9.8mV change in the analog output (1LSB = 10V x 1/1024 = 9.8mV). If in actual use, however, a 1LSB change in the input code results in a change of only 2.45mV (1/4LSB) in analog output, the differential nonlinearity error would be 7.35mV, or 3/4LSB. The AD561K and T have a max differential linearity error of 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 2.5ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.025% (100 x 2.5ppm/°C of error). The resulting error could then be as much as 0.025% + 0.025% = 0.05% of F.S. (1/2LSB represents 0.05% of F.S.). To be sure of accurate performance all versions of the AD561 are therefore 100% tested to be monotonic over the full operating temperature range.

AD561 ORDERING GUIDE

MODEL	TEMP RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE OPTIONS[1]
AD561JD	0 to +70°C	±½LSB max	80ppm max	D16A
AD561JN	0 to +70°C	±½LSB max	80ppm max	N16A
AD561KD	0 to +70°C	±¼LSB max	30ppm max	D16A
AD561KN	0 to +70°C	±¼LSB max	30ppm max	N16A
AD561SD	-55 to +125°C	±½LSB max	60ppm max	D16A
AD561TD	-55 to +125°C	±¼LSB max	30ppm max	D16A

[1] See Section 19 for package outline information.

CONNECTING THE AD561 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510, AD741L, AD301AL) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to 1/2LSB on a 10 volt scale). If a 25Ω fixed resistor is substituted for the 50Ω trimmer, unipolar zero will typically be within ±1/10LSB (plus op amp offset), and full scale accuracy will be within ±1LSB. Substituting a 25Ω resistor for the 50Ω bipolar offset trimmer will give a bipolar zero error typically within ±1LSB.

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25picofarad DAC output capacitance.

FIGURE 5. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust op amp trimmer, R_1, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 50Ω gain trimmer, R_2, until the output is 9.990 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.23V full scale is desired (exactly 10mV/bit), insert a 120Ω resistor in series with R_2.

FIGURE 6. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.990 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . ZERO ADJUST

Turn ON MSB only, turn OFF all other bits. Adjust 50Ω trimmer R_3, to give 0.000 output volts. For maximum resolution a 120Ω resistor may be placed in parallel with R_3.

STEP II . . . GAIN ADJUST

Turn OFF all bits, adjust 50Ω gain trimmer to give a reading of -5.000 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 4. ±10 VOLT BUFFERED BIPOLAR OUTPUT

The AD561 can also be connected for a ±10 volt bipolar range with an additional external resistor as shown in Figure 4. A larger value trimmer is required to compensate for tolerance in the thin film resistors (which are trimmed to match the full scale current). For best full scale temperature coefficient performance, the external resistors should have a T.C. of -50ppm/°C.

PIN CONFIGURATION
TOP VIEW

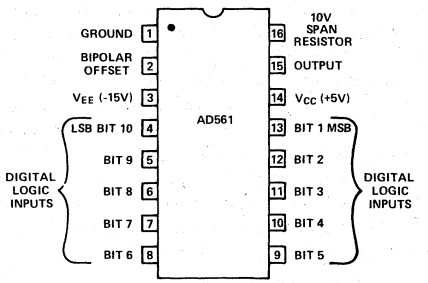


Figure 1.

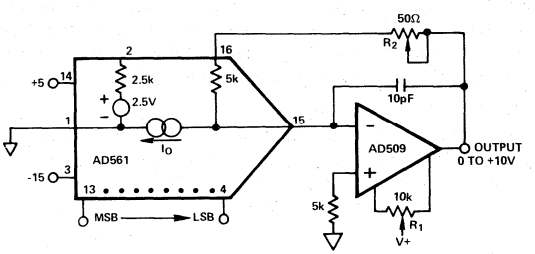


Figure 2. 0 to +10V Unipolar Voltage Output

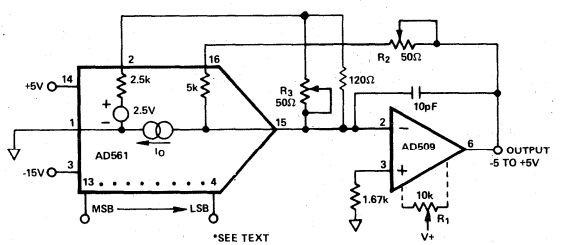


Figure 3. ±5V Buffered Bipolar Voltage Output

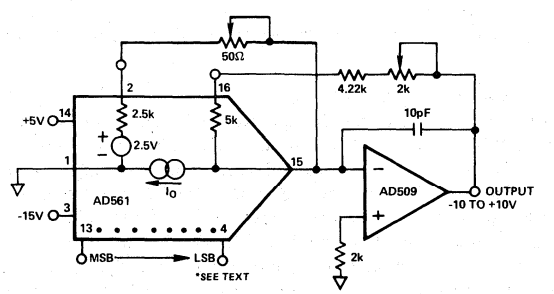


Figure 4. ±10V Buffered Voltage Output

CIRCUIT DESCRIPTION

A simplified schematic with the essential circuit features of the AD561 is shown in Figure 5. The voltage reference, CR1, is a buried zener (or subsurface breakdown diode). This device exhibits far better all-around performance than the NPN base-emitter reverse-breakdown diode (surface zener), which is in nearly universal use in integrated circuits as a voltage reference. Greatly improved long term stability and lower noise are the major benefits the buried zener derives from isolating the breakdown point from surface stress and mobile oxide charge effects. The nominal 7.5 volt device (including temperature compensation circuitry) is driven by a current source to the negative supply so that the positive supply can be allowed to go as low as 4.5 volts. The temperature coefficient of each diode is determined individually; this data is then used to laser trim a compensating circuit to balance the overall T.C. to zero. The typical resulting T.C. is 0 to ±15ppm/°C.

The negative reference level is inverted and scaled by A_1 to give a +2.5 volt reference (which can be driven by the low positive supply). The AD561, packaged in the 16-pin DIP, has the +2.5 volt reference (REF OUT) connected directly to the input of the control amplifier (REF IN). The buffered reference is not directly available externally except through the 2.5kΩ bipolar offset resistor.

The 2.5kΩ scaling resistor and control amplifier A_2 then force a 1mA reference current to flow through reference transistor Q1, which has a relative emitter area of 8A. This is accomplished by forcing the bottom of the ladder to the proper voltage. Since Q_1 and Q_2 have equal emitter areas and have equal 5kΩ emitter resistors, Q_2 also carries 1mA. The ladder voltage drop constrains Q_7 (with area 4A) to carry only 0.5mA; Q_8 carries 0.25mA, etc.

The first four significant bit cells are scaled exactly in emitter area to match Q_1 for optimum V_{BE} and V_{BE} drift match, as well as for beta match. These effects are insignificant for the lower order bits, which account for a total of only 1/16 of full scale. However, the 18mV V_{BE} difference between two matched transistors carrying emitter currents in a ratio of 2:1 must be corrected. This is done by forcing 120μA through the 150Ω interbase resistors. These resistors and the R-2R ladder resistors are actively laser-trimmed at the wafer level to bring total device accuracy to better than 1/4LSB. Sufficient ratio accuracy in the last two bits is obtained by simple emitter area ratio such that it is unnecessary to use additional area for ladder resistors. The current in Q_{16} is added to the ladder to balance it properly but is not switched to the output; thus full scale is 1023/1024 x 2mA.

The switching cell of Q_3, Q_4, Q_5 and Q_6 serves to steer the cell current either to ground (BIT 1 low) or to the DAC output (BIT 1 high). The entire switching cell carries the same current whether the bit is on or off, thus minimizing thermal transients and ground current errors. The logic threshold, which is generated from the positive supply (see Digital Logic Interface) is applied to one side of each cell.

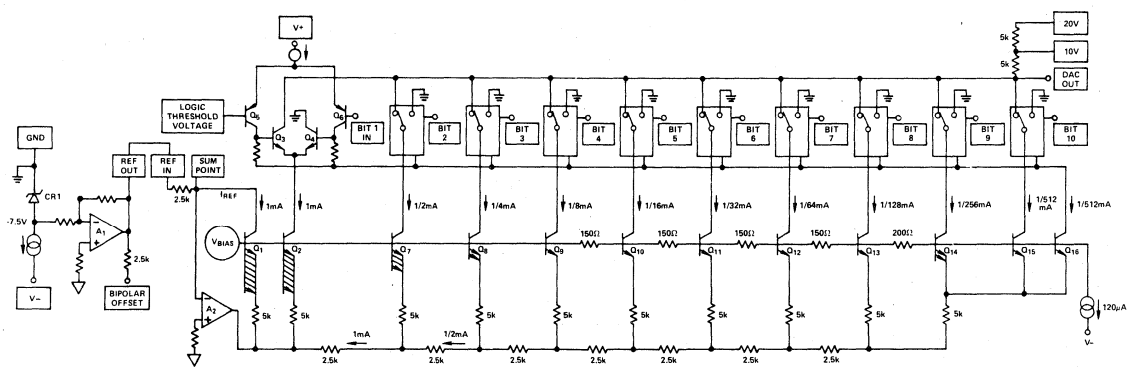


Figure 5. Circuit Diagram Showing Reference, Control Amplifier, Switching Cell, R-2R Ladder, and Bit Arrangement of AD561

DIGITAL LOGIC INTERFACE

All standard positive supply logic families interface easily with the AD561. The digital code is positive true binary (all bits high, Logic "1", gives positive full scale output). The logic input load factor (100nA max at Logic "1", -25μA max at Logic "0", 3pF capacitance), is less than one equivalent digital load for all logic families, including unbuffered CMOS. The digital threshold is set internally as a function of the positive supply, as shown in Figure 6. For most applications, connecting V_{CC} to the positive logic supply will set the threshold at the proper level for maximum noise immunity. For nonstandard applications, refer to Figure 6 for threshold levels. Uncommitted bit input lines will assume a "1" state (similar to TTL), but they are high impedance and subject to noise pickup. Unused digital inputs should be connected directly to ground or V_{CC}, as desired.

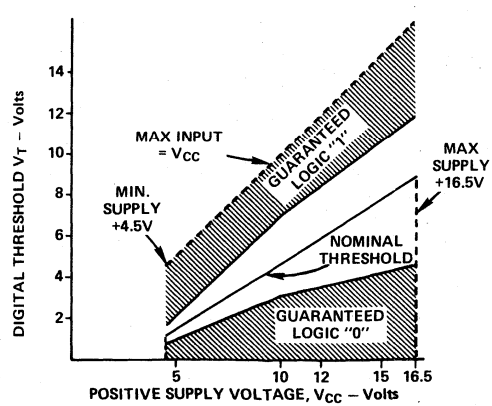


Figure 6. Digital Threshold Vs. Positive Supply

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD561 are specifically designed for fast settling operation. The typical settling time to ±0.05% (1/2LSB) for the worst case transition (major carry, 0111111111 to 1000000000) is less than 250ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB.) But full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD561 is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see next page), or in many display applications. This form of conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 9. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD561 output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.05% of full scale (for a full scale transition) requires 7.6 time constants. This effect is important for $R > 1k\Omega$.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown previously in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 600ns unipolar and 1.1μs bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices; 0.1μF will be sufficient since the AD561 runs at constant supply current regardless of input code.

POWER SUPPLY SELECTION

The AD561 will operate over a wide range of power supply voltages, with a total supply from 15.3 to 33 volts. Symmetrical supplies are not required, and in many applications not recommended. Maximum allowable supplies are ±16.5V.

The positive supply level determines the digital threshold level, as explained on page 6 and shown in Figure 6. It is therefore recommended that V_{CC} be connected directly to the digital supply for best threshold match.

Positive output voltage compliance range is unaffected by the positive supply level because of the open collector output stage design; thus the full +10 volt compliance is available even with a +5 volt V_{CC} level. Power supply rejection is excellent, so that digital supply noise will not be reflected to the output. but use of a 0.1μF bypass capacitor near the AD561 is recommended for decoupling.

The nominal negative supply level is -15 volts, with an allowable range of -10.8 to -16.5 volts. The negative supply level affects the negative compliance range, as shown in Figure 7.

OUTPUT VOLTAGE COMPLIANCE

The AD561 has a typical output compliance range from -3 to +10 volts. The output current is unaffected by changes in the output terminal voltage over that range. This results from the use of open collector output switching stages in a cascode configuration, and gives an output impedance of 40MΩ. Positive compliance range is limited only by collector breakdown (and is independent of positive supply level), but the negative range is limited by the required bias levels and resistor ladder voltage. Negative compliance varies with negative supply, as shown in Figure 7. The compliance range is guaranteed to be -2 to +10 volts with V_{EE} = -15 volts.

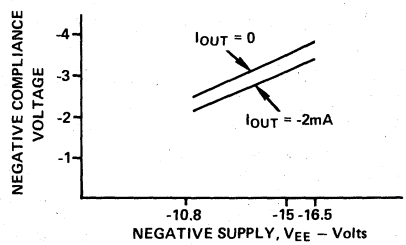


Figure 7. Typical Negative Compliance Range Vs. Negative Supply

DIRECT UNBUFFERED VOLTAGE OUTPUT

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar output resistors to give a ±1.66 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 2.5 volt reference voltage for bipolar offset. For example, setting R_X = 2.5kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance. A 0 to +10 volt output can be obtained by connecting the 5kΩ gain resistor to 9.99 volts; again the digital code is complementary binary.

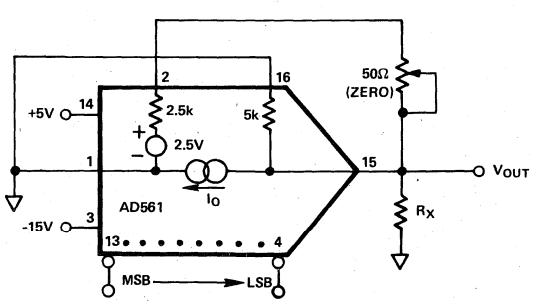


Figure 8. Unbuffered Bipolar Voltage Output

HIGH SPEED 10-BIT A/D CONVERTERS

The fast settling characteristics of the AD561 make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 10-bit converter system to be constructed with a minimum parts count. Shown here is a configuration using standard components; this system completes a full 10-bit conversion in 5.5μs unipolar or 12μs bipolar. This converter will be accurate to ±1/2LSB of 10 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.99 volts, with each bit having a value of 9.76mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +4.9mV; trim R_1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.985 volts (10 volts − 1LSB − 1/2LSB); then trim R_2 again until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.99 volts. Bipolar offset trimming is done by applying a +4.9mV input signal and trimming R_1 for the LSB transition (MSB "1", all other bits "0"). Full scale is set by applying -4.995 volts and trimming R_2 for the LSB transition (all other bits "0"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 10-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance of 1kΩ, 1LSB = 2mV) to the point that comparator performance will be sacrificed. A 1kΩ resistor is the optimum value for this application for 10-bit accuracy. The chart shown in the figure gives the speed of the ADC for ±1/2LSB accuracy (and no missing codes) for 6, 8 and 10-bit resolution.

A much faster converter can be constructed by using higher performance external components. Each individual high-order bit settles in less than 250ns; the low-order bits less than 200ns. Because of this, a staged clock which speeds up for lower bits will improve the speed. Also, a faster comparator and Schottky TTL or ECL logic would be necessary. 10-bit converters in the 3 to 5μs range could be built around the AD561 with these techniques.

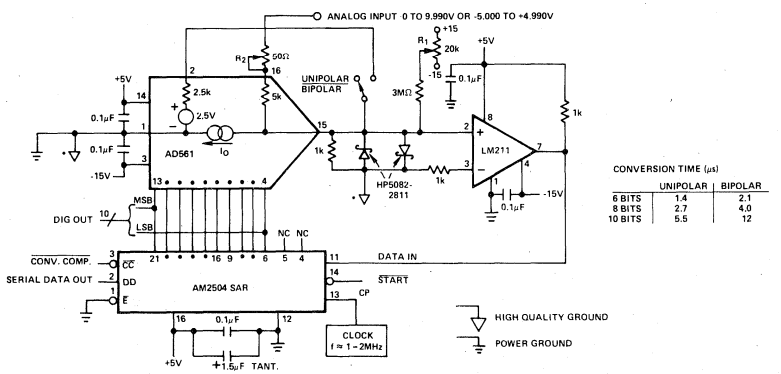


Figure 9. Fast Precision Analog-to-Digital Converter

DIGITAL 4 TO 20mA OR 1 TO 5 VOLT CONVERTER

A direct digital 4 to 20mA or 1 to 5 volt line driver can be built with the AD561 as shown in Figure 10. The 2.5 volt reference is divided to provide 1 volt at the op amp noninverting input − thus a zero input code results in a 1 volt output at the Darlington emitter (V_{OUT}). The 2k feedback resistance converts the nominal 2mA (±20%) full scale output from the AD561 to 4 volts, for a total output of 5 volts F.S. The voltage at the emitter forces a proportional current through the 250Ω (which appears at the collector as I_{OUT}). The AD561 current is added to the 4−20mA line; thus 5 volts full scale gives 22mA in the current loop. For exactly 20mA, trim the 1k pot for 4.5V F.S. (A single op amp circuit will not produce both 1 to 5 volt and 4 to 20mA outputs simultaneously.)

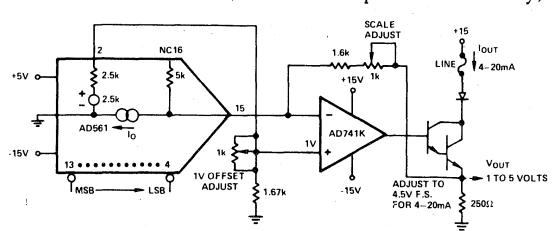


Figure 10. Digital 4-to-20mA or 1-to-5 Volt Line Driver

DIGITALLY PROGRAMMABLE SET-POINT COMPARATOR

Figure 11 demonstrates a high accuracy systems-oriented set-point comparator. The 2.5 volt reference is buffered and amplified by the AD741K to produce an exact 10.000 volt reference which could be used as a primary system reference for several such circuits. The +10 volt compliance of the AD561 then allows it to generate a zero to +10 volt output swing through the 5kΩ application resistor without an additional op amp. The digital code for this system will be complementary binary (all 1's give 0.00 volts out).

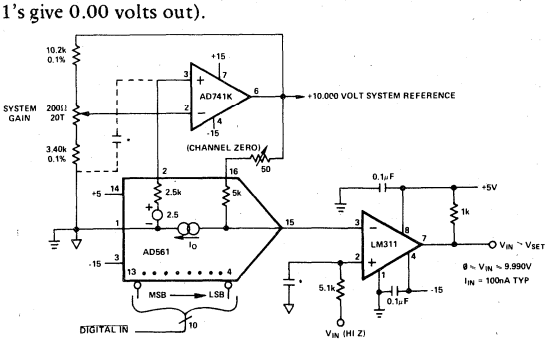


Figure 11. Digitally Programmable Set-Point Comparator

ANALOG DEVICES

IC 12-Bit D/A Converter

AD562/AD563*

FEATURES

True 12-Bit Accuracy
Guaranteed Monotonicity Over Full Temperature Range
Hermetic 24-Pin DIP
TTL/DTL and CMOS Compatibility
Positive True Logic

PRODUCT DESCRIPTION

The AD562/AD563 are monolithic 12-bit digital-to-analog converters consisting of especially designed precision bipolar switches and control amplifiers and compatible high stability silicon chromium thin film resistors. The AD563 also includes its own internal voltage reference.

A unique combination of advanced circuit design, high stability SiCr thin film resistor processing and laser trimming technology provide the AD562/AD563 with true 12-bit accuracy. The maximum error at +25°C is limited to ±½LSB on all versions and monotonicity is guaranteed over the full operating temperature range.

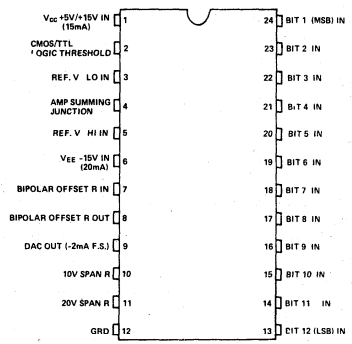
The AD562 and AD563 are recommended for high accuracy 12-bit D/A converter applications where true 12-bit performance is required, but low cost and small size are considerations. Both devices are also ideal for use in constructing A/D conversion systems and as building blocks for higher resolution D/A systems. J and K versions are specified for operation over the 0 to +70°C temperature range, the S and T for operation over the extended temperature range, -55°C to +125°C.

PRODUCT HIGHLIGHTS

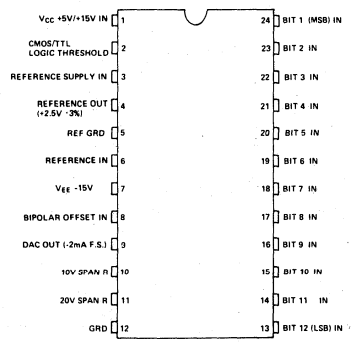
1. The AD562 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, the AD563 is recommended with its internal low drift voltage reference.
2. True 12-bit resolution is achieved with guaranteed monotonicity over the full operating temperature range. Voltage outputs are easily implemented by using an external operational amplifier and the AD562/AD563s internally provided feedback resistors.
3. The devices incorporate a newly developed and fully differential, non-saturating precision current switching cell structure which provides increased immunity to supply voltage variation and also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation.

***Covered by Patent Nos. 3,961,326; 4,141,004; 3,747,088; RE 28,633; 3,803,590; 4,020,486; the AD563 is also covered by 4,213,806; 4,136,349.**

AD562, AD563 PIN CONFIGURATIONS



AD562



AD563

4. The thin film resistor network contains gain, range, and bipolar offset resistors so that various output voltage ranges can be programmed by changing connections to the device terminal leads. Thin film resistors are laser trimmed while the device is powered to accurately calibrate all scale factors. The scale factors are dependent upon the tracking coefficient (<±2ppm/°C) of these resistors, rather than upon their absolute temperature coefficients.
5. TTL or CMOS input can be accommodated for supply voltages from +5V to +15V.
6. Positive true logic eliminates the need for additional inverter components.

SPECIFICATIONS (T_A = +25°C, unless otherwise specified)

MODEL	AD562KD/BIN AD562KD/BCD	AD562AD/BIN AD562AD/BCD	AD562SD/BIN AD562SD/BCD
DATA INPUTS (positive True, Binary (BCD) and Offset Binary (BCD))			
TTL, V_{CC} = +5V, Pin 2			
Open Circuit			
Bit ON Logic "1"	+2.0V	*	*
Bit OFF Logic "0"	+0.8V max	*	*
CMOS, 4.75 ≤ V_{CC} ≤ 15.8, Pin 2 Tied to Pin 1			
Bit ON Logic "1"	70%V_{CC} min	*	*
Bit OFF Logic "0"	30%V_{CC} max	*	*
Logic Current (Each Bit)			
Bit ON Logic "1"	+20nA typ, +100nA max	*	*
Bit OFF Logic "0"	-50μA typ, -100μA max	*	*
OUTPUT			
Current			
Unipolar	-1.6mA min, -2.0mA typ, -2.4mA max	*	*
Bipolar	±0.8mA min, ±1.0mA typ, ±1.2mA max	*	*
Resistance (Exclusive of Span Resistors)	5.3kΩ min, 6.6kΩ typ, 7.9kΩ max	*	*
Unipolar Zero (All Bits OFF)	0.01% of F.S. typ, 0.05% of F.S. max	*	*
Capacitance	33pF typ	*	*
Compliance Voltage	-1.5V to +10V typ	*	*
RESOLUTION			
Binary	12 Bits	*	*
BCD	3 Digits	*	*
ACCURACY (Error Relative to Full Scale)			
Binary	±1/2LSB max	*	±1/4LSB max
BCD	±1/2LSB max	*	±1/10LSB max
DIFFERENTIAL NONLINEARITY	±1/2LSB max	*	*
SETTLING TIME TO 1/2LSB			
All Bits ON-to-OFF or OFF-to-ON	1.5μs typ	*	*
POWER REQUIREMENTS			
V_{CC}, +4.75 to +15.8V dc	15mA typ, 18mA max	*	*
V_{EE}, -15V dc ±5%	20mA typ, 25mA max	*	*
POWER SUPPLY GAIN SENSITIVITY			
V_{CC} @ +5V dc	2ppm of F.S./% max	*	*
V_{CC} @ +15V dc	2ppm of F.S./% max	*	*
V_{EE} @ -15V dc	6ppm of F.S./% max	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C typ	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C typ	*	*
TEMPERATURE COEFFICIENT			
Unipolar Zero	2ppm of F.S./°C max	*	2ppm of F.S./°C max
Bipolar Zero	4ppm of F.S./°C max	*	*
Gain	5ppm of F.S./°C max	*	*
Differential Nonlinearity	2ppm of F.S./°C	*	1ppm of F.S./°C
MONOTONICITY	Guaranteed Over Full Operating Temperature Range	*	*
EXTERNAL ADJUSTMENTS[1]			
Gain Error with Fixed 50Ω Resistor	±0.2% of F.S. typ	*	*
Bipolar Zero Error with Fixed 50Ω Resistor	±0.1% of F.S. typ	*	*
Gain Adjustment Range	±0.25% of F.S. typ	*	*
Binary Bipolar Zero Adjustments Range	±0.25% of F.S. typ	*	*
BCD Bipolar Offset Adjustment Range	±0.17% of F.S. typ	*	*
PROGRAMMABLE OUTPUT RANGES	0 to +5V typ	*	*
	-2.5V to +2.5V typ	*	*
	0V to +10V typ	*	*
	-5V to +5V typ	*	*
	-10V to +10V typ	*	*
REFERENCE INPUT			
Input Impedance	20kΩ typ	*	*

NOTES
*Specifications same as AD562KD. **Specifications same as AD563KD. ***Specifications same as AD563JD. [1]Device calibrated with internal reference.
Specifications subject to change without notice.

AD563JD/BIN AD563JD/BCD	AD563KD/BIN AD563KD/BCD	AD563SD/BIN AD563SD/BCD	AD563TD/BIN AD563TD/BCD
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	±1/4LSB	**	**
*	±1/4LSB	**	**
*	*	*	*
*	*	*	*
15mA typ, 20mA max	***	***	***
*	*	*	*
3ppm of F.S./% typ, 10ppm of F.S./% max	***	***	***
3ppm of F.S./% typ, 10ppm of F.S./% max	***	***	***
14ppm of F.S./% typ, 25ppm of F.S./% max	***	***	***
*	*	-55°C to +125°C	-55°C to +125°C
*	*	*	*
With Internal Reference			
1ppm of F.S./°C typ, 2ppm of F.S./°C max	***	***	***
10ppm of F.S./°C max	***	***	***
50ppm of F.S./°C max	20ppm of F.S./°C max	30ppm of F.S./°C max	10ppm of F.S./°C max
*	*	*	*
*	*	*	*
With Fixed 10Ω Resistor			
±0.2% of F.S. typ	***	***	***
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
*	*	*	*
5kΩ typ	***	***	***

THE AD562/AD563 OFFERS TRUE 12-BIT RESOLUTION OVER FULL TEMPERATURE RANGE

Accuracy: Analog Devices defines accuracy as the maximum deviation of the actual DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) *for any bit combination.* The AD563, for example, is laser trimmed to ¼LSB (0.006% of F.S.) maximum error at +25°C for K, S and T versions . . . ½LSB for the J version.

Monotonicity: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a single-valued function of the input. All versions of the AD562/AD563 are monotonic over their full operating temperature range.

Differential Nonlinearity: Monotonic behavior requires that the differential nonlinearity error be <1LSB both at 25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a one LSB change in digital input code. For example, for a 10V full-scale output, a change of one LSB in the digital input code should result in a 2.4mV change in the analog output (10V x 1/4096 = 2.4mV). If in actual use, however, a one LSB change in the input code results in a change of 1.3mV in analog output, the differential nonlinearity would be 1.1mV, or 0.011% of F.S. The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1ppm/°C) of error. The resulting error could then be as much as 0.006% + 0.01% = 0.016% of F.S. (1LSB represents 0.024% of F.S.). All versions of the AD563 are 100% tested to be monotonic over the full operating temperature range.

UNIPOLAR DAC's

STEP I . . . OUTPUT RANGE

Determine the output range required. For +10V F.S., connect the external operational amplifier output to Pin 10 and leave Pin 11 unconnected. For +5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

STEP II . . . ZERO ADJUST

Turn all bits OFF and adjust R_1 until op amp output is 0 volts.

STEP III . . . GAIN ADJUST

Turn all bits ON for binary DAC's (bits 1, 4, 5, 8, 9 and 12 ON for BCD DAC's). Adjust R_2 until op amp output is:

BINARY	BCD
4.9988V for +5V Range	4.9950 for +5V Range
9.9976 for +10V Range	9.9900 for +10V Range

BIPOLAR DAC's

Figure 1b is a typical connection scheme for the AD563 used in bipolar operation.

STEP I . . . OUTPUT RANGE

Determine the output range required. For ±10V F.S., connect the external op amp output to Pin 11 and leave Pin 10 unconnected. For ±5V F.S., connect the external op amp output to Pin 10 and leave Pin 11 unconnected. For ±2.5V F.S., connect the external op amp output to Pin 10 and short Pin 11 to Pin 9.

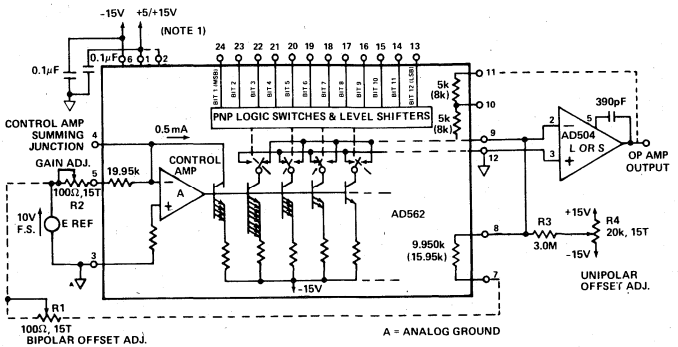
STEP II . . . OFFSET ADJUST

Turn all bits OFF and adjust R_3 until op amp output is:

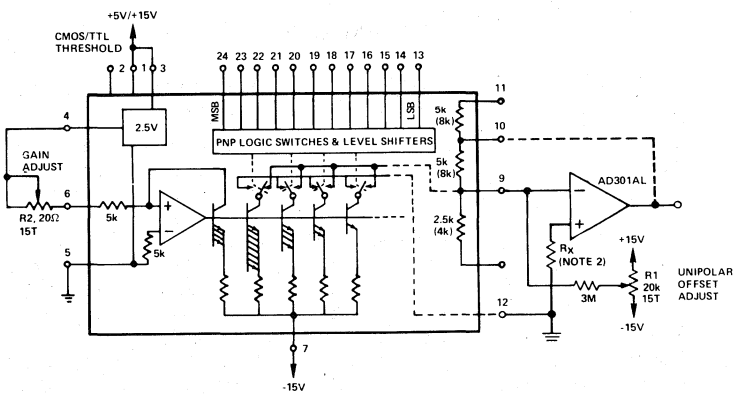
-2.5000V for ±2.5V Range
-5.0000V for ±5V Range
-10.0000V for ±10V Range

STEP III . . . GAIN ADJUST (Bipolar Zero)

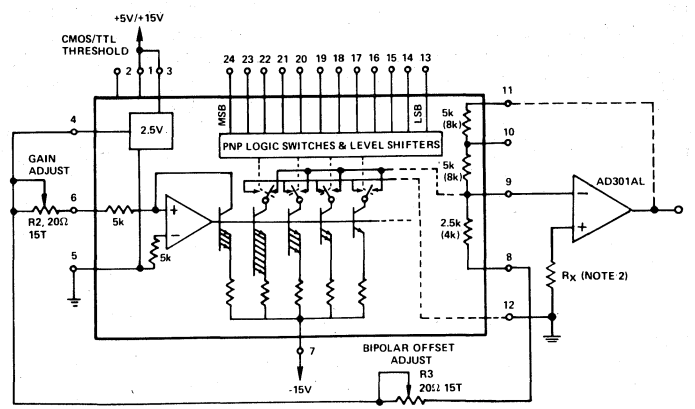
Turn bit 1 ON for Binary DAC's (bits 2 and 4 ON for BCD DAC's). Adjust R_2 until op amp output is 0 volts.



AD562 in Typical Unipolar and Bipolar Connection Scheme



AD563 in Typical Unipolar Connection Scheme



NOTE 1.
- A. FOR TTL AND DTL COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND LEAVE PIN 2 OPEN.
- B. FOR LOW VOLTAGE CMOS COMPATIBILITY, CONNECT +5 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.
- C. FOR HIGH VOLTAGE CMOS COMPATIBILITY, CONNECT +15 VOLTS TO PIN 1 AND SHORT PIN 2 TO PIN 1.

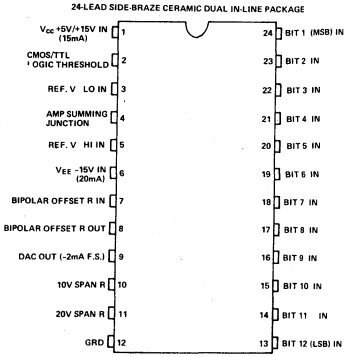
NOTE 2. IN UNIPOLAR OPERATION, R_X SHOULD BE MADE EQUAL TO THE PARALLEL COMBINATION OF THE INTERNAL FEEDBACK RESISTOR AND 6.6k. IN BIPOLAR, R_X EQUALS THE FEEDBACK RESISTOR IN PARALLEL WITH 1.8k.

NOTE 3. RESISTOR VALUES IN PARENTHESES ARE FOR BCD MODEL.

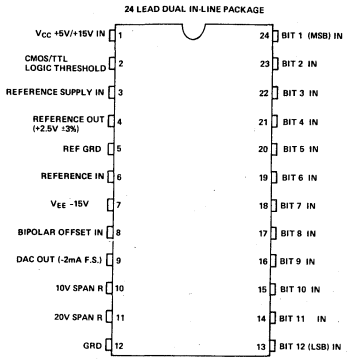
NOTE 4. SUPPLIES MAY BE BYPASSED WITH 0.1μF CAPACITORS.

AD563 in Typical Bipolar Connection Scheme

PIN CONFIGURATIONS
TOP VIEW



AD562



AD563

ORDERING GUIDE

MODEL	INPUT CODE	TEMP. RANGE	ACCURACY @ +25°C	GAIN T.C. (of F.S./°C)	PACKAGE[1] OPTIONS
AD562KD/BIN	Binary	0 to +70°C	±1/2LSB max	3ppm max	D24A
AD562KN/BIN	Binary	0 to +70°C	±1/2LSB max	3ppm max	N24A
AD562KD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	3ppm max	D24A
AD562KN/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	3ppm max	N24A
AD562AD/BIN	Binary	-25°C to +85°C	±1/2LSBmax	3ppm max	D24A
AD562AD/BCD	Binary Coded Decimal	-25°C to +85°C	±1/2LSB max	3ppm max	D24A
AD562SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	3ppm max	D24A
AD562SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/10LSB max	3ppm max	D24A
AD563JD/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	D24A
AD563JN/BIN	Binary	0 to +70°C	±1/2LSB max	50ppm max	N24A
AD563JD/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	D24A
AD563JN/BCD	Binary Coded Decimal	0 to +70°C	±1/2LSB max	50ppm max	N24A
AD563KD/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	D24A
AD563KN/BIN	Binary	0 to +70°C	±1/4LSB max	20ppm max	N24A
AD563KD/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	D24A
AD563KN/BCD	Binary Coded Decimal	0 to +70°C	±1/4LSB max	20ppm max	N24A
AD563SD/BIN	Binary	-55°C to +125°C	±1/4LSB max	30ppm max	D24A
AD563SD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	30ppm max	D24A
AD563TD/BIN	Binary	-55°C to +125°C	±1/4LSB max	10ppm max	D24A
AD563TD/BCD	Binary Coded Decimal	-55°C to +125°C	±1/4LSB max	10ppm max	D24A

[1] See Section 19 for package outline information.

Complete High Speed 12-Bit Monolithic D/A Converter

AD565A*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 250ns max
Full Scale Switching Time: 30ns
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD565AK, T)
Guaranteed for Operation with ±12V Supplies
Low Power: 225mW Including Reference
Pin-Out Compatible with AD563, AD565

PRODUCT DESCRIPTION

The AD565A is a fast 12-bit digital-to-analog converter combined with a high stability voltage reference on a single monolithic chip. The AD565A chip uses 12 precision, high speed bipolar current steering switches, control amplifier, laser-trimmed thin film resistor network, and buried Zener voltage reference to produce a very fast, high accuracy analog output current.

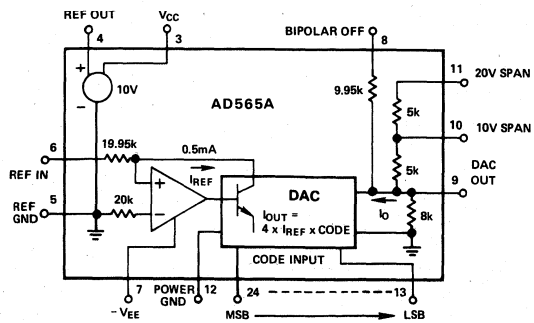
The combination of performance and flexibility in the AD565A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming (LWT) techniques. The AD565A has a 10 – 90% full scale transition time under 35 nanoseconds and settles to within ±1/2LSB in 250 nanoseconds max. The AD565A chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. This high speed and accuracy make the AD565A the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD565A is thus well suited for wide temperature range performance with maximum linearity error ±1/2LSB and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD565A is available in four performance grades. The AD565AJ and K are specified for use over 0 to +70°C temperature range and are available in a 24-pin hermetically-sealed, side-brazed ceramic DIP or plastic DIP. The AD565AS and T grades are specified for the −55°C to +125°C range and are available in the ceramic package.

*Covered by Patent Nos.: 3,803,590; RE 28,633; 4,213,806; 4,136,349.

AD565A FUNCTIONAL BLOCK DIAGRAM



24-PIN DUAL IN LINE PACKAGE

PRODUCT HIGHLIGHTS

1. The AD565A is a self-contained current output DAC and voltage reference fabricated on a single IC chip.
2. The device incorporates a newly developed, fully differential, non-saturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset resistors.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The pin-out of the AD565A is compatible with the industry-standard AD563, AD565 so that a system can easily be upgraded to higher speed performance without board changes.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

MODEL	AD565AJ MIN	AD565AJ TYP	AD565AJ MAX	AD565AK MIN	AD565AK TYP	AD565AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	0.05		0.01	0.05	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	50		10	20	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		150	250		150	250	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	5		3	5	mA
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	±0.25		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	±0.15		±0.05	±0.1	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (available for external loads)[3]	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

NOTES

[1] The digital inputs are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc.

[3] For operation at elevated temperatures the reference cannot supply current for external loads. It, therefore, should be buffered if additional loads are to be supplied.

Specifications subject to change without notice.

MODEL	AD565AS MIN	AD565AS TYP	AD565AS MAX	AD565AT MIN	AD565AT TYP	AD565AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	**+2.0**		**+5.5**	**+2.0**		**+5.5**	V
Bit OFF Logic "0"			**+0.8**			**+0.8**	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	**+300**		+120	**+300**	μA
Bit OFF Logic "0"		+35	**+100**		+35	**+100**	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	**-1.6**	-2.0	**-2.4**	**-1.6**	-2.0	**-2.4**	mA
Bipolar (all bits on or off)	**±0.8**	±1.0	**±1.2**	**±0.8**	±1.0	**±1.2**	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	**0.05**		0.01	**0.05**	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	**0.15**		0.05	**0.1**	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	**±1/2**		±1/8	**±1/4**	LSB
		(0.006)	**(0.012)**		(0.003)	**(0.006)**	% of F.S. Range
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	**±3/4**		±1/4	**±1/2**	LSB
T_{min} to T_{max}	**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	**2**		1	**2**	ppm/°C
Bipolar Zero		5	**10**		5	**10**	ppm/°C
Gain (Full Scale)		15	**30**		10	**15**	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		150	250		150	250	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating	-55		+125	-55		+125	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	**5**		3	**5**	mA
V_{EE}, -11.4 to -16.5V dc		-12	**-18**		-12	**-18**	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	**10**		3	**10**	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	**25**		15	**25**	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGES (see Figures 2, 3, 4)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω							
Resistor for R2 (Figure 2)		±0.1	**±0.25**		±0.1	**±0.25**	% of F.S. Range
Bipolar Zero Error with Fixed							
50Ω Resistor for R1 (Figure 3)		±0.05	**±0.15**		±0.05	**±0.1**	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	**9.90**	10.00	10.10	**9.90**	10.00	**10.10**	V
Current (available for external loads)[3]	**1.5**	2.5		**1.5**	2.5		mA
POWER DISSIPATION		225	345		225	345	mW

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . .0V to +18V
V_{EE} to Power Ground . . . . . .0V to -18V
Voltage on DAC Output (Pin 9) . . . . . .-3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . . -1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out. . . . . .Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

THE AD565A OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

ACCURACY: Analog Devices defines accuracy as the maximum deviation of the actual, adjusted DAC output (see next page) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD565A is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and T Versions—1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD565A are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD565AK and T have a max differential linearity error of 1/2LSB, which is a tighter specification than to simply guarantee monotonicity.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could under worst case conditions for a temperature change of +25°C to +125°C add 0.01% (100 x 1.0ppm/°C of error). The resulting error could then be as much as 0.01% + 0.006% = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD565A are therefore 100% tested for monotonicity over the full operating temperature range.

AD565A ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	MAX GAIN T.C. (ppm of F.S./°C)	Package Style[1]
AD565AJN/BIN	Plastic	0 to +70°C	±1/2LSB	50	N24A
AD565AJD/BIN	Ceramic	0 to +70°C	±1/2LSB	50	D24A
AD565AKN/BIN	Plastic	0 to +70°C	±1/4LSB	20	N24A
AD565AKD/BIN	Ceramic	0 to +70°C	±1/4LSB	20	D24A
AD565ASD/BIN	Ceramic	-55°C to +125°C	±1/2LSB	30	D24A
AD565ATD/BIN	Ceramic	-55°C to +125°C	±1/4LSB	15	D24A

[1] See Section 19 for package outline information.

CONNECTING THE AD565A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 2. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 8, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 8 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 3. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 4. OTHER VOLTAGE RANGES

The AD565A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 4.

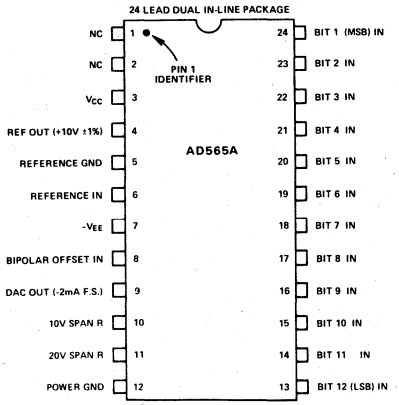


Figure 1.

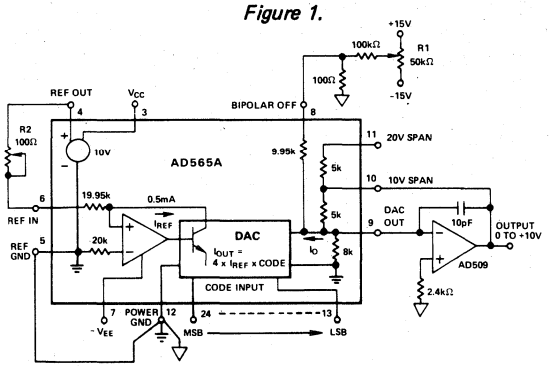


Figure 2. 0 to +10V Unipolar Voltage Output

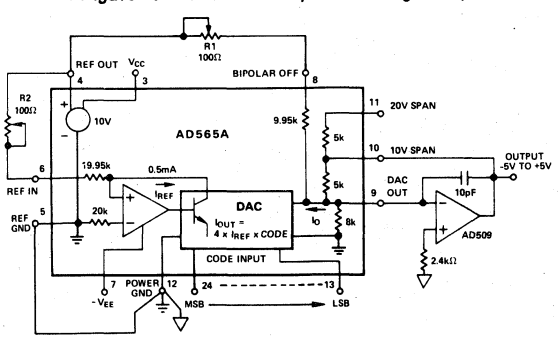


Figure 3. ±5V Bipolar Voltage Output

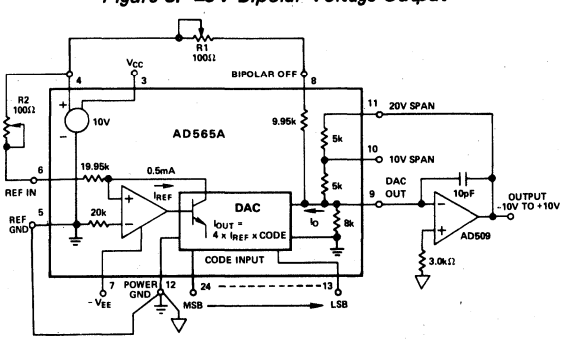


Figure 4. ±10V Voltage Output

INTERNAL/EXTERNAL REFERENCE USE

The AD565A has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD565A is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale and bipolar) is done in this configuration.

The AD565A can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference. For external reference applications, the AD566A series is recommended.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset, if used). A minimum of 1.5mA is available for driving external circuits. For use over the extended temperature range, however, a buffer should be used to preserve the accuracy. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

DIGITAL INPUT CONSIDERATIONS

The AD565A uses a standard positive true straight binary code for unipolar outputs (all 1's give full scale output), and an offset binary code for bipolar output ranges. In the bipolar mode, with all 0's on the inputs, the output will go to negative full scale; with 100. . . 00 (only the MSB on), the output will be 0.00 volts; with all 1's, the output will go to positive full scale.

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 5. The input line can be modeled as a 30kΩ resistance connected to a −0.7V rail.

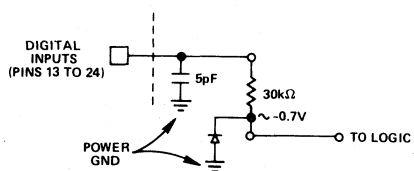


Figure 5. Equivalent Digital Input Circuit

GROUNDING RULES

The AD565A brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD565A; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD565A has a typical output compliance range from −2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 6.

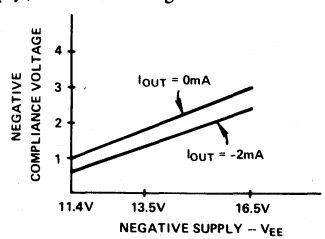


Figure 6. Typical Negative Compliance Range vs. Negative Supply

SETTLING TIME

The high speed NPN current steering switching cell and internally compensated reference amplifier of the AD565A are specifically designed for fast settling operation. The typical settling time to ±0.01% (1/2LSB) for the worst case transition (major carry or full scale step) is about 200ns; the lower order bits all settle in less than 200ns. (Worst case settling occurs when all bits are switched, especially the MSB).

The excellent high speed performance of the AD565A is demonstrated in these oscilloscope photographs. The measurements are made with the AD565A driving directly into an equivalent 50Ω load, and amplified with a low capacitance MOS-input, UHF amplifier. Both figures show the worst case situation, which is full scale transition from switching all bits ON to OFF.

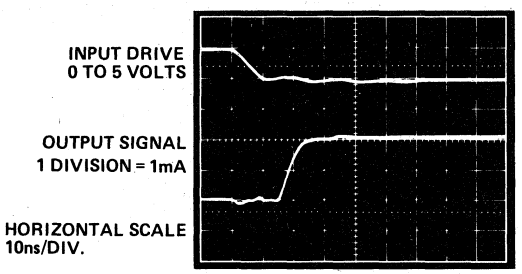


Figure 7. Full Scale Transition

The full transition characteristic is shown in Figure 7. There is about a 6-8ns delay, followed by a 10ns rise time and minimal overshoot. The transition in the other direction shows approximately a 20ns delay prior to a 10ns rise time. The slewing characteristics for smaller transitions show a similar characteristic.

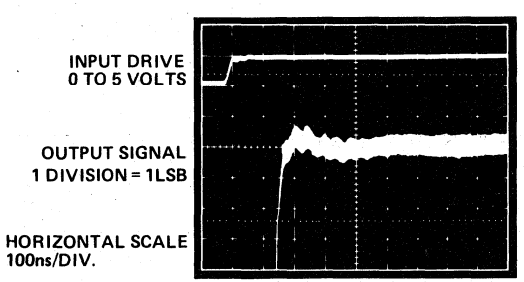


Figure 8. Settling Characteristic Detail

The fine detail of the full scale settling characteristic is shown in Figure 8. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance. The final portion of the signal slews to within 10LSB's in less than 150ns, reaches and stays within 1/2LSB in about 200ns, and shows less than 1/2LSB overshoot. The characteristic is completely settled out in less than 250ns.

HIGH SPEED SYSTEM DESIGN

Full realization of this high speed performance requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD565A is specified in terms of the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter (see the next page), or in many display applications. This form of current-to-voltage conversion can give very fast operation if proper design and layout is done. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 9. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD565A output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp must be used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits are shown in the applications circuits using the fast settling AD509. The circuits shown settle to ±1/2LSB in 1μs unipolar or bipolar. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor, as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. Both supplies should be bypassed near the devices: 0.1μF will be sufficient since the AD565A runs at constant supply current regardless of input code.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 9 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. Using a 50Ω resistor for R_X would allow interface to a 50Ω cable with a ±50mV full scale swing. Settling time would be very fast, as discussed in the section above.

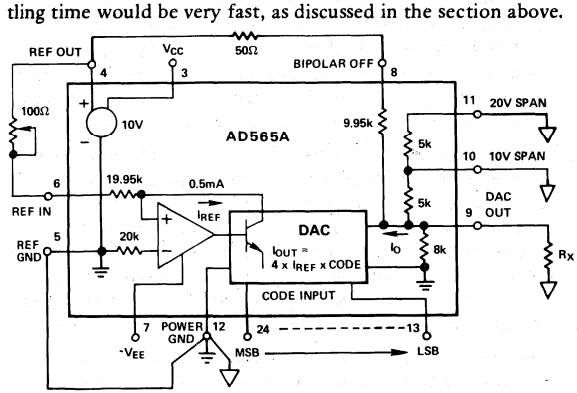


Figure 9. Unbuffered Bipolar Voltage Output

HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD565A make it ideal for high speed successive approximation A/D converters. The internal reference and trimmed application resistors allow a 12-bit converter system to be constructed with a minimum parts count. Shown in Figure 10 is a configuration using standard components; this system completes a full 12-bit conversion in 10μs unipolar or bipolar. This converter will be accurate to ±1/2LSB of 12 bits and have a typical gain T.C. of 10ppm/°C.

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts − 1LSB − 1/2LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is -5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a -4.9988V input signal and trimming R1 for the LSB transition (all other bits "0").

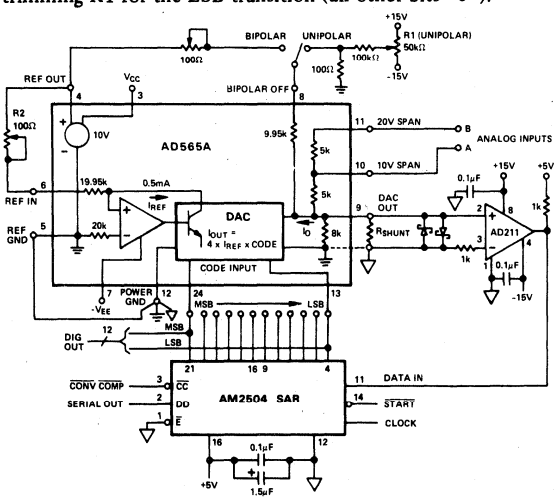


Figure 10. Fast Precision Analog to Digital Converter

Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1"). In many applications, the pretrimmed application resistors are sufficiently accurate that external trimmers will be unnecessary, especially in situations requiring less than full 12-bit ±1/2LSB accuracy.

For fastest operation, the impedance at the comparator summing node must be minimized, as mentioned in the section on settling time. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1kΩ, 1LSB = 0.5mV), to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will vary with the input configuration, as shown in the input range table.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

HIGH-RESOLUTION CIRCUITS

Sixteen-bit resolution digital-to-analog converters can be built by cascading an AD565A 12-bit DAC with an AD559 or AD1408 8-bit DAC. This technique can be used either to provide a 16-bit binary DAC or a 4-digit BCD DAC. By using an AD565AK with ±1/8LSB typical linearity to 12 bits, the total circuit will typically achieve ±1/2LSB accuracy for 14 binary bits, and ±1/2 least significant digit to 4 digits BCD. The binary configuration is shown in Figure 11. The AD559, with its thin-film ladder network similar to the AD565A, is preferred for good performance over temperature.

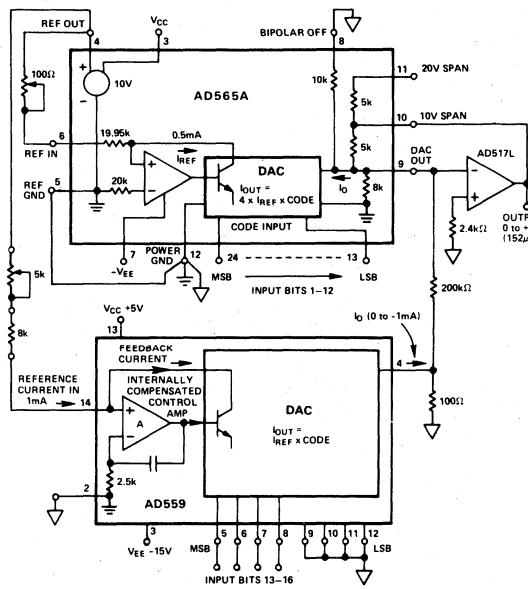


Figure 11. 16-Bit Binary DAC

COMPLEMENTARY BINARY CODE CIRCUITS

The AD565A can be used in circuits where only a complementary binary code is available. This is done by connecting the 10 volt span resistor to the 10 volt reference and connecting the DAC output to a noninverting amplifier as shown in Figure 12. The 8kΩ DAC output impedance and the 5kΩ span resistor will form a divider which will give a full scale output voltage (with all bits off) to the amplifier of about 6.15 volts. To obtain a 10 volt full scale, the amplifier is shown with a gain network back to the inverting input.

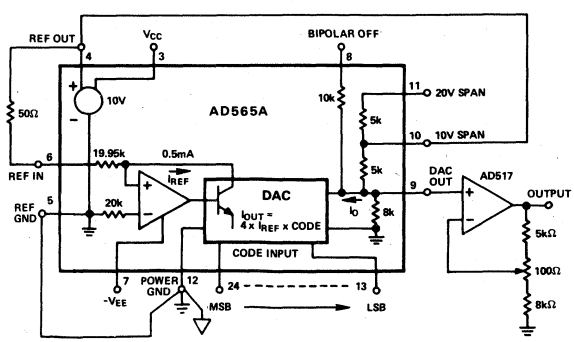


Figure 12. Complementary Output DAC

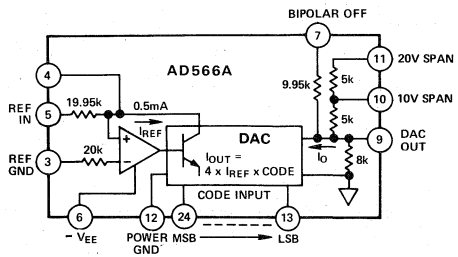
Low Cost High Speed 12-Bit Monolithic D/A Converter

AD566A*

FEATURES

Single Chip Construction
Very High Speed: Settles to 1/2LSB in 350ns max
Full Scale Switching Time: 30ns
Guaranteed for Operation with -12V Supply
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD566AK, T)
Low Power: 180mW
Pin-Out Compatible with AD562, AD566

AD566A FUNCTIONAL BLOCK DIAGRAM



24-PIN DUAL IN LINE PACKAGE

9

PRODUCT DESCRIPTION

The AD566A is a fast 12-bit digital-to-analog converter which incorporates the latest advances in analog circuit design into a low power monolithic chip.

The AD566A chip uses 12 precision, high speed bipolar current steering switches, control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current.

The combination of performance and flexibility in the AD566A has resulted from major innovations in circuit design, an important new high-speed bipolar process, and continuing advances in laser-wafer-trimming techniques (LWT). The AD566A has a 10—90% full scale transition time less than 35 nanoseconds and settles to within ±1/2LSB in 350 nanoseconds max. AD566A chips are laser-trimmed at the wafer level to ±1/8LSB typical linearity and are specified to ±1/4LSB max error (K and T grades) at +25°C. High speed and accuracy make the AD566A the ideal choice for high speed display drivers as well as fast analog-to-digital converters.

The AD566A is available in four performance grades. The AD566AJ and K are specified for use over the 0 to +70°C temperature range and the AD566AS and AT grades are specified for the -55°C to +125°C range. All are packaged in a 24-pin hermetic ceramic dual in line package.

PRODUCT HIGHLIGHTS

1. The wide output compliance range is ideally suited for fast, low noise, accurate voltage output configurations without an output amplifier.
2. The device incorporates a newly developed, fully differential, nonsaturating precision current switching cell structure which combines the dc accuracy and stability first developed in the AD562 with very fast switching times and an optimally-damped settling characteristic.
3. The chip also contains SiCr thin film application resistors which can be used with an external op amp to provide a precision voltage output or as input resistors for a successive approximation A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
4. The pin-out of the AD566A is compatible with the industry-standard AD562 so that a system can easily be upgraded to provide higher speed performance.

***Covered by patent numbers: 3,803,590; RE 28,633; 4,020,486; 3,747,088.**

SPECIFICATIONS (T_A = +25°C, V_{EE} = -15V, unless otherwise specified)

MODEL	AD566AJ MIN	AD566AJ TYP	AD566AJ MAX	AD566AK MIN	AD566AK TYP	AD566AK MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R.
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

NOTES
[1] The digital input levels are guaranteed but not tested over the temperature range.
[2] The power supply gain sensitivity is tested in reference to a V_{EE} of -15V dc.
Specifications subject to change without notice.

MODEL	AD566AS MIN	AD566AS TYP	AD566AS MAX	AD566AT MIN	AD566AT TYP	AD566AT MAX	UNITS
DATA INPUTS[1] (Pins 13 to 24)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"	0		+0.8	0		+0.8	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	+300		+120	+300	μA
Bit OFF Logic "0"		+35	+100		+35	+100	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (all bits on or off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar (adjustable to zero per Figure 3)		0.01	0.05		0.01	0.05	% of F.S.R.
Bipolar (Figure 4 R_1 and R_2 = 50Ω fixed)		0.05	0.15		0.05	0.1	% of F.S.R
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	±1/2		±1/8	±1/4	LSB
		(0.006)	(0.012)		(0.003)	(0.006)	% of F.S.R.
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
		(0.012)	(0.018)		(0.006)	(0.012)	% of F.S.R.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{min} to T_{max}	MONOTONICITY GUARANTEED			MONOTONICITY GUARANTEED			
TEMPERATURE COEFFICIENTS							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		7	10		2	3	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2LSB							
All Bits On-to-OFF or OFF-to-ON (Figure 8)		250	350		250	350	ns
FULL SCALE TRANSITION							
10% to 90% Delay plus Rise Time		15	30		15	30	ns
90% to 10% Delay plus Fall Time		30	50		30	50	ns
POWER REQUIREMENTS							
V_{EE}, -11.4 to -16.5V dc		-12	-18		-12	-18	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{EE} = -11.4 to -16.5V dc		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT							
RANGE (see Figures 3, 4, 5)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor R2 (Figure 3)		±0.1	±0.25		±0.1	±0.25	% of F.S.R.
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 4)		±0.05	±0.15		±0.05	±0.1	% of F.S.R.
Gain Adjustment Range (Figure 3)	±0.25			±0.25			% of F.S.R.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.R.
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
POWER DISSIPATION		180	300		180	300	mW

MULTIPLYING MODE PERFORMANCE (All Models)	
Quadrants	Two (2): Bipolar Operation at Digital Input Only
Reference Voltage	+1V to +10V, Unipolar
Accuracy	10 Bits (±0.05% of Reduced F.S.) for 1V dc Reference Voltage
Reference Feedthrough (unipolar mode, all bits OFF, and 1 to +10V [p-p], sinewave frequency for 1/2LSB [p-p] feedthrough)	40kHz typ
Output Slew Rate 10%–90%	5mA/μs
90%–10%	1mA/μs
Output Settling Time (all bits on and a 0–10V step change in reference voltage)	1.5μs to 0.01% F.S.

CONTROL AMPLIFIER	
Full Power Bandwidth	300kHz
Small-Signal Closed-Loop Bandwidth	1.8MHz

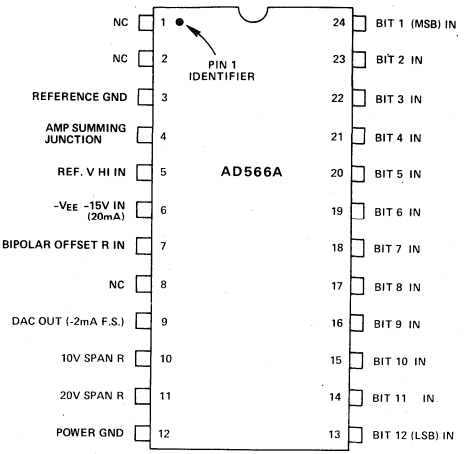
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{EE} to Power Ground . . . . . .0V to −18V
Voltage on DAC Output (Pin 9) . . . . . .−3V to +12V
Digital Inputs (Pins 13 to 24) to Power Ground . . . .−1.0V to +7.0V
Ref In to Reference Ground . . . . . .±12V
Bipolar Offset to Reference Ground . . . . . .±12V
10V Span R to Reference Ground . . . . . .±12V
20V Span R to Reference Ground . . . . . .±24V
Power Dissipation 1000mW

PIN CONFIGURATION

TOP VIEW



AD566A ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @+25°C	MAX GAIN T.C. (ppm of F.S./°C)	PACKAGE OPTION[1]
AD566AJN/BIN	Plastic	0 to +70°C	±1/2LSB	10	N24A
AD566AJD/BIN	Ceramic	0 to +70°C	±1/2LSB	10	D24A
AD566AKN/BIN	Plastic	0 to +70°C	±1/4LSB	3	N24A
AD566AKD/BIN	Ceramic	0 to +70°C	±1/4LSB	3	D24A
AD566ASD/BIN	Ceramic	−55°C to +125°C	±1/2LSB	10	D24A
AD566ATD/BIN	Ceramic	−55°C to +125°C	±1/4LSB	3	D24A

[1] See Section 19 for package outline information.

THE AD566A OFFERS TRUE 12-BIT PERFORMANCE

ACCURACY: Analog Devices defines accuracy as the maximi- deviation of the actual, adjusted DAC output (see the next page) from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD566A is laser trimmed to 1/4LSB (0.025% of F.S.) maximum error at +25°C for the K and T version and to 1/2LSB for the J and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of the input. All versions of the AD566A are monotonic over their entire operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential nonlinearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, if a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential nonlinearity error would be 1.83mV, or 3/4LSB. The AD566AK and T have a max differential linearity error of 1/2LSB, which is a tighter specification than simply guaranteed monotonicity.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 1.

The input reference current to the DAC, I_{REF}, is developed from the external reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC} which is a function of the digital input code, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

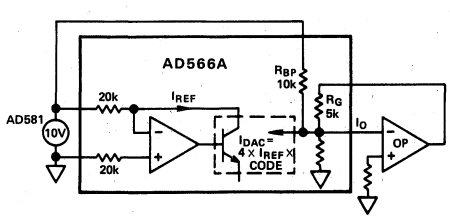


Figure 1. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ±1/2LSB max and the differential linearity error of ±3/4LSB max guarantee monotonic performance over the range of −55°C to +125°C. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift of 2ppm/°C max (which comes from leakage currents) causes a linear shift in the transfer curve as shown in Figure 2. The gain drift causes a change in the slope of the curve which results from reference drift and the device gain drift. The device gain drift is the DAC drift and drift in R_{GAIN} relative to the DAC resistors for a total of 3ppm/°C max (AD566AK, T). Total absolute error due to all of these effects is guaranteed to be less than ±0.05% of full scale from −55°C to +125°C.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to V_{REF} (see Figure 1) to generate a current which exactly balances the current of the MSB so that the output voltage is zero with the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 2. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD566A this error is held to 10ppm max. The total of all these errors is held to ±0.15% of full scale from −55°C to +125°C (AD566AT). Note that, in the bipolar ranges, full scale is defined as the total range from $-V_{FS}$ to $+V_{FS}$.

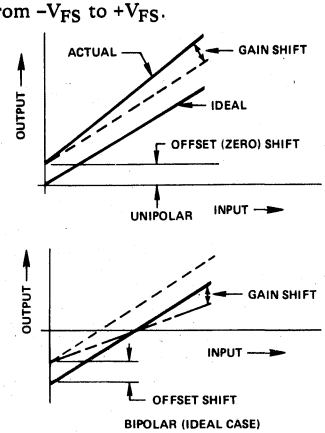


Figure 2. Unipolar and Bipolar Drifts

CONNECTING THE AD566A FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). If a 50Ω fixed resistor is substituted for the 100Ω trimmer, unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±1/2LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

FIGURE 3 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 7, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, but pin 7 should then be connected to pin 12.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer, R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 10 to the op amp output.

FIGURE 4. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 output volts.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 5. OTHER VOLTAGE RANGES

The AD566A can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 11. For a 5 volt span (0 to +5V or ±2.5V), the two 5k resistors are used in parallel by shorting pin 11 to pin 9 and connecting pin 10 to the op amp output and the bipolar offset resistor either to ground for unipolar or to V_{REF} for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 11 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 5.

DIGITAL INPUT		ANALOG OUTPUT		
MSB	LSB	Straight Binary	Offset Binary	Two's Compl.*
000000000000		Zero	-Full Scale	Zero
011111111111		Mid Scale -1LSB	Zero -1LSB	+FS -1LSB
100000000000		+1/2 FS	Zero	-FS
111111111111		+FS -1LSB	+ Full Scale -1LSB	Zero -1LSB

*Invert the MSB of the offset binary code with an external inverter to obtain two's complement.

Table I. Digital Input Codes

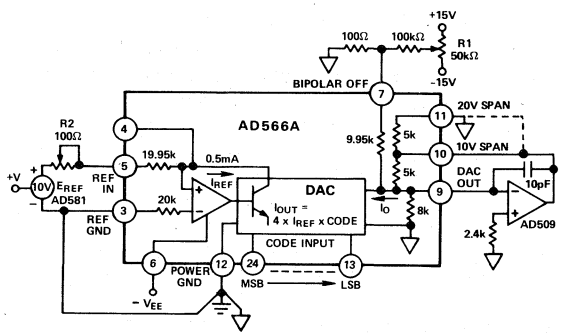


Figure 3. 0 to +10V Unipolar Voltage Output

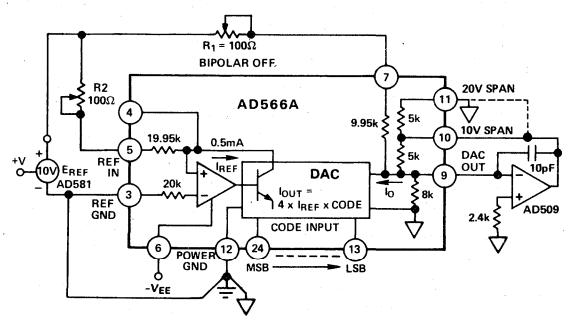
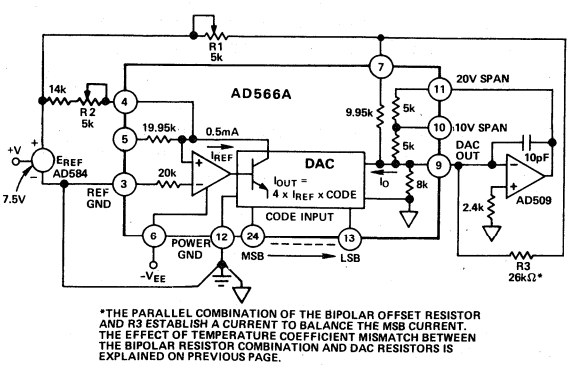


Figure 4. ±5V Bipolar Voltage Output



*THE PARALLEL COMBINATION OF THE BIPOLAR OFFSET RESISTOR AND R3 ESTABLISH A CURRENT TO BALANCE THE MSB CURRENT. THE EFFECT OF TEMPERATURE COEFFICIENT MISMATCH BETWEEN THE BIPOLAR RESISTOR COMBINATION AND DAC RESISTORS IS EXPLAINED ON PREVIOUS PAGE.

Figure 5. ±10V Voltage Output

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 2.0 volts and does not vary with supply voltage. The input lines can interface with any type of 5 volt logic, TTL/DTL or CMOS, and have sufficiently low input currents to interface easily with unbuffered CMOS logic. The configuration of the input circuit is shown in Figure 6. The input line can be modelled as a 30kΩ resistance connected to a -0.7V rail.

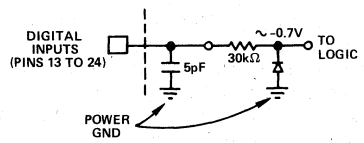


Figure 6. Equivalent Digital Input Circuit

GROUNDING RULES

The AD566A brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds must be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize the current flow in low-level signal paths. In this way, logic gate return currents are not summed into the same return path with analog signals.

The reference ground at pin 3 is the ground point for the internal reference and is thus the "high quality" ground for the AD566A; it should be connected directly to the analog reference point of the system. The power ground at pin 12 can be connected to the most convenient ground point; analog power return is preferred. If the power ground contains high frequency noise in excess of 200mV, this noise may feed through to the output of the converter; thus some caution is required in applying these grounds.

OUTPUT VOLTAGE COMPLIANCE

The AD566A has a typical output compliance range of -2 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8kΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are a function of output current and negative supply, as shown in Figure 7.

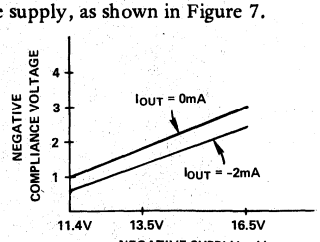


Figure 7. Typical Neg. Compliance Range vs. Neg. Supply

HIGH SPEED SYSTEM DESIGN

Full realization of the AD566A high speed capabilities requires strict attention to detail by the user in all areas of application and testing.

The settling time for the AD566A is specified for the current output, an inherently high speed DAC operating mode. However, most DAC applications require a current-to-voltage conversion at some point in the signal path, although an unbuffered voltage level (not using an op amp) is suitable for use in a successive-approximation A/D converter or in many display applications (see next page). With proper design this form of current-to-voltage conversion can give very fast operation. The fastest voltage conversion is achieved by connecting a low value resistor directly to the output, as shown in Figure 8. In this case, the settling time is primarily determined by the cell switching time and by the RC time constant of the AD566A output capacitance of 25 picofarads (plus stray capacitance) combined with the output resistor value. Settling to 0.01% of full scale (for a full scale transition) requires 9 time constants. This effect is important for an equivalent resistance over 1kΩ.

If an op amp is used to provide a low impedance output signal, some loss in settling time will be seen due to op amp dynamics. The normal current-to-voltage converter op amp circuits, based on the fast settling AD509, are shown in the applications circuit. The unipolar or bipolar circuits shown settle to ±1/2LSB in 1μs. The DAC output capacitance, which acts as a stray capacitance at the op amp inverting input, must be compensated by a feedback capacitor as shown. The value should be chosen carefully for each application and each op amp type.

Fastest operation will be obtained by minimizing lead lengths, stray capacitance and impedance levels. The supply should be bypassed near the device; 0.1μF will be sufficient since the AD566A runs at constant supply current regardless of input code. Output capacitance effects can be minimized by grounding pin 11 in 10V span applications.

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar output resistors to give a ±1.60 volt bipolar swing. In this situation, the digital code is complementary binary. Other combinations of internal and external output resistors (R_X) can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to -2mA unipolar output current and using the 10.0 volt reference voltage for bipolar offset. For example, setting R_X = 2.67kΩ gives a ±1 volt range with a 1kΩ equivalent output impedance.

This connection is especially useful for directly driving a long cable at high speed. A 50Ω R_X resistor drives a 50Ω cable with a ±50mV full scale swing; settling time is very fast as discussed in the section above.

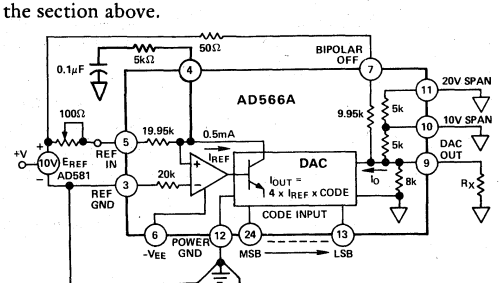


Figure 8. Unbuffered Bipolar Voltage Output

MICROPROCESSOR CONTROL FOR A 12-BIT DAC

A common I/O interface is the Digital-to-Analog Converter output, which provides a voltage corresponding to a data word from a microprocessor.

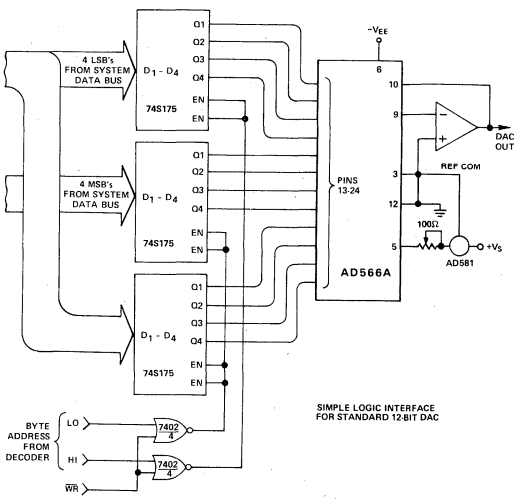


Figure 9.

Interfacing is more complex when the DAC needs more bits of resolution than the system data bus can carry in 1 byte. For example, applications using an 8-bit microprocessor to drive a 12-bit DAC are common. Several hardware formats are possible; the most convenient one depends on the desired data format. If the least significant 8 bits are in one byte of memory, they can be transferred into an 8-bit latch in one memory-or I/O-write cycle. An adjacent cycle can be used to transfer the 4 least-significant bits of another data word into a latch controlling the 4 most-significant bits of the DAC. The least-significant bits of the data bus drive two 4-bit latches which are controlled by two separate addresses. The Hi Byte address allows the microprocessor to write in the 4 most significant data bits and the Lo Byte address allows the microprocessor to write in the 8 remaining bits. When all 12 bits are latched, the DAC output will assume its proper new value. An intermediate value will be momentarily present at the DAC terminals between Hi and Lo Byte write cycles. For applications such as CRT displays where this intermediate value cannot be tolerated, double buffering can be effectively employed. This could be implemented with a separately-controlled 12-bit latch at the DAC inputs or a sample and hold amplifier on the output.

D/A CONVERTER DISPLAYS

In Figure 10, a counter-driven AD566A is shown as a sawtooth sweep generator. When used for displays, this scheme provides a highly-repeatable, controllable linear sweep.

Raster displays are usually generated by a fast horizontal scan and a slower vertical scan which is derived from the horizontal scan. Intensity modulation during each horizontal scan provides the pictorial information. The picture resolution is expressed in terms of the number of discernible data points per line multiplied by the number of lines. The minimum frame period is the time allowed for the horizontal scan-plus-retrace multiplied by the number of lines, plus vertical retrace time.

A family of monolithic D/A converters is available from Analog Devices that are suitable for vertical sweeps. The line-spacing uniformity depends on linearity while maximum number of lines depends on DAC resolution. A display of 1024 lines would require 10 bits of resolution and 12 bits of linearity (0.012% of linearity provides less than 12% of spacing error). Switching transients created within the vertical sweep DAC are blanked because they occur during the horizontal retrace interval.

For horizontal sweeps, the DAC requirements are more severe. For example, to resolve 500 points per line, at 500 lines per frame, at a 30Hz frame rate, requires that each digital horizontal step settle within 100ns (typical full scale settling time is 200ns), and that there be no "glitches". Even if the display is blanked between horizontal steps, large glitches at major carries can cause deflection-amplifier transients, which distort the pattern.

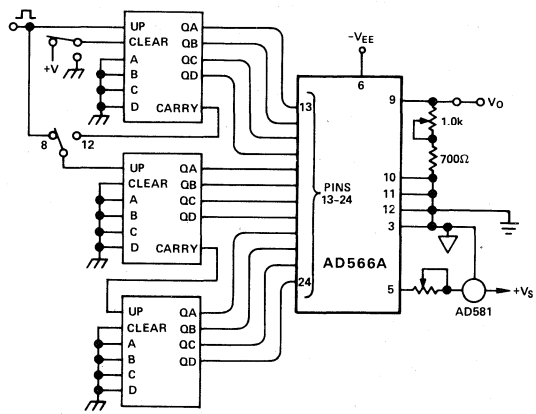


Figure 10.

The excellent high speed performance of the AD566A is demonstrated in the oscilloscope photograph of Figure 11. This measurement is made with the AD566A driving directly into an equivalent 50Ω load, amplified with a low capacitance MOS-input, UHF amplifier. The figure shows the worst case situation, which is full scale transition from switching all bits OFF to ON. The equipment and circuitry used to make the measurements adds about 50ns to the actual device performance.

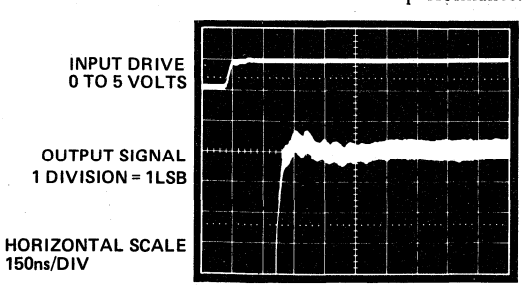


Figure 11. Settling Characteristic Detail

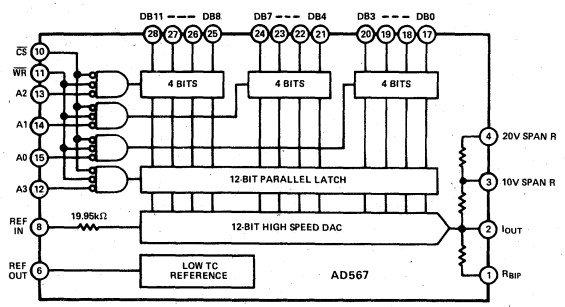
Microprocessor-Compatible 12-Bit D/A Converter

AD567*

FEATURES

Single Chip Construction
Double-Buffered Latch for 8-Bit μP-Compatibility
Fast Settling Time: 500ns max to ±1/2LSB
High Stability Buried Zener Reference on Chip
Monotonicity Guaranteed Over Temperature
Linearity Guaranteed Over Temperature: 1/2LSB max (AD567K)
Guaranteed for Operation with ±12V or ±15V Supplies
Low Power: 300mW Including Reference
TTL/5V CMOS Compatible Logic Inputs

AD567 FUNCTIONAL BLOCK DIAGRAM



28-PIN DIP

PRODUCT DESCRIPTION

The AD567 is a complete high speed 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD567 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD567 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K grade) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD567 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 10ppm/°C.

The AD567 is available in three performance grades. The AD567J and K are specified for use over the 0 to +70°C temperature range and are available in either a 28-pin hermetically-sealed, ceramic DIP or a 28-pin molded plastic DIP (N package). The AD567S is specified for the −55°C to +125°C range and is available in the ceramic package.

PRODUCT HIGHLIGHTS

1. The AD567 is a complete current output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The chip also contains SiCr thin film application resistors which can be used either with an external op amp to provide a precision voltage output or as input resistors for an A/D converter. The resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current switch design* provides high dc accuracy and an optimally-damped settling characteristic. Output current settling time is 500 nanoseconds maximum to ±1/2LSB.

SPECIFICATIONS (T_A = +25°C, V_{CC} = +12V or +15V, V_{EE} = -12V or -15V, unless otherwise specified)

MODEL	AD567J MIN	AD567J TYP	AD567J MAX	AD567K MIN	AD567K TYP	AD567K MAX	UNITS
DATA INPUTS[1] (Pins 10–15 and 17–28)							
TTL or 5 Volt CMOS							
Input Voltage							
Bit ON Logic "1"	**+2.0**		**+5.5**	**+2.0**		**+5.5**	V
Bit OFF Logic "0"			**+0.8**			**+0.8**	V
Logic Current (each bit)							
Bit ON Logic "1"		+120	**+300**		+120	**+300**	μA
Bit OFF Logic "0"		+35	**+100**		+35	**+100**	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current							
Unipolar (all bits on)	**-1.6**	-2.0	**-2.4**	**-1.6**	-2.0	**-2.4**	mA
Bipolar (all bits on or off)	**±0.8**	±1.0	**±1.2**	**±0.8**	±1.0	**±1.2**	mA
Resistance (exclusive of span resistors)	6k	8k	10k	6k	8k	10k	Ω
Offset							
Unipolar		0.01	**0.05**		0.01	**0.05**	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	**0.15**		0.05	**0.1**	% of F.S. Range
Capacitance		25			25		pF
Compliance Voltage							
T_{min} to T_{max}	-1.5		+10	-1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	**±1/2**		±1/8	**±1/4**	LSB
		(0.006)	**(0.012)**		(0.003)	**(0.006)**	% of F.S. Range
T_{min} to T_{max}		±1/2	**±3/4**		±1/4	**±1/2**	LSB
		(0.012)	**(0.018)**		(0.006)	**(0.012)**	% of F.S. Range
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	**±3/4**		±1/4	**±1/2**	LSB
T_{min} to T_{max}	**MONOTONICITY GUARANTEED**			**MONOTONICITY GUARANTEED**			
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	**2**		1	**2**	ppm/°C
Bipolar Zero		5	**10**		5	**10**	ppm/°C
Gain (Full Scale)		15	**50**		10	**20**	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
TEMPERATURE RANGE							
Operating	0		+70	0		+70	°C
Storage	-65		+150	-65		+150	°C
POWER REQUIREMENTS							
V_{CC}, +11.4 to +16.5V dc		3	**5**		3	**5**	mA
V_{EE}, -11.4 to -16.5V dc		-17	**-25**		-17	**-25**	mA
POWER SUPPLY GAIN SENSITIVITY[2]							
V_{CC} = +11.4 to +16.5V dc		3	**10**		3	**10**	ppm of F.S./%
V_{EE} = -11.4 to -16.5V dc		15	**25**		15	**25**	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGE (see Figures 1, 2, 3)		0 to +5			0 to +5		V
		-2.5 to +2.5			-2.5 to +2.5		V
		0 to +10			0 to +10		V
		-5 to +5			-5 to +5		V
		-10 to +10			-10 to +10		V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 2)		±0.1	**±0.25**		±0.1	**±0.25**	% of F.S. Range
Bipolar Zero Error with Fixed 50Ω Resistor for R1 (Figure 3)		±0.05	**±0.15**		±0.05	**±0.1**	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S. Range
REFERENCE INPUT							
Input Impedance	15k	20k	25k	15k	20k	25k	Ω
REFERENCE OUTPUT							
Voltage	**9.90**	10.00	10.10	**9.90**	10.00	**10.10**	V
Current (available for external loads)	**0.1**	1.0		**0.1**	1.0		mA
POWER DISSIPATION		300	495		300	495	mW
PACKAGE[3] Ceramic DIP (D28A)		AD567JD			AD567KD		
Plastic DIP (N28A)		AD567JN			AD567KN		

NOTES

[1] The digital input specifications are guaranteed but not tested over the operating temperature range.

[2] The power supply gain sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V dc ±10%.

[3] See Section 19 for package outline information.

Specifications subject to change without notice.

MODEL	AD567SD MIN	TYP	MAX	UNITS
DATA INPUTS[1] (Pins 10–15 and 17–28)				
TTL or 5 Volt CMOS				
Input Voltage				
Bit ON Logic "1"	**+2.0**		**+5.5**	V
Bit OFF Logic "0"			**+0.7**	V
Logic Current (each bit)				
Bit ON Logic "1"		+120	**+300**	μA
Bit OFF Logic "0"		+35	**+100**	μA
RESOLUTION			12	Bits
OUTPUT				
Current				
Unipolar (all bits on)	**−1.6**	−2.0	**−2.4**	mA
Bipolar (all bits on or off)	**±0.8**	±1.0	**±1.2**	mA
Resistance (exclusive of span resistors)	6k	8k	10k	Ω
Offset				
Unipolar		0.01	**0.05**	% of F.S. Range
Bipolar (Figure 3, R_2 = 50Ω fixed)		0.05	**0.15**	% of F.S. Range
Capacitance		25		pF
Compliance Voltage				
T_{min} to T_{max}	−1.5		+10	V
ACCURACY (error relative to full scale) +25°C		±1/4	**±1/2**	LSB
		(0.006)	**(0.012)**	% of F.S. Range
T_{min} to T_{max}		±1/2	**±3/4**	LSB
		(0.012)	**(0.018)**	% of F.S. Range
DIFFERENTIAL NONLINEARITY				
+25°C		±1/2	**±3/4**	LSB
T_{min} to T_{max}	**MONOTONICITY GUARANTEED**			
TEMPERATURE COEFFICIENTS				
With Internal Reference				
Unipolar Zero		1	**2**	ppm/°C
Bipolar Zero		5	**10**	ppm/°C
Gain (Full Scale)		15	**30**	ppm/°C
Differential Nonlinearity		2		ppm/°C
TEMPERATURE RANGE				
Operating	−55		+125	°C
Storage	−65		+150	°C
POWER REQUIREMENTS				
V_{CC}, +11.4 to +16.5V dc		3	**5**	mA
V_{EE}, −11.4 to −16.5V dc		−17	**−25**	mA
POWER SUPPLY GAIN SENSITIVITY[2]				
V_{CC} = +11.4 to +16.5V dc		3	**10**	ppm of F.S./%
V_{EE} = −11.4 to −16.5V dc		15	**25**	ppm of F.S./%
PROGRAMMABLE OUTPUT				
RANGES (see Figures 1, 2, 3)		0 to +5		V
		−2.5 to +2.5		V
		0 to +10		V
		−5 to +5		V
		−10 to +10		V
EXTERNAL ADJUSTMENTS				
Gain Error with Fixed 50Ω				
Resistor for R2 (Figure 2)		±0.1	±0.25	% of F.S. Range
Bipolar Zero Error with Fixed				
50Ω Resistor for R1 (Figure 3)		±0.05	±0.15	% of F.S. Range
Gain Adjustment Range (Figure 2)	±0.25			% of F.S. Range
Bipolar Zero Adjustment Range	±0.15			% of F.S. Range
REFERENCE INPUT				
Input Impedance	15k	20k	25k	Ω
REFERENCE OUTPUT				
Voltage	**9.90**	10.00	**10.10**	V
Current (available for external loads)	**0.1**	1.0		mA
POWER DISSIPATION		300	495	mW
PACKAGE[3] (D28A)		AD567SD		

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

TIMING SPECIFICATIONS

(All Models, T_A = 25°C, V_{CC} = +12V or +15V, V_{EE} = −12V or −15V)

Symbol	Parameter	Min	Typ	Max	
t_{DW}	Data Valid to End of $\overline{WR}$	50	–	–	ns
t_{CW}	$\overline{CS}$ Valid to End of $\overline{WR}$	100	–	–	
t_{AW}	Address Valid to End of $\overline{WR}$	100	–	–	ns
t_{WP}	Write Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Current Settling Time	–	400	500	ns

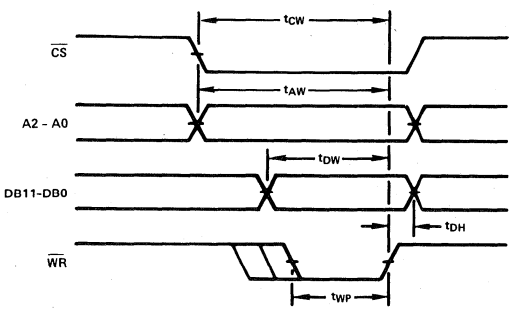
ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . .0V to +18V
V_{EE} to Power Ground . . . . . .0V to −18V
Voltage on DAC Output (Pin 2) . . . . . −3V to +12V
Digital Inputs (Pins 10–15, 17–28)
to Power Ground. . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out. . . . . .Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

TIMING DIAGRAMS

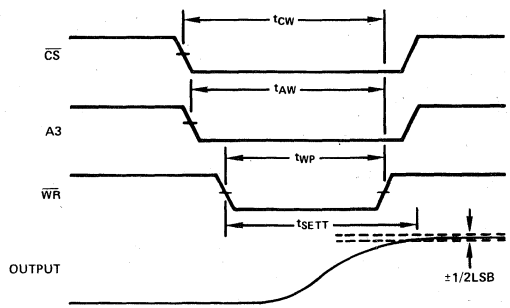
WRITE CYCLE #1

(Load First Rank from Data Bus; A3 = 1)



WRITE CYCLE #2

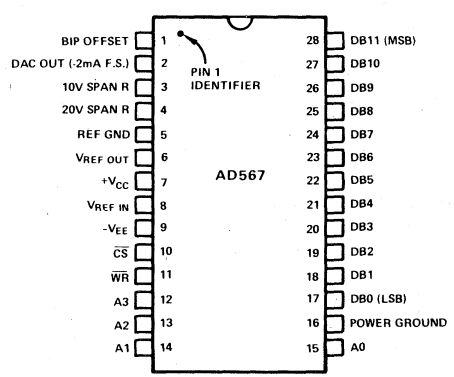
(Load Second Rank from First Rank; A_2, A_1, A_0 = 1)



AD567 ORDERING GUIDE

MODEL	PACKAGE	TEMP RANGE	LINEARITY ERROR MAX @ 25°C	GAIN T.C. MAX
AD567JN	Plastic	Com	±1/2LSB	50ppm/°C
AD567KN	Plastic	Com	±1/4LSB	20ppm/°C
AD567JD	Ceramic	Com	±1/2LSB	50ppm/°C
AD567KD	Ceramic	Com	±1/4LSB	20ppm/°C
AD567SD	Ceramic	Extended	±1/2LSB	30ppm/°C

PIN CONNECTIONS
TOP VIEW



THE AD567 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

RELATIVE ACCURACY: Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. − 1LSB) for any bit combination. The AD567 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K version and 1/2LSB for the J and S.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a non-decreasing function of input. All versions of the AD567 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V x 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be 1.83mV, or 3/4LSB. The AD567K has a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2LSB.

The differential nonlinearity temperature coefficient must also be considered if the device is to remain monotonic over its full operating temperature range. A differential nonlinearity temperature coefficient of 1.0ppm/°C could, under worst case conditions for a temperature change of +25°C to +125°C, add 0.01% (100°C x 1.0ppm/°C) of error. The resulting error could then be as much as 0.01% + 0.006% (initial error, 1/4LSB) = 0.016% of F.S. (1/2LSB represents 0.012% of F.S.). To be sure of accurate performance all versions of the AD567 are 100% tested for monotonicity over the full operating temperature range.

ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L; AD517L; AD741L; AD301AL; AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within ±1/2LSB (plus op amp offset), and full scale accuracy will be within 0.1% (0.25% max). Substituting a 50Ω resistor for the 100Ω bipolar offset trimmer will give a bipolar zero error typically within ±2LSB (0.05%).

The AD544 is recommended for buffered voltage-output applications which require fast settling time to ±1/2LSB. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 25 picofarad DAC output capacitance.

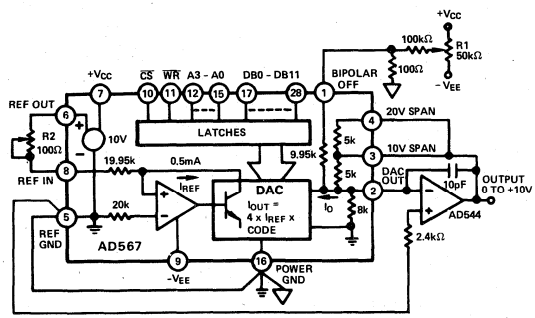


Figure 1. 0 to +10V Unipolar Voltage Output

FIGURE 1. UNIPOLAR CONFIGURATION
This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar terminal, pin 1, should be grounded if not used for trimming.

STEP I . . . ZERO ADJUST
Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 1 should be connected to pin 5.

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 3 to the op amp output.

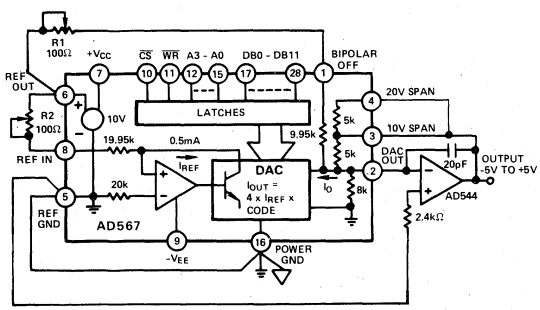


Figure 2. ±5V Bipolar Voltage Output

FIGURE 2. BIPOLAR CONFIGURATION
This configuration will provide a bipolar output voltage from -5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust 100Ω trimmer R1 to give -5.000 volts output.

STEP II . . . GAIN ADJUST
Turn ON All bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

FIGURE 3 OTHER VOLTAGE RANGES

The AD567 can also be easily configured for a unipolar 0 to +5 volt range or ±2.5 volt and ±10 volt bipolar ranges by using the additional 5k application resistor provided at the 20 volt span R terminal, pin 4. For a 5 volt span (0 to +5 or ±2.5), the two 5k resistors are used in parallel by shorting pin 4 to pin 2 and connecting pin 3 to the op amp output and the bipolar offset either to ground for unipolar or to REF OUT for the bipolar range. For the ±10 volt range (20 volt span) use the 5k resistors in series by connecting only pin 4 to the op amp output and the bipolar offset connected as shown. The ±10 volt option is shown in Figure 3.

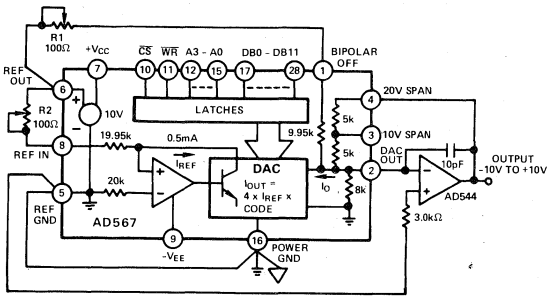


Figure 3. ±10V Voltage Output

The internal resistor values shown in Figures 1, 2, and 3 are nominal values only, as is the output current. These values are subject to an absolute tolerance of approximately ±20%. Furthermore, the resistors in the AD567 exhibit a temperature coefficient of approximately −50ppm/°C. While these absolute tolerances may appear excessively wide, the ratios of the resistor values and tracking TC are extremely well-controlled. In applications where the internal feedback resistor determines the output voltage range it is the ratios which determine the accuracy. However, in applications where the desired full scale range requires use of an external resistor, sufficient trim range must be provided to compensate for the tolerance of the internal resistance.

INTERNAL/EXTERNAL REFERENCE USE

The AD567 has an internal low-noise buried zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete zener reference diodes. The performance of the AD567 is specified with the internal reference driving the DAC since all trimming and testing (especially for full scale error and bipolar offset) is done in this configuration.

The AD567 can be used with an external reference, but may not have sufficient trim range to accommodate a reference which does not match the internal reference.

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 0.5mA to Ref In and 1.0mA to Bipolar Offset). A minimum of 0.1mA is available for driving external loads. The AD567 reference output should be buffered with an external op amp if it is required to supply additional output current. The reference is typically trimmed to ±0.2%, then tested and guaranteed to ±1.0% max error. The temperature coefficient is comparable to that of the full scale TC for a particular grade.

OUTPUT VOLTAGE COMPLIANCE

The AD567 has a typical output compliance range from −1.5 to +10 volts. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 8k in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 4.

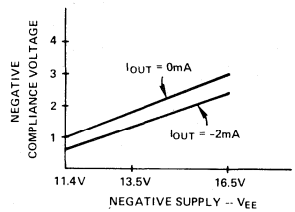


Figure 4. Typical Negative Compliance Range vs. Negative Supply

GROUNDING RULES

The AD567 brings out separate reference and power grounds to allow optimum connections for low noise and high speed performance. These grounds should be tied together at one point, usually the device power ground. The separate ground returns are provided to minimize current flow in low-level signal paths. In this way, logic return currents are not summed into the same return path with analog signals.

The reference ground at pin 5 is the ground point for the internal reference and is thus the "high quality" ground for the AD567; it should be connected directly to the analog reference point of the system. The power ground at pin 16 can be connected to the most convenient ground point; analog power return is preferred. If power ground contains high frequency noise beyond 200mV, this noise may feed through the converter, thus some caution will be required in applying these grounds.

It is also important to properly apply decoupling capacitors on the power supplies for the AD567 and the output amplifier. The correct method for decoupling is to connect a capacitor from each power supply pin of both the AD567 and the amplifier directly to the reference ground pin of the AD567. Any load driven by the output amplifier should also be referred to the reference ground pin.

Output Range	Connect Pin 3 to:	Connect Pin 4 to:	Connect Pin 1 to:
0 to +5V	Amplifier Output	Pin 2	Pin 5
0 to +10V	Amplifier Output	Amplifier Output	Pin 5
−2.5V to +2.5V	Amplifier Output	Pin 2	Pin 6 (through 50Ω)
−5V to +5V	Amplifier Output	Amplifier Output	Pin 6 (through 50Ω)
−10V to +10V	—	Amplifier Output	Pin 6 (through 50Ω)

Table I. Connections for Various Output Ranges

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD567 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values. Figure 5 shows the block diagram of the AD567 logic section.

The latches are controlled by the address inputs, A0–A3, and the $\overline{CS}$ and $\overline{WR}$ inputs. All control inputs are active low, consistent with general practice in microprocessor systems. The $\overline{CS}$ and $\overline{WR}$ inputs must both be low for any operation to occur. The four address lines each enable one of the four latches, as indicated in Table II below.

All latches in the AD567 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

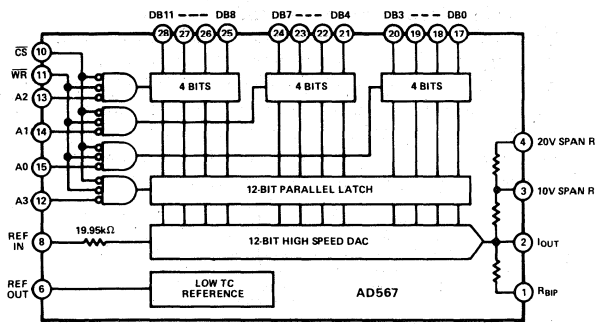


Figure 5. AD567 Block Diagram

$\overline{CS}$	$\overline{WR}$	A3	A2	A1	A0	Operation
1	X	X	X	X	X	No Operation
X	1	X	X	X	X	No Operation
0	0	1	1	1	0	Enable 4 LSBs of First Rank
0	0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table II. AD567 Truth Table

MICROPROCESSOR BUS INTERFACING

The AD567 interface logic is configured with enough flexibility to allow relatively simple interface to the various microprocessor bus structures. The required control signals, $\overline{CS}$ and $\overline{WR}$, are easily derived in most systems. Usually a base address is decoded, and this active-low signal is used for $\overline{CS}$ (Chip Select). Either I/O Write or Memory Write can be used for $\overline{WR}$, depending on the system design. The relative timing of these signals is not important and they are interchangeable.

The address lines determine which of the latches are being enabled. It is permissible to enable two or more latches simultaneously, as in the examples of 8-, 12-, and 16-bit interfaces.

The double-buffered latch permits data to be loaded into the first rank latches of several AD567s and subsequently strobed into the second rank registers of all the DACs. All analog outputs will then update simultaneously.

4-BIT PROCESSOR INTERFACE

Many industrial control applications use four-bit microprocessors but require 12-bit accurate analog control voltages. The AD567 is well suited to these applications, due to its flexible control structure.

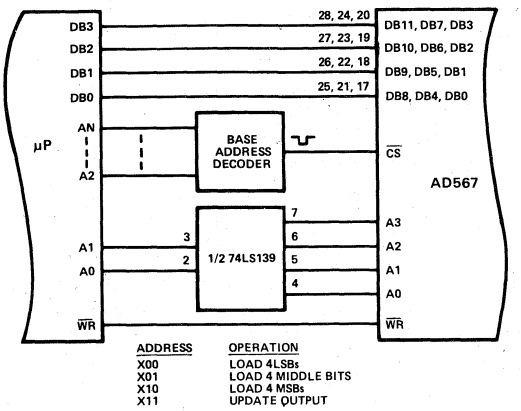


Figure 6. Addressing for 4-Bit Microprocessor Interface

Each AD567 occupies four locations in a 4-bit microprocessor system. A single 74LS139 2-to-4 decoder is used to provide sequential addresses for the four AD567 registers. $\overline{CS}$ is derived from an address decoder driven from the high order address bits. The system $\overline{WR}$ is used for the $\overline{WR}$ input of the AD567.

8-BIT MICROPROCESSOR INTERFACE

The AD567 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

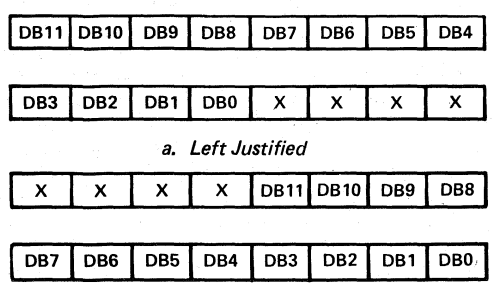


Figure 7. 12-Bit Data Formats for 8-Bit Systems

Figure 8 shows an addressing scheme for use with an AD567 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD567 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

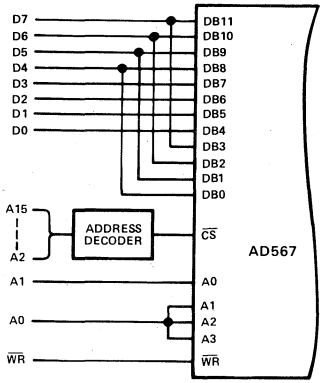


Figure 8. Left-Justified 8-Bit Bus Interface

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD567 still occupies two adjacent locations in the processor's memory map.

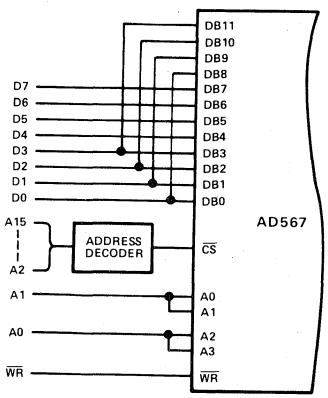
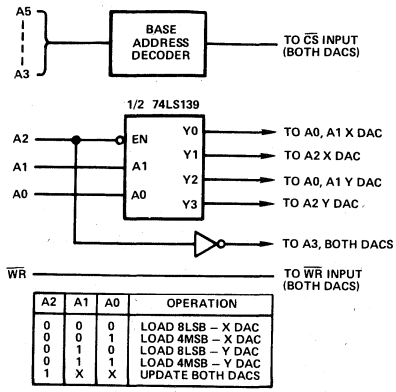


Figure 9. Right-Justified 8-Bit Bus Interface

USING MULTIPLE AD567 DACS IN 8-BIT SYSTEMS

Many applications use multiple digital-to-analog converters driven from the same data bus. For example, automatic test equipment systems often require all analog outputs to be produced simultaneously. Vector-scan graphic systems require that the X and Y coordinates of the stroke endpoints be updated simultaneously. The AD567 can be used with a very simple address decoder to perform this function, as shown in Figure 10. The 74LS139 two-line to four-line decoder and one inverter provide a set of distinct address pulses which assign the registers of the two DACs to a block of consecutive memory locations. In this circuit, write operations to addresses X000 and X001 load the first rank registers of one DAC in a right-justified data format. Addresses X010 and X011 load the first rank of another DAC, also in a right-justified format. A write to any address from X100 to X111 will load the second rank registers of both DACs simultaneously from their respective first rank registers.



A2	A1	A0	OPERATION
0	0	0	LOAD 8LSB – X DAC
0	0	1	LOAD 4MSB – X DAC
0	1	0	LOAD 8LSB – Y DAC
0	1	1	LOAD 4MSB – Y DAC
1	X	X	UPDATE BOTH DACS

Figure 10. Addressing for Two DACs (Right-Justified) on 8-Bit Bus

USING THE AD567 WITH 12- AND 16-BIT BUSES

The AD567 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied to low, and the latch is enabled by $\overline{CS}$ and $\overline{WR}$ going low. The AD567 thus occupies a single memory location.

This configuration renders the second rank register transparent, using the first rank of registers as the data latch. The $\overline{CS}$ input can be driven from an active-low decoded address, and $\overline{WR}$ can be the system $\overline{WR}$ signal. It should be noted that any data bus activity during the period when $\overline{CS}$ and $\overline{WR}$ are both active will cause activity at the AD567 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

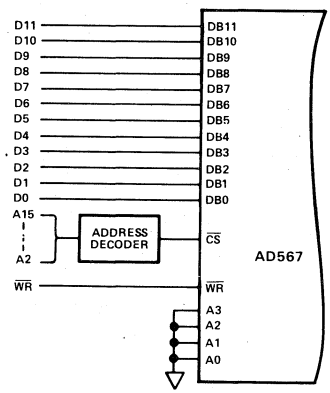


Figure 11. Connections for 12- and 16-Bit Bus Interface

DIGITAL INPUT CONSIDERATIONS

The threshold of the digital input circuitry is set at 1.4 volts and does not vary with supply voltage. The input lines can thus interface with any type of 5 volt logic. The configuration of the input circuit is shown in Figure 12. The input line can be modeled as a 30kΩ resistance connected to a –0.7V rail, in parallel with a 5pF capacitance to ground.

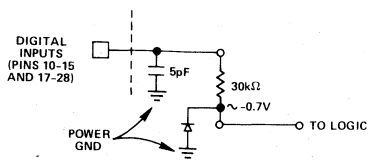


Figure 12. Equivalent Digital Input Circuit

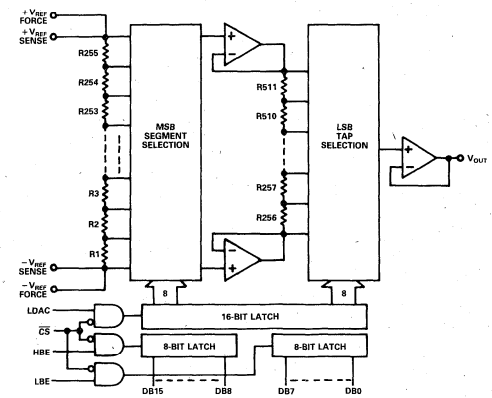
ANALOG DEVICES

Monolithic 16-Bit DAC

AD569

FEATURES
Guaranteed 16-Bit Monotonicity
Voltage Output, 6μs Settling Time
Monolithic BIMOS Construction
±0.02% Nonlinearity
8- and 16-Bit Bus Compatible
6μs Settling Time
Low Drift
Low Power: 150mW
Low Cost

AD569 FUNCTIONAL BLOCK DIAGRAM



9

PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit Digital-to-Analog Converter (DAC) manufactured in Analog Devices' new BIMOS process. This process allows the fabrication of low power CMOS logic functions on the same chip as high speed precision bipolar linear circuitry. The AD569 includes two resistor ladders, selector switches, decoding logic, buffer amplifiers, and double-buffered input latches on the same chip.

The voltage-segmented architecture of the AD569 insures 16-bit monotonicity without linearity trimming of any kind and extremely low gain drift. Integral linearity is maintained at ±0.01%, while differential linearity is ±0.00076%. The on-chip high-speed buffer amplifiers provide voltage output settling time of 6μs to within ±0.001% for a full-scale step.

The output range is determined by the reference input voltage, and can be either unipolar or bipolar. Nominal reference range is ±5V. Separate connections are provided for reference force and sense, in order to preserve absolute accuracy. The AD569 may also be used with a variable or ac reference in multiplying applications.

Data may be loaded into the AD569 latches from either 8- or 16-bit data buses. The double-buffered latches simplify interfacing to 8-bit buses, and allow multiple DACs to be loaded asynchronously and updated simultaneously. The latches are controlled by the CS, LBE, HBE, and LDAC signals. All inputs are TTL/LSTTL/5V CMOS compatible.

The AD569 is available in four grades: JN and KN versions are specified from 0 to +70°C and are packaged in a 28-pin plastic DIP; AD and BD versions are specified from −25°C to +85°C and are packaged in a 28-pin ceramic DIP.

PRODUCT HIGHLIGHTS

1. BIMOS processing allows low power CMOS digital circuits to be integrated with high precision bipolar linear circuits on a single chip.
2. Monotonicity to 16 bits over temperature is insured by the voltage-segmented architecture used in the AD569.
3. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift are negligible.
4. The AD569's versatile data input structure allows loading from either 8- or 16-bit buses.
5. The on-chip output buffer amplifier can supply ±5V into a 1kΩ load, and can drive capacitive loads up to 1000pF without oscillation.
6. Kelvin connections to the reference inputs preserve the absolute accuracy of the transfer function in the presence of wiring resistances and ground loops.

SPECIFICATIONS (T_A = +25°C, $+V_S$ = +12V, $-V_S$ = −12V, $+V_{REF}$ = +5V, $-V_{REF}$ = −5V, unless otherwise noted)

Model	AD569JN/AD			AD569KN/BD			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
RESOLUTION			16			16	Bits
LOGIC INPUTS							
Logic "1"	2.0		5.5	2.0		5.5	Volts
Logic "0"	0		0.8	0		0.8	Volts
TRANSFER FUNCTION CHARACTERISTICS							
Gain Error	−2		+2	−2		+2	LSB[1]
T_{min} to T_{max}	−3		+3	−3		+3	LSB
Integral Nonlinearity	−0.025		+0.025	−0.02		+0.02	%FSR[2]
T_{min} to T_{max}	−0.05		+0.05	−0.04		+0.04	%FSR
Differential Nonlinearity	−1		+1	−1/2		+1/2	LSB
T_{min} to T_{max}	−1		+1	−1		+1	LSB
Unipolar Offset	−400		+400	−200		+200	μV
T_{min} to T_{max}	−800		+800	−300		+300	μV
Bipolar Zero	−200		+200	−100		+100	μV
T_{min} to T_{max}	−800		+800	−300		+300	μV
REFERENCE INPUT							
$+V_{REF}$ Range	−5		+5	−5		+5	V
$-V_{REF}$ Range	−5		+5	−5		+5	V
Resistance	18	23	28	18	23	28	kΩ[3]
OUTPUT CHARACTERISTICS							
Voltage	−5		+5	−5		+5	V
Current	−5		+5	−5		+5	mA
Capacitive Load			1000			1000	pF
Settling Time		6			6		μs[4]
LOGIC TIMING							
Pulse Width (HBE, LBE, CS, LDAC)	100			100			ns
Data Setup Time	50			50			ns
Data Hold Time	30			30			ns
POWER SUPPLIES							
Voltage							
$+V_S$	+11.4	+12	+12.6	+11.4	+12	+12.6	Volts
$-V_S$	−11.4	−12	−12.6	−11.4	−12	−12.6	Volts
Current							
$+I_S$		+6	+8		+6	+8	mA
$-I_S$	−8	−6		−8	−6		mA
Power Supply Gain Sensitivity	−1		+1	−1		+1	ppm/% Change
TEMPERATURE RANGE							
Specified							
JN, KN	0		+70	0		+70	°C
AD, BD	−25		+85	−25		+85	°C
Storage							
JN, KN	−65		+150	−65		+150	°C
AD, BD	−65		+150	−65		+150	°C
PACKAGE STYLE[5]							
JN, KN				N28A			
AD, BD				D28A			

NOTES

[1]Gain error is actually a dc voltage error equal to 2LSBs for a 10V FSR (approximately 300μV). Of course, at lower FS ranges, this fixed error will represent a greater number of LSBs.

[2] FSR stands for Full Scale Range, and is 10V for a −5 to +5V span.

[3]Measured between $+V_{REF}$ Force and $-V_{REF}$ Force.

[4]Settling time is measured for a 10V step on the output settling to ±0.001%

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

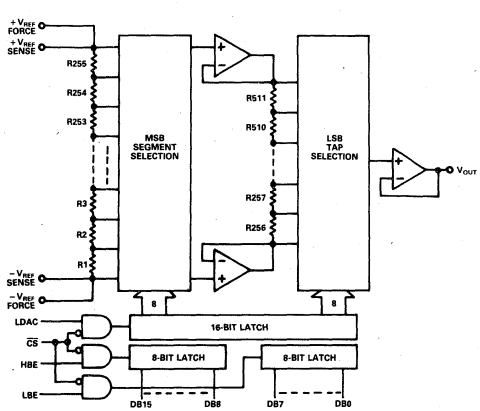


Figure 1. AD569 Block Diagram

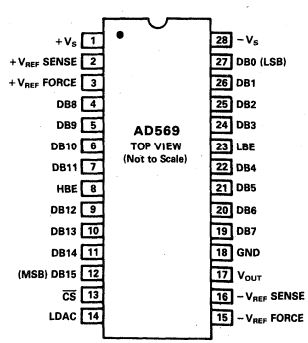


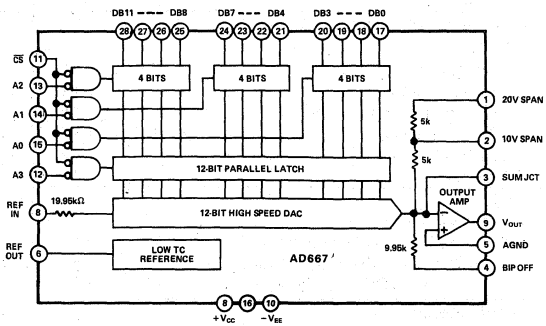
Figure 2. AD569 Pin Out in 28-Pin Package

Microprocessor-Compatible 12-Bit D/A Converter

AD667*

FEATURES
- **Complete 12-Bit D/A Function**
  - **Double-Buffered Latch**
  - **On Chip Output Amplifier**
  - **High Stability Buried Zener Reference**
- **Single Chip Construction**
- **Monotonicity Guaranteed Over Temperature**
- **Linearity Guaranteed Over Temperature: 1/2LSB max**
- **Settling Time: 4μs max to 0.01%**
- **Guaranteed for Operation with ±12V or ±15V Supplies**
- **Low Power: 300mW Including Reference**
- **TTL/5V CMOS Compatible Logic Inputs**

AD667 FUNCTIONAL BLOCK DIAGRAM



9

PRODUCT DESCRIPTION

The AD667 is a complete, voltage output, 12-bit digital-to-analog converter including a high stability buried zener voltage reference and double-buffered input latch on a single chip. The converter uses 12 precision high speed bipolar current steering switches and a laser trimmed thin film resistor network to provide fast settling time and high accuracy.

Microprocessor compatibility is achieved by the on-chip double-buffered latch. The design of the input latch allows direct interface to 4-, 8-, 12-, or 16-bit buses. The 12 bits of data from the first rank of latches can then be transferred to the second rank, avoiding generation of spurious analog output values. The latch responds to strobe pulses as short as 100ns, allowing use with the fastest available microprocessors.

The functional completeness and high performance in the AD667 results from a combination of advanced switch design, high speed bipolar manufacturing process, and the proven laser wafer-trimming (LWT) technology. The AD667 is trimmed at the wafer level and is specified to ±1/4LSB maximum linearity error (K, B grades) at 25°C and ±1/2LSB over the full operating temperature range.

The subsurface (buried) Zener diode on the chip provides a low-noise voltage reference which has long-term stability and temperature drift characteristics comparable to the best discrete reference diodes. The laser trimming process which provides the excellent linearity, is also used to trim both the absolute value of the reference as well as its temperature coefficient. The AD667 is thus well suited for wide temperature range performance with ±1/2LSB maximum linearity error and guaranteed monotonicity over the full temperature range. Typical full scale gain T.C. is 5ppm/°C.

***Covered by Patent Numbers 3,803,590; 3,890,611; 3,932,863; 3,978,473; 4,020,486; and others pending.**

The AD667 is available in five performance grades. The AD667JN and KN are specified for use over the 0 to +70°C temperature range and are available in a 28-pin molded plastic DIP (N package). The AD667S grade is specified for the −55°C to +125°C range and is available in the ceramic or LCC package. The AD667A and B are specified for use over the −25°C to +85°C temperature range and are available in either a 28-pin hermetically sealed ceramic DIP or LCC package.

PRODUCT HIGHLIGHTS

1. The AD667 is a complete voltage output DAC with voltage reference and digital latches on a single IC chip.
2. The double-buffered latch structure permits direct interface to 4-, 8-, 12-, or 16-bit data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. The internal buried zener reference is laser-trimmed to 10.00 volts with a ±1% maximum error. The reference voltage is also available for external application.
4. The gain settling and bipolar offset resistors are matched to the internal ladder network to guarantee a low gain temperature coefficient and are laser-trimmed for minimum full scale and bipolar offset errors.
5. The precision high speed current switch steering and on-board high speed output amplifier have been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs when properly compensated.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted)

Model	AD667J			AD667K			Units
	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUTS							
Resolution			12			12	Bits
Logic Levels (TTL Compatible)[1]							
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)			300			300	μA
I_{IL} (V_{IL} = 0.8V)			100			100	μA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2	LSB
$T_A = T_{min}$ to T_{max}		Monotonicity Guaranteed			Monotonicity Guaranteed		LSB
Gain Error[2]		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Offset Error[2]		±1	±2		±1	±2	LSB
DRIFT							
Differential Linearity		±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} on T_{max}		±5	±30		±5	±15	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} on T_{max}		±1	±3			±3	ppm of FSR/°C
Bipolar Offset T_A = 25°C to T_{min} on T_{max}		±5	±10			±10	ppm of FSR/°C
CONVERSION SPEED							
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)							
with 10kΩ Feedback		3	4		3	4	μs
with 5kΩ Feedback		2	3		2	3	μs
For LSB Change		1			1		μs
Slew Rate	10			10			V/μs
ANALOG OUTPUT							
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			mA
Output Impedance (dc)		0.05			0.05		Ω
Short Circuit Current			40			40	mA
Reference Output	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY							
V_{CC} = +11.4 to +16.5V dc		15	25		15	25	ppm of FS/%
V_{EE} = −11.4 to +16.5V dc		3	10		3	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS							
Rated Voltages		±15			±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	V
Supply Drain							
+11.4 to +16.5V dc		5	8.5		5	8.5	mA
−11.4 to +16.5V dc		18	25		18	25	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]The digital input specifications are guaranteed but not tested over the temperature range.
[2]Adjustable to zero.
[3]FSR means "Full Scale Range" and is 20V for ±10V range and 10V for the ±5V range.
[4]A minimum power supply of ±12.5V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD667A			AD667B			AD667S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DIGITAL INPUT										
Resolution			12			12			12	Bits
Logic Levels (TTL Compatible)[1]										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.7	V
I_{IH} (V_{IH} = 5.5V)			300			300			300	µA
I_{IL} (V_{IL} = 0.8V)			100			100			100	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C		±1/4	±1/2		±1/8	±1/4		±1/8	±1/2	LSB
$T_A = T_{min}$ to T_{max}		±1/2	±3/4		±1/4	±1/2		±1/2	±3/4	LSB
Differential Linearity Error @ +25°C		±1/2	±3/4		±1/4	±1/2			±3/4	LSB
$T_A = T_{min}$ to T_{max}	Monotonicity Guaranteed			Monotonicity Guaranteed			Monotonicity Guaranteed			LSB
Gain Error[2]		±0.1	±0.3		±0.1	±0.2		±0.1	±0.2	%FSR[3]
Offset Error[2]		±1	±2		±1	±2		±1	±2	LSB
DRIFT										
Differential Linearity		±2			±2			±2		ppm of FSR/°C
Gain (Full Scale) T_A = 25°C to T_{min} on T_{max}		±5	±30		±5	±15		±15	±30	ppm of FSR/°C
Unipolar Offset T_A = 25°C to T_{min} on T_{max}		±1	±3			±3			±3	ppm of FSR/°C
Bipolar Offset T_A = 25°C to T_{min} on T_{max}		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩ Feedback		3	4		3	4		3	4	µs
with 5kΩ Feedback		2	3		2	3		2	3	µs
For LSB Change		1			1			1		µs
Slew Rate	10			10			10			V/µs
ANALOG OUTPUT										
Ranges[4]		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Reference Output	9.90	10.00	10.10	9.90	10.00	10.10	9.90	10.00	10.10	V
External Current	0.1	1.0		0.1	1.0		0.1	1.0		mA
POWER SUPPLY SENSITIVITY										
V_{CC} = +11.4 to +16.5V dc		15	25		15	25		15	25	ppm of FS/%
V_{EE} = −11.4 to +16.5V dc		3	10		3	10		3	10	ppm of FS/%
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range[4]	±11.4		±16.5	±11.4		±16.5	±11.4		±16.5	V
Supply Drain										
+11.4 to +16.5V dc		5	8.5		5	8.5		5	8.5	mA
−11.4 to +16.5V dc		18	25		18	25		18	25	mA
TEMPERATURE RANGE										
Specification	−25		+85	−25		+85	−55		+125	°C
Operating	−55		+125	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	−65		+150	°C

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TIMING SPECIFICATIONS

(All Models, $T_A = 25°C$, $V_{CC} = +12V$ or $+15V$, $V_{EE} = -12V$ or $-15V$)

Symbol	Parameter	Min	Typ	Max	
t_{DC}	Data Valid to End of $\overline{CS}$	50	–	–	ns
t_{AC}	Address Valid to End of $\overline{CS}$	100	–	–	ns
t_{CP}	$\overline{CS}$ Pulse Width	100	–	–	ns
t_{DH}	Data Hold Time	0	–	–	ns
t_{SETT}	Output Voltage Settling Time	–	2	4	µs

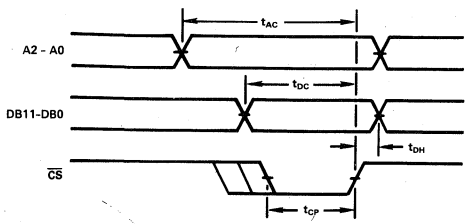
ABSOLUTE MAXIMUM RATINGS

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 11–15, 17–28)
to Power Ground . . . . . −1.0V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out, V_{OUT} (Pins 6, 9) . . Indefinite short to power ground
Momentary Short to V_{CC}
Power Dissipation 1000mW

TIMING DIAGRAMS

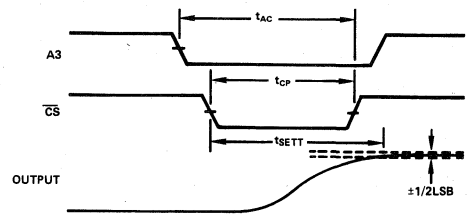
WRITE CYCLE #1

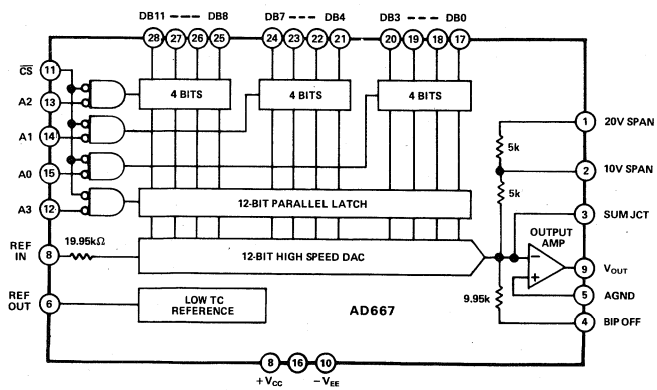
(Load First Rank from Data Bus; A3 = 1)



WRITE CYCLE #2

(Load Second Rank from First Rank; A2, A1, A0 = 1)





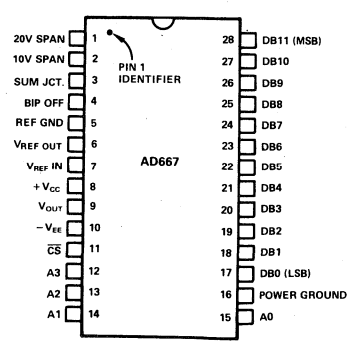
AD667 Block Diagram

AD667 ORDERING GUIDE

Model	Package[1]	Temperature Range – °C	Linearity Error Max @ 25°C	Gain T.C. Max ppm/°C
AD667JN	Plastic (N28A)	0 to +70	±1/2LSB	30
AD667KN	Plastic (N28A)	0 to +70	±1/4LSB	15
AD667AD	Ceramic (D28A)	−25 to +85	±1/2LSB	30
AD667AE	LCC (E28A)	−25 to +85	±1/2LSB	30
AD667BD	Ceramic (D28A)	−25 to +85	±1/4LSB	15
AD667BE	LCC (E28A)	−25 to +85	±1/4LSB	15
AD667SD	Ceramic (D28A)	−55 to +125	±1/2LSB	30
AD667SE	LCC (E28A)	−55 to +125	±1/2LSB	30

[1]See Section 19 for package outline information.

PIN CONNECTIONS
TOP VIEW



*NOTE DIP PACKAGE PIN NUMBERS AND LCC CONTACT NUMBERS SERVE THE SAME FUNCTION.

THE AD667 OFFERS TRUE 12-BIT PERFORMANCE OVER THE FULL TEMPERATURE RANGE

RELATIVE ACCURACY: Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to F.S. – 1LSB) for any bit combination. The AD667 is laser trimmed to 1/4LSB (0.006% of F.S.) maximum error at +25°C for the K and B versions and 1/2LSB for the J, A and S versions.

MONOTONICITY: A DAC is said to be monotonic if the output either increases or remains constant for increasing digital inputs such that the output will always be a nondecreasing function of input. All versions of the AD667 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: Monotonic behavior requires that the differential linearity error be less than 1LSB both at +25°C and over the temperature range of interest. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 10 volt full scale output, a change of 1LSB in digital input code should result in a 2.44mV change in the analog output (1LSB = 10V × 1/4096 = 2.44mV). If in actual use, however, a 1LSB change in the input code results in a change of only 0.61mV (1/4LSB) in analog output, the differential linearity error would be −1.83mV, or −3/4LSB. The AD667K and B grades have a max differential linearity error of 1/2LSB, which specifies that every step will be at least 1/2LSB and at most 1 1/2 LSB.

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD667 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V.

Gain and offset drift are minimized in the AD667 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table I.

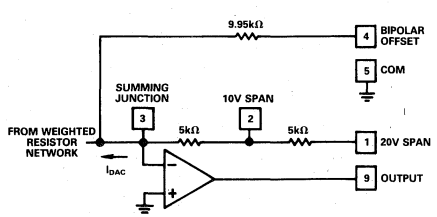


Figure 1. Output Amplifier Voltage Range Scaling Circuit

UNIPOLAR CONFIGURATION (Figure 2)

This configuration will provide a unipolar 0 to +10 volt output range. In this mode, the bipolar offset terminal, pin 4, should be grounded if not used for trimming.

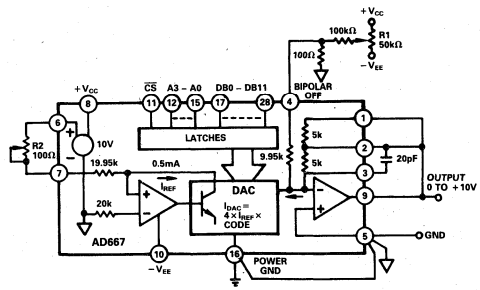


Figure 2. 0 to +10V Unipolar Voltage Output

STEP I . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer R1, until the output reads 0.000 volts (1LSB = 2.44mV). In most cases this trim is not needed, and pin 4 should be connected to pin 5.

STEP II . . . GAIN ADJUST

Turn all bits ON and adjust 100Ω gain trimmer R2, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.2375V full scale is desired (exactly 2.5mV/bit), insert a 120Ω resistor in series with the gain resistor at pin 2 to the op amp output.

BIPOLAR CONFIGURATION (Figure 3)

This configuration will provide a bipolar output voltage from −5.000 to +4.9976 volts, with positive full scale occurring with all bits ON (all 1's).

STEP I . . . OFFSET ADJUST

Turn OFF all bits. Adjust 100Ω trimmer R1 to give −5.000 volts output.

STEP II . . . GAIN ADJUST

Turn ON all bits. Adjust 100Ω gain trimmer R2 to give a reading of +4.9976 volts.

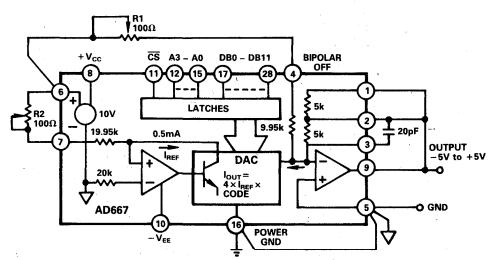


Figure 3. ±5V Bipolar Voltage Output

Output Range	Digital Input Codes	Connect Pin 9 to	Connect Pin 1 to	Connect Pin 2 to	Connect Pin 4 to
±10V	Offset Binary	1	9	NC	6 (through 50Ω fixed or 100Ωtrim resistor)
±5V	Offset Binary	2	2	9	6 (through 50Ω fixed or 100Ωtrim resistor)
±2.5V	Offset Binary	2	3	9	6 (through 50Ω fixed or 100Ωtrim resistor)
0 to +10V	Straight Binary	2	2	9	5 (or optional trim – See Figure 2)
0 to +5V	Straight Binary	2	3	9	5 (or optional trim – See Figure 2)

Table I. Output Voltage Range Connections

DIGITAL CIRCUIT DETAILS

The bus interface logic of the AD667 consists of four independently addressable registers in two ranks. The first rank consists of three four-bit registers which can be loaded directly from a 4-, 8-, 12-, or 16-bit microprocessor bus. Once the complete 12-bit data word has been assembled in the first rank, it can be loaded into the 12-bit register of the second rank. This double-buffered organization avoids the generation of spurious analog output values.

The latches are controlled by the address inputs, A0-A3, and the $\overline{CS}$ input. All control inputs are active low, consistent with general practice in microprocessor systems. The four address lines each enable one of the four latches, as indicated in Table II.

All latches in the AD667 are level-triggered. This means that data present during the time when the control signals are valid will enter the latch. When any one of the control signals returns high, the data is latched.

$\overline{CS}$	A3	A2	A1	A0	Operation
1	X	X	X	X	No Operation
X	1	1	1	1	No Operation
0	1	1	1	0	Enable 4 LSBs of First Rank
0	1	1	0	1	Enable 4 Middle Bits of First Rank
0	1	0	1	1	Enable 4 MSBs of First Rank
0	0	1	1	1	Loads Second Rank from First Rank
0	0	0	0	0	All Latches Transparent

"X" = Don't Care

Table II. AD667 Truth Table

8-BIT MICROPROCESSOR INTERFACE

The AD667 interfaces easily to 8-bit microprocessor systems of all types. The control logic makes possible the use of right- or left-justified data formats.

Whenever a 12-bit DAC is loaded from an 8-bit bus, two bytes are required. If the program considers the data to be a 12-bit binary fraction (between 0 and 4095/4096), the data is left-justified, with the eight most significant bits in one byte and the remaining bits in the upper half of another byte. Right-justified data calls for the eight least significant bits to occupy one byte, with the 4 most significant bits residing in the lower half of another byte, simplifying integer arithmetic.

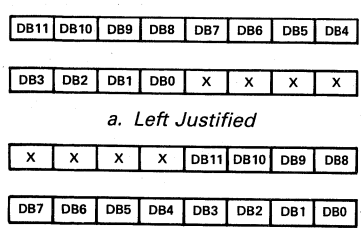


Figure 4. 12-Bit Data Formats for 8-Bit Systems

Figure 5 shows an addressing scheme for use with an AD667 set up for left-justified data in an 8-bit system. The base address is decoded from the high-order address bits and the resultant active-low signal is applied to $\overline{CS}$. The two LSBs of the address bus are connected as shown to the AD667 address inputs. The latches now reside in two consecutive locations, with location X01 loading the four LSBs and location X10 loading the eight MSBs and updating the output.

Right-justified data can be similarly accommodated. The overlapping of data lines is reversed, and the address connections are slightly different. The AD667 still occupies two adjacent locations in the processor's memory map.

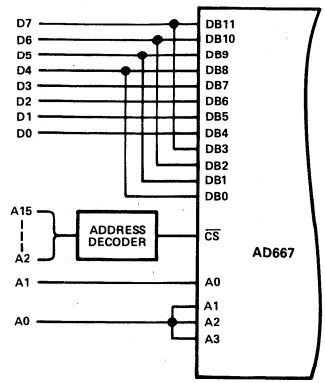


Figure 5. Left-Justified 8-Bit Bus Interface

USING THE AD567 WITH 12- AND 16-BIT BUSES

The AD667 is easily interfaced to 12- and 16-bit data buses. In this operation, all four address lines (A0 through A3) are tied to low, and the latch is enabled by $\overline{CS}$ going low. The AD667 thus occupies a single memory location.

This configuration renders the second rank register transparent, using the first rank of registers as the data latch. The $\overline{CS}$ input can be driven from an active-low decoded address. It should be noted that any data bus activity during the period when $\overline{CS}$ is active will cause activity at the AD667 output. If data is not guaranteed stable during this period, the second rank register can be used to provide double buffering.

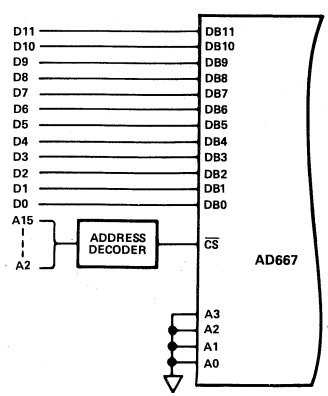


Figure 6. Connections for 12- and 16-Bit Bus Interface

ANALOG DEVICES

8-Bit Monolithic Multipling D/A Converter

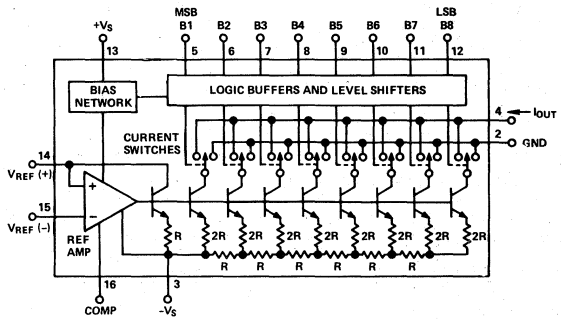
AD1408/AD1508*

PRELIMINARY TECHNICAL DATA

FEATURES

- Improved Replacement for Industry Standard 1408/1508
- Improved Settling Time: 250ns typ
- Improved Linearity: ±0.1% Accuracy Guaranteed Over Temperature Range (-9 Grade)
- High Output Voltage Compliance: +0.5V to -5.0V
- Low Power Consumption: 157mW typ
- High Speed 2-Quadrant Multiplying Input: 4.0mA/μs Slew Rate
- Single Chip Monolithic Construction
- Hermetic 16-Pin Ceramic DIP

AD1408/AD1508 FUNCTIONAL BLOCK DIAGRAM



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9

PRODUCT DESCRIPTION

The AD1408 and AD1508 are low cost monolithic integrated circuit 8-bit multiplying digital-to-analog converters, consisting of matched bipolar switches, a precision resistor network and a control amplifier. The single chip is mounted in a hermetically sealed ceramic 16 lead dual-in-line package.

Advanced circuit design and precision processing techniques result in significant performance advantages over older industry standard 1408/1508 devices. The maximum linearity error over the specified operating temperature range is guaranteed to be less than ±¼LSB (-9 grade) while settling time to ±½LSB is reduced to 250ns typ. The temperature coefficient of gain is typically 20ppm/°C and monotonicity is guaranteed over the entire operating temperature range.

The AD1408/AD1508 is recommended for all low-cost 8-bit DAC requirements; it is also suitable for upgrading overall performance where older, less accurate and slower 1408/1508 devices have been designed in. The AD1408 series is specified for operation over the 0 to +75°C temperature range, the AD1508 series for operation over the extended temperature range of -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monolithic IC construction makes the AD1408/AD1508 an optimum choice for applications where low cost is a major consideration.
2. The AD1408/AD1508 directly replaces other devices of this type.
3. Versatile design configuration allows voltage or current outputs, variable or fixed reference inputs, CMOS or TTL logic compatibility and a wide choice of accuracy and temperature range specifications.
4. Accuracies within ±¼LSB allow performance improvement of older applications without redesign.
5. Faster settling time (250ns typ) permits use in higher speed applications.
6. Low power consumption improves stability and reduces warm-up time.
7. The AD1408/AD1508 multiplies in two quadrants when a varying reference voltage is applied. When multiplication is not required, a fixed reference is used.

*Covered by Patent Numbers 3,961,326; 4,141,004.

SPECIFICATIONS (typical @ +25°C and V_{CC} = +5.0V dc, V_{EE} = -15V dc unless otherwise noted)

MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
POWER SUPPLY VOLTAGE	V_{CC}	+5.5	V dc
	V_{EE}	-16.5	V dc
DIGITAL INPUT VOLTAGE	V_5 thru V_{12}	+5.5, 0	V dc
APPLIED OUTPUT VOLTAGE	V_0	+0.5, -5.2	V dc
REFERENCE CURRENT	I_{14}	5.0	mA
REFERENCE AMPLIFIER INPUTS	V_{14}, V_{15}	V_{CC}, V_{EE}	V dc
POWER DISSIPATION			
(Package Limitation)		1000	mW
Derate above T_A = +25°C	P_D	6.7	mW/°C
OPERATING TEMPERATURE RANGE			
AD1408 Series	T_A	0 to +75	°C
AD1508 Series	T_A	-55 to +125	°C
STORAGE TEMPERATURE RANGE	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V dc, V_{EE} = -15V dc, $\frac{V_{REF}}{R14}$ = 2.0mA, **AD1508 Series:** T_A = -55°C to +125°C
AD1408 Series: T_A = 0 to +75°C unless otherwise noted. All digital inputs at high logic level.)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT
RELATIVE ACCURACY					
(Error Relative to Full Scale I_O)					
AD1508-9, AD1408-9	E_r	–	–	±0.10	%
AD1508-8, AD1408-8	E_r	–	–	±0.19	%
AD1408-7	E_r	–	–	±0.39	%
SETTLING TIME					
to Within 1/2LSB [Includes t_{PLH}]					
(T_A = +25°C)	t_S	–	250	–	ns
PROPAGATION DELAY TIME					
T_A = +25°C	t_{PLH}, t_{PHL}	–	30	100	ns
OUTPUT FULL SCALE CURRENT DRIFT	TCI_O	–	-20	–	ppm/°C
DIGITAL INPUT LOGIC LEVELS (MSB)					
High Level, Logic "1"	V_{IH}	2.0	–	–	V dc
Low Level, Logic "0"	V_{IL}	–	–	0.8	V dc
DIGITAL INPUT CURRENT (MSB)					
High Level, V_{IN} = 5.0V	I_{IH}	–	0	0.04	mA
Low Level, V_{IL} = 0.8V	I_{IL}	–	-0.4	-0.8	mA
REFERENCE INPUT BIAS CURRENT					
(Pin 15)	I_{15}	–	-1.0	-3.0	μA
OUTPUT CURRENT RANGE					
V_{EE} = -5.0V	I_{OR}	0	2.0	2.1	mA
V_{EE} = -6.0V to -15V	I_{OR}	0	2.0	4.2	mA
OUTPUT CURRENT					
V_{REF} = 2.000V, R14 = 1000Ω	I_O	1.9	1.99	2.1	mA
OUTPUT CURRENT					
(All Bits Low)	I_O (min)	–	0	4.0	μA
OUTPUT VOLTAGE COMPLIANCE					
($E_I \leq$ 0.19% at T_A = +25°C)					
V_{EE} = -5V	V_O	–	–	-0.6, +0.5	V dc
V_{EE} below -10V	V_O	–	–	-5.0, +0.5	V dc
REFERENCE CURRENT SLEW RATE	SRI_{REF}	–	4.0	–	mA/μs
OUTPUT CURRENT POWER SUPPLY					
SENSITIVITY	$PSSI_O$	–	0.5	2.7	μA/V
POWER SUPPLY CURRENT					
(All Bits Low)	I_{CC}	–	+9	+14	mA
	I_{EE}	–	-7.5	-13	mA
POWER SUPPLY VOLTAGE RANGE					
(T_A = +25°C)	V_{CCR}	+4.5	+5.0	+5.5	V dc
	V_{EER}	-4.5	-15	-16.5	V dc
POWER DISSIPATION					
All Bits Low					
V_{EE} = -5.0V dc	P_D	–	82	135	mW
V_{EE} = -15V dc	P_D	–	157	265	mW
All Bits High					
V_{EE} = -5.0V dc	P_D	–	70	–	mW
V_{EE} = -15V dc	P_D	–	132	–	mW

Specifications subject to change without notice.

APPLYING THE AD1408/1508

Reference Amplifier Drive and Compensation

Figures 2a and 2b are the connection diagrams for using the AD1408/AD1508 in basic voltage output modes. In Figure 2a, a positive reference voltage, V_{REF}, is converted to a current by resistor R14. This reference current determines the scale factor for the output current such that the full scale output is 1LSB (1/256) less than the reference current. R15 provides bias current compensation to the reference control amplifier to minimize temperature drift; it is nominally equal to R14 although it needn't be a stable precision resistor. This configuration develops a negative output voltage across R_L and requires a positive V_{REF}.

If a negative V_{REF} is to be used, connections to the reference control amplifier must be reversed as shown in Figure 2b. This circuit also delivers a negative output voltage, but presents a high impedance to the reference source. The negative V_{REF} must be at least 4 volts above the V_{EE} supply.

Two quadrant multiplication may be performed by applying a bipolar ac signal as the reference as long as pin 14 is positive relative to pin 15 (reference current must flow into pin 14). If the ac reference is applied to pin 14 through R14, a negative voltage equal to the negative peak of the ac reference must be applied through R15 to pin 15; if the ac reference is applied to pin 15 through R15, a positive voltage equal to the positive peak of the ac reference must be applied through R14 to pin 14.

When a dc reference is used, capacitive bypass from reference to ground will improve noise rejection.

The compensation capacitor, C, provides proper phase margin for the reference control amplifier. As R14 is increased, the closed-loop gain of the amplifier is decreased, therefore C must be increased. For R14 = 1.0kΩ, 2.5kΩ and 5.0kΩ, minimum values of capacitance are 15pF, 37pF and 75pF respectively. C may be tied to either V_{EE} or ground, but tying it to V_{EE} increases negative supply noise rejection. If the reference is driven by a high-impedance current source, heavy compensation of the amplifier is required; this causes a reduction in overall bandwidth.

Output Current Range

The nominal value for output current range is 0 to 1.992mA as determined by a 2mA reference current. If V_{EE} is more negative than -7.0 volts, this range may be increased to a maximum of 0 to 4.2mA. An increase in speed may be realized at increased output current levels, but power consumption will increase, possibly causing small shifts in linearity.

Pin 1, range control, may be grounded or unconnected. Although other older devices of this type require different terminations for various applications, the AD1408/AD1508 compensates automatically. This pin is not connected internally, therefore any previously installed connections will be tolerated.

Output Voltage Range

The voltage on pin 4 is restricted to a +0.5 to -0.6 volt range when V_{EE} = -5V. When V_{EE} is more negative than -10 volts, this range is extended to +0.5 to -5.0 volts. If the current into pin 14 is 2mA (full-scale output current = 1.992mA), a 2.5kΩ resistor between the output, pin 4, and ground will provide a 0 to -4.980 volt full-scale. If R_L exceeds 500Ω however, the settling time of the device is increased.

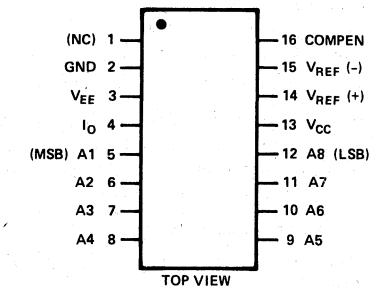
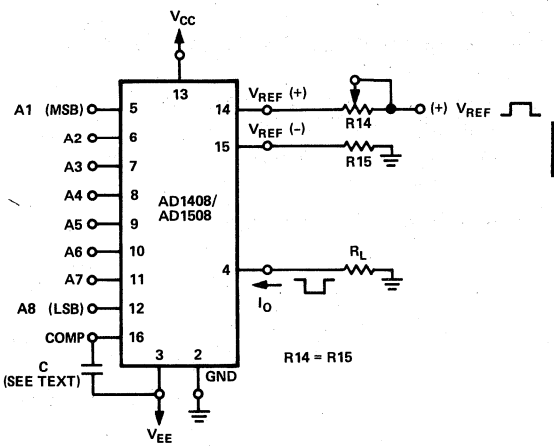
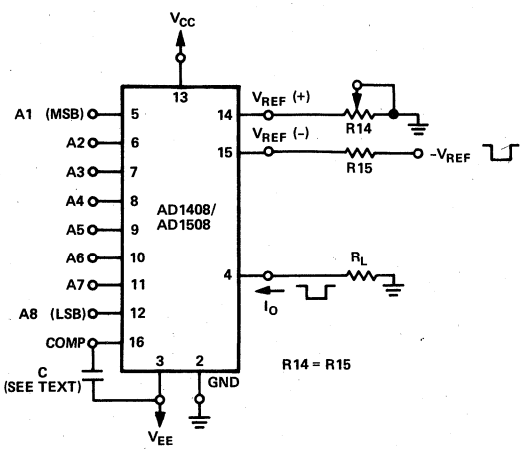


Figure 1. Pin Connections



a. Connections for Use with Positive Reference



b. Connections for Use with Negative Reference

Figure 2. Basic Connections

Voltage Output

A low impedance voltage output may be derived from the output current of the AD1408/AD1508 by using an output amplifier as shown in Figure 3. The output current I_O flows in R_O to create a positive-going voltage range at the output of amplifier A1. R_O may be chosen for the desired range of output voltage; the complete circuit transfer function is given in Figure 3.

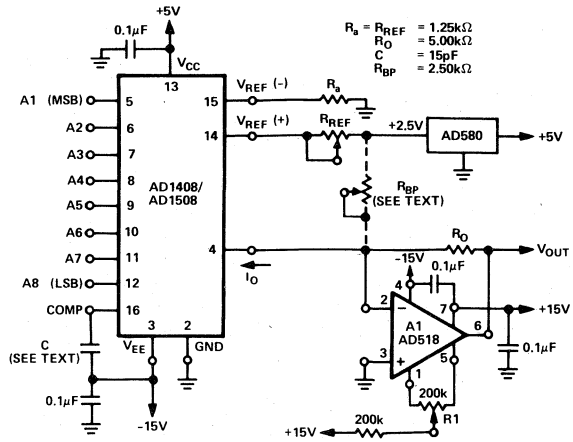
If a bipolar output voltage range is desired, R_{BP}, shown dotted, must be installed. Its purpose is to provide an offset equal to one-half of full-scale at the output of A1. The procedure for calibrating the circuit of Figure 3 is as follows:

Calibration for Unipolar Outputs (No R_{BP})

1. With all bits "OFF", adjust the A1 null-pot, R1, for V_{OUT} = 0.00V.
2. With all bits "ON", adjust R_{REF} for V_{OUT} = (Nominal Full Scale) − 1LSB = +9.961 volts

Calibration for Bipolar Outputs (R_{BP} installed, R1 not required)

1. With all bits "OFF", adjust R_{BP} for V_{OUT} = -F.S. = -5.000 volts
2. With Bit 1 (MSB) "ON", and all other Bits "OFF", adjust R_{REF} for V_{OUT} = 0.000V.
3. With all bits "ON", verify that E_{OUT} = +5.000V− 1LSB = 4.961V.



$$V_{OUT} = \frac{V_{REF}}{R_{REF}}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

ADJUST V_{REF}, R_{REF} OR R_O SO THAT WITH ALL DIGITAL INPUTS AT LOGIC "1", V_{OUT} = 9.961 VOLTS:

$$V_{OUT} = \frac{2.5}{1.25k\Omega}(5k\Omega)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right] = 9.961 \text{ VOLTS}$$

Figure 3. Typical Connection Diagram, AD1408/AD1508, Voltage Output, Fixed Reference

AD1408/AD1508 ORDERING GUIDE

Model	Accuracy (±% F.S.)	Temperature Range (°C)	Package Style[1]
AD1408-7D	0.39	0 to +75	Q16A
AD1408-8D	0.19	0 to +75	Q16A
AD1408-9D	0.10	0 to +75	Q16A
AD1508-8D	0.19	-55 to +125	Q16A
AD1508-9D	0.10	-55 to +125	Q16A

[1] See Section 19 for package outline information.

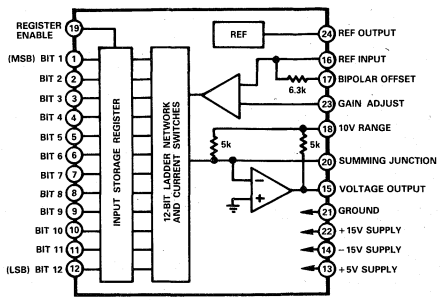
ANALOG DEVICES

Complete, Voltage Output 12-Bit Buffered DAC

AD3860

FEATURES
Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
12-Bit Input Register
Small Size: 24 pin DIP
Fast Settling: 5μs to ±0.01%
Internal Reference
Internal Output Amplifier

AD3860 FUNCTIONAL BLOCK DIAGRAM



9

PRODUCT DESCRIPTION

The AD3860 is a precision 12-bit D/A converter designed for direct interface to microprocessors.

The functional diagram shows that the AD3860 consists of a 12-bit input storage register, a 12-bit DAC, internal reference, and a fast output amplifier. It is TTL compatible and the register enable facilitates deglitching and microprocessor interfacing. The low noise, high stability subsurface zener diode is used to produce a reference voltage with excellent long term stability, external current capability and temperature drift characteristics. The output amplifier gives the user a voltage output and combines with the other features of this circuit to produce a functionally complete digital to analog converter.

The AD3860 is laser trimmed to achieve ± 1/4LSB linearity typical and ± 1/2LSB maximum over the full operating temperature range. The low T.C. Binary ladder guarantees that the AD3860 will be monotonic over the specified temperature range.

The AD3860 is available in two versions. The AD3860K is specified for use over 0 to +70°C temperature range. The AD3860S is specified for the −55°C to +125°C temperature range and is especially recommended for high reliability needs in harsh environments. All units are in supplied in 24-pin, hermetically-sealed ceramic DIPs.

PRODUCT HIGHLIGHTS

1. The AD3860 is a functionally complete voltage output DAC with voltage reference, digital latches, and output amplifier in a single hybrid package.
2. The input buffer latches permit interface to microprocessor data buses. All logic inputs are TTL or 5 volt CMOS compatible.
3. Laser trimming the thin-film resistors assures superior linearity and accuracy stability over temperature. Both commercial and military temperature range models have ± 1/2LSB linearity maximum guaranteed over the full operating temperature range.
4. Monotonicity is also guaranteed over the full operating temperature range. The typical full scale temperature coefficient is 10ppm/°C.
5. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
6. The fast output amplifier provides a voltage output with a 5μs settling time to 0.01% for a 20 volt step. The AD3860 is designed for military and industrial applications where high speed D/A conversion is required.

SPECIFICATIONS (typical @ +25°C, rated power supplies unless otherwise noted)

Model	AD3860K	AD3860S
DIGITAL INPUTS		
Resolution	12 Bits	*
Logic Coding: Unipolar Ranges	Complementary Straight Binary	*
Bipolar Ranges	Complementary Offset Binary	*
Logic Levels (TTL Compatible): Logic "1"	+2.0V dc min, +5.5V dc max	*
Logic "0"	0V dc min, 0.8V dc max	*
Input Currents		
Data Inputs: Logic "1"	30μA max	*
Logic "0"	−0.6mA max	*
Register Enable: Logic "1"	60μA max	*
Logic "0"	−1.2mA max	*
ANALOG OUTPUT		
Output Impedance	0.5Ω	*
Output Current @ Z_L = 2kΩ‖250pF	±10mA, ±5mA min	*
ACCURACY		
Linearity Error (T_{min} to T_{max})	±1/4LSB[1], ±1/2LSB max	±1/2LSB max
Differential Linearity Error	±1/2LSB, ±1LSB max	±1LSB
Monotonicity	Guaranteed Over Temperature	*
Full Scale Absolute Accuracy Error[2]	±0.05% FSR[3], ±0.1% FSR max	*
T_{min} to T_{max}	±0.15% FSR, ±0.3% FSR max	*
Zero Error	±0.025% FSR, ±0.05% FSR max	*
T_{min} to T_{max}	±0.05% FSR, ±0.1% FSR max	*
Gain Error	±0.1%	*
DRIFT		
Gain	±10ppm/°C	*
Offset	±5ppm/°C	*
DYNAMIC CHARACTERISTICS		
Settling Time to ±0.01% for: 20V Step	5μs, 7μs max	*
10V Step	3μs, 5μs max	*
Output Slew Rate	20V/μs	*
Register Enable[4]		
Pulse Width	60ns min	*
Setup Time Digital Data to Enable	40ns min	*
INTERNAL REFERENCE VOLTAGE		
Voltage	+6.3V	*
Accuracy	±2%	*
External Current	2.5mA max	*
POWER SUPPLIES		
Power Supply Range: +15V Supply	+14.55V min, +15.45V max	*
−15V Supply	−14.55V min, −15.45V max	*
+5V Supply	+4.75V min, +5.25V max	*
Power Supply Rejection: +15V Supply	±0.002% FSR/% V_S ±0.01% FSR/% V_S max	*
−15V Supply	±0.002% FSR/% V_S ±0.004% FSR/% V_S max	*
Current Drain: +15V Supply	10mA, 20mA max	*
−15V Supply	−12mA, −30mA max	*
+5V Supply	30mA, 50mA max	*
Power Consumption	675mW, 1W max	*
TEMPERATURE RANGE		
Operating	0 to +70°C	−55°C to +125°C
Storage	−65°C to +150°C	*
PACKAGE OPTION[5]		
24-Pin DIP	HY24C	*

NOTES
[1]Least Significant Bit (LSB).
[2]Absolute Accuracy Error includes gain, offset, linearity, noise and all other errors and is specified without adjustment.
[3]FSR is Full Scale Range and is 20 V for ±10 range.
[4]The AD3860's analog output will follow its digital input when register enable is a logic "0". Digital Input date will be latched and analog output voltage constant when register enable is a logic "1".
[5]See Section 19 for package outline information.
*Same as AD3860K.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

+15 Volt Supply (pin 22) . . . . . +18V
−15 Volt Supply (pin 14) . . . . . −18V
+5 Volt Supply (pin 13) . . −0.5V to +7V
Register Enable (pin 19) . −0.5V to +5.5V
Digital Inputs (pins 1–12) . −0.5V to +5.5V

PIN CONFIGURATION

24 LEAD DUAL IN-LINE-PACKAGE

PIN NO.	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12 (LSB)
13	LOGIC SUPPLY
14	$-V_S$
15	V_{OUT}
16	REF INPUT
17	BIPOLAR OFFSET
18	10V RANGE
19	REGISTER ENABLE
20	SUMMING JUNCTION
21	COMMON
22	$+V_S$
23	GAIN ADJUST
24	$6.3V_{REF}$ OUT

APPLICATIONS INFORMATION

OUTPUT VOLTAGE RANGE SELECTION

Output Range	0 to +10V	±5V	±10V
Pin Connection			
Connect Pin 24 to	16	16	16
Connect Pin 17 to	21	20	20
Connect Pin 15 to	18	18	NC
Connect Pin 20 to	NC	17	17

INPUT LOGIC CODING

Digital Input MSB LSB	Analog Output 0 to +10V	±5V	±10V
0000 0000 0000	+9.9976V	+4.9976V	+9.9951V
0000 0000 0001	+9.9951V	+4.9951V	+9.9902V
0111 1111 1111	+5.0000V	0.0000V	0.0000V
1000 0000 0000	+4.9976V	−0.0024V	−0.0049V
1111 1111 1110	+0.0024V	−4.9976V	−9.9951V
1111 1111 1111	0.0000V	−5.0000V	−10.0000V

CODING NOTES:
1. For unipolar operation, the coding complementary straight binary (CSB).
2. For bipolar operation, the coding complementary offset binary (COB).
3. For FSR = 20V, 1LSB = 4.88mV.
4. For FSR = 10V, 1LSB = 2.44mV.

Layout Considerations

Proper layout and decoupling is necessary to obtain the AD3860's specified accuracy. Ground (pin 21) must be tied to circuit analog ground as close to the package as possible. Grounding through a large ground plane beneath the package is preferred.

Power supplies should be decoupled with electrolytic or tantalum capacitors near the unit. A 1μF capacitor is parallel with a 0.01μF ceramic capacitor on all supplies is recommended, see Figure 1.

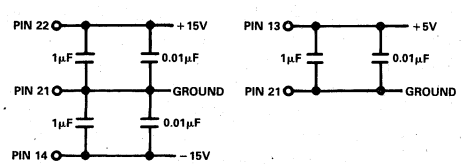


Figure 1. Power Supply Decoupling

Coupling between analog and digital signals should be minimized to avoid noise pick up. Use short jumpers to tie the reference output (pin 24) to the reference input (pin 16) and to tie the bipolar offset (pin 17) to the summing junction (pin 20).

If the external full scale and zero adjustments are used, the series 6.8MΩ resistors should be placed as close to the unit as possible.

Reference Output

The AD3860 is laser trimmed to operate from the internal 6.3 volt voltage reference. The user has the option of supplying an external reference but for specified operation the reference output (pin 24) must be connected to the reference input (pin 16). The internal reference can be used to drive an external load, but it should be buffered if load current will exceed 2.5mA.

Optional Full Scale and Zero (−Full Scale) Adjustments

The AD3860 will operate as specified without adjustment, however, absolute accuracy error can be reduced to ±1LSB by trimming as described below. Adjustments should be made after warmup. As shown in Figures 2 and 3 the zero

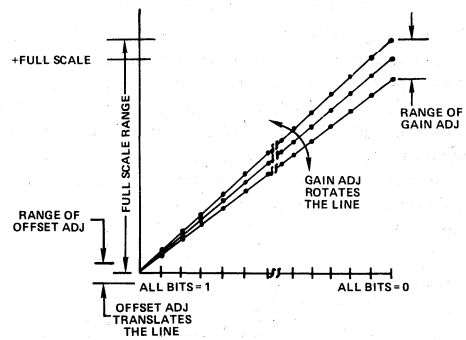


Figure 2. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

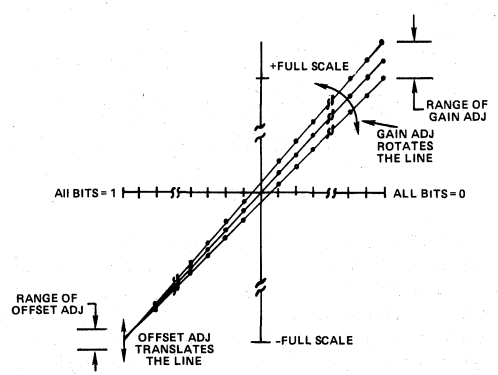
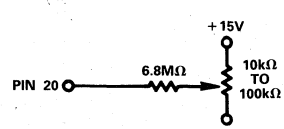


Figure 3. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

(−full scale) adjustment should be made before the full scale adjustment. We recommend multiturn potentiometers with maximum temperature coefficients of 100ppm/°C. Series resistors can be ±20% carbon composition or better. If these adjustments are not used pins 20 and 23 should not be grounded.

Zero (−Full Scale) Adjustment

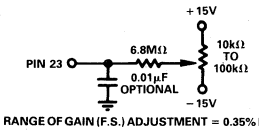
Connect the potentiometer as shown and apply all "1s" to the digital inputs. Adjust the potentiometer until the analog output is equal to zero volts for unipolar output ranges and minus full scale for bipolar output ranges.



RANGE OF ZERO (−F.S.) ADJUSTMENT = ±0.2% FSR

Full Scale Adjustment

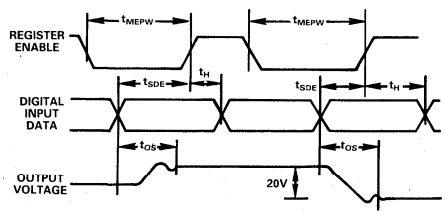
Connect the potentiometer as shown and apply all "0s" to the digital inputs. Adjust the potentiometer for maximum chosen analog output.



RANGE OF GAIN (F.S.) ADJUSTMENT = 0.35% FSR

REGISTER ENABLE

When the register enable (pin 19) is high (hold mode) the digital data in the input register will be latched. When the register enable is low (track mode) the converter's output will follow its input. To latch new digital data into the register, the register enable must go low for a minimum of 60ns and the digital input data must be valid for a minimum of 40ns before the register enable goes high again. See the timing diagram below.



TIMING NOTES:

t_{MEPW} MIMINUM ENABLE PULSE WIDTH IS 60ns.

t_{SDE} MINIMUM SETUP TIME DIGITAL INPUT DATA TO ENABLE IS 40ns.

t_H HOLD TIME IS DEFINED AS THE REQUIRED DELAY BETWEEN THE LEADING EDGE OF REGISTER ENABLE AND THE END OF VALID INPUT DATA. THE HOLD TIME IS ZERO FOR THE AD3860.

t_{OS} OUTPUT SETTLING TIME FOR A 20 VOLT CHANGE TO ± 1/2LSB IS 7μs MAX.

Figure 4. Input Register Timing Diagram

8-BIT MICROPROCESSOR INTERFACE

Whenever a 12-bit DAC is loaded from an 8-bit bus, two write cycles are required. The organization most often used is "right justified." Right-justified data calls for the eight least significant bits to occupy one byte, with the four most significant bits residing in the lower half of another byte. This organization simplifies integer arithmetic. Figure 5 shows an addressing

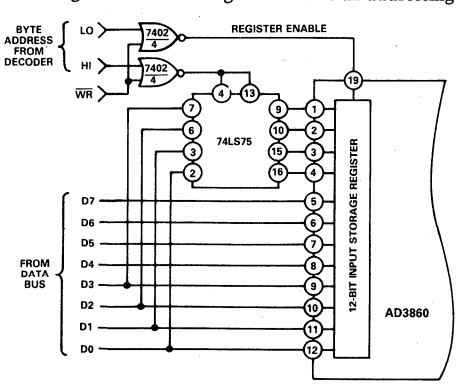


Figure 5. Right-Justified 8-Bit Bus Interface

scheme for the AD3860 set up for right justified data in an 8-bit system. The four MSBs are latched into the 74LS75 latch in the first write cycle. The entire 12-bit word is then loaded into the AD3860's internal input storage register on the next write cycle. An alternate scheme is to use an eight-bit intermediate register, such as the 74LS373, to allow the user to load the lower order bits in the first write cycle.

Left-justified data can be similarly accommodated. The overlapping of data lines is reversed as shown in Figure 6. The AD3860

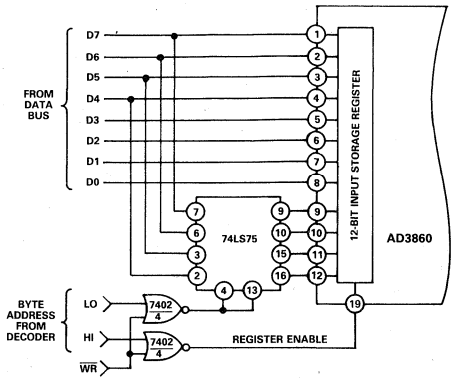


Figure 6. Left-Justified 8-Bit Bus Interface

still occupies two adjacent locations in the processor's memory map. A left-justified format is convenient in applications when the data represents a 12-bit binary fraction (between 0 and $\frac{4095}{4096}$).

Left-justified data has the four least significant bits in the upper half of the first byte and the eight most significant bits in the second byte. The four LSBs on the intermediate latch and the eight MSBs on the data bus are all latched into the AD3860s latch simultaneously. This double buffering technique avoids the analog output slewing to an undesirable state determined by the MSBs of the new digital data and the LSBs of the previous digital data.

Many of the popular microprocessor families include components specifically designed to ease the interface between the microprocessor and a peripheral device such as a converter. These components are called Programmable Peripheral Interface (PPI), Peripheral Interface Adaptor (PIA), Parallel I/O Controller (PIO), or similar names. They typically feature two or more 8-bit wide parallel data ports which can, under program control, be configured as either inputs or outputs. Their control signals are made compatible with the particular processor they serve, and in many systems can provide an attractive alternative to a collection of random logic. For example, the 8255 PPI has two 8-bit and two 4-bit ports which can be used as input, as output, or as a combination of input, output, and control. Each of the 4-bit words can be grouped with one of the 8-bit words so that the interface is split into two 12-bit ports. The ports can be set up as outputs, under program control, for controlling two AD3860s with a single PPI. The 8255 contains two bits of address input. That is, A0 and A1 of the 8255 are driven directly by the address bus, and these bits need not be used by the address decoder. Though the 8255 is an 8080 system component, it is adaptable to other μP systems.

USING THE AD3860 WITH 12- AND 16-BIT BUSES

The AD3860 is easily interfaced to 12- and 16-bit data buses. The AD3860's Register Enable signal can usually be derived by NANDing the desired address lines with the processor's MEMORY WRITE or I/O WRITE line. For most processors, valid data remains on the data bus for some time after either the valid address or control signals are removed. Therefore, the data is latched into the AD3860 immediately after one of the address or control signals changes but before valid data goes away. The AD3860 thus occupies a single memory location.

ANALOG DEVICES

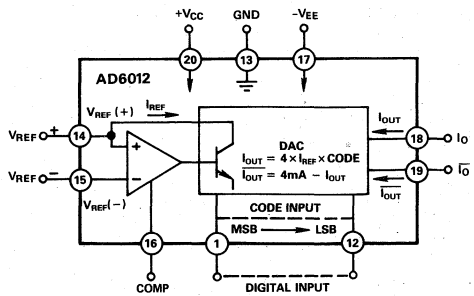
Low Cost Monolithic 12-Bit D/A Converter

AD6012

FEATURES

- **1/2LSB max Differential Linearity Error Over Temperature**
- **250ns Typical Settling Time**
- **Full Scale Current 4mA**
- **High Speed Multiplying Capability**
- **TTL/CMOS/ECL/HTL Compatible**
- **High Output Compliance: −5V to +10V**
- **Complementary Current Outputs**
- **Low Power Consumption: 230mW**

AD6012 FUNCTIONAL BLOCK DIAGRAM



20-PIN DUAL-IN-LINE PACKAGE

9

PRODUCT DESCRIPTION

The AD6012 is an industry standard monolithic 12-bit digital-to-analog converter. Complementary current output and high speed multiplying capability make the AD6012 useful in a wide range of applications such as video displays, process control circuitry and fast A/D converters. The 6012 is the first D/A to achieve 12-bit differential linearity without the use of thin film resistors or active trimming. The 6012's unique circuit design insures monotonicity without the precision trimming associated with most other 12-bit DAC architectures.

The AD6012 is packaged in a 20-pin plastic DIP. The maximum differential linearity error of the AD6012N is guaranteed to be less than ±1LSB (±0.025%). Although tested and specified at ±15V, the AD6012 works well over a wide range of power supply voltages. Performance is essentially independent of supply voltage over the range of +5 volts, −12 volts to ±18 volts.

Guaranteed monotonicity and low cost make the AD6012 an ideal choice for high volume applications requiring fine local resolution. Typical applications include printer graphics and video displays. These applications need a minimum of 12 bits of resolution, although conformance to an ideal straight line from zero to full scale is less important.

ORDERING INFORMATION

Model	Package	Temperature Range	Differential Nonlinearity
AD6012N	20-Pin Plastic DIP	0 to +70°C	±0.025%

PRODUCT HIGHLIGHTS

1. A segmented design technique guarantees monotonicity without the requirement of ultra precise internal components. Resistor tolerances can be as much as 8 times lower than that of conventional R-2R DAC designs while maintaining monotonicity over temperature. This advantage has been used in the AD6012 to provide 12-bit differential linearity over temperature without the use of laser trimmed thin film resistors.
2. The high output current of 4mA full scale accommodates the use of lower load impedances required in higher speed applications. Relatively high output voltages are obtained when small load impedances are used to minimize the output RC time constant.
3. Fully complementary current outputs effectively double the peak-to-peak output swing.
4. Less board space is used by the single width 20-pin dual-in-line package. Most other 12-bit DACs are packaged in larger 24-pin DIPs requiring more than twice the board area of the AD6012.
5. Reference circuit slew rate of 8mA/μs typical accommodates high speed multiplication applications.
6. The AD6012 is compatible with the industry standard 6012 in both pinout and specifications.

SPECIFICATIONS (typical @ $+V_{CC} = +15V$, $-V_{EE} = -15V$, $I_{REF} = 1mA$ over specified temperature range unless otherwise specified)

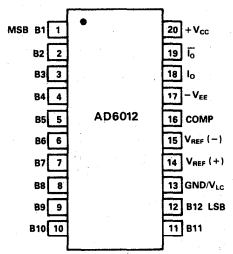
MODEL	AD6012N MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1 to 12)				
TTL or 5 Volt CMOS				
Input Voltage				
Bit ON Logic "1"	+2.0			V
Bit OFF Logic "0"			+0.8	V
Logic Current (each bit)				
$V_{IN} = -5V$ to $+18V$			40	μA
RESOLUTION	12		12	Bits
OUTPUT				
Full Scale Current	3.935	3.999	4.063	mA
$V_{REF} = 10.000V$, $T_A = 25°C$				
$R_1 = R_2 = 10.000k\Omega$				
Full Scale Symmetry Error			±2.0	μA
Zero Scale Current			0.1	μA
Capacitance		20		pF
Compliance Voltage[1]				
$R_{OUT} > 10M\Omega$ typ	−5		+10	V
RELATIVE ACCURACY (error relative to full scale) T_{min} to T_{max}			±0.05	% FS
DIFFERENTIAL NONLINEARITY		±1/2	±1 (±0.025% FS)	LSB
	MONOTONICITY GUARANTEED			
FULL SCALE TEMPCO		10	40	ppm/°C
SETTLING TIME TO 1/2LSB				
All Bits ON-to-OFF or OFF-to-ON				
$T_A = 25°C$		250	500	ns
PROPAGATION DELAY				
50% to 50%		25	50	ns
TEMPERATURE RANGE				
Specified	0		70	°C
Operating	−25		+85	°C
POWER REQUIREMENTS				
Current				
$V_{CC} = +5V$ dc to $+15V$ dc		5.7	8.5	mA
$V_{EE} = -15V$		−13.7	−18	mA
Voltage				
V_{CC}	+4.5		+18	V
V_{EE}	−18		−10.8	V
POWER SUPPLY SENSITIVITY				
$V_{CC} = +13.5V$ to $+16.5V$,				
$V_{EE} = -15V$		±0.0005	±0.001	%FS/%
$V_{EE} = -13.5V$ to $-16.5V$,				
$V_{CC} = +15V$		±0.00025	±0.001	%FS/%
REFERENCE CURRENT RANGE	0.2	1.0	1.1	mA
REFERENCE BIAS CURRENT	0	−0.5	−2.0	μA
REFERENCE INPUT SLEW RATE				
$R_{IN} = 800\Omega$	4.0	8.0		mA/μs
POWER DISSIPATION				
$V_{CC} = +5V$, $V_{EE} = -15V$		234	312	mW
$V_{CC} = +15V$, $V_{EE} = -15V$		291	397	mW
PACKAGE OPTION[2]		N20A		

NOTES
[1]D.N.L. specifications guaranteed over compliance range.
[2]See Section 19 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0 to +70°C
Storage Temperature	−65°C to +125°C
Power Supply Voltage	±18V
Logic Inputs	−5V to +18V
Voltage at Current Output Pins	−8V to +12V
Reference Inputs	$+V_{CC}$ to $-V_{EE}$, ±18V max Differential
Reference Input Current	1.25mA

PIN CONFIGURATION



FUNCTIONAL DESCRIPTION

The segmented design of the AD6012, shown in the functional block diagram, insures that there are no significant differential nonlinearities in the transfer characteristic. The eight major carries of the most significant bits are not subject to the gross differential nonlinearities that can occasionally occur in an R-2R type DAC. This advantage is due to the fundamentally different way that the current is handled in an AD6012.

In a conventional R-2R type DAC, when the input code is incremented past a major carry, a current representing the new code is substituted for the sum of all the less significant bit currents that were previously on. To avoid any nonlinearities, the two total currents must be extremely well matched. In the case of the MSB major carry in a 12-bit DAC, the match must be better than one part in 2048 to maintain monotonicity. However, in the AD6012, a new current is never substituted for the sum of several smaller ones, but redirected through alternate channels and incremented one step at a time.

For example, consider the MSB carry in an AD6012. In the initial state of 011111111111 as shown in the functional block diagram, the switches in the segment generator are set in such a way that currents I_O, I_1 and I_2 are steered directly into the noninverting output I_{OUT}. In addition, a portion of I_3 is directed through the 9-bit DAC that is controlled by the 9 least significant bits into I_{OUT}. With the 9LSBs set to "1", all of the I_3 current is directed to I_{OUT} except for the 1/512 that goes to ground through the right-most transistor in the 9-bit DAC. After the input word is changed to 100000000000, the segment decoder switch for I_3 will be all the way to the right, the switch for I_4 will be in the middle, and all the switches in the 9-bit DAC will be to the left. I_{OUT} will be composed of I_0, I_1, I_2 and I_3. None of I_4 will be directed into I_{OUT} until a higher code is reached. In other words, I_3 is now steered directly to I_{OUT} instead of being divided by a factor of 511/512 in the 9-bit DAC. Since no major current substitution occurs, there is less chance of a large nonlincarity at this transition than in a comparable R-2R DAC.

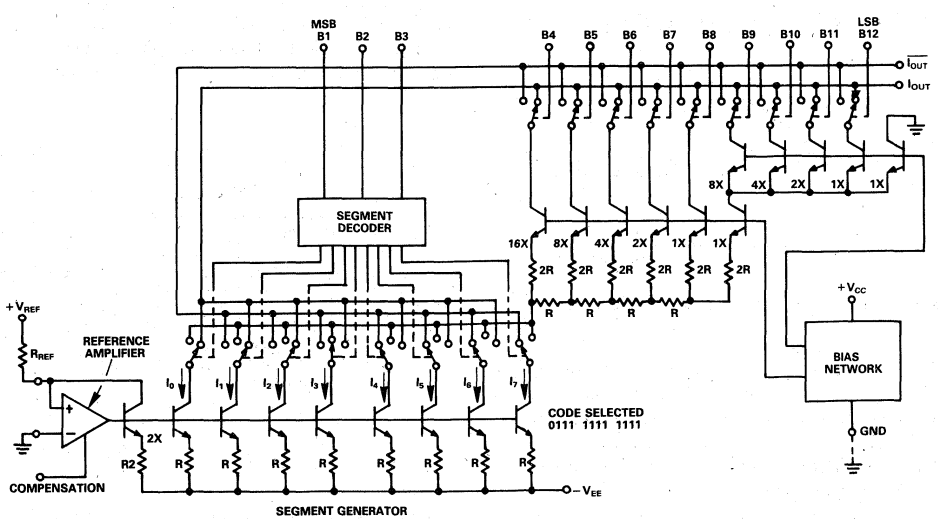


Figure 1. AD6012 Functional Block Diagram

RELATIVE ACCURACY VS. DIFFERENTIAL NON-LINEARITY

Analog Devices defines relative accuracy as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn between the lowest code output voltage and the highest code output voltage) for any bit combination. Relative accuracy is often referred to as nonlinearity. The DAC transfer function shown in Figure 2a has a bow that results in a maximum relative accuracy error of 3LSB. This must be distinguished from a differential linearity error. Differential nonlinearity is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in digital input code. For example, for a 4mA full scale output, a change of 1LSB in digital input code should result in a 0.98μA change in the analog output current (1LSB = 4mA × 1/4096 = 0.98μA). If in actual use, however, a 1LSB change in the input code results in a change of only 0.24μA (1/4LSB) in output current, the differential linearity error would be 0.74μA or 3/4LSB.

The DAC of Figure 1 has very good differential linearity in spite of the poor relative accuracy. Conversely, the DAC of Figure 2 has very good relative accuracy but poor differential linearity. The anomaly in the middle of the transfer function is the result of a positive differential linearity error followed by a negative differential linearity error greater than 1LSB. A negative output step for an increase in digital input code is referred to as nonmonotonic behavior. In general, if a DAC has a differential linearity error specification greater than 1LSB, it may be non-monotonic at one or more of the major carries. In most cases the worst differential linearity error will occur at the MSB transition point.

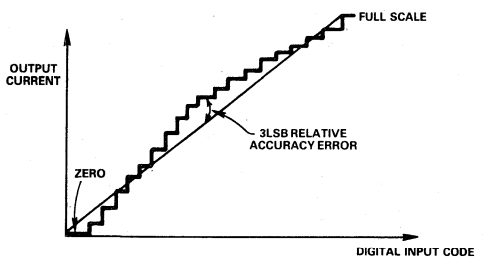


Figure 2a. Relative Accuracy Error

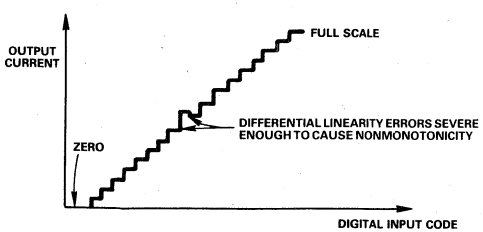


Figure 2b. Example of Nonmonotonic Behavior

As noted in the functional description, the 6012's unique design minimizes differential linearity errors at the transition points of the 3MSBs. This results in a tight specification on maximum differential nonlinearity over temperature. The AD6012N is specified at ±1LSB. Differential linearity is verified on all AD6012s with 100% final testing.

In many converter applications, uniform step size (or minimum differential linearity error) is more important than conformance to an ideal straight line. Twelve-bit converters are usually needed for high resolution rather than high linearity as evidenced by the fact that few transducers are more linear than 0.1%. This is also true in video graphics, where the human eye has difficulty discerning nonlinearity of less than 5%. The AD6012 is especially well suited for these applications since it has inherently low differential linearity error.

For applications requiring 12 bits of resolution and more accuracy than 0.05%, the AD565A and AD566A are recommended. These units feature 0.012% (1/2LSB) max accuracy error over temperature.

ANALOG CIRCUIT CONNECTIONS

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD510L, AD517L, AD741L, AD301AL, AD OP-07) is used, excellent performance can be obtained in many situations without trimming (an op amp with less than 0.5mV max offset voltage should be used to keep offset errors below 1/2LSB). Unipolar zero will typically be within ±0.1LSB (plus op amp offset), and full scale accuracy will be within 0.5% (1.5% max).

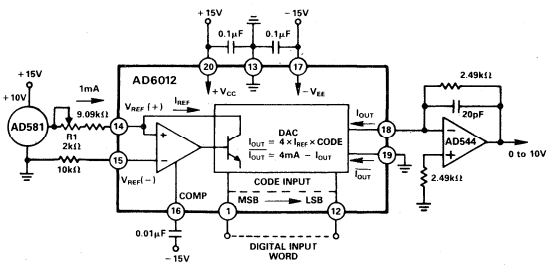


Figure 3. Unipolar 0 to 10V

FIGURE 3 UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range. The following trim adjustment may not be necessary if the application can tolerate up to ±1 1/2% gain error.

Gain Adjust

Turn all bits ON and adjust 2kΩ gain trimmer R1, until the output is 9.9976 volts. (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.) If a 10.24V full scale is desired (exactly 2.5mV/bit), adjust R1 until the output is 10.2375 volts.

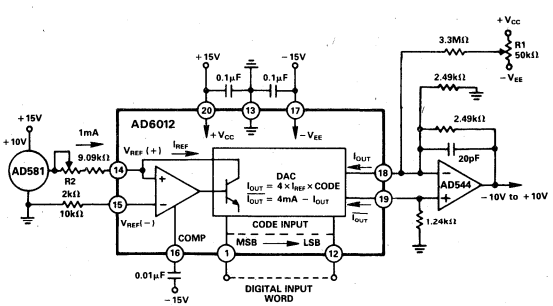


Figure 4. Bipolar −10V to +10V

FIGURE 4 BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −10.000 to +9.995 volts, with positive full scale occurring with all bits ON (all 1s).

Step I . . . Offset Adjust
Turn OFF all bits except the MSB. Adjust 50kΩ trimmer R1 to give 0.000 volts output.

Step II . . . Gain Adjust
Turn ON all bits. Adjust 2kΩ gain trimmer R2 to give a reading of +9.995 volts. Turn OFF all bits. The output should read −10.000 volts. It may be necessary to repeat steps 1 and 2 for the optimal calibration.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, an op amp trim is unnecessary unless the untrimmed offset drift of the op amp is excessive.

OTHER VOLTAGE RANGES

The AD6012 can be easily configured for other voltage ranges by using either larger or smaller gain setting resistors and/or an offset resistor from the precision reference. For example, by substituting 1.24kΩ for the 2.49kΩ resistors and 625Ω for the 1.24kΩ resistor in Figure 4, the output voltage swing will be ±5V. A similar modification on the unipolar circuit of Figure 3 will yield an output voltage range of 0 to +5V.

In addition, the complement of the output voltage can be achieved by switching I_{OUT} and $\overline{I_{OUT}}$. Starting with the unipolar connection in Figure 3 and switching the outputs results in an output voltage swing of +10V to 0V. Specifically, an input of all zeros causes an output of +9.9976V, and all ones causes 0V. Going one step farther and shifting the output by the addition of a 2.49kΩ resistor from $\overline{I_{OUT}}$ to the 10V reference results in an output voltage going from 0 to −9.9976V. This circuit is shown in Figure 5.

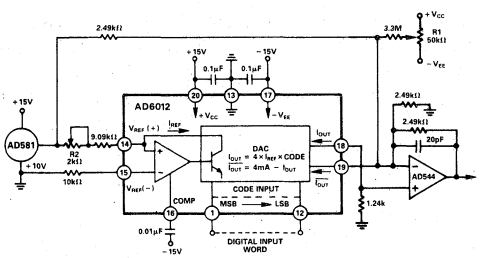


Figure 5. Negative Unipolar 0V to −10V

POWER SUPPLY DECOUPLING

As in any video speed circuit, low impedance ground returns and decoupled power supplies are critical for proper circuit operation. A minimum of 0.1μF bypass capacitor is recommended on the positive and negative supplies. In circuits with at least 400mV headroom on the negative supply, settling time can be enhanced with the RC decoupling circuit shown below:

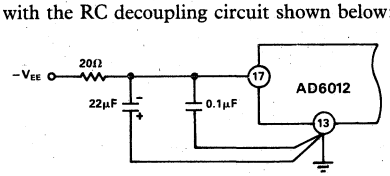


Figure 6.

OUTPUT VOLTAGE COMPLIANCE

The AD6012 has a typical output compliance range from −5V to +10V. The current-steering output stages will be unaffected by changes in the output terminal voltage over that range. However, there is an equivalent output impedance of 10MΩ in parallel with 25pF at the output terminal which produces an equivalent error current if the voltage deviates from analog common. This is a linear effect which does not change with input code. Operation beyond the compliance limits may cause either output stage saturation or breakdown which results in nonlinear performance. Compliance limits are not affected by the positive power supply, but are a function of output current and negative supply, as shown in Figure 7.

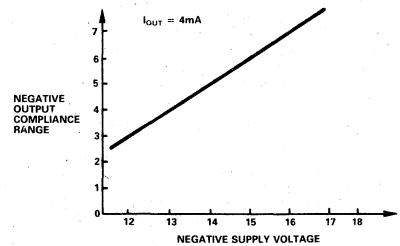


Figure 7. Typical Negative Compliance Range vs. Negative Supply

DIRECT UNBUFFERED VOLTAGE OUTPUT FOR CABLE DRIVING

The wide compliance range allows direct current-to-voltage conversion with just an output resistor. Figure 8 shows a connection using the gain and bipolar output resistors to give a ±5V bipolar swing. In this situation, the digital code is complementary binary. Other combinations of gain and offset resistors can be used to scale to alternate voltage ranges, simply by appropriately scaling the 0 to −4mA output current and using the 10V reference voltage for bipolar offset. For example, setting $R_X = 555\Omega$ gives a ±1 volt range with a 500Ω equivalent output impedance.

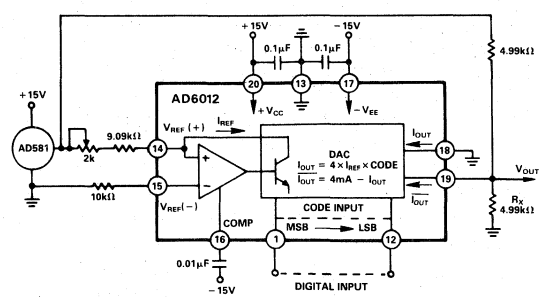


Figure 8. Unbuffered Bipolar Voltage Output

This connection is especially useful for direcly driving a long cable at high speed. Using a 51Ω resistor for R_X would allow interface to a 50Ω cable with a ±100mV full scale swing. Settling time would be very fast since the load impedance matches the characteristic impedance of the cable.

REFERENCE AMPLIFIER CONNECTIONS

The current into the reference amplifier at pin 14 must be approximately 1mA to realize the full scale output current of 4mA. If a dc reference is used, a 0.01μF compensation capacitor should be connected between pin 16 and $-V_{EE}$. However, for ac reference applications, a minimum value is often used for the compensation capacitor to maximize bandwidth. The value of this capacitor is dependent upon the equivalent resistance at pin 14. The values to maximize bandwidth without oscillation are as follows:

R14 Equiv. (kΩ)	C16 (pF)
10	50
5	25
2	10
1	5
0.5	0

HIGH SPEED 12-BIT A/D CONVERTERS

The fast settling characteristics of the AD6012 make it ideal for high speed successive approximation A/D converters.

Shown in Figure 9 is a configuration using standard components; this system completes a full 12-bit conversion in 8.5μs unipolar or bipolar. This converter will have 12 bits of resolution and have a typical gain T.C. of 10ppm/°C.

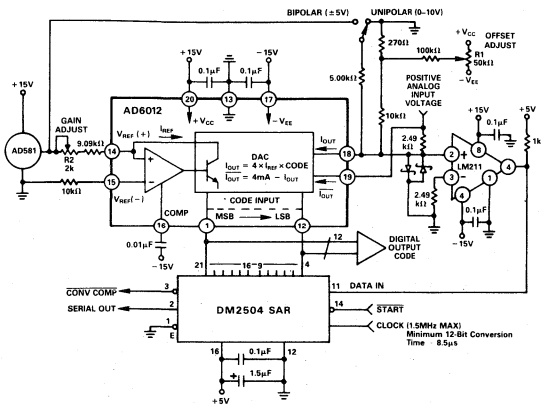


Figure 9. Analog-to-Digital Converter

In the unipolar mode, the system range is 0 to 9.9976 volts, with each bit having a value of 2.44mV. For true conversion accuracy, an A/D converter should be trimmed so that a given bit code output results from input levels from 1/2LSB below to 1/2LSB above the exact voltage which that code represents. Therefore, the converter zero point should be trimmed with an input voltage of +1.22mV; trim R1 until the LSB just begins to appear in the output code (all other bits "0"). For full scale, use an input voltage of +9.9963 volts (10 volts – 1LSB – 1/2LSB); then trim R2 until the LSB just begins to appear (all other bits "1").

The bipolar signal range is −5.0 to +4.9976 volts. Bipolar offset trimming is done by applying a −4.9988V input signal and trimming R1 for the LSB transition (all other bits "0"). Full scale is set by applying +4.9963 volts and trimming R2 for the LSB transition (all other bits "1").

For fastest operation, the impedance at the comparator summing node must be minimized. However, lowering the impedance will reduce the voltage signal to the comparator (at an equivalent impedance at the summing node of 1kΩ, 1LSB = 1.0mV) to the point that comparator performance will be sacrificed. The contribution to this impedance from the DAC will be approximately 10MΩ.

To prevent dynamic errors, the input signal should have a low dynamic source impedance, such as that of the AD509 high speed op amp.

D/A CONVERTER DISPLAYS

In Figure 10, a latched AD6012 is shown as a CRT deflection controller. Using the resistors shown, the output to the CRT yoke will swing ±110V. With a second AD6012 in the same configuration, both the vertical and horizontal position can be controlled. As in all vector scan schemes, this circuit provides a method of precisely locating the beam with minimum delay between locations. The AD6012 is an ideal choice in these applications since its settling time is only 500ns max. With a frame update time of 1/60th of a second, more than 33 thousand locations can be covered in each frame.

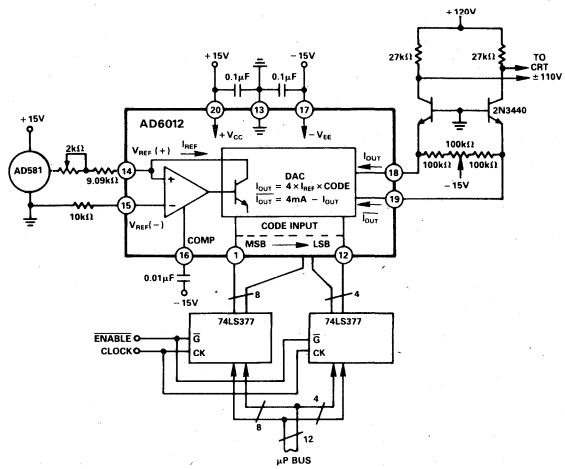


Figure 10. Vector Scan Video CRT Control

In raster scan applications, the AD6012 can be used for the slower vertical sweep. However, the horizontal sweep requires a settling time of 100ns or less to achieve a picture of suitable quality. In either vector or raster scan applications, a third AD6012 can be used for intensity modulation. In addition to its fast settling time, the reference can be clamped to zero whenever "blacker than black" is required (for retrace or lead zeroes in picture field).

LOGIC BIASING

The AD6012 can be used with many different logic families by setting GND/V_{LC} (Pin 13) at two diode drops below the desired logic threshold voltage. When GND/V_{LC} is connected to logic common, the AD6012 inputs interface directly to TTL. Other logic families can be connected directly to the logic inputs by using the logic bias circuit shown in Figure 11.

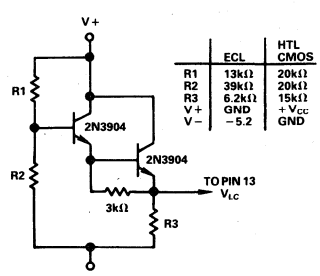


Figure 11. HTL, CMOS, or ECL Bias Circuit

ANALOG DEVICES

CMOS LOGDAC™ Digitally Controlled Audio Attenuator

AD7110*

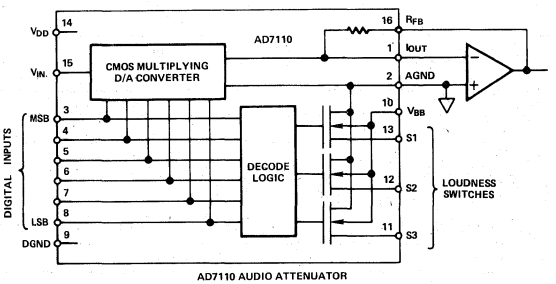
FEATURES

Attenuation Range: 0 to 88.5dB Plus Full Muting
Resolution: 1.5dB
Low Distortion: THD Better Than -98dB
IMD Better Than -92dB
Includes Switches for Loudness Compensation
Low Power Consumption
Excellent S/N Ratio: 100dB (20Hz – 20kHz)
Low Cost
Complies with DIN 45403 and DIN 45405
Latch-Proof Operation

APPLICATIONS

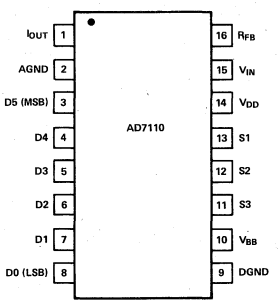
Digitally Controlled Audio Gain
Wide Dynamic Range D/A Converters

AD7110 FUNCTIONAL BLOCK DIAGRAM



AD7110 AUDIO ATTENUATOR

PIN CONFIGURATION



16-PIN DIP
TOP VIEW

GENERAL DESCRIPTION

The AD7110 is a monolithic CMOS digitally controlled audio attenuator (patent pending). With the addition of an external operational amplifier it provides 0 to 88.5dB of attenuation in 1.5dB steps, plus full muting of the audio input signal for digital input code 1111XX, where X can be 1 or 0. The audio input is applied to the V_{IN} pin and the device delivers a logarithmically related output current which is determined by a 6-bit binary input code. Loudness compensation switches are provided on the device to enable additional bass boost at low volume settings.

The device is manufactured using an advanced thin-film on CMOS monolithic wafer fabrication process and is packaged in a 16-pin DIP.

ORDERING INFORMATION

Model	Package	Operating Temperature Range
AD7110KN	16-Pin Plastic DIP	0 to +50°C

Package Style:[1] N16B

*Patent Pending
LOGDAC is a registered trademark of Analog Devices, Inc.

[1] See Section 19 for package outline information.

AUDIO SPECIFICATIONS

(V_{DD} = +12V, V_{BB} = 0 to -12V, Pins 11-13 Open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	AD7110 WITH "IDEAL OP AMP"	AD7110 WITH TL071 OP-AMP (FIG. 1)	UNITS	TEST CONDITIONS/COMMENTS
ATTENUATION RANGE	0 to -88.5	0 to -88.5	dB	V_{IN} = 10V rms @ 1kHz
RESOLUTION	1.5 max	1.5 max	dB	Frequency Range: 20Hz to 20kHz
ATTENUATION ACCURACY (Absolute) 0dB to -48dB -48dB to -88.5dB	 ±0.7 max Monotonic	 ±0.7 max Monotonic	 dB	The AD7110 is guaranteed monotonic for all attenuation settings between 0 and -88.5dB
TOTAL HARMONIC DISTORTION (THD)	-98 max	-85 typ	dB	per DIN 45403, BLATT 2 (with input level of 1V rms)
INTERMODULATION DISTORTION (IMD)	-92 max	-79 typ	dB	per DIN 45403, BLATT 4
V_{IN}	30 max	10 max	V peak	for <1% (max) THD (Note 1)
FEEDTHROUGH ERROR	Better than -85dB @ 1kHz. Feedthrough is primarily dependent upon printed circuit board layout.			
OUTPUT NOISE VOLTAGE DENSITY	30 max	70 typ	$nV/\sqrt{Hz}$	20Hz to 20kHz (Note 2)
BANDWIDTH	D.C. to 150 min	D.C. to 250 typ	kHz	0dB Attenuation

ELECTRICAL SPECIFICATIONS

(V_{DD} = +12V, V_{BB} = 0 to -12V, Pins 11-13 Open, T_A = 0 to +50°C unless otherwise noted)

PARAMETER	LIMIT	TEST CONDITIONS/COMMENTS
ANALOG INPUT		Input resistance for a given unit is constant for all input conditions.
Input Resistance of V_{IN} (pin 15)	18kΩ max 9kΩ min	 V_{OUT} = 0V
LOUDNESS SWITCHES		
Switch ON Resistance R_{ON}	 600Ω max	 Switch Current = 1mA
Switch OFF Leakage Current	1μA max	V_{switch} = +12V
Switch Coding	See Table 1	
DIGITAL INPUTS		
V_{INH}	11.5V min	
V_{INL}	0.5V max	
I_{INH}	1μA max	
I_{INL}	1μA max	
C_{IN}	5pF typ	
POWER REQUIREMENTS		
V_{DD}	+12V	
V_{DD} Range	+5V to +12V	Functionality with degraded performance.
V_{BB}	-12V	
I_{DD}	1mA max	Digital Inputs = V_{INL} or V_{INH}
I_{BB}	100μA max	
Total Power Dissipation	5mW typ	

NOTES

[1] Output amplifier (and amplifier supplies) must be capable of 30V peak output.

[2] Output noise voltage density includes op amp noise.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

*V_{DD} (to GND)	+14V
*V_{BB} (to GND)	-14V
Voltage (pins 11, 12, 13) to GND	V_{BB}, +14V
V_{IN} (to GND)	±35V
Digital Input Voltage to GND	-0.3V to V_{DD}
Output Voltage (Pin 1) to GND	-100mV to VDD
Power Dissipation (Package)	670mW
Operating Temperature	0 to +70°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

*If Loudness Compensation Switches (S1, S2, S3) are not used, the negative power supply may be omitted and V_{BB} (Pin 10) connected instead to DGND (Pin 9). In this case the absolute maximum rating of V_{DD} is +17V.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes. The AD7110 resolution is 1.5dB.

MONOTONICITY: The AD7110 digitally controlled audio attenuator is monotonic if the analog output decreases (or remains constant) as the digital input code (attenuation setting) increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when the digital input code is set to mute the input signal.

ANALOG CIRCUIT PERFORMANCE:

Table I gives the nominal attenuation in dB for the AD7110 for all digital input codes. It also shows the Loudness Switch states and the nominal output voltage when using an external operational amplifier (as shown in Figure 1) and a fixed -10 volt reference applied to V_{IN} (pin 15). It may be seen that the transfer function for the circuit of Figure 1 is given by

$$V_{OUT} = -V_{IN}\ 10\ \exp -\left\{\frac{1.5N}{20}\right\}$$

where N is the binary input for values 0 to 59. For N = 60 through 63 the input is fully muted, that is, the attenuation is infinite.

HIGH FREQUENCY AMPLIFIERS

R_{FB} and the output capacitance of the AD7110 create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 30—50pF of feedback capacitance (C1) ensures stability.

DC PERFORMANCE OF AD7110

For fixed-reference applications, an output amplifier with low offset voltage (less than 50μV) is required, e.g. the AD517L. This combination will provide the utmost stability at the expense of slow settling times.

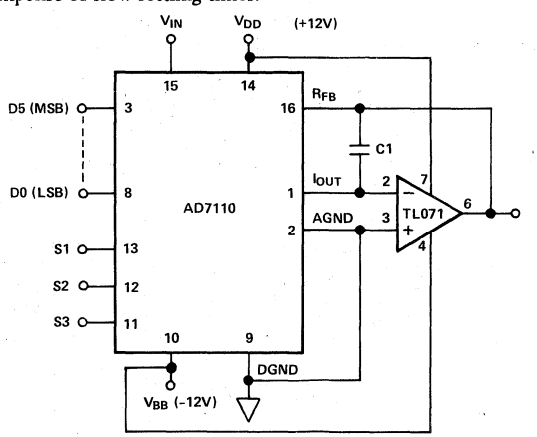


Figure 1.

9

Table I

N	Digital Input D5 D0	Attenuation dB	Switches[1] S1	S2	S3	V_{OUT}[2]
0	00 00 00	0.0				10.00
1	00 00 01	1.5				8.414
2	00 00 10	3.0				7.079
3	00 00 11	4.5				5.957
4	00 01 00	6.0				5.012
5	00 01 01	7.5				4.217
6	00 01 10	9.0				3.548
7	00 01 11	10.5				2.985
8	00 10 00	12.0				2.512
9	00 10 01	13.5				2.113
10	00 10 10	15.0				1.778
11	00 10 11	16.5				1.496
12	00 11 00	18.0				1.259
13	00 11 01	19.5				1.059
14	00 11 10	21.0				0.891
15	00 11 11	22.5				0.750
16	01 00 00	24.0				0.631
17	01 00 01	25.5				0.531
18	01 00 10	27.0				0.447
19	01 00 11	28.5				0.376
20	01 01 00	30.0				0.316
21	01 01 01	31.5				0.266
22	01 01 10	33.0				0.224
23	01 01 11	34.5				0.188
24	01 10 00	36.0				0.158
25	01 10 01	37.5				0.133
26	01 10 10	39.0				0.112
27	01 10 11	40.5				0.0944
28	01 11 00	42.0				0.0794
29	01 11 01	43.5				0.0668
30	01 11 10	45.0				0.0562
31	01 11 11	46.5				0.0473
32	10 00 00	48.0	■			0.0398
33	10 00 01	49.5	■			0.0335
34	10 00 10	51.0	■			0.0282
35	10 00 11	52.5	■			0.0237
36	10 01 00	54.0	■			0.0200
37	10 01 01	55.5	■			0.0168
38	10 01 10	57.0	■			0.0141
39	10 01 11	58.5	■			0.0119
40	10 10 00	60.0		■		0.0100
41	10 10 01	61.5		■		0.00841
42	10 10 10	63.0		■		0.00708
43	10 10 11	64.5		■		0.00596
44	10 11 00	66.0		■		0.00501
45	10 11 01	67.5		■		0.00422
46	10 11 10	69.0		■		0.00355
47	10 11 11	70.5		■		0.00299
48	11 00 00	72.0		■		0.00251
49	11 00 01	73.5		■		0.00211
50	11 00 10	75.0		■		0.00178
51	11 00 11	76.5		■		0.00150
52	11 01 00	78.0		■		0.00126
53	11 01 01	79.5		■		0.00106
54	11 01 10	81.0		■		0.000891
55	11 01 11	82.5		■		0.000750
56	11 10 00	84.0		■		0.000631
57	11 10 01	85.5		■		0.000531
58	11 10 10	87.0		■		0.000447
59	11 10 11	88.5		■		0.000376
60	11 11 XX[3]	∞		■	■	

NOTES:
[1] Switch closed in shaded area.
[2] V_{IN} = -10V dc
[3] X = 1 or 0. Output is fully muted for N≥60.

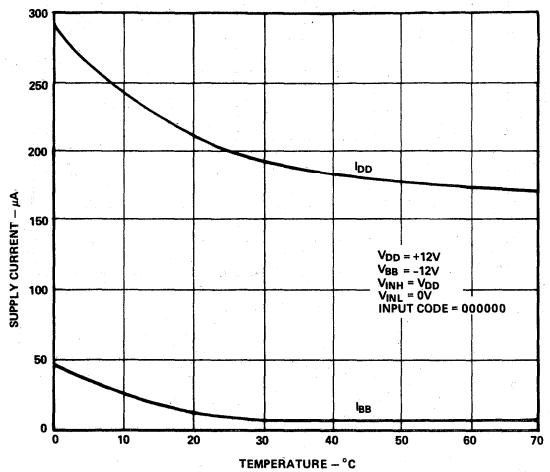


Figure 2. Power Supply Current vs. Temperature

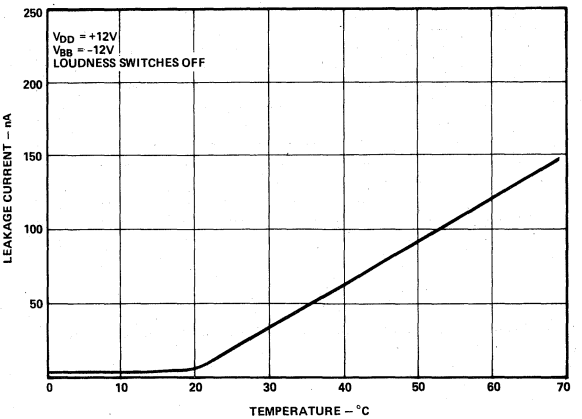


Figure 5. Loudness Switch Leakage Current vs. Temperature

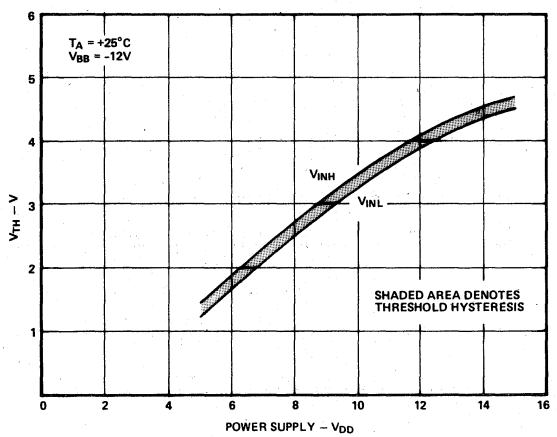


Figure 3. Digital Threshold Voltage vs. Power Supply Voltage

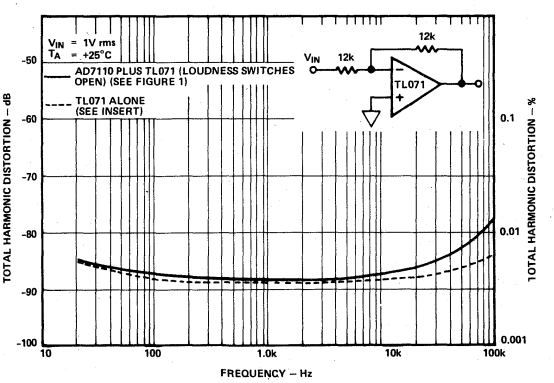


Figure 6. Total Harmonic Distortion vs. Frequency

Figure 6 shows that the total harmonic distortion of the attenuator circuit of Figure 1 is almost totally dependent on the characteristics of the operational amplifier used.

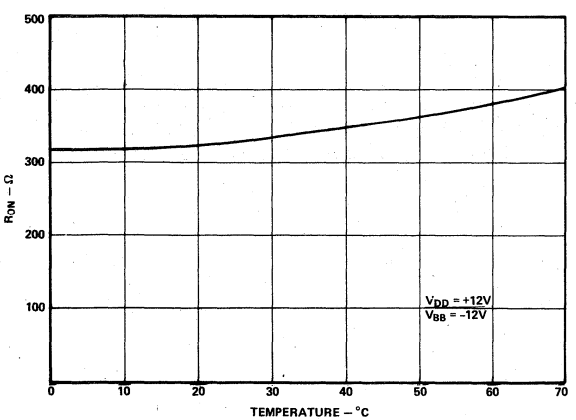


Figure 4. Loudness Switch On Resistance vs. Temperature

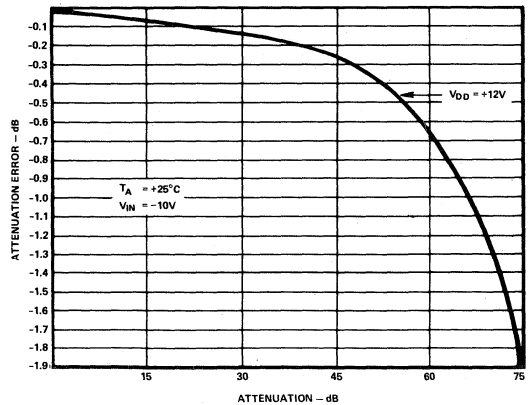


Figure 7. Typical dc Attenuation Error vs. Attenuation

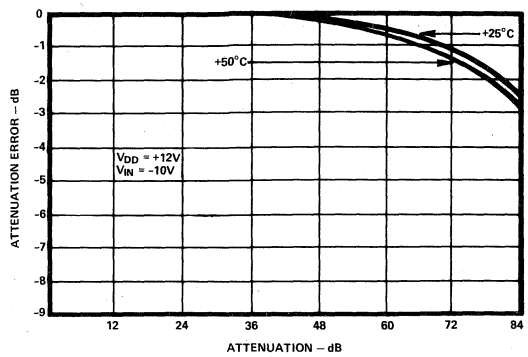


Figure 8. Typical dc Attenuation Error vs. Attenuation & Temperature

Applications Information

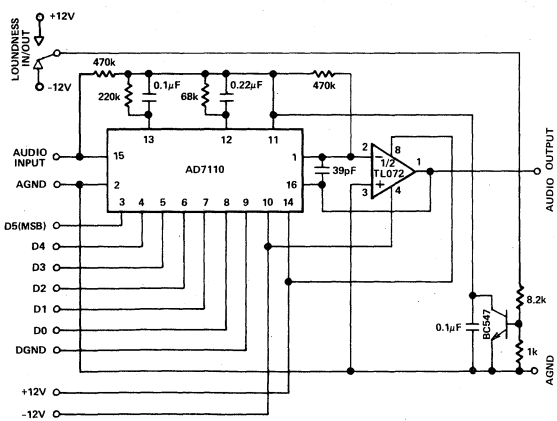


Figure 9. Single Channel Audio Attenuator with Loudness Compensation

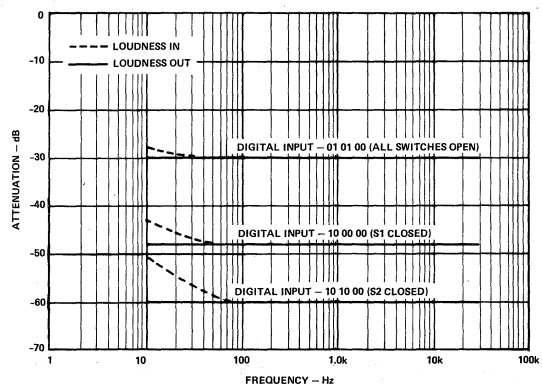


Figure 10.

Figure 10 shows the Attenuation vs. Frequency for the circuit of Figure 9. The attenuation is plotted against frequency for the two digital input codes at which the loudness compensation switches S1 and S2 are activated.

ANALOG DEVICES

LOGDAC™ CMOS Logarithmic D/A Converter*

AD7111

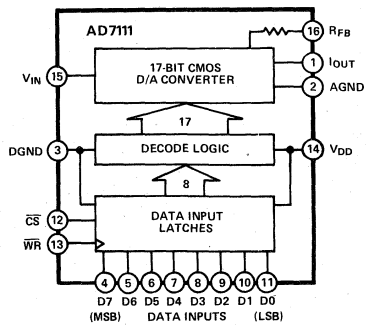
FEATURES

Dynamic Range: 88.5dB
Resolution: 0.375dB
On-Chip Data Latches
Full ±25V Input Range Multiplying DAC
Low Distortion
Single +5V Supply
Latch-Up Free (No Protection Schottky Required)

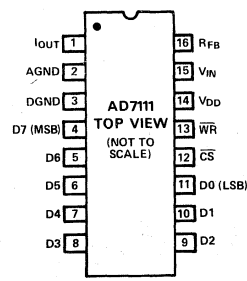
APPLICATIONS

Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

AD7111 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7111 is a CMOS multiplying D/A converter which can attenuate an analog input signal over the range 0 to -88.5dB in 0.375dB steps.

The degree of attenuation is determined by an 8-bit data word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{CS}$ and $\overline{WR}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is packaged in a 16-pin dual-in-line plastic, cerdip or ceramic package.

ORDERING INFORMATION

Specified Accuracy Range	Temperature Range and Package		
	Plastic 0 to +70°C	Cerdip[1] -25°C to +85°C	Ceramic -55°C to +125°C
0 to 60dB	AD7111KN	AD7111BQ	AD7111TD
0 to 72dB	AD7111LN	AD7111CQ	AD7111UD

NOTE
[1] Analog Devices reserves the right to ship Ceramic packages in lieu of Cerdip packages.
*Patent Pending

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP (D16B)
Suffix N: Plastic DIP (N16B)
Suffix Q: Cerdip (Q16B)

[1] See Section 19 for package outline information.

9

SPECIFICATIONS (V_{DD} = +5V, V_{IN} = -10V dc, V_{PIN2} = V_{PIN1} = 0V, output amplifier AD544 except where stated)

Parameter	AD7111L/C/U GRADES T_A = +25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.375	0.375	0.375	0.375	dB	
ACCURACY RELATIVE TO 0dB ATTENUATION						
0.375dB Steps:						
Accuracy ≤ ±0.17dB	0 to 36	0 to 36	0 to 30	0 to 30	dB min	Guaranteed attenuation ranges
Monotonic	0 to 54	0 to 54	0 to 48	0 to 48	dB min	for specified step sizes
0.75dB Steps:						
Accuracy ≤ ±0.35dB	0 to 48	0 to 42	0 to 42	0 to 36	dB min	
Monotonic	0 to 72	0 to 66	0 to 72	0 to 60	dB min	
1.5dB Steps:						
Accuracy ≤ ±0.7dB	0 to 54	0 to 48	0 to 48	0 to 42	dB min	
Monotonic	Full Range	0 to 78	0 to 85.5	0 to 72	dB min	Full Range is from 0 to 88.5dB
3.0dB Steps:						
Accuracy ≤ ±1.4dB	0 to 66	0 to 54	0 to 60	0 to 48	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
6.0dB Steps:						
Accuracy ≤ ±2.7dB	0 to 72	0 to 60	0 to 60	0 to 60	dB min	
Monotonic	Full Range	Full Range	Full Range	Full Range		
GAIN ERROR	±0.1	±0.15	±0.15	±0.20	dB max	
V_{IN} INPUT RESISTANCE (PIN 15)	9/11/15	9/11/15	7/11/18	7/11/18	kΩ min/typ/max	
R_{FB} INPUT RESISTANCE (PIN 16)	9.3/11.5/15.7	9.3/11.5/15.7	7.3/11.5/18.8	7.3/11.5/18.8	kΩ min/typ/max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±10	±1	±10	μA max	Digital Inputs = V_{DD}
SWITCHING CHARACTERISTICS[1]						
t_{CS}	0	0	0	0	ns min	Chip Select to Write Setup Time
t_{CH}	0	0	0	0	ns min	Chip Select to Write Hold Time
t_{WR}	350	500	350	500	ns min	Write Pulse Width
t_{DS}	175	250	175	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	10	10	ns min	Data Valid to Write Hold Time
t_{RFSH}	3	4.5	3	4.5	μs min	Refresh Time
POWER SUPPLY						
V_{DD}	+5	+5	+5	+5	V	
I_{DD}	1	4	1	4	mA max	Digital Inputs = V_{IH} or V_{IL}
	500	1000	500	1000	μA max	Digital Inputs = 0V or V_{DD}. See Figure 7.

NOTE
[1] Sample tested at +25°C to ensure compliance.
Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.
V_{DD} = +5V, V_{IN} = -10V dc except where stated, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated.

Parameter	AD7111L/C/U GRADES T_A = 25°C	AD7111L/C/U GRADES T_A = T_{min}, T_{max}	AD7111K/B/T GRADES T_A = +25°C	AD7111K/B/T GRADES T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC Supply Rejection, ΔGain/ΔV_{DD}	0.001	0.005	0.001	0.005	dB per % max	ΔV_{DD} = ±10%, Input Code = 00000000
Propagation Delay	3.0	4.5	3.0	4.5	μs max	Full Scale Change Measured from $\overline{WR}$ going high, $\overline{CS}$ = 0V.
Digital to Analog Glitch Impulse	100	–	100	–	nV secs typ	Measured with ADLH0032CG as Output Amplifier for Input Code Transition 10000000 to 00000000. C1 of Figure 1 is 0pF
Output Capacitance, Pin 1	185	185	185	185	pF max	
Input Capacitance, Pin 15 and Pin 16	7	7	7	7	pF max	
Feedthrough at 1kHz	-94	-72	-92	-68	dB max	Feedthrough is also determined by circuit
Total Harmonic Distortion	-91	-91	-91	-91	dB typ	layout (see Figure 4).
Output Noise Voltage Density	70	70	70	70	nV/√Hz max	V_{IN} = 6V rms at 1kHz
Digital Input Capacitance	7	7	7	7	pF max	Includes AD544 Amplifier Noise

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (to DGND) . . . . . +7V
V_{IN} (to AGND) . . . . . ±35V
Digital Input Voltage to DGND . . . . . −0.3V to V_{DD}
Output Voltage (Pin 1) to AGND . . . . . −0.3V to V_{DD}
V_{RFB} to AGND . . . . . ±35V
AGND to DGND . . . . . 0 to V_{DD}
DGND to AGND . . . . . 0 to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C 670mW
Derates Above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D) or Cerdip (Suffix Q)
To +75°C 450mW
Derates Above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (KN, LN Versions) . . . . . 0 to +70°C
Industrial Ceramic (BQ, CQ Versions) . . . . −25°C to +85°C
Extended Ceramic (TD, UD Versions) . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

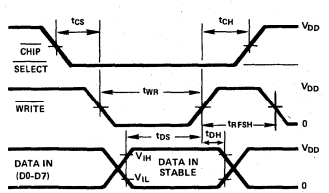
ACCURACY: The difference (measured in dB) between the ideal transfer function as listed in Table I and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL TO ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7111 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 8-bit binary input into a 17-bit word which is used to drive the D/A converter. Input data on the D7–D0 bus is loaded into the input data latches using $\overline{CS}$ and $\overline{WR}$ control signals. The rising edge of $\overline{WR}$ latches the input data and initiates the internal data transfer to the decoder. A minimum time t_{RFSH}, the refresh time, is required for the data to propagate through the decoder before a new data write is attempted.

The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10\ \exp - \frac{0.375\ N}{20}$$

or

$$\left|\frac{V_O}{V_{IN}}\right| \text{ dB} = -0.375\ N$$

Where 0.375 is the step size (resolution) in dB and N is the input code in decimal for values 0 to 239. For $240 \leqslant N \leqslant 255$ the output is zero. Table I gives the output attenuation relative to 0dB for all possible input codes.

The graphs on the last page give a pictorial representation of the specified accuracy and monotonic ranges for all grades of the AD7111. High attenuation levels are specified with less accuracy than low attenuation levels. The range of monotonic behavior depends upon the attenuation step size used. For example, the AD7111L is guaranteed monotonic in 0.375dB steps from 0 to -54dB inclusive and in 0.75dB steps from 0 to -72dB inclusive. To achieve monotonic operation over the entire 88.5dB range it is necessary to select input codes so that the attenuation step size at any point is consistent with the step size guaranteed for monotonic operation at that point.

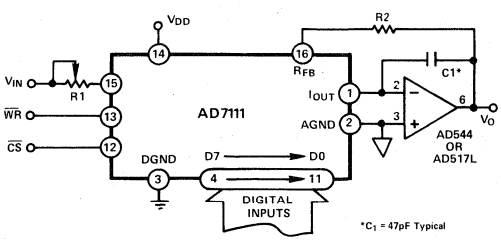


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7111 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C–see Figure 11. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 60pF to 185pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A converters" which is available from Analog Devices, Publication Number G479–15–8/78.

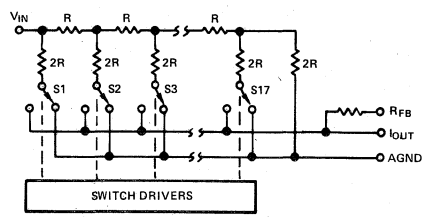


Figure 2. Simplified D/A Circuit of AD7111

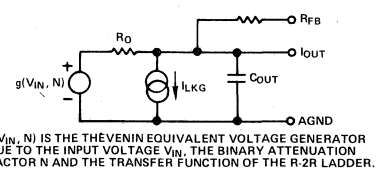


Figure 3. Equivalent Analog Output Circuit of AD7111

D7–D4 \ D3–D0	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	0.0	0.375	0.75	1.125	1.5	1.875	2.25	2.625	3.0	3.375	3.75	4.125	4.5	4.875	5.25	5.625
0001	6.0	6.375	6.75	7.125	7.5	7.875	8.25	8.625	9.0	9.375	9.75	10.125	10.5	10.875	11.25	11.625
0010	12.0	12.375	12.75	13.125	13.5	13.875	14.25	14.625	15.0	15.375	15.75	16.125	16.5	16.875	17.25	17.625
0011	18.0	18.375	18.75	19.125	19.5	19.875	20.25	20.625	21.0	21.375	21.75	22.125	22.5	22.875	23.25	23.625
0100	24.0	24.375	24.75	25.125	25.5	25.875	26.25	26.625	27.0	27.375	27.75	28.125	28.5	28.875	29.75	29.625
0101	30.0	30.375	30.75	31.125	31.5	31.875	32.25	32.625	33.0	33.375	33.75	34.125	34.5	34.875	35.25	35.625
0110	36.0	36.375	36.75	37.125	37.5	37.875	38.25	38.625	39.0	39.375	39.75	40.125	40.5	40.875	41.25	41.625
0111	42.0	42.375	42.75	43.125	43.5	43.875	44.25	44.625	45.0	45.375	45.75	46.125	46.5	46.875	47.25	47.625
1000	48.0	48.375	48.75	49.125	49.5	49.875	50.25	50.625	51.0	51.375	51.75	52.125	52.5	52.875	53.25	53.625
1001	54.0	54.375	54.75	55.125	55.5	55.875	56.25	56.625	57.0	57.375	57.75	58.125	58.5	58.875	59.25	59.625
1010	60.0	60.375	60.75	61.125	61.5	61.875	62.25	62.625	63.0	63.375	63.75	64.125	64.5	64.875	65.25	65.625
1011	66.0	66.375	66.75	67.125	67.5	67.875	68.25	68.625	69.0	69.375	69.75	70.125	70.5	70.875	71.25	71.625
1100	72.0	72.375	72.75	73.125	73.5	73.875	74.25	74.625	75.0	75.375	75.75	76.125	76.5	76.875	77.25	77.625
1101	78.0	78.375	78.75	79.125	79.5	79.875	80.25	80.625	81.0	81.375	81.75	82.125	82.5	82.875	83.25	83.625
1110	84.0	84.375	84.75	85.125	85.5	85.875	86.25	86.625	87.0	87.375	87.75	88.125	88.5	88.875	89.25	89.625
1111	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE	MUTE

Table I. Ideal Attenuation in dB vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7111 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7111 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

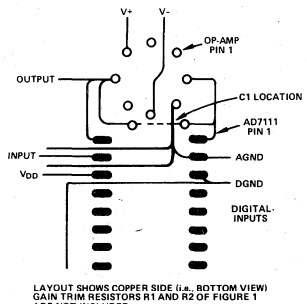


Figure 4. Suggested Layout for AD7111 and Op-Amp

It is recommended that when using the AD7111 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7111 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

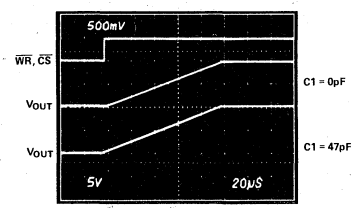


Figure 5. Response of AD7111 with AD517

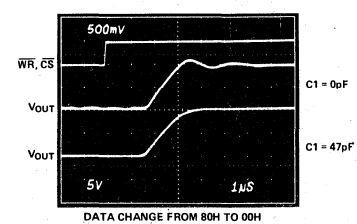


Figure 6. Response of AD7111 with AD544

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7111 has been designed to minimize these glitches as much as possible.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 12. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7111.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7111 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 11.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7111 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7111 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7111 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7111 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7111 D/A converter circuit results in a constant attenuation error over the whole range. The AD7111 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors—R1 and R2 in Figure 1—can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00000000. The accuracy and monotonic range specifications of the AD7111 are not affected in any way by this gain trim procedure. For the AD7111L/C/U grades, suitable values for R1 and R2 of Figure 1 are R1 = 500Ω, R2 = 180Ω; for the K/B/T grades suitable values are R1 = 1000Ω, R2 = 270Ω. For additional information on gain error the reader is referred to Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices Inc., Publication Number E630–10–6/81.

Typical Performance Characteristics

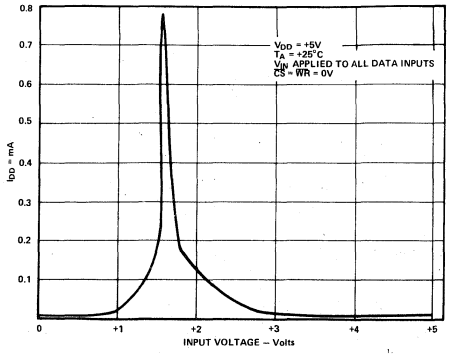


Figure 7. Typical Supply Current vs. Logic Input Level

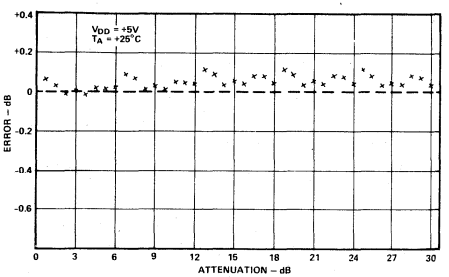


Figure 8. Typical Attenuation Error for 0.75dB Steps

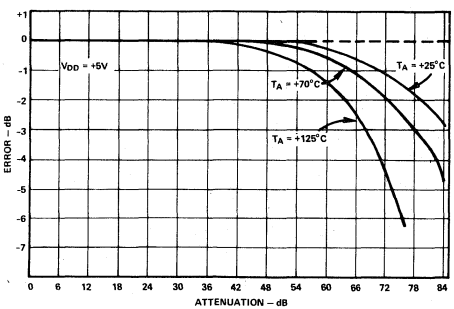


Figure 9. Typical Attenuation Error for 3dB Steps vs. Temperature

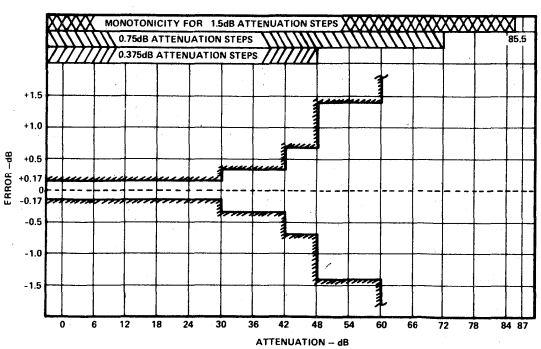


Figure 10. Accuracy Specification for K/B/T Grade Devices at T_A = +25°C

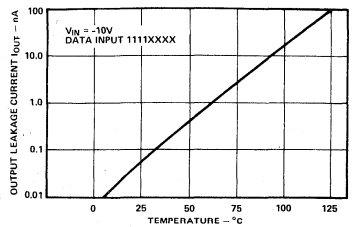


Figure 11. Output Leakage Current vs. Temperature

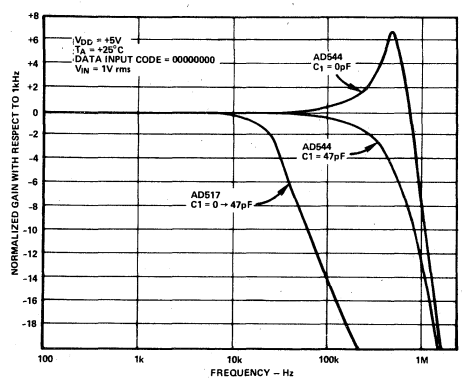


Figure 12. Frequency Response with AD544 and AD517 Amplifiers

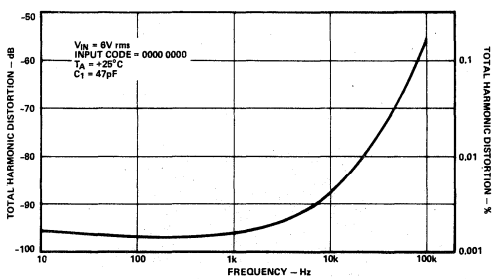


Figure 13. Distortion vs. Frequency Using AD544 Amplifier

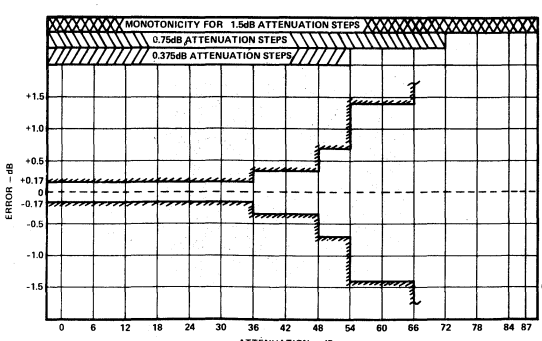


Figure 14. Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ANALOG DEVICES

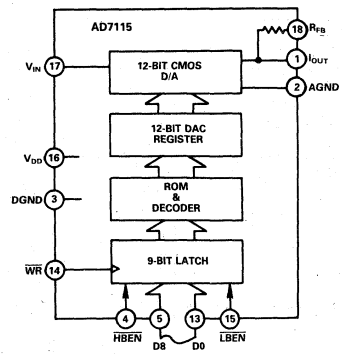
LOGDAC™ CMOS 0.1dB Step Attenuator

AD7115

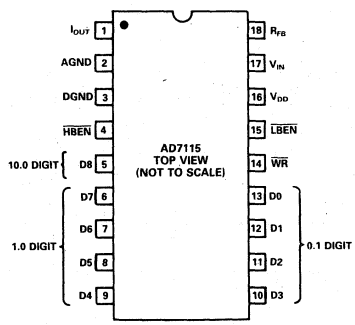
FEATURES
Dynamic Range: 0 to 19.9dB Plus Full Muting
Resolution: 0.1dB
2 1/2 Digit BCD Input Coding
On-Chip Data Latches
Full ±25V Input Range
Low Distortion and Noise
Latch-Up Free (No Protection Schottky Required)
TTL Compatible

APPLICATIONS
Audio Attenuators
Function Generators
Test Equipment
Digitally Controlled AGC Systems

AD7115 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7115 is a digitally programmable attenuator which attenuates an analog input signal over the range 0 to −19.9dB in 0.1dB steps.

The degree of attenuation is controlled by a 2 1/2 digit BCD coded input word which is latched into on-chip data latches using microprocessor compatible control signals $\overline{WR}$, $\overline{LBEN}$ and $\overline{HBEN}$. Operating frequency range of the device is from dc to several hundred kHz.

The device is packaged in an 18-pin dual-in-line plastic, cerdip or ceramic package.

PRODUCT HIGHLIGHTS

1. High resolution 0.1dB steps from 0 to 19.9dB with step accuracies better than ±0.04dB allow precision attenuators and other special purpose function generators to be built at low cost.
2. A resolution of 0.1dB is equivalent to step sizes of 1% of reading.
3. The 2 1/2 digit BCD input code can be loaded into the on-chip latches in one $\overline{WRITE}$ operation. Alternatively, for use with an 8-bit data bus, data can be loaded in two $\overline{WRITE}$ operations by using byte enable signals $\overline{HBEN}$ and $\overline{LBEN}$.
4. The AD7115 can be used in series with standard attenuator blocks to position its attenuation range as required, e.g., −40dB to −60dB in 0.1dB steps.
5. Analog input signal can be up to ±25V with V_{DD} = +5V.

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LOGDAC is a registered trademark of Analog Devices, Inc.

SPECIFICATIONS (V_{DD} = +5V, V_{IN} = −10V dc, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated)

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Conditions/Comments
NOMINAL RESOLUTION	0.1	0.1	dB	Full range is from 0 to 19.9dB. A resolution of 0.1dB is equivalent to steps of 1% of Reading
ACCURACY RELATIVE TO 0dB ATTENUATION	±0.04	±0.05	dB max	Accuracy is measured using circuit of Figure 4 and excludes any gain error effects due to mismatch between R_{FB} and the R-2R ladder circuit.
GAIN ERROR (at 0dB)	±0.1	±0.12	dB max	Typical gain change over 100°C range is ±0.01dB
INPUT RESISTANCE V_{IN} (pin 17), R_{FB} (pin 18)	7/11/18	7/11/18	kΩ min/typ/max	
DIGITAL INPUTS V_{IH} (Input High Voltage) V_{IL} (Input Low Voltage) Input Leakage Current	 2.4 0.8 ±1	 2.4 0.8 ±10	 V min V max μA max	 Digital Inputs = V_{DD} or 0V
SWITCHING CHARACTERISTICS[2]				
t_{WR}	600	800	ns min	Write Pulse Width. See Figure 1.
t_{DS}	170	250	ns min	Data Valid to Write Setup Time
t_{DH}	10	10	ns min	Data Valid to Write Hold Time
t_{ENS}	0	0	ns min	Byte Enable to Write Setup Time
t_{ENH}	0	0	ns min	Byte Enable to Write Hold Time
t_{RFSH}	4	6	μs min	Refresh Time
POWER SUPPLY V_{DD} I_{DD}	 +5 4	 +5 4	 V mA max	 Digital Inputs = V_{IH} or V_{IL}, See Figure 10.

NOTES
[1]Temperature range as follows: KN Version; 0 to +70°C
BQ Version; −25°C to +85°C
TD Version; −55°C to +125°C

[2]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.

V_{DD} = +5V, V_{IN} = −10V dc except where stated, V_{PIN1} = V_{PIN2} = 0V, output amplifier AD544 except where stated.

Parameter	T_A = +25°C	T_A = T_{min}, T_{max}	Units	Conditions/Comments
DC SUPPLY REJECTION $\Delta GAIN/\Delta V_{DD}$	0.0066	0.033	dB per V max	ΔV_{DD} = ±0.5V Input Code = 00.0 BCD
PROPAGATION DELAY	5	7	μs max	Full Scale Change Measured from $\overline{WR}$ going HIGH, $\overline{LBEN}$ = $\overline{HBEN}$ = 0V. See definitions on next page.
DIGITAL TO ANALOG GLITCH IMPULSE	600	–	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 00.0 BCD to Full Mute Code. See Figure 4, C1 = 0pF.
OUTPUT CAPACITANCE, PIN 1	150	150	pF max	For 00.0 input code. Output capacitance is code dependent and decreases with increasing attenuation.
FEEDTHROUGH AT 1kHz[1]	−92 −96	−68 −76	dB max dB typ	Feedthrough is also determined by circuit layout (see Figure 5).
TOTAL HARMONIC DISTORTION	−91	−91	dB typ	V_{IN} = 6V rms at 1kHz
OUTPUT NOISE VOLTAGE DENSITY	70	70	nV/√Hz typ	Includes AD544 amplifier noise. From 20Hz to 20kHz.
SIGNAL INPUT CAPACITANCE V_{IN} (pin 17), R_{FB} (pin 18)	10	10	pF max	
DIGITAL INPUT CAPACITANCE Control Input Data Input	10 5	10 5	pF max pF max	

NOTES
[1] Feedthrough may be further reduced by grounding the metal lid on the suffix D package.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	+7V
V_{IN} to AGND	±35V
V_{RFB} to AGND	±35V
Digital Input Voltage to DGND	−0.3V to V_{DD}
Output Voltage (Pin 1) to AGND	−0.3V to V_{DD}
AGND to DGND	0 to V_{DD}
DGND to AGND	0 to V_{DD}
Power Dissipation (Package)	
Plastic (Suffix N)	
To +70°C	670mW
Derates above +70°C by	8.3mW/°C
Ceramic (Suffix D) or Cerdip (Suffix Q)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial Plastic (KN Version)	0 to +70°C
Industrial Cerdip (BQ Version)	−25°C to +85°C
Extended Ceramic (TD Version)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

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TERMINOLOGY

Resolution: Nominal change in attenuation when moving between two adjacent codes.

Monotonicity: The device is monotonic if the analog output decreases (or remains constant) as the digital code (attenuation setting) increases.

Feedthrough Error: That portion of the input signal which reaches the output when the DAC is muted. See section on Dynamic Performance.

Output Leakage Current: Current which appears on the I_{OUT} terminal when the DAC is muted.

Total Harmonic Distortion: A measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

Gain Error: Gain Error is due to mismatch between R_{FB} and the R-2R ladder circuit and is a constant percentage of reading (i.e. constant dB offset) over the entire code range. Gain error can be trimmed to zero.

Accuracy: The difference (measured in dB) between the ideal transfer function and the actual transfer function as measured with the device after calibration for 0dB gain error.

Output Capacitance: Capacitance from I_{OUT} to ground.

Digital to Analog Glitch Impulse: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

Propagation Delay: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

ORDERING INFORMATION

		Temperature Range and Package		
Relative Accuracy T_{min} to T_{max}	**Gain Error T_A = +25°C**	**Plastic 0 to +70°C**	**Cerdip[1] −25°C to +85°C**	**Ceramic −55°C to +125°C**
±0.05dB	±0.1dB	AD7115KN	AD7115BQ	AD7115TD

NOTE:
[1]Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

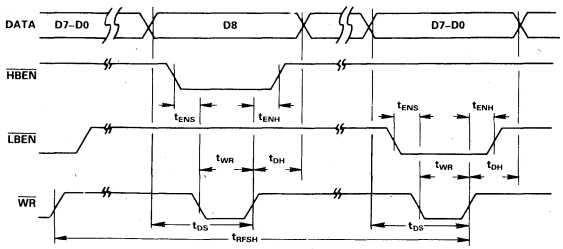
PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D18B)
Suffix Q: Cerdip – (Q18A)
Suffix N: Plastic DIP – (N18B)

[1]See Section 19 for package outline information.

CIRCUIT DESCRIPTION

The AD7115 consists of a 12-bit R-2R CMOS multiplying D/A converter with extensive digital logic. The logic translates the 2 1/2 digit BCD input code into a 12-bit word which is used to drive the D/A converter. Input data is loaded into the input latches under the control of $\overline{WR}$ (WRITE) and byte enable signals $\overline{LBEN}$ (LOW BYTE ENABLE) and $\overline{HBEN}$ (HIGH BYTE ENABLE). The rising edge of $\overline{WR}$ latches the input data. See Figure 1 for the data loading waveforms using an 8-bit data bus.



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. Data Loading Waveforms with 8-Bit Data Bus

In applications where the input data bus is at least nine bits wide $\overline{LBEN}$ and $\overline{HBEN}$ can be exercised together to load new data in one write operation. For 8-bit data bus applications two write operations are required to load completely new data into the AD7115. Table I shows the data loading truth table.

AD7115 Control Inputs			AD7115 Operation
$\overline{WR}$	$\overline{HBEN}$	$\overline{LBEN}$	
1	X	X	No Operation
X	1	1	No Operation
↓	0	1	Load HIGH Byte
↓	1	0	Load LOW Byte and Update DAC Register
↓	0	0	Load HIGH and LOW Byte and Update DAC Register

NOTES
1. X indicates "don't care" states.
2. ↓ indicates LOW to HIGH transition.

Table I. Data Loading Truth Table

Note that $\overline{HBEN}$ and $\overline{WR}$ simply load D8 data into the input latch whereas $\overline{LBEN}$ and $\overline{WR}$ load D7–D0 into the input latch and on the rising edge of $\overline{WR}$ updates the DAC register with the input latch contents (D8–D0) approximately 5μs later. Thus the proper sequence for loading completely new data into the AD7115 from an 8-bit bus is a high byte load followed by a low byte load. After any low byte load operation a minimum time is required for the data to propagate through the decoder before another low byte load operation is attempted. This time is the refresh time, t_{RFSH}, of Figure 1.

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7115 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, approximately doubles every 10°C – see Figure 12. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the current steering switches S1 to S12 and varies from about 40pF to 150pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Inc., Publication Number G479–15–8/78.

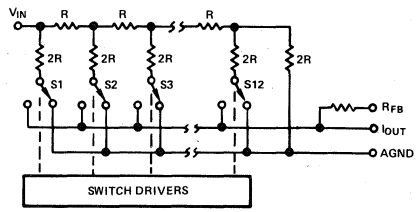
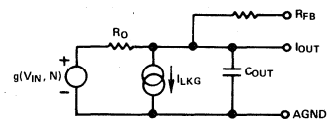


Figure 2. Simplified D/A Circuit of AD7115



g(V_{IN}, N) IS THE THEVENIN EQUIVALENT VOLTAGE GENERATOR DUE TO THE INPUT VOLTAGE V_{IN}, THE BCD ATTENUATION FACTOR N AND THE TRANSFER FUNCTION OF THE R 2R LADDER.

Figure 3. Equivalent Analog Output Circuit of AD7115

TYPICAL CIRCUIT CONFIGURATION

Figure 4 shows the AD7115 in a typical circuit configuration with an AD544. The transfer function for this circuit is given by:

$$V_O = -V_{IN}\ 10\ \exp\ -\left(\frac{0.1N}{20}\right)$$

Where 0.1 is the step size (resolution) in dB and N is the BCD input code, 0 to 199.

Note that a number of non-BCD codes exist which allow the user to mute the output, i.e., to achieve infinite attenuation. The basic mute code is XX0XX1111 for D8 to D0 respectively where X is a "don't care" input.

For example, 000001111 is one such suitable code.

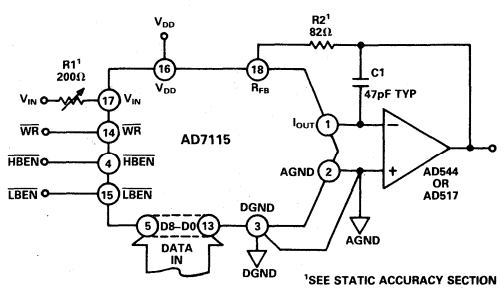


Figure 4. Typical Circuit Configuration

DYNAMIC PERFORMANCE

The dynamic performance of the AD7115 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 5 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7115 is to be achieved. Most application problems stem from poor layout, grounding errors, or inappropriate choice of amplifier.

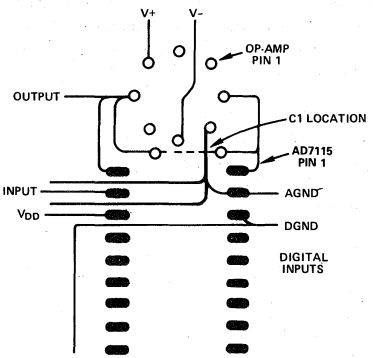


Figure 5. Suggested Layout for AD7115 and Op-Amp (Not to Scale)

It is recommended that when using the AD7115 with a high speed amplifier, a capacitor (C1) be connected in the feedback path as shown in Figure 4. This capacitor, which should be between 20pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 6 and 7 show the performance of the AD7115 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

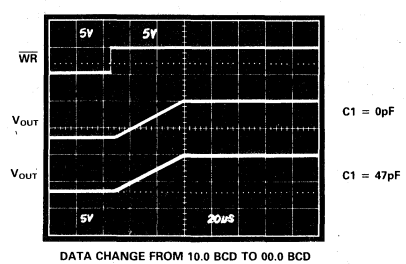


Figure 6. Response of AD7115 with AD517

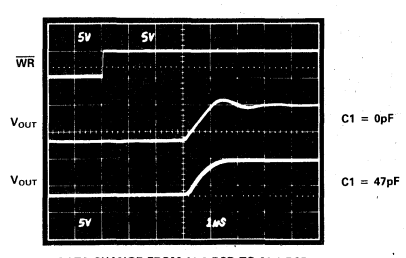


Figure 7. Response of AD7115 with AD544

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 7 and 11. In circuits when C1 is not included, the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7115.

Feedthrough and absolute accuracy are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7115 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 12.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7115 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

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STATIC ACCURACY PERFORMANCE

The choice of output amplifier will be strongly influenced by the absolute attenuation range over which the AD7115 is to operate, e.g., from 0 to −20dB, −20dB to −40dB, −40dB to −60dB, etc. To obtain optimum static performance from the device (especially at high absolute attenuation levels as shown for Figure 8), it is necessary to play close attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7115 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. It is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07) in dc applications. Amplifiers with higher offset voltage may cause audible "thumps" in ac applications due to dc output changes.

The AD7115 accuracy is specified and tested using only the internal feedback resistor. Any Gain Error (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7115 D/A converter circuit results in a constant attenuation error over the whole range. The AD7115 accuracy is specified relative to 0dB attenuation, hence "Gain" trim resistors – R1 and R2 in Figure 4 – can be used to adjust $V_{OUT} = V_{IN}$ precisely (i.e., 0dB attenuation) with input code 00.0BCD. The accuracy specifications of the AD7115 are not affected in any way by this gain trim procedure. For the AD7115K/B/T grades, suitable values for R1 and R2 of Figure 4 are R1 = 200Ω, R2 = 82Ω.

For additional information on gain error the reader is referred to Application Note "Gain Temperature Coefficient of CMOS Multiplying DACs" by Phil Burton available from Analog Devices, Inc., Publication Number E630–10–6/81.

0 TO 80dB ATTENUATOR WITH 0.1dB RESOLUTION

It is possible to extend the attenuation range beyond 20dB by using a precision attenuator or programmable gain amplifier in series with the AD7115 to provide a fixed amount of the total attenuation required. Figure 8 shows one possible configuration where a precision resistor divider string provides tapped outputs at signal levels 0dB, −20dB, −40dB and −60dB below the input signal level. The switch used, an AD7591DI, is a quad SPST switch with on-chip data latches. The output signal is buffered by an AD517 amplifier before being applied to the input pin, V_{IN}, of the AD7115. The accuracy and monotonicity range, particularly when switching from one 20dB segment to another is critically dependant on the resistor divider tolerances. Other error sources include leakage currents of the AD7591DI switches, signal source impedance, offset drift of the buffer AD517 amplifier and feed-through. These may be minimized by operating the circuit as close to +25°C as possible and by paying due attention to circuit layout and shielding.

Decoder Inputs D10	Decoder Inputs D9	Attenuation
0	0	0dB via S1
0	1	−20dB via S2
1	0	−40dB via S3
1	1	−60dB via S4

Table II. Decoder Truth Table for Figure 8

Note that the data inputs D10–D0 of Figure 8 may be driven by a three digit BCD coded word. The lower two digits and the "1" line of digit 3 control the AD7115. The "4" and "2" lines of digit 3 feed D10 and D9 respectively to control the precision divider. This arrangement allows the circuit attenuation to be programmed from 0dB to 79.9dB with 0.1dB resolution by a corresponding three digit BCD word.

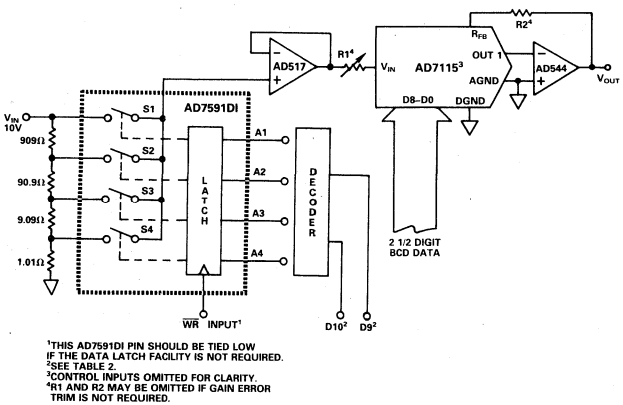

Figure 8. 0 to 80dB Attenuator with 0.1dB Resolution

THUMBWHEEL SWITCH ATTENUATOR

Figure 9 shows the AD7115 when used as a simple stand-alone thumbwheel switch attenuator. The BCD coded thumbwheel assembly applies BCD data to the AD7115 data inputs. Resistor R3 limits current if make before break switches are used. The facility to mute the output is provided by gates G1 to G6 and SPDT switch S1. A number of alternatives exist for generating the $\overline{WR}$ pulse required to load new data into the AD7115, a push-button switch S2 as shown in Figure 9 being the simplest. Alternatively the $\overline{WR}$ input can be driven by a simple oscillator to provide continuous $\overline{WR}$ pulses. Another option allows automatic loading of new data whenever any of the thumbwheel switches are moved. This requires switches which have guaranteed make before break action. Moving any thumbwheel switch to a new setting will cause a momentary pulse of current through R3 and produce a voltage glitch on the switch side of R3. This voltage glitch can be detected and stretched to provide a properly timed $\overline{WR}$ signal for the AD7115.

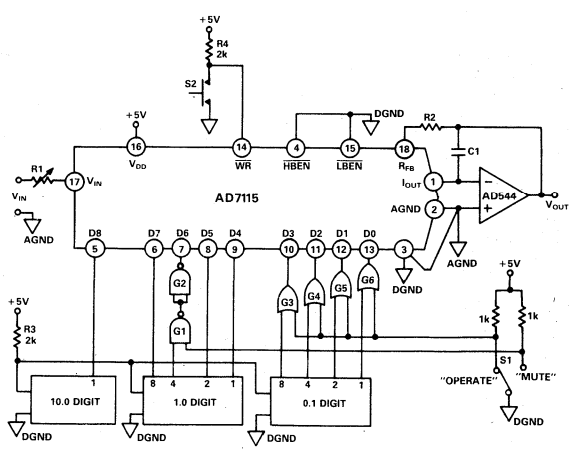

Figure 9. Thumbwheel Switch Attenuator

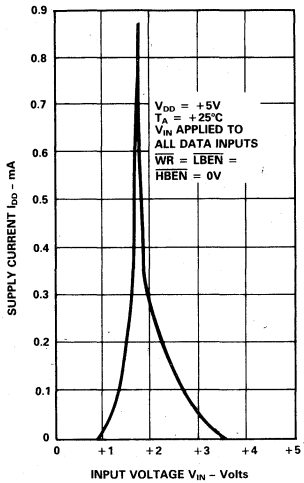

Figure 10. Typical Supply Current vs. Logic Input Level

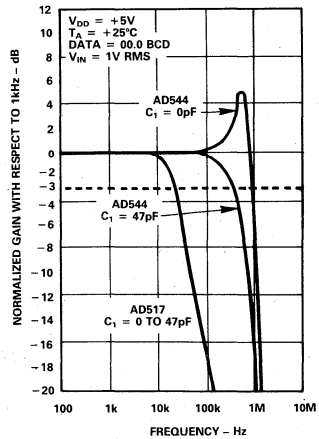

Figure 11. Frequency Response with AD544 and AD517 Amplifiers

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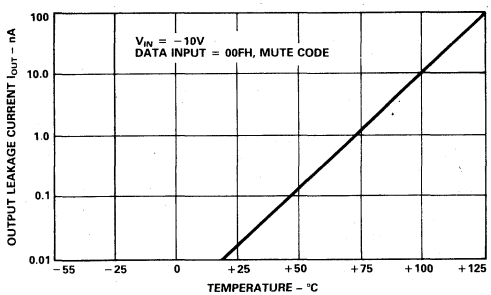


Figure 12. Typical Output Leakage Current vs. Temperature

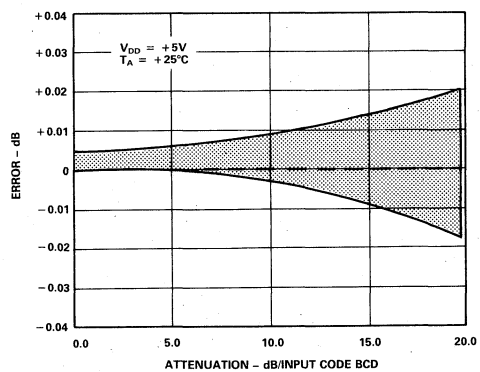


Figure 13. Typical Attenuation Error vs. Attenuation/Input Code

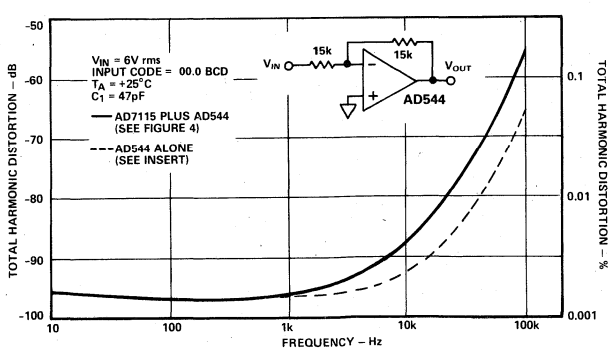


Figure 14. Typical Distortion vs. Frequency Using AD544 Amplifier

ANALOG DEVICES

LOGDAC™ CMOS Logarithmic D/A Converter

AD7118*

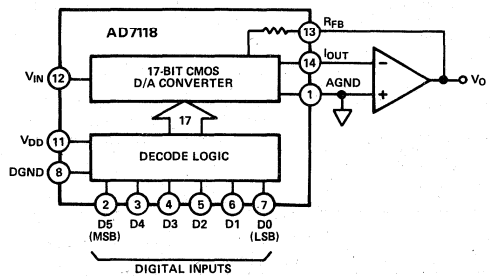
FEATURES

Dynamic Range 85.5dB
Resolution 1.5dB
Full ±25V Input Range Multiplying DAC
Full Military Temperature Range -55°C to +125°C
Low Distortion
Low Power Consumption
Latch Proof Operation (Schottky Diodes Not Required)
Single 5V to 15V Supply

APPLICATIONS

Digitally Controlled AGC Systems
Audio Attenuators
Wide Dynamic Range A/D Converters
Sonar Systems
Function Generators

AD7118 FUNCTIONAL BLOCK DIAGRAM



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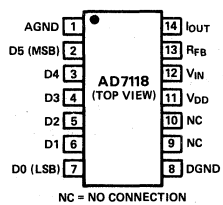
GENERAL DESCRIPTION

The AD7118 is a CMOS multiplying D/A converter which attenuates an analog input signal over the range 0 to -85.5dB in 1.5dB steps. The analog output is determined by a six bit attenuation code applied to the digital inputs. Operating frequency range of the device is from dc to several hundred kHz.

The device is manufacured using an advanced monolithic silicon gate thin-film on CMOS process and is packaged in a 14-pin dual-in-line package.

PIN CONFIGURATION (Not to Scale)



NC = NO CONNECTION

ORDERING INFORMATION

Specified Accuracy Range[1]	Temperature Range and Package		
	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0 to 42dB	AD7118KN	AD7118BD	AD7118TD
0 to 48dB	AD7118LN	AD7118CD	AD7118UD

NOTE
[1] All devices are guaranteed monotonic at +25°C (see spec).

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP – (D14B)
Suffix N: Plastic DIP – (N14B)

[1] See Section 19 for package outline information.

*Patent Pending.
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SPECIFICATIONS

(V_{DD} = +5V or +15V, V_{IN} = -10V dc, $V_{PIN\ 14}$ = V_{PIN1} = 0V, output amplifier AD544 except where stated)

PARAMETER		T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	TEST CONDITIONS/ COMMENTS
		V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
NOMINAL RESOLUTION		1.5	1.5	1.5	1.5	dB	
ACCURACY RELATIVE TO V_{IN}							
AD7118L/C/U							
0 to -30dB		±0.35	±0.35	±0.4	±0.4	dB max	Accuracy is measured using
-31.5 to -42dB		±0.7	±0.5	±0.8	±0.7	dB max	circuit of Figure 1 and includes
-43.5 to -48dB		±1.0	±0.7	±1.3	±1.0	dB max	any effects due to mismatch
AD7118K/B/T							between R_{FB} and the R-2R
0 to -30dB		±0.5	±0.5	±0.5	±0.5	dB max	ladder circuit.
-31.5 to -42dB		±0.75	±0.75	±1.0	±0.8	dB max	
MONOTONIC RANGE							
Nominal 1.5dB Steps	L/C/U Grade	Monotonic Over Full		0 to -72	0 to -72	dB	Digital Inputs 000000 to 110000
	K/B/T Grade	Code Range		0 to -66	0 to -66	dB	Digital Inputs 000000 to 101100
Nominal 3dB Steps	All Grades	Monotonic Over Full Code Range					
V_{IN} INPUT RESISTANCE	All Grades	9	9	9	9	kΩ min	
(PIN 12)	L/C/U Grade	17	17	17	17	kΩ max	
	K/B/T Grade	21	21	21	21	kΩ max	
R_{FB} INPUT RESISTANCE	All Grades	9.45	9.45	9.45	9.45	kΩ min	
(PIN 13)	L/C/U Grade	18	18	18	18	kΩ max	
	K/B/T Grade	22	22	22	22	kΩ max	
DIGITAL INPUTS							
Input High Voltage Requirements V_{IH}		3.0	13.5	3.0	13.5	V min	
Input Low Voltage Requirements V_{IL}		0.8	1.5	0.8	1.5	V max	
Input Leakage Current		±1	±1	±10	±10	μA max	Digital Inputs = V_{DD}
POWER SUPPLY							
V_{DD} for Specified Accuracy		5	—	5	—	V min	
		—	15	—	15	V max	
I_{DD}		0.5	1	1	2	mA max	Digital Inputs = 0V or V_{DD} (See Figure 7)

Specifications subject to change without notice.

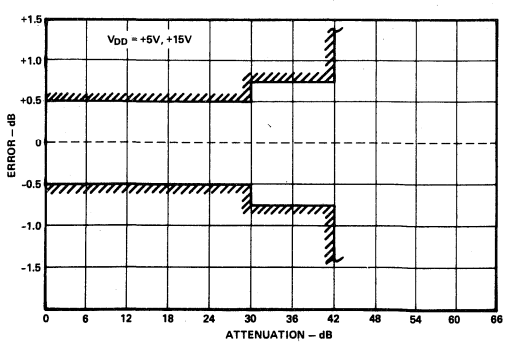
AC PERFORMANCE CHARACTERISTICS

These characteristics are included for design guidance only and are not subject to test.

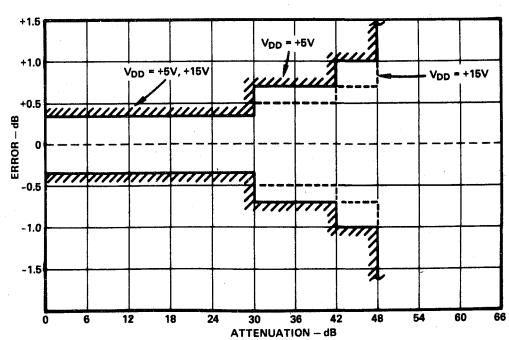
V_{DD} = +5V or +15V, V_{IN} = -10V except where stated, $V_{PIN\ 14}$ = $V_{PIN}1$ = 0V, output amplifier AD544 except where stated.

PARAMETER	T_A = +25°C		T_A = T_{min}, T_{max}		UNITS	
	V_{DD} = +5V	V_{DD} = +15V	V_{DD} = +5V	V_{DD} = +15V		
DC Supply Rejection, $\Delta Gain/\Delta V_{DD}$	0.01	0.005	0.01	0.005	dB per % max	ΔV_{DD} = ±10%, Input code = 100000
Propagation Delay	1.8	0.4	2.2	0.5	μs max	Full Scale Change
Digital to Analog Glitch Impulse	225	1200	—	—	nV secs typ	Measured with ADLH0032CG as output amplifier for input code transition 100000 to 000000. C1 of Figure 1 is 0pF.
Output Capacitance (Pin 14)	100	100	100	100	pF max	
Input Capacitance Pin 12 and Pin 13	7	7	7	7	pF max	
Feedthrough at 1kHz L/C/U Grade	-86	-86	-68	-68	dB max	Feedthrough is also deter-
K/B/T Grade	-80	-80	-63	-63	dB max	mined by circuit layout
Total Harmonic Distortion	-85	-85	-85	-85	dB typ	V_{IN} = 6V rms
Intermodulation Distortion	-79	-79	-79	-79	dB typ	per DIN 45403 Blatt 4
Output Noise Voltage Density	70	70	70	70	nV/$\sqrt{Hz}$ max	Includes AD544 amplifier noise
Digital Input Capacitance	7	7	7	7	pF max	

Specifications subject to change without notice.



Accuracy Specification for K/B/T Grade Devices at T_A = +25°C



Accuracy Specification for L/C/U Grade Devices at T_A = +25°C

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DD} (to DGND) . . . . . +17V
V_{IN} (to AGND) . . . . . ±35V
Digital Input Voltage to DGND . . . . . -0.3V to V_{DD}
Output Voltage (Pin 14) to AGND . . . . . -0.3V to V_{DD}
AGND to DGND . . . . . 0 to V_{DD}
DGND to AGND . . . . . 0 to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C 670mW
Derates Above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C 450mW
Derates Above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (KN, LN Versions) . . . . . 0 to +70°C
Industrial Ceramic (BQ, CQ Versions) . . . . -25°C to +85°C
Extended Ceramic (TD, UD Versions) . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RESOLUTION: Nominal change in attenuation when moving between two adjacent binary codes.

MONOTONICITY: The device is monotonic if the analog output decreases (or remains constant) as the digital code increases.

FEEDTHROUGH ERROR: That portion of the input signal which reaches the output when all digital inputs are high. See section on Applications.

OUTPUT LEAKAGE CURRENT: Current which appears on the I_{OUT} terminal with all digital inputs high.

TOTAL HARMONIC DISTORTION: Is a measure of the harmonics introduced by the circuit when a pure sinusoid is applied to the input. It is expressed as the harmonic energy divided by the fundamental energy at the output.

ACCURACY: Is the difference (measured in dB) between the ideal transfer function as listed in Table 1 and the actual transfer function as measured with the device.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} to ground.

DIGITAL TO ANALOG GLITCH IMPULSE: The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-Secs or nV-Secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{IN} = AGND.

PROPAGATION DELAY: This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

INTERMODULATION DISTORTION: Is a measure of the interaction which takes place within the circuit between two sinusoids applied simultaneously to the input.

The reader is referred to Hewlett Packard Application Note 192 for further information.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7118 consists of a 17-bit R-2R CMOS multiplying D/A converter with extensive digital input logic. The logic translates the 6-bit binary input into a 17-bit word which is used to drive the D/A converter. Table I gives the nominal output voltages (and levels relative to 0dB = 10V) for all possible input codes. The transfer function for the circuit of Figure 1 is given by:

$$V_O = -V_{IN}\ 10 \exp - \left\{\frac{1.5N}{20}\right\}$$

$$\text{or } \left|\frac{V_O}{V_{IN}}\right|_{dB} = -1.5N$$

where N is the binary input for values 0 to 57. For $60 \leqslant N \leqslant 63$ the output is zero. See note 3 at bottom of Table 1.

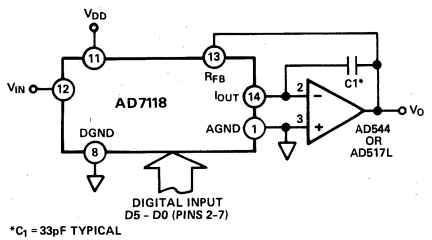


Figure 1. Typical Circuit Configuration

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows a simplified circuit of the D/A converter section of the AD7118 and Figure 3 gives an approximate equivalent circuit.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and as with most semiconductor devices, roughly doubles every 10°C—see Figure 10. The resistor R_O as shown in Figure 3 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 12kΩ. C_{OUT} is the capacitance due to the N channel switches and varies from about 50pF to 80pF depending upon the digital input. For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" which is available from Analog Devices, Publication Number G479—15—8/78.

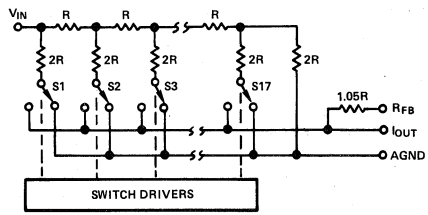
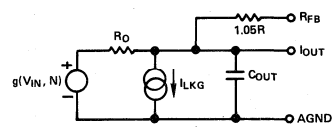


Figure 2. Simplified D/A Circuit of AD7118



g(VIN, N) IS THE THEVENIN EQUIVALENT VOLTAGE GENERATOR DUE TO THE INPUT VOLTAGE VIN, THE BINARY ATTENUATION FACTOR N AND THE TRANSFER FUNCTION OF THE R-2R LADDER.

Figure 3. Equivalent Analog Output Circuit of AD7118

N	Digital Input D5 D0	Attenuation dB	V_{OUT}[1]	N	Digital Input	Attenuation	V_{OUT}[1]
0	00 00 00	0.0	10.00	31	01 11 11	46.5	0.0473
1	00 00 01	1.5	8.414	32	10 00 00	48.0	0.0398
2	00 00 10	3.0	7.079	33	10 00 01	49.5	0.0335
3	00 00 11	4.5	5.957	34	10 00 10	51.0	0.0282
4	00 01 00	6.0	5.012	35	10 00 11	52.5	0.0237
5	00 01 01	7.5	4.217	36	10 01 00	54.0	0.0200
6	00 01 10	9.0	3.548	37	10 01 01	55.5	0.0168
7	00 01 11	10.5	2.985	38	10 01 10	57.0	0.0141
8	00 10 00	12.0	2.512	39	10 01 11	58.5	0.0119
9	00 10 01	13.5	2.113	40	10 10 00	60.0	0.0100
10	00 10 10	15.0	1.778	41	10 10 01	61.5	0.00841
11	00 10 11	16.5	1.496	42	10 10 10	63.0	0.00708
12	00 11 00	18.0	1.259	43	10 10 11	64.5	0.00596
13	00 11 01	19.5	1.059	44	10 11 00	66.0	0.00501
14	00 11 10	21.0	0.891	45	10 11 01	67.5	0.00422
15	00 11 11	22.5	0.750	46	10 11 10	69.0	0.00355
16	01 00 00	24.0	0.631	47	10 11 11	70.5	0.00299
17	01 00 01	25.5	0.531	48	11 00 00	72.0	0.00251
18	01 00 10	27.0	0.447	49	11 00 01	73.5	0.00211
19	01 00 11	28.5	0.376	50	11 00 10	75.0	0.00178
20	01 01 00	30.0	0.316	51	11 00 11	76.5	0.00150
21	01 01 01	31.5	0.266	52	11 01 00	78.0	0.00126
22	01 01 10	33.0	0.224	53	11 01 01	79.5	0.00106
23	01 01 11	34.5	0.188	54	11 01 10	81.0	0.000891
24	01 10 00	36.0	0.158	55	11 01 11	82.5	0.000750
25	01 10 01	37.5	0.133	56	11 10 00	84.0	0.000631
26	01 10 10	39.0	0.112	57	11 10 01	85.5	0.000531
27	01 10 11	40.5	0.0944	58	11 10 10	87.0	0.000447
28	01 11 00	42.0	0.0794	59	11 10 11	88.5	0.000376
29	01 11 01	43.5	0.0668	60	11 11 XX[2]	∞	
30	01 11 10	45.0	0.0562				

NOTES
[1] V_{IN} = -10V dc
[2] X = 1 or 0. Output is fully muted for $N \geqslant 60$
[3] Monotonic operation is not guaranteed for N = 58, 59

Table I. Ideal Attenuation vs. Input Code

DYNAMIC PERFORMANCE

The dynamic performance of the AD7118 will depend upon the gain and phase characteristics of the output amplifier, together with the optimum choice of PC board layout and decoupling components. Figure 4 shows a printed circuit layout which minimizes feedthrough from V_{IN} to the output in multiplying applications. Circuit layout is most important if the optimum performance of the AD7118 is to be achieved. Most application problems stem from either poor layout, grounding errors, or inappropriate choice of amplifier.

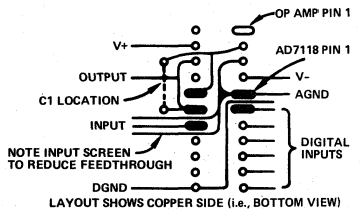


Figure 4. Suggested Layout for AD7118 and Op Amp

It is recommended that when using the AD7118 with a high speed amplifier, a capacitor C1 be connected in the feedback path as shown in Figure 1. This capacitor, which should be between 30pF and 50pF, compensates for the phase lag introduced by the output capacitance of the D/A converter. Figures 5 and 6 show the performance of the AD7118 using the AD517, a fully compensated high gain superbeta amplifier, and the AD544, a fast FET input amplifier. The performance without C1 is shown in the middle trace and the response with C1 in circuit is shown in the bottom trace.

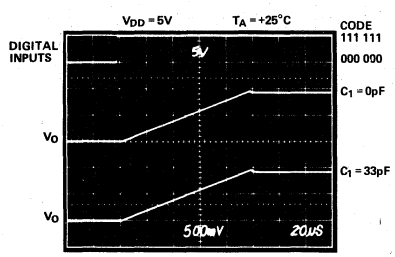


Figure 5. Response of AD7118 with AD517L

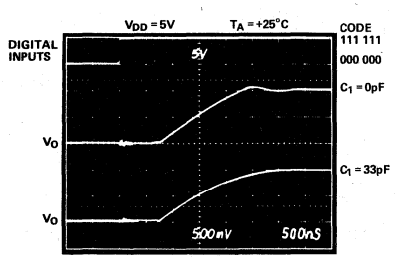


Figure 6. Response of AD7118 with AD544S

In conventional CMOS D/A converter design parasitic capacitance in the N-channel D/A converter switches can give rise to glitches on the D/A converter output. These glitches result from digital feedthrough. The AD7118 has been designed to minimize these glitches as much as possible. It is recommended that for minimum glitch energy the AD7118 be operated with V_{DD} = 5V. This will reduce the available energy for coupling across the parasitic capacitance. It should be noted that the accuracy of the AD7118 improves as V_{DD} is increased (see Figure 8) but the device maintains monotonic behavior to at least -66dB in the range $5 \leqslant V_{DD} \leqslant 15$ volts.

For operation beyond 250kHz, capacitor C1 may be reduced in value. This gives an increase in bandwidth at the expense of a poorer transient response as shown in Figures 6 and 11. In circuits where C1 is not included the high frequency roll-off point is primarily determined by the characteristics of the output amplifier and not the AD7118.

Feedthrough and absolute accuracy for attenuation levels beyond 42dB are sensitive to output leakage current effects. For this reason it is recommended that the operating temperature of the AD7118 be kept as close to 25°C as is practically possible, particularly where the device's performance at high attenuation levels is important. A typical plot of leakage current vs. temperature is shown in Figure 10.

Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects between analog input and output. The user is cautioned to ensure that the manufacturing process for circuits using the AD7118 does not allow such films to form. Otherwise the feedthrough, accuracy and maximum usable range will be affected.

9

STATIC ACCURACY PERFORMANCE

The D/A converter section of the AD7118 consists of a 17-bit R-2R type converter. To obtain optimum static performance at this level of resolution it is necessary to pay great attention to amplifier selection, circuit grounding, etc.

Amplifier input bias current results in a dc offset at the output of the amplifier due to the current flowing through the feedback resistor R_{FB}. It is recommended that an amplifier with an input bias current of less than 10nA be used (e.g., AD517 or AD544) to minimize this offset.

Another error arises from the output amplifier's input offset voltage. The amplifier is operated with a fixed feedback resistance, but the equivalent source impedance (the AD7118 output impedance) varies as a function of attenuation level. This has the effect of varying the "noise" gain of the amplifier, thus creating a varying error due to amplifier offset voltage. To achieve an output offset error less than one half the smallest step size, it is recommended that an amplifier with less than 50µV of input offset be used (such as the AD517 or AD OP-07).

If dc accuracy is not critical in the application, it should be noted that amplifiers with offset voltage up to approximately 2 millivolts can be used. Amplifiers with higher offset voltage may cause audible "thumps" due to dc output changes.

The AD7118 accuracy is specified and tested using only the internal feedback resistor. It is not recommended that "gain" trim resistors be used with the AD7118 because the internal logic of the circuit executes a proprietary algorithm which approximates a logarithmic curve with a binary D/A converter: as a result no single point on the attenuator transfer function can be guaranteed to lie exactly on the theoretical curve. Any "gain-error" (i.e., mismatch of R_{FB} to the R-2R ladder) that may exist in the AD7118 D/A converter circuit results in a constant attenuation error over the whole range. Since the gain-error of CMOS multiplying D/A converters is normally less than 1%, the accuracy error contribution due to "gain-error" effects is normally less than 0.09dB.

Typical Performance Characteristics

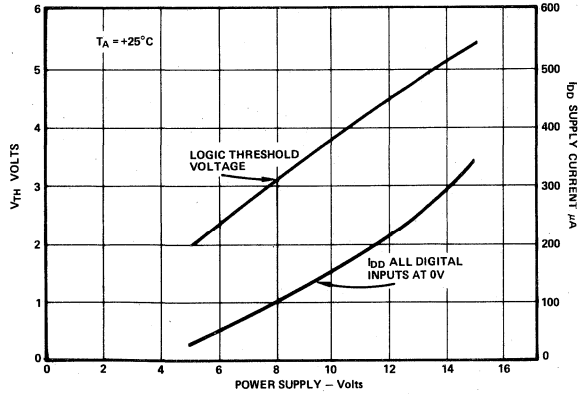


Figure 7. Digital Threshold & Power Supply Current vs Power Supply

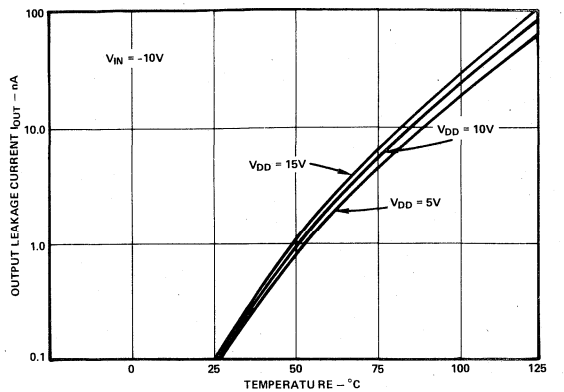


Figure 10. Output Leakage Current vs Temperature at V_{DD} = 5, 10 and 15 Volts

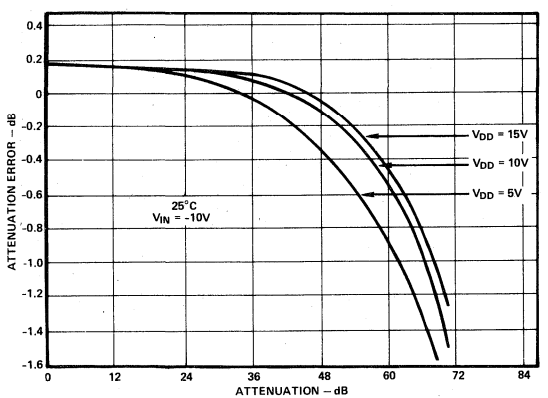


Figure 8. DC Attenuation Error vs. Attenuation & V_{DD}

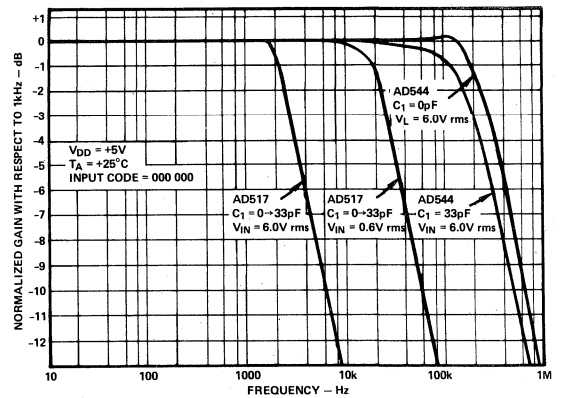


Figure 11. Frequency Response with AD544 and AD517 Amplifiers

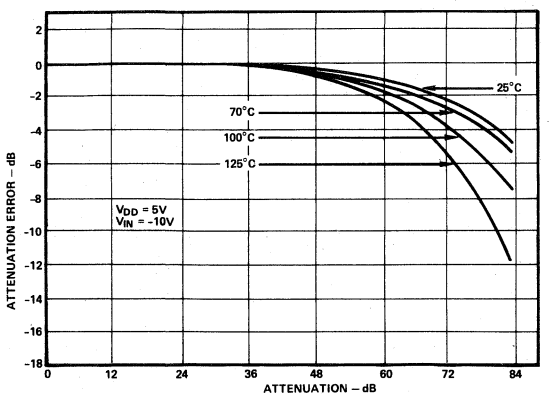


Figure 9. DC Attenuation Error vs. Attenuation & Temperature

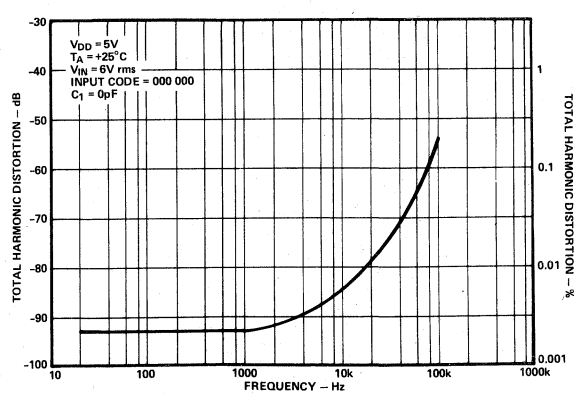


Figure 12. Distortion vs. Frequency Using AD544 Amplifier

ANALOG DEVICES

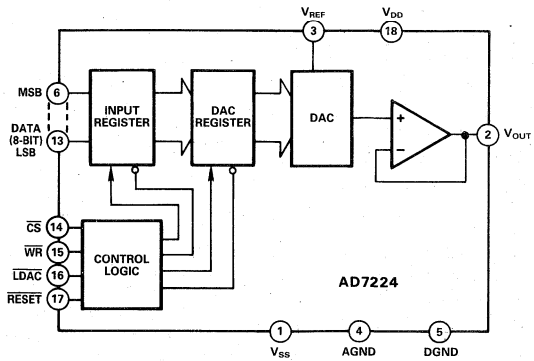
LC²MOS Double Buffered 8-Bit DAC

AD7224

FEATURES
8-Bit DAC with Output Amplifier
Full Double Buffered Logic
Microprocessor Compatible
TTL/CMOS Compatible
No User Trim
0.3″ Wide 18-Pin DIP
Single Supply Operation Possible

APPLICATIONS
Process Control
Automatic Test Equipment
Digital Control of Gain/Attenuation

AD7224 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The AD7224 is a precision 8-bit voltage-output digital-to-analog converter, with output amplifier and full double buffered interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

The internal two-stage input storage registers consists of two, 8-bit registers–an input register and a DAC register. The DAC register is used to retain the DAC data while the input register is being updated. Only the data held in the DAC register determines the analog output of the converter. Both registers may be made transparent under control of the three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. The contents of both registers are reset by a "LOW" pulse on the $\overline{RESET}$ line. With both registers transparent the $\overline{RESET}$ line functions like a zero override. All logic inputs are TTL and CMOS (5V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

The output buffer amplifier is capable of developing +10V across a 2kΩ load. The amplifier offset is laser trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. Single Supply Operation
   The voltage-mode configuration of the DAC allows the AD7224 to be operated from a single power supply rail.
2. Versatile Interfacing Structure
   The AD7224 features full double-buffered interface logic with a zero override function which allows for versatile interfacing to microprocessors. All control signals are level triggered.
3. Small Size
   The AD7224 contains one D/A converter, an output buffer amplifier and double buffered interface logic on a small 0.3″ wide 18-pin DIP, allowing reduction in board space requirements and complexity.

ORDERING INFORMATION[1]

Total Unadjusted Error	Plastic (N18B)	Cerdip[2] (Q18B)	Side Brazed Ceramic (D18B)
T_{min} to T_{max}	0 to +70°C	−25°C to +85°C	−55°C to +125°C
±2LSB	AD7224KN	AD7224BQ	AD7224TD
±1LSB	AD7224LN	AD7224CQ	AD7224UD

NOTES
[1]See Section 19 for package outline information.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

DUAL SUPPLY SPECIFICATIONS

(V_{DD} = +11.4V to +16.5V; V_{SS} = −5V ±25%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} − 4V)[1] unless otherwise stated).
All specifications T_{min} to T_{max} unless otherwise stated

Parameter	AD7224K,B,T[2]	AD7224L,C,U[2]	Units	Test Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15V ±5%, V_{REF} = +10V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	LSB max	Guaranteed Monotonic
Full Scale Error	±1 1/2	±1/2	LSB max	
Full Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	±10	mV max	
Zero Code Error Temperature Coefficient	±50	±30	µV/°C typ	
REFERENCE INPUT				
Voltage Range	2 to (V_{DD} − 4)	2 to (V_{DD} − 4)	V_{min} to V_{max}	
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	50	50	pF min	Occurs when DAC is loaded with all 0's
	100	100	pF max	Occurs when DAC is loaded with all 1's
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2.5	2.5	V/µs min	
Voltage Output Settling Time[4]				
Positive Full Scale Change	5	5	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Negative Full Scale Change	7	7	µs max	V_{REF} = +10V; Settling Time to ±1/2LSB
Digital Feedthrough	50	50	nV sec typ	
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLY				
V_{DD} Range	11.4/16.5	11.4/16.5	V min/V max	For Specified Performance
I_{DD}	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	3	3	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows: AD7224KN, LN 0 to +70°C
AD7224BQ, CQ −25°C to +85°C
AD7224TD, UD −55°C to +125°C
[3]Guaranteed by design. Not production tested.
[4]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

SINGLE SUPPLY SPECIFICATIONS

(V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V unless otherwise stated.)
All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7224K,B,T[1]	AD7224L,C,U[1]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[2]	50	50	pF min	Occurs when DAC is loaded with all 0's
	100	100	pF max	Occurs when DAC is loaded with all 1's
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[3]	2	2	V/μs min	
Voltage Output Settling Time[3]				
Positive Full Scale Change	5	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	20	μs max	Settling Time to ± 1/2LSB
Digital Feedthrough	50	50	nV sec typ	V_{REF} = 0V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10V
POWER SUPPLY				
V_{DD} Range	14.25/15.75	14.25/15.75	V min/V max	For Specified Performance
I_{DD}	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}

NOTES

[1]Temperature ranges are as follows:

AD7224KN, LN	0 to +70°C
AD7224BQ, CQ	−25°C to +85°C
AD7224TD, UD	−55°C to +125°C

[2]Guaranteed by design. Not production tested.
[3]Sample tested at 25°C to ensure compliance.
Specifications subject to change without notice.

9

Applying the 7224

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7224, with the output voltage having the same positive polarity as V_{REF}. The AD7224 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 1. The voltage at V_{REF} must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table I.

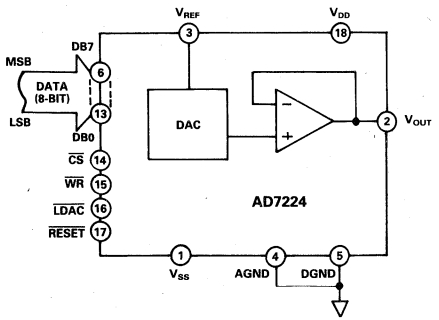


Figure 1. Unipolar Output Circuit

DAC Register Contents MSB	LSB	Analog Output, V_{OUT}
1111	1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000	0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000	0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111	1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000	0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table I. Unipolar Code Table

BIPOLAR OUTPUT OPERATION

The AD7224 can be configured to provide bipolar output operation using one external amplifier and two resistors. Figure 2 shows a circuit used to implement offset binary coding. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in the DAC register.

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature. Once again the AD7224 can be operated in single supply or from positive/negative supplies. Table II shows the digital code versus output voltage relationship for the circuit of Figure 2 with R1 = R2.

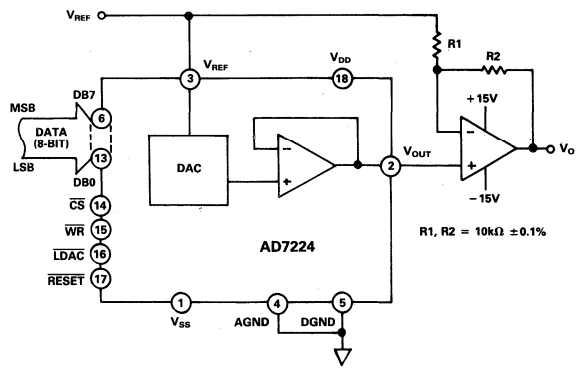


Figure 2. Bipolar Output Circuit

DAC Register Contents MSB	LSB	Analog Output, V_{OUT}
1111	1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000	0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000	0000	0V
0111	1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000	0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000	0000	$V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

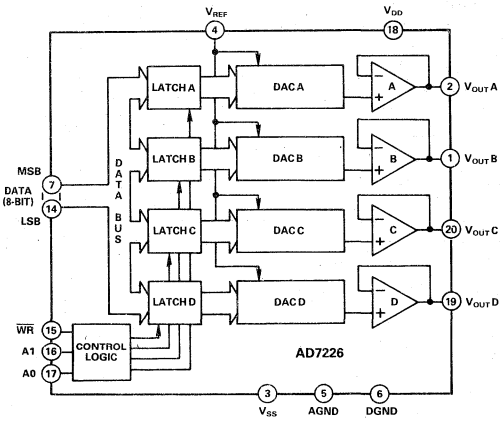
Table II. Bipolar (Offset Binary) Code Table

LC²MOS
Quad 8-Bit D/A Converter
AD7226

FEATURES
- Four 8-Bit DACs with Output Amplifiers
- 0.3" Wide, 20-Pin DIP
- Microprocessor Compatible
- TTL/CMOS Compatible
- No User Trims
- Single Supply Operation Possible

APPLICATIONS
- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters
  e.g., Gain/Offset

AD7226 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7226 contains four 8-bit voltage-output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the four D/A converters. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Control inputs A0 and A1 determine which DAC is loaded when $\overline{WR}$ goes low. The control logic is speed-compatible with most 8-bit microprocessors.

Each D/A converter includes an output buffer amplifier capable of driving up to 5mA of output current. The amplifiers' offsets are laser-trimmed during manufacture, thereby eliminating any requirement for offset nulling.

Specified performance is guaranteed for input reference voltages from +2V to +12.5V with dual supplies. The part is also specified for single supply operation at a reference of +10V.

The AD7226 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC^2MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC-to-DAC Matching:
   Since all four DACs are fabricated on the same chip at the same time, precise matching and tracking between the DACs is inherent.
2. Single Supply Operation:
   The voltage mode configuration of the DACs allows the AD7226 to be operated from a single power supply rail.
3. Microprocessor Compatibility:
   The AD7226 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered.
4. Small Size:
   Combining four DACs and four op-amps plus interface logic into a small, 0.3" wide, 20-pin DIP allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all the analog inputs and outputs at one end of the package and all the digital inputs at the other.

DUAL SUPPLY SPECIFICATIONS

(V_{DD} = 11.4V to 16.5V; V_{SS} = −5V ±10%; AGND = DGND = 0V; V_{REF} = 2V to (V_{DD} −4V)[1] unless otherwise stated). All specifications T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	AD7226K,B,T[2]	UNITS	CONDITIONS/COMMENTS
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error[3]	±2	LSB max	V_{DD} = +15V ± 5%, V_{REF} = +10V
Relative Accuracy[3]	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	Guaranteed Monotonic
Full Scale Error[3]	±1 1/2	LSB max	
Full Scale Temperature Coefficient	±20	ppm/°C typ	V_{DD} = 14V to 16.5V, V_{REF} = +10V
Zero Code Error	±30	mV max	
Zero Code Error Temperature Coefficient	±50	µV/°C typ	
REFERENCE INPUT			
Voltage Range	2 to (V_{DD} −4)	V_{MIN} to V_{MAX}	
Input Resistance	2	kΩ min	
Input Capacitance[4]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	µA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[5]	2.5	V/µs min	
Voltage Output Settling Time[5]			
Positive Full Scale Change	5	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Negative Full Scale Change	7	µs max	V_{REF} = +10V; Settling Time to ± 1/2LSB
Digital Crosstalk[3]	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	11.4/16.5	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	12[6]	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
I_{SS}	9[6]	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}.
SWITCHING CHARACTERISTICS[5]			
Address to Write Setup Time, t_{AS}			
@25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7226KN 0 to +70°C
AD7226BQ −25°C to +85°C
AD7226TD −55°C to +125°C
[3]See Terminology.
[4]Guaranteed by design. Not production tested.
[5]Sample Tested at 25°C to ensure compliance.
[6]On T grade part, I_{DD} is 13mA and I_{SS} is 11mA.
[7]On T grade part, I_{DD} is 13mA.
Specifications subject to change without notice.

SINGLE SUPPLY SPECIFICATIONS

(V_{DD} = +15V ±5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V[1] unless otherwise stated). All specifications T_{MIN} to T_{MAX} unless otherwise noted.

PARAMETER	AD7226K,B,T[2]	UNITS	CONDITIONS/COMMENTS
STATIC PERFORMANCE			
Resolution	8	Bits	
Total Unadjusted Error[3]	±2	LSB max	
Differential Nonlinearity[3]	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT			
Input Resistance	2	kΩ min	
Input Capacitance[4]	65	pF min	Occurs when each DAC loaded with all 0's.
	300	pF max	Occurs when each DAC loaded with all 1's.
DIGITAL INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
Input Low Voltage, V_{INL}	0.8	V max	
Input Leakage Current	±1	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance	8	pF max	
Input Coding	Binary		
DYNAMIC PERFORMANCE			
Voltage Output Slew Rate[5]	2	V/μs min	
Voltage Output Settling Time[5]			
Positive Full Scale Change	5	μs max	Settling Time to ± 1/2LSB
Negative Full Scale Change	20	μs max	Settling Time to ± 1/2LSB
Digital Crosstalk[3]	50	nV secs typ	
Minimum Load Resistance	2	kΩ min	V_{OUT} = +10V
POWER SUPPLIES			
V_{DD} Range	14.25 to 15.75	V_{MIN}/V_{MAX}	For Specified Performance
I_{DD}	12[7]	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[5]			
Address to Write Setup Time, t_{AS}			
@25°C	0	ns min	
T_{MIN} to T_{MAX}	0	ns min	
Address to Write Hold Time, t_{AH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Data Valid to Write Setup Time, t_{DS}			
@25°C	90	ns min	
T_{MIN} to T_{MAX}	100	ns min	
Data Valid to Write Hold Time, t_{DH}			
@25°C	10	ns min	
T_{MIN} to T_{MAX}	10	ns min	
Write Pulse Width, t_{WR}			
@25°C	150	ns min	
T_{MIN} to T_{MAX}	200	ns min	

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{SS} to AGND	−7V, V_{DD}
V_{SS} to DGND	−7V, V_{DD}
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND[1]	V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C	500mW
Derates above 75°C by	2.0mW/°C
Operating Temperature	
Commerical	0 to +70°C
Industrial	−25°C to +85°C
Extended	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

NOTES
[1]Outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60mA.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

TOTAL UNADJUSTED ERROR
This is a comprehensive specification which includes full scale error, relative accuracy and zero code error. Absolute full scale is V_{REF} −1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the offset will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the offset, will also vary in terms of LSB's over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10V.

RELATIVE ACCURACY
Relative Accuracy or end-point nonlinearity, is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after allowing for zero and full scale and is normally expressed in LSB's or as a percentage of full scale reading.

DIFFERENTIAL NONLINEARITY
Differential Nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

DIGITAL CROSSTALK
The glitch impulse transferred to the output of one converter due to a change in the digital input code to another of the converters. It is specified in nV secs and is measured at V_{REF}=0V.

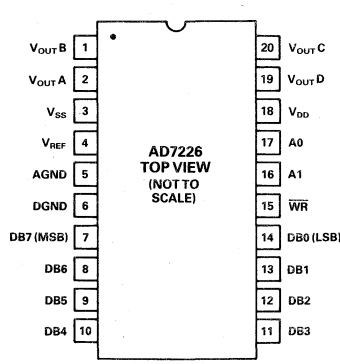
FULL SCALE ERROR
Full Scale Error is defined as:
Measured Value – Zero Code Error – Ideal Value.

ORDERING INFORMATION[1]

Total Unadjusted Error	Plastic (N20B)	Cerdip[2] (Q20B)	Side Brazed Ceramic (D20B)
$T_A = T_{min}$ to T_{max} ±2 LSB	0 to +70°C AD7226KN	−25°C to +85°C AD7226BQ	−55°C to +125°C AD7226TD

NOTES
[1]See Section 19 for package outline information.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

PIN CONFIGURATION



CIRCUIT INFORMATION

D/A SECTION

The AD7226 contains four, identical, 8-bit, voltage-mode digital-to-analog converters. The output voltages from the converters have the same polarity as the reference voltage allowing single supply operation. A novel DAC switch pair arrangement on the AD7226 allows a reference voltage range from +2V to +12.5V.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for one channel is shown in Figure 1. Note that V_{REF} (pin 4) and AGND (pin 5) are common to all four DACs.

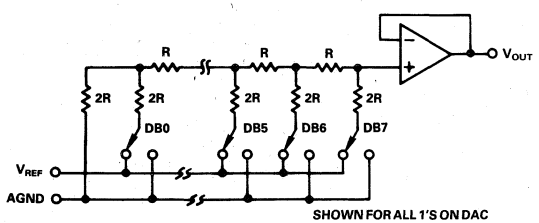


Figure 1. D/A Simplified Circuit Diagram

The input impedance at the V_{REF} pin of the AD7226 is the parallel combination of the four individual DAC reference input impedances. It is code dependent and can vary from 2kΩ to infinity. The lowest input impedance (i.e., 2kΩ) occurs when all four DACs are loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminal is also code dependent and typically varies from 100pF to 250pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X V_{REF}$$

where D_X is a fractional representation of the digital input code and can vary from 0 to 255/256.

The source impedance is the output resistance of the buffer amplifier.

OP-AMP SECTION

Each voltage-mode D/A converter output is buffered by a unity gain, noninverting CMOS amplifier. This buffer amplifier is capable of developing +10V across a 2kΩ load and can drive capacitive loads of 3300pF. The output stage of this amplifier consists of a bipolar transistor from the V_{DD} line and a current load to V_{SS}, the negative supply for the output amplifiers. This output stage is shown in Figure 2.

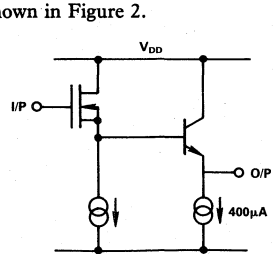


Figure 2. Amplifier Output Stage

The NPN transistor supplies the required output current drive (up to 5mA). The current load consists of NMOS transistors which normally act as a constant current sink of 400μA to V_{SS}, giving each output a current sink capability of approximately 400μA if required.

The AD7226 can be operated single supply or dual supply resulting in different performance in some parameters from the output amplifiers.

In single supply operation (V_{SS} = 0V = AGND), with the output approaching AGND (i.e., digital code approaching all 0's) the current load ceases to act as a current sink and begins to act as a resistive load of approximately 2kΩ to AGND. This occurs as the NMOS transistors come out of saturation. This means that, in single supply operation, the sink capability of the amplifiers is reduced when the output voltage is at or near AGND. A typical plot of the variation of current sink capability with output voltage is shown in Figure 3.

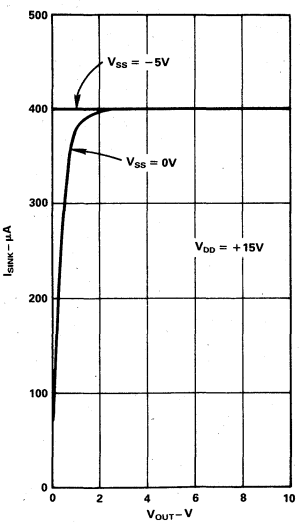


Figure 3. Variation of I_{SINK} with V_{OUT}

If the full sink capability is required with output voltages at or near AGND (=0V), then V_{SS} can be brought below 0V by 5V and thereby maintain the 400μA current sink as indicated in Figure 3. Biasing V_{SS} below 0V also gives additional headroom in the output amplifier which allows for better zero code error performance on each output. Also improved is the slew-rate and the negative-going settling-time of the amplifiers (discussed later).

Each amplifier offset is laser trimmed during manufacture to eliminate any requirement for offset nulling.

DIGITAL SECTION

The digital inputs of the AD7226 are both TTL and CMOS (5V) compatible from V_{DD} = +11.4V to +16.5V. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from DGND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

Address lines A0 and A1 select which DAC will accept data from the input port. Table I shows the selection table for the four DACs with Figure 4 showing the input control logic. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent and its output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of $\overline{WR}$. While $\overline{WR}$ is high the analog outputs remain at the value corresponding to the data held in their respective latches.

AD7226 Control Inputs $\overline{WR}$	A1	A0	AD7226 Operation
H	X	X	No Operation Device Not Selected
↓	L	L	DAC A Transparent
↑	L	L	DAC A Latched
↓	L	H	DAC B Transparent
↑	L	H	DAC B Latched
↓	H	L	DAC C Transparent
↑	H	L	DAC C Latched
↓	H	H	DAC D Transparent
↑	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

Table I. AD7226 Truth Table

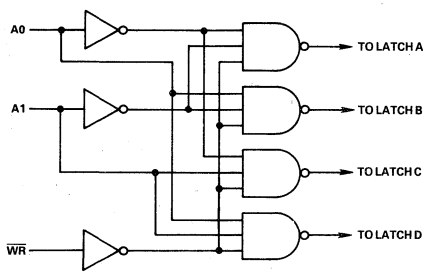
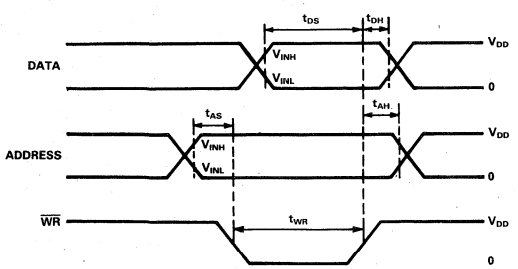


Figure 4. Input Control Logic



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% of V_{DD}. $t_r = t_f = 20ns$ OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$
3. SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW, THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS.

Figure 5. Write Cycle Timing Diagram

Typical Performance Characteristics

($T_A = 25°C$, $V_{DD} = +15V$, $V_{SS} = -5V$)

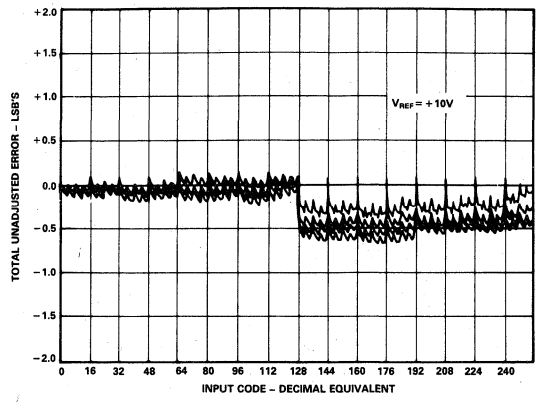


Figure 6. Channel-to-Channel Matching

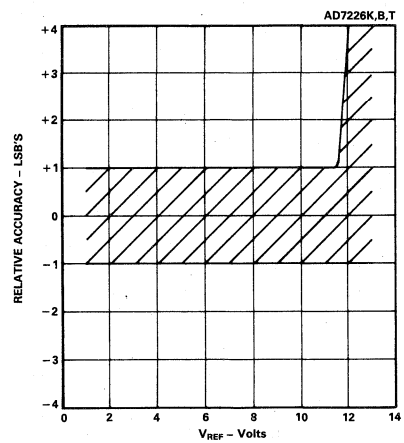


Figure 7. Relative Accuracy vs. V_{REF}

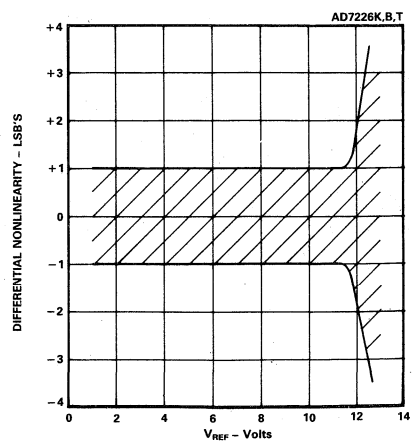


Figure 8. Differential Nonlinearity vs. V_{REF}

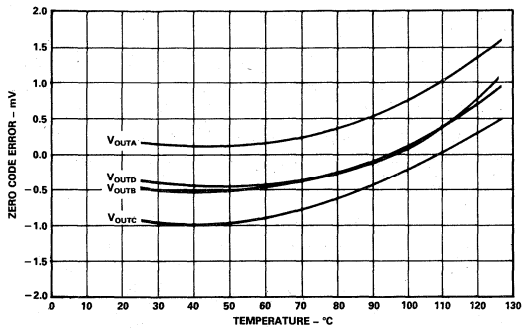


Figure 9. Zero Code Error vs. Temperature

SPECIFICATION RANGES

In order for the DACs to operate to their specifications, the reference voltage must be at least 4V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

The AD7226 is specified to operate over a V_{DD} range from +12V ±5% to +15V ±10% (i.e., from 11.4V to +16.5V) with a V_{SS} of −5V ±10%. Operation is also specified for a single +15V ±5% V_{DD} supply. Applying a V_{SS} of −5V results in improved zero code error, improved output sink capability with outputs near AGND, and improved negative-going settling-time.

Performance is specified over a wide range of reference voltages from 2V to (V_{DD} −4V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5V bandgap reference and the AD584, a precision +10V reference. Note that in order to achieve an output voltage range of 0V to +10V, a nominal +15V ±5% power supply voltage is required by the AD7226.

SETTLING TIME

The output stage of the buffer amplifiers consists of a bipolar NPN transistor from the V_{DD} line and a constant current load to V_{SS}. V_{SS} is the negative power supply for the output buffer amplifiers. As mentioned in the op-amp section, in single supply operation the NMOS transistor will come out of saturation as the output voltage approaches AGND and will act as a resistive load of approximately 2kΩ to AGND. As a result, the settling-time for negative-going signals approaching AGND in single supply operation will be longer than for dual supply operation where the current load of 400μA is maintained all the way down to AGND. Positive-going settling-time is not affected by V_{SS}.

The settling-time for the AD7226 is limited by the slew-rate of the output buffer amplifiers. This can be seen from Figure 10 which shows the dynamic response for the AD7226 for a full scale change. Figures 11a and 11b show expanded settling-time photographs with the output waveforms derived from a differential input to an oscilloscope. Figure 11a shows the settling-time for a positive-going step and Figure 11b shows the settling-time for a negative-going output step.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7226. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7226 AGND and DGND pins (IN914 or equivalent).

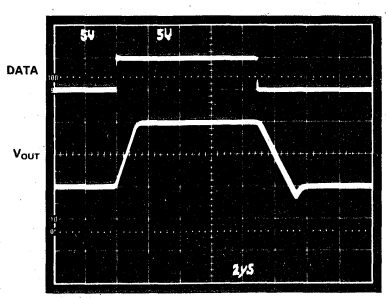


Figure 10. Dynamic Response (V_{SS} = −5V)

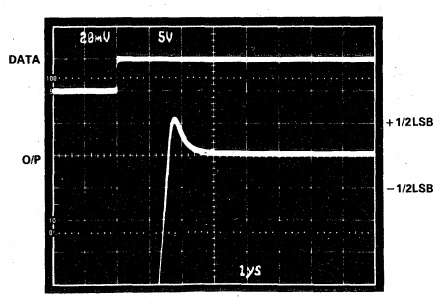


Figure 11a. Positive-Step Settling-Time (V_{SS} = −5V)

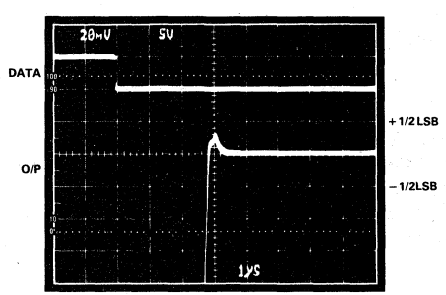


Figure 11b. Negative-Step Settling-Time (V_{SS} = −5V)

Applying the AD7226

Unipolar Output Operation

This is the basic mode of operation for each channel of the AD7226, with the output voltages having the same positive polarity as $+V_{REF}$. The AD7226 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). The code table for unipolar output operation is shown in Table II. Note that the voltage at V_{REF} must never be negative with respect to DGND in order to prevent parasitic transistor turn-on. Connections for the unipolar output operation are shown in Figure 12.

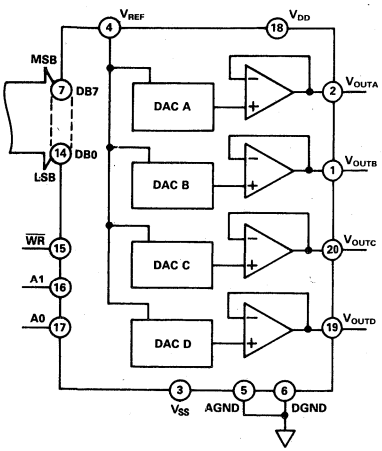


Figure 12. Unipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{255}{256}\right)$
1000 0001	$+V_{REF}\left(\frac{129}{256}\right)$
1000 0000	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0111 1111	$+V_{REF}\left(\frac{127}{256}\right)$
0000 0001	$+V_{REF}\left(\frac{1}{256}\right)$
0000 0000	0V

Note: $1LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

Table II. Unipolar Code Table

Bipolar Output Operation

Each of the DACs of the AD7226 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 13 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7226. In this case

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot (D_A\, V_{REF}) - \left(\frac{R2}{R1}\right) \cdot (V_{REF})$$

With R1 = R2

$$V_{OUT} = (2D_A - 1) \cdot V_{REF}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R1 and R2 causes gain and offset errors and therefore these resistors must match and track over temperature. Once again the AD7226 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 13 with R1 = R2.

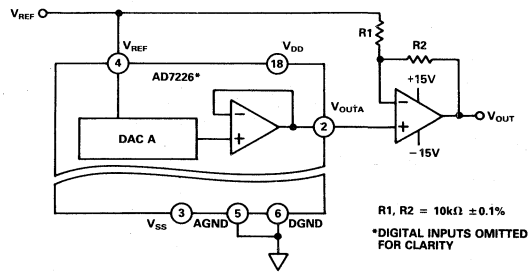


Figure 13. AD7226 Bipolar Output Circuit

DAC Latch Contents MSB LSB	Analog Output
1111 1111	$+V_{REF}\left(\frac{127}{128}\right)$
1000 0001	$+V_{REF}\left(\frac{1}{128}\right)$
1000 0000	0V
0111 1111	$-V_{REF}\left(\frac{1}{128}\right)$
0000 0001	$-V_{REF}\left(\frac{127}{128}\right)$
0000 0000	$V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

Table III. Bipolar (Offset Binary) Code Table

AGND BIAS

The AD7226 AGND pin can be biased above system GND (AD7226 DGND) to provide an offset "zero" analog output voltage level. Figure 14 shows a circuit configuration to achieve

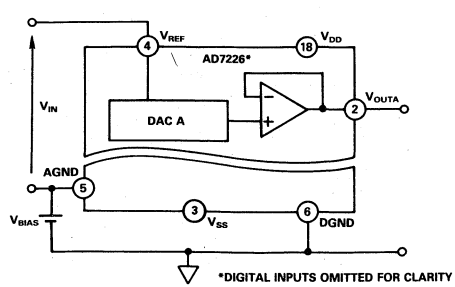


Figure 14. AGND Bias Circuit

this for channel A of the AD7226. The output voltage, V_{OUTA}, can be expressed as:

$$V_{OUTA} = V_{BIAS} + D_A (V_{IN})$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the AD7226. Note that V_{DD} and V_{SS} for the AD7226 should be referenced to DGND.

3-PHASE SINE WAVE

The circuit of Figure 15 shows an application of the AD7226 in the generation of 3-phase sine waves which can be used to control small 3-phase motors. The proper codes for synthesising a full sine wave are stored in EPROM, with the required phase-shift of 120° between the three D/A converter outputs being generated in software.

Data is loaded into the three D/A converters from the sine EPROM via the microprocessor or control logic. Three loops are generated in software with each D/A converter being loaded from a separate loop. The loops run through the look-up table producing successive triads of sinusoidal values with 120° separation which are loaded to the D/A converters producing 3 sine wave voltages 120° apart. A complete sine wave cycle is generated by stepping through the full look-up table. If a 256-element sine wave table is used then the resolution of the circuit will be 1.4° (360°/256). Figure 17 shows typical resulting waveforms. The sine waves can be smoothed by filtering the D/A converter outputs.

The fourth D/A converter of the AD7226, DAC D, may be used in a feedback configuration to provide a programmable reference voltage for itself and the other three converters. This configuration is shown in Figure 15. The relationship of V_{REF} to V_{IN} is dependent upon digital code and upon the ratio of R_F to R and is given by the formula

$$V_{REF} = \frac{(1 + G)}{(1 + G.D_D)} \cdot V_{IN}$$

where $G = R_F/R$

and D_D is a fractional representation of the digital word in latch D.

Alternatively, for a given V_{IN} and resistance ratio, the required value of D_D for a given value of V_{REF} can be determined from the expression

$$D_D = (1 + R/R_F) \cdot \frac{V_{IN}}{V_{REF}} - \frac{R}{R_F}$$

Figure 16 shows typical plots of V_{REF} versus digital code for three different values of R_F. With $V_{IN} = +2.5V$ and $R_F = 3R$ the peak-to-peak sine wave voltage from the converter outputs will vary between +2.5V and +10V over the digital input code range of 0 to 255.

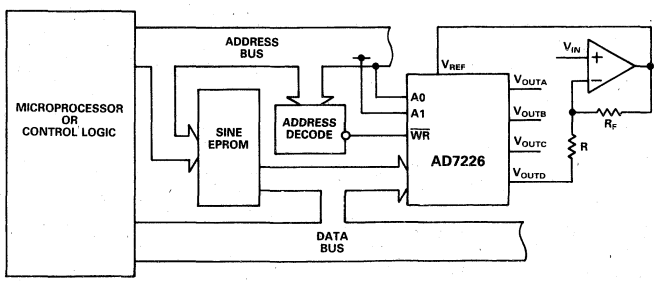


Figure 15. 3–Phase Sine Wave Generation Circuit

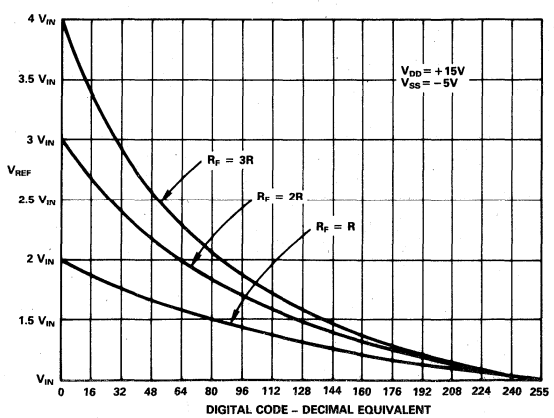


Figure 16. Variation of V_{REF} with Feedback Configuration

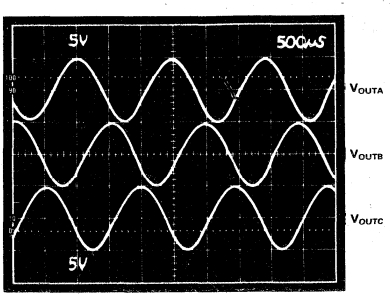


Figure 17. 3-Phase Sine Wave Output

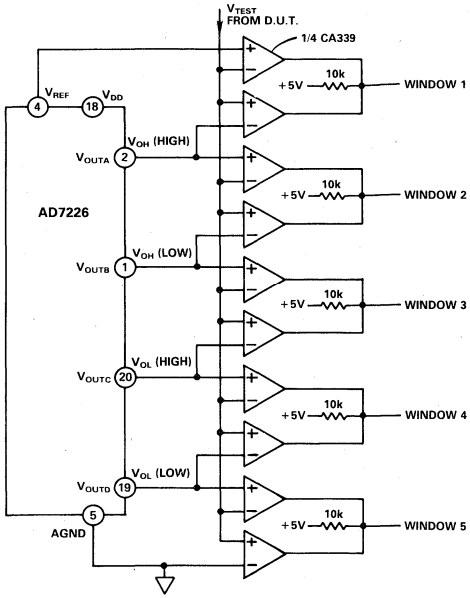


Figure 18a. Logic Level Measurement

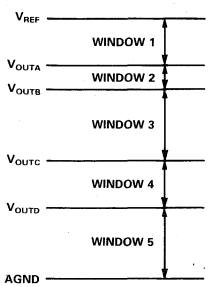


Figure 18b. Window Structure

STAIRCASE WINDOW COMPARATOR

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator of Figure 18a is a circuit which can be used, for example, to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmably set using the AD7226. Each adjacent pair of comparators forms a window of programmable size. If V_{TEST} lies within a window then the output for that window will be high. With a reference of 2.56V applied to the V_{REF} input, the minimum window size is 10mV.

The circuit can easily be adapted to allow for overlapping of windows as shown in Figure 19a. If the three outputs from this circuit are decoded then five different nonoverlapping programmable windows can again be defined.

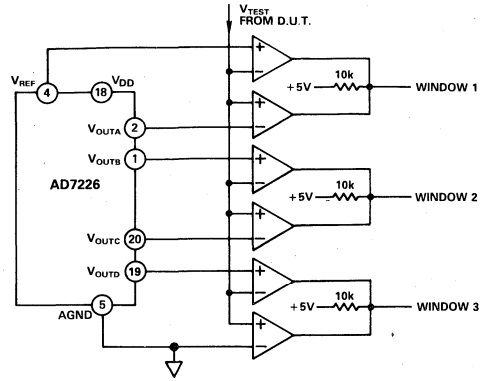


Figure 19a. Overlapping Windows

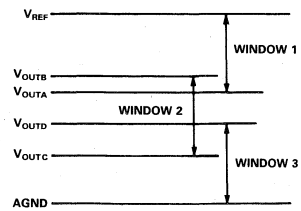


Figure 19b. Window Structure

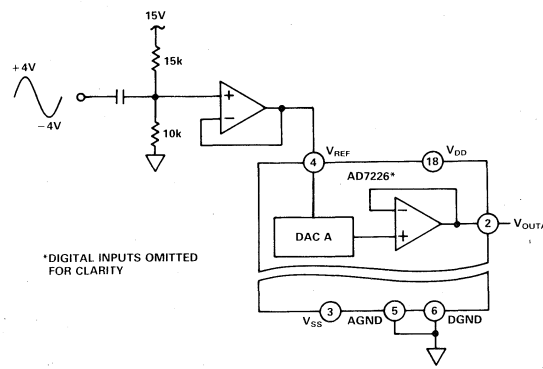


Figure 20. Varying Reference Signal

VARYING REFERENCE SIGNAL

In some applications, it may be desirable to have a varying signal applied to the reference input of the AD7226. The AD7226 has multiplying capability within upper and lower limits of reference voltage when operated with dual supplies. The upper and lower limits are those required by the AD7226 to achieve its linearity specification. Figure 20 shows a sine wave signal applied to the reference input of the AD7226. For input signal frequencies up to 50kHz the output distortion typically remains less than 0.1%. Typical 3dB bandwidth figure is 700kHz.

OFFSET ADJUST

Figure 21 shows how the AD7226 can be used to provide programmable input offset voltage adjustment for the AD544 op amp. Each output of the AD7226 can be used to trim the input offset voltage on one AD544. The 750kΩ resistor tied to +15V provides a fixed bias current to one offset node. For symmetrical adjustment, this bias current should equal the current in the other offset node with the half-full scale code (i.e. 10000000) on the DAC. Changing the code on the DAC varies the bias current and hence provides offset adjust for the AD544. For example, the input offset voltage on the AD544J, which has a maximum of ±2mV, can be programmably trimmed to ±10μV.

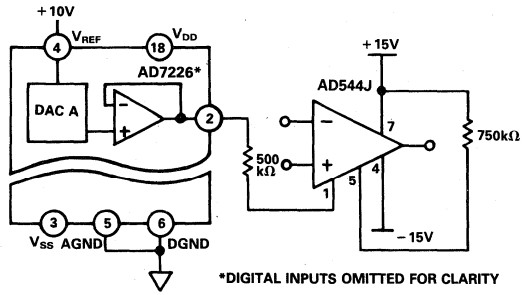


Figure 21. Offset Adjust for AD544

Microprocessor Interface

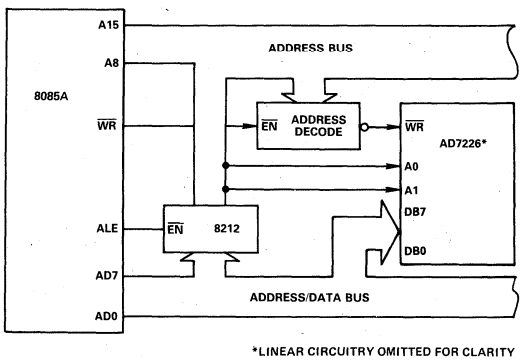


Figure 22. AD7226 to 8085A Interface

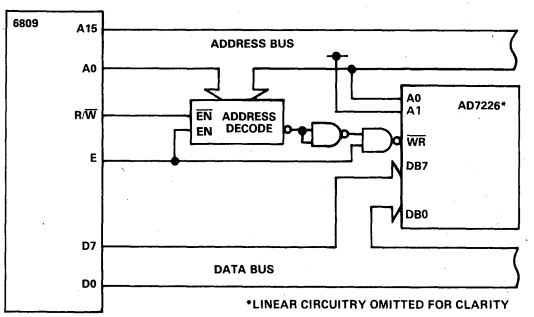


Figure 23. AD7226 to 6809 Interface

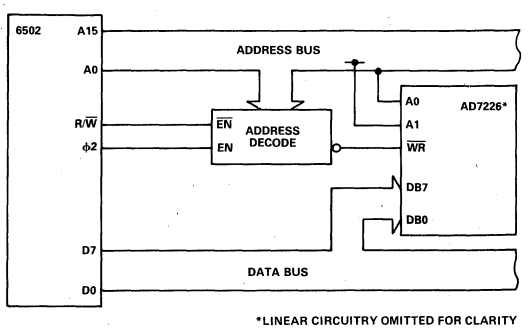


Figure 24. AD7226 to 6502 Interface

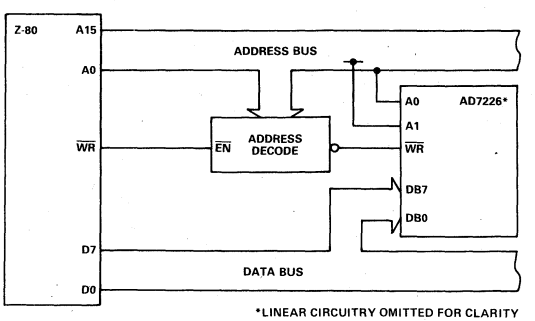


Figure 25. AD7226 to Z-80 Interface

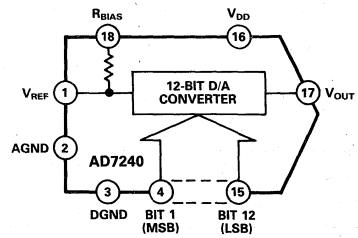
LC²MOS High Speed 12-Bit Voltage DAC

AD7240

FEATURES
Fast Voltage Settling Time: 550ns to 0.01%
Total Unadjusted Error: 1LSB max
Single Supply Operation
Latch Up Proof (No Protection Schottky Required)
Superb Differential Nonlinearity: 1/2LSB max over Temperature
Low Power Dissipation: 30mW

APPLICATIONS
Battery Powered Instrumentation
High Speed A/D Converters
Programmable Gain Amplifiers
Vector Graphics
S/D Converters

AD7240 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The Analog Devices AD7240 is a fast settling (550ns typically to 1/2LSB) 12-bit voltage output digital to analog converter. It is fabricated using an advanced high speed Linear Compatible CMOS process (LC²MOS) which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

The AD7240 operates with single +15 volts V_{DD} supply and exhibits exceptionally fast settling times due to the small (and code independent) value of capacitance at the output of the DAC.

The AD7240 also gives superior performance to other CMOS DACs when configured in the current steering mode as a multiplying DAC.

PRODUCT HIGHLIGHTS

1. **Single Supply Operation:** Voltage mode operation allows the AD7240 to be run from a single supply rail.
2. **High Speed Voltage Settling:** The high speed LC²MOS process gives the AD7240 extremely small propagation delays. The low capacitance of the AD7240 reduces the time constant at the DAC output. Thus the overall settling time is small (settling to 0.01% – typically 550ns).
3. **Total Unadjusted Error:** Includes gain error, offset error and relative accuracy. Connection of an AD7240 to a fixed reference guarantees the output voltage without external trimming. Connection of two or more DAC's to the same reference means that their output voltages will track to within the accuracy limits of the AD7240.
4. **Guaranteed Monotonicity:** All grades are guaranteed monotonic to 12 bits over all temperature ranges, in both the voltage mode and the current mode.

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N18B)
Suffix "Q" – Cerdip (Q18A)
Suffix "D" – Ceramic DIP (D18B)

[1]See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +1.23V, AGND = DGND = R_{BIAS} = 0V unless noted otherwise)

Parameter	Version	T_A = +25°C	T_A = T_{min} to T_{max}	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits min	
Total Unadjusted Error[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	This specification applies to all codes, however
	K,B,T	+1/2, −1	+1/2, −1 1/2	LSB max	equal or superior specifications apply for zero code and Full Scale Code – See Below
Relative Accuracy[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	
	K,B,T	+1/2, −1	+1/2, −1 1/2	LSB max	
Full Scale (Gain) Error[1,2]	J,A,S	+1/2, −1 1/4	+1/2, −2	LSB max	
	K,B,T	+1/2, −1/2	+1/2, −1/2	LSB max	
Full Scale (Gain) Tempco	J,A,S		±6	ppm/°C max	
(ΔFull Scale/ΔTemp)	K,B,T		±1.2	ppm/°C max	
Zero Code (Offset) Error[1,2]	J,A,S	+1/4, −1/2	+1/2, −1/2	LSB max	
	K,B,T	+1/8, −1/2	+1/4, −1/2	LSB max	
Differential Nonlinearity[1,2]	All	±1/2	±1/2	LSB max	All grades guaranteed monotonic to 12 bits T_{min} to T_{max}.
Power Supply Rejection (Ratio ΔGain/ΔV_{DD})	All	±0.005	±0.01	% per % max	V_{DD} = +15.5V to +14.5V; all digital inputs HIGH
REFERENCE INPUT					
Input Resistance (pin 1)	All	4.7	4.7	kΩ min	Min input resistance is approximately 0.67 × R_{LADDER}.
Input Capacitance[3] (pin 1)	All	40	40	pF min	All digital inputs LOW
		100	100	pF max	All digital Inputs HIGH
DIGITAL INPUTS					
V_{INH}	All	2.4	2.4	V min	
V_{INL}	All	0.8	0.8	V max	
Input Leakage Current	All	±1	±1	μA max	V_{IN} = 0V or 15V.
Input Capacitance	All	8	8	pF max	
Input Coding		Binary			Can be configured for offset binary–see Figures 14 and 16.
ANALOG OUTPUT					
Output Capacitance[3] (pin 17)	All	2.8	2.8	pF max	
Output Resistance (pin 17)	All	7k	7k	Ω min	
		12k	12k	Ω typ	
		15k	15k	Ω max	
Output Resistance Tempco	All	−300	−300	ppm/°C typ	
R_{BIAS}	All	7k	7k	Ω min	
		12k	12k	Ω typ	
		15k	15k	Ω max	
R_{BIAS}–R_{LADDER} Match.	All	0.1	0.1	% typ	
DYNAMIC PERFORMANCE					
Propagation Delay[3,4]	All	100	100	ns max	Measured from 50% of digital input to 10% of final analog output.
Voltage Settling Time[3,4,5,6,7]	All	900	900	ns max	To 0.01% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	550	550	ns typ	To 0.01% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	470	470	ns typ	To 0.04% of FSR for all 0's to all 1's or all 1's to all 0's.
	J,K	400	400	ns typ	To 0.2% of FSR for all 0's to all 1's or all 1's to all 0's.
Glitch Energy[4]	All	45	45	nV secs typ	Around major carry transition.
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V_{min}/V_{max}	Accuracy is guaranteed at +15V ±5%.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
I_{DD}	All	100	100	μA max	All digital inputs 0V or V_{DD}.

NOTES
[1]1LSB = V_{REF}/4096.
[2]DAC load $R_L > 10^{10}\Omega$.
[3]Guaranteed by design, not subject to test.
[4]Input logic levels 0 to 5V.
[5]Assuming a maximum external load capacitance of 2.8pF.
[6]Metal ceramic packages typically exhibit 20% higher inter-pin capacitance than plastic packages. Therefore metal ceramic devices typically exhibit settling times approximately 10% longer than plastic parts.
[7]FSR is full scale range.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . −0.3V, +17V
Digital Input Voltage to DGND . . . . . −0.3V, V_{DD}
V_{BIAS}, V_{OUT} to DGND . . . . . ±25V
V_{REF} to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package) to 75°C 450mW
Derates above +75°C . . . . . 6mW/°C
Operating Temperature
Commercial . . . . . 0 to +70°C
Industrial . . . . . −25°C to +85°C
Extended . . . . . −55°C to +125°C
Storage Temperature . . . . . +65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

SPECIFICATION DEFINITIONS

TOTAL UNADJUSTED ERROR

This is a comprehensive specification which includes gain error, relative accuracy and zero code offset when configured as shown in Figure 11.

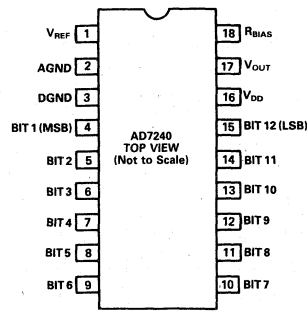
Absolute full scale is V_{REF} – 1LSB (IDEAL) where 1LSB (IDEAL) is $\frac{V_{REF}}{4096}$.

NOTE: "ERROR" defined is ACTUAL VALUE – IDEAL VALUE.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

PIN CONFIGURATION



ORDERING INFORMATION

Total Unadjusted Error	Plastic	Cerdip[1]	Side Brazed Ceramic
$T_A = T_{MIN}$ to T_{MAX}	0 to +70°C	−25°C to +85°C	−55°C to +125°C
+1/2, −2LSB	AD7240JN	AD7240AQ	AD7240SD
+1/4, −1 1/2LSB	AD7240KN	AD7240BQ	AD7240TD

NOTE
[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

9

Typical Performance Characteristics

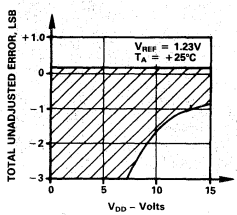


Figure 1. Total Error vs V_{DD} (Shaded Area Shows Typical Range of Total Unadjusted Error vs. Supply Voltage for AD7240JN)

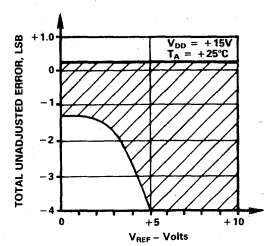


Figure 2. Total Error vs. Reference Voltage (Shaded Area Shows Range of Values of Total Unadjusted Error That Typically Occurs for AD7240JN)

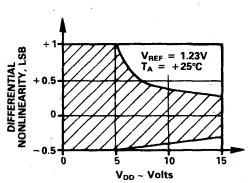


Figure 3. Differential Nonlinearity vs. V_{DD} (Shaded Area Shows Typical Range of DNL vs. Supply Voltage)

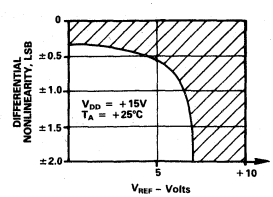


Figure 4. Differential Nonlinearity vs. Reference Voltage (Shaded Area Shows Range of Values of DNL That Typically Occur for K and J Grades)

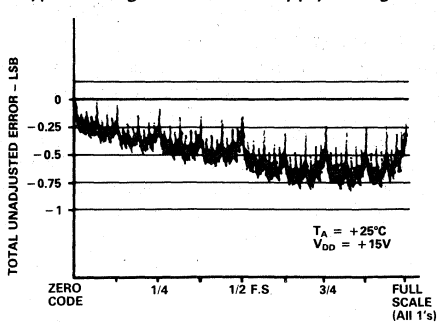


Figure 5. Total Unadjusted Error vs. Digital Code

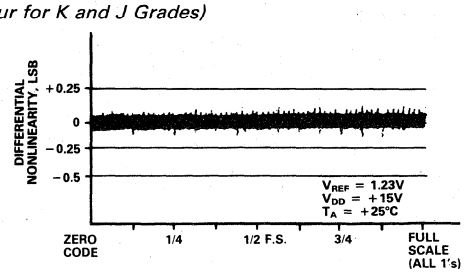


Figure 6. Differential Nonlinearity vs. Digital Code

CIRCUIT INFORMATION

ANALOG SECTION

The AD7240 12-bit voltage DAC consists of a highly stable thin film R-2R ladder and twelve high speed N MOS single pole double throw switches.

The AD7240 has low capacitance at the V_{OUT} terminal, and hence exhibits fast output voltage settling times.

The simplified circuit diagram of the D/A converter is shown in Figure 7.

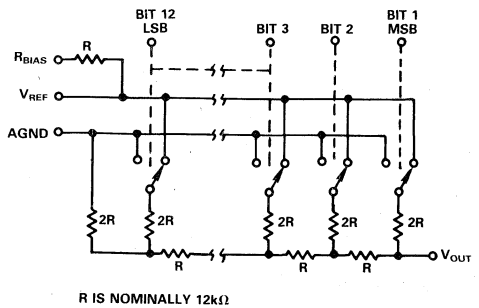


Figure 7. AD7240 Functional Diagram (Inputs High)

DIGITAL SECTION

The 12 digital inputs are designed to be both TTL and CMOS compatible when V_{DD} equals +15V. All logic inputs are static protected MOS gates with typical input currents of less than 1nA. Internal input protection is achieved by an on-chip distributed diode from GND to each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and GND) as practically possible.

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

When operated in the voltage switching mode the AD7240 exhibits code independent (fixed) output capacitance and output resistance. This means that settling time of the AD7240 is virtually the same for all code changes when operated as per Figure 10.

In contrast, the output impedance and thus the settling time of current mode DACs is code dependent. Moreover, with a current mode CMOS DAC the large output capacitance places a limitation on the realizable settling time, even when using a fast output op amp.

The low values of output capacitance of the AD7240 ensure very fast voltage settling when configured with a high speed follower.

SETTLING TIME

The time taken for voltage settling of the AD7240 to less than 1/2LSB is given by the approximation:

*Settling Time	≃	$t_{pd} + 9R(C_{OUT} + C_{EXT})$
t_{pd}	–	Logic Propagation Delay
R	–	DAC Ladder Resistance
C_{OUT}	–	DAC Output Capacitance
C_{EXT}	–	Capacitance due to External Circuit.

*This approximation assumes very high load impedance.

Figure 8 shows the output voltage transient response waveform for the transition resulting when all digital inputs change from 0 volts to +5 volts.

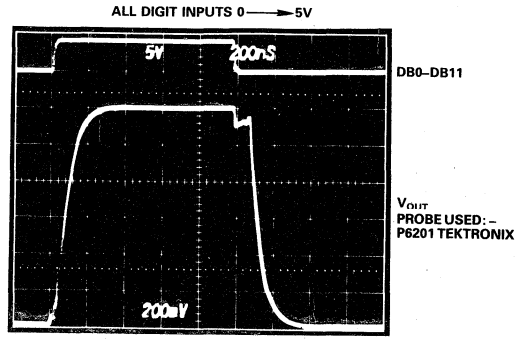


Figure 8. AD7240 Transient Response Waveform

Figure 9 shows the glitch energy waveform for the major transition. Figure 10 shows the circuit used to achieve the waveforms shown in Figures 8 and 9.

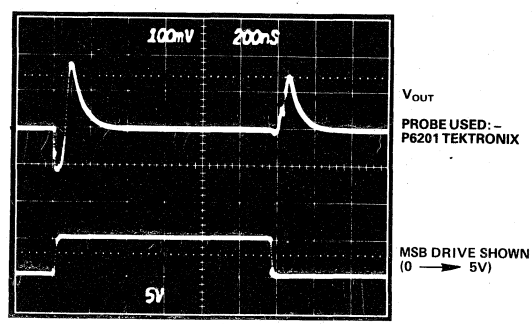


Figure 9. AD7240 – Major Transition Glitch

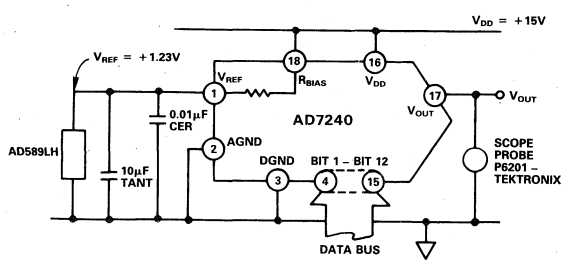


Figure 10. Dynamic Performance Test Circuit

VOLTAGE REFERENCE

The input impedance at the V_{REF} pin of the AD7240 is code dependent and can vary from 7K up to infinity. The nodal capacitance at the reference terminal is also code dependent and typically varies from 40pF to 90pF. Therefore it is essential that the reference be adequately decoupled at pin 1 of the AD7240 in order to present a low output impedance and thus maintain full accuracy under changing load conditions.

APPLICATION INFORMATION

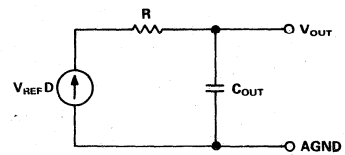
LOAD IMPEDANCE

The AD7240 equivalent output circuit of Figure 11 shows a Thevenin voltage source V_{REF} D with a fixed output resistance and capacitance of R and C_{OUT} respectively. D is a fractional representation of the digital input word N i.e. D = N/4096.

Resistive loading at pin 17 of the AD7240 causes scale factor error. Op amp bias current through the DAC output impedance (12kΩ nominal) introduces an offset term.

For example, a 60MΩ load resistance on pin 17 introduces a 1LSB scale factor error at pin 17. Op amp bias current of 25 nanoamps introduces a 1LSB offset term. Effects of amplifier bias current can be minimized by ensuring the parallel combination of R1 and R2 (Figure 12) is equal to the DAC's output impedance at pin 17 (nominally 12kΩ). If the amplifier circuit (of Figure 12) is configured to provide a gain of +1, resistor R2 should be included and should equal 12kΩ to minimize output error due to bias current.

Figure 11 shows the equivalent circuit of the output of the AD7240.



R – DAC LADDER RESISTANCE (12KΩ TYP)
C_{OUT} – DAC OUTPUT CAPACITANCE (2.8pF MAX)
V_{REF} D – THEVENIN VOLTAGE SOURCE (O ≤ D ≤ 4095/4096)

Figure 11. Equivalent Output Circuit of AD7240

AD7240 OPERATION MODES

The AD7240 can operate in several different modes. Each mode has its own particular characteristics. These are summarized below and discussed in detail in the paragraphs following.

9

SUMMARY OF OPERATION MODES

Mode	Performance Feature	Circuit Constraints
1. VOLTAGE SWITCHING (Figure 12)	• Single supply operation. • Positive V_{IN} gives Positive V_{OUT} • Reduced charge injection. • Constant output impedance. • Low output capacitance obviates need for extra op amp compensation thus reducing settling time.	• Code dependent input impedance requires well buffered reference voltage. • V_{IN} must never go negative. • For 12-bit linearity max V_{IN} range must be AGND < V_{IN} ≤ +2.0V
2. VOLTAGE SWITCHING WITH AGND BIAS VOLTAGE (Figure 13)	• Single supply operation with variable "zero" output level.	• Same as for 1.
3. VOLTAGE SWITCHING OFFSET BINARY (Figure 14)	• Bipolar Output • Same as 1.	• Needs DUAL rail power supply for op amp. • Same as for 1.
4. CURRENT STEERING (Figures 15 & 16)	• Four quadrant multiplication. • Good power supply rejection. • Low distortion • Constant input impedance at V_{REF} • 1ppm/°C typical gain tempco.	• Needs DUAL rail power supply for op amp. • Output op amp must have low input offset voltage to minimize "noise gain" effects on analog output.
5. CURRENT STEERING WITH AGND BIAS VOLTAGE (Figures 17 and 18)	• Single supply operation. • Four quadrant multiplication. • Good power supply rejection. • Low output leakage current.	• Need op amp with low input offset voltage to minimize "noise gain" effects.

AD7240 Operation Modes

1. VOLTAGE SWITCHING MODE

The circuit in Figure 12 shows the AD7240 connected in the voltage switching mode. Since V_{OUT} is the same polarity as V_{REF}, this configuration allows single supply operation. Note that the voltage V_{REF} must always be positive with respect to DGND in order to prevent parasitic transistor turn-on.

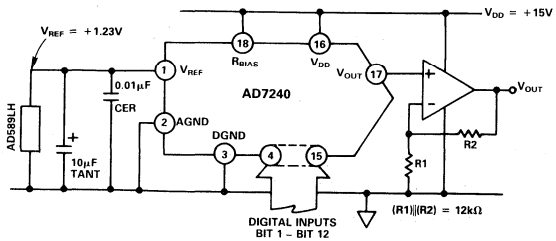


Figure 12. AD7240 in Single Supply Voltage Switching Mode

To maintain linearity, the voltages at V_{REF} and AGND should remain within 2.0 volts of each other for a V_{DD} of +15 volts. If V_{DD} is reduced from 15V or the differential voltage between V_{REF} and AGND is increased to more than 2.0 volts, the accuracy of the DAC will be degraded. Figures 1 and 2 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. A suitable reference for this configuration is the AD589HL – a two terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage. The bandgap reference is conveniently biased by connecting the R_{BIAS} pin to the positive supply. However due to the internal V_{REF} bond wire resistance, the AD589 bias current develops an error voltage which appears in series with the reference voltage on pin 1. This error voltage (0.5 LSB's typ) acts to shift the Total Unadjusted Error plot of Figure 5 in a positive direction. Therefore, R_{BIAS} should only be used in applications which can accommodate this shift, otherwise use an external bias resistor and tie pin 18 to pin 2 (as shown in Figure 14).

Note that the output voltage range has been extended by using a noninverting gain stage.

The output voltage V_{OUT} is expressed as:

$$V_{OUT} = (V_{REF})(D)\left(\frac{R_1 + R_2}{R_2}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

Fastest settling can be achieved by using dual supply op amp.

2. VOLTAGE SWITCHING MODE WITH AGND BIAS VOLTAGE

AGND can be biased above DGND to provide an offset "zero" analog output voltage level. Figure 13 shows this circuit configuration. Note that the output voltage range has been extended by using a noninverting gain stage to buffer the DAC.

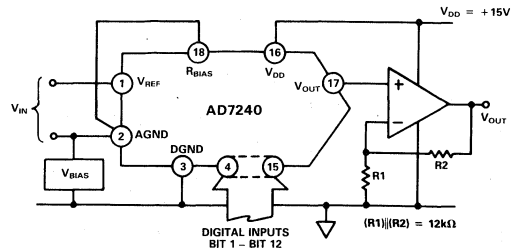


Figure 13. AD7240 in Single Supply Voltage Switching Mode with AGND Bias Voltage

The output voltage V_{OUT} is expressed as:

$$V_{OUT} = (V_{BIAS})\left(\frac{R_1 + R_2}{R_1}\right) + (V_{IN})(D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where $V_{IN} \leq +2.0V$, and where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

The effect of V_{BIAS} on total unadjusted error and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset (see Figures 1 and 3).

3. VOLTAGE SWITCHING MODE – OFFSET BINARY OPERATION

Figure 14 shows a circuit used to implement offset binary coding in the voltage switching mode. Mismatch between R1 and R2 causes both offset and full scale error, therefore, these resistors must match (to within 0.01%) and track over temperature.

Table I shows the digital code vs output voltage relationship for Figure 14.

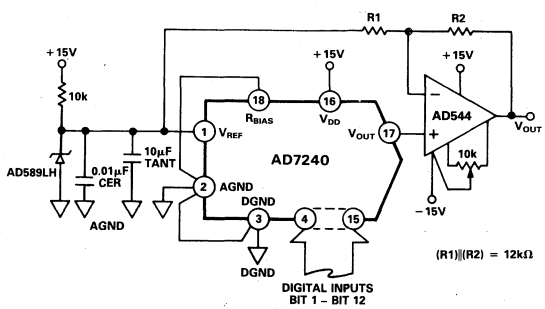


Figure 14. AD7240 in Offset-Binary Voltage-Switching Mode

Digital Input	Analog Output
1111 1111 1111	$+V_{REF} \cdot \left\{\frac{2047}{2048}\right\}$
1000 0000 0000	0V
0000 0000 0000	$-V_{REF}$

Table I. Offset Binary Code Table for Figure 14 with R1 = R2

4. CURRENT STEERING MODE

Unipolar Operation (2 Quadrant Multiplication)

The circuit in Figure 15 shows the AD7240 connected in the current steering mode with a unipolar voltage output. In this configuration R_{BIAS} is used as the feedback resistor providing a typical gain error of ±4LSBs. Typical gain T.C. in this mode is 1ppm/°C. Resistors R1 and R2 have been included to allow gain trimming. See Reference 2 for additional information.

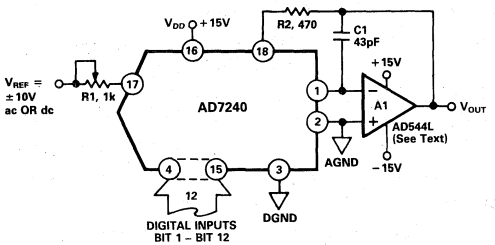


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

Capacitor C1 provides phase compensation and helps to prevent overshoot and ringing when using high speed op amps. Note that the circuit has a constant input impedance of R_{LADDER} at pin 17. V_{REF} can be a fixed dc voltage or an ac signal or a fixed dc or ac current. Table II shows the digital code vs. output voltage relationship for Figure 15.

Digital Input	Analog Output
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\,V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 15

Bipolar Operation (4 Quadrant Multiplication)

Figure 16 and Table III illustrate the recommended circuit and code relationship for Bipolar Operation in the current steering mode. The D/A function itself uses offset binary code. An inverter can be connected to the MSB line to convert offset binary input code to 2's complement code. R3, R4 and R5 must be selected to match within 0.01% and they should have the same temperature coefficients.

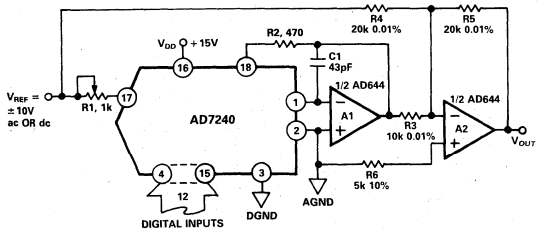


Figure 16. Bipolar Operation (4 Quadrant) Offset Binary Code

Digital Input	Analog Output
1111 1111 1111	$+V_{REF}\cdot\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\cdot\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\cdot\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\cdot\left(\frac{2048}{2048}\right)$

Table III. Offset Binary Table for Circuit of Figure 16

In the current steering mode, the AD7240 has a code dependent output resistance which in turn can cause a code dependent error voltage or "noise gain" at the output of amplifier A1. The maximum amplitude of this error voltage, which adds to the D/A converter nonlinearity, depends on V_{OS} where V_{OS} is the amplifier input offset voltage (Ref 1). To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation.

5. CURRENT STEERING MODE WITH AGND BIAS VOLTAGE

The AD7240 has been designed so that AGND (pin 2) can be biased to any voltage between DGND and (V_{DD} – 10V). V_{DD} must be kept at least 10V above V_{REF} to ensure that monotonicity is preserved. This feature allows single supply operation in the current steering mode. Figure 17 shows the basic circuit configuration. The AD584 pin programmable reference fixes AGND at +5.0V. The output voltage swing is from +5V to +10V allowing operation from a single +15V power supply.

The output voltage V_{OUT} is

$$V_{OUT} = V_{BIAS} + (D)(V_{BIAS})$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

The circuit of Figure 17 can be modified to allow any full scale range to be chosen. Figure 18 shows the circuit modified to provide an output range of ±2.5V about a "pseudo-analog ground" of +5V i.e. from +2.5V to 7.5V.

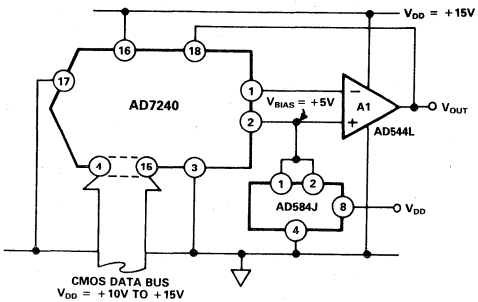


Figure 17. AD7240 in Single Supply Current Steering Mode with AGND Bias Voltage

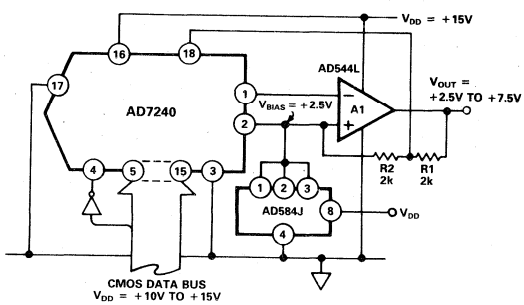


Figure 18. AD7240 in Single Supply Current Steering Mode with AGND Bias Voltage and Gain Resistors (2's Complement Coding)

This voltage range allows operation from a single +10V to +15V power supply. The AD584 pin programmable reference now fixes AGND at +2.5V.

The output voltage V_{OUT} is

$$V_{OUT} = \left(\frac{R_1 + R_2}{R_2}\right)(D)(V_{BIAS}) + (V_{BIAS})$$

Where D is a fractional representation of the digital input word at the DAC ($0 \leq D \leq 4095/4096$).

REFERENCE MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

1. Applications Guide to CMOS Multiplying D/A Converters available from Analog Devices, Publication Number G479.
2. Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs – Application Note, Publication Number E630–10–6/81 available from Analog Devices.
3. Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.
4. "Input Resistor Stabilizes MDAC's Gain" – Paul Brokaw, EDN January 7th, 1981; – not available from Analog Devices.

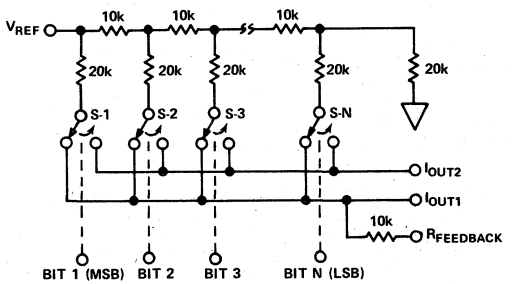
CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

AD7520, AD7521

FEATURES
AD7520: 10-Bit Resolution
AD7521: 12-Bit Resolution
End Point Linearity: 8-, 9- and 10-Bit
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 1/2LSB @ 100kHz
TTL/DTL/CMOS Compatible

Note: AD7533 is recommended for new 10-bit designs. AD7541A or AD7545 is recommended for new 12-bit designs.

AD7520, AD7521 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7520: N=10
AD7521: N=12
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

9

GENERAL DESCRIPTION

The AD7520 (AD7521) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The devices use advanced CMOS and thin film technologies providing up to 10-bit accuracy with TTL/DTL/CMOS compatibility.

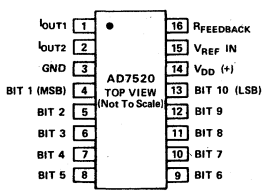
The AD7520 (AD7521) operates from +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical AD7520 (AD7521) applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

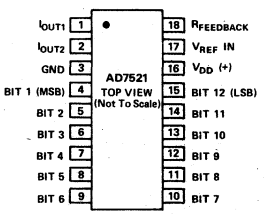
ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7521JN	AD7520JD AD7521JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7521KN	AD7520KD AD7521KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7521LN	AD7520LD AD7521LD	AD7520UD AD7521UD

PIN CONFIGURATIONS



16-PIN DIP



18-PIN DIP

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP Package
AD7520: (D16B)
AD7521: (D18B)

Suffix N: Plastic DIP Package
AD7520 (N16B)
AD7521 (N18B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER	AD7520	AD7521	TEST CONDITIONS
DC ACCURACY[1]			
Resolution	10 Bits	12 Bits	
Relative Accuracy (See Figure 5)			
	J, 0.2% of FSR max (8 Bit)	*	S,T,U: over -55°C to +125°C
	S, 0.2% of FSR max (8 Bit)	*	$-10V \leq V_{REF} \leq +10V$
	K, 0.1% of FSR max (9 Bit)	*	
	T, 0.1% of FSR max (9 Bit)	*	
	L, 0.05% of FSR max (10 Bit)	*	
	U, 0.05% of FSR max (10 Bit)	*	
Nonlinearity Tempco	2ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Gain Error[2]	0.3% of FSR typ	*	$-10V \leq V_{REF} \leq +10V$
Gain Error Tempco[2]	10ppm of FSR/°C max	*	$-10V \leq V_{REF} \leq +10V$
Output Leakage Current (either output)	200nA max	*	Over specified temperature range
Power Supply Rejection (See Figure 6)	50ppm of FSR/% typ	*	
AC ACCURACY			To 0.05% of FSR
Output Current Settling Time (See Figure 10)	500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (See Figure 9)[4]	10mV p-p max		V_{REF} = 20V p-p, 100kHz
		*	All digital inputs low
REFERENCE INPUT			
Input Resistance[3]	5kΩ min	*	
	10kΩ typ	*	
	20kΩ max	*	
ANALOG OUTPUT			
Output Capacitance I_{OUT1}	120pF typ	*	All digital inputs high
(See Figure 8) I_{OUT2}	37pF typ	*	All digital inputs high
I_{OUT1}	37pF typ	*	All digital inputs low
I_{OUT2}	120pF typ	*	All digital inputs low
Output Noise (both outputs) (See Figure 7)	Equivalent to 10kΩ typ Johnson noise	*	
DIGITAL INPUTS[5]			
Low State Threshold	0.8V max	*	Over specified temperature range
High State Threshold	2.4V min	*	Over specified temperature range
Input Current (low to high state)	1μA typ	*	Over specified temperature range
Input Coding	Binary	*	See Tables I & II under Applications
POWER REQUIREMENTS			
Power Supply Voltage Range	+5V to +15V	*	
I_{DD}	5nA typ	*	All digital inputs at GND
	2mA max	*	All digital inputs high or low
Total Dissipation (Including ladder)	20mW typ	*	

NOTES
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] Using the internal $R_{FEEDBACK}$
[3] Ladder and feedback resistor tempco is approximately -150ppm/°C.
[4] To minimize feedthrough with the ceramic package, the user must ground the metal lid. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.
[5] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . -100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +70°C
JD, KD, LD Versions . . . . . -25°C to +85°C
SD, TD, UD Versions . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{DD} = +15V unless otherwise noted

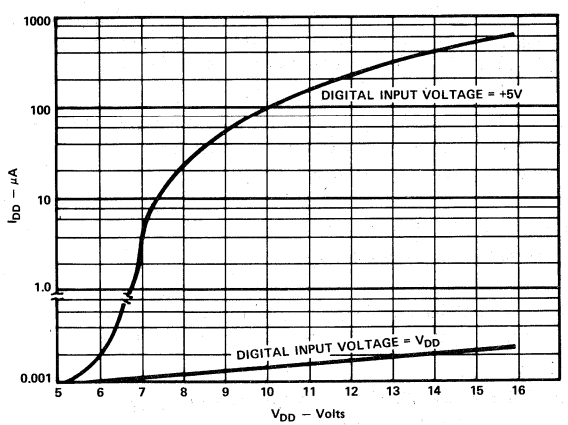


Figure 1. Supply Current vs. Supply Voltage

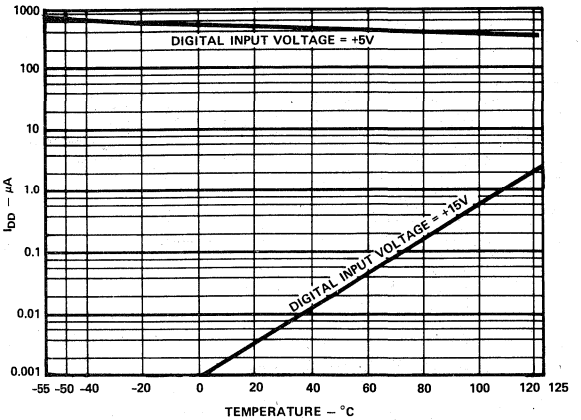


Figure 2. Supply Current vs. Temperature

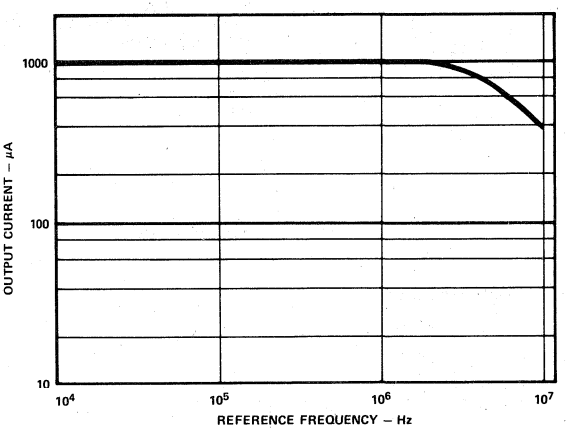


Figure 3. Output Current Bandwidth

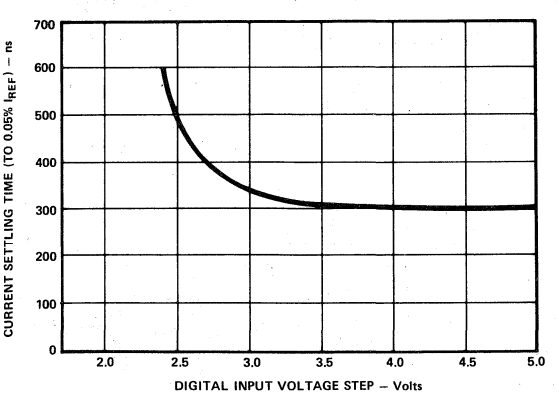


Figure 4. Output Current Settling Time vs. Digital Input Voltage

TEST CIRCUITS

Note: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7521.

DC PARAMETERS

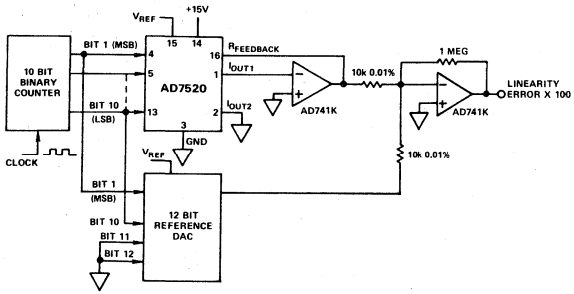


Figure 5. Relative Accuracy

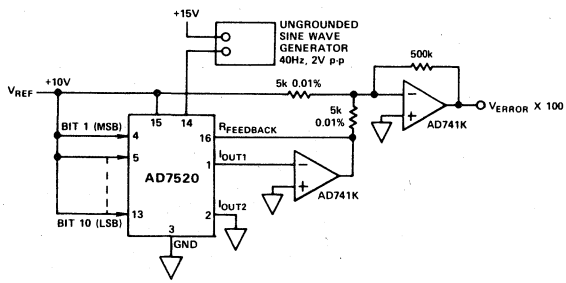


Figure 6. Power Supply Rejection

AC PARAMETERS

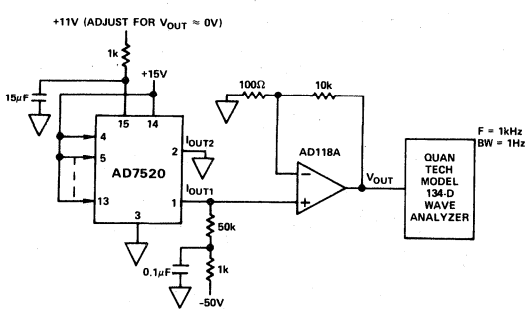


Figure 7. Noise

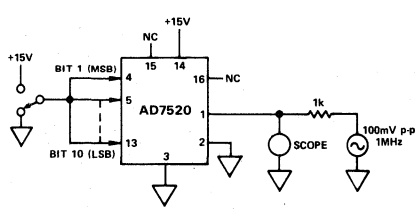


Figure 8. Output Capacitance

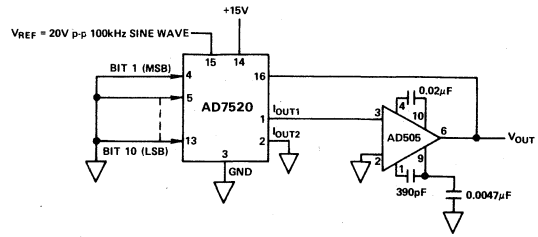


Figure 9. Feedthrough Error

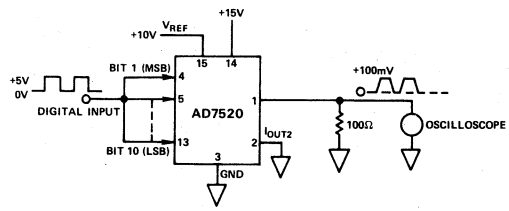


Figure 10. Output Current Settling Time

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

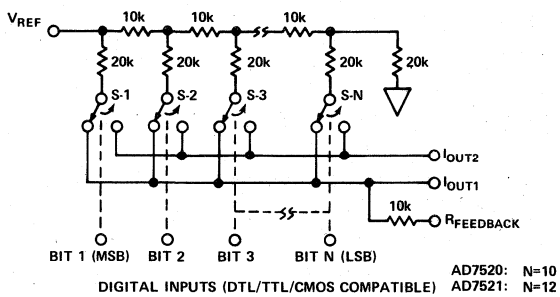
OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7521), a 10-bit (12-bit) multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten (twelve) CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 11. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.



(Switches shown for Inputs "High")

Figure 11. AD7520 (AD7521) Functional Diagram

One of the CMOS current switches is shown in Figure 12. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the first six switches are binarily scaled so the voltage drop across each switch is the same. For example, switch-1 of Figure 12 was designed for an "ON" resistance of 20 ohms, switch-2 of 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

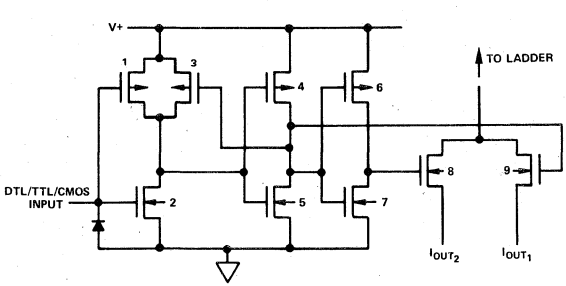


Figure 12. CMOS Switch

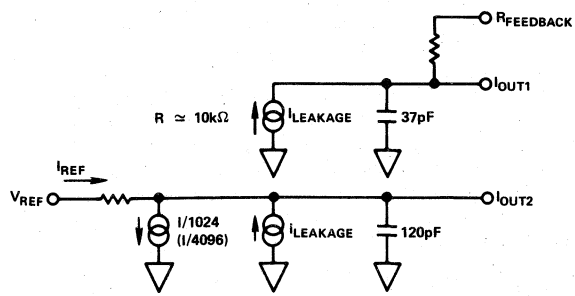


Figure 13. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 13 and 14. In Figure 13 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}\left(\frac{I}{4096}\right)$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 37pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 14 is similar to Figure 13; however, the "ON" switches are now on terminal I_{OUT1}, hence the 120pF at that terminal.

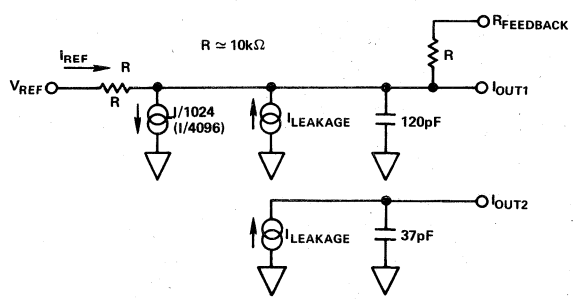


Figure 14. AD7520 (AD7521) Equivalent Circuit– All Digital Inputs High

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 15 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I. Protection Schottky shown in Figure 15 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

R1 provides full scale trim capability [i.e.—load the DAC register to 11 1111 1111, adjsut R1 for $V_{OUT} = -V_{REF}(1 - 2^{-10})$]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at I_{OUT1}).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ).

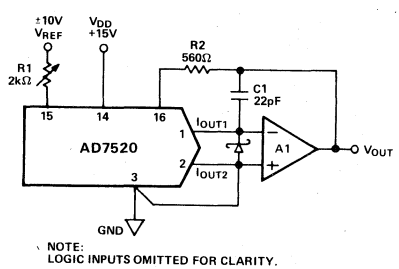


Figure 15. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 16 and Table II illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) or an ac reference the circuit provides offset binary operation. Protection Schottky shown in Figure 16 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

With the DAC register loaded to 10 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

Offset Adjustment

1. Make V_{REF} approximately +10V.
2. Tie all digital inputs to +15V (Logic "1").
3. Adjust amplifier #2 offset trimpot for 0V ±1mV at amplifier #2 output.
4. Tie MSB (Bit 1) to +15V, all other bits to ground.
5. Adjust amplifier #1 offset trimpot for 0V ±1mV at V_{OUT}.

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table II. Code Table — Bipolar (Offset Binary) Operation

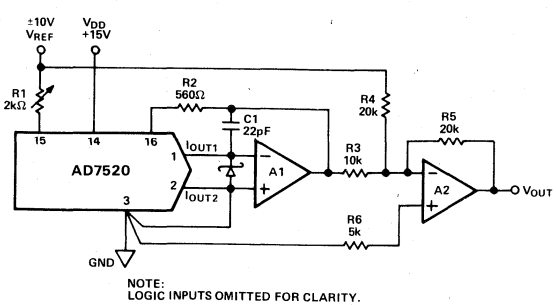


Figure 16. Bipolar Operation (4-Quadrant Multiplication)

10-BIT AND SIGN MULTIPLYING DAC

Figure 17 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 10-bit resolution in each quadrant. The 10 magnitude bits provide digitally controlled attenuation of the reference while the sign bit provides polarity control. The AD7512 is a fully protected CMOS change-over switch. Mismatch between R4 and R5 introduces a gain error. Table III shows the Code Table for the circuit of Figure 17.

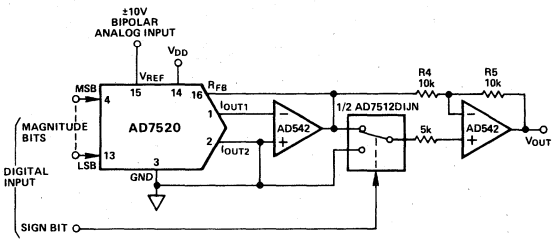


Figure 17. 10-Bit and Sign Multiplying DAC

Sign Bit	Binary Numbers in DAC Register	Analog Output
0	11 1111 1111	$+V_{IN} \cdot 1-2^{-10}$
0	00 0000 0000	0 Volts
1	00 0000 0000	0 Volts
1	11 1111 1111	$-V_{IN} \cdot 1-2^{-10}$

Table III. 10-Bit Plus Sign Magnitude Table

9

DIGITALLY PROGRAMMABLE LIMIT DETECTOR

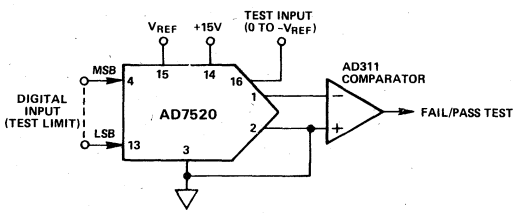


Figure 18. Programmable Limit Detector

The circuit of Figure 18 shows how the AD7520 is used to implement a programmable limit detector. If the test input does not meet the test limit set by the digital input, then the pass/fail output will indicate a fail.

VOLTAGE MODE OPERATION

The AD7520 can also be used in the voltage-switching mode and the circuit of Figure 19 shows how the DAC can be connected for voltage switching by reversing the roles of the reference input and I_{OUT1}. It is a single supply application with the DAC and the CMOS operational amplifier both powered from a single +15V supply. With a single supply operational amplifier, offset is difficult to remove completely; therefore, some offset may have to be tolerated usually amounting to less than one-half LSB at 3.5V reference. The voltage switching mode permits only a single polarity of input (positive with respect to common).

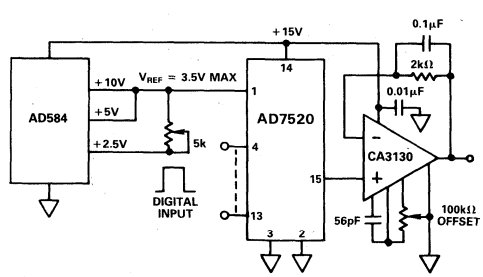


Figure 19. Single Supply Voltage Mode Operation

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_0 = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 20, the transfer function becomes

$$V_0 = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit 10) ON, the gain is 1024. With all bits ON, the gain is 1 (±1 LSB).

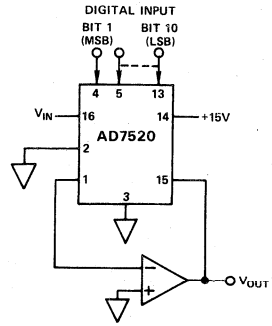


Figure 20. Analog/Digital Divider

ANALOG DEVICES

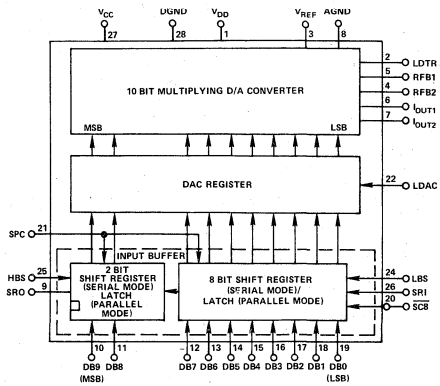
CMOS 10-Bit, Buffered Multiplying D/A Converter

AD7522

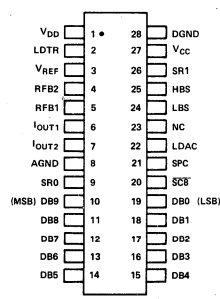
FEATURES

10-Bit Resolution
8-, 9- & 10-Bit Linearity
Microprocessor Compatible
Double Buffered Inputs
Serial or Parallel Loading
DTL/TTL/CMOS Direct Interface
Nonlinearity Tempco: 2ppm of FSR/°C
Gain Tempco: 10ppm of FSR/°C
Very Low Power Dissipation
Very Low Feedthrough

AD7522 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7522 is a monolithic CMOS 10-bit multiplying D/A converter, with an input buffer and a holding register, allowing direct interface with microprocessors. Most applications require the addition of only an operational amplifier and a reference voltage.

The key to easy interface to a data bus is the AD7522's ability to load the input buffer in two bytes (an 8-bit and a 2-bit byte), and subsequently move this data to a holding register, where the digital word is converted into an analog current or voltage (with external operational amplifier). The input loading of either 8 or 10 bits can be done in a parallel or serial mode.

The AD7522 is packaged in a 28-pin DIP, and operates with a +15V main supply at 2mA max, and a logic supply of +5V for TTL interface, or +10 to +15V for CMOS interface.

A thin film on high density CMOS process, using silicon nitride passivation, ensures high reliability and excellent stability.

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0 to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8-Bit)	AD7522JN	AD7522JD	AD7522SD
0.1% (9-Bit)	AD7522KN	AD7522KD	AD7522TD
0.05% (10-Bit)	AD7522LN	AD7522LD	AD7522UD

PACKAGE IDENTIFICATION[1]

Suffix "D": Ceramic DIP Package – (D28B)
Suffix "N": Plastic DIP Package – (N28B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{REF} = ±10V, TA = +25°C unless otherwise noted)

PARAMETER		TA = +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
STATIC ACCURACY				
Resolution	All	10 Bits min	10 Bits min	$\overline{SC8}$ = "1"
Nonlinearity	AD7522J	±0.2% FSR max		
	AD7522S	±0.2% FSR max	±0.2% FSR max	
	AD7522K	±0.1% FSR max		
	AD7522T	±0.1% FSR max	±0.1% FSR max	
	AD7522L	±0.05% FSR max		
	AD7522U	±0.05% FSR max	±0.05% FSR max	$-10V \leq V_{REF} \leq +10V$
Nonlinearity Tempco[1]	AD7522J,K,L	±1ppm FSR/°C typ	±2ppm FSR/°C max	
	AD7522S,T,U		±2ppm FSR/°C max	
Gain Error	AD7522J,K,L	±0.3% Reading typ		
Gain Error Tempco[1]	AD7522J,K,L	±5ppm of Reading/°C typ	±10ppm of Reading/°C max	
	AD7522S,T,U		±10ppm of Reading/°C max	
Output Leakage Current at I_{OUT1} or I_{OUT2}	All		200nA max	I_{OUT1}: DB0 through DB9 = 0 I_{OUT2}: DB0 through DB9 = 1
Power Supply Rejection	AD7522J,K,L	50ppm of Reading/% typ		
AC ACCURACY				
Feedthrough Error[1]	All	1mV p-p typ, 10mV p-p max		V_{REF}= 20V p-p; 10kHz
Output Current Settling Time	AD7522J,K,L	500ns typ		To 0.05% of FSR for a FSR Step. HBS and LBS Low to High LDAC = 1
REFERENCE INPUT				
Input Resistance	All	5kΩ min/20kΩ max	50kΩ min/20kΩ max	
ANALOG OUTPUT				
Output Capacitance				
C_{OUT1}	AD7522J,K,L	120pF typ		All Data Input High
C_{OUT2}	AD7522J,K,L	40pF typ		All Data Input High
C_{OUT1}	AD7522J,K,L	40pF typ		All Data Inputs Low
C_{OUT2}	AD7522J,K,L	120pF typ		All Data Inputs Low
DIGITAL INPUTS				
Low State Threshold	All	0.8V max	0.8V max	V_{CC} = +5V
	All	1.5V max	1.5V max	V_{CC} = +15V
High State Threshold	All	2.4V min	2.4V min	V_{CC} = +5V
	All	13.5V min	13.5V min	V_{CC} = +15V
Input Current	AD7522J,K,L	1μA typ		
LDAC Pulse Width[1]	All	500ns min	500ns min	LDAC: 0 to +3V
HBS, LBS Pulse Width[1]	All	500ns min	500ns min	HBS, LBS: 0 to +3V
Serial Clock Frequency[1]	All	1MHz max	1MHz max	
HBS, LBS Data Set Up[2]	All	250ns min	250ns min	
Data Hold Time[3]	All	500ns min, 200ns typ	500ns min	
POWER REQUIREMENTS				
I_{DD}	All	2mA max		In Quiescent State
I_{CC}	All	2mA max		In Quiescent State

NOTES
[1] Guaranteed by design. Not tested.
[2] Data setup time is the minimum amount of time required for DB0 - DB9 to be stable prior to strobing HBS, LBS.
[3] Data hold time is the minimum amount of time required for DB0 - DB9 to be stable after strobing HBS, LBS.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{REF} to GND . . . . . ±25V
V_{DD} to GND . . . . . +17V
V_{CC} to GND . . . . . +17V
V_{CC} to V_{DD} . . . . . +0.4V
Output Voltage (pins 6 & 7) . . . . . −0.3V to V_{DD}
Operating Temperature
JN, KN, LN versions . . . . . 0 to +70°C
JD, KD, LD versions . . . . . −25°C to +85°C
SD, TD, UD versions . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation (Package)
Up to +50°C:
Plastic (Suffix N) 1200mW
Ceramic (Suffix D) 1000mW
Derate Above +50°C by
Plastic (Suffix N) . . . . . 12mW/°C
Ceramic (Suffix D) . . . . . 10mW/°C
Digital Input Voltage Range . . . . . V_{DD} to GND

CAUTION:

1. Do not apply voltages higher than V_{CC} to SRO.
2. Do not apply voltages higher than V_{DD} or less than GND to any other input/output terminal except V_{REF}, R_{FB1} or R_{FB2}.
3. The digital control inputs are zener protected, however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
4. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

TERMINOLOGY

RESOLUTION

Value of the LSB. For example, a unipolar n-bit converter has a resolution of (2^{-n}) (V_{REF}). A bipolar n-bit converter has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

GAIN

The "gain" of a converter is that analog scale factor setting that establishes the nominal conversion relationship, e.g., 10V full scale. It is a linear error which can be externally adjusted (see gain adjustment on next page).

OUTPUT LEAKAGE CURRENT

Current which appears on the OUT1 terminal when the DAC register is loaded with all "0's" or on the OUT2 terminal when the DAC register is loaded with all "1's."

DAC CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7522's DAC functional block consists of a highly stable Silicon Chromium thin film R-2R ladder, and ten SPDT N-channel current steering switches. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used — that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

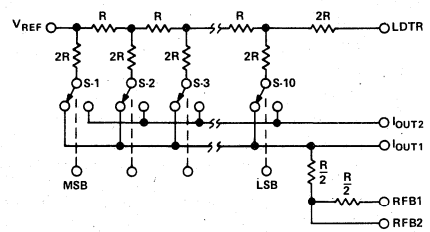


Figure 1. DAC Functional Diagram

EQUIVALENT CIRCUIT

The DAC equivalent circuit is shown in Figure 2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the $I_{REF}/1024$ current source represents the 1LSB of current lost through the ladder termination resistor to ground. The C_{OUT1} and C_{OUT2} output capacitances are as shown when the DAC latches feed the DAC with all "1's." If the DAC latches are loaded with all "0's," C_{OUT1} is 37pF, while C_{OUT2} is 120pF. In addition, C_{SD} is replaced by 10 ohms, and the 10 ohm R_{ON} in I_{OUT1} is replaced by a C_{SD} of 10pF. When fast amplifiers are used, it will be necessary to provide phase compensation (in the form of feedback capacitance) to cancel the pole formed by $R_{FEEDBACK}$ and C_{OUT} if stability is to be maintained.

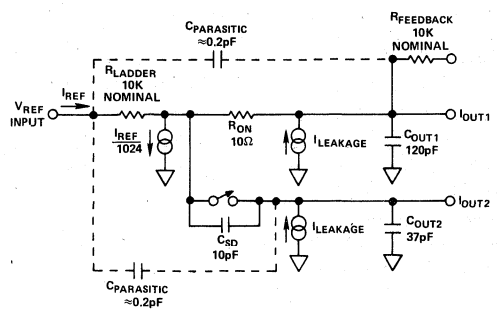


Figure 2. Equivalent Circuit (Shown for all Digital Inputs High)

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	V_{DD}	+15V (nominal) Main Supply.
2	LDTR	R-2R Ladder Termination Resistor. Normally grounded for unipolar operation or terminated at I_{OUT2} for bipolar operation.
3	V_{REF}	Reference Voltage Input. Since the AD7522 is a multiplying DAC, V_{REF} may vary over the range of ±10V.
4	RFB2	$R_{FEEDBACK} \div 2$; gives full scale equal to $V_{REF}/2$.
5	RFB1	$R_{FEEDBACK}$, used for normal unity gain (at full scale) D/A conversion.
6	I_{OUT1}	DAC Current OUT1 Bus. Normally terminated at virtual ground of output amplifier.
7	I_{OUT2}	DAC Current OUT2 Bus, terminated at ground for unipolar operation, or virtual ground of op amp for bipolar operation.
8	AGND	Analog Ground. Back gate of DAC N-channel SPDT current steering switches.
9	SRO	Serial Output. An auxiliary output for recovering data in the input buffer.
10	DB9	Data Bit 9. Most significant parallel data input.
11	DB8	Data Bit 8.
12	DB7	Data Bit 7.
13	DB6	Data Bit 6.
14	DB5	Data Bit 5.
15	DB4	Data Bit 4.
16	DB3	Data Bit 3.
17	DB2	Data Bit 2.
18	DB1	Data Bit 1.
19	DB0	Data Bit 0. Least significant parallel data input.
20	$\overline{SC8}$	8-Bit Short Cycle Control. When in serial mode, if $\overline{SC8}$ is held to Logic "0", the two least significant input latches in the input buffer are bypassed to provide proper serial loading of 8-bit serial words. If $\overline{SC8}$ is held to Logic "1", the AD7522 will accept a 10-bit serial word. Data bits 0 (LSB) and DB1 are in a parallel load mode when $\overline{SC8}$ = 0 and should be tied to a logic low state to prevent false data from being loaded.
21	SPC	Serial/Parallel Control. If SPC is a Logic "0", the AD7522 will load parallel data appearing on DB0 through DB9 into the input buffer when the appropriate strobe inputs are exercised (see HBS and LBS). If SPC is a Logic "1", the AD7522 will load serial data appearing on Pin 26 into the input buffers. Each serial data bit must be "strobed" into the buffer with the HBS and LBS.
22	LDAC	Load DAC: When LDAC is a Logic "0", the AD7522 is in the "hold" mode, and digital activity in the input buffer is locked out. When LDAC is a Logic "1", the AD7522 is in the "load" mode, and data in the input buffer loads the DAC register.
23	NC	No Connection.
24	LBS	Low Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB0 (LSB) through DB7 inputs will be "clocked" into the input buffer on the positive going edge of the LBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edge of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
25	HBS	High Byte Strobe. When in "parallel load" mode (SPC = 0), parallel data appearing on the DB9 (MSB) and DB8 data inputs will be "clocked" into the input buffer on the positive going edge of HBS. When in "serial load" mode (SPC = 1), serial data bits appearing at the serial input terminal, Pin 26, will be "clocked" into the input buffer on the positive going edges of HBS and LBS. (HBS and LBS must be clocked simultaneously when in "serial load" mode.)
26	SRI	Serial Input.
27	V_{CC}	Logic Supply. If +5V is applied, all digital inputs/outputs are TTL compatible. If +10V to +15V is applied, digital inputs/outputs are CMOS compatible.
28	DGND	Digital Ground

Note 1

Note 1: Logic "1" applied to a data bit steers that bit's current to the I_{OUT1} terminal.

APPLICATIONS

(Note: Protection Schottky CR3 in Figure 3 and CR3, CR4 in Figure 4 are not required when using TRI-FET amps such as the AD542 or AD544).

UNIPOLAR OPERATION

Figure 3 shows the analog circuit connections required for unipolar operation. The input code/output voltage relationship is shown in Table I.

Zero Offset Adjustment

1. Adjust the op amp's offset potentiometer for $<$1mV on the amplifier junction.

Gain Adjustment

1. Set R1 and R2 to 0Ω. Load the DAC register with all "1's."
2. If analog out is greater than $-V_{REF}$, increase R1 for required full scale output. If analog out is less than $-V_{REF}$, increase R2 for required full scale output.

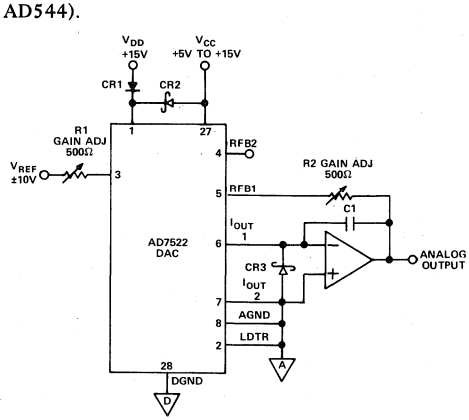


Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-10})$
1000000001	$-V_{REF}\ (1/2 + 2^{-10})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}\ (1/2 - 2^{-10})$
0000000001	$-V_{REF}\ (2^{-10})$
0000000000	0

Table I. Unipolar Code Table

BIPOLAR OPERATION

Figure 4 shows the analog circuit connections required for bipolar operation. The input code/ouput voltage relationship is shown in Table II.

Zero Offset Adjustment

1. Adjust the offset potentiometer of amplifier A1 and A2 for <1mV on the respective summing junctions. If the analog out for code 1000000000 is not zero, sum current into or out of the summing junction of A1 for 0V at analog out.

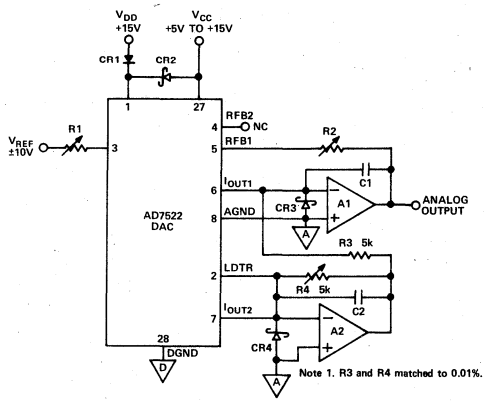


Figure 4. Bipolar Operation

Gain Adjustment

1. Load the DAC register with all "0's." Set R1 and R2 to 0Ω.
2. If analog out is greater than $+V_{REF}$, increase R2 until it reads precisely $+V_{REF}$. If analog out is less than $+V_{REF}$, increase R1 until it reads precisely V_{REF}.

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}\ (1 - 2^{-9})$
1000000001	$-V_{REF}\ (2^{-9})$
1000000000	0
0111111111	$V_{REF}\ (2^{-9})$
0000000001	$V_{REF}\ (1 - 2^{-9})$
0000000000	V_{REF}

Table II. Bipolar Code Table

SINGLE BYTE PARALLEL LOADING

Figure 5 illustrates the logic connections for loading single byte parallel data into the input buffer. DB0 should be grounded on "K" and "T" versions, and DB0 and DB1 should be grounded on "J" and "S" versions for monotonic operation of the DAC. DB9 is always the MSB, whether 8-bit, 9-bit, or 10-bit linear AD7522's are used.

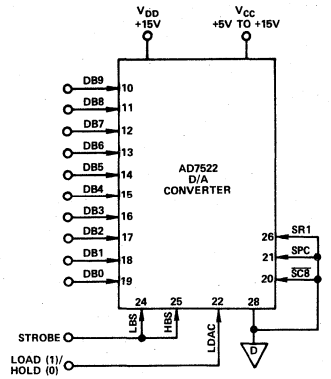


Figure 5. Single Byte Parallel Loading

When data is stable on the parallel inputs (DB0-DB9), it can be transferred into the input buffer on the positive edge of the strobe pulse.

Data is transferred from the input buffer to the DAC register when LDAC is a Logic "1." LDAC is a level-actuated (versus edge-triggered) function and must be held "high" at least 0.5μs for data transfer to occur.

TWO BYTE PARALLEL LOADING

Figures 6 and 7 show the logic connections and timing requirements for interfacing the AD7522 to an 8-bit data bus for two byte loading of a 10-bit word.

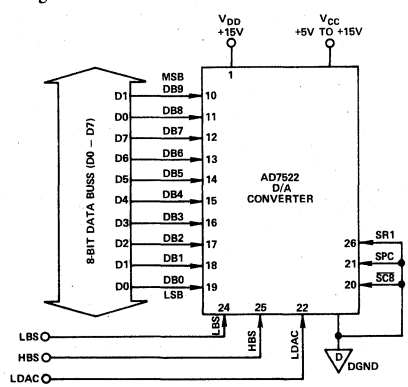


Figure 6. Two Byte Parallel Loading

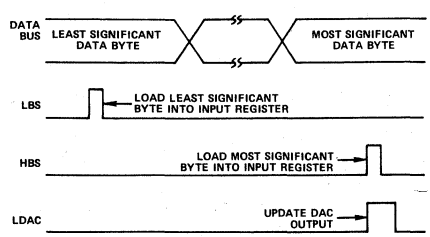


Figure 7. Timing Diagram

First, the least significant data byte (DB0 through DB7) is loaded into the input buffer on the positive edge of LBS. Subsequently, the data bus is used for status indication and

instruction fetching by the CPU. When the most significant data byte (DB8 and DB9) is available on the bus, the input buffer is loaded on the positive edge of HBS. The DAC register updates to the new 10-bit word when LDAC is "high." LDAC may be exercised coincident with, or at any time after HBS loads the second byte of data into the input buffer.

SERIAL LOADING

Figure 8 and Figure 9 show the connections and timing diagram for serial loading.

To load a 10-bit word ($\overline{SC8}$ = 1), HBS and LBS must be strobed simultaneously with exactly 10 positive edges to clock the serial data into the input buffer. For 8-bit words ($\overline{SC8}$ = 0), only 8 positive edges are required.

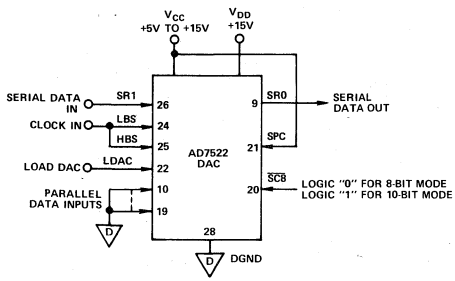


Figure 8. Serial 8- and 10-Bit Loading (Analog Outputs Not Shown for Clarity)

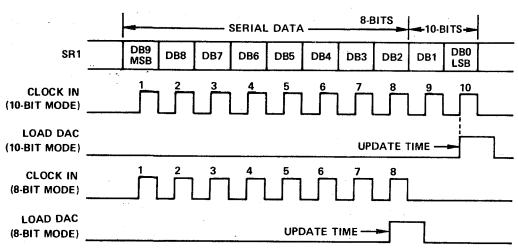


Figure 9. Timing Diagram for Serial 8- and 10-Bit Loading

APPLICATION HINTS

1. CR1 and CR2 on Figures 3 and 4 protect the AD7522 against latch-up V_{CC} exceeds V_{DD}, and may be omitted if V_{DD} and V_{CC} are driven from the same voltage.
2. Diodes CR3 on Figure 3 and CR3 and CR4 on Figure 4 clamp the amplifier junction to -300mV if they attempt to swing negative during power up or power down. The input structures of some high-speed op amps can supply substantial current under the transient conditions encountered during power sequencing. It is recommended that the PC layout be able to accommodate the diodes.
3. Fast op amps will require phase compensation for stability due to the pole formed by C_{OUT1} or C_{OUT2} and $R_{FEEDBACK}$.
4. During serial loading, all data inputs (DB0 through BD9), should be grounded.

ANALOG DEVICES

CMOS 8-Bit Multiplying D/A Converter

AD7523

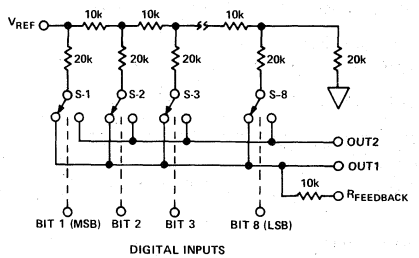
FEATURES

- Low Cost
- Fast Settling: 100ns
- Low Power Dissipation
- Low Feedthrough: ½LSB @ 200kHz
- Full Four-Quadrant Multiplying

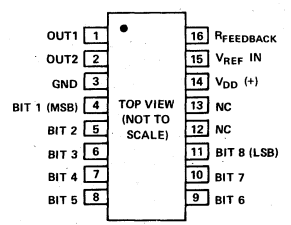
APPLICATIONS

- Battery Operated Equipment
- Low Power, Ratiometric A/D Converters
- Digitally Controlled Gain Circuits
- Digitally Controlled Attenuators
- CRT Character Generation
- Low Noise Audio Gain Control

AD7523 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7523 is a low cost, monolithic multiplying digital-to-analog converter packaged in a 16-pin DIP. The device uses an advanced monolithic, thin-film-on-CMOS technology to provide 8-bit resolution with accuracy to 10-bits and very low power dissipation.

The AD7523's excellent multiplying characteristics and low cost allow it to be used in a wide ranging field of applications such as: low noise audio gain control, CRT character generation, motor speed control, digitally controlled attenuators, etc.

ORDERING INFORMATION

Model	Linearity	Package	Operating Temperature Range	Package Identification[1]
AD7523JN	±1/2LSB	16 pin Plastic	0 to +70°C	N16B
AD7523KN	±1/4LSB			
AD7523LN	±1/8LSB			

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = T_{min} to T_{max}	TEST CONDITION
STATIC ACCURACY			
Resolution	8 Bits min	8 Bits min	
Nonlinearity[1]			
AD7523JN	±1/2LSB max (±0.2% FSR max)	±1/2LSB max (±0.2% FSR max)	V_{OUT1} = V_{OUT2} = 0V
AD7523KN	±1/4LSB max (±0.1% FSR max)	±1/4LSB max (±0.1% FSR max)	
AD7523LN	±1/8LSB max (±0.05% FSR max)	±1/8LSB max (±0.05% FSR max)	
Monotonicity	Guaranteed over T_{min} to T_{max}		V_{OUT1} = V_{OUT2} = 0V
Gain Error[1,2,3]	-1.5% of FSR min, +1.5% of FSR max	-1.8% of FSR min, +1.8% of FSR max	Digital Inputs = V_{INH}
Power Supply Rejection (Gain)[1,2]	0.02% per % max	0.03% per % max	V_{DD} = +14V to +15V Digital Inputs = V_{INH}
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INL}
I_{OUT2} (pin 2)	±50nA max	±200nA max	V_{OUT1} = V_{OUT2} = 0V, V_{REF} = ±10V Digital Inputs = V_{INH}
DYNAMIC PERFORMANCE			
Output Current			
Settling Time[4]	150ns max	200ns max	To 0.2% FSR, Load = 100Ω Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error[4]	±1/2LSB max	±1LSB max	Digital Inputs = V_{INL} V_{REF} = 20V p-p, 200kHz sinewave
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max		V_{OUT1} = V_{OUT2} = 0V
Temperature Coefficient		-500ppm/°C max	
ANALOG OUTPUTS[4]			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max	100pF max	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	30pF max	30pF max	
C_{OUT1} (pin 1)	30pF max	30pF max	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max	100pF max	
DIGITAL INPUTS			
Logic Thresholds			
V_{INH}	+14.5V min	+14.5V min	
V_{INL}	+0.5V max	+0.5V max	
Input Leakage Current			
I_{IN} (per input)	±1μA max	±1μA max	V_{IN} = 0V or +15V
Input Capacitance			
C_{IN}[4]	4pF max	4pF max	
Input Coding	Unipolar Binary of Offset Binary (see next page)		
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Device Functionality. Accuracy is tested and guaranteed only at V_{DD} = +15V
I_{DD}	100μA max	100μA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor, Full Scale Range (FSR) is equal to (V_{REF} - 1LSB) in the unipolar circuit on the next page.
[3] Max gain change from +25°C to T_{min} or T_{max} is ±0.3% FSR.
[4] Guaranteed by design. Not subject to test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0V, +17V
V_{REF} to GND . . . . . ±25V
Digital Input Voltage (V_{IN}) to GND . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . . . . . -0.3V to V_{DD}

Power Dissipation (package)
To +70°C 670mW
Derate Above +70°C by . . . . . 8.3mW/°C
Operating Temperature . . . . . 0 to +70°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7523 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figure 1 and 2. Protection diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BASIC OPERATION

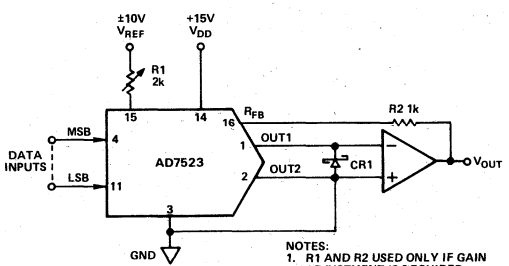


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table I. Unipolar Binary Code Table

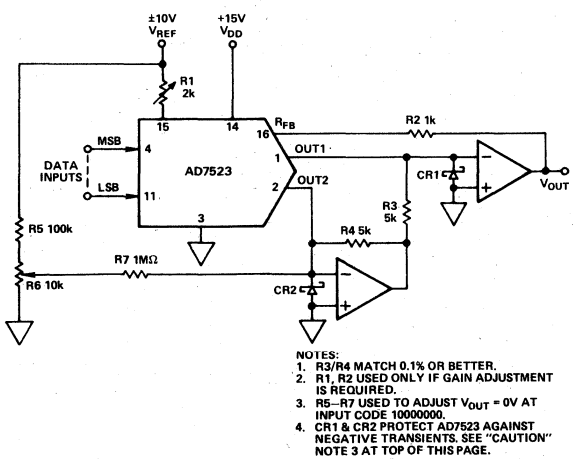


Figure 2. Bipolar (4-Quadrant) Operation

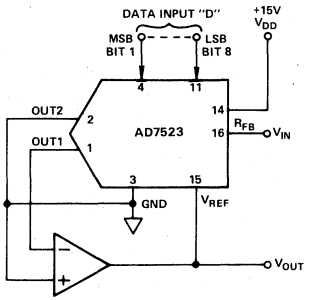
DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table II. Bipolar (Offset Binary) Code Table

APPLICATIONS

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$$V_{OUT} = -\frac{V_{IN}}{D}$$

$$A_V = \frac{V_{OUT}}{V_{IN}} = -\frac{1}{D}$$ where: A_V = Voltage Gain

and where:

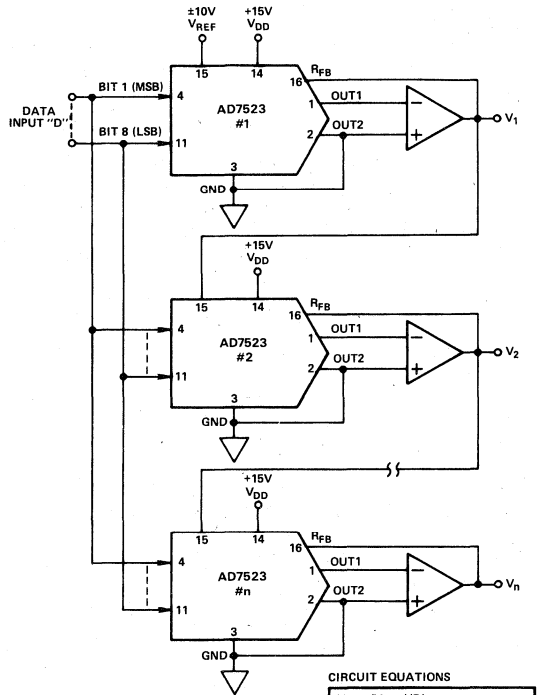
$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \frac{BIT\ 8}{2^8}$$

(BIT N = 1 or 0)

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)
D = 00000001, $A_V = -256$
D = 10000000, $A_V = -\frac{256}{128} = -2$
D = 11111111, $A_V = -\frac{256}{255}$

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$
$V_2 = +(V_{REF})(D^2)$
$V_n = -(V_{REF})(D^n)$, n an odd integer
$V_n = +(V_{REF})(D^n)$, n an even integer

ANALOG DEVICES

CMOS 8-Bit Buffered Multiplying DAC

AD7524

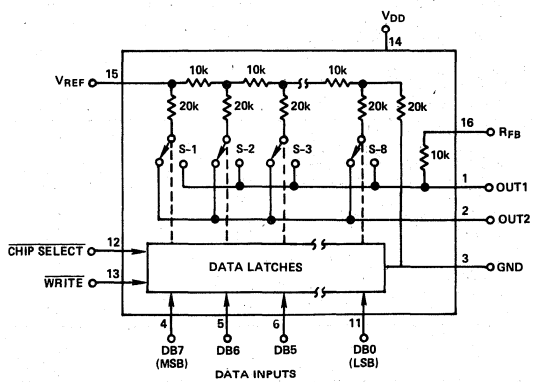
FEATURES

Microprocessor Compatible (6800, 8085, Z80, Etc.)
TTL/CMOS Compatible Inputs
On-Chip Data Latches
End Point Linearity
Low Power Consumption
Monotonicity Guaranteed (Full Temperature Range)
Latch Free (No Protection Schottky Required)

APPLICATIONS

Microprocessor Controlled Gain Circuits
Microprocessor Controlled Attenuator Circuits
Microprocessor Controlled Function Generation
Precision AGC Circuits
Bus Structured Instruments

AD7524 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The AD7524 is a low cost, 8-bit monolithic CMOS DAC designed for direct interface to most microprocessors.

Basically an 8-bit DAC with input latches, the AD7524's load cycle is similar to the "write" cycle of a random access memory. Using an advanced thin-film on CMOS fabrication process, the AD7524 provides accuracy to 1/8LSB with a typical power dissipation of less than 10 milliwatts.

A newly improved design eliminates the protection Schottky previously required and guarantees TTL compatibility when using a +5V supply. Loading speed has been increased for compatibility with most microprocessors.

Featuring operation from +5V to +15V, the AD7524 interfaces directly to most microprocessor buses or output ports. Excellent multiplying characteristics (2- or 4-quadrant) make the AD7524 an ideal choice for many microprocessor controlled gain setting and signal control applications.

PACKAGE IDENTIFICATION[1]

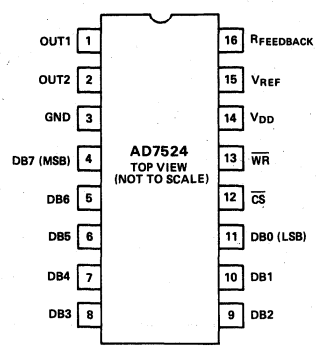
Suffix "D": Ceramic DIP – (D16B)
Suffix "N": Plastic DIP – (N16B)

[1] See Section 19 for package outline information.

ORDERING INFORMATION

Nonlinearity (V_{DD} = +5V to +15V)	Temperature Range and Package: Plastic 0 to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
±1/2 LSB	AD7524JN	AD7524AD	AD7524SD
±1/4 LSB	AD7524KN	AD7524BD	AD7524TD
±1/8 LSB	AD7524LN	AD7524CD	AD7524UD

PIN CONFIGURATION



SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

PARAMETER	LIMIT, T_A = +25°C V_{DD} = +5V	LIMIT, T_A = +25°C V_{DD} = +15V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = 5V	LIMIT, T_{MIN}, T_{MAX}[1] V_{DD} = +15V	UNITS	TEST CONDITIONS/COMMENTS
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy						
AD7524JN, AD, SD	±0.2	±0.2	±0.2	±0.2	% FSR max	
AD7524KN, BD, TD	±0.2	±0.1	±0.2	±0.1	% FSR max	
AD7524LN, CD, UD	±0.2	±0.05	±0.2	±0.05	% FSR max	
Monotonicity	guaranteed	guaranteed	guaranteed	guaranteed		
Gain Error[2]	±1.0	±0.5	±1.4	±0.6	% FSR max	
Average Gain TC[3]	±0.004	±0.001	±0.004	±0.001	% FSR/°C	Gain TC measured from +25°C to T_{min} or from +25°C to T_{max}
dc Supply Rejection,[3] $\Delta Gain/\Delta V_{DD}$	0.08 0.002	0.02 0.001	0.16 0.01	0.04 0.005	% FSR/% max % FSR/% typ	ΔV_{DD} = ±10%
Output Leakage Current						
I_{OUT1} (Pin 1)	±50	±50	±400	±200	nA max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
I_{OUT2} (Pin 2)	±50	±50	±400	±200	nA max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V; V_{REF} = ±10V
DYNAMIC PERFORMANCE						
Propagation Delay[3] (From digital input to 90% of final analog output current)						
AD7524JN, KN, LN, AD, BD, CD	150	65	175	80	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ =
AD7524SD, TD, UD	150	65	200	90	ns max	0V; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.
Output Current Settling Time[3] (to 1/2 LSB)	150	100	200	150	ns max	OUT1 Load = 100Ω, C_{EXT} = 13pF; $\overline{WR}$, $\overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} to 0V.
ac Feedthrough[3]						
at OUT1	0.25	0.25	0.5	0.5	% FSR max	V_{REF} = ±10V, 100kHz sine wave; DB0–DB7 =
at OUT2	0.25	0.25	0.5	0.5	% FSR max	0V; $\overline{WR}$, $\overline{CS}$ = 0V
REFERENCE INPUT						
R_{IN} (pin 15 to GND)[4]	5 20	5 20	5 20	5 20	kΩ min kΩ max	
ANALOG OUTPUTS						
Output Capacitance[3]						
C_{OUT1} (pin 1)	120	120	120	120	pF max	DB0–DB7 = V_{DD}; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	30	30	30	30	pF max	
C_{OUT1} (pin 1)	30	30	30	30	pF max	DB0–DB7 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT2} (pin 2)	120	120	120	120	pF max	
DIGITAL INPUTS						
Input HIGH Voltage Requirement						
V_{IH}	+2.4	+13.5	+2.4	+13.5	V min	
Input LOW Voltage Requirement						
V_{IL}	+0.8	+1.5	+0.8	+1.5	V max	
Input Current						
I_{IN}	±1	±1	±10	±10	μA max	V_{IN} = 0V or V_{DD}
Input Capacitance[3]						
DB0–DB7	5	5	5	5	pF max	V_{IN} = 0V
$\overline{WR}$, $\overline{CS}$	20	20	20	20	pF max	V_{IN} = 0V
SWITCHING CHARACTERISTICS						
Chip Select to Write Setup Time[5]						See timing diagram
t_{CS}						t_{WR} = t_{CS}
AD7524JN, KN, LN, AD, BD, CD	170	100	220	130	ns min	
AD7524SD, TD, UD	170	100	240	150	ns min	
Chip Select to Write Hold Time						
t_{CH}						
All Grades	0	0	0	0	ns min	
Write Pulse Width						
t_{WR}						$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
AD7524JN, KN, LN, AD, BD, CD	170	100	220	130	ns min	
AD7524SD, TD, UD	170	100	240	150	ns min	
Data Setup Time						
t_{DS}						
AD7524JN, KN, LN, AD, BD, CD	135	60	170	80	ns min	
AD7524SD, TD, UD	135	60	170	100	ns min	
Data Hold Time						
t_{DH}						
All Grades	10	10	10	10	ns min	
POWER SUPPLY						
I_{DD}	1	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
	100	100	500	500	μA max	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: AD7524JN, KN, LN; 0 to +70°C
AD7524AD, BD, CD; −25°C to +85°C
AD7524SD, TD, UD; −55°C to +125°C

[2] Gain error is measured using internal feedback resistor. Ideal Full Scale Range (FSR) = (V_{REF} −1LSB) as shown in Table I.

[3] Guaranteed, not tested.

[4] DAC thin-film resistor temperature coefficient is approximately −300ppm/°C.

[5] AC parameter, sample tested @ 25°C to ensure conformance to specifications.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
V_{RFB} to GND . . . . . ±25V
V_{REF} to GND . . . . . ±25V
Digital Input Voltage to GND . . . . . -0.3V to V_{DD}
V_{OUT1}, V_{OUT2} (pin 1, pin 2) to GND . . . . . -0.3V to V_{DD}
Power Dissipation (package)
Plastic (N Suffix)
To +70°C 670mW
Derate above +70°C by . . . . . 8.3mW/°C
Ceramic (D Suffix)
To +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (JN, KN, LN) Grades . . . . . 0 to +70°C
Industrial (AQ, BD, CD) Grades . . . . . -25°C to +85°C
Extended (SD, TD, UD) Grades . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. Do not insert this device into powered sockets. Remove power before insertion or removal.

9

TERMINOLOGY

RELATIVE ACCURACY: A measure of the deviation from a straight line through the end points of the DAC transfer function. Normally expressed as a percentage of full scale range. For the AD7524 DAC, this holds true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

PROPAGATION DELAY: Time required for the output current to reach 90% of its final value from a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's full scale output voltage to the ideal output voltage. Ideal full scale output is V_{REF} - 1LSB. Gain error is adjustable to zero.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from OUT1 and OUT2 terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on OUT1 terminal with all digital inputs LOW or on OUT2 terminal when all inputs are HIGH. This is an error current which contributes an offset voltage at the amplifier output.

CIRCUIT DESCRIPTION

CIRCUIT INFORMATION

The AD7524, an 8-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and eight N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

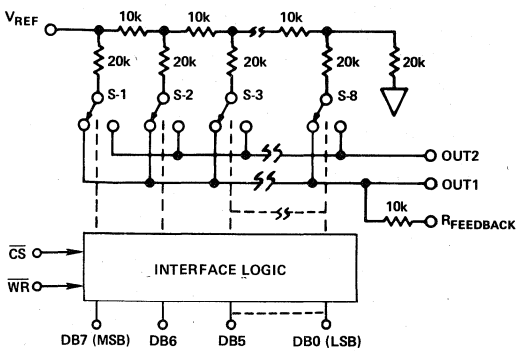


Figure 1. AD7524 Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuit for all digital inputs LOW is shown in Figures 2. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{1}{256}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switches is 120pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 30pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs high is similar to Figure 2 however, the "ON" switches are now on terminal OUT1, hence the 120pF appears at that terminal.

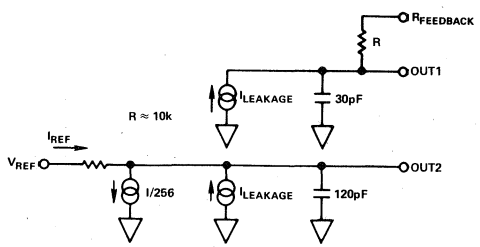


Figure 2. AD7524 DAC Equivalent Circuit – All Digital Inputs Low

INTERFACE LOGIC INFORMATION

MODE SELECTION

AD7524 mode selection is controlled by the $\overline{CS}$ and $\overline{WR}$ inputs.

WRITE MODE

When $\overline{CS}$ and $\overline{WR}$ are both LOW, the AD7524 is in the WRITE mode, and the AD7524 analog output responds to data activity at the DB0–DB7 data bus inputs. In this mode, the AD7524 acts like a nonlatched input D/A converter.

HOLD MODE

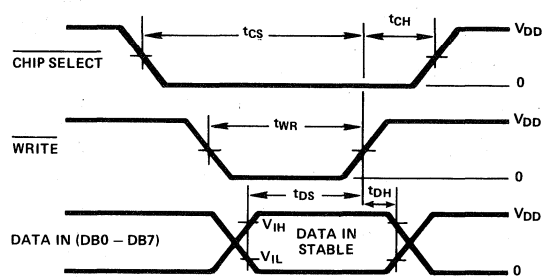
When either $\overline{CS}$ or $\overline{WR}$ is HIGH, the AD7524 is in the HOLD mode. The AD7524 analog output holds the value corresponding to the last digital input present at DB0–DB7 prior to $\overline{WR}$ or $\overline{CS}$ assuming the HIGH state.

MODE SELECTION TABLE

$\overline{CS}$	$\overline{WR}$	MODE	DAC RESPONSE
L	L	Write	DAC responds to data bus (DB0 – DB7) inputs
H	X	Hold	Data bus (DB0 – DB7) is locked out;
X	H	Hold	DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed HIGH state.

L = Low State, H = High State, X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. All input signal rise and fall times measured from 10% to 90% of V_{DD}. V_{DD} = +5V, $t_r = t_f$ = 20ns; V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. Timing Measurement Reference level is $\frac{V_{IH} + V_{IL}}{2}$
3. $t_{DS} + t_{DH}$ is approximately constant at 145ns min at +25°C, V_{DD} = +5V and t_{wr} = 170ns min. The AD7524 is specified for a minimum t_{DH} of 10ns, however, in applications where $t_{DH} > 10$ns, t_{DS} may be reduced accordingly up to the limit t_{DS} = 65ns, t_{DH} = 80ns.

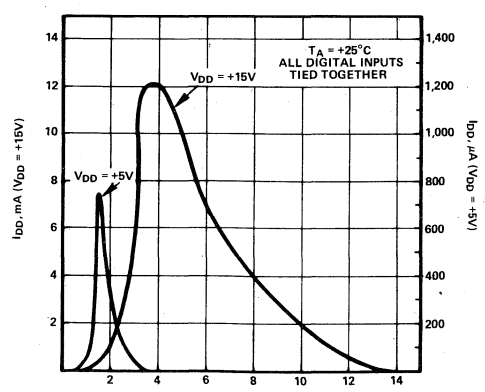


Figure 3. Supply Current vs. Logic Level

Typical plots of supply current, I_{DD}, versus logic input voltage, V_{IN}, for V_{DD} = +5V and V_{DD} = +15V are shown above.

ANALOG CIRCUIT CONNECTIONS

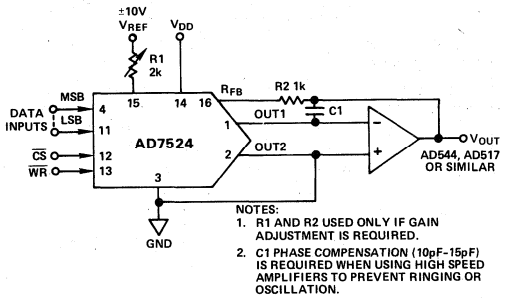


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

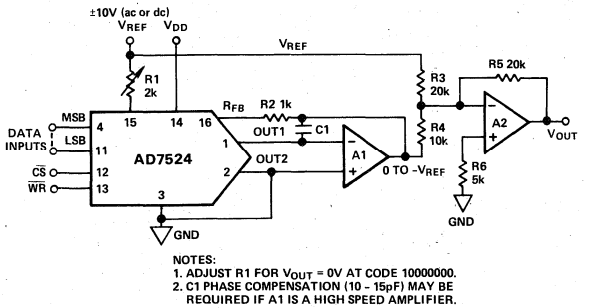


Figure 5. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$-V_{REF}\left(\frac{255}{256}\right)$
10000001		$-V_{REF}\left(\frac{129}{256}\right)$
10000000		$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111		$-V_{REF}\left(\frac{127}{256}\right)$
00000001		$-V_{REF}\left(\frac{1}{256}\right)$
00000000		$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{REF}) = \frac{1}{256}(V_{REF})$

Table I. Unipolar Binary Code Table

DIGITAL INPUT MSB	LSB	ANALOG OUTPUT
11111111		$+V_{REF}\left(\frac{127}{128}\right)$
10000001		$+V_{REF}\left(\frac{1}{128}\right)$
10000000		0
01111111		$-V_{REF}\left(\frac{1}{128}\right)$
00000001		$-V_{REF}\left(\frac{127}{128}\right)$
00000000		$-V_{REF}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{REF}) = \frac{1}{128}(V_{REF})$

Table II. Bipolar (Offset Binary) Code Table

MICROPROCESSOR INTERFACE

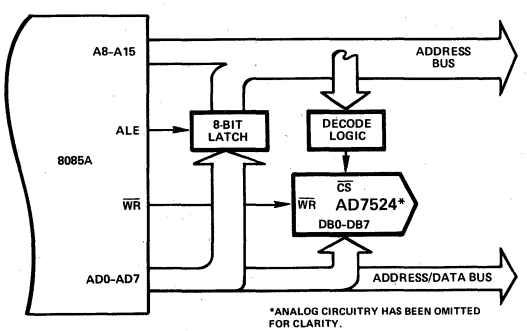


Figure 6. AD7524/8085A Interface

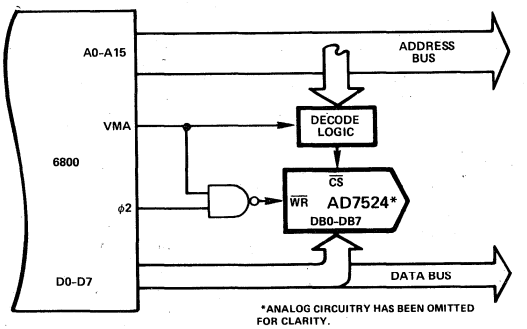
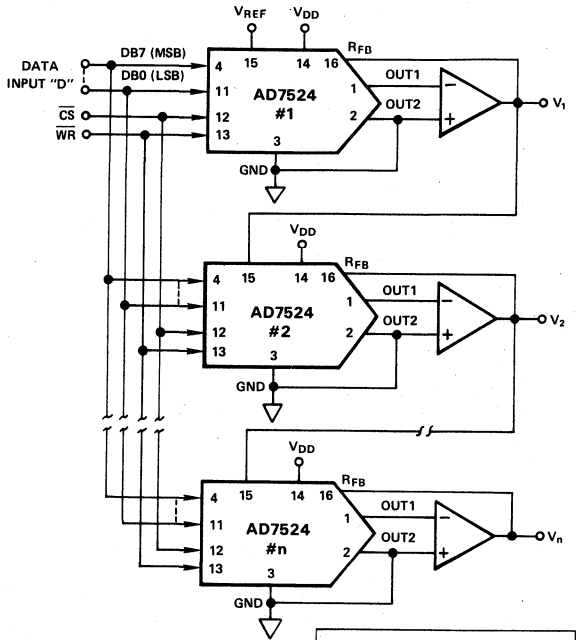


Figure 7. AD7524/MC6800 Interface

POWER GENERATION



CIRCUIT EQUATIONS

$V_1 = -(V_{REF})(D)$

$V_2 = +(V_{REF})(D^2)$

$V_n = -(V_{REF})(D^n)$, n an odd integer

$V_n = +(V_{REF})(D^n)$, n an even integer

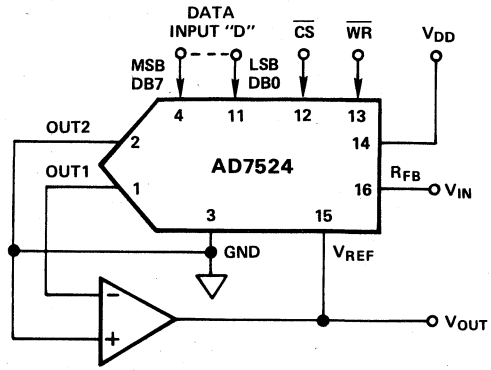
WHERE:

$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$

and

DB_n = 1 or 0

DIVIDER (DIGITALLY CONTROLLED GAIN)



EQUATIONS

$V_{OUT} = \frac{-V_{IN}}{D}$

$A_V = \frac{-V_{OUT}}{V_{IN}} = -\frac{1}{D}$ WHERE: A_V = VOLTAGE GAIN

and where:

$D = \frac{DB7}{2^1} + \frac{DB6}{2^2} + \ldots \frac{DB0}{2^8}$

DB_N = 1 or 0

EXAMPLES

D = 00000000, $A_V = -A_{OL}$ (OP AMP)

D = 00000001, $A_V = -256$

D = 10000000, $A_V = -\frac{256}{128} = -2$

D = 11111111, $A_V = -\frac{256}{255}$

3½ Digit BCD Monolithic CMOS Digitally Controlled Potentiometer

AD7525

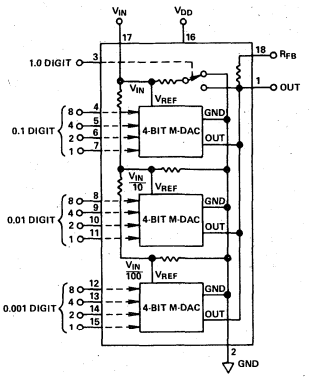
FEATURES

Resolution: 3 1/2 Digit BCD (1999 Counts)
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Gain Error: ±0.05% FS
Excellent Repeatability Accuracy
Low Power Dissipation

APPLICATIONS

Thumbwheel Switch Voltage Dividers
Digitally Controlled Gain Circuits
Digitally Controlled Attenuators
BCD Multiplying DACs
Low Power Converters

AD7525 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7525 is a monolithic CMOS 3½ digit BCD digitally controlled potentiometer designed for precision incremental voltage-divider applications.

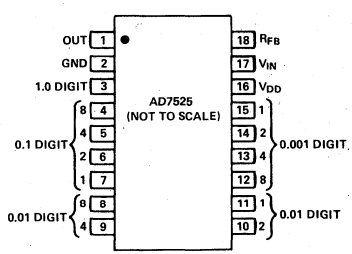
With the addition of an external op amp, the output can be digitally controlled from 0 to 1.999V_{IN} with resolution of 0.001V_{IN}.

AC or DC voltage up to ±10V can be applied to the input providing high application flexibility in fields such as audio gain control, etc.

Digital control, excellent repeatability and 0.05% accuracy make the AD7525 an ideal replacement for 10-turn potentiometers or thumbwheel switch voltage dividers using discrete resistor networks.

Packaged in an 18-pin DIP, the AD7525 uses an advanced CMOS fabrication process combined with wafer laser trimming.

PIN CONFIGURATION



18-PIN DIP
TOP VIEW

ORDERING INFORMATION

Package and Temperature	Nonlinearity ±1/2LSB	Nonlinearity ±1LSB
18-Pin Plastic 0 to +70°C	AD7525LN	AD7525KN
18-Pin Ceramic -25°C to +85°C	AD7525CD	AD7525BD
18-Pin Ceramic -55°C to +125°C	AD7525UD	AD7525TD

PACKAGE IDENTIFICATION[1]

Suffix "N": Plastic DIP – (N18B)
Suffix "D": Ceramic DIP – (D18B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +15V; V_{PIN1} = 0V; V_{IN} = +10V unless otherwise stated)

PARAMETER	T_A = +25°C	T_A = Operating Temperature Range	CONDITION
ACCURACY			
Resolution[1]	1 part in 2000	1 part in 2000	
Nonlinearity[2]			
AD7525KN, BD, TD	±1LSB max	±1LSB max	BCD 0.000 to 1.999
AD7525LN, CD, UD	±1/2LSB max	±1/2LSB max	BCD 0.000 to 1.999
Gain Error[3]	±0.05% FS typ	–	BCD = 1.999
Gain TC	±25ppm/°C max	–	BCD = 1.999
Output Leakage Current (pin 1)	100nA max	400nA max	BCD = 0.0000
DYNAMIC PERFORMANCE			
Switching Time	1μs max[4]	1μs max[5]	V_{IN} = +5V, R_{OUT} (pin 1) = 100Ω, Digital Inputs = V_{IL} to V_{IH} or V_{IL}, V_{PIN1} measured from 10% to 90%
Feedthrough Error	±0.05%V_{IN} max[5]	±0.1%V_{IN}[5]	V_{IN} = ±10V, 20kHz sinewave
ANALOG INPUT			
Input Resistance (pin 17)[6]	2kΩ min/10kΩ max	2kΩ min/10kΩ max	
V_{IN} Range (recommended)	±10V max	±10V max	
ANALOG OUTPUT			
Output Capacitance			
C_{OUT} (pin 1)	60pF max[5]	60pF max[5]	Digital Inputs = BCD 0000
	200pF max[5]	200pF max[5]	Digital Inputs = BCD 1999
R_{FB} Resistance (pin 18 to pin 1)[6]	8kΩ min/40kΩ max	8kΩ min/40kΩ max	
DIGITIAL INPUTS			
Input HIGH Voltage			
V_{IH}	+14.5V min	+14.5V min	
Input LOW Voltage			
V_{IL}	+0.5V max	+0.5V max	
Input Leakage Current	±1μA max	±10μA max	Digital Input = 0V or V_{DD}
Input Capacitance	5pF max[5]	5pF max[5]	
Input Coding	3½ Digit BCD (1999 Counts)	3½ Digit BCD (1999 Counts)	
POWER SUPPLY			
V_{DD} Range	+5V to +17V	+5V to +17V	Functional with Degraded Performance
V_{DD}	+15V ±5%	+15V ±5%	Rated Accuracy
I_{DD}	500μA max	1mA max	Digital Inputs = V_{IL} or V_{IH}

NOTES
[1] Commercial devices are sample tested over temperature.
[2] Monotonicity is guaranteed on the AD7525LN, CD and UD versions over T_{min} to T_{max}.
[3] Gain Error is measured using the AD7525 internal feedback resistor. FS is "Full Scale" (BCD = 1.999).
[4] AC parameter, sample tested at +25°C to ensure conformance to specification.
[5] Guaranteed, not tested.
[6] Thin-Film resistor temperature coefficient is approximately -300ppm/°C.
Specifications subject to change without notice.

CAUTION

1. ESD (electro-static discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.
2. Do not apply voltages more negative than GND or more positive than V_{DD} to any pin except V_{IN} (pin 17) and R_{FB} (pin 18).
3. The inputs of some IC amplifiers (especially high speed types) present a low impedance to V– during power sequencing. To prevent the AD7525 OUT terminal (pin 1) from exceeding –300mV (which causes catastrophic substrate current), a Schottky diode, HSCH 1001 or equivalent, is recommended. While not required for most amplifier types, provision for the diode should be made during layout. The diode should be connected between OUT (pin 1) and GND (pin 2) as shown in Figure 4. Protection Schottkys not required when using TRI-FET output amplifiers such as the AD542 or AD544.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

V_{DD} (to GND) . . . . . –0.3V, +17V
V_{IN} (to GND) . . . . . ±25V
R_{FB} (to GND) . . . . . ±25V
Digital Input Voltage (to GND) . . . . . –0.3V to V_{DD}
V_{PIN1} (to GND) . . . . . –0.3V to V_{DD}
Power Dissipation (Package)
  Plastic (Suffix N)
    To +70°C 670mW
    Derates above +70°C by . . . . . 8.3mW/°C
  Ceramic (Suffix D)
    To +75°C 450mW
    Derates above +75°C by . . . . . 6mW/°C
Operating Temperature
  Commercial Plastic (KN, LN Versions) . . . . . 0 to +70°C
  Industrial Ceramic (BD, CD Versions) . . . . –25°C to +85°C
  Extended Ceramic (TD, UD Versions) . . . –55°C to +125°C

TERMINOLOGY

SWITCHING TIME: In a D/A converter, the switching time is the time taken for an analog switch to change to a new state from the previous one. It includes delay time, and rise time from 10% to 90%, but does not include settling time, which is a function of the output amplifier used.

OUTPUT CAPACITANCE: Capacitance from OUT terminal (pin 1) to ground.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{IN} (pin 17) to OUT (pin 1) with all digital inputs LOW.

PRINCIPLES OF OPERATION

CIRCUIT DESCRIPTION

The AD7525, a 3½ digit BCD multiplying DAC, consists of a thin-film R/2R ladder, interquad voltage dividers and 13 N-channel MOS SPDT current steering switches. Most applications require the addition of only an external operational amplifier.

Referring to Figure 1, the "1.0 Digit" is a 1-bit multiplying DAC (composed of SW_1 and R_1) while the 0.1, 0.01, and 0.001 digits are 4-bit multiplying DAC's (DAC1, DAC2, and DAC3) connected by 10:1 dividers (composed of R_{IN2}, R_2, R_3 and R_{IN3}, R_4, R_5.

DAC1 is expanded to show the R/2R ladder and switch network. With input voltage V_{IN}, the currents in each shunt arm are (starting at the left) $V_{IN}/2R$, $V_{IN}/4R$, $V_{IN}/8R$ and $V_{IN}/16R$. A logic ONE applied to a digital input steers that shunt arm's current to OUT, while a logic ZERO steers the current to GND.

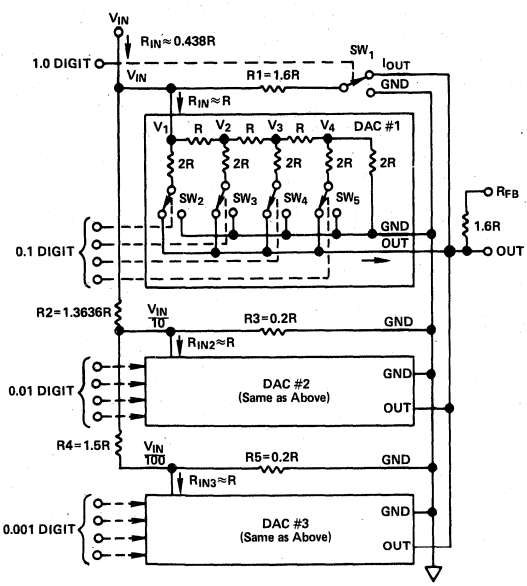


Figure 1. AD7525 Circuit Diagram

EQUIVALENT CIRCUIT

As shown in Figure 2, the AD7525 is a digitally controlled π-network attenuator with signal input "V_{IN}" (pin 17), signal output "OUT" (pin 1), signal common "GND" (pin 2) and digital control "BCD input" (pins 3–15).

With OUT (pin 1) terminated at op amp virtual ground and R_{FB} (pin 18) connected to the op amp output, the nominal transfer equation is:

$$V_{OUT} = -V_{IN}\ BCD$$
where $0.000 \leqslant BCD \leqslant 1.999$

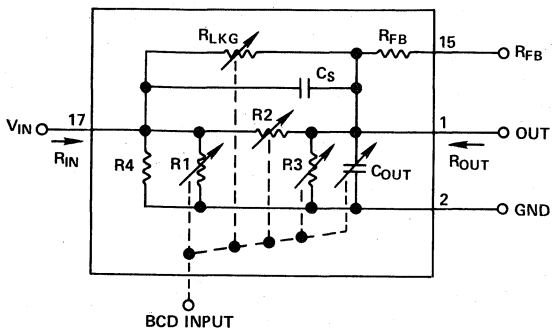


Figure 2. Functional Equivalent Circuit

OUTPUT AMPLIFIER CONSIDERATIONS

Amplifier Offset

The output resistance at OUT (pin 1) is code dependent, varying between ∞ to 0.35 R_{LDR}. For a fixed feedback resistor of value 1.6 R_{LDR} (Figure 3), the output error for a fixed amplifier offset (V_{OS}) is:

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{R_{OUT}}\right) V_{OS}$$

Case 1: ($R_{OUT} = \infty$)

$$V_{ERROR} = \left(1 + \frac{R_{FB}}{\infty}\right) V_{OS}$$

$$V_{ERROR} = V_{OS}$$

Case 2: ($R_{OUT} = 0.35\ R_{LDR}$)

$$V_{ERROR} = \left(1 + \frac{1.6\ R_{LDR}}{0.35 R_{LDR}}\right) V_{OS}$$

$$V_{ERROR} = (1 + 4.6)V_{OS} = 5.6\ V_{OS}$$

Cases 1 and 2 show that amplifier offset in conjunction with a changing output resistance at OUT (pin 1) create nonlinearity error, in addition to a simple offset term.

It is therefore recommended that amplifier initial offset be adjusted to less than 100μV (as measured between the amplifier input terminals). The offset voltage over the temperature range of interest should not exceed 250μV. See application hint #2, below.

Do not include the usual bias current compensation resistor in the amplifier noninverting terminal. Instead, the amplifier should have a bias current which is low over the temperature range of interest. Bias current causes "output offset" of magnitude $(I_B)R_{FB}$.

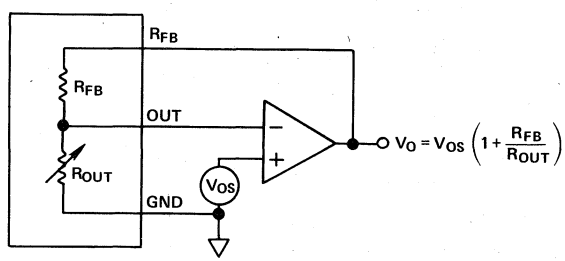


Figure 3. Noise Gain Equivalent Circuit

High Frequency Amplifiers

R_{FB} and C_{OUT} create a phase lag in the output amplifier's feedback circuit. This phase lag, in conjunction with the amplifier's phase lag, may cause ringing or oscillation. When using a high speed amplifier, shunting the amplifier input to output with 5–20pF of feedback capacitance ensures stability.

APPLICATION HINTS

1. If an output voltage range of ±19.99 volts is required (i.e., AD7525 V_{IN} = ±10V, BCD = 1.999), a high voltage output amplifier with appropriate supply voltages must be used.
2. To maintain circuit linearity, the op amp offset voltage should not exceed 2% of the circuit resolution. (Resolution = $V_{IN} \div 1000$)
3. CMOS logic inputs exhibit an input impedance on the order of 100MΩ. Unused CMOS inputs must always be tied to a known logic state. If single-pole single-throw thumbwheel switches are used to drive the digital inputs of the AD7525, external 10kΩ pull-down (pull-up if switch coding is complementary (BCD) resistors must be used.

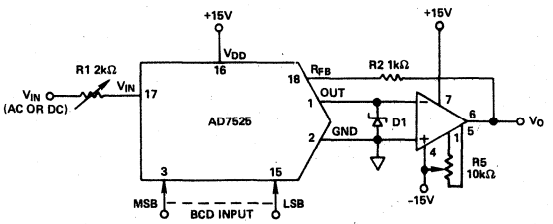


Figure 4. Digitally Controlled Attenuator Circuit

BCD INPUT					ANALOG OUTPUT	
	Digital Input			Equivalent Decimal Input	V_O/V_{IN}	V_O
1.0	0.1	0.01	0.001			
1	1001	1001	1001	1.999	-1.999	$-1.999V_{IN}$
1	0000	0000	0001	1.001	-1.001	$-1.001V_{IN}$
1	0000	0000	0000	1.000	-1.000	$-1.000V_{IN}$
0	1001	1001	1001	0.999	-0.999	$-0.999V_{IN}$
0	0101	0000	0000	0.500	-0.500	$-0.500V_{IN}$
0	0000	0000	0000	0.000	0	0

Note 1:
For proper BCD coding, the 0.1 digit, 0.01 digit or 0.001 digit must not exceed BCD "9" (1001).

Table I. Analog Input/Output Relationship vs. Digital Input

CALIBRATION PROCEDURE

Offset Adjustment:

1. Apply BCD code 0.000 (0 0000 0000 0000) to the AD7525 digital inputs.
2. Connect a high resolution, high impedance voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
3. Adjust amplifier's trimpot for minimum reading on the voltmeter (<100μV).

Gain Adjustment:

1. Apply BCD code 1.000 (1 0000 0000 0000) to the AD7525 digital input.
2. Apply +10V to the V_{IN} input of Figure 1.
3. Connect the voltmeter between V_O (amplifier output) and pin 2 of the AD7525.
4. Adjust R_1 until $V_O = -10V$.

APPLICATION – THUMBWHEEL SWITCH ATTENUATOR

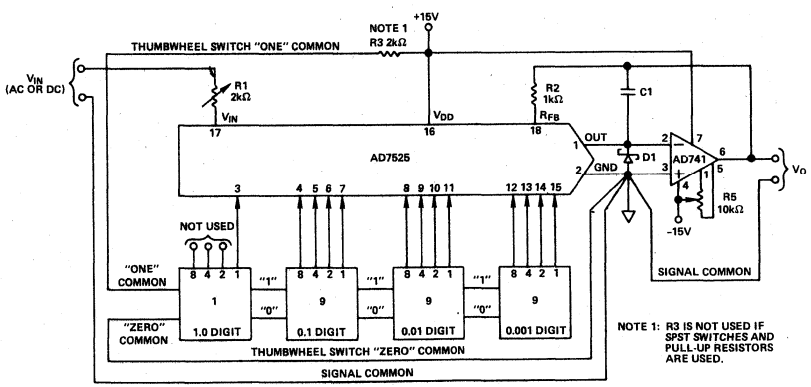


Figure 5. Thumbwheel Switch Attenuator

The circuit shown in Figure 5 is a precision voltage divider similar to 10-turn pots and thumbwheel switch incremental-voltage-divider assemblies. Advantages of the circuit are:

- ☐ Economy
- ☐ Low Output Impedance
- ☐ Resolution 0.1% V_{IN}
- ☐ Excellent Repeatability Accuracy
- ☐ Overrange Capability

The BCD coded thumbwheel assembly applies BCD data to the AD7525 digital inputs. The switch assembly shown has single-pole-double-throw action, thus the BCD inputs are pulled either to +15V or GND (available from AMP, Harrisburg, PA; CHERRY, Waukegan, Illinois; or SAE, Santa Clara, California). Resistor R_3 limits current if make-before-break switches are used. SPST switch assemblies can be used; however, appropriate pull-up or pull-down resistors must be used on each digital input, depending upon whether the switch coding is BCD or complementary BCD. This ensures each digital input has appropriate V_{IH} or V_{IL} levels applied.

Resistors R_1 and R_2 provide gain adjustment capability. R_5 is used to adjust the amplifier input offset voltage to less than 100μV. Diode D_1 (HSCH 1001) provides AD7525 output protection (see Caution note 3).

ANALOG DEVICES

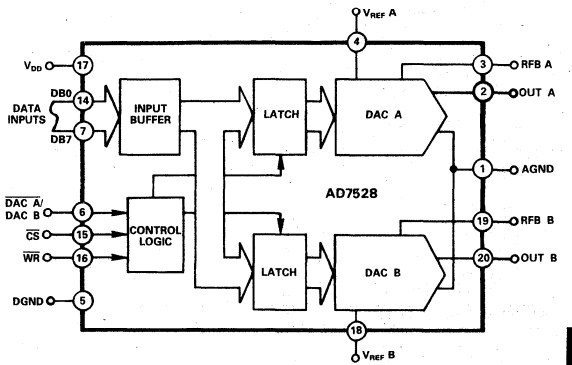
CMOS Dual 8-Bit Buffered Multiplying DAC

AD7528

FEATURES
On-Chip Latches for Both DACs
+5V to +15V Operation
DACs Matched to 1%
Four Quadrant Multiplication
TTL/CMOS Compatible
Latch Free (Protection Schottkys not Required)

APPLICATIONS
Digital Control of:
Gain/Attenuation
Filter Parameters
Stereo Audio Circuits
X–Y Graphics

AD7528 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter produced in a small 0.3″ wide 20-pin DIP, featuring excellent DAC-to-DAC matching.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A}}$/DAC B determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5V to +15V power supply, dissipating only 20mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

PRODUCT HIGHLIGHTS

1. DAC to DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent.The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A}}$/DAC B select line has allowed the AD7528 to be packaged in a small 20-pin 0.3″ wide DIP.

SPECIFICATIONS (V_{REF} A = V_{REF} B = +10V; OUT A = OUT B = 0V unless otherwise specified)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
STATIC PERFORMANCE[2]							
Resolution	All	8	8	8	8	Bits	
Relative Accuracy	J, A, S	±1	±1	±1	±1	LSB max	This is an Endpoint Linearity Specification
	K, B, T	±½	±½	±½	±½	LSB max	
	L, C, U	±½	±½	±½	±½	LSB max	
Differential Nonlinearity	All	±1	±1	±1	±1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range
Gain Error	J, A, S	±4	±6	±4	±5	LSB max	Measured Using Internal RFB A and RFB B.
	K, B, T	±2	±4	±2	±3	LSB max	Both DAC Latches Loaded with 11111111.
	L, C, U	±1	±3	±1	±1	LSB max	Gain Error is Adjustable Using Circuits of Figures 4 and 5.
Gain Temperature Coefficient ΔGain/ΔTemperature	All	±0.007	±0.007	±0.0035	±0.0035	%/°C max	
Output Leakage Current							
OUT A (Pin 2)	All	±50	±400	±50	±200	nA max	DAC Latches Loaded with 00000000
OUT B (Pin 20)	All	±50	±400	±50	±200	nA max	
Input Resistance (V_{REF} A, V_{REF} B)	All	8	8	8	8	kΩ min	Input Resistance TC = −300ppm/°C, Typical
		15	15	15	15	kΩ max	Input Resistance is 11kΩ
V_{REF} A/V_{REF} B Input Resistance Match	All	±1	±1	±1	±1	% max	
DIGITAL INPUTS[3]							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance							
DB0–DB7	All	10	10	10	10	pF max	
$\overline{WR}$, $\overline{CS}$, DAC A/DAC B	All	15	15	15	15	pF max	
SWITCHING CHARACTERISTICS[4]							See Timing Diagram
Chip Select to Write Set Up Time t_{CS}	All	200	230	60	80	ns min	
Chip Select to Write Hold Time t_{CH}	All	20	30	10	15	ns min	
DAC Select to Write Set Up Time t_{AS}	All	200	230	60	80	ns min	
DAC Select to Write Hold Time t_{AH}	All	20	30	10	15	ns min	
Data Valid to Write Set Up Time t_{DS}	All	110	130	30	40	ns min	
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min	
Write Pulse Width t_{WR}	All	180	200	60	80	ns min	
POWER SUPPLY							See Figure 3
I_{DD}	All	1	1	1	1	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS[5] (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version[1]	V_{DD} = +5V T_A = +25°C	V_{DD} = +5V T_{min}, T_{max}	V_{DD} = +15V T_A = +25°C	V_{DD} = +15V T_{min}, T_{max}	Units	Test Conditions/Comments
DC SUPPLY REJECTION (ΔGAIN/ΔV_{DD})	All	0.02	0.04	0.01	0.02	% per % max	ΔV_{DD} = ±5%
CURRENT SETTLING TIME[2]	All	350	400	180	200	ns max	To 1/2LSB. Out A/Out B load = 100Ω. $\overline{WR}$ = $\overline{CS}$ = 0V. DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	V_{REF} A = V_{REF} B = +10V OUT A, OUT B Load = 100Ω C_{EXT} = 13pF $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V
DIGITAL TO ANALOG GLITCH IMPULSE	All	160	–	440	–	nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
C_{OUT} A	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
C_{OUT} B		50	50	50	50	pF max	
C_{OUT} A		120	120	120	120	pF max	DAC Latches Loaded with 11111111
C_{OUT} B		120	120	120	120	pF max	
AC FEEDTHROUGH[6]							
V_{REF} A to OUT A	All	−70	−65	−70	−65	dB max	V_{REF} A, V_{REF} B = 20V p-p Sine Wave
V_{REF} B to OUT B		−70	−65	−70	−65	dB max	@ 100kHz
CHANNEL TO CHANNEL ISOLATION							Both DAC Latches Loaded with 11111111.
V_{REF} A to OUT B	All	−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} B = 0V see Figure 6.
V_{REF} B to OUT A		−77	–	−77	–	dB typ	V_{REF} A = 20V p-p Sine Wave @ 100kHz V_{REF} A = 0V see Figure 6.
DIGITAL CROSSTALK	All	30	–	60	–	nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	85	–	−85	–	dB typ	V_{IN} = 6V rms @ 1kHz

NOTES

[1]Temperature Ranges are JN, KN, LN: 0 to +70°C
AQ, BQ, CQ: −25°C to +85°C
SD, TD, UD: −55°C to +125°C

[2]Specification applies to both DACs in AD7528.

[3]Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1nA.

[4]Guaranteed by design but not production tested.

[5]These characteristics are for design guidance only and are not subject to test.

[6]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	V_{DD}
DGND to AGND	V_{DD}
Digital Input Voltage to DGND	−0.3V, +15V
V_{PIN2}, V_{PIN20} to AGND	−0.3V, +15V
V_{REF} A, V_{REF} B to AGND	±25V
V_{RFB} A, V_{RFB} B to AGND	±25V
Power Dissipation (Any Package) to +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Commercial (JN, KN, LN) Grades	0 to +70°C
Industrial (AQ, BQ, CQ) Grades	−25°C to +85°C
Extended (SD, TD, UD) Grades	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 secs.)	+300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy:
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity:
Differential nonlinearity is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range ensures monotonicity.

Gain Error:
Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7528, ideal full-scale output is V_{REF} −1LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance:
Capacitance from OUT A or OUT B to AGND.

Digital to Analog Glitch Impulse:
The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay:
This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation:
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

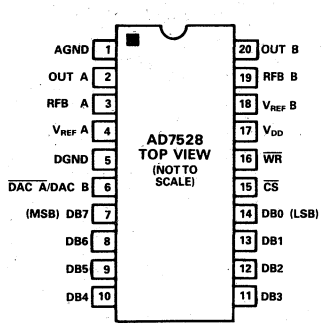
Digital Crosstalk:
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

ORDERING INFORMATION

Relative Accuracy	Gain Error T_A = +25°C	Temperature Range and Package[1] Plastic 0 to +70°C	Cerdip[2] −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±4LSB	AD7528JN	AD7528AQ	AD7528SD
±1/2LSB	±2LSB	AD7528KN	AD7528BQ	AD7528TD
±1/2LSB	±1LSB	AD7528LN	AD7528CQ	AD7528UD

NOTES
[1]The AD7528 is available in chip carriers–contact the factory for information.
[2]Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

PIN CONFIGURATION



PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP (D20A)
Suffix Q: Cerdip (Q20A)
Suffix N: Plastic DIP (N20A)

[1] See Section 19 for package outline information.

INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A}}$/DAC B selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

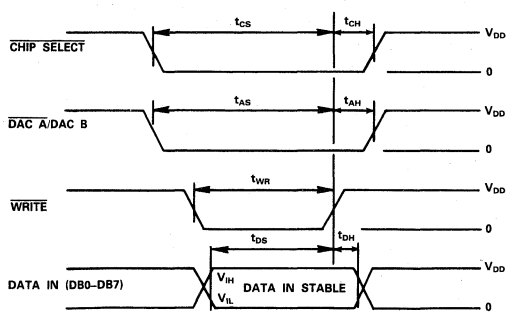
The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

$\overline{\text{DAC A}}$/ DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care

Mode Selection Table

WRITE CYCLE TIMING DIAGRAM



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
   V_{DD} = +5V, $t_r = t_f$ = 20ns;
   V_{DD} = +15V, $t_r = t_f$ = 40ns.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION–D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

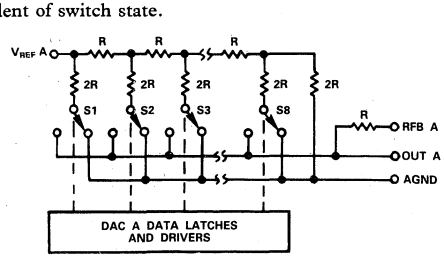


Figure 1. Simplified Functional Circuit for DAC A

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source $I_{LEAKAGE}$ is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C. The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0's code) from 0.8R to 2R. R is typically 11kΩ. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50pF to 120pF depending upon the digital input. g(V_{REF} A, N) is the Thevenin equivalent voltage generator due to the reference input voltage V_{REF} A and the transfer function of the R-2R ladder.

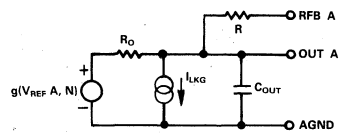


Figure 2. Equivalent Analog Output Circuit of DAC A

For further information on CMOS multiplying D/A converters refer to "Appplication Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

CIRCUIT INFORMATION–DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with V_{DD} = 5V, the buffer converts TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

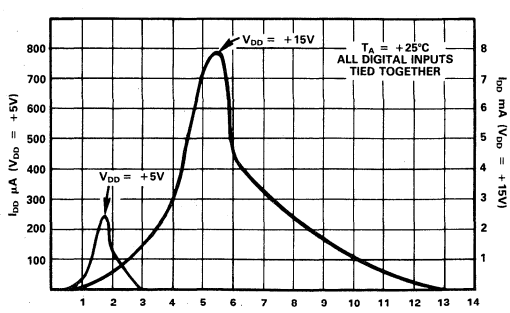
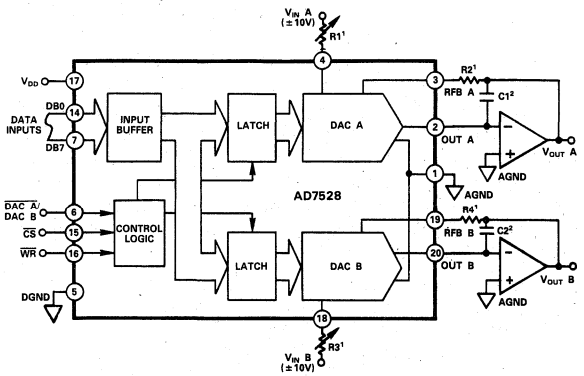
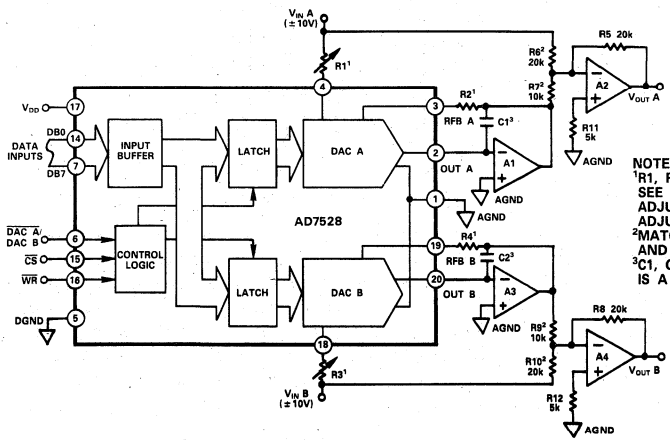


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN}, for V_{DD} = +5V and +15V



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
[2]C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication). See Table I.



NOTES:
[1]R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE 3 FOR RECOMMENDED VALUES.
ADJUST R1 FOR V_{OUT} A = 0V WITH CODE 10000000 IN DAC A LATCH.
ADJUST R3 FOR V_{OUT} B = 0V WITH CODE 10000000 IN DAC B LATCH.
[2]MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
[3]C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BY REQUIRED IF A1/A3 IS A HIGH-SPEED AMPLIFIER.

Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication). See Table II.

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$-V_{IN}\left(\frac{255}{256}\right)$
10000001	$-V_{IN}\left(\frac{129}{256}\right)$
10000000	$-V_{IN}\left(\frac{128}{256}\right) = -\frac{V_{IN}}{2}$
01111111	$-V_{IN}\left(\frac{127}{256}\right)$
00000001	$-V_{IN}\left(\frac{1}{256}\right)$
00000000	$-V_{IN}\left(\frac{0}{256}\right) = 0$

Note: $1LSB = (2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$

Table I. Unipolar Binary Code Table

DAC Latch Contents MSB LSB	Analog Output (DAC A or DAC B)
11111111	$+V_{IN}\left(\frac{127}{128}\right)$
10000001	$+V_{IN}\left(\frac{1}{128}\right)$
10000000	0
01111111	$-V_{IN}\left(\frac{1}{128}\right)$
00000001	$-V_{IN}\left(\frac{127}{128}\right)$
00000000	$-V_{IN}\left(\frac{128}{128}\right)$

Note: $1LSB = (2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table II. Bipolar (Offset Binary) Code Table

Trim Resistor	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD
R1;R3	1k	500	200
R2;R4	330	150	82

Table III. Recommended Trim Resistor Values vs. Grade

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7528 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: AC or transient voltages between the AD7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7528. In more complex systems where the AGND–DGND intertie is on the back-plane, it is recommended that diodes be connected in inverse parallel between the AD7528 AGND and DGND pins (1N914 or equivalent).
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1LSB over the temperature range of interest.
3. HIGH FREQUENCY CONSIDERATIONS: The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relationship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7528 and the AD644 dual op-amp which minimizes feedthrough and crosstalk.

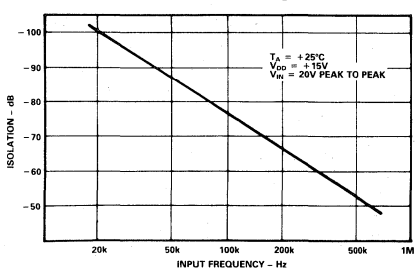


Figure 6. Channel to Channel Isolation

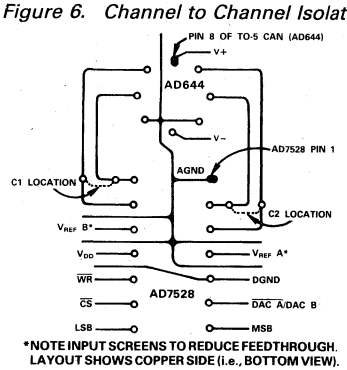


Figure 7. Suggested P.C. Board Layout for AD7528 with AD644 Dual Op-Amp

SINGLE SUPPLY APPLICATIONS

The AD7528 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD}. Figure 8 shows a circuit which provides two +5V to +8V analog outputs by biasing AGND +5V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the V_{REF} A and V_{REF} B inputs are at +2V. The two analog output voltages range from +5V to +8V for DAC codes 00000000 to 11111111.

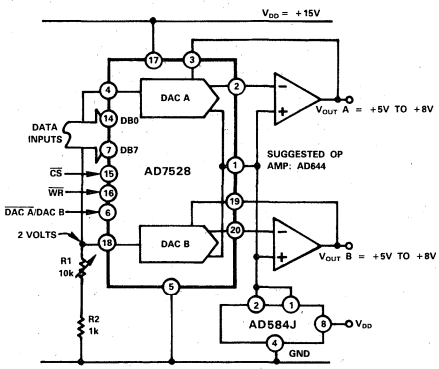


Figure 8. AD7528 Single Supply Operation

Figure 9 shows DAC A of the AD7528 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 to +2.5V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC V_{REF} A pin.

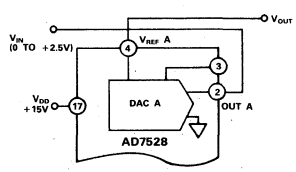


Figure 9. AD7528 in Single Supply, Voltage Switching Mode

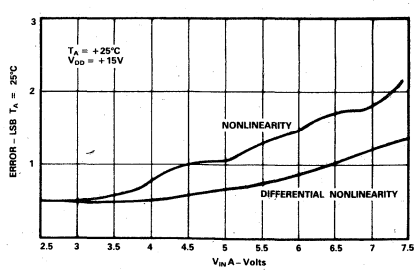


Figure 10. Typical AD7528 Performance in Single Supply Voltage Switching Mode (K/B/T, L/C/U Grades)

MICROPROCESSOR INTERFACE

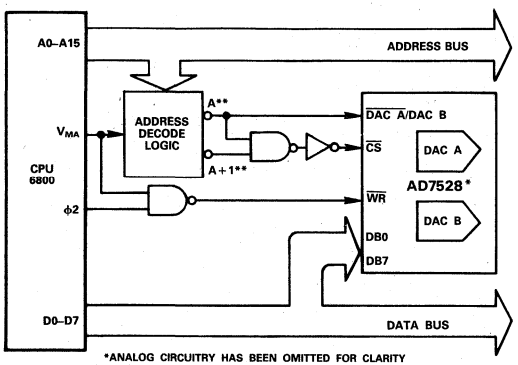


Figure 11. AD7528 Dual DAC to 6800 CPU Interface

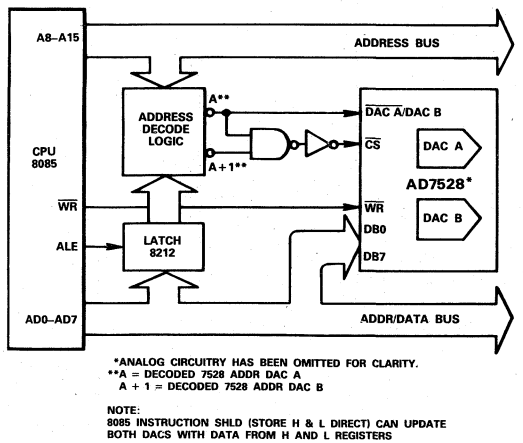


Figure 12. AD7528 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

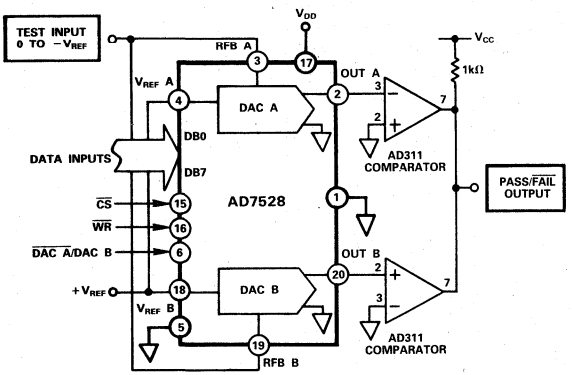


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7528 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

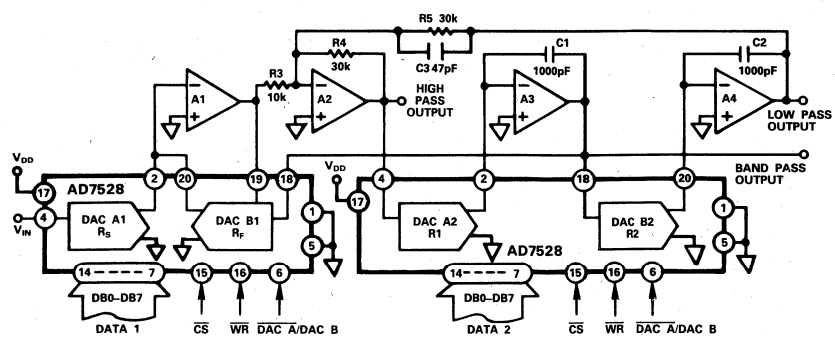


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$C_1 = C_2,\ R_1 = R_2,\ R_4 = R_5$

$$f_C = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_O = -\frac{R_F}{R_S}$$

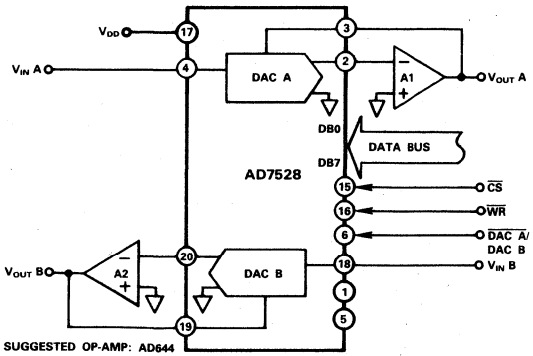
Note:
DAC equivalent resistance equals
$\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. Op amps are 2 × AD644. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is fc = 0 to 15kHz and Q = 0.3 to 4.5.

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR



In this configuration the AD7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 to 15.5dB range.

$$\text{Input Code} = 256 \times 10 \exp\left(-\frac{\text{Attenuation, dB}}{20}\right)$$

Figure 15. Digitally Controlled Dual Telephone Attenuator

Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0	1 1 1 1 1 1 1 1	255	8.0	0 1 1 0 0 1 1 0	102
0.5	1 1 1 1 0 0 1 0	242	8.5	0 1 1 0 0 0 0 0	96
1.0	1 1 1 0 0 1 0 0	228	9.0	0 1 0 1 1 0 1 1	91
1.5	1 1 0 1 0 1 1 1	215	9.5	0 1 0 1 0 1 1 0	86
2.0	1 1 0 0 1 0 1 1	203	10.0	0 1 0 1 0 0 0 1	81
2.5	1 1 0 0 0 0 0 0	192	10.5	0 1 0 0 1 1 0 0	76
3.0	1 0 1 1 0 1 0 1	181	11.0	0 1 0 0 1 0 0 0	72
3.5	1 0 1 0 1 0 1 1	171	11.5	0 1 0 0 0 1 0 0	68
4.0	1 0 1 0 0 0 1 0	162	12.0	0 1 0 0 0 0 0 0	64
4.5	1 0 0 1 1 0 0 0	152	12.5	0 0 1 1 1 1 0 1	61
5.0	1 0 0 1 0 0 0 0	144	13.0	0 0 1 1 1 0 0 1	57
5.5	1 0 0 0 1 0 0 0	136	13.5	0 0 1 1 0 1 1 0	54
6.0	1 0 0 0 0 0 0 0	128	14.0	0 0 1 1 0 0 1 1	51
6.5	0 1 1 1 1 0 0 1	121	14.5	0 0 1 1 0 0 0 0	48
7.0	0 1 1 1 0 0 1 0	114	15.0	0 0 1 0 1 1 1 0	46
7.5	0 1 1 0 1 1 0 0	108	15.5	0 0 1 0 1 0 1 1	43

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

For further applications information the reader is referred to Analog Devices Application Note on the AD7528.

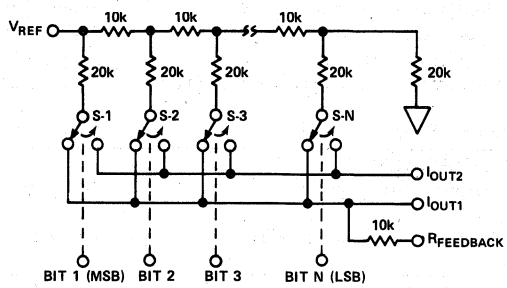
CMOS 10- & 12-Bit Monolithic Multiplying D/A Converters

AD7530, AD7531

FEATURES
AD7530: 10-Bit Resolution
AD7531: 12-Bit Resolution
8-, 9- and 10-Bit End Point Linearity
DTL/TTL/CMOS Compatible
Nonlinearity Tempco: 2ppm of FSR/°C
Low Power Dissipation: 20mW
Current Settling Time: 500ns
Feedthrough Error: 10mV p-p @ 50kHz
Low Cost

Note: AD7533 is Recommended for New 10-Bit Designs. AD7541A or AD7545 is Recommended for New 12-Bit Designs.

AD7530, AD7531 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

AD7530: N = 10
AD7531: N = 12
(Switches shown in "High" state)

9

GENERAL DESCRIPTION

The AD7530 (AD7531) is a low cost, monolithic 10-bit (12-bit) multiplying digital-to-analog converter packaged in a 16-pin (18-pin) DIP. The device uses advanced CMOS and thin film technologies providing up to 10-bit accuracy with DTL/TTL/CMOS compatibility.

The AD7530 (AD7531) operates from a +5V to +15V supply and dissipates only 20mW, including the ladder network.

Typical applications include: digital/analog multiplication, CRT character generation, programmable power supplies, digitally controlled gain circuits, etc.

ORDERING INFORMATION

Nonlinearity	Temperature Range	
	0 to +70°C	−25°C to +85°C
0.2% (8-Bit)	AD7530JN	AD7530JD
	AD7531JN	AD7531JD
0.1% (9-Bit)	AD7530KN	AD7530KD
	AD7531KN	AD7531KD
0.05% (10-Bit)	AD7530LN	AD7530LD
	AD7531LN	AD7531LD

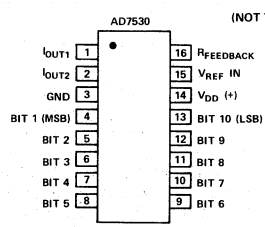
PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP
AD7530: (D16A)
AD7531: (D18A)
Suffix N: Plastic DIP
AD7530: (N16B)
AD7531: (N18B)

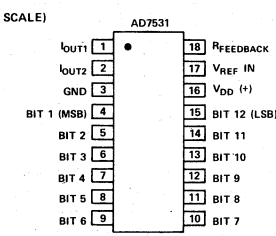
[1] See Section 19 for package outline information.

PIN CONFIGURATION

(NOT TO SCALE)



16-PIN DIP
TOP VIEW



18-PIN DIP
TOP VIEW

SPECIFICATIONS (V_{DD} = +15, V_{REF} = +10V, T_A = +25°C unless otherwise noted)

PARAMETER		AD7530	AD7531	TEST CONDITIONS
DC ACCURACY (Note 1)				
Resolution		10 Bits	12 Bits	
Relative Accuracy	AD7530J	0.2% of FSR max (8 Bit)	*	
	AD7530K	0.1% of FSR max (9 Bit)	*	
	AD7530L	0.05% of FSR max (10 Bit)	*	$-10V < V_{REF} < +10V$
Nonlinearity Tempco		2ppm of FSR/°C max	*	
Gain Error		0.3% of FSR typ	*	
Gain Error Tempco		10ppm of FSR/°C max	*	
Output Leakage Current (Either Output)		300nA max	*	Over specified temperature range.
Power Supply Rejection		50ppm of FSR/% typ	*	
AC ACCURACY				To 0.05%
Output Current Settling Time		500ns typ	*	All digital inputs low to high and high to low
Feedthrough Error (Note 2)		10mV p-p max	*	V_{REF} = 20V p-p, 50kHz. All digital inputs low
REFERENCE INPUT		±10V	*	
Input Range		±1mA	*	
Input Resistance		10kΩ typ	*	
ANALOG OUTPUT				
Output Current Range (Both Outputs)		±1mA	*	
Output Capacitance	I_{OUT1}	120pF typ	*	All digital inputs high
	I_{OUT2}	37pF typ	*	
	I_{OUT1}	37pF typ	*	All digital input low
	I_{OUT2}	120pF typ	*	
Output Noise (Both Outputs)		Equivalent to 10kΩ Johnson noise typ	*	
DIGITAL INPUTS (Note 3)				
Low State Threshold		0.8V max	*	Over specified temperature range
High State Threshold		2.4V min	*	Over specified temperature range
Input Current (low to high state)		1μA typ	*	
Input Coding		Binary	*	See Tables I & II
POWER REQUIREMENTS				
Power Supply Voltage Range		+5V to +15V	*	
I_{DD}		5nA typ	*	All digital inputs at GND
		2mA max	*	All digital inputs high or low
Total Dissipation		20mW typ	*	

NOTES
[1] Full scale range (FSR) is 10V for unipolar mode and ±10V for bipolar mode.
[2] To minimize feedthrough with the ceramic package, the user must ground the metal lid. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.
[3] Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
*Same specifications as for AD7530.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to Gnd) . . . . . +17V
V_{REF} (to Gnd) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to Gnd
Voltage at Pin 1, Pin 2 . . . . . −100mV to V_{DD}
Power Dissipation (package)
up to +75°C 450mW
Operating Temperature
JN, KN, LN Versions . . . . . 0 to +75°C
JD, KD, LD Versions . . . . . −25°C to +85°C
Storage Temperature . . . . . −65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 1 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table I. Protection Schottky shown in Figure 1 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

R1 provides full scale trim capability [i.e.—load the DAC register to 11 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}(1 - 2^{-10})$]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at I_{OUT1}).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ).

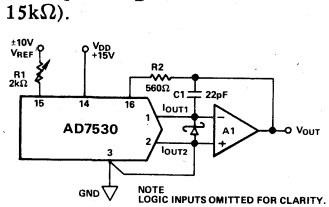


Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(1/2 + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$\frac{-V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(1/2 - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

NOTE: 1 LSB = 2^{-10} V_{REF}

Table I. Code Table — Unipolar Binary Operation

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 2 and Table II illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) or an ac reference the circuit provides offset binary operation. Protection Schottky shown in Figure 2 is not required when using TRIFET output amplifiers such as the AD542 or AD544.

With the DAC register loaded to 10 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full Scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

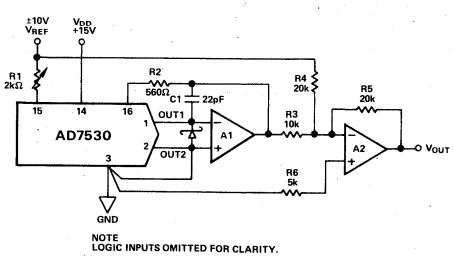


Figure 2. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

NOTE: 1 LSB = 2^{-9} V_{REF}

Table II. Code Table — Bipolar (Offset Binary) Operation

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the end-points of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

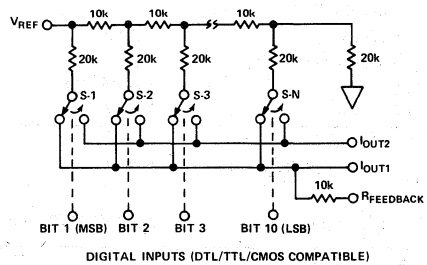
CMOS Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
- Lowest Cost 10-Bit DAC
- Low Cost AD7520 Replacement
- Linearity: 1/2, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface
- Latch Free (Protection Schottky not Required)
- End-Point Linearity

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control

AD7533 FUNCTIONAL BLOCK DIAGRAM



Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

9

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

PACKAGE IDENTIFICATION[1]

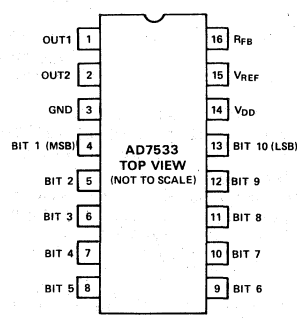
Suffix "D" – Ceramic DIP (D16B)
Suffix "N" – Plastic DIP (N16B)

[1] See Section 19 for package outline information.

ORDERING INFORMATION

Nonlinearity	Temperature Range and Package		
	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Extended (Ceramic) -55°C to +125°C
±0.2%	AD7533JN	AD7533AD	AD7533SD
±0.1%	AD7533KN	AD7533BD	AD7533TD
±0.05%	AD7533LN	AD7533CD	AD7533UD

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range[1]	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[2,3]			
AD7533JN, AD, SD	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD	±0.05% FSR max	±0.05% FSR max	
Gain Error[3,4,5]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[6]			
ΔGain/ΔV_{DD}	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[7]	800ns[6]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[6]	±0.1% FSR max[6]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sinewave.
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[8]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max[6]	100pF max[6]	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	35pF max[6]	35pF max[6]	
C_{OUT1} (pin 1)	35pF max[6]	35pF max[6]	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max[6]	100pF max[6]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}[3]	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}[3]	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}[3]	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	5pF max[6]	5pF max[6]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[6]	+5V to +16V	+5V to +16V	Functionality with degraded performance
I_{DD}[3]	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES

[1] Plastic (JN, KN, LN versions): 0 to +70°C.
Commercial Ceramic (AD, BD, CD versions): -25°C to +85°C.
Extended Ceramic (SD, TD, UD versions): -55°C to +125°C.

[2] "FSR" is Full Scale Range.

[3] Final electrical tests are: Relative Accuracy, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).

[4] Full Scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$

[5] Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.

[6] Guaranteed, not tested.

[7] AC parameter, sample tested to ensure specification compliance.

[8] Absolute temperature coefficient is approximately -300ppm/°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . . -0.3V, +17V
R_{FB} to GND . . . . . ±25V
V_{REF} to GND. . . . . ±25V
Digital Input Voltage Range . . . . . -0.3V to V_{DD}
Output Voltage (pin 1, pin 2) . . . . . -0.3V to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . . .8.3mW/°C
Ceramic (Suffix D)
To +70°C. 450mW
Derates above +75°C by . . . . . .6mW/°C
Operating Temperature Range
Commercial (JN, KN, LN versions). . . . . 0 to +70°C
Industrial (AD, BD, CD versions) . . . . . -25°C to +85°C
Extended (SD, TD, UD versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).

9

TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN ERROR: Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

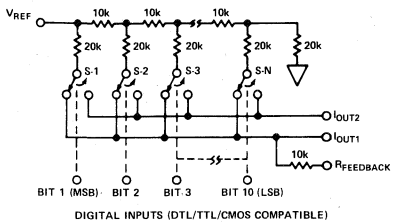


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 for 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

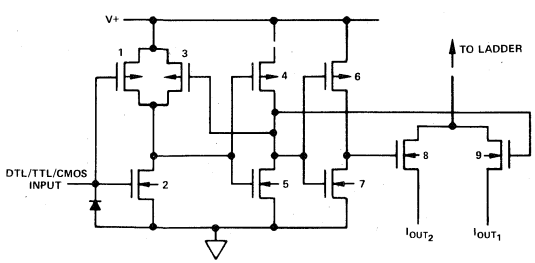


Figure 2. CMOS Switch

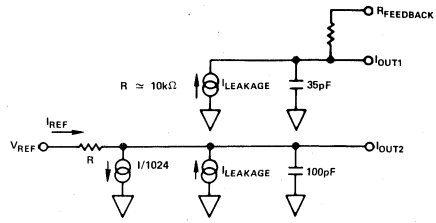


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

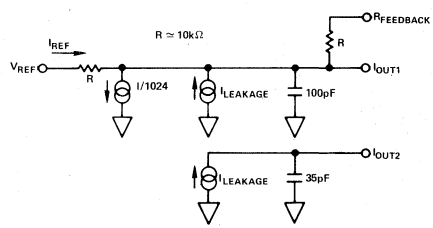
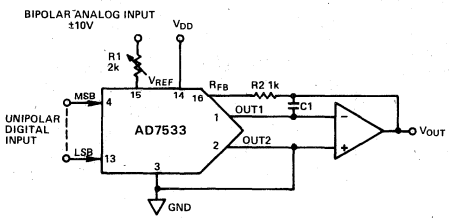


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

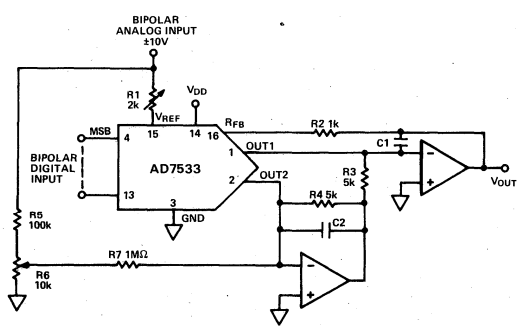
Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB	DIGITAL INPUT LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1111111111		$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001		$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000		$-V_{REF}\left(\frac{512}{1024}\right) = \frac{V_{REF}}{2}$
0111111111		$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001		$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000		$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal Full Scale for the circuit of Figure 5 is given by $FS = -V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED
3. C1, C2 PHASE COMPENSATION (5 - 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB	DIGITAL INPUT LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1111111111		$-V_{REF}\left(\frac{511}{512}\right)$
1000000001		$-V_{REF}\left(\frac{1}{512}\right)$
1000000000		0
0111111111		$+V_{REF}\left(\frac{1}{512}\right)$
0000000001		$+V_{REF}\left(\frac{511}{512}\right)$
0000000000		$+V_{REF}\left(\frac{512}{512}\right)$

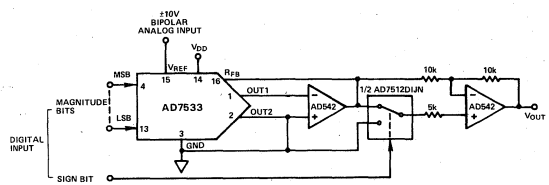
NOTES:
1. Nominal Full Scale Range for the circuit of Figure 6 is given by $FSR = V_{REF}\left(\frac{1023}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table

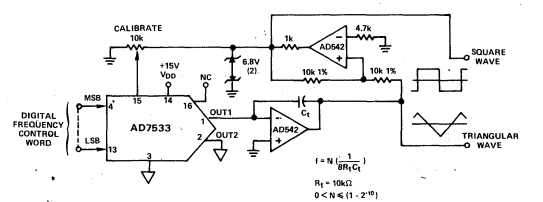
9

APPLICATIONS

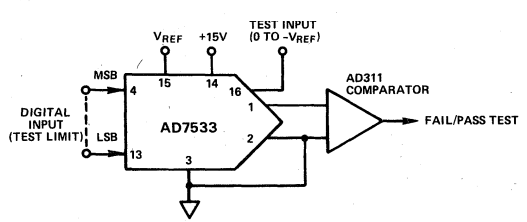
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR

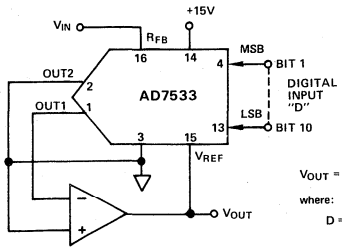


DIGITALLY PROGRAMMABLE LIMIT DETECTOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



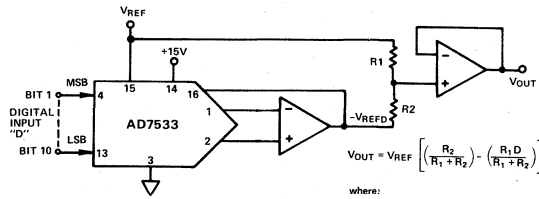
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

LC²MOS µP-Compatible 14-Bit DAC

AD7534

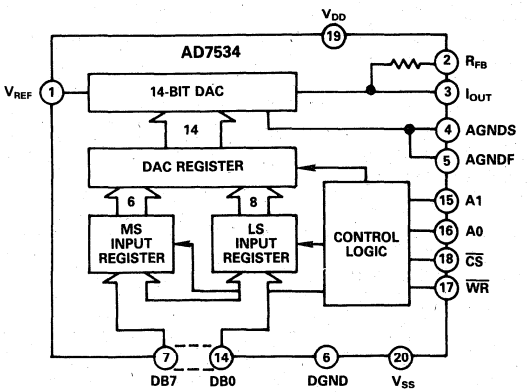
FEATURES

- All Grades 14-Bit Monotonic over the Full Temperature Range
- Full 4-Quadrant Multiplication
- Microprocessor Compatible with Double Buffered Inputs
- Exceptionally Low Gain Temperature Coefficient, 0.5ppm/°C typ
- Small 20-Pin Package
- Low Output Leakage (<20nA) over the Full Temperature Range

APPLICATIONS

- Microprocessor Based Control Systems
- Digital Audio Reconstruction
- High Precision Servo Control
- Control and Measurement in High Temperature Environments

AD7534 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The AD7534 is a 14-bit monolithic CMOS D/A converter which uses thin-film resistors and laser trimming to achieve excellent linearity.

The device is configured to accept right-justified data in two bytes from an 8-bit data bus. Standard Chip Select and Memory Write logic is used to access the DAC. Address lines A0 and A1 control internal register loading and transfer.

A novel low leakage configuration (patent pending) enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

The device is fully protected against CMOS "latch up" phenomena and does not require the use of external Schottky diodes or the use of a FET Input op-amp. The AD7534 is manufactured using the Linear Compatible CMOS (LC²MOS) process. It is speed compatible with most microprocessors and accepts TTL or CMOS logic level inputs.

PRODUCT HIGHLIGHTS

1. Guaranteed Montonicity
   The AD7534 is guaranteed monotonic to 14-bits over the full temperature range for all grades.
2. Low Output Leakage
   By tying V_{SS} (pin 20) to a negative voltage, it is possible to achieve a low output leakage current at high temperatures.
3. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allows direct interfacing to most of the popular 8-bit and 16-bit microprocessors.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3" 20-pin package.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Full Scale Error T_{min} to T_{max}	Temperature Range and Package[1]		
		Plastic (N20B) 0 to +70°C	Ceramic (D20B) −25°C to +85°C	Ceramic (D20B) −55°C to +125°C
±2LSB	±8LSB	AD7534JN	AD7534AD	AD7534SD
±1LSB	±4LSB	AD7534KN	AD7534BD	AD7534TD

[1]See Section 19 for package outline information.

SPECIFICATIONS[1] (V_{DD} = +12V to +15V[2], V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV. All specifications T_{min} to T_{max} unless otherwise stated)

Parameter	AD7534JN AD7534AD	AD7534KN AD7534BD	AD7534SD	AD7534TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	14	14	14	14	Bits	
Relative Accuracy	±2	±1	±2	±1	LSB max	All grades guaranteed monotonic
Differential Nonlinearity	±1	±1	±1	±1	LSB max	over temperature.
Full Scale Error	±8	±4	±8	±4	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain T.C.
Gain Temperature Coefficient[3]						
ΔGain/ΔTemperature	±5	±2.5	±5	±2.5	ppm/°C max	Typical value is 0.5ppm/°C
Output Leakage Current I_{OUT} (Pin 3)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs 0V
T_{min} to T_{max}	±10	±10	±20	±20	nA max	V_{SS} = −300mV
T_{min} to T_{max}	±25	±25	±150	±150	nA max	V_{SS} = 0V
REFERENCE INPUT						
Input Resistance, Pin 1	3.5	3.5	3.5	3.5	kΩ min	Typical Input Resistance = 6kΩ
	10	10	10	10	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V min	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V max	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[3]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over
V_{SS} Range	−200/−500	−200/−500	−200/−500	−200/−500	mV min/mV max	this range.
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	500	500	500	500	μA max	All digital inputs 0V or V_{DD}

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test.
(V_{REF} = +10V, V_{PIN3} = V_{PIN4} = 0V, V_{SS} = −300mV, Output Amplifier is AD544 except where stated).

Parameter	V_{DD} = +12V to +15V T_A=25°C	T_A=T_{min}, T_{max}	Units	Test Conditions/Comments
Output Current Settling Time	1.5	–	μs max	To 0.003% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's. Typical value of Settling Time Time is 0.8μs.
Digital to Analog Glitch Impulse	100	–	nV-sec typ	Measured with V_{REF} = 0V. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1's and all 0's.
Multiplying Feedthrough Error[4]	3	5	mV p-p typ	V_{REF} = ±10V, 10kHz sine wave DAC register loaded with all 0's.
Power Supply Rejection ΔGain/ΔV_{DD}	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance C_{OUT} (Pin 3)	260	260	pF max	DAC register loaded with all 1's
C_{OUT} (Pin 3)	130	130	pF max	DAC register loaded with all 0's
Output Noise Voltage Density (10Hz–100kHz)	15	–	nV$\sqrt{Hz}$ typ	Measured between R_{FB} and I_{OUT}

NOTES
[1]Temperature range as follows: JN, KN Versions: 0 to +70°C
AD, BD Versions: −25°C to +85°C
SD, TD Versions: −55°C to +125°C
[2]Specifications are guaranteed for a V_{DD} of +12V to +15V with a tolerance of ±5%. At V_{DD} = 5V, the device is fully functional with a slight degradation in performance.
[3]Guaranteed by Product Assurance testing.
[4]Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
Specifications subject to change without notice.

CMOS 12-Bit Monolithic Multiplying DAC

AD7541

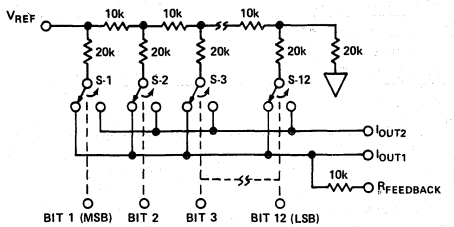
FEATURES

Full Four Quadrant Multiplication
12-Bit Linearity (±1/2LSB)
Pretrimmed Gain
TTL/CMOS Compatible
Low Power Consumption
Low Feedthrough Error
Low Cost

APPLICATIONS

Digital/Synchro Conversion
Programmable Amplifiers
Ratiometric A/D Conversion
Function Generation
AD7541A Recommended for New Designs

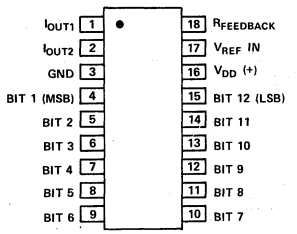
AD7541 FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

PIN CONFIGURATION

TOP VIEW
(NOT TO SCALE)



GENERAL DESCRIPTION

The Analog Devices AD7541 is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter fabricated using advanced double-layer-metal CMOS technology and packaged in a standard 18-pin DIP.

Pin compatible with the AD7521, this new device uses laser wafer trimming to provide full 12-bit linearity and excellent absolute accuracy.

The inherently low power dissipation, coupled with the current switching R-2R ladder, ensures that the performance is maintained over the full temperature range.

ORDERING INFORMATION

	Temperature Range and Package		
Nonlinearity	Plastic 0 to +70°C	Ceramic -25°C to +85°C	Ceramic -55°C to +125°C
0.02%	AD7541JN	AD7541AD	AD7541SD
0.01%	AD7541KN	AD7541BD	AD7541TD

PACKAGE IDENTIFICATION[1]

Suffix "D": Ceramic DIP (D18B)
Suffix "N": Plastic DIP (N18B)

[1] See Section 19 for package outline information.

9

SPECIFICATIONS (V_{DD} = 15V, V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 Bits min	12 Bits min	
Nonlinearity			
AD7541JN, AD7541AD, AD7541SD[1]	±1LSB max	±1LSB max	V_{OUT1} = V_{OUT2} = 0V
AD7541KN, AD7541BD, AD7541TD[2]	±1/2LSB max	±1/2LSB max	
Gain Error[3,4]	±12.5LSB max	±16.7LSB max	
Power Supply Rejection	±0.01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[5]	1μs max	1μs max	To ±1/2LSB of Full Scale Range
Feedthrough Error[5]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V min	2.4V min	
V_{INL}	0.8V max	0.8V max	
Input Leakage Current	±1μA max	±1μA max	V_{IN} = 0 or 15V
Input Capacitance[5]	8pF max	8pF max	
Input Coding	Binary or Offset Binary (see Page 5)		
ANALOG OUTPUTS			
Output Capacitance[5]			
C_{OUT1}	200pF max	200pF max	Digital Inputs = V_{INH}
C_{OUT2}	60pF max	60pF max	
C_{OUT1}	60pF max	60pF max	Digital Inputs = V_{INL}
C_{OUT2}	200pF max	200pF max	
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1] J, A and S versions are monotonic to 11 bits.
[2] K, B and T versions are monotonic to 12 bits.
[3] Using internal feedback resistor.
[4] Max gain change from +25°C to T_{min} or T_{max} is ±4.2LSB max.
[5] Guaranteed by design, not subject to test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . –0.3V to V_{DD}
Power Dissipation (Package)
Up to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C
Operating Temperature
JN, KN Versions . . . . . 0 to +70°C
AD, BD Versions . . . . . –25°C to +85°C
SD, TD Versions . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

TYPICAL PERFORMANCE CHARACTERISTICS

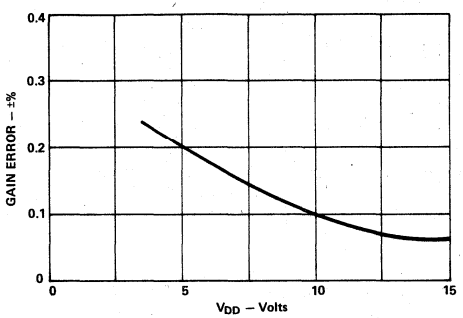


Figure 1. Gain Error vs. Supply Voltage

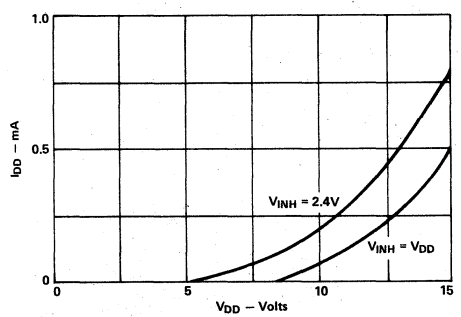


Figure 2. Supply Current vs. Supply Voltage

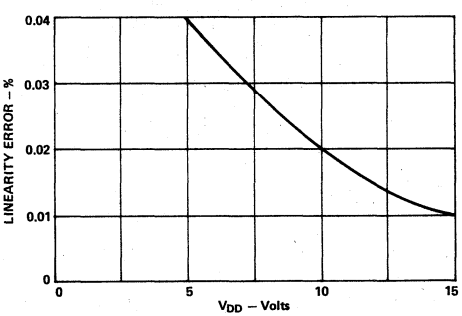


Figure 3. Linearity Error vs. Supply Voltage

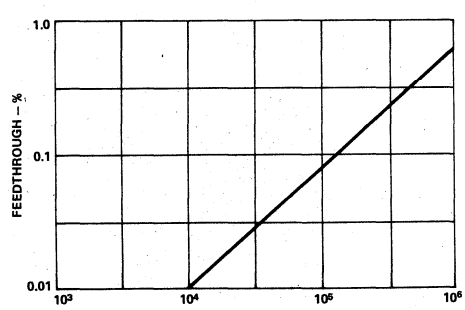


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifiers non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifiers offset voltage and bias current is necessary.

The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

9

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7541, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 5. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

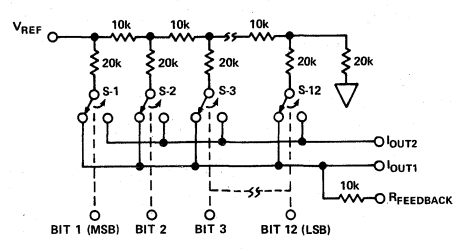


Figure 5. AD7541 Functional Diagram (Inputs "HIGH")

One of the CMOS current switches is shown in Figure 6. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily scaled so the voltage drop across each switch is the same. For example, switch 1 of Figure 6 was designed for an "ON" resistance of 10 ohms, switch 2 of 20 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on,

thus maintaining a constant 5mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

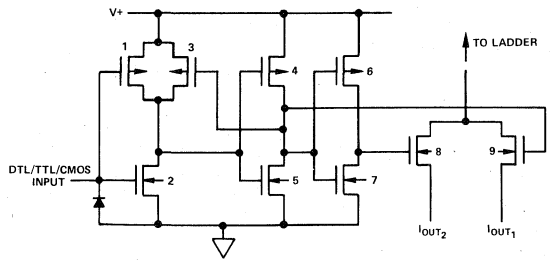


Figure 6. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 7 and 8. In Figure 7 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the 1/4096 current source represents a constant 1-bit current drain through the

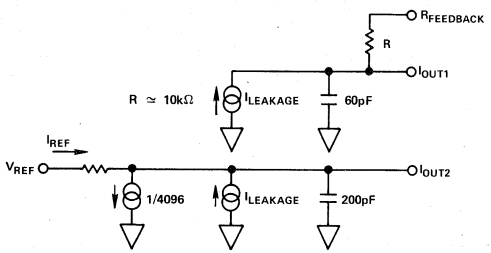


Figure 7. AD7541 Equivalent Circuit – All Digital Inputs Low

termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the I_{OUT2} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 8, is similar to Figure 7; however, the "ON" switches are now on terminal I_{OUT1}, hence the 200pF at that terminal.

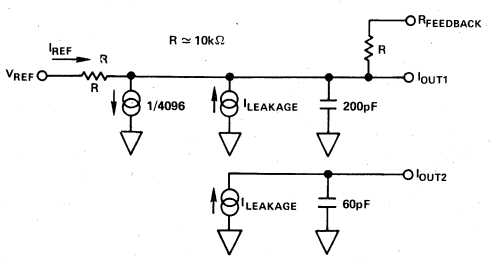


Figure 8. AD7541 Equivalent Circuit – All Digital Inputs High

DYNAMIC PERFORMANCE

OUTPUT IMPEDANCE

The preceding circuit analysis shows that the output capacitance is dependent upon the digital code, as is the output resistance. Looking back into I_{OUT1} the resistance seen is anything between 10kΩ ($R_{FEEDBACK}$ alone) and 5kΩ (R_{FB} in parallel with the 10kΩ network resistance).

This variation affects both static accuracy and dynamic performance. The effect on static accuracy is further considered on pages 5 and 6. The dynamic performance of the AD7541 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components.

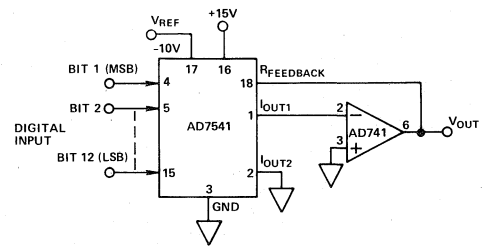


Figure 9. DAC Circuit Using AD741K

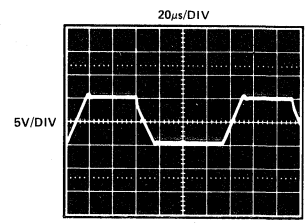


Figure 10. Output Waveform

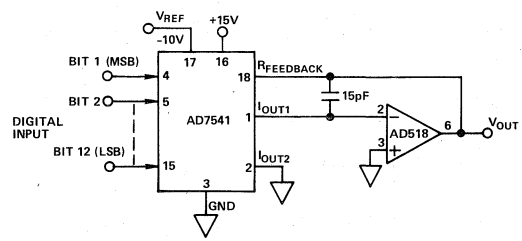


Figure 11. DAC Circuit Using AD518K

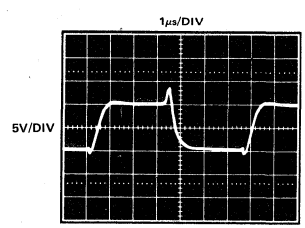


Figure 12. Output Waveform

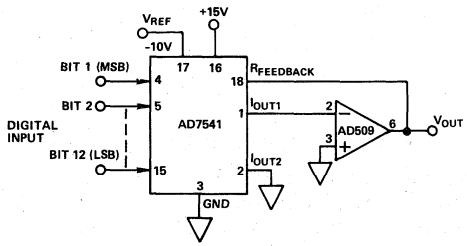


Figure 13. DAC Circuit Using AD509K

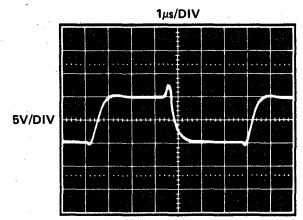


Figure 14. Output Waveform

The circuits and waveforms shown in Figures 9 to 14 are representative of the three principal types of output amplifiers. A general purpose low drift (AD741K), a high speed low cost (AD518), and a fast settling unit (AD509).

Points to remember when applying high speed amplifiers include:

1. Protection diodes as shown in Figures 15 and 16.
2. Phase compensation for the DAC's output capacitance.
3. Power supply decoupling and correct load earthing.

APPLICATIONS

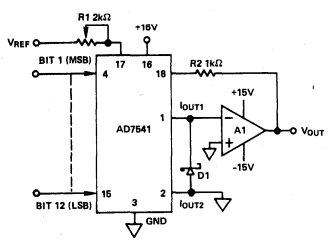


Figure 15. Unipolar Binary Operation

UNIPOLAR BINARY OPERATION (Figure 15)

The connections required for unipolar digital binary operation are shown above. V_{REF} may be positive or negative so 2-quadrant multiplication may be performed. Schottky diode D1 (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers. The diodes are not required when using TRI-FET amplifiers such as the AD542 or AD544.

BIPOLAR (4-QUADRANT) BINARY OPERATION (Figure 16)

The digital input is offset binary coded and multiplies V_{REF} according to Table II. Resistors R3 and R4 should be equal within 0.1% at all temperatures, but need not track the resistors within the AD7541. D1 and D2 perform the same function as in Figure 15. Network R5, R6, R7 sum 1/2LSB of current into I_{OUT2} to ensure correct coding at zero.

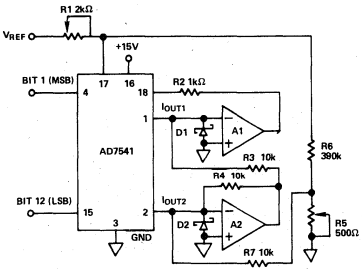


Figure 16. Bipolar (4-Quadrant) Binary Operation

R1 can be adjusted to produce the outputs shown in Table I. However, it is recommended that when the application permits it, R1 and R2 be omitted. The maximum gain error in this condition is 0.3% of full scale. The offset voltage of amplifier A1 should be adjusted to less than 0.5mV over the temperature range.

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99975 V_{REF}
100000000000	-0.50000 V_{REF}
011111111111	-0.49975 V_{REF}
000000000000	0

Table I. Code Table for Circuit of Figure 15

DIGITAL INPUT	NOMINAL ANALOG OUTPUT
111111111111	-0.99951 V_{REF}
100000000001	-0.00049 V_{REF}
100000000000	0
010000000000	+0.50000 V_{REF}
000000000000	+1.00000 V_{REF}

Table II. Code Table for Circuit of Figure 16

Amplifiers A1 and A2 should be adjusted to an input offset of less than 0.1mV and should be better than 0.5mV over the temperature range. With V_{REF} set to approximately 10V, R5 should be adjusted so that with code 10000000000 V_{OUT} = 0V ±0.2mV. R1 should be adjusted so that with code 000000000000 $V_{OUT} = V_{REF}$.

As with the unipolar circuit R1 and R2 can be omitted, with a resulting maximum gain error of 0.3% of full scale. R5 may be replaced by a 100Ω fixed resistor. The maximum zero error if this is done is 0.015% of F.S.R.

OUTPUT AMPLIFIER CONSIDERATIONS

It has already been pointed out that the DAC output resistance varies with the digital code. The effect this has on static accuracy will now be considered.

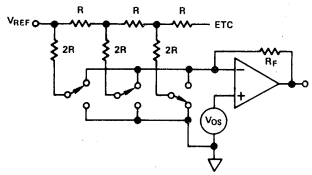


Figure 17.

$$\text{The error voltage} = V_{OS}\left(1 + \frac{R_F}{R_O}\right)$$

R_O is a function of the digital code.
$R_O \cong 10k\Omega$ for any more than 4-bits Logic 1.
$R_O \cong 30k\Omega$ for any single bit Logic 1.

The gain for offset, therefore, changes as follows:

$$\text{At code } 001111111111\ V_{ERROR1} = V_{OS}\left(1 + \frac{10k}{10k}\right) = 2\ V_{OS}$$

$$\text{At code } 010000000000\ V_{ERROR2} = V_{OS}\left(1 + \frac{10k}{30k}\right) = \frac{4}{3}\ V_{OS}$$

The error difference is therefore $\frac{2}{3}\ V_{OS}$

Since, for a 12-bit resolution DAC, one LSB has a weight (for V_{REF} = +10V) of 2.5mV, it is clearly important that V_{OS} be nulled, either using the amplifiers nulling facility or an external network.

It is important to realize that an offset can be caused by including the usual bias current compensation resistor in the amplifiers non-inverting input terminal. This should not be included. Instead the amplifier should have a bias current which is low over the temperature range of interest, and should certainly not exceed 75nA.

ANALOG/DIGITAL DIVISION

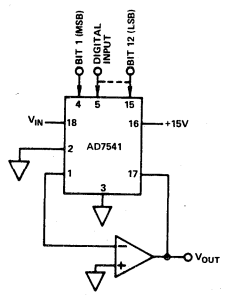


Figure 18. Analog/Digital Divider

With the AD7541 connected in its normal multiplying configuration as shown in Figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}\right)$$

where the coefficients A_X assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 18, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots\ldots \frac{A_{12}}{A^{12}}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero is not defined. With the LSB (Bit 12) ON, the gain is 4096. With all bits ON, the gain is 1 (±1LSB).

DIGITAL/SYNCHRO CONVERTER

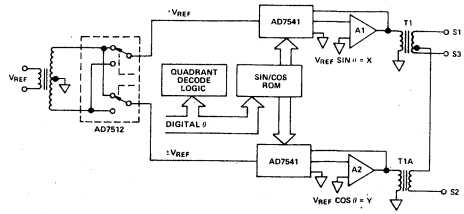


Figure 19. 14-Bit Digital to Synchro Converter

The low cost and high accuracy available from the AD7541, together with its bipolar multiplying capability is exploited fully in the circuit of Figure 19. V_{REF} is commonly 400Hz but by replacing the transformers with dc coupled circuits coordinate transformation may be performed.

The SIN/COS ROM is readily available at low cost and the AD7512 switch enables greater resolution to be obtained.

Resolver-to-synchro transformation is performed by the Scott connected pair T1 and T1A. The power available to the load connected to S1, S2 and S3 is determined by the amplifiers A1 and A2. A particular advantage of the circuit shown in Figure 19 is that it is invariant with respect to θ, and may be used to directly drive equipment such as CRT displays.

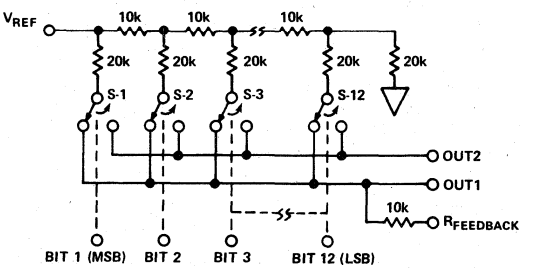
ANALOG DEVICES

CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

FEATURES
- Improved Version of AD7541
- Full Four Quadrant Multiplication
- 12-Bit Linearity (End-Point)
- ±1LSB Gain Error
- All Parts Guaranteed Monotonic
- TTL/CMOS Compatible
- Low Cost
- Protection Schottky not Required
- Low Logic Input Leakage

AD7541A FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)
Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

9

GENERAL DESCRIPTION

The Analog Devices' AD7541A is a low cost, high performance 12-bit monolithic multiplying digital to analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and packaged in a standard 18-pin DIP.

The AD7541A is functionally and pin compatible with the industry standard AD7541 device and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output Schottky protection diodes are required.

This new device uses laser wafer trimming to provide full 12-bit end-point linearity with several new high performance grades.

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error T_A = +25°C	Temperature Range and Package[1] Plastic 0 to +70°C	Cerdip[2] −25°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±6LSB	AD7541AJN	AD7541AAQ	AD7541ASD
±1/2LSB	±1LSB	AD7541AKN	AD7541ABQ	AD7541ATD

NOTES:
[1]Analog Devices is offering the AD7541A in chip carriers. For information contact your Analog Devices' sales office.
[2]Analog Devices reserves the right to ship Ceramic Packages in lieu of Cerdip Packages.

PACKAGE IDENTIFICATION[1]

Suffix "N": – Plastic DIP (N18B)
Suffix "Q": – Cerdip[2] (Q18A)
Suffix "D": – Ceramic DIP (D18B)

[1]See Section 19 for package outline information.
[2]Analog Devices reserves the right to ship ceramic pages in lieu of Cerdip Packages.

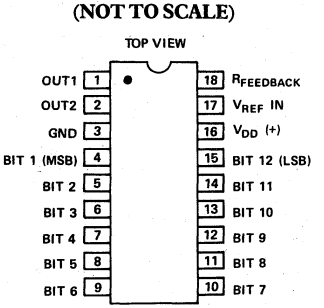
PRODUCT HIGHLIGHTS

Compatability: The AD7541A can be used as a direct replacement for any AD7541–type device. As with the Analog Devices AD7541, the digital inputs are TTL/CMOS compatible and have been designed to have a ±1μA maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced with premium grade versions having a maximum gain error of ±1LSB which eliminates the need for gain trimming.
2. Gain Error temperature coefficient has been reduced to 2ppm/°C typical and 5ppm/°C maximum.
3. Digital to analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.
5. Improvements in laser wafer trimming provides 1/2LSB max differential nonlinearity for top grade devices over the operating temperature range (vs. 1LSB on older 7541 types).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

PIN CONFIGURATION (NOT TO SCALE)



SPECIFICATIONS (V_{DD} = +15V, V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V unless otherwise specified)

Parameter	Version	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1LSB = ±0.024% of Full Scale
	K, B, T	±1/2	±1/2	LSB max	±1/2LSB = ±0.012% of Full Scale
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All grades guaranteed monotonic
	K, B, T	±1/2	±1/2	LSB max	to 12 bits, T_{min} to T_{max}
Gain Error	J, A, S	±6	±8	LSB max	Measured using internal R_{FB} and includes
	K, B, T	±1	±3	LSB max	effect of leakage current and gain T.C.
					Gain error can be trimmed to zero.
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	5	5	ppm/°C max	Typical value is 2ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K	±5	±10	nA max	All digital inputs = 0V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
OUT 2 (Pin 2)	J, K	±5	±10	nA max	All digital inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
REFERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical input resistance = 11kΩ.
					Typical input resistance temperature coefficient = −300ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic inputs are MOS gates. I_{IN} typ (25°C) = 1nA.
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0V
POWER SUPPLY REJECTION					
$\Delta Gain/\Delta V_{DD}$	All	±0.01	±0.02	%per% max	ΔV_{DD} = ±5%
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy is not guaranteed over this range.
I_{DD}	All	2	2	mA max	All digital inputs V_{IL} or V_{IH}.
		100	500	μA max	All digital inputs 0V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are Included for Design Guidance Only and are not Subject to Test.
V_{DD} = +15V, V_{IN} = +10V except where stated, V_{PIN1} = V_{PIN2} = 0V, Output Amp is AD544 except where stated.

Parameter	Version[1]	T_A = +25°C	T_A = T_{min}, T_{max}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input					OUT 1 Load = 100Ω C_{EXT} = 13pF
Change to 90% of Final Analog Output)	All	100	–	ns typ	Digital Inputs = 0V to V_{DD} or V_{DD} to 0V.
DIGITAL TO ANALOG GLITCH					V_{REF} = 0V. All digital inputs 0V to V_{DD} or V_{DD} to 0V.
IMPULSE	All	1000	–	nV-sec typ	Measured using Model 50K as output amplifier.
MULTIPLYING FEEDTHROUGH ERROR[3]					
(V_{REF} to OUT1)	All	1.0	–	mV p-p typ	V_{REF} = ± 10V, 10kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	–	μs typ	To 0.01% of full scale range.
					OUT1 load = 100Ω, C_{EXT} = 13pF.
					Digital inputs = 0V to V_{DD} or V_{DD} to 0V
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	$= V_{IH}$
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	$= V_{IL}$

NOTES
[1]Temperature range as follows: JN, KN versions: 0 to +70°C
AQ, BQ versions: −25°C to +85°C
SD, TD versions: −55°C to +125°C.
[2]Guaranteed by design but not production tested.
[3]To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (pin 16) to GND	+17V
V_{REF} (pin 17) to GND	±25V
V_{RFB} (pin 18) to GND	±25V
Digital Input Voltage to GND (pins 4-15)	−0.3V, V_{DD}
V_{PIN1}, V_{PIN2} to GND	−0.3V, V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	
Commercial Plastic (JN, KN versions)	0 to +70°C
Industrial Cerdip (AQ, BQ versions)	−25°C to +85°C
Extended Ceramic (SD, TD versions)	−55°C to +125°C
Storage Temperature	+65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full scale range or (sub)multiples of 1LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal full-scale output is $-\left(\frac{4095}{4096}\right)(V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 4, 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0pF.

GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used–that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

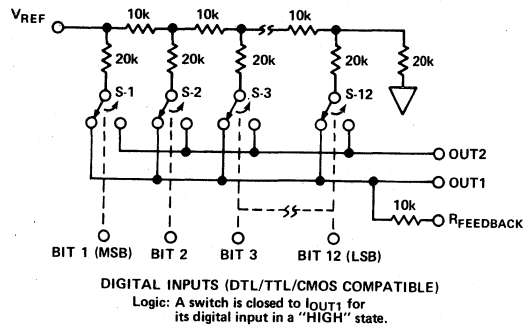


Figure 1. AD7541A Functional Diagram (Inputs "High")

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 2 and 3. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 200pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 70pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 3 is similar to Figure 2; however, the "ON" switches are now on terminal OUT1, hence the 200pF at that terminal.

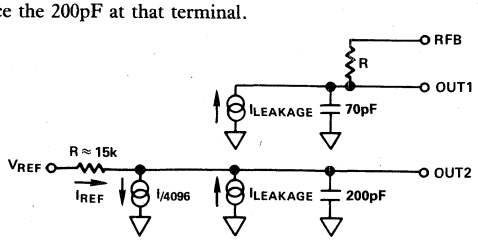


Figure 2. AD7541A DAC Equivalent Circuit All Digital Inputs LOW

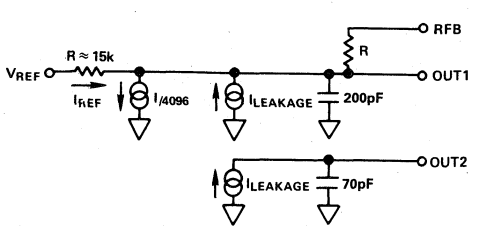


Figure 3. AD7541A DAC Equivalent Circuit All Digital Inputs HIGH

Applications

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.–load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq$ 10% of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 11kΩ). The AD544L is a high-speed implanted FET-input op amp with low factory-trimmed V_{OS}.

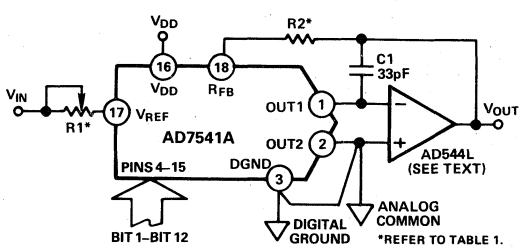


Figure 4. Unipolar Binary Operation

Trim Resistor	JN/AQ/SD	KN/BQ/TD
R1	100Ω	100Ω
R2	47Ω	33Ω

Table I. Recommended Trim Resistor Values vs. Grades

Binary Number in DAC MSB			LSB	Analog Output, V_{OUT}
1111	1111	1111		$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000		$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\,V_{IN}$
0000	0000	0001		$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000		0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 5 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 50pF) may be required for stability, depending on amplifier used.

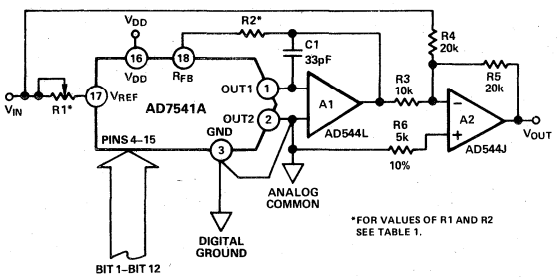


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
1111 1111 1111		$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001		$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000		0V
0111 1111 1111		$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000		$-V_{IN}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 5

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

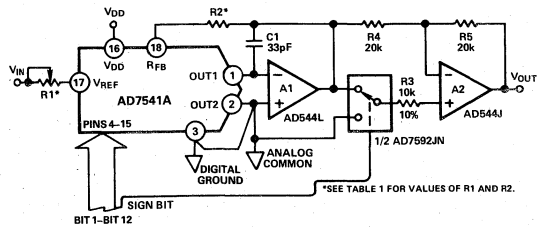


Figure 6. 12-Bit Plus Sign Magnitude Operation

Sign Bit	Binary Number in DAC MSB	LSB	Analog Output, V_{OUT}
0	1111 1111 1111		$+V_{IN}\cdot\left(\frac{4095}{4096}\right)$
0	0000 0000 0000		0 Volts
1	0000 0000 0000		0 Volts
1	1111 1111 1111		$-V_{IN}\cdot\left(\frac{4095}{4096}\right)$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn can cause a code dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

Digital Glitches: One cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This should be minimized by screening the analog pins of the AD7541A (pins 1, 2, 17, 18) from the digital pins by a ground track run between pins 2 and 3 and between pins 16 and 17 of the AD7541A. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and GND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7541A, particularly in circuits with high currents and fast rise and fall times.

Temperature Coefficients: The gain temperature coefficient of the AD7541A has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

Figure 7 shows the AD7541A connected in a voltage switching mode. OUT1 is connected to the reference voltage and OUT2 is connected to GND. The D/A converter output voltage is available at the V_{REF} pin (pin 17) and has a constant output impedance equal to R_{LDR}. The feedback resistor R_{FB} is not used in this circuit.

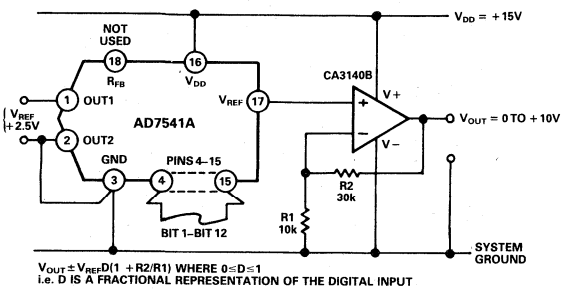


Figure 7. Single Supply Operation Using Voltage Switching Mode

The reference voltage must always be positive. If OUT1 goes more than 0.3V less than GND an internal diode will be turned on and a heavy current may flow causing device damage (the AD7541A is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices). Suitable references include the AD580 and AD584.

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltage at OUT1 should remain within 2.5V of GND, for a V_{DD} of 15V. If V_{DD} is reduced from 15V or the reference voltage at OUT1 increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A Converters, Publication Number G479–15–8/78 available from Analog Devices.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DAC Application Note, Publication Number E630–10–6/81 available from Analog Devices.

Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.

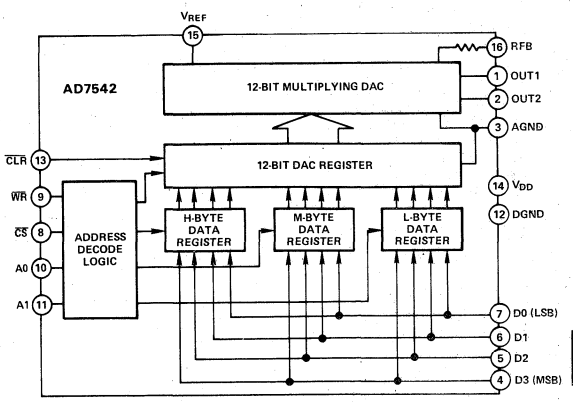
CMOS µP-Compatible 12-Bit DAC

AD7542

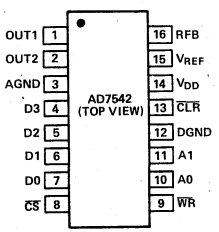
FEATURES

Resolution: 12 Bits
Nonlinearity: ±1/2LSB T_{min} to T_{max}
Low Gain Drift: 2ppm/°C typ, 5ppm/°C max
Microprocessor Compatible
Full 4-Quadrant Multiplication
Low Multiplying Feedthrough
Low Power Dissipation: 40mW max
Low Cost
Small Size: 16-Pin DIP
Latch Free (Protection Schottky Not Required)

AD7542 FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (NOT TO SCALE)



GENERAL DESCRIPTION

The AD7542 is a precision 12-bit CMOS multiplying DAC designed for direct interface to 4- or 8-bit microprocessors.

The functional diagram shows the AD7542 to consist of three 4-bit data registers, a 12-bit DAC register, address decoding logic and a 12-bit CMOS multiplying DAC. Data is loaded into the data registers in three 4-bit bytes, and subsequently transferred to the 12-bit DAC register. All data loading or data transfer operations are identical to the WRITE cycle of a static RAM. A clear input allows the DAC register to be easily reset to all zeros when powering up the device.

The AD7542 is manufactured using an advanced thin-film on monolithic CMOS fabrication process. Multiplying capability, low power dissipation, +5V operation, small size (16-pin DIP) and easy µP interface make the AD7542 ideal for many instrumentation, industrial control and avionics applications.

ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Gain Error +25°C	Temperature Range and Package[1] Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Extended (Ceramic) -55°C to +125°C
±1LSB	±12.3LSB	AD7542JN	AD7542AD	AD7542SD
±1/2LSB	±12.3LSB	AD7542KN	AD7542BD	AD7542TD
±1/2LSB	±1LSB	AD7542GKN	AD7542GBD	AD7542GTD

[1] Analog Devices is offering the AD7542 in chip carriers. For information contact the factory.

PACKAGE IDENTIFICATION[1]

Suffix "N": – Plastic DIP (N16B)
Suffix "D": – Ceramic DIP (D16B)

[1] See Section 19 for package outline information.

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SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GKN, GBD, GTD	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 5 & 6)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	DAC register loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	DAC register loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	DAC register loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 5 and 6). Data is loaded into data registers in 4-bit bytes.				
SWITCHING CHARACTERISTICS[5]	(See Figure 7)				
t_{WR}	120	220	220	ns min	t_{WR}: WRITE pulse width
t_{AWH}	50	65	65	ns min	t_{AWH}: Address-to-WRITE hold time
t_{CWH}	50	100	100	ns min	t_{CWH}: Chip select-to-WRITE hold time
t_{CLR}	200	300	300	ns min	t_{CLR}: Minimum CLEAR pulse width
Byte Loading					
t_{CWS}	60	130	130	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	80	180	180	ns min	t_{AWS}: Address valid-to-WRITE setup time
t_{DS}	50	65	65	ns min	t_{DS}: Data setup time
t_{DH}	50	65	65	ns min	t_{DH}: Data hold time
DAC Loading					
t_{CWS}	60	150	150	ns min	t_{CWS}: Chip select-to-WRITE setup time
t_{AWS}	120	240	240	ns min	t_{AWS}: Address valid-to-WRITE setup time
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	±5% for specified performance
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES
[1] Temperature Ranges as follows: AD7542JN, KN, GKN: 0 to +70°C
AD7542AD, BD, GBD: -25°C to +85°C
AD7542SD, TD, GTD: -55°C to +125°C
[2] See definitions on next page.
[3] Guaranteed but not tested.
[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to AGND . . . . . 0V, +7V
V_{DD} to DGND . . . . . 0V, +7V
AGND to DGND . . . . . V_{DD}
DGND to AGND . . . . . V_{DD}
Digital Input Voltage to DGND
(pins 4–11, 13) . . . . . –0.3V, +15.3V
V_{PIN1}, V_{PIN2} to AGND . . . . . –0.3V, +15V
V_{REF} to AGND . . . . . ±25V
V_{RFB} to AGND . . . . . ±25V
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . . .8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derates above +75°C by . . . . . .6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN, GKN versions). . . 0 to +70°C
Industrial Ceramic (AD, BD, GBD versions)
. . . . . –25°C to +85°C
Extended Ceramic (SD, TD, GTD versions) . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

9

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy on endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % or ppm of full scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1LSB change between any two adjacent codes. A specified differential nonlinearity of ±1LSB max over the operating temperature range insures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7542 would exhibit a gain of –4095/4096. Gain error is adjustable using external trims as shown in Figures 5 and 6.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with the DAC register loaded to all 0s or at OUT2 with the DAC register loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0s.

PIN	MNEMONIC	FUNCTION	PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground	7	D0	Data Input (LSB)
			8	$\overline{CS}$	Chip Select Input
			9	$\overline{WR}$	WRITE Input
2	OUT2	DAC current output bus. Normally terminated at ground	10	A0	Address Bus Input
			11	A1	Address Bus Input
3	AGND	Analog Ground	12	DGND	Digital Ground
4	D3	Data Input (MSB)	13	$\overline{CLR}$	Clear Input
5	D2	Data Input	14	V_{DD}	+5V Supply Input
6	D1	Data Input	15	V_{REF}	Reference Input
			16	R_{FB}	DAC Feedback Resistor

Table I. Pin Function Description

Analog Circuit Description

GENERAL CIRCUIT INFORMATION

The AD7542, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

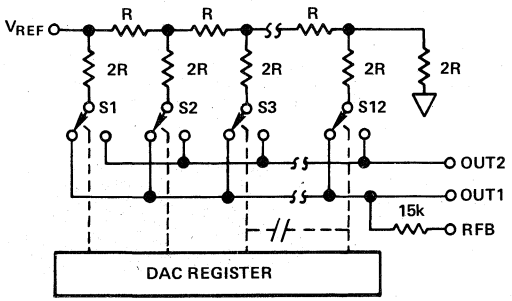


Figure 1. AD7542 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

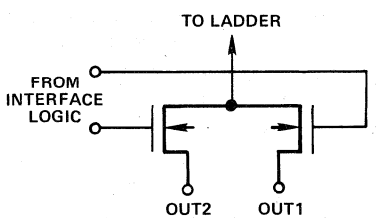


Figure 2. N-Channel Current Steering Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

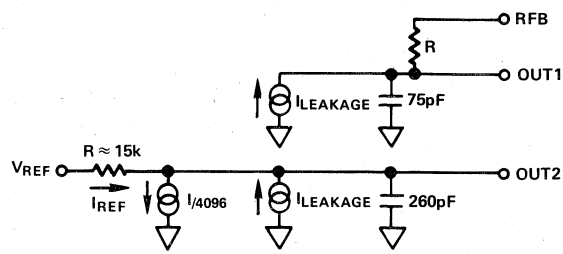


Figure 3. AD7542 DAC Equivalent Circuit All Digital Inputs LOW

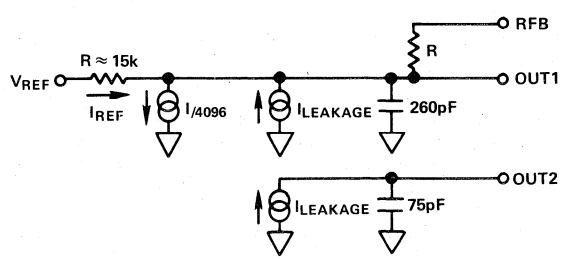


Figure 4. AD7542 DAC Equivalent Circuit All Digital Inputs HIGH

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leqslant 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

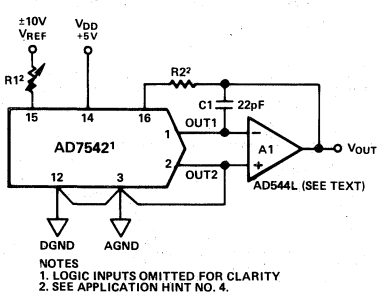


Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table II. Unipolar Binary Code Table for Circuit of Figure 5

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 6 and Table III illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0V (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for V_{OUT} = 0V). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 or 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

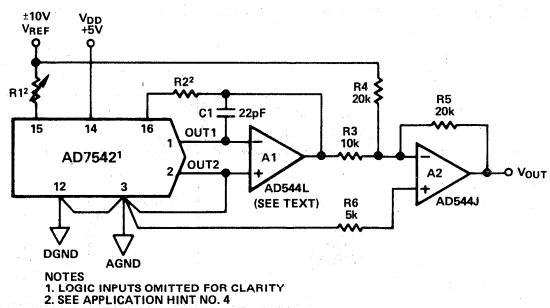


Figure 6. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table III. Bipolar Code Table for Offset Binary Circuit of Figure 6

INTERFACE LOGIC

INTERFACE LOGIC INFORMATION

The AD7542 is designed to interface as a memory-mapped output device.

A typical system configuration is shown in Figure 8 on next page. $\overline{CS}$ is the decoded *device* address, and is derived by decoding the three higher order address bits. A0 and A1 is the AD7542 *operation* address, and is decoded internally in the AD7542 to point to the desired loading operation (i.e., load high byte, middle byte, low byte or DAC register). Table IV shows the AD7542 truth table.

All data loading operations are identical to the write cycle of a RAM as shown in Figure 7.

Additionally, the CLR input allows the AD7542 DAC register to be cleared asynchronously to 0000 0000 0000. When operating the AD7542 in a unipolar mode (Figure 5), a CLEAR causes the DAC output to assume 0V. In the bipolar mode (Figure 6), a CLEAR causes the DAC output to go to $-V_{REF}$.

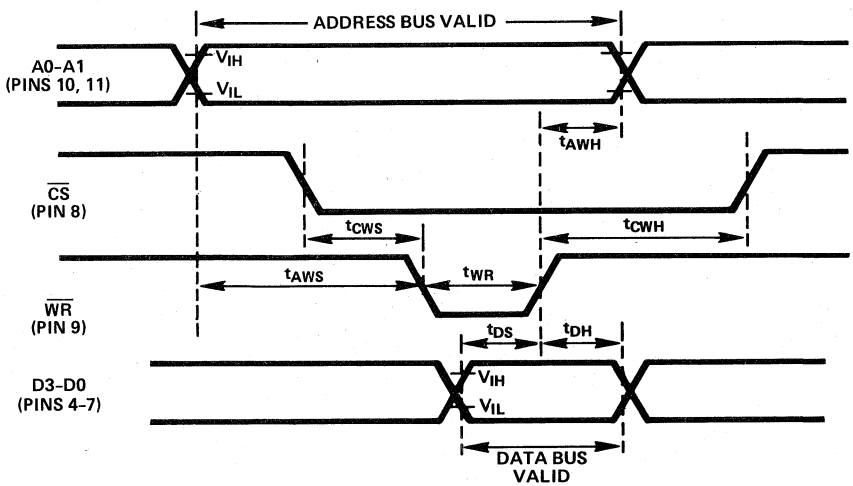
In summary:

1. The AD7542 DAC register can be asynchronously cleared with the $\overline{CLR}$ input.
2. Each AD7542 requires 4 locations in memory.
3. Performing any of the four basic loading operations (i.e. load low byte data register, middle byte data register, high byte data register or 12-bit DAC register) is accomplished by executing a memory WRITE operation to the applicable address location for the required DAC operation.

AD7542 Control Inputs					AD7542 Operation	
A_1	A_0	$\overline{CS}$	$\overline{WR}$	$\overline{CLR}$		
X	X	X	X	0	Resets DAC 12-Bit Register to Code 0000 0000 0000	
X	X	1	X	1	No Operation Device Not Selected	
0	0	0	↓	1	Load LOW Byte[5] Data Register On Edge As Shown	Load Applicable Data Register With Data At $D_0 - D_3$
0	1	0	↓	1	Load MIDDLE Byte[5] Data Register On Edge As Shown	
1	0	0	↓	1	Load HIGH Byte[5] Data Register On Edge As Shown	
1	1	0	⊓	1	Load 12-Bit DAC Register With Data In LOW Byte, MIDDLE Byte & HIGH Byte Data Registers[6]	

NOTES:
[1] 1 indicates logic HIGH
[2] 0 indicates logic LOW
[3] X indicates don't care
[4] ↓ indicates LOW to HIGH transition
[5] MSB → XXXX (high byte) XXXX (middle byte) XXXX (low byte) ← LSB
[6] These control signals are level triggered.

Table IV. AD7542 Truth Table



NOTE: TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 7. AD7542 Timing Diagram

APPLICATION HINTS

The AD7542 is a precision 12-bit multiplying DAC designed for system interface. To ensure system performance consistent with AD7542 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7542 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7542. In more complex systems where the AGND-DGND intertie is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7542 AGND and DGND pins (1N914 or equivalent).

2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}(2^{-n})$ where n is the number of bits exercised].

3. HIGH FREQUENCY CONSIDERATIONS: AD7542 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7542 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 5 and 6 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7542 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm/°C}$$

However, if the AD7542GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

5. For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

AD7542 INTERFACE TO MC6800

A typical 6800 system configuration is shown in Figure 8. Since the AD7542 contains four registers each AD7542 is assigned four locations in memory. A0 and A1 provides the operational addresses and are decoded internally to point to the desired register. Register loading is accomplished by executing a memory WRITE instruction to one of the four addresses. Table V gives a sample loading subroutine written in re-entrant form.

Choosing an arbitrary start address of PPQQ, locations PPQQ, PPQQ+1 and PPQQ+2 select the low, middle and high byte registers respectively while address PPQQ+3 selects the 12-bit DAC register. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1.

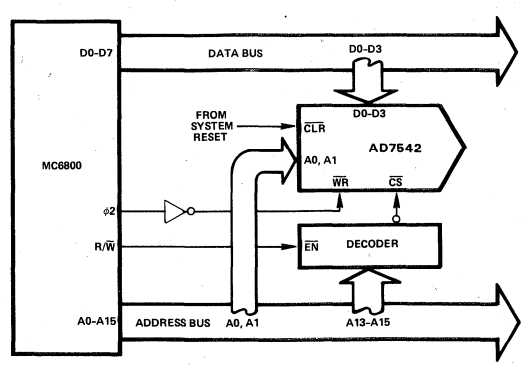


Figure 8. Interfacing the AD7542 to an MC6800 Microprocessor

```
        JSR     WWZZ
WWZZ    PSH A                   PUSH ACC. A ONTO STACK
        TPA
        PSH A                   PUSH CCR ONTO STACK
        LDA A   XXYY
        STA A   PPQQ            LOAD LOW BYTE
        ROR A
        ROR A
        ROR A
        ROR A
        STA A   PPQQ+1          LOAD MIDDLE BYTE
        LDA A   XXYY+1
        STA A   PPQQ+2          LOAD HIGH BYTE
        STA A   PPQQ+3          LOAD DAC REGISTER
        PUL A
        TAP                     POP CCR FROM STACK
        PUL A                   POP ACC. A FROM STACK
        RTS                     RETURN TO MAIN PROGRAM
```

Table V. Sample Routine for AD7542–6800 Interface

```
        CALL    7542
7542    PUSH    PSW             PUSH REGISTER CONTENTS
        PUSH    B               ONTO STACK
        PUSH    H
        LXI     H, XXYY
        MOV     A, M
        STA     PPQQ            LOAD LOW BYTE
        MVI     B, 04
LOOP    RAR
        DCR     B
        JNZ     LOOP
        STA     PPQQ+1          LOAD MIDDLE BYTE
        INX     H
        MOV     A, M
        STA     PPQQ+2          LOAD HIGH BYTE
        STA     PPQQ+3          LOAD DAC REGISTER
        POP     H               POP REGISTER CONTENTS
        POP     B               FROM STACK
        POP     PSW
        RET                     RETURN TO MAIN PROGRAM
```

Table VI. Sample Routine for AD7542–8085 Interface

AD7542 INTERFACE TO 8085

A typical 8085 system configuration is shown in Figure 9. The AD7542 $\overline{CS}$ input is decoded from the three high order address lines A13–A15. The 8085 $\overline{WR}$ output is directly connected to the $\overline{WR}$ input of the AD7542. Table VI gives a sample loading subroutine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY+1. The four most significant data bits are assumed to occupy the lower half of XXYY+1. As before, arbitrary addresses PPQQ to PPQQ+3 select the low byte, middle byte, high byte and DAC registers respectively.

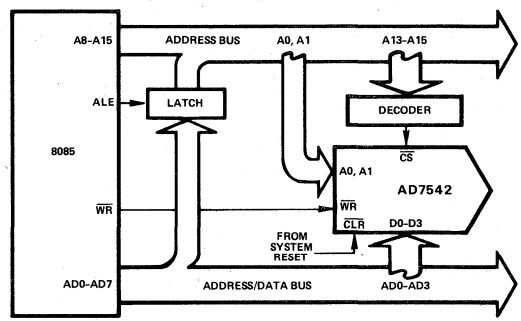


Figure 9. Interfacing the AD7542 to an 8085 Microprocessor

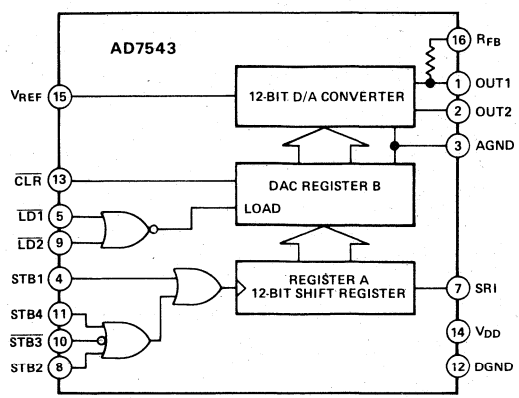
CMOS Serial Input 12-Bit DAC

AD7543

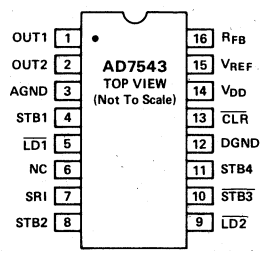
FEATURES

- Resolution: 12 Bits
- Nonlinearity: ±1/2LSB T_{min} to T_{max}
- Low Gain T.C.: 2ppm/°C typ, 5ppm/°C max
- Serial Load on Positive or Negative Strobe
- Asynchronous CLEAR Input for Initialization
- Full 4-Quadrant Multiplication
- Low Multiplying Feedthrough: 1LSB max @ 10kHz
- Requires no Schottky Diode Output Protection
- Low Power Dissipation: 40mW max
- +5V Supply
- Small Size: 16-Pin DIP
- Low Cost

AD7543 FUNCTIONAL DIAGRAM



PIN CONFIGURATION



GENERAL DESCRIPTION

The AD7543 is a precision 12-bit monolithic CMOS multiplying DAC designed for serial interface applications.

The DAC's logic circuitry consists of a 12-bit serial-in parallel-out shift register (Register A) and a 12-bit DAC input register (Register B). Serial data at the AD7543 SRI pin is clocked into Register A on the leading or trailing edge (user selected) of the strobe input. Once Register A is full its contents are loaded into Register B under control of the LOAD inputs.

Initialization is simplified by the use of the CLR input which provides an asynchronous reset of Register B.

Packaged in a 16-pin DIP, the AD7543 features excellent gain T.C. (2ppm/°C typ; 5ppm/°C max), +5V operation and latch-free operation. (No protection Schottky diodes required.)

ORDERING INFORMATION

Relative Accuracy T_{min} to T_{max}	Gain Error +25°C	Temperature Range and Package: Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Extended (Ceramic) -55°C to +125°C
±1LSB	±12.3LSB	AD7543JN	AD7543AD	AD7543SD
±1/2LSB	±12.3LSB	AD7543KN	AD7543BD	AD7543TD
±1/2LSB	±1LSB	AD7543GKN	AD7543GBD	AD7543GTD

PACKAGE IDENTIFICATION[1]

Suffix "N": – Plastic DIP (N16B)
Suffix "D": – Ceramic DIP (D16B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{DD} = +5V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, unless otherwise noted)

Parameter	Limit At T_A = +25°C	Limit At[1] T_A = 0, +70°C, -25°C & +85°C	Limit At[1] T_A = -55°C & +125°C	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Relative Accuracy[2]					
JN, AD, SD Versions	±1	±1	±1	LSB max	
KN, BD, TD Versions	±1/2	±1/2	±1/2	LSB max	
GKN, GBD, GTD Versions	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity[2]					
JN, AD, SD Versions	±2	±2	±2	LSB max	Monotonic to 11 bits from T_{min} to T_{max}
KN, BD, TD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
GKN, GBD, GTD Versions	±1	±1	±1	LSB max	Monotonic to 12 bits from T_{min} to T_{max}
Gain Error[2]					
JN, KN, AD, BD, SD, TD	±12.3	±13.5	±14.5	LSB max	Using internal RFB only (gain error can be
GKN, GBD, GTD	±1	±1	±2	LSB max	trimmed to zero using circuits of Figures 6 & 7)
Gain Temperature Coefficient					
ΔGain/ΔTemperature	5	5	5	ppm/°C max	Typical value is 2ppm/°C
Power Supply Rejection					
ΔGain/ΔV_{DD}	0.005	0.01	0.01	% per % max	V_{DD} = +4.75V to +5.25V
Output Leakage Current					
I_{OUT1} (Pin 4)	1	10	200	nA max	DAC Register loaded with all 0s
I_{OUT2} (Pin 5)	1	10	200	nA max	DAC Register loaded with all 1s
DYNAMIC PERFORMANCE					
Current Settling Time[3]	2.0	2.0	2.0	μs max	To 1/2LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{LD1}$ and $\overline{LD2}$, see Figure 5.
Multiplying Feedthrough Error[3]	2.5	2.5	2.5	mV p-p max	V_{REF} = ±10V, 10kHz sine wave
REFERENCE INPUT					
Input Resistance (pin 15)	8/15/25	8/15/25	8/15/25	kΩ min/typ/max	Typical temperature coefficient is -300ppm/°C
ANALOG OUTPUTS					
Output Capacitance					
C_{OUT1}[3]	75	75	75	pF max	Register B loaded to 0000 0000 0000
C_{OUT1}[3]	260	260	260	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	75	75	75	pF max	Register B loaded to 1111 1111 1111
C_{OUT2}[3]	260	260	260	pf max	Register B loaded to 0000 0000 0000
LOGIC INPUTS					
V_{INH} (Logic HIGH Voltage)	+3.0	+3.0	+3.0	V min	
V_{INL} (Logic LOW Voltage)	+0.8	+0.8	+0.8	V max	
I_{IN}[4]	1	1	1	μA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[3]	8	8	8	pF max	
Input Coding	12-Bit Unipolar Binary or 12-Bit Offset Binary (see Figures 6 and 7), serial load (MSB First)				
SWITCHING CHARACTERISTICS[5]					
t_{DS1}	50	100	100	ns min	(Serial Input to Strobe Setup Time) STB1 used as a strobe
t_{DS4}	0	0	0	ns min	STB4 used as a strobe
t_{DS3}	0	0	0	ns min	$\overline{STB3}$ used as a strobe
t_{DS2}	20	40	40	ns min	STB2 used as a strobe
t_{DH1}	30	60	60	ns min	(Serial Input to Strobe Hold Time) STB1 used as a strobe
t_{DH4}	80	160	160	ns min	STB4 used as a strobe
t_{DH3}	80	160	160	ns min	$\overline{STB3}$ used as a strobe
t_{DH2}	60	120	120	ns min	STB2 used as a strobe
t_{SRI}	80	160	160	ns min	SRI data pulse width
t_{STB1}	80	160	160	ns min	STB1 pulse width
t_{STB4}	100	200	200	ns min	STB4 pulse width
t_{STB3}	100	200	200	ns min	$\overline{STB3}$ pulse width
t_{STB2}	80	160	160	ns min	STB2 pulse width
t_{LD1}, t_{LD2}	150	300	300	ns min	Load pulse width
t_{ASB}	0	0	0	ns min	Min time between strobing LSB into Register A and loading Register B
t_{CLR}	200	400	400	ns min	CLR pulse width
POWER SUPPLY					
V_{DD} (Supply Voltage)	+5	+5	+5	V	
I_{DD} (Supply Current)	2.5	2.5	2.5	mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES

[1] Temperature ranges as follows: AD7543JN, KN, GKN: 0 to +70°C
AD7543AD, BD, GBD: -25°C to +85°C
AD7543SD, TD, GTD: -55°C to +125°C

[2] See Terminology on following page.

[3] Guaranteed but not tested.

[4] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[5] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to A_{GND} . . . . . 0V, +7V
V_{DD} to D_{GND} . . . . . 0V, +7V
A_{GND} to D_{GND} . . . . . V_{DD}
D_{GND} to A_{GND} . . . . . V_{DD}
Digital Input Voltage to D_{GND}
(pins 4 - 11, 13) . . . . . -0.3V, +15V
V_{PIN1}, V_{PIN2} to A_{GND} . . . . . -0.3V, +15V
V_{REF} to A_{GND} . . . . . ±25V
V_{RFB} to A_{GND} . . . . . ±25V
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
Operating Temperature Range
Commercial Plastic (JN, KN, GKN versions) . . . 0 to +70°C
Industrial Ceramic (AD, BD, GBD versons)
. . . . . -25°C to +85°C
Extended Ceramic (SD, TD, GTD versions)
. . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

9

TERMINOLOGY

RELATIVE ACCURACY
Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % or ppm of full-scale range or (sub) multiples of 1LSB.

DIFFERENTIAL NONLINEARITY
Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

GAIN ERROR
Gain is defined as the ratio of the DAC's Full Scale output to its reference input voltage. An *ideal* AD7543 would exhibit a gain of -4095/4096. Gain error is adjustable using external trims as shown in Figures 6 and 7.

OUTPUT LEAKAGE CURRENT
Current which appears at OUT1 with Register B loaded to all 0's or at OUT 2 with Register B loaded to all 1's.

MULTIPLYING FEEDTHROUGH ERROR
AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC register loaded to all 0's.

PIN	MNEMONIC	FUNCTION
1	OUT1	DAC current output bus. Normally terminated at op amp virtual ground
2	OUT2	DAC current output bus. Normally terminated at AGND
3	AGND	Analog Ground
4	STB1	Register A Strobe 1 input, see Table II
5	$\overline{LD1}$	DAC Register B Load 1 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
6	N/C	No Connection
7	SRI	Serial Data Input to Register A
8	STB2	Register A Strobe 2 input, see Table II
9	$\overline{LD2}$	DAC Register B Load 2 input. When $\overline{LD1}$ and $\overline{LD2}$ go low the contents of Register A are loaded into DAC Register B
10	$\overline{STB3}$	Register A Strobe 3 input, see Table II
11	STB4	Register A Strobe 4 input, see Table II
12	DGND	Digital Ground
13	$\overline{CLR}$	Register B CLEAR input (active LOW), can be used to asynchronously reset Register B to 0000 0000 0000
14	V_{DD}	+5V Supply Input
15	V_{REF}	Reference input. Can be positive or negative dc voltage or ac signal
16	R_{FB}	DAC Feedback Resistor

Table I. Pin Function Description

GENERAL CIRCUIT INFORMATION

The AD7543, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve N-channel current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

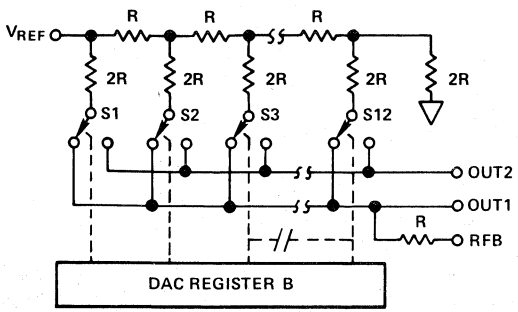


Figure 1. AD7543 Functional Diagram

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). The reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.

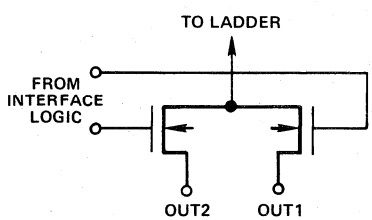


Figure 2. N-Channel Current Steering Switch

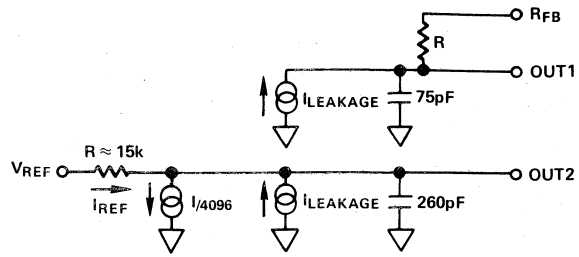


Figure 3. AD7543 DAC Equivalent Circuit All Digital Inputs LOW

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 3 and 4. In Figure 3 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I/4096 current source represents a constant 1 least significant bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N-channel switch is 260pF, as shown on the OUT2 terminal. The "OFF" switch capacitance is 75pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal OUT1, hence the 260pF at that terminal.

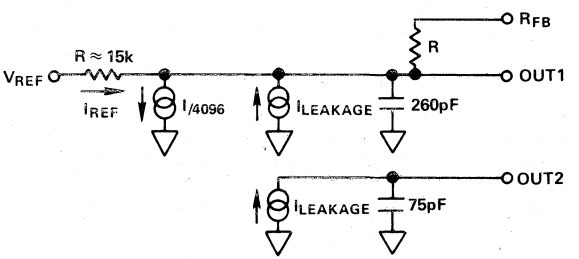


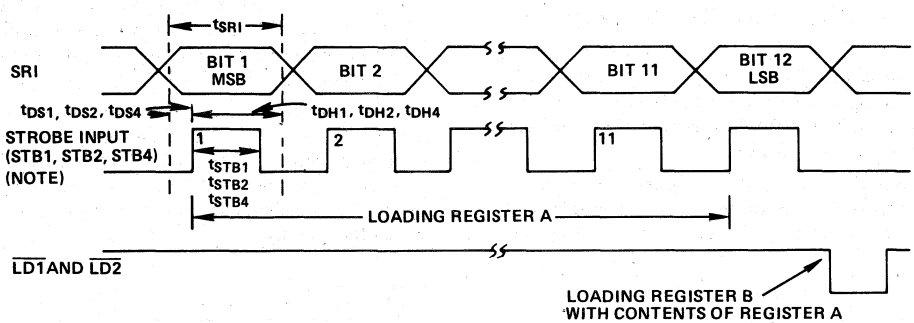
Figure 4. AD7543 DAC Equivalent Circuit All Digital Inputs HIGH

INTERFACE LOGIC INFORMATION

Shown in the AD8543 Functional Diagram Register A is a 12-bit shift register. Serial data appearing at pin SR1 is clocked into the shift register on the leading (rising) edge of STB1, STB2 or STB4 or on the leading (falling) edge of $\overline{STB3}$. Table II defines the various logic states required on the Register A control inputs, while Figure 5 illustrates the Register A loading sequence.

Once Register A is full, the data is transferred to Register B by bringing $\overline{LD1}$ and $\overline{LD2}$ momentarily LOW.

Register B can be asynchronously reset to 0000 0000 0000 by bringing $\overline{CLR}$ momentarily LOW. This allows the DAC output voltage to be set to a known condition, thus simplifying system initialization procedure. When operating the AD7543 in the unipolar circuit of Figure 6, a CLEAR causes the DAC output voltage to equal 0V. When using the bipolar circuit of Figure 7, a CLEAR causes the DAC output to equal $-V_{REF}$.



NOTE:
STROBE WAVEFORM IS INVERTED IF STB3 IS USED TO STROBE SERIAL DATA BITS INTO REGISTER A.

Figure 5. Timing Diagram

AD7543 Logic Inputs							AD7543 Operation	Notes
Register A Control Inputs				Register B Control Inputs				
STB4	$\overline{STB3}$	STB2	STB1	$\overline{CLR}$	$\overline{LD2}$	$\overline{LD1}$		
0	1	0	↓	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	1	↓	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
0	↑	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
↓	1	0	0	X	X	X	Data Appearing At SRI Strobed Into Register A	2,3
1	X	X	X				No Operation (Register A)	3
X	0	X	X					
X	X	1	X					
X	X	X	1					
				0	X	X	Clear Register B To Code 0000 0000 0000 (Asynchronous Operation)	1,3
				1	1	X	No Operation (Register B)	3
				1	X	1		
				1	0	0	Load Register B With The Contents Of Register A	3

NOTES:
1. CLR = 0 Asynchronously resets Register B to 0000 0000 0000, but has no effect on Register A.
2. Serial data is loaded into Register A MSB first, on edges shown ↓ is positive edge ↑ is negative edge.
3. 0 = Logic LOW, 1 = Logic HIGH, X = Don't Care.

Table II. AD7543 Truth Table

APPLYING THE AD7543

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. The logic inputs are omitted for clarity. With a dc reference voltage or current (positive or negative polarity) applied at pin 15, the circuit is a unipolar D/A converter. With an ac reference voltage or current (again of + or – polarity) the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table III.

R1 provides full scale trim capability [i.e.—load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10pF to 25pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq 10\%$ of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 15kΩ). The AD544L is a high-speed implanted FET-input op amp with low, factory-trimmed V_{OS}.

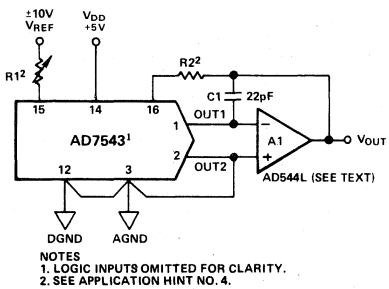


Figure 6. Unipolar Binary Operation (2-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -1/2\ V_{REF}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table III. Unipolar Binary Code Table for Circuit of Figure 6

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table IV illustrate the circuitry and code relationship for bipolar operation. With a dc reference (positive or negative polarity) the circuit provides offset binary operation. With an ac reference, the eleven LSBs provide digitally controlled attenuation of the ac reference while the MSB provides polarity control.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively, one can omit R1 and R2 and adjust the ratio of R3 to R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{REF} or by varying the value of R5.

As in unipolar operation, A1 must be chosen for low V_{OS} and low I_B. R3, R4 and R5 must be selected for matching and tracking. Mismatch of 2R3 to R4 causes both offset and Full Scale error. Mismatch of R5 to R4 to 2R3 causes Full Scale error. C1 phase compensation (10pF to 25pF) may be required for stability.

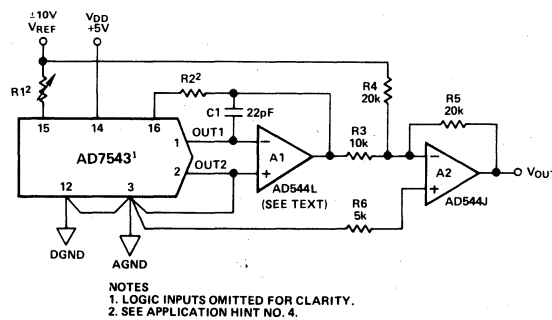


Figure 7. Bipolar Operation (4-Quadrant Multiplication)

BINARY NUMBER IN DAC REGISTER MSB LSB	ANALOG OUTPUT, V_{OUT}
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table IV. Bipolar Code Table for Offset Binary Circuit of Figure 7

APPLICATION HINTS

The AD7543 is a precision 12-bit multiplying DAC designed for serial interface. To ensure system performance consistent with AD7543 specifications, careful attention must be given to the following points:

1. GENERAL GROUND MANAGEMENT: Voltage differences between the AD7543 AGND and DGND cause loss of accuracy (dc voltage difference between the grounds introduces gain error. AC or transient voltages between the grounds cause noise injection into the analog output). The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7543. In more complex systems where the AGND-DGND connection is on the back-plane, it is recommended that diodes be connected back-to-back between the AD7543 AGND and DGND pins to prevent possible device damage.
2. OUTPUT AMPLIFIER OFFSET: CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of the DAC's output resolution over the temperature range of interest [output resolution = $V_{REF}\ 2^{-n}$ where n is the number of bits exercised].
3. HIGH FREQUENCY CONSIDERATIONS: AD7543 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This not only reduces closed loop bandwidth, but can also cause ringing or oscillation if the spurious pole frequency is less than the amplifier's 0dB crossover frequency. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.
4. GAIN TEMPERATURE COEFFICIENTS: The gain temperature coefficient of the AD7543 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to gain shifts of 2.0LSBs and 0.82LSBs respectively over a 100°C temperature range. When trim resistors are used to adjust full-scale range as shown in Figures 6 and 7 the temperature coefficient of R1 and R2 should be taken into account. It may be shown that the additional gain temperature coefficients introduced by R1 and R2 may be approximately expressed as follows:—

$$\text{Temperature Coefficient contribution due to R1} = -\frac{R_1}{R_{IN}}(\gamma_1 + 300)$$

$$\text{Temperature Coefficient contribution due to R2} = +\frac{R_2}{R_{IN}}(\gamma_2 + 300)$$

Where γ_1 and γ_2 are the temperature coefficients in ppm/°C of R1 and R2 respectively and R_{IN} is the DAC input resistance at the V_{REF} terminal (pin 2). For high quality wirewound resistors and trimming potentiometers γ is of the order of 50ppm/°C. It will be seen that if R1 and R2 are small compared with R_{IN}, their contribution to gain temperature coefficient will also be small. For the standard AD7543 gain error specification of ±12.3LSBs it is recommended that R1 = 120Ω and R2 = 60Ω. With γ = 50 these values result in an overall maximum gain error temperature coefficient of:

$$5 + \frac{0.06}{7}(50 + 300) = 8\text{ppm/°C}$$

However, if the AD7543GTD is used which has a specified gain error of ±1LSB, then with R1 = 10Ω and R2 = 5Ω the overall maximum gain temperature coefficient is increased by only 0.25ppm/°C. Where possible R1 should be a select on test fixed resistor since the resulting gain temperature coefficient will be tighter in all cases. For further gain T.C. information refer to application note, "Gain Error and Gain Temperature Coefficients of CMOS Multiplying DACs", Publication Number E630–10–6/81 available from Analog Devices.

5. For additional information on multiplying DACS refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

9

AD7543 INTERFACE TO MC6800

In this example, it is assumed that the 12-bit data is contained in two memory locations (0000 and 0001). The four most significant bits are assumed to occupy the lower half of memory location 0000. The eight least significant bits occupy memory location 0001. The data is presented bit by bit on the D7 line and strobed into the AD7543 by executing memory write instructions. In this case the strobe signal (STB1) is supplied by decoding address 2000, R/$\overline{W}$ and ϕ_2. A memory write instruction to a different address (4000) loads the data from Register A to the DAC register.

Figure 8 shows the interface circuitry and Table V gives a listing of the procedure.

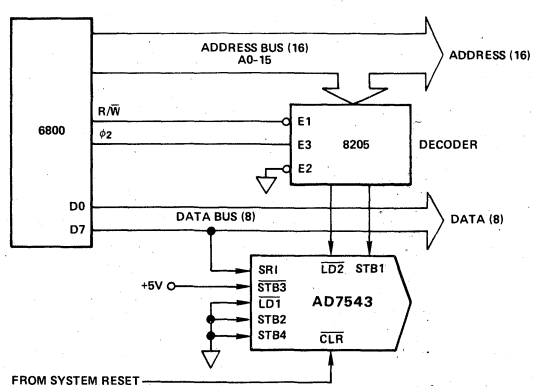


Figure 8. AD7543–MC6800 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
	LDA	B, 04	
	LDA	A, 0000	Load 4 Most Significant Bits
LOOP	ROL	A	Reposition in the Data
	DEC	B	in ACC A
	BNE	LOOP	
	LDA	B, 04	
	BSR	SHIFT	Output Data
	LDA	B, 08	
	LDA	A, 0001	Load 8 Least Significant Bits
	BSR	SHIFT	Output Data
	STA	A, 4000	Load DAC Register
	RTS		Return to Main Program
SHIFT	STA	A,2000	Strobe Data
	ROL	A	into AD7543
	DEC	B	
	BNE	SHIFT	
	RTS		

Table V. Sample Routine for AD7543–MC6800 Interface

LABEL	MNEMONIC	OPERAND	COMMENT
	MVI	B, 05	Shift Data Up to
LOOP	CALL	SHIFT	Most Significant
	DCR	B	Segment of HL with
	JNZ	LOOP	MSB as Carry
	MVI	B, OC	
LUP	MVI	A, 80	SOD Enable in ACC
	RAR		Shift in MSB of H
	SIM		Set Interrupt Mask
	STA	8000	Strobe Data into AD7543
	CALL	SHIFT	Get Next Bit into Carry
	DCR	B	
	JNZ	LUP	Go Back if Not Finished
	STA	A000	Load DAC Register of AD7543
	RET		Return to Main Program
SHIFT	MOV	A, L	Shift H and L Left
	RAL		One Place and
	MOV	L, A	Leave Uppermost Bit
	MOV	A, H	of H in Carry
	RAL		
	MOV	H, A	
	RET		

Table VI. Sample Routine for AD7543–8085 Interface

AD7543 INTERFACE TO MCS-85

Figure 9 shows the AD7543 interfaced to the 8085. This system makes use of the serial output facility (SOD) on the 8085.

The data is presented serially on the SOD line and strobed into the AD7543 by executing memory write instructions. In this example the strobe signal (STB2) is supplied by decoding address 8000 and $\overline{WR}$. A memory write instruction to a different address (A000) loads the DAC Register with Register A data. Table VI gives a listing of this procedure. Note, it is assumed that the required serial data is already present in right-justified format in Registers H and L when this procedure is implemented. Note that the sample routine of Table VI can be speeded up by replacing the SHIFT routine with a DAD H instruction.

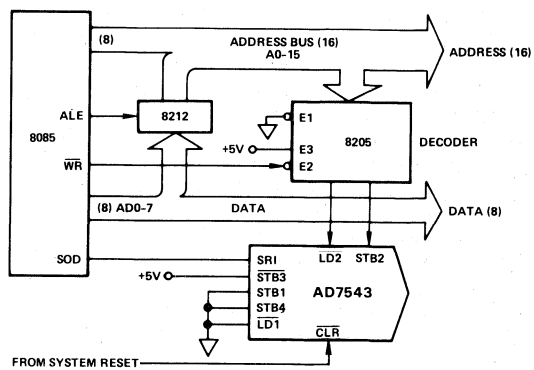


Figure 9. AD7543–8085 Interface

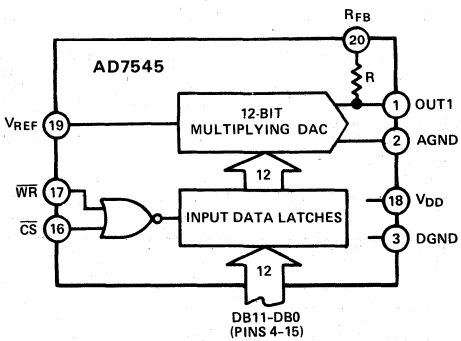
CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES

- 12-Bit Resolution
- Low Gain T.C.: 2ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5V to +15V Supply
- Small 20-Pin 0.3" DIP
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment

AD7545 FUNCTIONAL BLOCK DIAGRAM



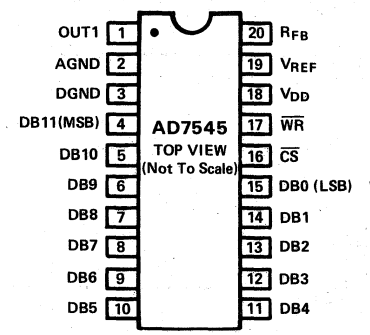
GENERAL DESCRIPTION

The AD7545 is a monolithic 12-bit CMOS multiplying DAC with on-board data latches. It is loaded by a single 12-bit wide word and interfaces directly to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

The AD7545 can be used with any supply voltage from +5V to +15V. With CMOS logic levels at the inputs the device dissipates less than 0.5mW for V_{DD} = +5V.

PIN CONFIGURATION



ORDERING INFORMATION

Relative Accuracy	Maximum Gain Error T_A = +25°C V_{DD} = +5V	Temperature Range and Package: Plastic 0 to +70°C	Cerdip[1] -25°C to +85°C	Ceramic -55°C to +125°C
±2LSB	±20LSB	AD7545JN	AD7545AQ	AD7545SD
±1LSB	±10LSB	AD7545KN	AD7545BQ	AD7545TD
±1/2LSB	±5LSB	AD7545LN	AD7545CQ	AD7545UD
±1/2LSB	±1LSB	AD7545GLN	AD7545GCQ	AD7545GUD

NOTES

[1] Analog Devices reserves the right to ship ceramic packages in lieu of Cerdip packages.

PACKAGE IDENTIFICATION[1]

Suffix "N": – Plastic DIP (N20B)
Suffix "Q": – Cerdip (Q20B)
Suffix "D": – Ceramic DIP (D20B)

[1] See Section 19 for package outline information.

SPECIFICATIONS (V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified)

Parameter	Version	V_{DD} = +5V Limits T_A = +25°C	T_{min}, T_{max} [1]	V_{DD} = +15V Limits T_A = +25°C	T_{min}, T_{max} [1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
Relative Accuracy	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{min} to T_{max}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{min} to T_{max}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5 and 6
Gain Temperature Coefficient[3] ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2ppm/°C for V_{DD} = +5V
DC Supply Rejection[3] ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0-DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	μs max	To 1/2LSB. OUT 1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.
Propagation Delay[3] (from Digital Input Change to 90% of final Analog Output)	All	300	–	250	–	ns max	OUT1 LOAD = 100Ω C_{EXT} = 13pF[4]
Digital to Analog Glitch Impulse	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5] At OUT1	All	5	5	5	5	mV p-p typ	V_{REF} = ±10V, 10kHz Sinewave
REFERENCE INPUT							
Input Resistance	All	7	7	7	7	kΩ min	Input Resistance TC = -300ppm/°C typ
(Pin 19 to GND)		25	25	25	25	kΩ max	Typical Input Resistance = 11kΩ
ANALOG OUTPUTS							
Output Capacitance[3]							
C_{OUT1}	All	70	70	70	70	pF max	DB0-DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V
C_{OUT1}	All	200	200	200	200	pF max	DB0-DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V
DIGITAL INPUTS							
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6] I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0-DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS							
Chip Select to Write Setup Time	All	280	380	180	200	ns min	See Timing Diagram on next page
t_{CS}		200	270	120	150	ns typ	
Chip Select to Write Hold Time t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time	All	140	210	90	120	ns min	
t_{DS}		100	150	60	80	ns typ	
Data Hold Time							
t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0V or V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0V or V_{DD}

NOTES

[1] Temperature Ranges as follows: JN, KN, LN, GLN: 0 to +70°C
AQ, BQ, CQ, GCQ: -25°C to +85°C
ST, TD, UD, GUD: -55°C to +125°C

[2] This includes the effect of 5ppm max gain TC.

[3] Guaranteed but not tested.

[4] DB0-DB11 = 0V to V_{DD} or V_{DD} to 0V.

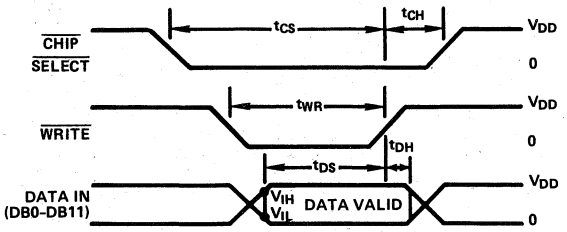
[5] Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

[6] Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.

[7] Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.

WRITE CYCLE TIMING DIAGRAM



MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0-DB11) inputs.	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0-DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
All input signal rise and fall times measured from 10% to 90% of V_{DD}.
Timing measurement reference level is $V_{IH} + V_{IL}/2$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND . . . . . -0.3V, +17V
Digital Input Voltage to DGND . . . . . -0.3V, V_{DD}
V_{RFB}, V_{REF} to DGND . . . . . ±25V
V_{PIN1} to DGND . . . . . -0.3V, V_{DD}
AGND to DGND . . . . . -0.3V, V_{DD}
Power Dissipation (Any Package) to 75°C 450mW
Derates above 75°C by . . . . . 6mW/°C
Operating Temperature
Commercial (JN, KN, LN, GLN) Grades . . . . . 0 to +70°C
Industrial (AQ, BQ, CQ, GCQ) Grades. . . . -25°C to +85°C
Extended (SD, TD, UD, GUD) Grades. . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds). . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

9

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TERMINOLOGY

RELATIVE ACCURACY: The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full scale points have been adjusted. This is an end point linearity measurement.

DIFFERENTIAL NONLINEARITY: The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1LSB then it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY: This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reached 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE: This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVsecs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33pF.

CIRCUIT INFORMATION – D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A converter section of the AD7545 and Figure 2 gives an approximate equivalent circuit. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

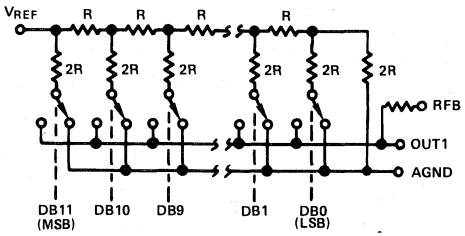


Figure 1. Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

One of the current switches is shown in Figure 2. The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

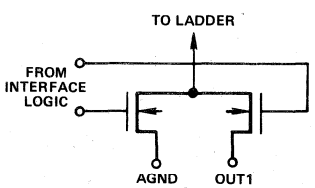


Figure 2. N-Channel Current Steering Switch

CIRCUIT INFORMATION–DIGITAL SECTION

Figure 3 shows the digital structure for one bit.

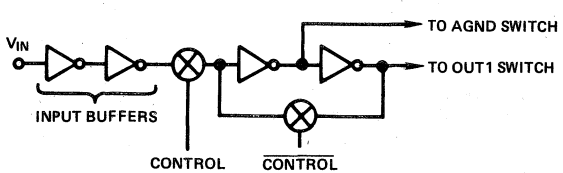


Figure 3. Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range $5 \leqslant V_{DD} \leqslant 15$ volts. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. The "G" versions (AD7545GLN, AD7545GCQ, AD7545GUD) have a guaranteed maximum gain error of ±1LSB at +25°C (V_{DD} = +5V) and in many applications it should be possible to dispense with gain trim resistors altogether. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that all the circuits of Figures 4, 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leqslant V_{IN} \leqslant +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

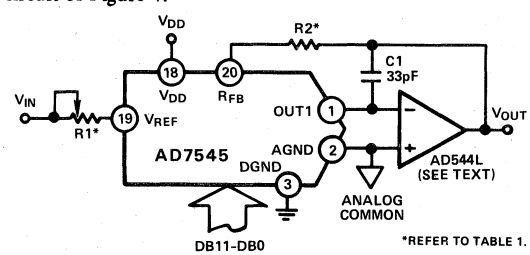


Figure 4. Unipolar Binary Operation

TRIM RESISTOR	JN/AQ/SD	KN/BQ/TD	LN/CQ/UD	GLN/GCQ/GUD
R1	500Ω	200Ω	100Ω	20Ω
R2	150Ω	68Ω	33Ω	6.8Ω

Table I. Recommended Trim Resistor Values vs. Grades for V_{DD} = +5V

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0 Volts

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software

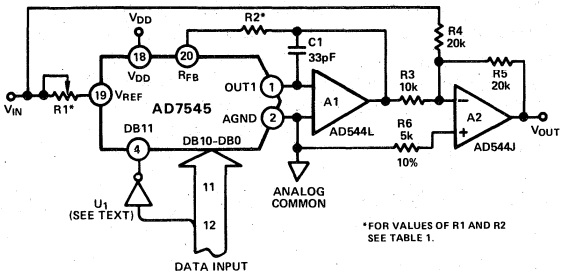


Figure 5. Bipolar Operation (2's Complement Code)

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \cdot \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{\frac{2048}{2048}\right\}$

Table III. 2's Complement Code Table for Circuit of Figure 5

using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wirewound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

Figure 6 shows an alternative method of achieving bipolar output. The circuit operates with sign plus magnitude code and has the advantage that it gives 12-bit resolution in each quadrant compared with 11-bit resolution per quadrant for

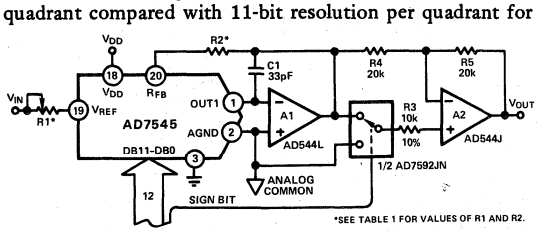


Figure 6. 12-Bit Plus Sign Magnitude D/A Converter

the circuit of Figure 5. The AD7592 is a fully protected CMOS change-over switch with data latches. R4 and R5 should match each other to 0.01% to maintain the accuracy of the D/A converter. Mismatch between R4 and R5 introduces a gain error.

Sign Bit	Binary Numbers in DAC Register			Analog Output
0	1111	1111	1111	$+V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$
0	0000	0000	0000	0 Volts
1	0000	0000	0000	0 Volts
1	1111	1111	1111	$-V_{IN} \cdot \left\{\frac{4095}{4096}\right\}$

Note: Sign bit of "0" connects R3 to GND.

Table IV. 12-Bit Plus Sign Magnitude Code Table for Circuit of Figure 6

APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse $\overline{WR}$ so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by screening the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid screening at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5 volts. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

SINGLE SUPPLY OPERATION

The ladder termination resistor of the AD7545 (Figure 1) is connected to AGND. This arrangement is particularly suitable for single supply operation because OUT 1 and AGND may be biased at any voltage between DGND and V_{DD}. OUT1 and AGND should never go more than 0.3 volts less than DGND or an internal diode will be turned on and a heavy current may flow which will damage the device. (The AD7545 is, however, protected from the SCR latch-up phenomenon prevalent in many CMOS devices.)

Figure 7 shows the AD7545 connected in a voltage switching mode. OUT1 is connected to the reference voltage and AGND is connected to DGND. The D/A converter output voltage is available at the V_{REF} pin and has a constant output impedance equal to R. R_{FB} is not used in this circuit.

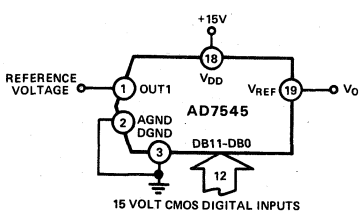


Figure 7. Single Supply Operation Using Voltage Switching Mode

The loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the behavior of the reference voltage with changing load conditions. To maintain linearity, the voltages at OUT1 and AGND should remain within 2.5 volts of each other, for a V_{DD} of 15 volts. If V_{DD} is reduced from 15V or the differential voltage between OUT1 and AGND is increased to more than 2.5V the differential nonlinearity of the DAC will increase and the linearity of the DAC will be degraded. Figures 8 and 9 show typical curves illustrating this effect for various values of reference voltage and V_{DD}. If the output voltage is required to be offset from ground by some value, then OUT1 and AGND may be biased up. The effect on linearity and differential nonlinearity will be the same as reducing V_{DD} by the amount of the offset.

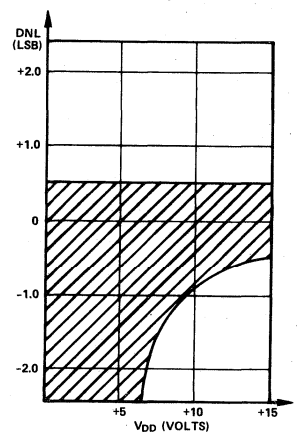


Figure 8. Differential Nonlinearity vs. V_{DD} for Figure 7 Circuit. Reference Voltage = 2.5 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C and U Grades.

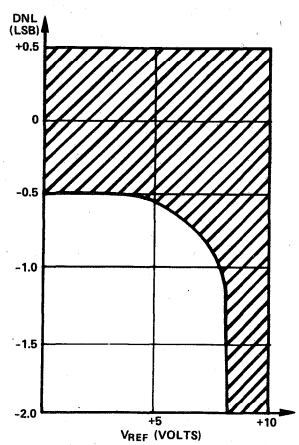


Figure 9. Differential Nonlinearity vs. Reference Voltage for Figure 7 Circuit. V_{DD} = 15 Volts. Shaded Area Shows Range of Values of Differential Nonlinearity that Typically Occur for L, C, and U Grades.

The circuits of Figures 4, 5 and 6 can all be converted to single supply operation by biasing AGND to some voltage between V_{DD} and DGND. Figure 10 shows the 2's Complement Bipolar circuit of Figure 5 modified to give a range from +2V to +8V about a "pseudo-analog ground" of 5V. This voltage range would allow operation from a single V_{DD} of +10V to +15V. The AD584 pin-programmable reference fixes AGND at +5V. V_{IN} is set at +2V by means of the series resistors R1 and R2. There is no need to buffer the V_{REF} input to the AD7545 with an amplifier because the input impedance of the D/A converter is constant. Note, however, that since the temperature coefficient of the D/A reference input resistance is typically -300ppm/°C, applications which experience wide temperature variations may require a buffer amplifier to generate the +2.0V at the AD7545 V_{REF} pin. Other output voltage ranges can be obtained by changing R4 to shift the zero point and (R1 + R2) to change the slope, or gain of the D/A transfer function. V_{DD} must be kept at least 5V above OUT1 to ensure that linearity is preserved.

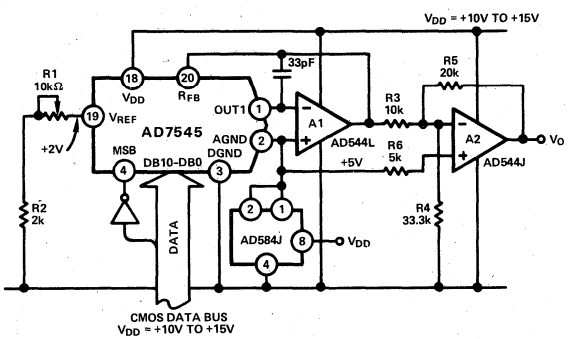


Figure 10. Single Supply "Bipolar" 2's Complement D/A Converter

MICROPROCESSOR INTERFACING OF THE AD7545

The AD7545 can interface directly to both 8- and 16-bit microprocessors via its 12-bit wide data latch using standard $\overline{CS}$ and $\overline{WR}$ control signals.

A typical interface circuit for an 8-bit processor is shown in Figure 11. This arrangement uses two memory addresses, one for the lower 8 bits of data to the DAC and one for the upper 4 bits of data into the DAC via the latch.

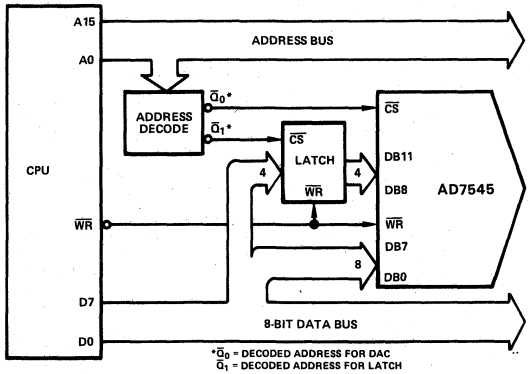


Figure 11. 8-Bit Processor to AD7545 Interface

Figure 12 shows an alternative approach for use with 8-bit processors which have a full 16-bit wide address bus such as 6800, 8080, Z80. This technique uses the 12 lower

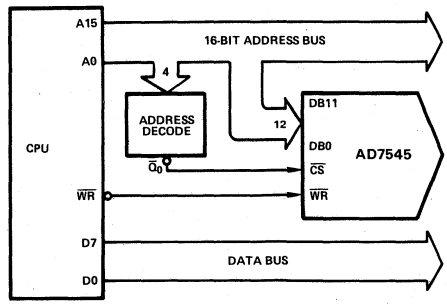


Figure 12. Connecting the AD7545 to 8-Bit Processors via the Address Bus

address lines of the processor address bus to supply data to the DAC, thus each AD7545 connected in this way uses 4k bytes of address locations. Data is written to the DAC using a single memory write instruction. The address field of the instruction is organized so that the lower 12 bits contain the data for the DAC and the upper 4 bits contain the address of the 4k block at which the DAC resides.

SUPPLEMENTAL APPLICATION MATERIAL

For further information on CMOS multiplying D/A converters the reader is referred to the following texts:

Application Guide to CMOS Multiplying D/A converters available from Analog Devices, Publication Number G479.

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACS – Application Note, Publication Number E630–10–6/81 available from Analog Devices.

Analog-Digital Conversion Notes – available from Analog Devices, price $5.95.

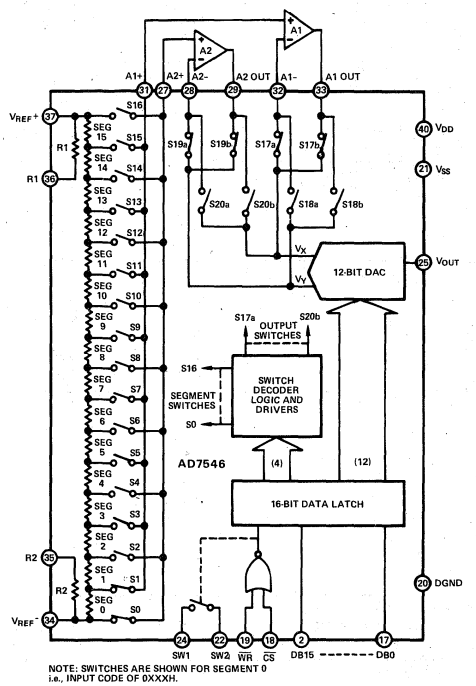
CMOS 16-Bit Voltage Out DAC*

AD7546

FEATURES

Monotonic to 16 Bits Over Temperature
On-Chip Deglitch Switch
Unipolar and Bipolar Operation
Microprocessor Compatible
TTL/CMOS Compatible Latched Inputs
Voltage Output (Constant Output Impedance)
Low Cost
Low Power Consumption: 50mW typ

AD7546 FUNCTIONAL BLOCK DIAGRAM



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0 i.e., INPUT CODE OF 0XXXH.

GENERAL DESCRIPTION

The AD7546 is a 16-bit voltage-output DAC with input data latches for interfacing to 16-bit microprocessors. It uses a novel design consisting of a 12-bit R-2R DAC, operated in the voltage switching mode, which is supplied with a reference voltage from a 4-bit segment DAC under the control of the four most significant bits. A monolithic CMOS device, the AD7546 offers outstanding differential nonlinearity specifications and monotonicity from 14 to 16 bits.

An on-chip deglitch switch which is synchronized with the latch loading signal is provided for use with track/hold circuits.

ORDERING INFORMATION

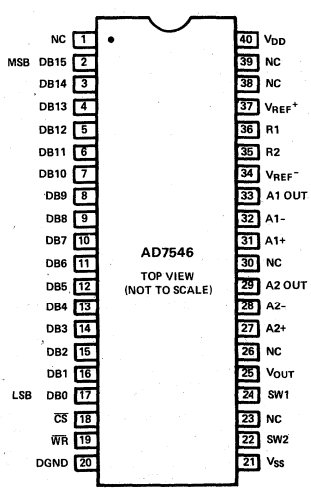
Relative Accuracy	Differential Nonlinearity	Temperature Range - Package: Plastic 0 to +70°C	Temperature Range - Package: Ceramic -25°C to +85°C	Monotonic Range
±0.05%	±0.006%	AD7546JN	AD7546AD	14 Bits
±0.012%	±0.0015%	AD7546KN	AD7546BD	16 Bits

PACKAGE IDENTIFICATION[1]

Suffix "D": – Ceramic DIP (D40A)
Suffix "N": – Plastic DIP – (N40A)

[1] See Section 19 for package outline information.

PIN CONFIGURATION



*Patent Pending.

SPECIFICATIONS (VDD = +15V, V_{SS} = -5V, (V_{REF}+ = +4V, V_{REF}- = -4V, A1, A2 = AD544K, unless otherwise noted)

Parameter	Limit at T_A = +25°C	Limit at T_A = T_{min}, T_{max}[1]	Units	Conditions/Comments
ACCURACY				
Resolution				
All Grades	16	16	Bits	
Relative Accuracy				
AD7546JN, AD	±0.05	±0.05	% FSR max[2]	This is an end-point linearity specification
AD7546KN, BD	±0.012	±0.012	% FSR max	assuming zero offset voltage for A1, A2.
Differential Nonlinearity				
AD7546JN, AD	±0.006	±0.006	% FSR max	Guaranteed monotonic to 14 bits (DB0 and DB1 = 0).
AD7546KN, BD	±0.0015	±0.0015	% FSR max	Guaranteed monotonic to 16 bits over temperature.
Gain Error[3]				
Positive Full Scale	-0.02	-0.02	% FSR max	DAC latches loaded with $FFFF_H$
Negative Full Scale	-0.02	-0.02	% FSR max	DAC latches loaded with 0000_H
Gain T.C.[4,5]	±2	±2	ppm of FS/°C max	
dc Supply Rejection[5]				
$\Delta Gain/\Delta V_{DD}$	100	100	µV per V typ	V_{DD} = +14.5V to +15.5V
DYNAMIC PERFORMANCE				
Voltage Settling Time[5,6]	4	4	µs typ	To 0.01% of final value.
	5	5	µs typ	To 0.003% of final value.
	10	10	µs typ	To 0.00076% of final value. Measured using the circuit of Figure 6.
SWITCHING CHARACTERISTICS[5,7]				With +5V input logic levels.
t_{CWS}	0	0	ns min	Chip select to WRITE setup time
t_{CWH}	0	0	ns min	Chip select to WRITE hold time
t_{WR}	400	600	ns min	WRITE pulse width
t_{DS}	200	300	ns min	Data setup time
t_{DH}	100	150	ns min	Data hold time
REFERENCE INPUTS				
Resistance				
V_{REF}^+ to V_{REF}^-	20/32/50	20/32/50	kΩ, min/typ/max	Typical Resistance TC is -300ppm/°C
R1, R2	20/30/50	20/30/50	kΩ, min/typ/max	
R1, R2 Match				
AD7546JN, AD	0.5	0.5	% max	Typical TC of R1, R2 match is ±1ppm/°C
AD7546 KN, BD	0.1	0.1	% max	
Voltage Range				
V_{REF}^+	+5	+5	V max	The AD7546 is tested with V_{REF}^+ =
V_{REF}^-	-5	-5	V max	+4V, V_{REF}^- = -4V
ANALOG OUTPUT				
R_{OUT} (Output Resistance)	10/15/25	10/15/25	kΩ, min/typ/max	
C_{OUT} (Output Capacitance)[5]	8	8	pF max	
DEGLITCH SWITCH				
R_{ON}	300/600	450/900	Ω typ/max	V_{SW} = ±4V, I_{SW} = 100µA
$I_{LEAKAGE}$, SW2 (pin 22)	1	10	nA max	Off switch leakage. V_{SW1} = ±4V, V_{SW2} = ∓4V.
LOGIC INPUTS				
V_{IH}	2.4	2.4	V min	
V_{IL}	0.8	0.8	V max	
I_{IN} (Input Leakage Current)	1	1	µA max	V_{IN} = 0V or V_{DD}
C_{IN} (Input Capacitance)[5]	8	8	pF max	
Input Coding	16-Bit Unipolar Binary			See Figure 7
	16-Bit Offset Binary			See Figure 8
POWER SUPPLY				
V_{DD}	+15	+15	V	±5% for specified performance
V_{SS}	-5	-5	V	±5% for specified performance
I_{DD}	4	4	mA max	V_{IN} = V_{IL} or V_{IH}
I_{DD}	200	200	µA max	V_{IN} = 0V or V_{DD}, $\overline{CS}$ = $\overline{WR}$ = 0V
I_{SS}	100	100	µA max	

NOTES

[1] Temperature ranges as follows: AD7546JN, KN; 0 to +70°C
AD7546AD, BD; -25°C to +85°C

[2] FSR is Full Scale Range.

[3] These gain error specifications have assumed an input offset voltage for A2 of 0V. Actual gain error figures should include amplifier A2 input offset voltage.

[4] Gain TC specifications have assumed a zero input offset voltage drift with temperature for A2. Actual gain TC figures should include amplifier A2 drift with temperature.

[5] Guaranteed but not tested.

[6] Voltage settling time will be a function of the time constant RC seen at the buffer amplifier inputs. The resistance component of this time constant is the equivalent output impedance of the resistor string and will vary depending on which segment is decoded. Maximum equivalent resistance occurs at mid-scale. Worst case settling thus occurs from zero to mid-scale or from full-scale to mid-scale.

[7] +15V logic can be used to reduce power dissipation but no improvement is achieved in the timing specifications. All control signals are measured with $t_r = t_f$ = 20ns for +5V logic and timed from $\frac{(V_{IH} + V_{IL})}{2}$. Data is timed from V_{IH} or V_{IL}. Sample tested at +25°C to ensure conformance.

Specifications subject to change without notice.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

(Note that cavity lid on Ceramic Package is Electrically Connected to V_{DD})

V_{DD} (Pin 40) to DGND . . . . . 0V, +17V
V_{SS} (Pin 21) to DGND . . . . . 0V, -7V
V_{REF}^+ (Pin 37) to DGND . . . . . V_{DD}, V_{REF}^-
V_{REF}^- (Pin 34) to DGND . . . . . V_{SS}, V_{REF}^+
R1 (Pin 36) to DGND . . . . . ±25V
R2 (Pin 35) to DGND . . . . . ±25V
*DB12 LOW (S17, S19 Closed)
A1 – (Pin 32) or A1 Out (Pin 33)
to A2 - (Pin 28) or A2 Out (Pin 29) . . . . . -0.3V, +5V
*DB12 HIGH (S18, S20 Closed)
A2 – (Pin 28) or A2 Out (Pin 29)
to A1 - (Pin 32) or A1 Out (Pin 33) . . . . . -0.3V, +5V
A1 + (Pin 31), A2 + (Pin 27) to DGND . . . . . V_{SS}, V_{DD}
V_{OUT} (Pin 25) to DGND . . . . . ±25V
SW1 (Pin 24), SW2 (Pin 22) to DGND . . . . . V_{SS}, V_{DD}
Digital Inputs (Pins 2 -19) to DGND . . . . . -0.3V, +17V
Power Dissipation (Package)
Plastic (AD7546JN, KN)
Up to +50°C 1200mW
Derates above +50°C by . . . . . 12mW/°C
Ceramic (AD7546AD, BD)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C

*The absolute maximum rating refers to the voltage V_X–V_Y across the inputs of the 12-bit DAC. See Functional Diagram of Figure 2.

STRESS
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

9

ACCURACY SPECIFICATIONS

Two types of nonlinearity errors exist in D/A converters, relative accuracy and differential nonlinearity. Relative accuracy is the error resulting from departure of the DAC transfer characteristic from the ideal straight line drawn between measured zero and measured full scale.

Differential Nonlinearity (DNL) is the difference between the measured output voltage change between two adjacent input codes and the ideal change of 1LSB. A specified DNL of ±1 LSB guarantees monotonicity (i.e. the output voltage will never decrease for any increase in input code). To ensure that the output voltage will always increase when the input code is increased requires a DNL specification of less than ±1LSB. This point is illustrated in Figure 1.

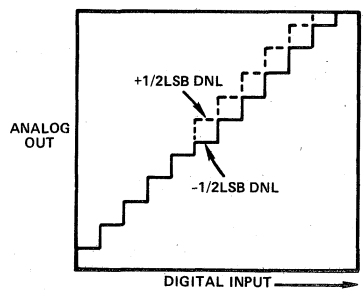


Figure 1a. ±1/2LSB Differential Nonlinearity

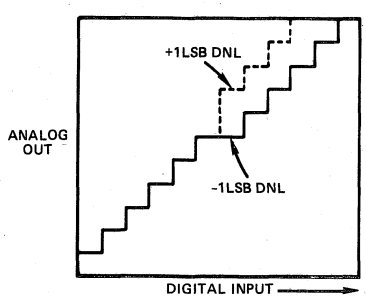


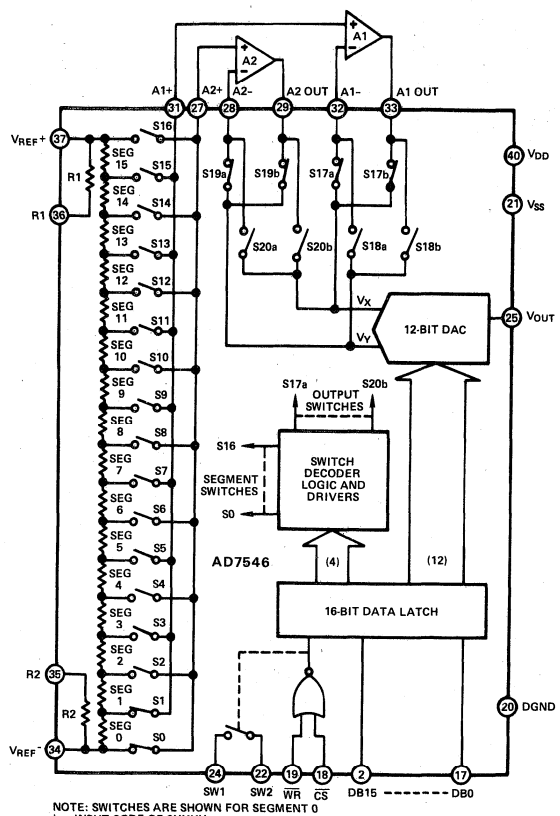
Figure 1b. ±1LSB Differential Nonlinearity

Many applications require high resolution DACs with guaranteed monotonicity (but not necessarily with an equivalent relative accuracy) for fine control of temperature, position and other physical parameters. Good differential nonlinearity is essential in such systems to maintain an even degree of control over the full range. Monotonicity is particularly important in feedback systems where nonmonotonic behavior constitutes positive feedback which may lead to catastrophic results. To ensure monotonic behavior of a particular device, only those bits which are guaranteed monotonic for that grade should be exercised e.g., for the AD7546JN (14-bit monotonic), DB0 and DB1 should be tied LOW and DB2 - DB15 exercised.

THEORY OF OPERATION OF THE AD7546

The traditional solution to achieving high resolution DACs with guaranteed monotonicity is the R-2R ladder approach. This technique usually constrains the converter to have ±1/2LSB nonlinearity in order to guarantee monotonicity, which in turn requires very tight resistor matching and tracking. The resistor ladder tolerance is most critical for the major carry where, in a 16-bit DAC, the 15LSBs turn off and the most significant bit turns on. If the MSB is more than 0.0015% low, the converter will be nonmonotonic. Table I shows the maximum tracking error which can be allowed over a 60°C range to maintain monotonicity, which is ±1LSB DNL. A standard R-2R approach therefore imposes severe constraints on resistor matching.

The design technique used in the AD7546 sidesteps the penalty inherent in the R-2R design (i.e. that tight differential nonlinearity figures require tight nonlinearity figures). The block diagram of the AD7546 is shown in Figure 2. The top four bits of the 16-bit input data are decoded to select, via the segment switches, one of the 16 voltage segments available along the resistor chain. This voltage segment, $\frac{V_{REF}^{+} - V_{REF}^{-}}{16}$,



NOTE: SWITCHES ARE SHOWN FOR SEGMENT 0
i.e., INPUT CODE OF 0XXXH.

Figure 2. AD7546 Functional Diagram

Converter Type	Initial Matching Required for: ±1LSB DNL	±1/2LSB DNL	Tracking Required for: ±1LSB DNL (1/2LSB INITIAL DNL)	±1/2LSB DNL (1/4LSB INITIAL DNL)
Straight R-2R	±0.0015%	±0.00076%	±0.127ppm/°C	±0.063ppm/°C
Segmented 4 Bits + 12 Bits	±0.024%	±0.012%	±2ppm/°C	±1ppm/°C

Table I. Resistor Matching Requirements for 16-Bit DAC

is used as a voltage reference to feed a 12-bit R-2R type D/A converter operating in the voltage switching mode (Reference 1). From Figure 2 the reference voltage is the voltage between V_X and V_Y and is always equal to one voltage segment. The output of the D/A converter may be expressed as follows:

$$V_{OUT} = V_Y + D(V_X - V_Y)$$

where D is the lower 12-bit digital code, V_X is the higher segment voltage and V_Y is the lower segment voltage. The 12-bit D/A converter reference inputs, V_X and V_Y, are connected to the two resistor chain nodes which define the segment of interest and the 12-bit D/A converter interpolates between these two points.

Thus the 65,536 output levels available from the 16-bit DAC are composed of 16 groups of 4,096 steps each. Since the major carry of the 12-bit DAC is repeated in each of the 16 segments it requires sixteen times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature. The resistors that determine monotonicity are in the 12-bit DAC. The truth table for the switch decoder is shown in Table II.

DB15	DB14	DB13	DB12	Segment Switches	Output Switches
1	1	1	1	S15, S16	S18, S20
1	1	1	0	S14, S15	S17, S19
1	1	0	1	S13, S14	S18, S20
1	1	0	0	S12, S13	S17, S19
1	0	1	1	S11, S12	S18, S20
1	0	1	0	S10, S11	S17, S19
1	0	0	1	S9, S10	S18, S20
1	0	0	0	S8, S9	S17, S19
0	1	1	1	S7, S8	S18, S20
0	1	1	0	S6, S7	S17, S19
0	1	0	1	S5, S6	S18, S20
0	1	0	0	S4, S5	S17, S19
0	0	1	1	S3, S4	S18, S20
0	0	1	0	S2, S3	S17, S19
0	0	0	1	S1, S2	S18, S20
0	0	0	0	S0, S1	S17, S19

Table II. Truth Table for Switch Decoder

Since the input impedance of the D/A converter is low and varies with code, two external amplifiers are used to buffer the selected reference segment from the D/A converter. The buffer amplifiers, A1, A2, could give rise to differential nonlinearity if connected directly to V_X and V_Y and stepped up the ladder.

For example consider A1 and A2 to have input offset voltages V_{OS1} and V_{OS2} respectively, then the first major carry from segment 0 to segment 1 occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_0 + V_{OS2}$

$$V_{OUT} = V_0 + V_{OS2} + (1 - 1/2^{12})[(V_1 + V_{OS1}) - (V_0 + V_{OS2})]$$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: $V_X = V_2 + V_{OS1}$, $V_Y = V_1 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS2}$$

The error term generated by this segment change is:

$$V_{OS2} - V_{OS1} + \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

It can be seen that V_{OS1} and V_{OS2} must match to within one LSB to guarantee monotonic behavior at this transition.

To overcome this problem the AD7546 circuit interchanges the amplifiers at each segment transition and, as a result, differential nonlinearity can be guaranteed for a very large range of V_{OS}. Switching inside the feedback loop of the op amp is used to remove the effect of switch R_{ON}. With this technique the first major carry from segment 0 to segment 1 now occurs as follows:

Segment 0: $V_X = V_1 + V_{OS1}$, $V_Y = V_0 + V_{OS2}$

$$V_{OUT} = V_1 + V_{OS1} - \frac{(V_1 - V_0)}{2^{12}} - \frac{(V_{OS1} - V_{OS2})}{2^{12}}$$

Segment 1: Interchange amplifiers

$$V_X = V_2 + V_{OS2}, V_Y = V_1 + V_{OS1}$$

$$V_{OUT} = V_1 + V_{OS1}$$

The error term at the transition from one segment to another is now $(V_{OS1} - V_{OS2})/4096$ which gives very good differential nonlinearity for reasonable offsets. At the next segment transition, $V_X = V_3 + V_{OS1}$, $V_Y = V_2 + V_{OS2}$ and so on through each segment. The amplifiers are interchanged via output switches S17 – S20, see Table II.

In the segmented DAC the precision of the resistor chain determines integral nonlinearity only. If the resistor chain is trimmed for perfect matching such that Vn + 1 = Vn = Vn – 1 = Vsegment, then the resulting nonlinearity due to amplifier offset voltage corresponds to a gain error in adjacent segments of $V_{OS1} - V_{OS2}$, see Figure 3. This term may be nulled to zero with offset adjustment of one op amp.

This adjustment is facilitated by tying $V_{REF}+$ and $V_{REF}-$ to ground, tying DB0 through DB11 and DB13 through DB15 to digital ground and toggling DB12. The AD7546 output (V_{OUT}, pin 25) will have a square wave at the toggling frequency with an amplitude of $V_{OS1} - V_{OS2}$. This can be adjusted to zero as mentioned.

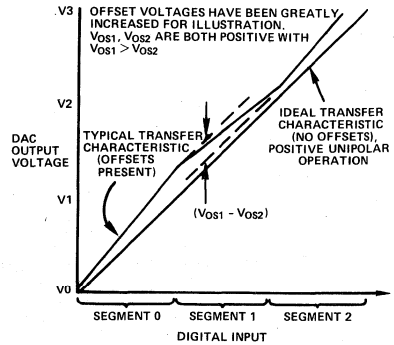


Figure 3. Positive Unipolar Transfer Characteristic (V_{REF}^- = 0V, V_{REF}^+ = +4V) Exaggerated to Show the Effect of Amplifier Offset Voltages

If offsets are equal in magnitude and sign, the result is a constant offset shift in the D/A transfer function and the device will have true 16-bit linearity.

(Reference 1. Analog Dialogue, Volume 14, Number 1 P16-17.)

OP-AMP SELECTION

Amplifiers A1 and A2 determine the overall performance of the AD7546. Since these are external to the converter, the user can choose amplifiers which will tailor the system performance to the required accuracy. Input bias current, open-loop gain and offset voltage of the amplifiers affect relative accuracy. Differential nonlinearity is affected by input bias current. (The offset voltage contribution to linearity has already been dealt with on previous pages.) The following two expressions deal with the relationship between device linearity and input bias current.

For Differential Nonlinearity:

$$\text{MAX DNL (in LSBs)} = \frac{14}{16} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

For Relative Accuracy:

$$\text{MAX NL (in LSBs)} = \frac{15}{2} \cdot \frac{(I_{BIAS})(R)}{1LSB}$$

Where I_{BIAS} = Input bias current for the noninverting input terminal of A1 or A2 in amps

$$1LSB = \frac{V_{REF}+ - V_{REF}-}{2^N} \text{ volts}$$

N is determined by the required system resolution up to N = 16.

R = R segment, typically 2kΩ

Low bias current op amps, BIFET or Super-Beta types, should be used such as the AD542K, AD544K, AD517K, TL071, TL081. Table III lists some important parameters against various op amps. Note that the AD7546 output settling time is dependent upon the op amps used. The figures in column two give the additional offset voltage contribution to nonlinearity of A1 and A2.

A1, A2	Maximum Additional Nonlinearity	Settling Time (μs) to ±1/2LSB 14 Bits	16 Bits
2 X AD544KH	±0.01%	15	35
1 X TL072BCP (Dual)	±0.05%	5	10
2 X AD517JH	±0.003%	90	100
1 X AD644JH (Dual AD544)	±0.01%	15	35
2 X LF256	±0.05%	5	10

Settling time measurements were made with a similar op amp to buffer V_{OUT} (A4 in Figure 8)

Table III. AD7546 Performance vs. A1, A2

DATA LOADING AND DEGLITCH SWITCH

The AD7546 timing specifications are included on Specifications page and illustrated here in Figure 4. Signals $\overline{CS}$ and $\overline{WR}$ have the same interpretation as in normal microprocessor systems. When both $\overline{CS}$ and $\overline{WR}$ are low the input latches are transparent and the DAC output voltage follows the input data. With $\overline{CS}$ low, the input data is latched on the rising edge of $\overline{WR}$.

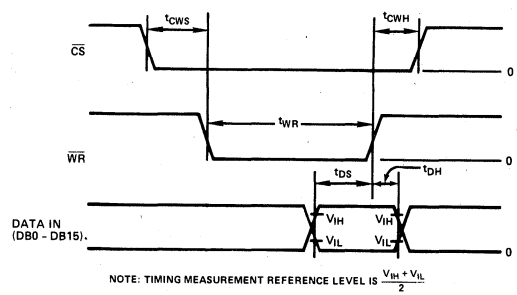


Figure 4. AD7546 Timing Waveforms

Included on the chip is an SPST switch intended for use in a Track/Hold circuit to remove glitches from the DAC output and simplify low-pass filtering of the reconstructed output voltage. The switch is synchronized with the latch loading signals, being open when both $\overline{CS}$ and $\overline{WR}$ inputs are low. The internal logic of the AD7546 ensures that the switch opens before data to the latches can change. To function as a Track/Hold the switch is placed in series with the DAC output as shown in Figure 5. Pin 23 is a no-connect pin which should be grounded to minimize any feedthrough resulting from stray capacitances at the two switch terminals. The switch should be used with pin 24 as the input and pin 22 as the output. When the switch is open the Hold capacitor stores the previous output voltage of the DAC. The $\overline{WR}$ pulse should be of sufficient duration to allow the DAC to settle to its new analog output and for all glitches to have settled out. Driving the $\overline{WR}$ input from a one-shot will ensure sufficient settling time.

When $\overline{WR}$ returns high the switch is closed, updating the output voltage on the capacitor. Typical output waveforms using the circuit of Figure 5 are shown below.

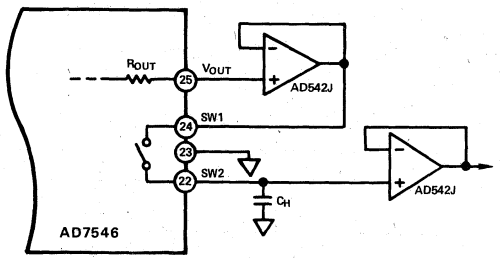
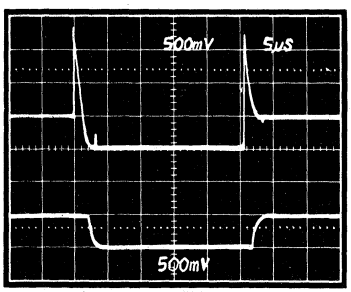


Figure 5. Track/Hold Circuit



UNIPOLAR OPERATION

Unipolar (single quadrant) operation is obtained when one end of the resistor chain is tied to ground i.e., when $V_{REF}+$ = $+V_{REF}$ and $V_{REF}-$ = 0V or when $V_{REF}+$ = 0V and $V_{REF}-$ = $-V_{REF}$. A typical unipolar circuit configuration for the AD7546 is shown in Figure 6a. In this positive unipolar application V_{SS} has been set to 0V and the AD7546 operates as a single supply device. If a full scale output is required which is different from the ideal V_{REF} – 1LSB then output amplifier A3 of Figure 6a can be configured to provide the necessary scaling. Figure 6b shows the additional components required to boost the full scale output voltage to +10V with V_{REF} = +4V. Any full scale gain error (introduced by R1, R2 tolerances) can be trimmed out by adjusting V_{REF}. Note that R1, R2 should be the same type of resistor (preferably metal film) so that their temperature coefficients match. The transfer characteristic for the circuit of Figure 6a is shown in Figure 7.

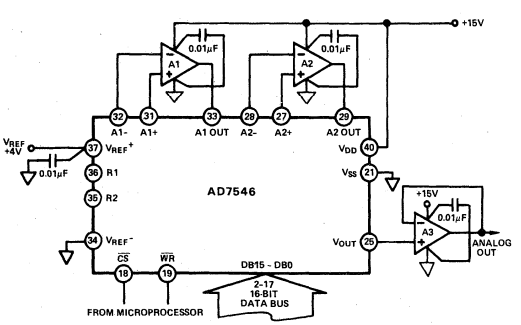


Figure 6a. Typical Unipolar Circuit Configuration for the AD7546 (Positive Reference, $V_{REF}+ = V_{REF}, V_{REF}- = 0V$)

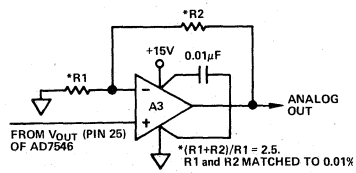


Figure 6b. Adding Gain Around A3 to Change Full Scale Output Voltage of Figure 6a.

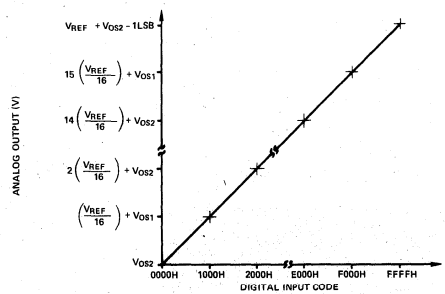


Figure 7. Unipolar Transfer Characteristic of Figure 6a.

BIPOLAR OPERATION

Bipolar (two quadrant) operation is obtained when both ends of the resistor chain are driven with voltage references of opposite polarity. A symmetrical transfer function around 0V is achieved with $|V_{REF}{}^{+}| = |V_{REF}{}^{-}|$. For this case the zero crossing occurs with DB15=1 and DB14 to DB0 all 0s. Figure 8 shows a typical bipolar circuit configuration for the AD7546 to obtain a symmetrical transfer function around 0V. Figure 9 shows the transfer characteristic of Figure 8.

Two equal trimmed resistors, R1 and R2, are included on the AD7546 to allow one reference to be generated from the other with the addition of an external amplifier (A3 in Figure 8). Note that $V_{REF}{}^{+}$ must always be more positive than $V_{REF}{}^{-}$; operation is confined to two quadrants (1st and 3rd). It is possible to use an ac reference signal with the AD7546 as long as $V_{REF}+$ always remains more positive than $V_{REF}-$.

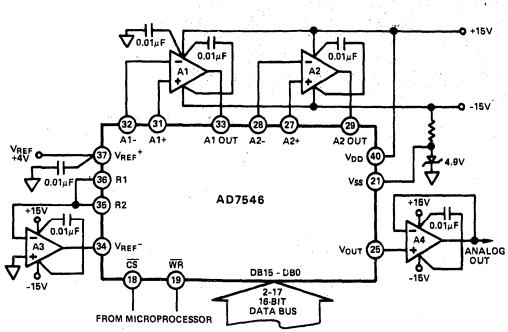


Figure 8. Typical Bipolar Circuit Configuration for the AD7546

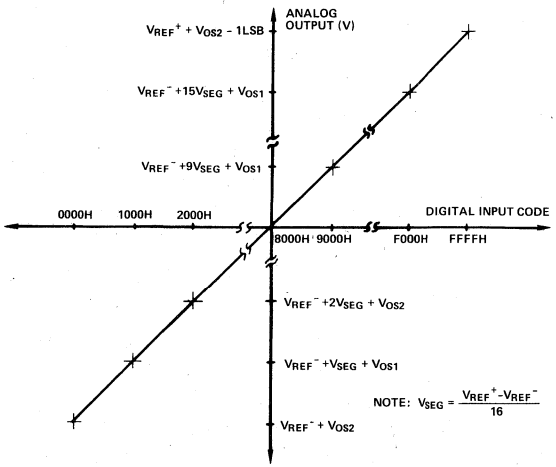


Figure 9. Bipolar Transfer Characteristic of Figure 8.

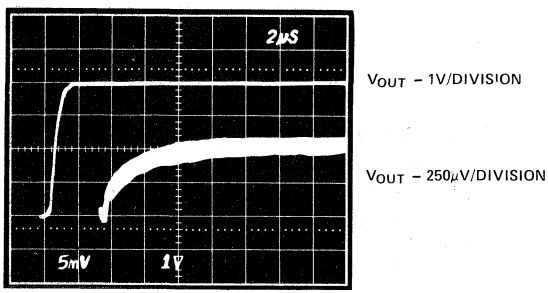


Figure 10. Typical Settling Characteristics of Figure 8 Using TL071 for Full Scale Code Change

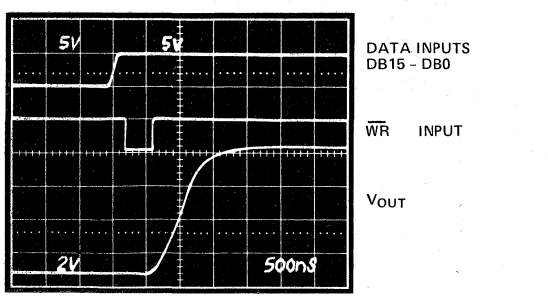


Figure 11. Typical Loading Waveforms with $\overline{CS}$ = 0V

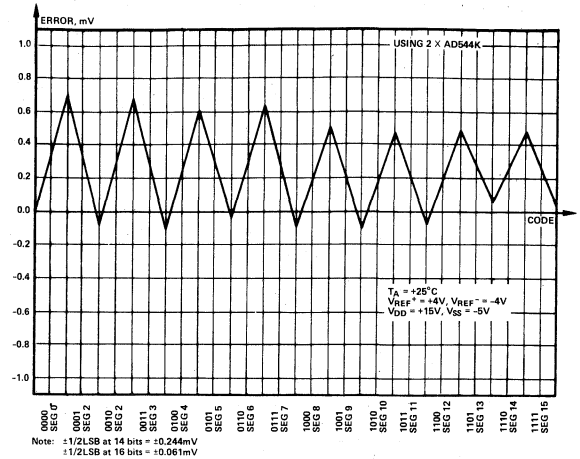


Figure 12a. Typical Error vs Input Code with A1 = A2 = AD544K

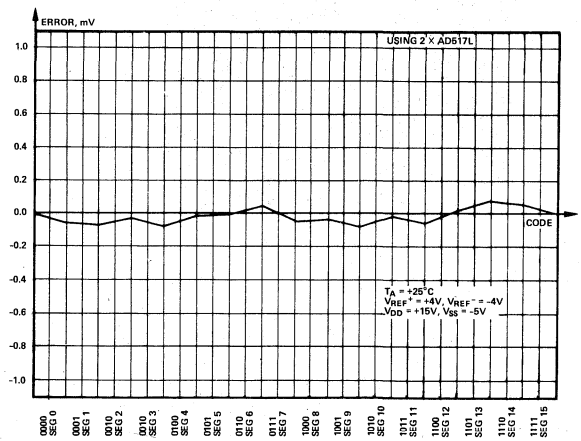


Figure 12b. Typical Error vs Input Code with A1 = A2 = AD517L

ANALOG DEVICES

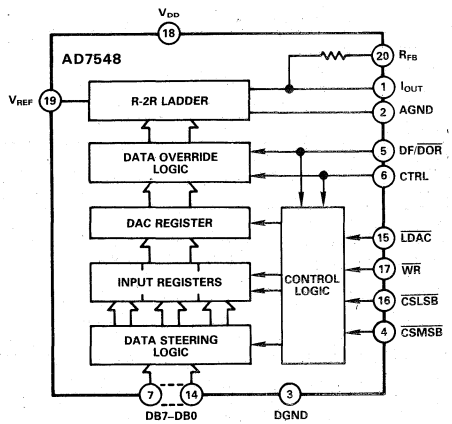
LC²MOS 8-Bit µP-Compatible 12-Bit DAC

AD7548

FEATURES
- 8-Bit Bus Compatible 12-Bit DAC
- All Grades 12-Bit Monotonic Over Full Temperature Ranges
- Operation Specified at +5V, +12V or +15V Power Supply
- Low Gain Drift of 5ppm/°C Maximum
- Full 4 Quadrant Multiplication
- Small 20-Pin Package

APPLICATIONS
- 8-Bit Microprocessor Based Control Systems
- Programmable Amplifiers
- Function Generation
- Servo Control

AD7548 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7548 is a 12-bit monolithic CMOS D/A converter for use with 8-bit bus microprocessors. Data is loaded in two bytes to input holding registers as shown in the block diagram opposite. The AD7548 can be configured to accept either left- or right-justified data, least significant byte or most significant byte first, using standard TTL compatible control inputs.

A separate load DAC control input allows the user the choice of updating the analog output coincident with loading new data to the DAC input register or at any time after the data loading event. This feature is especially important in multi-DAC systems where simultaneous update of all DACs is required.

The new Linear Compatible CMOS (LC² MOS) process used in the manufacture of the AD7548 allows precision thin-film linear circuitry and high-speed low-power CMOS logic to be integrated on the same small chip. The high-speed logic allows direct interfacing to most of the popular 8-bit microprocessors.

PRODUCT HIGHLIGHTS

1. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allow direct interfacing to most of the popular 8-bit microprocessors.
2. Guaranteed Monotonicity
   The AD7548 is guaranteed monotonic to 12-bits over the full temperature range for all grades and at all specified supply voltages.
3. Selectable Data Input Format
   Left- or right-justified data, least significant or most significant byte first. This allows the AD7548 to be interfaced with microprocessors using either Motorola or Intel-type data formatting.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3″ 20-pin package.
5. Single Supply Operation – See Figure 8.
6. Low Gain Error and Gain Error T.C.

9

SPECIFICATIONS[1] (V_{DD} = +5V, V_{REF} = +10V; $V_{PIN1} = V_{PIN2}$ = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	AD7548JN AD7548AQ	AD7548KN AD7548BQ	AD7548SD	AD7548TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V max	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V min	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	Specifications guaranteed over this range
I_{DD}	2	2	2	2	mA max	All digital inputs V_{IL} or V_{IH}
	300	300	300	300	μA max	All digital inputs 0V or V_{DD}

SPECIFICATIONS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V; $V_{PIN1} = V_{PIN2}$ = 0V. All specifications T_{min} to T_{max} unless otherwise specified)

Parameter	AD7548JN AD7548AQ	AD7548KN AD7548BQ	AD7548SD	AD7548TD	Units	Test Conditions/Comments
ACCURACY						
Resolution	12	12	12	12	Bits	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1/2	±1	±1/2	LSB max	All grades guaranteed monotonic to 12-bits over temperature.
Full Scale Error	±6	±3	±6	±3	LSB max	Measured using internal R_{FB} and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero.
Gain Temperature Coefficient[2]; ΔGain/ΔTemperature	±5	±5	±5	±5	ppm/°C max	Typical value is 2ppm/°C
Output Leakage Current I_{OUT} (Pin 1)						
+25°C	±5	±5	±5	±5	nA max	All digital inputs = 0V
T_{min} to T_{max}	±25	±25	±150	±150	nA max	
REFERENCE INPUT						
Input Resistance, Pin 19	7	7	7	7	kΩ min	Typical Input Resistance = 11kΩ
	20	20	20	20	kΩ max	
DIGITAL INPUTS						
V_{IH} (Input High Voltage)	2.4	2.4	2.4	2.4	V max	
V_{IL} (Input Low Voltage)	0.8	0.8	0.8	0.8	V min	
I_{IN} (Input Current)						
+25°C	±1	±1	±1	±1	μA max	V_{IN} = 0V or V_{DD}
T_{min} to T_{max}	±10	±10	±10	±10	μA max	
C_{IN} (Input Capacitance)[2]	7	7	7	7	pF max	
POWER SUPPLY						
V_{DD} Range	11.4/15.75	11.4/15.75	11.4/15.75	11.4/15.75	V min/V max	Specifications guaranteed over this range
I_{DD}	3	3	3	3	mA max	All digital inputs V_{IL} or V_{IH}
	1	1	1	1	mA max	All digital inputs 0V or V_{DD}

NOTES

[1]Temperature range as follows: JN, KN, Versions: 0 to +70°C
AQ, BQ, Versions: −40°C to +85°C
SD, TD, Versions: −55°C to +125°C

[2]Guaranteed by design but not production tested.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = +5V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = 0 to +70°C −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	240	240	290	ns min	Data Valid Setup Time
t_{DH}	50	50	70	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	250	280	320	ns min	Write Pulse Width

TIMING CHARACTERISTICS[1] (V_{DD} = +12V to +15V, V_{REF} = +10V, V_{PIN1} = V_{PIN2} = 0V unless otherwise stated)

Parameter	Limit at T_A = 25°C	Limit[2] at T_A = 0 to +70°C −40°C to +85°C	Limit[2] at T_A = −55°C to +125°C	Units	Test Conditions/Comments
t_{DS}	160	190	230	ns min	Data Valid Setup Time
t_{DH}	30	30	50	ns min	Data Valid Hold Time
t_{CWS}	30	40	50	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time
t_{CWH}	15	20	25	ns min	$\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time
t_{LWS}	30	40	50	ns min	$\overline{LDAC}$ to $\overline{WR}$ Setup Time
t_{LWH}	15	20	25	ns min	$\overline{LDAC}$ to $\overline{WR}$ Hold Time
t_{WR}	170	200	240	ns min	Write Pulse Width

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AC PERFORMANCE CHARACTERISTICS These characteristics are included for Design Guidance only and are not subject to test. (V_{REF} = +10V; V_{PIN1} = V_{PIN2} = 0V, Output Amplifier is AD544 except where stated)

		V_{DD} = +5V		V_{DD} = +12V to +15V			
Parameter	Version	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	T_A = +25°C	T_A = T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
Output Current Settling Time		1.5	–	1	–	µs typ	To 0.01% of full scale range. I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Digital to Analog Glitch Impulse		400	–	330	–	nV-sec typ	Measured with V_{REF} = 0V, I_{OUT} load = 100Ω, C_{EXT} = 13pF. DAC register alternately loaded with all 1s and all 0s
Multiplying Feedthrough Error[3]		3	5	3	5	mV p-p typ	V_{REF} = ±5V, 10kHz sine wave DAC register loaded with all 0s.
Total Harmonic Distortion		−85	–	−85	–	dB typ	V_{REF} = 6V rms @ 1kHz. DAC register loaded with all 1s.
Power Supply Rejection $\Delta GAIN/\Delta V_{DD}$		±0.015	±0.03	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
Output Capacitance I_{OUT} (Pin 1)		200	200	200	200	pF max	DAC register loaded with all 1s.
		100	100	100	100	pF max	DAC register loaded with all 0s.
Output Noise Voltage Density (10Hz–100kHz)		15	–	15	–	nV/√Hz typ	Measured between R_{FB} and I_{OUT}

NOTES

[1]Temperature range as follows: JN, KN, Versions: 0 to +70°C
AQ, BQ, Versions: −40°C to +85°C
SD, TD, Versions: −55°C to +125°C

[2]Guaranteed by design but not production tested.

[3]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (Suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} (pin 18) to DGND . . . . . +17V
V_{REF} (pin 19) to AGND . . . . . ±25V
V_{RFB} (pin 20) to AGND . . . . . ±25V
Digital Input Voltage (pins 4–17) to DGND . . −0.3V, V_{DD}
$V_{PIN\ 1}$ to DGND . . . . . −0.3V, V_{DD}
AGND to DGND . . . . . −0.3V, V_{DD}
Power Dissipation (Any Package)
To +75°C 450mW
Derates above +75°C . . . . . 6mW/°C

Operating Temperature Range
Commercial Plastic (JN, KN versions) . . . . . 0 to +70°C
Industrial Cerdip (AQ, BQ versions) . . . −40°C to +85°C
Extended Ceramic (SD, TD versions) . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING INFORMATION

Relative Accuracy T_{MIN} to T_{MAX}	Full Scale Error T_{MIN} to T_{MAX}	Temperature Range and Package		
		Plastic 0 to +70°C	Cerdip[1] −40°C to +85°C	Ceramic −55°C to +125°C
±1LSB	±6LSB	AD7548JN	AD7548AQ	AD7548SD
±1/2LSB	±3LSB	AD7548KN	AD7548BQ	AD7548TD

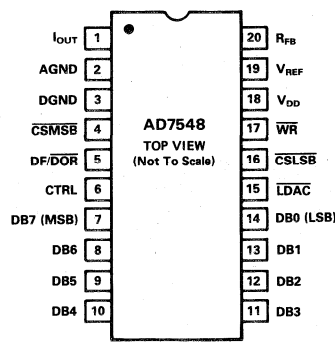
NOTE
1. Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

PACKAGE IDENTIFICATION [1]

Suffix "N": – Plastic Dip (N20B)
Suffix "Q": – Cerdip (Q20B)
Suffix "D": – Ceramic (D20B)

[1]See Section 19 for package outline information.

PIN CONFIGURATION

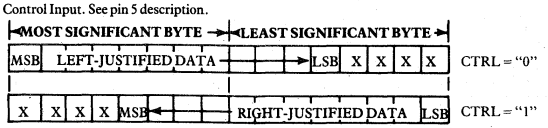


PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	I_{OUT}	DAC current OUT bus. Normally terminated at virtual ground of output amplifier.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	$\overline{CSMSB}$	Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
5	DF/$\overline{DOR}$	Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held HIGH.

DF/$\overline{DOR}$	CTRL	FUNCTION
0	0	DAC register contents overridden by all 0's
0	1	DAC register contents overriden by all 1's
1	0	Left-justified input data selected
1	1	Right-justified input data selected

6	CTRL	Control Input. See pin 5 description.



X = Don't care states.

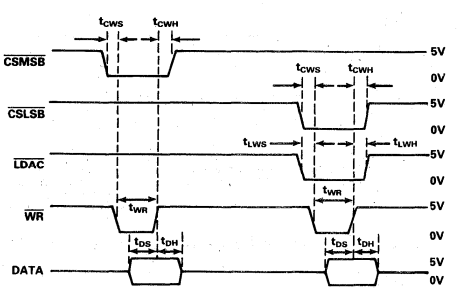
7	DB7	Data Bit 7. Most Significant Bit (MSB).
8	DB6	Data Bit 6.
9	DB5	Data Bit 5.
10	DB4	Data Bit 4.
11	DB3	Data Bit 3.
12	DB2	Data Bit 2.
13	DB1	Data Bit 1.
14	DB0	Data Bit 0. Least Significant Bit (LSB).
15	$\overline{LDAC}$	Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus.
16	$\overline{CSLSB}$	Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers.
17	$\overline{WR}$	WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register.

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	FUNCTION
0	1	0	1	Load LS Byte to Input Register.
0	1	0	0	Load LS Byte to Input Register and DAC Register.
0	0	1	1	Load MS Byte to Input Register.
0	0	1	0	Load MS Byte to Input Register and DAC Register.
0	1	1	0	Load Input Register to DAC Register.
1	X	X	X	No Data Transfer

18	V_{DD}	+5V to +15V Supply Input.
19	V_{REF}	Reference Voltage Input.
20	R_{FB}	Feedback Resistor. Used for normal D/A conversion.

CONTROL INPUT INFORMATION

Figure 1a shows the data load timing diagram for the AD7548. Figure 1b shows the simplified input control structure of the AD7548.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$.
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V.
   FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

Figure 1a. AD7548 Timing Diagram

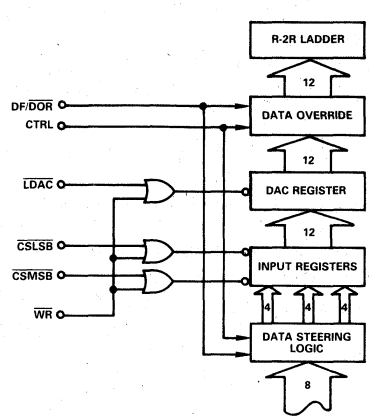


Figure 1b. Simplified AD7548 Input Control Structure

GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used, which steers binarily weighted currents between I_{OUT} and AGND, thus maintaining a constant current in each ladder leg independent of the switch state.

The input resistance at V_{REF} is constant and equal to the value "R" in Figure 2. Since the input resistance is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor).

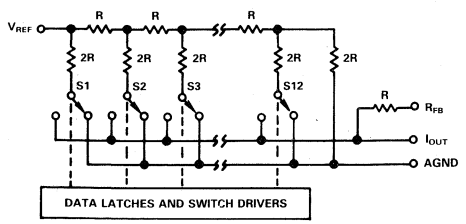


Figure 2. AD7548 Simplified Functional Diagram

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7548 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor R_O, denotes the equivalent output resistance of the DAC which varies with input code (excluding all 0's code) from 0.8R to 2R, where R is typically 11kΩ. C_{OUT} is the capacitance due to the current steering switches and varies from about 50pF to 120pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, V_{REF}, and the transfer function of R-2R ladder, N.

For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

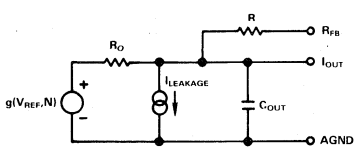


Figure 3. AD7548 Equivalent Analog Output Circuit

DATA LOADING

The AD7548 accepts incoming data in either left-justified format or right-justified format depending on the control inputs DF/$\overline{DOR}$ and CTRL.

(See pin description of DF/$\overline{DOR}$ and CTRL on preceding page).

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, the automatic transfer mode and the strobed transfer mode.

AUTOMATIC TRANSFER MODE

This is the simplest and fastest method of transferring data to the DAC register. It is facilitated by connecting $\overline{LDAC}$ to either $\overline{CSMSB}$, as shown in Figure 10, or $\overline{CSLSB}$.

Figure 4 shows the timing diagram for automatic transfer of 8 + 4-bit data to the DAC register. The first write cycle loads the first byte of data to the input register. The second write cycle loads the second byte of data to the input register and automatically transfers both bytes to the DAC register.

Updating a single byte (High or Low) in the DAC register can be achieved in one write cycle using the automatic transfer mode.

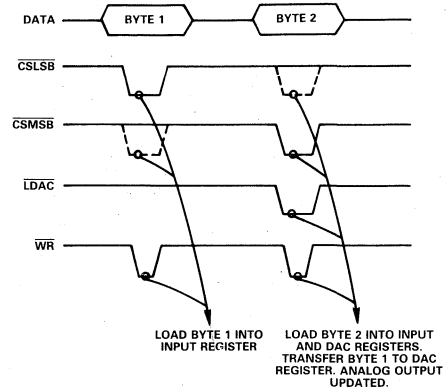


Figure 4. Automatic Transfer Mode

STROBED TRANSFER MODE

Figure 5 shows the timing diagram for the strobed transfer of 8 + 4-bit data to the DAC register. Three write cycles are required for this transfer mode. The first two write cycles sequentially load bytes 1 and 2 into the input register. The third write cycle transfers data from the input register to the DAC register.

The strobed transfer mode allows the DAC registers of several AD7548's to be updated simultaneously, as shown in Figure 13, by means of a master strobe signal connected to the $\overline{LDAC}$ of each device.

A single byte of data (High or Low) can be transferred to the DAC register in two write cycles using the strobed transfer mode.

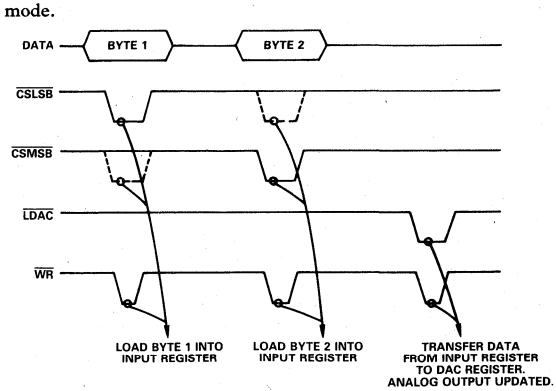


Figure 5. Strobed Transfer Mode

DATA OVERRIDE

The contents of the DAC register can be overridden by pulling DF/$\overline{DOR}$ (pin 5) LOW. The CTRL (pin 6) input then determines whether the DAC register data is overidden by all 0s (CTRL LOW) or all 1s (CTRL HIGH). This feature allows the user to calibrate the AD7548 in circuits such as Figure 6 without calling on the microprocessor to load calibration data.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary operation. With a dc input voltage or current (positive or negative polarity) applied at pin 19, the circuit is a unipolar D/A converter. With an ac input voltage the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

Table I shows the code relationship for the circuit of Figure 6.

For full scale trimming the DAC register is loaded with 1111 1111 1111. This is most easily accomplished by using the data override function. R1 is then adjusted for $V_{OUT} = -V_{IN}$ (4095/4096). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps.

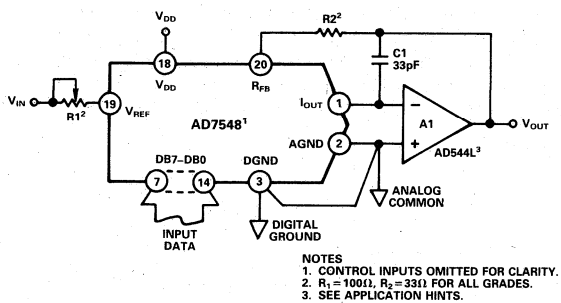


Figure 6. Unipolar Binary Operation

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$
0000 0000 0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

Table I. Unipolar Binary Code Table for Circuit of Figure 6

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The circuit uses offset binary input coding. However, 2's complement coding can be accommodated if the MSB is inverted (done in software) before data is loaded into the DAC.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively one can omit R1 and R2 and adjust the ratio of R3 and R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of V_{IN} or by varying the value of R5.

R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably metal film) so that their temperature coefficients match. Mismatch of R3 to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

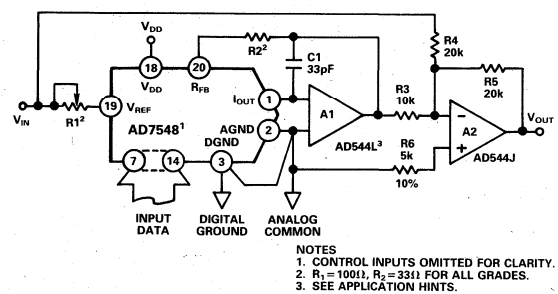


Figure 7. Bipolar Operation (Offset Binary Coding)

Binary Number in DAC Register MSB LSB	Analog Output, V_{OUT}
1111 1111 1111	$+V_{IN}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{IN}\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-V_{IN}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{IN}\left(\frac{2048}{2048}\right)$

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 7

SINGLE SUPPLY OPERATION

Figure 8 shows the AD7548 connected in a voltage switching mode. The input voltage is connected to I_{OUT}. The D/A converter output voltage is taken from the V_{REF} pin and has a constant impedance equal to R. R_{FB} is not used in this circuit. The input voltage V_{IN} must always be positive with respect to AGND in order to prevent an internal diode from turning on. To maintain linearity the input voltage should remain within 2.5V of AGND with V_{DD} from +12V to +15V.

The output voltage V_{OUT} of Figure 8 is expressed as

$$V_{OUT} = (V_{IN})\ (D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

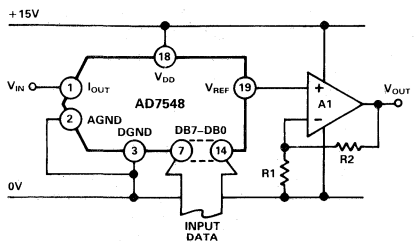


Figure 8. Single Supply Operation Using Voltage Switching Mode

APPLICATION HINTS

Output Offset: CMOS D/A converters in circuits such as Figures 6 and 7 exhibit a code dependent output resistance which in turn cause a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which, depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7548. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7548 AGND and DGND pins (1N914 or equivalent).

Temperature Coefficients: The gain temperature coefficient of the AD7548 has a maximum value of 5ppm/°C and typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

High Frequency Considerations: AD7548 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

Feedthrough: The dynamic performance of the AD7548 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 6 is shown in Figure 9 which minimizes feedthrough from V_{REF} to the output in multiplying applications.

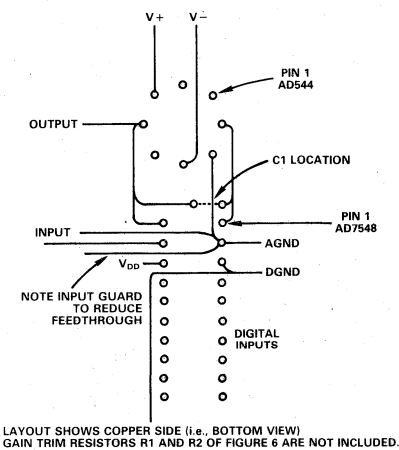


Figure 9. Suggested Layout for AD7548 and Op Amp

For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

MICROPROCESSOR INTERFACING

AD7548 – MC6800 INTERFACE

A typical 6800 configuration using the automatic transfer mode of the AD7548 is shown in Figure 10. Table III gives a sample loading routine written in re-entrant form. Data load and store instructions use extended addressing. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The data is considered right-justified with the four most significant bits occupying the lower half of XXYY + 1. The AD7548 is assigned a base address of PPQQ. This address selects the low byte register of the AD7548. Address PPQQ + 1 selects both the high byte register and the $\overline{\text{LDAC}}$ control input.

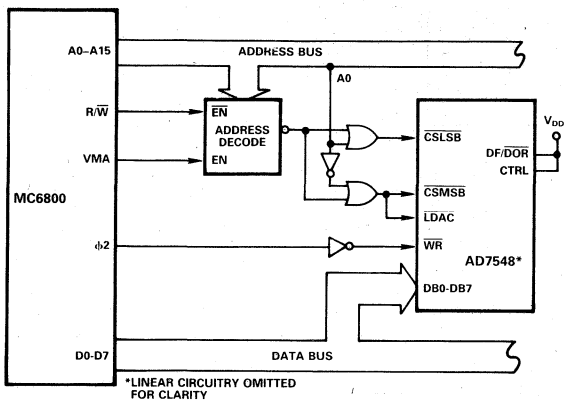


Figure 10. AD7548 – MC6800 Interface (Automatic Transfer Mode)

	JSR	WWZZ	Jump to AD7548 subroutine
WWZZ	PSH A		Push A onto stack
	TPA		
	PSH A		Push CCR onto stack
	LDA A	$XXYY	
	STA A	$PPQQ	Load low byte to AD7548
	LDA A	$XXYY + 1	
	STA A	$PPQQ + 1	Load high byte to AD7548 and update analog output
	PUL A		
	TAP		Pull CCR from stack
	PUL A		Pull A from stack
	RTS		Return to main program

Table III. Sample Routine for AD7548 – MC6800 Interface

AD7548 – 8085A INTERFACE

Figure 11 shows a typical AD7548 to 8085A microprocessor interface configured for automatic transfer of 8 + 4-bit right-justified data. Table IV gives a sample loading routine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The four most significant data bits occupy the lower half of XXYY + 1. As before, addresses PPQQ and PPQQ + 1 select the $\overline{\text{CSLSB}}$ and $\overline{\text{CSMSB}}/\overline{\text{LDAC}}$ control inputs respectively. Since only two instructions (LHLD, SHLD) are required to both fetch and load the 12-bit data word to the AD7548, it may be more efficient to insert these instructions as required in the main program rather than use a subroutine such as illustrated here.

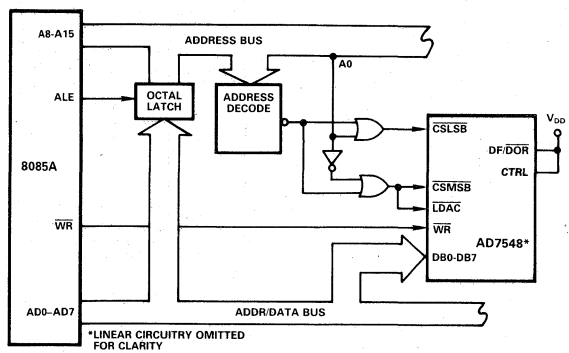


Figure 11. AD7548 – 8085A Interface (Automatic Transfer Mode)

	CALL	7548	
7548	PUSH	PSW	Push register contents onto stack
	PUSH	H	
	LHLD	XXYY	Fetch 12-bit data
	SHLD	PPQQ	Load 12-bit data
	POP	H	Pop register contents from stack
	POP	PSW	
	RET		Return to main program

Table IV. Sample Routine for AD7548–8085A Interface

AD7548 – MC6809 INTERFACE

The AD7548 can be interfaced to the MC6809 microprocessor as shown in Figure 12 for automatic transfer of 8 + 4-bit data. Similar to the 8085A instructions LHLD and SHLD, the 6809 has two instructions to fetch and store 12-bit (16-bit) data to the AD7548, LDD and STD. However, in the 6809, the high byte of data is moved first, then the low byte (this is the opposite of the 8085A). This means that if the 12-bit data is assumed to reside at addresses XXYY and XXYY + 1 then XXYY must contain the high byte. It also means that the address decoding logic of Figure 11 must be slightly changed so that the even-order AD7548 address, PPQQ from before, selects the $\overline{\text{CSMSB}}$ input to load the high byte first. In this automatic transfer configuration $\overline{\text{LDAC}}$ is tied to the $\overline{\text{CSLSB}}$ input. The AD7548 analog output can thus be updated using only two instructions as follows:

```
LDD     $XXYY
STD     $PPQQ
```

The strobed transfer configuration is shown in Figure 13 with a dedicated decoder output assigned to each chip select input. The common $\overline{\text{LDAC}}$ signal allows simultaneous update of both AD7548 DAC registers.

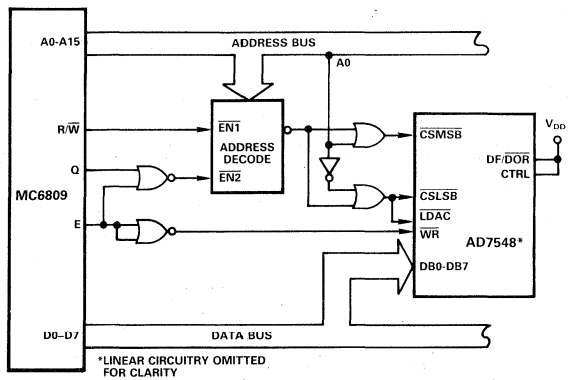


Figure 12. AD7548 – MC6809 Interface (Automatic Transfer Mode)

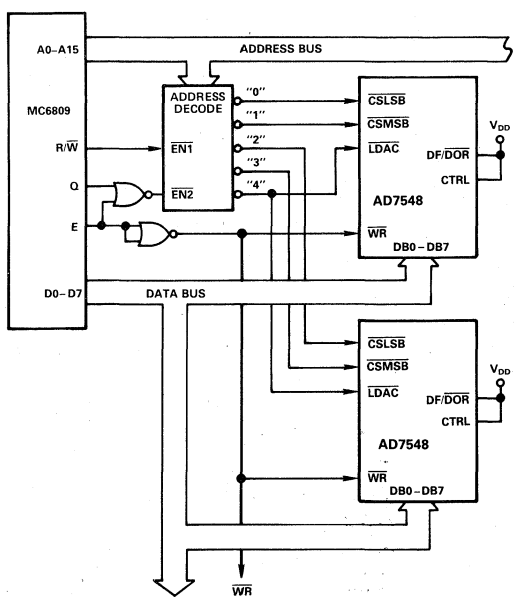


Figure 13. AD7548 – MC6809 Interface (Strobed Transfer Mode)

AD7548 – 6502 INTERFACE

Figure 14 shows a typical AD7548 to 6502 microprocessor interface configured for automatic transfer of right-justified data. As a programming example, Figure 15 shows a flow chart for producing a 12-bit (4095-step-max) voltage ramp under 6502 control. Index registers X and Y of the 6502 form a 12-bit counter with the X-register holding the low byte of data and the Y-register the high byte. Table V shows the program listing. The X-register is compared with FF_H and the Y-register with 10_H to determine when the ramp voltage has reached its maximum value (FFF_H). By changing the comparison data in the program the maximum ramp output voltage can be varied from levels corresponding to FFF_H down to 000_H. In the program listing of Table V the AD7548 has been assigned contiguous addresses 0400 (low byte) and 0401 (high byte and DAC register).

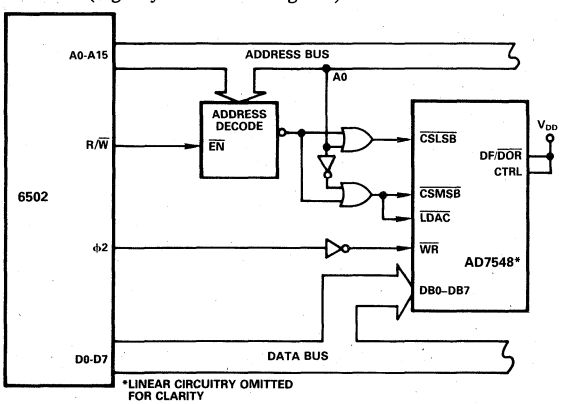


Figure 14. AD7548 – 6502 Interface (Automatic Transfer Mode)

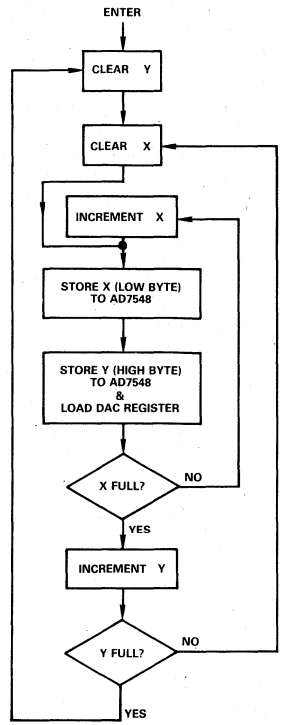


Figure 15. Flow Chart for Voltage Ramp Generation

ADDRESS	OP-CODE	MNEMONIC	OPERAND
0000	A0	LDY	# 00
01	00		
02	A2	LDX	# 00
03	00		
04	4C	JMP	0008
05	08		
06	00		
07	E8	INX	
08	8E	STX	0400
09	00		
0A	04		
0B	8C	STY	0401
0C	01		
0D	04		
0E	E0	CPX	# FF
0F	FF		
10	D0	BNE	0007
11	F5		
12	C8	INY	
13	C0	CPY	# 10
14	10		
15	D0	BNE	0002
16	EB		
17	FO	BEQ	0000
0018	E7		

Table V. Program Listing for Figure 15

AD7548 – Z80 INTERFACE

Figure 16 shows a typical AD7548 to Z80 microprocessor interface configured for automatic transfer of right-justified data. Similar to the 8085A and 6809 cases, 16-bit load instructions are available in the Z80 which can fetch and load 12-bit data to the AD7548. Since the low byte of data is moved first and assuming the 12-bit data resides at addresses XXYY and XXYY + 1, address XXYY must contain the low byte. As before, addresses PPQQ and PPQQ + 1 select the AD7548 $\overline{\text{CSLSB}}$ and $\overline{\text{CSMSB}}/\overline{\text{LDAC}}$ control inputs respectively. Choosing the Z80 register pair BC to hold the 12-bit data, the two instructions required to update the AD7548 analog output are as follows:

```
LD BC, (XXYY)
LD (PPQQ), BC
```

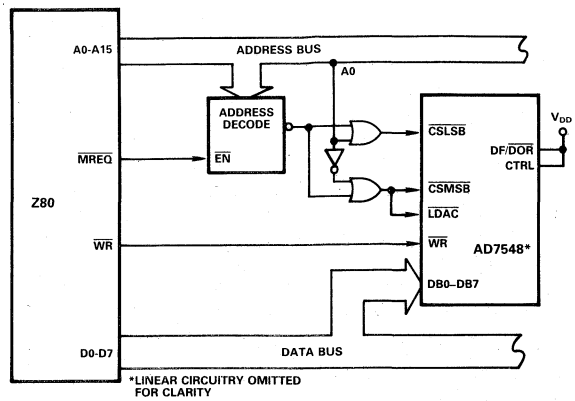


Figure 16. AD7548 – Z80 Interface (Automatic Transfer Mode)

ANALOG DEVICES

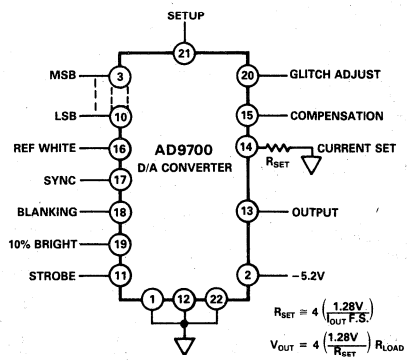
Monolithic Video D/A Converter

AD9700

FEATURES
Update Rates to 125MHz
2ns Rise Time
On-Chip Reference Voltage
Single −5.2V Power Supply
Complete Composite Inputs

APPLICATIONS
Raster Scan Displays
Color Graphics
Automated Test Equipment
TV Video Reconstruction

AD9700 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The AD9700 digital-to-analog converter is a monolithic device capable of accepting eight bits of ECL-compatible data at update rates as high as 125MHz. On-chip latches on the data lines help minimize "glitches" in the output signal. Incorporating the AD9700 into system designs is eased by its blanking, sync, 10% brightness, and reference white control signals. An on-board reference also eliminates external circuits and makes it easier to design the AD9700 into high-speed applications.

The unit is housed in a 22-pin package, operates from a single −5.2V power supply, and dissipates only 625mW, making this the smallest, lowest power D/A converter available to design engineers who need true "graphics ready" converters for raster scan, color graphics, and other high-speed systems.

This device is a natural extension of the Analog Devices advanced technology that produced the first hybrid converters which included composite capabilities. Like the earlier HDG-Series D/A converters, the AD9700 is designed to have general output compatibility with EIA Standards RS-170 and RS-343.

Its size and electrical performance make the AD9700 extremely attractive for use in a broad range of high-speed data applications. But in addition to the other characteristics which recommend its use, pricing also makes the AD9700 a viable economic candidate for large-scale production requirements.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	12	GROUND
2	−5.2V	13	OUTPUT
3	BIT 1 (MSB)	14	CURRENT SET
4	BIT 2	15	COMPENSATION
5	BIT 3	16	REFERENCE WHITE
6	BIT 4	17	COMPOSITE SYNC
7	BIT 5	18	COMPOSITE BLANKING
8	BIT 6	19	10% BRIGHT
9	BIT 7	20	GLITCH ADJUST
10	BIT 8 (LSB)	21	SETUP
11	STROBE	22	GROUND

NOTE: PINS 1, 12, AND 22 NEED TO BE CONNECTED TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9700BD
RESOLUTION	Bits	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (adjustable)	mV	2.5
Current (adjustable)	μA	67
ACCURACY (GS = Gray Scale; FS = Full Scale)		
Differential Linearity	% GS	±0.2
Integral Linearity	% GS	±0.2
Zero Offset (Initial) Voltage	mV	0.3
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	30
Gain	ppm/°C	50
Zero Offset	ppm/°C	12
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]		
Settling Time to 0.4% GS; 0V to 637.5mV GS change		
Voltage	ns	10
Update Rate[2]	MHz (min)	125 (100)
Slew Rate	V/μs	300
Rise Time	ns	2
Glitch Energy[3]	pV-s	50
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Coding		Complementary Binary (CBN)
Logic Levels		
"1"	V	−0.9
"0"	V	−1.7
Loading (each bit)		5pF and 50kΩ to −5.2V
STROBE INPUT		
Logic Compatibility		ECL
Logic Levels		
"1"	V	−0.9
"0"	V	−1.7
Loading		5pF and 50kΩ to −5.2V
Set-up Time (Data	ns, min	2.5
Hold Time (Data)	ns, min	1.5
Propagation Delay	ns	4
REFERENCE WHITE, COMPOSITE SYNC, BLANKING, AND 10% BRIGHT INPUTS[4]		
Logic Compatibility		ECL
Logic Levels		
"1"	V	−0.9
"0"	V	−1.7
Loading		5pF and 50Ω to −5.2V
SPEED PERFORMANCE – CONTROL INPUTS		
Settling Time to 10% of Final Value for:		
Reference White	ns	10
Composite Sync	ns	10
Composite Blanking	ns	10
10% Bright	ns	10
SETUP CONTROL		
Ground	mV (IRE Units)	0 (0)
Open	mV (IRE Units)	53.25 (7.5)
1k to −5.2V	mV (IRE Units)	71 (10)
−5.2V	mV (IRE Units)	142 (20)
ANALOG OUTPUT		
FS Current	mA	0 to −17
FS Voltage[5]	V (±1%)	0 to −0.6375
Compliance	V	−1.1 to +0.1
Internal Impedance	Ω (max)	800 (±40)
OUTPUT – COMPOSITE SYNC[4]		
Current	mA (±5%)	0 or −7.6
Voltage	mV (±5%)	0 or −286
OUTPUT – COMPOSITE BLANKING[4]		
Current[6]	mA (±1%)	−17.0, −18.4, or −20.8
Voltage[6]	mV (±1%)	−637.5, −690.8, or −780
OUTPUT – 10% BRIGHT[4]		
Current	mA (±5%)	0 or −1.9
Voltage	mV (±5%)	0 or −71
POWER REQUIREMENTS		
−5.2V ±0.25V	mA	120
Power Supply Rejection Ratio	%/%	0.024/4.8
Power Dissipation	mW	625
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
MTBF[7]		
Mean Time Between Failures	Hours	1.95×10^5
PACKAGE OPTION[8]		D22A

NOTES
[1]Settling to percentage of Gray Scale includes FS and MSB transitions. Inherent 3ns register delay (50% points) has been disregarded.
[2]Update rate shown limited by full-scale settling time for eight bits. Unit can be updated to 125MHz with some settling time degradation.
[3]Glitch can be reduced to less than 25pV-s with glitch adjustment.
[4]Reference White, Composite Sync, and Composite Blanking are enabled with logic "0"; 10% Bright is enabled with logic "1". Composite Sync or Composite Blanking control signals reset input registers.
[5]LSB value of 2.5mV used for calibration. $I_{OUT} = (1.28/R_{SET}) \times 4$ when $R_{SET} \cong 300\Omega$.
[6]Outputs shown correspond to externally selected IRE units of 0, 7.5, and 20.
[7]Calculated using MIL HNBK-217; Ground; Fixed; +25°C Ambient Temperature.
[8]See Section 19 for package outline information.

Specifications subject to change without notice.

ANALOG DEVICES

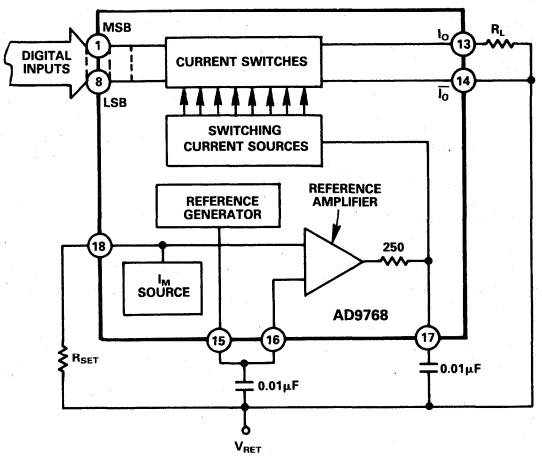
Ultra High-Speed IC D/A Converter

AD9768

FEATURES
5ns Settling Time
100MHz Update Rate
20mA Output Current
ECL-Compatible
40MHz Multiplying Mode

APPLICATIONS
Raster Scan & Vector Graphic Displays
High-Speed Waveform Generation
Digital VCOs
Ultra-Fast Digital Attenuators

AD9768 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices AD9768SD D/A converter is a monolithic current-output converter which can accept 8 bits of ECL-level digital input voltages and convert them into analog signals at update rates as high as 100MHz. In addition to its use as a standard D/A converter, it can also be utilized as a two-quadrant multiplying D/A at multiplying bandwidths as high as 40MHz.

An inherently low glitch design is used, and the complementary current outputs are suitable for driving transmission lines directly. Nominal full-scale output is 20mA, which corresponds to a 1-volt drop across a 50Ω load, or ±1 volt across 100Ω returned to +1 volt. The actual output current is determined by the on-chip reference voltage ($V_{REF} \approx -1.26V$) and an external current setting resistor, R_{SET}.

Full-scale output current I_{OUT} with digital "1" at all inputs is calculated with the equation:

$$I_{OUT} = 4 \times \frac{V_{RET} - V_{REF}}{R_{SET}}$$

The setting resistor R_{SET} and the output load resistor should both have low temperature coefficients. A complementary $\overline{I_{OUT}}$ is also provided.

The reference voltage source is a modified bandgap type and is nominally −1.26 volts. This reference supply requires no external regulation. To reduce the possibility of noise generation and/or instability, pin 15 (REFERENCE OUT) can be decoupled using a high-quality ceramic chip capacitor. Stabilization of the internal loop amplifier is by a single capacitor connected from pin 17 (COMPENSATION) to ground. The minimum value for this capacitor is 3900pF, although a 0.01μF ceramic chip capacitor is recommended.

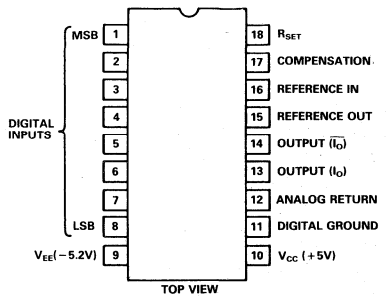
The incredible speed characteristics of the AD9768SD D/A converter make it attractive for a wide range of high-speed applications. The ability of the unit to operate as a two-quadrant multiplying D/A converter adds another dimension to its usefulness and makes the AD9768SD a truly versatile device.

9

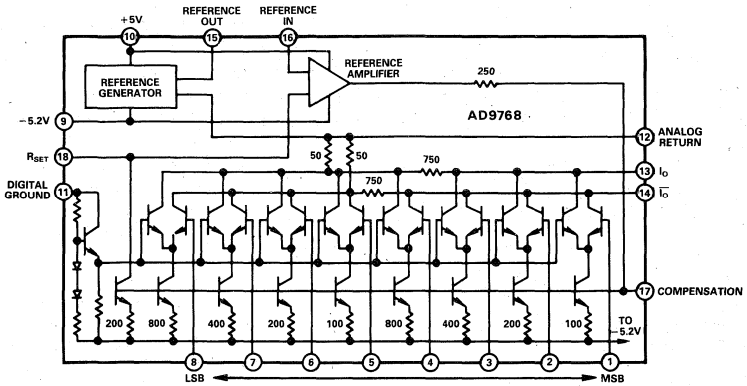
SPECIFICATIONS (typical @ +25°C under following conditions unless otherwise noted; nominal digital input levels; nominal power supplies; $R_L = 50\,\Omega$; $R_{SET} = 220\,\Omega$; $V_{RET} = 0V$)

	Units	AD9768SD
RESOLUTION (FS = FULL SCALE)	Bits	8
LSB WEIGHT (CURRENT)	μA	78
ACCURACY[1]		
Differential Nonlinearity	±% FS	0.2
Integral Nonlinearity	±% FS	0.2
Monotonicity		Guaranteed
Zero Offset (Initial)	μA	60
TEMPERATURE COEFFICIENTS		
Zero Offset	ppm/°C	1.5
Reference Voltage (−1.26V)	ppm/°C	70
DIGITAL DATA INPUTS		
Logic Compatibility		ECL
Logic Voltage Levels "1" =	V	−0.9
"0" =	V	−1.7
Coding	Binary (BIN) = Unipolar Out Offset Binary (OBN) = Bipolar Out	
OUTPUT		
Current (Unipolar) FS	mA (max)	2 to 20 (30)
I_{OUT} (@ Pin 13)		
All Digital "1" Input	mA	20
All Digital "0" Input	mA	0
$\overline{I_{OUT}}$ (@ Pin 14)		
All Digital "1" Input	mA	0
All Digital "0" Input	mA	20
Compliance	V	−0.7 to +3.0
Impedance	Ω (±5%)	830
SPEED PERFORMANCE		
Settling Time (to 0.2% FS)[2]	ns	5
Slew Rate	V/μs	400
Update Rate	MHz	100
Rise Time	ns	1.8
Glitch Energy	pV-sec	200
REFERENCE		
Internal, Monolithic[3]	V	−1.26
External, Variable[4]		
Voltage-Multiplying Mode	V (max)	0 to −1.1 (−2)
Current-Multiplying Mode	mA (max)	0 to −5 (−7.5)
VOLTAGE-MULTIPLYING MODE[4] (See Figure 2)		
V_M Range (at Pin 16)	V	±0.5
V_M Center	V	−0.6
Resistance (at Pin 16)	kΩ	800
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: −0.1 V_M Input = 0mA I_{OUT} −1.1 V_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: −0.1 V_M Input = 1mA I_{OUT} −1.1 V_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	kHz	250
CURRENT-MULTIPLYING MODE (See Figure 4)		
I_M Range (at Pins 17 & 18)	mA	0 to 5
Resistance (at Pin 18)	Ω	160
Transfer Function –	Measured at Pin 13; Digital "0" Applied to Bits 1-8: 1mA I_M Input = 0mA I_{OUT} 5mA I_M Input = 0mA I_{OUT} Measured at Pin 13; Digital "1" Applied to Bits 1-8: 1mA I_M Input = 4mA I_{OUT} 5mA I_M Input = 20mA I_{OUT}	
Large Signal Bandwidth (−3dB Point)	MHz	40
POWER REQUIREMENTS		
−5.2V ±0.25	mA (max)	66 (70)
+5.0V ±0.25	mA (max)	14 (15)
Power Dissipation	mW (max)	410 (430)
Power Supply Sensitivity[5]	%/%	0.07
TEMPERATURE RANGES[6]		
Operating	°C	−30 to +115
Storage	°C	−55 to +150
THERMAL RESISTANCE[7]		
Junction to Air, θja (free Air)	°C/W	90
Junction to Case, θja	°C/W	20
PACKAGE OPTION[8]		D18A

AD9768SD PIN CONNECTIONS (TOP VIEW)



NOTES
[1]Relative to FS, including linearity (within voltage compliance limits).
[2]Worst case settling time; includes FS and Most Significant Bit (MSB) transitions.
[3]Applies when operating AD9768 as standard D/A.
[4]Based on R_L = 50 ohms; R_{SET} = 220 ohms; V_{RET} = 0V.
[5]1% change in either power supply voltage causes 0.07% change in analog output.
[6] Case temperature.
[7]Maximum junction temperature 125°C.
[8]See Section 19 for package outline information.
Specifications subject to change without notice.



AD9768SD D/A Schematic

THEORY OF OPERATION

Refer to the AD9768SD schematic.

The transistors pictured on the bottom of the diagram, connected to paired transistors in the middle of the schematic, are current sources which are always "on". The paired transistors are differential current switches, designed to steer current from the current sources to either pin 13 (I_O) or pin 14 ($\overline{I_O}$).

Digital inputs applied to pins 1-8 determine which transistors will be operating in each pair and establish what current will flow at pins 13 and 14.

The transistor on the extreme left of the schematic is a base reference for the paired current switches and is used to assure the switches will be centered around an ECL voltage swing. The diodes connected to the base of this transistor are temperature compensation devices for the base reference circuit.

There are three different current sources in the AD9768 D/A. The eight transistors shown on the bottom of the schematic are structured as two identical groups of four current sources, each of which is binarily weighted. The MSB group, comprised of the four on the right, is connected to the LSB group through a 15:1 current divider made up of two 50Ω and two 750Ω resistor networks. The geometry of the AD9768 guarantees the binary weighing ratios among the 100, 200, 400 and 800 resistors in each emitter circuit are correct.

The resistor values which are shown indicate the ratios among the resistors, and not their nominal values.

The third current source is a single transistor, pictured in the lower left portion of the schematic with its collector connected to pin 18 R_{SET}. Its function is to help establish the base voltage on the eight current sources; it works in conjunction with the external R_{SET} resistor selected by the user of the AD9768, and the reference amplifier. Current flowing through this transistor is referred to as I_M in the figures and test.

When the AD9768 is operating as a conventional current-output D/A converter, I_M develops a voltage across R_{SET} which is one of the inputs to the on-board reference amplifier shown in the schematic. The other input to this amplifier is the on-chip reference voltage of -1.26 volts.

The output of the reference amplifier adjusts the current-source base reference voltage at pin 17; this, in turn, adjusts the value of I_M in the single-transistor current source and causes it to develop a voltage across R_{SET} which maintains pin 18 at the -1.26 volts of the on-chip reference supply.

To maintain good stability in the internal loop reference amplifier, a ceramic chip capacitor with a nominal value of 0.01μF should be connected to pin 17 COMPENSATION; minimum recommended value for this capacitor is 3900pF.

The temperature coefficient of the load resistor (R_L) can affect the performance of the AD9768 D/A converter, as it can with any current-output converter. The design and use of the AD9768 and its dependence on an external R_{SET} resistor, however, make it sensitive also to the tempco of R_{SET}. The user is cautioned to select R_L and R_{SET} resistors which have low temperature coefficients.

DIGITAL GROUND (pin 11) and ANALOG RETURN (pin 12) are normally connected together; this connection should be made as close as possible to the device case to minimize possible noise problems. The AD9768 D/A is similar to any other high-speed, high performance device: optimum use requires careful attention to all design details, including the layout of the circuit in which the converter is used.

CONVENTIONAL AD9768

Refer to Figure 1, Conventional AD9768SD.

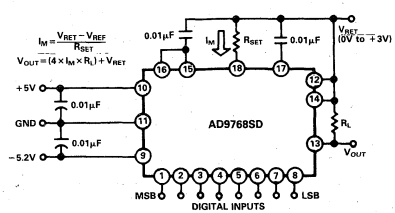


Figure 1. Conventional AD9768SD

The output current of the AD9768 appears at pin 13 (I_O) and develops a voltage across the load resistor R_L which is based on:

A. I_M (the current flowing through the single-transistor source discussed above)
B. Value of R_L

I_M is a function of the return voltage (V_{RET}), the reference voltage (V_{REF}), and the value of R_{SET}; all of these are selected by the user for his application. The necessary equations for calculating precise values for each are part of Figure 1. As indicated,

the voltage drop across R_L is added to the return voltage; the resulting voltage is the total V_{OUT} of the converter.

VOLTAGE MULTIPLYING MODE

In addition to its use as an ultra-high speed current output D/A converter, the AD9768 can also be used as a two-quadrant multiplying D/A in either a voltage mode or a current mode.

Refer to Figure 2, Multiplying AD9768 (Voltage Mode).

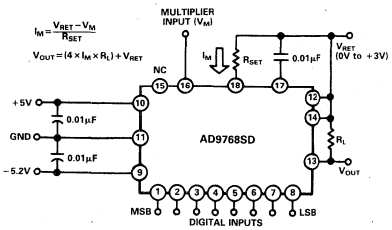


Figure 2. Multiplying AD9768 (Voltage Mode)

When operating in this mode, the analog output of the AD9768 is influenced by the digital inputs and an external multiplying voltage (V_M) applied to pin 16 REFERENCE IN, which takes the place of the internal reference used when the D/A is operating in a conventional manner.

The value of I_M flowing through R_{SET} is set by the voltage of V_{RET} minus the multiplying voltage (V_M), divided by R_{SET}; the amount of this current is part of the equation which establishes the analog output (V_{OUT}) of the AD9768 and is chosen by the user for his application. As it is when operating the D/A in a conventional fashion, V_{RET} can be any value between 0 volts and +3 volts. V_M (for purposes of discussion here) is some negative voltage and can be varied over a range which is approximately 1 volt peak-to-peak.

If the load resistor (R_L) has a value of 50 ohms, if R_{SET} has a value of 220 ohms, and if V_{RET} is 0V, the center of the V_M voltage will be −0.6V; and it can vary from −0.1V to −1.1V. Typically, the frequency of these variations has an upper limit of 250kHz when operating in the voltage multiplying mode; that frequency is the 3dB point of the bandwidth of the internal reference amplifier.

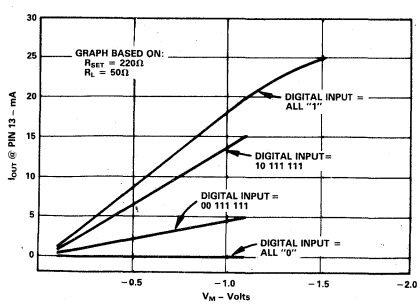


Figure 3. I_{OUT} vs. Multiplying Voltage

The combined effects of variations in V_M and changes in digital input values are shown in Figure 3, I_{OUT} vs. Multiplying Voltage. In this illustration, the ordinate of the graph is expressed in terms of milliamps of I_{OUT} current at pin 13. V_{OUT}, of course, will be a function of the value of R_L chosen by the user.

The negative value of V_M on the horizontal axis is shown starting at approximately −0.1V, rather than 0V, because the AD9768 must have some small value of voltage applied to perform a multiplying function. For the conditions shown in the figure, output current starts to become nonlinear at approximately 20mA because of the maximum 30mA output drive capabilities of the device. Different values for R_{SET} and R_L would alter the point where limiting first appears.

CURRENT MULTIPLYING MODE

The AD9768 D/A converter can be operated at markedly higher multiplying rates when operated in a current-multiplying mode, as contrasted with the voltage-multiplying mode. Refer to Figure 4, Multiplying AD9768SD (Current Mode).

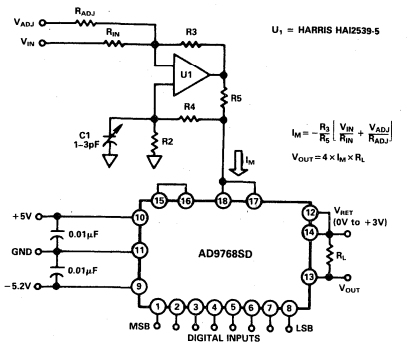


Figure 4. Multiplying AD9768SD (Current Mode)

In this mode, the internal reference amplifier and its inherent frequency limitations are replaced by a current source comprised of U1 and associated circuits. These circuits supply a unipolar current I_M which is one-fourth the full-scale output current (with digital "1" applied to all inputs) and set current flow through the load resistor.

V_{IN} is some voltage chosen by the user for his particular application; the value of this voltage is based in part on the size of the load resistor and the 0mA to 5mA range of I_M. V_{IN} can have frequency components as high as 40MHz. V_{ADJ} and R_{ADJ} provide an offset adjustment to compensate for the dc component of V_{IN} to assure I_M is always a unipolar current between 0mA and 5mA. The values of the required voltages and resistors can be calculated using the equations which are part of Figure 4.

Refer to Figure 5, I_{OUT} vs. Multiplying Current.

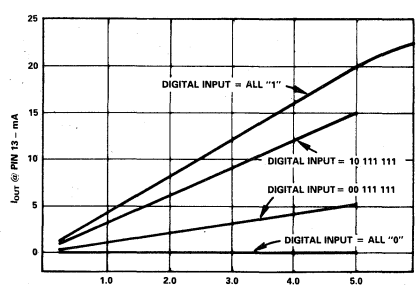


Figure 5. I_{OUT} vs. Multiplying Current

As shown, I_M can vary over the range of 0mA to 5mA; a value of approximately 0.3mA may be the practical lower limit because of nonlinearities at extremely small current levels. These changes in I_M are combined with variations in digital inputs, producing complex changes in the output current (at pin 13) and in V_{OUT}. The "rounding" of the current curve in the graph is the result of I_{OUT} approaching the 30mA maximum drive capabilities of the AD9768 and needs to be taken into account to assure optimum performance in the selected application.

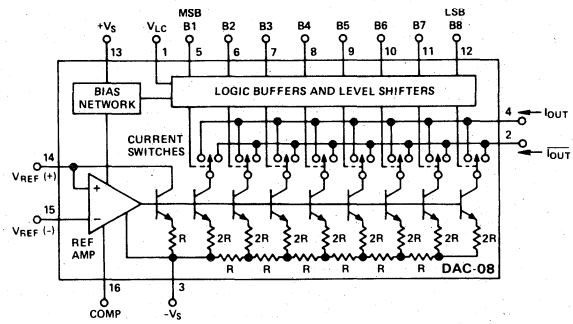
8-Bit Monolithic High Speed Multiplying D/A Converter

AD DAC-08

FEATURES

Exact Replacement for Industry Standard DAC-08
Fast (85ns typical) Settling Time
Linearity Error ±1/4LSB (±0.1%) Guaranteed Over Full Temperature Range
Wide Output Voltage Compliance: -10V to +18V
Single Chip Monolithic Construction

AD DAC-08 FUNCTIONAL BLOCK DIAGRAM



TO-116

9

PRODUCT DESCRIPTION

The AD DAC-08 is a low-cost, 8-bit monolithic multiplying digital-to-analog converter featuring typical settling times of 85ns. The chip contains 8 matched bipolar current steering switches, a precision resistor network, and high-speed control amplifier, thus integrating all important circuit functions on a single chip.

The AD DAC-08 provides matching of full-scale output current to the reference current within 1LSB. Analog Devices' precision linear processing makes this matching possible without the use of laser trimming. Diffused resistors are used rather than thin-film resistors in order to provide specified performance at low cost.

The AD DAC-08 is recommended for use in applications requiring 8-bit accuracy and fast settling times coupled with ease of use. The AD DAC-08 also provides an alternate source for designs already using the standard DAC-08.

The AD DAC-08 is available in 5 performance grades: the AD DAC-08A and AD DAC-08 are rated for the -55°C to +125°C extended temperature range; and the AD DAC-08H, E, and C grades are specified for the 0 to +70°C commercial temperature range. All models are guaranteed monotonic over their full temperature range, and all are packaged in a hermetically-sealed 16-pin ceramic dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD DAC-08 is a true second-source equivalent to the industry standard DAC-08.
2. The versatile current-in, current-out design, choice of fixed or variable reference, and CMOS or TTL compatible inputs offer the user greater flexibility in applying the device.
3. The fast settling time allows the AD DAC-08 to be used in applications such as CRT displays, waveform generators, and high-speed analog-to-digital converters.
4. The high impedance current output can drive a resistor directly, or be used with an external op amp to produce a low impedance output voltage.
5. The AD DAC-08 is available in chip form for use in hybrid microcircuits. Consult the chip section for available grades and application details.

SPECIFICATIONS

The AD DAC-08 and AD DAC-08A specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = -55°C$ to $+125°C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08 MIN	AD DAC-08 TYP	AD DAC-08 MAX	AD DAC-08A MIN	AD DAC-08A TYP	AD DAC-08A MAX	UNITS
RESOLUTION					8			8	Bits
MONOTONICITY		$T_A = -55°C$ to $+125°C$		GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = -55°C$ to $+125°C$			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	135		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$ typ	-10		+18	-10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, R_{15} = 5.000kΩ; $T_A = 25°C$	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	($I_{FS4} - I_{FS2}$)		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	V- = -5.0V	0	2.0	2.1	0	2.0	2.1	mA
		V- = -7.0 to -18V	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$							
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		-2.0	-10		-2.0	-10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	V- = -15V	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{IHR}	$V_S = \pm 15V$	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0	+0.1	-1.0	-3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V- = 4.5V to -18V		±0.002	±0.01		±0.002	±0.01	%/%
		$I_{REF} = 1.0mA$							
POWER SUPPLY CURRENT									
From $+V_S$	I+		0.4	2.3	3.8	0.4	2.3	3.8	mA
From $-V_S$	I-		-0.8	-6.4	-7.8	-0.8	-6.4	-7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48	mW
		+5V, -15V, $I_{REF} = 2.0mA$		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08D			AD DAC-08AD		

NOTES
[1] See Section 19 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- AD DAC-08, DAC-08A. . . . . -55°C to +125°C
- AD DAC-08E, C, H . . . . . 0 to +70°C

Storage Temperature . . . . . -65°C to +150°C
- Power Dissipation 500mW
  - Above 100°C Derate by . . . . . 10mW/°C

Lead Soldering Temperature . . . . . 300°C (60sec)
$-V_S$ Supply to $+V_S$ Supply 36V
Logic Inputs. . . . . $-V_S$ to ($-V_S$ +36V)
- V_{LC} . . . . . $-V_S$ to $+V_S$

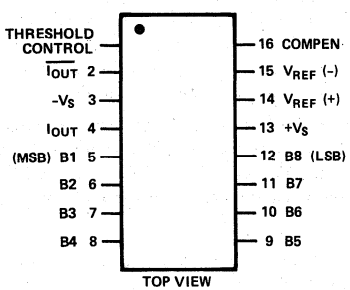
Reference Inputs (V_{14}, V_{15}). . . . . $-V_S$ to $+V_S$
Reference Input Differential
- Voltage (V_{14} to V_{15}). . . . . ±18V

Reference Input Current (I_{14}) 5.0mA

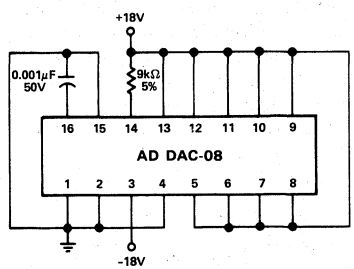
SPECIFICATIONS

The AD DAC-08C, E, and H specifications apply for $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 0$ to $+70°C$ unless otherwise noted.

MODEL / CHARACTERISTIC	SYMBOL	CONDITIONS	AD DAC-08C MIN	AD DAC-08C TYP	AD DAC-08C MAX	AD DAC-08E MIN	AD DAC-08E TYP	AD DAC-08E MAX	AD DAC-08H MIN	AD DAC-08H TYP	AD DAC-08H MAX	UNITS
RESOLUTION					8			8			8	Bits
MONOTONICITY		$T_A = 0$ to $+70°C$		GUARANTEED			GUARANTEED			GUARANTEED		
NONLINEARITY		$T_A = 0$ to $+70°C$			±0.39			±0.19			±0.1	% FS
SETTLING TIME	t_s	Full Scale Step to ±1/2LSB		85	150		85	150		85	135	ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35	60		35	60		35	60	ns
FULL SCALE TEMPCO	TC I_{FS}			±10	±80		±10	±50		±10	±50	ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$; $R_{OUT} > 20M\Omega$	−10		+18	−10		+18	−10		+18	V dc
FULL SCALE CURRENT	I_{FS4}	$V_{REF} = 10.000V$; R_{14}, R_{15} = 5.000kΩ; $T_A = 25°C$	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
FULL SCALE SYMMETRY	I_{FSS}	$(I_{FS4} - I_{FS2})$		±2.0	±16		±1.0	±8.0		±0.5	±4.0	μA
ZERO SCALE CURRENT	I_{ZS}			0.2	4.0		0.2	2.0		0.1	1.0	μA
OUTPUT CURRENT RANGE	I_{FSR}	V− = −5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	mA
		V− = −7.0 to −18V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	mA
LOGIC INPUT LEVELS												
Logic "0"	V_{IL}	$V_{LC} = 0V$			0.8			0.8			0.8	V
Logic "1"	V_{IH}	$V_{LC} = 0V$	2.0			2.0			2.0			V
LOGIC INPUT CURRENTS		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		−2.0	−10		−2.0	−10		−2.0	−10	μA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002	10		0.002	10	μA
LOGIC INPUT SWING	V_{IS}	V− = −15V	−10		+18	−10		+18	−10		+18	V
LOGIC THRESHOLD RANGE	V_{THL}	$V_S = \pm 15V$	−10		+13.5	−10		+13.5	−10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	+0.1	−1.0	−3.0	μA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		+0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
	$PSSI_{FS-}$	V− = −4.5V to −18V, $I_{REF} = 1.0mA$		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	%/%
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8	0.4	2.3	3.8	0.4	2.3	3.8	mA
	I−	From $-V_S$	−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	−0.8	−6.4	−7.8	mA
POWER DISSIPATION	P_D	±5V, $I_{REF} = 1.0mA$		33	48		33	48		33	48	mW
		+5V, −15V, $I_{REF} = 2.0mA$		108	136		108	136		108	136	mW
		±15V, $I_{REF} = 2.0mA$		135	174		135	174		135	174	mW
PACKAGE STYLE[1] "D" (Q16A)				AD DAC-08CD			AD DAC-08ED			AD DAC-08HD		



Pin Connections



Burn-In Circuit

APPLYING THE AD DAC-08

Reference Connections

Figure 1 shows the block diagram of the AD DAC-08 circuit. A reference current (equal to the desired full-scale output current) is applied to pin 14. The reference amplifier adjusts the base voltage of the NPN current source transistors. The collector currents are binarily weighted, and their sum is equal to 255/256 times the reference current. The binary weighting is accomplished by the diffused resistor R-2R ladder network. The individual collector currents are steered into either the I_{OUT} or $\overline{I_{OUT}}$ lines by the current switches. These switches are driven by level shifters which can accept TTL or CMOS logic levels directly. The I_{OUT} and $\overline{I_{OUT}}$ lines can drive an op amp summing junction or can drive resistive loads directly due to the wide range of output compliance voltage.

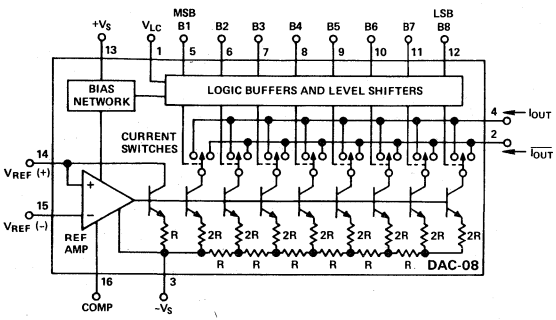


Figure 1. AD DAC-08 Block Diagram

Figure 2 illustrates the connections for positive and negative references. When a positive reference is used (Figure 2a), resistor R14 (equal to V_{REF} divided by the desired I_{FS}) establishes the reference current into pin 14. Reference amplifier bias current errors are minimized by connecting R15 (equal to R14) from pin 15 to ground. Adjustment of the output scale can be done by trimming R14, although in most applications the tight initial matching between reference current and output current will be adequate.

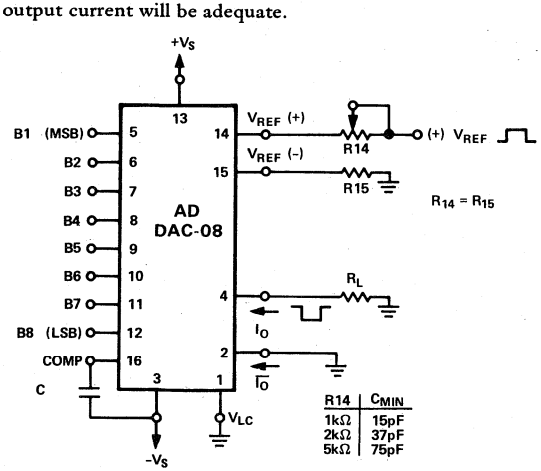


Figure 2a. Connections for Use with Positive Reference

Figure 2b shows the connections for a negative reference. Note that the reference current flows from ground into pin 14 through R14, which should be a low TC resistor as in the positive reference configuration. Resistor R15 serves the purpose

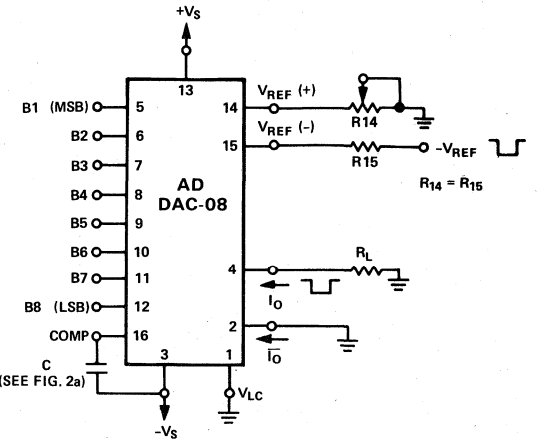


Figure 2b. Connections for Use with Negative Reference

of bias current cancellation only and need not be a precision resistor. Note that the input impedance for a negative reference is very high, while a positive reference sees an impedance equal to R14.

When a dc reference is used, a 0.01μF reference bypass capacitor is recommended. The reference should be a low-drift, well-regulated and filtered type, such as the AD581 10V reference IC. Other values of reference voltage may be used, provided that R14 is chosen for a reference current between 0.2mA and 4.0mA.

MULTIPLYING MODE PERFORMANCE

The AD DAC-08 can be used to perform two-quadrant digital-analog multiplication by applying an ac reference signal. When an ac reference is used, pin 15 must be offset to insure that pin 14 is always at a higher potential than pin 15.

The reference amplifier must be properly compensated in ac applications to insure stability. The value of the capacitor from pin 16 to $-V_S$ depends on the value of R14. Minimum values of compensation capacitor for R14 values of 1, 2 and 5kΩ are 15, 37 and 75pF respectively.

For fastest response to a pulsed reference, low values of R14 should be used, allowing smaller values of compensation capacitor. It is possible to lower the equivalent resistance at pin 14 by connecting a shunt resistor to ground. Figure 3 shows the performance with equivalent resistance of 200Ω and no compensation capacitor. Slew rate is approximately 15mA/μs under these conditions.

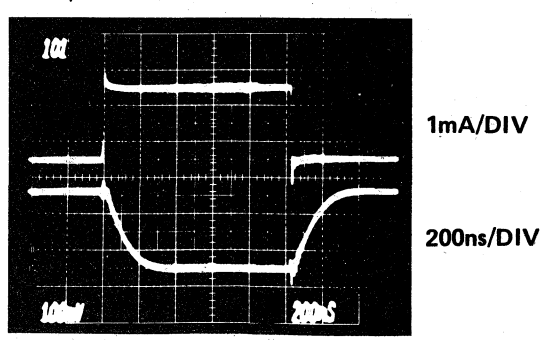


Figure 3. Fast Pulsed Reference Operation

The photographs on this page demonstrate the dynamic performance of the AD DAC-08. The AD DAC-08 is capable of extremely fast settling time, typically 85 nanoseconds for a full-scale step with I_{REF} = 2.0mA. As with any high speed circuitry, component layout must be optimized for minimum parasitic capacitances if full speed is to be realized.

Figure 4 below shows the output settling characteristic for a full-scale step. The vertical scale is 1LSB per division. Note that the zero-to-full scale settling time (Figure 4a) to within 1/2LSB is approximately 70 nanoseconds.

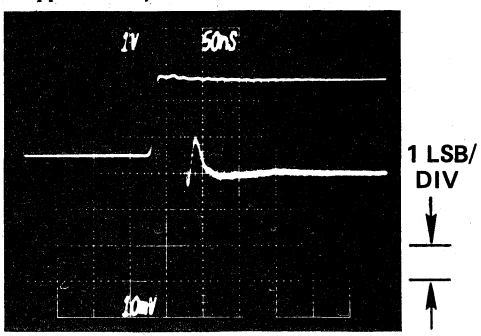


Figure 4a. Zero to Full-Scale Settling

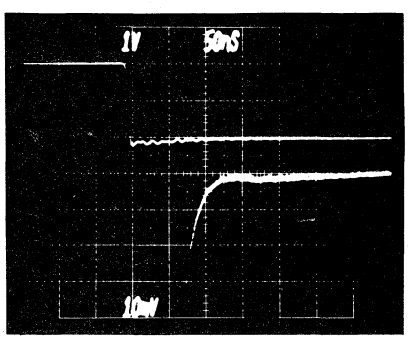


Figure 4b. Full-Scale to Zero Settling

Since the settling time of a DAC circuit includes propagation delay, slewing time, and final settling, switching time is best measured when only the LSB is switched. This minimizes the slewing time necessary. The LSB switching characteristic is shown in Figure 5.

SETTLING TIME MEASUREMENT

It should be noted that settling time measurement is not a simple matter. Since 1/2LSB of a 2.0mA full scale is only 4μA, a 1kΩ load resistance is needed to provide adequate drive for most oscilloscopes. However, any stray capacitance can cause the settling time of the fixture to be longer than the DAC settling time. For example, 15pF stray capacitance can cause a settling time to 1/2LSB of nearly 100 nanoseconds in the test fixture alone. The circuit of Figure 6 reduces the capacitance at the measurement node to less than 5pF, allowing more accurate determination of settling time.

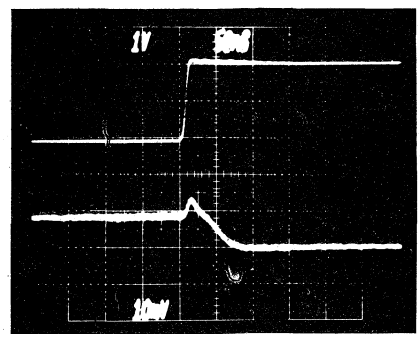


Figure 5. LSB Switching

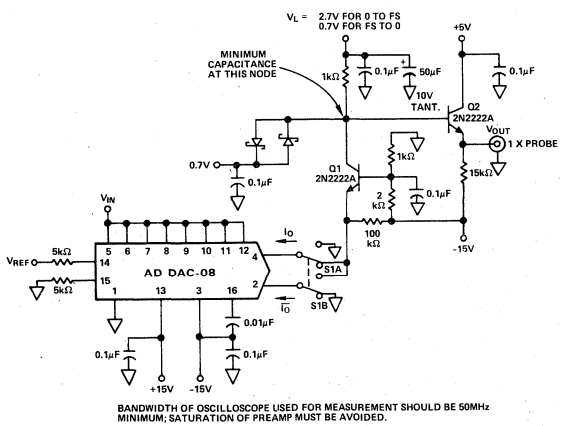


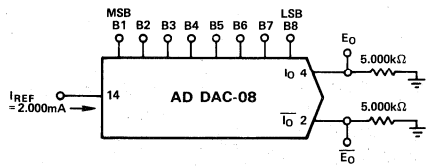
Figure 6. Settling Time Test Circuit

LOGIC INPUT CIRCUIT

The AD DAC-08 digital inputs will accommodate all popular logic families. The switching threshold is adjustable by applying a voltage to the logic threshold control pin (pin 1). The threshold is nominally 1.4 volts above V_{LC} at room temperature. For TTL/DTL interface, pin 1 is simply grounded. The logic inputs will tolerate wide voltage swings; for example, for $-V_S$ = −15V, the inputs may swing between −10V and +18V.

OUTPUT CONNECTIONS

The I_O and $\overline{I_O}$ outputs provide the user with several possible output configurations. Current is steered into the I_O terminal when a bit is at Logic "1", and into $\overline{I_O}$ when the bit is at Logic "0". Either output may be used, or both may be used simultaneously. If only one output is used, the unused output must still be connected to ground or some other point capable of sourcing I_{FS}.



	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	-9.960	0.000
FULL SCALE -LSB	1	1	1	1	1	1	1	0	1.984	0.008	-9.920	-0.040
HALF SCALE + LSB	1	0	0	0	0	0	0	1	1.008	0.984	-5.040	-4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	-5.000	-4.960
HALF SCALE -LSB	0	1	1	1	1	1	1	1	0.992	1.000	-4.960	-5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	-0.040	-9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	0.000	-9.960

Figure 7. High Impedance Voltage Output

The wide output compliance range permits the AD DAC-08 to drive a resistive load directly. For example, with I_{REF} = 2.0mA, and a 5kΩ resistor from pin 4 to ground, the voltage at pin 4 varies from 0V with all bits OFF to -9.960V with all bits ON. While this is the simplest current-to-voltage conversion, it presents a 5kΩ output impedance, which adversely affects settling time and requires buffering.

An operational amplifier configured as a current-to-voltage converter will lower the output impedance and provide a voltage inversion. An output range of zero to +9.960V is then produced with a 5kΩ feedback resistor as shown in Figure 8.

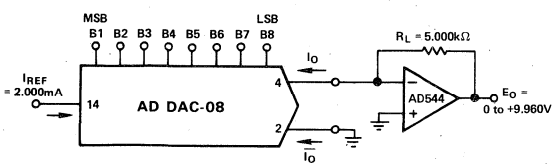
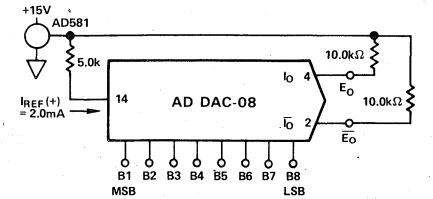


Figure 8. Low Impedance Voltage Output

Bipolar output voltage ranges are also possible. Figure 9 demonstrates the simplest scheme, providing a -9.92 to +10.00 volt scale in 80 millivolt steps. The voltage output has a high impedance as shown and should be buffered with an amplifier connected as a voltage follower.



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
POS FULL SCALE	1	1	1	1	1	1	1	1	- 9.920	+10.000
POS FULL SCALE -LSB	1	1	1	1	1	1	1	0	- 9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	- 0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.080
ZERO SCALE -LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	- 9.920

Figure 9. Bipolar Voltage Output

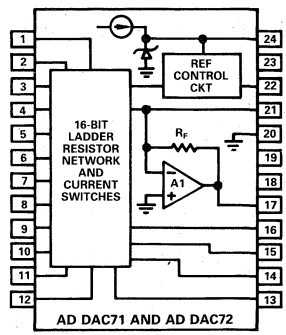
ANALOG DEVICES

High Resolution 16-Bit D/A Converter

AD DAC71/AD DAC72*

FEATURES
16-Bit Resolution
±0.003% Maximum Nonlinearity
Low Gain Drift ±7ppm/°C
0 to +70°C Operation (AD DAC71, AD DAC71H, AD DAC72C)
−25°C to +85°C Operation (AD DAC72)
Current and Voltage Models Available
Improved Second-Source
Low Cost

AD DAC71 AND AD DAC72 FUNCTIONAL DIAGRAM



9

PRODUCT DESCRIPTION

The AD DAC71 and AD DAC72 are high resolution 16-bit hybrid IC digital-to-analog converters including reference, scaling resistors and output amplifier (V models).

The devices offer outstanding accuracy, including maximum linearity error of 0.003% at room temperature and maximum gain drifts of 15ppm/°C (AD DAC71, AD DAC71H, AD DAC72C) and 7ppm/°C (AD DAC72). This performance is possible due to the innovative design, using proprietary monolithic D/A converter chips. Laser-trimmed thin film resistors provide the linearity and wide temperature range for guaranteed monotonicity.

The AD DAC71 and AD DAC72 digital inputs are TTL-compatible. Coding is complementary straight binary (CSB) for unipolar output versions and complementary offset binary (COB) for bipolar output versions.

All versions are packaged in a 24-pin ceramic DIP. The AD DAC71, AD DAC71H and AD DAC72C are specified for operation from 0 to +70°C, and the AD DAC72 is specified from −25°C to +85°C. The AD DAC71H, AD DAC72 and AD DAC72C are supplied in hermetically-sealed packages.

The AD DAC71 and AD DAC72 are intended to serve as improved second sources to DAC71 and DAC72 devices from other manufacturers.

***Covered by Patent Numbers: 3,978,473; RE28,633; 4,020,486; 3,747,088; 3,803,590; 3,961,326; 4,213,806; 4,136,349.**

PRODUCT HIGHLIGHTS

1. The AD DAC71 and AD DAC72 provide 16-bit resolution with 0.003% linearity error.
2. The proprietary chips used in the hybrid design provide excellent stability over temperature and improved reliability.
3. Unipolar and bipolar current and voltage output versions are available to fill a wide range of system requirements.
4. The AD DAC71 and AD DAC72 are improved second source replacements for DAC71 and DAC72 devices from other manufacturers.

SPECIFICATIONS (@ T_A = +25°C, rated power supplies unless otherwise noted)

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
DIGITAL INPUTS										
Resolution		16			16			16		Bits
Logic Levels (TTL-Compatible)[1]										
Logical "1"	+2.4		+5.5	+2.4		+5.5	+2.4		+5.5	V dc
Logical "0"	+0		+0.4	+0		+0.4	+0		+0.4	V dc
ACCURACY[2]										
Linearity Error at 25°C			±0.003			±0.003			±0.003	% of FSR[3]
Gain Error[4], Voltage		±0.01	±0.1		±0.05	±0.15		±0.05	±0.15	%
Current		±0.05	±0.25		±0.05	±0.25		±0.05	±0.25	%
Offset Error[4], Voltage, Unipolar		±0.1	±2.0		±0.1	±2.0		±0.1	±2.0	mV
Voltage, Bipolar			±5.0			±10.0			±10.0	mV
Current, Unipolar			±1.0			±1.0			±1.0	μA
Current, Bipolar			±5.0			±5.0			±5.0	μA
Monotonicity Temp. Range (14-Bits)	0		+50	0		+50	0		+70	°C
DRIFT (Over Specified Temp. Range)										
Total Bipolar Drift (includes gain, offset, and linearity drift)										
Voltage										
T_{min} to 25°C		±7	±15		±7	±15		±5	±19	ppm of FSR/°C
25°C to T_{max}		±7	±15		±7	±15		±5	±11	ppm of FSR/°C
Current										
T_{min} to T_{max}		±15			±15			±10		ppm of FSR/°C
TOTAL ERROR OVER TEMP. RANGE[5]										
Voltage, Unipolar										
T_{min} to +25°C			±0.083			±0.083			±0.100	% of FSR
+25°C to T_{max}			±0.083			±0.083			±0.072	% of FSR
Voltage, Bipolar										
T_{min} to +25°C			±0.071			±0.071			±0.100	% of FSR
+25°C to T_{max}			±0.071			±0.071			±0.072	% of FSR
Current, Unipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
Bipolar (T_{min} to T_{max})			±0.23			±0.23			±0.24	% of FSR
TEMPERATURE COEFFICIENTS										
Gain										
Voltage										
T_{min} to +25°C			±15			±15			±15	ppm of FSR/°C
+25°C to T_{max}			±15			±15			±7	ppm of FSR/°C
Current		±15			±15			±10		ppm of FSR/°C
Offset										
Voltage, Unipolar		±1	±2		±1	±2		±1	±2	ppm of FSR/°C
Bipolar			±10			±10			±8	ppm of FSR/°C
Current, Unipolar			±1			±1			±1	ppm of FSR/°C
Bipolar		±15			±15			±10		ppm of FSR/°C
Differential Linearity over Temperature			±2			±2			±1	ppm of FSR/°C
Linearity Error over Temperature			±2			±2			±1	ppm of FSR/°C
SETTLING TIME										
Voltage Models (to ±0.003% of FSR)										
Output: 20V Step		5	10		5	10		5	10	μs
1LSB Step[6]		3	5		3	5		3	5	μs
Slew Rate		20			20			20		V/μs
Current Models (to ±0.003% of FSR)[7]										
Output: 2mA step 10Ω to 100Ω Load			1			1			1	μs
1kΩ Load			3			3			3	μs
Switching Transient		500			500			500		mV
ANALOG OUTPUT										
Voltage Models										
Ranges–CSB		0 to +10			0 to +10			0 to +10		V
COB		±10			±10			±10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges–CSB		0 to −2			0 to −2			0 to −2		mA
COB		±1			±1			±1		mA
Output Impedance–Unipolar		6.0			6.0			6.0		kΩ
Bipolar		3.0			3.0			3.0		kΩ
Compliance	−1.5		+10	−1.5		+10	−1.5		+10	V
INTERNAL REFERENCE VOLTAGE	6.0	6.3	6.6	6.0	6.3	6.6	6.0	6.3	6.6	V
Maximum External Current[8]			±3			±3			±3	mA
Temp. Coeff. of Drift			±10			±10			±5	ppm/°C
POWER SUPPLY SENSITIVITY										
Unipolar Offset										
±15V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S
Bipolar Offset										
±15V dc		±0.0004			±0.0004			±0.0004		% of FSR/% V_S
+5V dc		±0.0001			±0.0001			±0.0001		% of FSR/% V_S

MODEL	AD DAC71/AD DAC71H MIN	TYP	MAX	AD DAC72C MIN	TYP	MAX	AD DAC72 MIN	TYP	MAX	UNITS
POWER SUPPLY SENSITIVITY (Continued)										
Gain										
± 15V dc		±0.001			±0.001			±0.001		% of FSR/% V_S
+ 5V dc		±0.0005			±0.0005			±0.0005		% of FSR/% V_S
POWER SUPPLY REQUIREMENTS										
DAC71/72	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	±14.5, +4.75	±15.0, +5.0	±15.5, +5.25	V dc
Supply Drain, + 15V dc (no load)		10	20		10	20		10	20	mA
− 15V dc (no load)		30	55		30	55		30	55	mA
+ 5V dc (logic supply)		10	20		10	20		10	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating (double above Drift Specs)	−25		+85	−25		+85	−55		+100	°C
Storage	−55		+100	−55		+100	−55		+110	°C

NOTES

[1]Adding external CMOS hex buffers CD4009A will provide 15V dc CMOS input compatibility.

[2]Accuracy is specified when using internal feedback resistors. Current output specifications are guaranteed at the voltage output of an external op amp using the internal feedback resistor.

[3]FSR means Full Scale Range and is 20V for ± 10V range.

[4]Adjustable to zero with external trim potentiometer.

[5]With gain and offset errors adjusted to zero at 25°C.

[6]LSB is for 14-bit resolution.

[7]Parameter guaranteed, not tested.

[8]Maximum with no degradation of specification.

Specifications subject to change without notice.

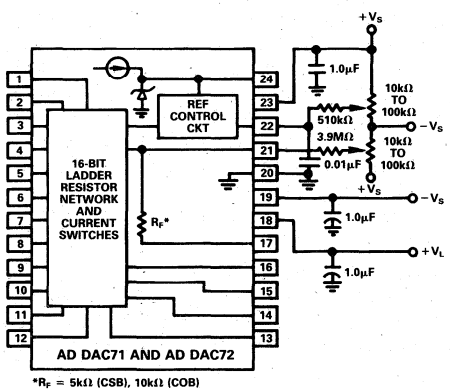


Figure 1. External Adjustment and Voltage Supply Connection Diagram, Current Model

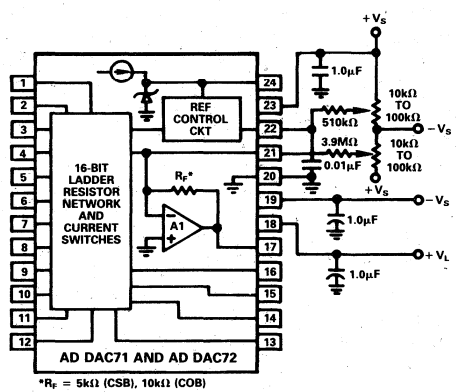


Figure 2. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The AD DAC71 and AD DAC72 accept complementary digital input codes in a binary format. The CSB (complementary straight binary) versions provide unipolar outputs proportional to the binary input code. The COB (complementary offset binary) versions deliver a bipolar analog output in response to the offset binary digital input code. The COB versions can also be used with CTS (complementary two's complement) coding by inverting the most significant bit. Table I shows the relationship between the digital inputs and analog outputs. If the DAC is used for 14-bit resolution, bits 15 and 16 should be tied to +5V through a 1kΩ resistor.

		CSB Compl. Straight Binary	COB Compl. Offset Binary	CTS Compl. Two's Compl.
All Bits On	0000 . . . 0000	+ Full Scale	+ Full Scale	− 1LSB
Mid-Scale	0111 . . . 1111	+ 1/2 Full Scale	Zero	− Full Scale
All Bits Off	1111 . . . 1111	Zero	− Full Scale	Zero
	1000 . . . 0000	Mid-Scale − 1LSB	− 1LSB	+ Full Scale

Table I. Digital Input Codes

ACCURACY

Linearity Error

Linearity error is the most important accuracy specification in a digital-to-analog converter, since it cannot be externally trimmed or adjusted. Linearity is defined as the deviation of the DAC's actual analog output from a straight line drawn between the endpoints. The AD DAC71 and AD DAC72 feature guaranteed maximum linearity error of 0.003% of full scale.

Differential Linearity Error

Differential linearity error is the deviation from an ideal 1LSB output change when the digital input changes 1LSB. A differential linearity error specification of 1/2LSB means that the output changes at least 1/2LSB and at most ±1 1/2LSB for a 1LSB increment in digital input code.

Monotonicity

Monotonicity indicates that the output of the DAC in question will always increase (or stay the same) for an increasing digital input code. Converters generally specify the maximum resolution for which monotonicity is guaranteed over a particular temperature range. The AD DAC71, AD DAC71H and AD DAC72C are guaranteed monotonic at 14-bit resolution for 0 to +50°C, while the AD DAC72 is guaranteed 14-bit monotonic from 0 to +70°C.

Drift

Gain drift is a measure of the change in full scale output range as a function of temperature, expressed in parts per million (ppm) per °C. Gain drift is computed by testing the full scale range at +25°C and the endpoints of the applicable temperature range. The resulting change is divided by the temperature change and converted to ppm/°C.

Offset drift is a measure of the actual change in output with all "1"s on the digital inputs as a result of changes in temperature. For COB versions, the bipolar offset drift is measured with an input code of 011111111111.

Settling Time

Settling time is defined as the total time required for the analog output to settle to within a particular error band around its final value after a change in the digital input code. In the case of the AD DAC71 and AD DAC72, the error band is specified as 0.003% of full scale. The specification for a 1LSB change is measured at the major carry (1000 . . . 00 to 0111 . . . 11) with the LSB defined as the 14-bit LSB.

Current output versions are specified for settling into two different resistive loads: 10Ω to 100Ω and 1000Ω.

Output Compliance Voltage

Compliance voltage is the maximum voltage swing allowed on the output of the current models while maintaining specified accuracy. The AD DAC71 and AD DAC72 are specified for a compliance range of −1.5 volts to +10 volts.

Power Supply Sensitivity

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of change in either the positive, negative, or logic supplies about the nominal power supply voltages.

Reference Supply

All AD DAC71 and AD DAC72 models are supplied with an internal +6.3V reference voltage supply. This reference voltage (pin 24) has a tolerance of 5% and is connected internally for specified operation. The zener is selected for a gain drift of typically 3ppm/°C and is burned-in for a total of 72 hours for guaranteed reliability. This reference may also be used externally but the current drain is limited to 3mA. An external buffer amplifier is recommended if the AD DAC71 and AD DAC72 internal reference is used externally in order to provide a constant load to the reference supply output.

TRIMMING INSTRUCTIONS

The AD DAC71 and AD DAC72 include provisions for calibration of gain and offset. Figures 1 and 2 show the proper connections. Offset adjustment should be performed prior to gain adjustment.

Offset Adjustment

For unipolar output (CSB) versions, offset trim is accomplished by applying the digital input code which should produce a zero output and adjusting the offset trim potentiometer for zero output. Bipolar output (COB) versions are trimmed by applying the digital input code corresponding to negative full scale output and adjusting the offset potentiometer for exactly −10.00000V.

Gain Adjustment

This step is the same for both unipolar and bipolar versions. Apply the digital code which corresponds to the maximum positive output voltage and adjust the gain trim potentiometer for an output of 1LSB below full scale (FS − 1LSB). Refer to Table II for the appropriate output values. The 510kΩ resistor shown in Figures 1 and 2 may be any value from 270kΩ to 1.5MΩ. Higher values will improve trim resolution but decrease trim range.

DIGITAL INPUT	OUTPUT			
	VOLTAGE		CURRENT	
	14 BIT	16 BIT	14 BIT	16 BIT
CSB (Complementary Straight Binary)				
All Bits "ON" (00...00)	+9.99939V	+9.99985V	−1.99988mA	−1.99997mA
All Bits "OFF" (11...11)	0	0	0	0
1LSB	610μV	153μV	0.122μA	0.031μA
COB (Complementary Offset Binary)				
All Bits "ON" (00...00)	+9.99878V	+9.99969V	−0.99988mA	−0.999978mA
MSB Only "ON" (01...11)	0	0	0	0
All Bits "OFF" (11...11)	−10.0000V	−10.0000V	+1.00000mA	+1.00000mA
1LSB	1.22mV	305μV	0.122μA	0.031μA

Table II. Ideal Analog Outputs at Various Digital Inputs

PRESERVING THE ACCURACY OF THE AD DAC71 AND AD DAC72

A great deal of care must be exercised when using high resolution converters such as the AD DAC71 and AD DAC72. Since one least significant bit of a 16-bit converter (LSB) represents an analog voltage of only 153 microvolts out of a 10V scale, normally negligible error sources become significant. Series resistances of connectors and wiring can be major contributors, as can thermocouple effects. Figure 3 illustrates the connections for voltage output versions of the AD DAC71 and AD DAC72.

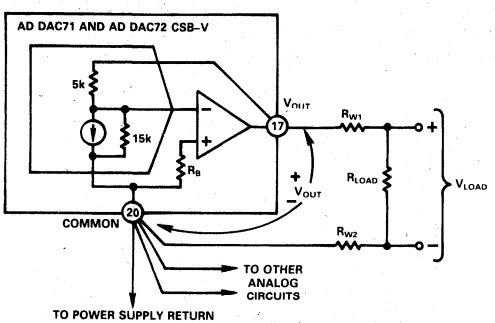


Figure 3. AD DAC71 and AD DAC72 Connection Diagram (Voltage Models)

In this circuit, the analog output voltage is accurately developed between pin 17 and pin 20 of the DAC. The voltage measured at the load will be inaccurate if there is significant resistance in the wiring (and any connectors) between the DAC and the load. If the load resistance is constant, the effects of R_{W1} and R_{W2} can be treated as a simple gain error, and can be trimmed out. However, if R_L is variable, then R_{W1} and R_{W2} should be reduced to a value less than $\frac{R_{L\ MIN}}{2^{16}}$. This will reduce the effect of the wiring resistances to a gain error of less than 1LSB. The AD DAC71 and AD DAC72 are rated at an output current of 5mA which translates to a minimum load resistance of 2kΩ. Thus wiring resistances should be held to a maximum of 30 milliohms. This corresponds to approximately six inches of #28 wire or a six inch long printed circuit track 0.050 inches wide.

The current output versions of the AD DAC71 and AD DAC72 use an external operational amplifier to convert the output current to an output voltage. The recommended configuration is shown in Figure 4. Notice that this configuration permits the voltage at the load to the sensed remotely. The resistance (R_{W1}) of the lead connecting the load to the internal feedback resistor introduces a gain error equal to $\frac{R_{W1}}{R_{LOAD}}$, independent of R_{LOAD} and R_{W2}. The error contributed by R_{W3} depends upon where the output is measured. If the output is measured between the top of R_{LOAD} and pin 20 of the DAC, no error results since R_{W3} effectively becomes part of the load resistance.

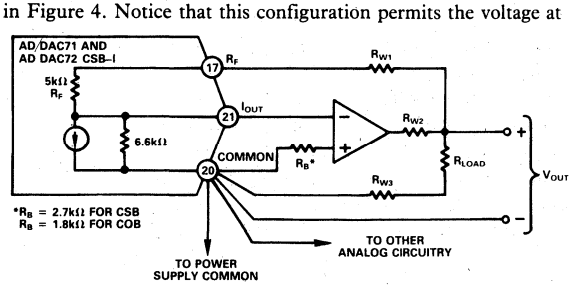


Figure 4. Connections for AD DAC71 and AD DAC72 Current Output Versions

In applications where R_{W3} is large or large currents flow in R_{W3}, it is necessary to use remote sensing as shown in Figure 5.

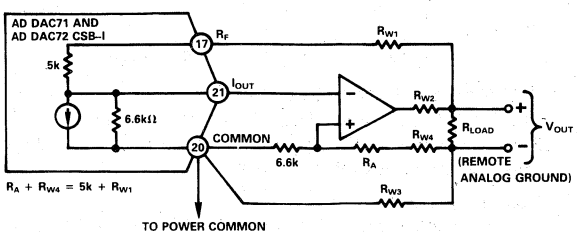


Figure 5. Use of Output Amplifier as Subtractor for Remote Ground Sensing

This circuit uses the output amplifier as a subtractor stage. Any spurious voltage developed across R_{W3} becomes a common mode voltage and its error contribution is reduced by the common mode rejection of the op amp.

In the circuits of both Figure 4 and Figure 5, R_{W2}'s effect is negligible since it is inside the loop of the amplifier. If current boosting is required in order to drive heavy loads, a suitable booster stage can be inserted between the amplifier's output and the load. Since the loop is closed from the load end, offsets and other errors induced by the booster are eliminated.

It is also important to minimize thermocouple effects in circuitry using the AD DAC71 and AD DAC72. Recalling that 1LSB of a 16 bit, 10 volt scale converter is only 153 microvolts, a stray uncompensated thermocouple can introduce several LSBs of offset in response to minor changes in ambient temperature. Any part of a circuit which includes a junction between two dissimilar metals forms a thermocouple. Such junctions include connectors, sockets, and any soldered connections. The solution to thermocouple errors is to insure that every junction is cancelled by an identical, but opposite, junction at the same temperature. While this is often automatically accomplished (for example, in a connector carrying both signal and return leads), careful attention should be given to the physical layout of circuits using the AD DAC71 and AD DAC72.

Another source of signal degradation in high-resolution converter circuits is magnetically-coupled interference from stray fields. Signal and return leads should be arranged in a way which minimizes both length and the total cross-section area of the loop. Of course, high resolution circuits should be located as far as possible from any sources of electromagnetic interference, including power transformers, digital logic and electromechanical devices.

ALTERNATE TRIM CIRCUIT

As shown in Figures 1 and 2, offset trimming is accomplished by using an external potentiometer connected through a 3.9MΩ resistor to pin 21 of the AD DAC71 and AD DAC72. In some applications, it may be desirable to use an equivalent "T" network of lower-value resistors. A suggested circuit is shown in Figure 6. These resistors and the trimming potentiometer should be located close to the DAC to minimize noise pickup.

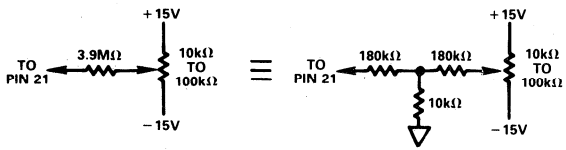


Figure 6. Equivalent Trim Circuit

DRIVING RESISTIVE LOADS

The AD DAC71 and AD DAC72 current output models can drive resistive loads directly without the use of an external op amp as a current-to-voltage converter.

Unipolar Models

The unipolar current output version of the AD DAC71 and AD DAC72 delivers a nominal −2mA full scale output. Since the output compliance voltage range is specified as ±2.5V, the parallel combination of the DAC resistance and load resistance must be held below a maximum value of 750Ω, limiting load resistance to a maximum of 857Ω. The output voltage for lower values of R_L can be computed from the formula:

$$V_{OUT} = -2mA \frac{(6k\Omega \times R_L)}{(6k\Omega + R_L)}$$

The output voltage thus produced will always be negative, and must be limited to a maximum of −1.5V for proper operation.

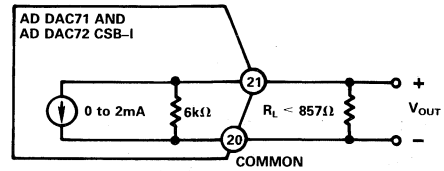


Figure 7. Connections for Unipolar Output AD DAC71 and AD DAC72 Driving Resistive Load

Bipolar Models

The bipolar current output versions of the AD DAC71 and AD DAC72 produce a nominal ±1mA output range. The output resistance of the bipolar versions is approximately 3kΩ. The external load resistance for a given output voltage range can be computed from the relationship:

$$V_{OUT} = \pm 1mA \frac{(3k\Omega \times R_L)}{(3k\Omega + R_L)}$$

The maximum permissible voltage swing is −1.5 to +10V, which limits the maximum value of R_L to 3kΩ.

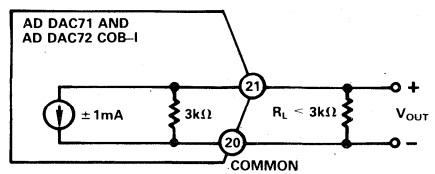


Figure 8. Connections for Bipolar Output AD DAC71 and AD DAC72 Driving Resistive Load

ORDERING GUIDE

Model	Output	Input Code	Temp Range	Seal	Package[1] Identification
AD DAC71–COB–I	Current	Comp. Offset Binary	0 to +70°C	Polymer	HY24B
AD DAC71–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Polymer	HY24B
AD DAC71H–COB–I	Current	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC71H–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–COB–I	Current	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–CSB–I	Current	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72–COB–I	Current	Comp. Offset Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC72–CSB–I	Current	Comp. Straight Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC71–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Polymer	HY24B
AD DAC71–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Polymer	HY24B
AD DAC71H–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC71H–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–COB–V	Voltage	Comp. Offset Binary	0 to +70°C	Hermetic	HY24B
AD DAC72C–CSB–V	Voltage	Comp. Straight Binary	0 to +70°C	Hermetic	HY24B
AD DAC72–COB–V	Voltage	Comp. Offset Binary	−25°C to +85°C	Hermetic	HY24B
AD DAC72–CSB–V	Voltage	Comp. Straight Binary	−25°C to +85°C	Hermetic	HY24B

[1]See Section 19 for package outline information.

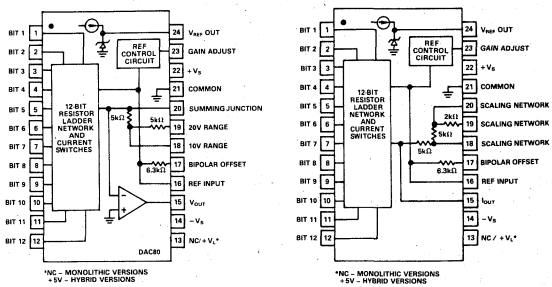
Complete Low Cost 12-Bit Monolithic D/A Converter

AD DAC80, AD DAC85, AD DAC87

FEATURES

- **Single Chip Construction**
- **On-Board Output Amplifier**
- **Low Power Dissipation: 300mW**
- **Monotonicity Guaranteed over Temperature**
- **Guaranteed for Operation with ±12V Supplies**
- **Improved Replacement for Standard DAC80, DAC800 HI-5680**
- **High Stability, High Current Output Buried Zener Reference**
- **Laser Trimmed to High Accuracy: ±1/2LSB max Nonlinearity**
- **Low Cost Plastic Packaging**

AD DAC80 SERIES FUNCTIONAL BLOCK DIAGRAM



9

PRODUCT DESCRIPTION

The AD DAC80 Series is a family of low cost 12-bit digital-to-analog converters with both a high stability voltage reference and output amplifier combined on a single monolithic chip. The AD DAC80 Series is recommended for all low cost 12-bit D/A converter applications where reliability and cost are of paramount importance.

Advanced circuit design and precision processing techniques result in significant performance advantages over conventional DAC80 devices. Innovative circuit design reduces the total power consumption to 300mW which not only improves reliability but also improves long term stability.

The AD DAC80 incorporates a fully differential, non-saturating precision current switching cell structure which provides greatly increased immunity to supply voltage variation. This same structure also reduces nonlinearities due to thermal transients as the various bits are switched; nearly all critical components operate at constant power dissipation. High stability, SiCr thin film resistors are trimmed with a fine resolution laser, resulting in lower differential nonlinearity errors. A low noise, high stability, subsurface zener diode is used to produce a reference voltage with excellent long term stability, high external current capability and temperature drift characteristics which challenge the best discrete zener references.

The AD DAC80 Series is available in three performance grades and two package types. The AD DAC80 is specified for use over the 0 to +70°C temperature range and is available in both plastic and ceramic DIP packages. The AD DAC85 and AD DAC87 are available in hermetically sealed ceramic packages and are specified for the −25°C to +85°C and −55°C to +125°C temperature ranges.

PRODUCT HIGHLIGHTS

1. The AD DAC80 series of D/A converters directly replaces all other devices of this type with significant increases in performance.
2. Single chip construction and low power consumption provides the optimum choice for applications where low cost and high reliability are major considerations.
3. The high speed output amplifier has been designed to settle within 1/2LSB for a 10V full scale transition in 2.0μs, when properly compensated.
4. The precision buried zener reference can supply up to 2.5mA for use elsewhere in the application.
5. The low TC binary ladder guarantees that all units are monotonic over the specified temperature range.
6. System performance upgrading is possible without redesign.

PRODUCT OFFERING

Analog Devices has developed a number of technologies to support products within the data acquisition market. In serving the market new products are implemented with the technology best suited to the application. The DAC80 series of products was first implemented in hybrid form and now it is available in a single monolithic chip. We will provide both the hybrid and monolithic versions of the family so that in existing designs changes to documentation or product qualification will not have to be done. Specifications and ordering information for both versions is delineated in this data sheet.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC80 Min	AD DAC80 Typ	AD DAC80 Max	AD DAC85 Min	AD DAC85 Typ	AD DAC85 Max	AD DAC87 Min	AD DAC87 Typ	AD DAC87 Max	Units
TECHNOLOGY		Monolithic			Monolithic			Monolithic		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	**+2.0**		**+5.5**	**+2.0**		**+5.5**	**+2.0**		**+5.5**	V
V_{IL} (Logic "0")	**0**		**+0.8**	**0**		**+0.8**	**0**		**+0.8**	V
I_{IH} (V_{IH} = 5.5V)			**250**			**250**			**250**	μA
I_{IL} (V_{IL} = 0.8V)			**100**			**100**			**100**	μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2			±1/2	LSB[1]
CCD										LSB
T_A @ T_{min} to T_{max}		±1/4	**±1/2**		±1/4	**±1/2**		±1/2	**±3/4**	LSB
Differential Linearity Error @ +25°C										
CBI			**±3/4**			**±3/4**			**±3/4**	LSB
CCD										LSB
T_A @ T_{min} to T_{max}			**±3/4**			**±1**			**±1**	LSB
Gain Error[2]		±0.1	**±0.3**		±0.1	**±0.2**		±0.1	**±0.2**	%FSR[3]
Offset Error[2]		±0.05	**±0.15**		±0.05	**±0.1**		±0.05	**±0.1**	%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	−25		+85	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20			±20			±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15		±0.12	±0.2		±0.18	±0.3	% of FSR
Bipolar		±0.06	±0.10		±0.08	±0.12		±0.14	±0.24	% of FSR
Gain										
Including Internal Reference		±15	**±30**			**±20**			**±20**	ppm of FSR/°C
Excluding Internal Reference		±4	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	**±3**			**±3**			**±3**	ppm of FSR/°C
Bipolar Offset		±5	**±10**			**±10**			**±10**	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩFeedback		3	4		3	4		3	4	μs
with 5kΩFeedback		2	3		2	3		2	3	μs
For LSB Change		1			1			1		μs
Slew Rate	10			10			10			V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Current			40			40			40	mA
Current Models										
Ranges – Unipolar	**−1.96**	−2.0	**−2.04**	**−1.96**	−2.0	**−2.04**	**−1.96**	−2.0	**−2.04**	mA
– Bipolar	**±0.96**	±1.0	**±1.04**	**±0.96**	±1.0	**±1.04**	**±0.96**	±1.0	**±1.04**	mA
Output Impedance – Bipolar	2.5	3.2	4.1	2.5	3.2	4.1	2.5	3.2	4.1	kΩ
– Unipolar	5.0	6.6	8.2	5.0	6.6	8.2	5.0	6.6	8.2	kΩ
Compliance	−2.5		+10	−2.5		+10	−2.5		+10	V
Internal Reference Voltage (V_R)	**+6.23**	+6.3	**+6.37**	**+6.23**	+6.3	**+6.37**	**+6.23**	+6.3	**+6.37**	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			**+2.5**			**+2.5**			**+2.5**	mA
Tempco of Drift		±10	±20		±10	±20			±10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable			**±0.002**			**±0.002**			**±0.002**	% of FSR/%V_S
±12V ±5%			**±0.002**			**±0.002**			**±0.002**	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15			±15			±15		V
Range										
Analog Supplies	±11.4[7]		±16.5	±11.4[7]		±16.5	±11.4[7]		±16.5	V
Logic Supplies									V	
Supply Drain										
+12, +15V		5	**10**		5	**10**		5	**10**	mA
−12, −15V		14	**20**		14	**20**		14	**20**	mA
+5V										mA
TEMPERATURE RANGE										
Specification	0		+70	−25		+85	−55		+125	°C
Operating	−25		+85	−55		+125	−55		+125	°C
Storage	−25		+125	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]A minimum of ±12.3V is required for a ±10V full scale output and ±11.4V is required for all other voltage ranges.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC80 Min	AD DAC80 Typ	AD DAC80 Max	AD DAC85C Min	AD DAC85C Typ	AD DAC85C Max	AD DAC85 Min	AD DAC85 Typ	AD DAC85 Max	Units
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD			3			3			3	Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+1			+1			+1		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI		±1/4	±1/2			±1/2			±1/2	LSB[1]
CCD		±1/8	±1/4			±1/4			±1/4	LSB
T_A @ T_{min} to T_{max}		±1/4	±1/2		±1/4	±1/2		±1/2	±1/2	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2	±3/4		±1/2			±1/2		LSB
CCD		±1/4	±1/2		±1/2			±1/2		LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1	±0.3		±0.1			±0.1		%FSR[3]
Offset Error[2]		±0.05	±0.15		±0.05			±0.05		%FSR[3]
Temperature Range for Guaranteed Monotonicity	0		+70	0		+70	−25		+85	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)			±20							ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		±0.08	±0.15							% of FSR
Bipolar		±0.06	±0.10							% of FSR
Gain										
Including Internal Reference		±15	±30			±20			±20	ppm of FSR/°C
Excluding Internal Reference		±5	±7			±10			±10	ppm of FSR/°C
Unipolar Offset		±1	±3		±1			±1		ppm of FSR/°C
Bipolar Offset		±5	±10			±10			±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ||500pF load)										
with 10kΩFeedback		5			5			5		μs
with 5kΩFeedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate	10	15			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD		±10			+10			+10		V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2			3.2		kΩ
– Unipolar		6.6			6.6			6.6		kΩ
Compliance		−1.5, +10			−2.5, +10			−2.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	±20		±10	±20		±10	±20	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002		% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14		±16	±14.5		±15.5	±14.5		±15.5	V
Logic Supplies	+4.5		+16	+4.5		+15.5	+4.5		+15.5	V
Supply Drain[7]										
+15V		10	20		15	20		15	20	mA
−15V		20	35		25	30		25	30	mA
+5V		8	20		15	20		15	20	mA
TEMPERATURE RANGE										
Specification	0		+70	0		+70	−25		+85	°C
Operating	−25		+85	−25		+85	−55		+125	°C
Storage	−55		+130	−65		+150	−65		+150	°C

NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
Specifications subject to change without notice.

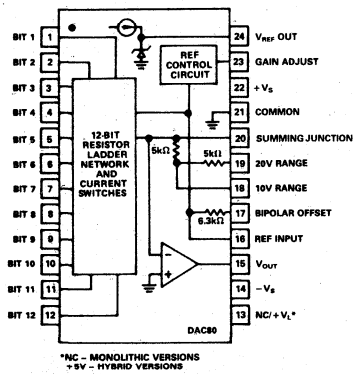
SPECIFICATIONS (T_A = +25°C, rated power supplies unless otherwise noted.)

Model	AD DAC85LD Min	AD DAC85LD Typ	AD DAC85LD Max	AD DAC85MIL Min	AD DAC85MIL Typ	AD DAC85MIL Max	AD DAC87 Min	AD DAC87 Typ	AD DAC87 Max	Units
TECHNOLOGY		Hybrid			Hybrid			Hybrid		
DIGITAL INPUT										
Binary – CBI			12			12			12	Bits
BCD – CCD		–			–			–		Digits
Logic Levels (TTL Compatible)										
V_{IH} (Logic "1")	+2.0		+5.5	+2.0		+5.5	+2.0		+5.5	V
V_{IL} (Logic "0")	0		+0.8	0		+0.8	0		+0.8	V
I_{IH} (V_{IH} = 5.5V)		+1			+1			+1		μA
I_{IL} (V_{IL} = 0.8V)		−100			−100			−100		μA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error @ +25°C										
CBI			±1/2			±1/2		±1/4	±1/2	LSB[1]
CCD		–			–			–		LSB
T_A @ T_{min} to T_{max}			±1/2			±3/4			±3/4	LSB
Differential Linearity Error @ +25°C										
CBI		±1/2			±1/2			±1/2		LSB
CCD										LSB
T_A @ T_{min} to T_{max}			±1			±1			±1	LSB
Gain Error[2]		±0.1			±0.1			±0.1	±0.2	% FSR[3]
Offset Error[2]		±0.05			±0.05			±0.05	±0.1	%FSR[3]
Temperature Range for Guaranteed Monotonicity	−25		+85	−55		+125	−55		+125	°C
DRIFT (T_{min} to T_{max})										
Total Bipolar Drift, max (includes gain, offset, and linearity drifts)		–			–			±15	±30	ppm of FSR/°C
Total Error (T_{min} to T_{max})[4]										
Unipolar		–			–			±0.13	±0.30	% of FSR
Bipolar		–			–			±0.12	±0.24	% of FSR
Gain										
Including Internal Reference			±10			±20		±10	±25	ppm of FSR/°C
Excluding Internal Reference								±5	±10	ppm of FSR/°C
Unipolar Offset		±1			±2			±1	±3	ppm of FSR/°C
Bipolar Offset			±5			±10		±5	±10	ppm of FSR/°C
CONVERSION SPEED										
Voltage Model (V)[5]										
Settling Time to ±0.01% of FSR for FSR change (2kΩ‖500pF load)										
with 10kΩFeedback		5			5			5		μs
with 5kΩFeedback		3			3			3		μs
For LSB Change		1.5			1.5			1.5		μs
Slew Rate		20			20			20		V/μs
Current Model (I)										
Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load		300			300			300		ns
for 1kΩ Load		1			1			1		μs
ANALOG OUTPUT										
Voltage Models										
Ranges – CBI		±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10			±2.5, ±5, ±10, +5, +10		V
– CCD										V
Output Current	±5			±5			±5			mA
Output Impedance (dc)		0.05			0.05			0.05		Ω
Short Circuit Duration		Indefinite to Common			Indefinite to Common			Indefinite to Common		
Current Models										
Ranges – Unipolar		−2.0			−2.0			−2.0		mA
– Bipolar		±1.0			±1.0			±1.0		mA
Output Impedance – Bipolar		3.2			3.2		2.5	3.2	4.1	kΩ
– Unipolar		6.6			6.6		5.0	6.6	8.2	kΩ
Compliance		−2.5, +10			−2.5, +10			−1.5, +10		V
Internal Reference Voltage (V_R)	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	+6.17	+6.3	+6.43	V
Output Impedance		1.5			1.5			1.5		Ω
Max External Current[6]			+2.5			+2.5			+2.5	mA
Tempco of Drift		±10	20		10	20		±5	10	ppm of V_R/°C
POWER SUPPLY SENSITIVITY										
±15V ±10%, 5V supply when applicable		±0.002			±0.002			±0.002	±0.003	% of FSR/%V_S
POWER SUPPLY REQUIREMENTS										
Rated Voltages		±15, 5			±15, 5			±15, 5		V
Range										
Analog Supplies	±14.5		±15.5	±14.5		±15.5	±13.5		±16.5	V
Logic Supplies	+4.5		+15.5	+4.5		+15.5	+4.5		+16.5	V
Supply Drain[7]										
+15V		15	20		15	20		10	20	mA
−15V		25	30		25	30		20	30	mA
+5V		15	20		15	20		10	20	mA
TEMPERATURE RANGE										
Specification	−25		+85	−55		+125	−55		+125	°C
Operating	−55		+125	−55		+125	−55		+125	°C
Storage	−55		+125	−55		+120	−65		+150	°C

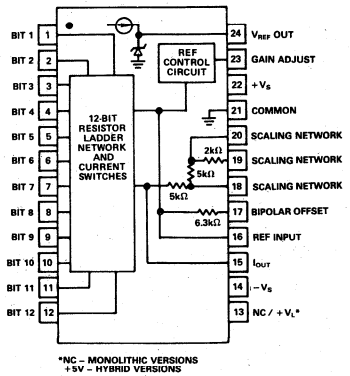
NOTES
[1]Least Significant Bit.
[2]Adjustable to zero with external trim potentiometer.
[3] FSR means "Full Scale Range" and is 20V for the ±10V range and 10V for the ±5V Range.
[4]Gain and offset errors adjusted to zero at +25°C.
[5]C_F = 0, see Figure 1a.
[6]Maximum with no degradation of specification, must be a constant load.
[7]Including 5mA load.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

$+V_S$ to Power Ground . . . . . 0V to +18V
$-V_S$ to Power Ground . . . . . 0V to −18V
Digital Inputs (Pins 1 to 12) to Power Ground . . . −1.0V to +7V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite short to power ground or $+V_S$



Voltage Model Functional Diagram and Pin Configuration



Current Model Functional Diagram and Pin Configuration

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ORDERING GUIDE

Model	Input Code	Output Mode	Technology	Temperature Range	Linearity Error	Package Option[1]
AD DAC80N-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	N24A
AD DAC80D-CBI-V	Binary	Voltage	Monolithic	0 to +70°C	±1/2LSB	D24A
AD DAC80D-CBI-I	Binary	Current	Monolithic	0 to +70°C	±1/2LSB	D24A
AD DAC85D-CBI-V	Binary	Voltage	Monolithic	−25°C to +85°C	±1/2LSB	D24A
AD DAC87D-CBI-V	Binary	Voltage	Monolithic	−55°C to +125°C	±1/2LSB	D24A
AD DAC80-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC80-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC80-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC80-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC80Z-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC80Z-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC80Z-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC80Z-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC85C-CBI-V	Binary	Voltage	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC85C-CBI-I	Binary	Current	Hybrid	0 to +70°C	±1/2LSB	HY24A
AD DAC85-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	HY24A
AD DAC85-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	HY24A
AD DAC85LD-CBI-V	Binary	Voltage	Hybrid	−25°C to +85°C	±1/2LSB	HY24A
AD DAC85LD-CBI-I	Binary	Current	Hybrid	−25°C to +85°C	±1/2LSB	HY24A
AD DAC85MIL-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	HY24A
AD DAC85MIL-CBI-I	Binary	Current	Hybrid	−55°C to +125°C	±1/2LSB	HY24A
AD DAC85C-CCD-V	Binary Coded Decimal	Voltage	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC85C-CCD-I	Binary Coded Decimal	Current	Hybrid	0 to +70°C	±1/4LSB	HY24A
AD DAC85-CCD-V	Binary Coded Decimal	Voltage	Hybrid	−25°C to +85°C	±1/4LSB	HY24A
AD DAC85-CCD-I	Binary Coded Decimal	Current	Hybrid	−25°C to +85°C	±1/4LSB	HY24A
AD DAC87-CBI-V	Binary	Voltage	Hybrid	−55°C to +125°C	±1/2LSB	HY24A

[1] See Section 19 for package outline information.

DIGITAL INPUT CODES

The AD DAC80 Series accepts complementary digital input code in binary (CBI) format. The CBI model may be connected by the user for anyone of three complementary codes: CSB, COB or CTC.

Digital Input		Analog Output		
MSB	LSB	CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
0 0 0 0 0 0 0 0 0 0 0 0		+ Full Scale	+ Full Scale	− 1LSB
0 1 1 1 1 1 1 1 1 1 1 1		+ 1/2 Full Scale	Zero	− Full Scale
1 0 0 0 0 0 0 0 0 0 0 0		Mid-Scale	− 1LSB	+ Full Scale
1 1 1 1 1 1 1 1 1 1 1 1		Zero	− Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected. Linearity error is specified over its entire temperature range. This means that the analog output will not vary by more than its maximum specification, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ± 1/2LSB means that the output voltage step sizes can range from 1/2LSB to 1 1/2LSB when the input changes from one adjacent input state to the next.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain drift is established by: 1) testing the end point differences for each AD DAC80 model at the lowest operating temperature, + 25°C and the highest operating temperature; 2) calculating the gain error with respect to the + 25°C value and; 3) dividing by the temperature change.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The maximum change in offset is referenced to the offset at + 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input.

Voltage Output Models. Three settling times are specified to ± 0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0 1 1 1 . . . 1 1 to 1 0 0 0 . . . 0 0), the point at which the worst case settling time occurs. The settling time characteristic depends on the compensation capacitor selected, the optimum value is 25pF as shown in Figure 1a.

Current Output Models. Two settling times are specified to ± 0.01% of FSR. Each is given for current models connected with two different resistive loads: 10 to 100 ohms and 1000 to 1875 ohms. Internal resistors are provided for connecting nominal load resistances of approximately 1000 to 1800 ohms for output voltage ranges of ± 1V and 0 to − 2V.

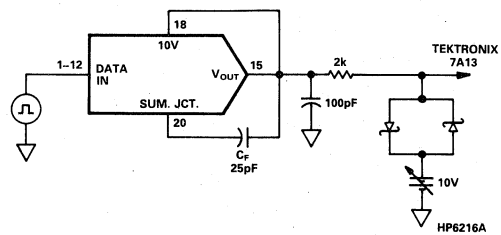


Figure 1a. Voltage Model Settling Time Circuit

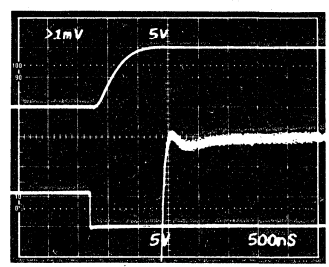


Figure 1b. Voltage Model Settling Time C_F = 25pF

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a per cent of FSR per per cent of change in either the positive or negative supplies about the nominal power supply voltages.

REFERENCE SUPPLY

All models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) is accurate to ± 1% and must be connected to the Reference Input (pin 16) for specified operation. This reference may also be used externally with external current drain limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations. All gain adjustments should be made under constant load conditions.

ANALYZING DEVICE ACCURACY OVER THE TEMPERATURE RANGE

For the purposes of temperature drift analysis, the major device components are shown in Figure 2. The reference element and buffer amplifier drifts are combined to give the total reference temperature coefficient. The input reference current to the DAC, I_{REF}, is developed from the internal reference and will show the same drift rate as the reference voltage. The DAC output current, I_{DAC}, which is a function of the digital input codes, is designed to track I_{REF}; if there is a slight mismatch in these currents over temperature, it will contribute to the gain T.C. The bipolar offset resistor, R_{BP}, and gain setting resistor, R_{GAIN}, also have temperature coefficients which contribute to system drift errors. The input offset voltage drift of the output amplifier, OA, also contributes a small error.

There are three types of drift errors over temperature: offset, gain, and linearity. Offset drift causes a vertical translation of the entire transfer curve; gain drift is a change in the slope of the curve; and linearity drift represents a change in the shape of the curve. The combination of these three drifts results in the complete specification for total error over temperature.

Total error is defined as the deviation from a true straight line transfer characteristic from exactly zero at a digital input which calls for zero output to a point which is defined as full scale. A specification for total error over temperature assumes that both the zero and full scale points have been trimmed for zero error at +25°C. Total error is normally expressed a percentage of the full scale range. In the bipolar situation, this means the total range from $-V_{FS}$ to $+V_{FS}$.

Several new design concepts not previously used in DAC80-type devices contribute to a reduction in all the error factors over temperature. The incorporation of low temperature coefficient silicon-chromium thin-film resistors deposited on a single chip, a patented, fully differential, emitter weighted, precision current steering cell structure, and a T.C. trimmed buried zener diode reference element results in superior wide temperature range performance. The gain setting resistors and bipolar offset resistor are also fabricated on the chip with the same SiCr material as the ladder network, resulting in low gain and offset drift.

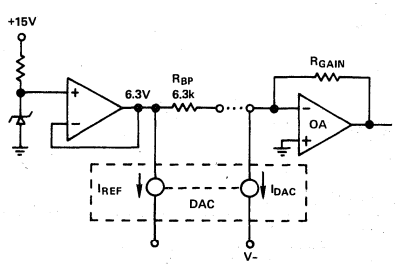


Figure 2. Bipolar Configuration

MONOTONICITY AND LINEARITY

The initial linearity error of ± 1/2LSB max and the differential linearity error of ± 3/4LSB max guarantee monotonic performance over the specified range. It can, therefore, be assumed that linearity errors are insignificant in computation of total temperature errors.

UNIPOLAR ERRORS

Temperature error analysis in the unipolar mode is straightforward: there is an offset drift and a gain drift. The offset drift (which comes from leakage currents and drift in the output amplifier (OA)) causes a linear shift in the transfer curve as shown in Figure 3. The gain drift causes a change in the slope of the curve and results from reference drift, DAC drift, and drift in R_{GAIN} relative to the DAC resistors.

BIPOLAR RANGE ERRORS

The analysis is slightly more complex in the bipolar mode. In this mode R_{BP} is connected to the summing node of the output amplifier (see Figure 2) to generate a current which, exactly balances the current of the MSB so that the output voltage is zero with only the MSB on.

Note that if the DAC and application resistors track perfectly, the bipolar offset drift will be zero even if the reference drifts. A change in the reference voltage, which causes a shift in the bipolar offset, will also cause an equivalent change in I_{REF} and thus I_{DAC}, so that I_{DAC} will always be exactly balanced by I_{BP} with the MSB turned on. This effect is shown in Figure 3. The net effect of the reference drift then is simply to cause a rotation in the transfer around bipolar zero. However, consideration of second order effects (which are often overlooked) reveals the errors in the bipolar mode. The unipolar offset drifts discussed before will have the same effect on the bipolar offset. A mismatch of R_{BP} to the DAC resistors is usually the largest component of bipolar drift, but in the AD DAC80 this error is held to 10ppm/°C max. Gain drift in the DAC also contributes to bipolar offset drift, as well as full scale drift, but again is held to 10ppm/°C max.

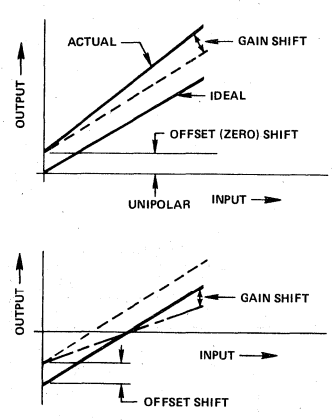


Figure 3. Unipolar and Bipolar Drifts

Using the AD DAC80 Series

POWER SUPPLY CONNECTIONS

For optimum performance power supply decoupling capacitors should be added as shown in the connection diagrams. These capacitors (1μF electrolytic recommended) should be located close to the AD DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for optimum high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external OFFSET and GAIN potentiometers. These potentiometers should be connected as shown in the block diagrams and adjusted as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 10MΩ resistors (20% carbon or better) should be located close to the AD DAC80 to prevent noise pickup. If it is not convenient to use these high-value resistors, a functionally equivalent "T" network, as shown in Figure 6 may be substituted in each case. The gain adjust (pin 23) is a high impedance point and a 0.01μF ceramic capacitor should be connected from this pin to common to prevent noise pickup.

Offset Adjustment. For unipolar (CSB) configurations, apply the digital input code that should produce zero potential output and adjust the OFFSET potentiometer for zero output. For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the FULL SCALE RANGE is connected for 20 volts, the maximum negative output voltage is −10V. See Table II for corresponding codes.

Gain Adjustment. For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the GAIN potentiometer for this positive full scale voltage. See Table II for positive full scale voltages.

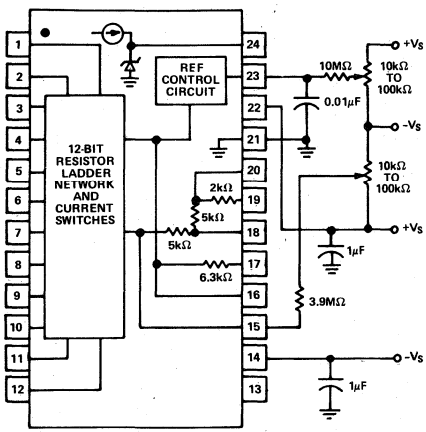


Figure 4. External Adjustment and Voltage Supply Connection Diagram, Current Model

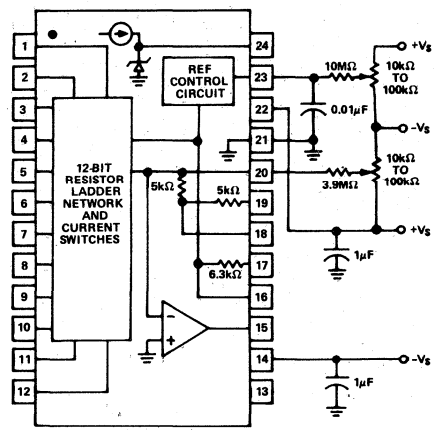


Figure 5. External Adjustment and Voltage Supply Connection Diagram, Voltage Model

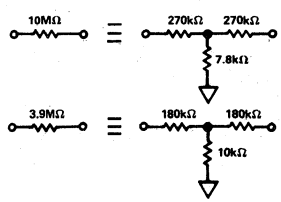


Figure 6. Equivalent Resistances

	Digital Input	Analog Output			
	12 Bit Resolution	Voltage*		Current	
	MSB LSB	0 to +10V	±10V	0 to −2mA	±1mA
CBI Model	0 0 0 0 0 0 0 0 0 0 0 0	+9.9976V	+9.9951V	−1.9995mA	−0.9995mA
	0 1 1 1 1 1 1 1 1 1 1 1	+5.0000V	0.0000V	−1.0000mA	0.0000mA
	1 0 0 0 0 0 0 0 0 0 0 0	+4.9976V	4.88mV	0.488mA	+1.000mA
	1 1 1 1 1 1 1 1 1 1 1 1	0.0000V	−10.0000V	0.0000mA	0.488μA
	1LSB	2.44mV	−0.0049V	−0.9995mA	+0.0005mA

*To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2; ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table II. Digital Input/Analog Output

VOLTAGE OUTPUT MODELS

Internal scaling resistors provided in the AD DAC80 may be connected to produce bipolar output voltage ranges of ±10, ±5 or ±2.5V or unipolar output voltage ranges of 0 to +5 or 0 to +10V (see Figure 7).

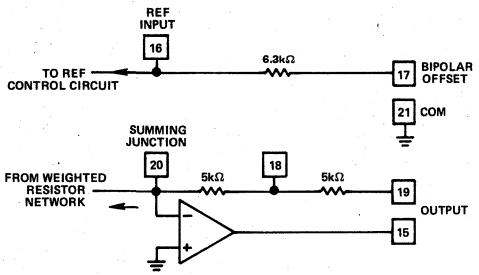


Figure 7. Output Amplifier Voltage Range Scaling Circuit

Gain and offset drift are minimized in the AD DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 4 microseconds for a 10kΩ feedback resistor; 3 microseconds for a 5kΩ feedback resistor when using the compensation capacitor shown in Figure 1.

The equivalent resistive scaling network and output circuit of the current model are shown in Figures 8 and 9. External R_{LS} resistors are required to produce exactly 0 to −2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the AD DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

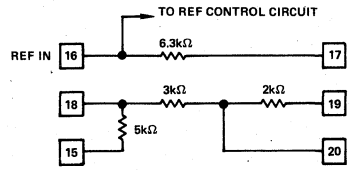


Figure 8. Internal Scaling Resistors

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to −2V. These resistors (R_{LI}: TCR = 20ppm/°C) are an integral part of the AD DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25ppm/°C or less to minimize drift. This will typically add ±50ppm/°C + the TCR of R_L (or R_F) to the total drift.

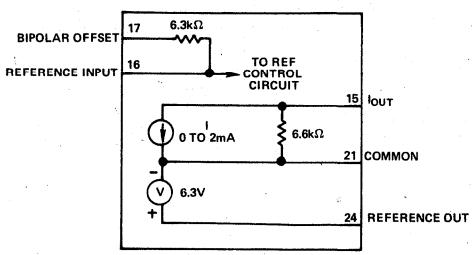


Figure 9. AD DAC80 Current Model Equivalent Output Circuit

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	20	15	24
±5V	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table III. Output Voltage Range Connections-Voltage Model AD DAC80

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	R_{LI} Connections			Reference	Bipolar Offset	
				Connect Pin 15 to	Connect Pin 18 to	Connect Pin 20 to	Connect Pin 16 to	Connect Pin 17 to	R_{LS}
CSB	0 to −2V	0.968kΩ	210Ω	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)
COB or CTC	±1V	1.2kΩ	249Ω	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)
CCD	0 to ±2V	3kΩ	N/A	N.C.	21	N.C.	24	N.C.	N/A

Table IV. Current Model/Resistive Load Connections

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 10 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{6.6k \times R_L}{6.6k + R_L}\right)$$

Where R_L max = 1.54kΩ

and V_{OUT} max = −2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to −2V. With $R_{LS} = 0$, $V_{OUT} = -1.69V$.

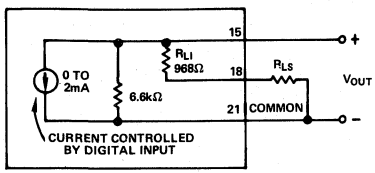


Figure 10. Equivalent Circuit AD DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent output circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1mA \left(\frac{R_L \times 3.22k}{R_L + 3.22k}\right)$$

Where R_L max = 11.18kΩ

and V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V. In this configuration, with R_{LS} equal to zero, the full scale range will be ±0.874V.

DRIVING AN EXTERNAL OP AMP

The current model AD DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. As seen in Figure 12,

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the AD DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model AD DAC80 provides output voltage ranges the same as the voltage model AD DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V and Figure 12.

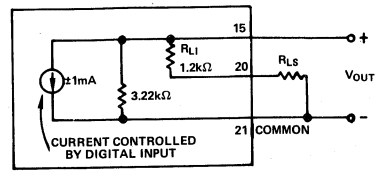


Figure 11. AD DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load

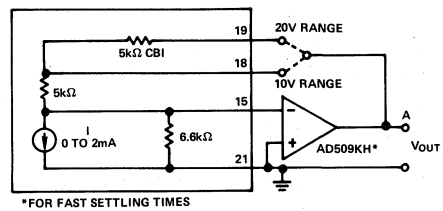


Figure 12. External Op Amp–Using Internal Feedback Resistors

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10 volts, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and −2mA for unipolar voltage ranges (see Figure 13). Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50ppm/°C + R_F drift to total drift.

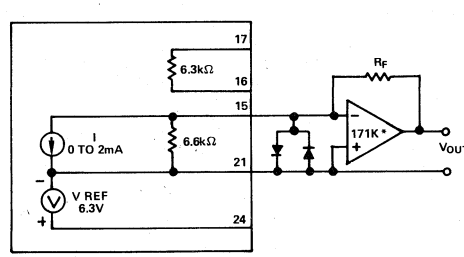


Figure 13. External Op Amp–Using External Feedback Resistors

Output Range	Digital Input Codes	Connect A to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	A	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24

Table V. External Op Amp Voltage Mode Connections

ANALOG DEVICES

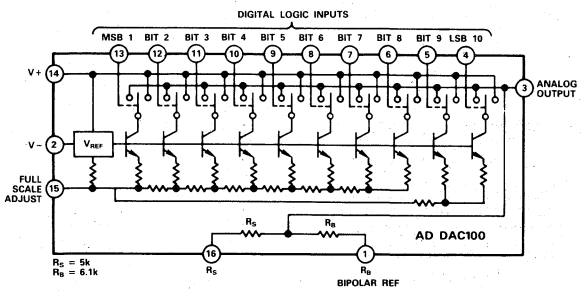
10-Bit Monolithic D/A Converter

AD DAC100

FEATURES

- **Complete Current Output Converter**
- **High Stability Buried Zener Reference**
- **Single Chip Monolithic Construction**
- **Wide Supply Range ±6V to ±18V**
- **Trimmed Output Application Resistors**
- **Fast Settling – 225ns (8 Bits), 375ns (10 Bits)**
- **Guaranteed Monotonicity Over Full Operating Temperature Range**
- **TTL and DTL Compatible Logic Inputs**
- **Hermetically-Sealed 16-Pin Ceramic DIP (All Grades)**

AD DAC100 FUNCTIONAL BLOCK DIAGRAM



9

PRODUCT DESCRIPTION

The AD DAC100 is a 10-bit digital-to-analog converter with a high stability voltage reference fabricated on a monolithic chip. Using 10 precision high-speed current-steering switches, a control amplifier, voltage reference, and laser-trimmed thin-film SiCr resistor network, the device produces a fast, accurate analog output current. Laser trimmed output application resistors are also included to facilitate accurate, stable current-to-voltage conversion.

The AD DAC100 also incorporates a low noise, high stability subsurface zener diode to produce a reference voltage with excellent long term stability and temperature cycle characteristics which challenge the best discrete zener references. A temperature compensation circuit is laser-trimmed to allow correction of the temperature coefficient of each device. This results in a maximum full-scale temperature coefficient of 15ppm/°C for the L version, 30ppm/°C max for the K and T versions, 60ppm/°C max for the J and S versions.

All grades are packaged in a 16-pin hermetically-sealed ceramic dual-in-line package. The J, K, L versions are specified for operation over the −25°C to +85°C temperature range, the AD DAC100S and T for operation over the extended temperature range from −55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD DAC100 is a true second-source equivalent to the industry standard DAC100.
2. The high impedance current output can be used with an external op amp and the internal applications resistors to produce a low impedance output voltage.
3. The AD DAC100 is available with a 10 volt range; for 5 volt version, consult factory.
4. The AD DAC100 is available in chip form for use in hybrid microcircuits.

SPECIFICATIONS ($V_S = \pm 15V$, $-25°C \leq T_A \leq +85°C$ for J, K, L devices; $-55°C \leq T_A \leq +125°C$ for S and T devices unless otherwise specified)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution					10	Bits
Nonlinearity	N_L	K, L, T ($\pm$ ½LSB – 10 Bits)	–	–	± 0.05	% FS
	N_L	J, S ($\pm$ ½LSB – 9 Bits)	–	–	± 0.1	% FS
Full Scale Tempco	T_C	L	–	–	± 15	ppm/°C
	T_C	K, T	–	–	± 30	ppm/°C
	T_C	J, S	–	–	± 60	ppm/°C
Settling Time $T_A = \pm 25°C$	t_S	to $\pm 0.05\%$ FS	–	–	375	ns
	t_S	to $\pm 0.1\%$ FS	–	–	300	ns
	t_S	to $\pm 0.2\%$ FS	–	–	225	ns
	t_S	to $\pm 0.4\%$ FS	–	–	150	ns
	t_S	to $\pm 0.8\%$ FS	–	–	100	ns
Full Range Output Voltage* (Adjustable to 10.0V with External 200Ω Trimmer)	V_{FR}	Connect FS Adjust to V–	10	–	11.1	V
Zero Scale Output Voltage	V_{ZS}	$V_{IN} = 2.1V$	–	–	0.013	% FS
Logic Inputs: High	V_{INH}	Measured with Respect to Output Pin	2.1	–	–	V
Logic Inputs: Low	V_{INL}	Measured with Respect to Output Pin	–	–	0.7	V
Logic Input Current, Each Input	I_{IN}	$V_{IN} = 0$ to $+6V$	–	–	5	µA
Logic Input Resistance	R_{IN}	$V_{IN} = 0$ to $+6V$	–	3	–	MΩ
Logic Input Capacitance	C_{IN}		–	2	–	pF
Output Resistance	R_O		–	500	–	kΩ
Output Capacitance	C_O		–	13	–	pF
Applied Power Supplies: V+		Linearity within Specification	+6	–	+18	V
Applied Power Supplies: V–		Linearity within Specification	–6	–	–18	V
Power Supply Sensitivity	P_{SS}	$V_S \pm \pm 6V$ to $\pm 18V$	–	–	± 0.10	% per volt
Power Consumption	P_D	$V_S = \pm 15V$	–	200	250	mW
Positive Supply Current	I+	$V_S = +15V$	–	–	8.33	mA
Negative Supply Current	I–	$V_S = -15V$	–	–	–8.33	mA

NOTES
*Using external op amp for I/V conversion (see Figure 3).
Specifications subject to change without notice.

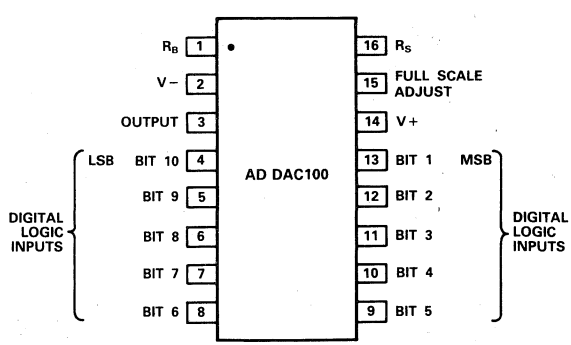
ABSOLUTE MAXIMUM RATINGS

V+ Supply to V– Supply . . . . . 0 to + 36V
V+ Supply to Output . . . . . 0 to +18V
V– Supply to Output . . . . . 0 to –18V
Logic Inputs to Output . . . . . –1V to +6V
Power Dissipation[1] 500mW

Operating Temperature Range
AD DAC100J, K, L . . . . . –25°C to +85°C
AD DAC100S, T . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering) . . . . . +300°C (60 sec)

NOTE
[1]Rating applies to ambient temperature of 100°C. Above 100°C, derate at 10mW/°

PIN CONFIGURATION
TOP VIEW



AD DAC100 ORDERING GUIDE

Model	Temperature Range	Maximum Linearity Error %	Max T.C. ppm/°C	Package Type[1]
AD DAC100JD	−25°C to +85°C	0.1	60	D16A
AD DAC100KD	−25°C to +85°C	0.05	30	D16A
AD DAC100LD	−25°C to +85°C	0.05	15	D16A

[1]See Section 19 for package outline information.

CROSS REFERENCE

Analog Devices	Precision Monolithics Inc.
AD DAC100JD	DAC-100 BCQ1, BCQ3, CCQ1, CCQ3, DDQ1, DDQ3
AD DAC100KD	DAC-100 ABQ1, ACQ1, ACQ3, BBQ1, BBQ3
AD DAC100LD	DAC-100 AAQ1

Applying the AD DAC100

DIGITAL INPUT CODES

The AD DAC100 accepts complementary digital input codes in either binary, offset binary or two's complement (see Table I).

DIGITAL INPUT	ANALOG OUTPUT		
MSB LSB	Compl. Straight Binary	Compl. Offset Binary	Compl.* Two's Compl.
0000000000	+Full Scale	+Full Scale	−LSB
0111111111	+½ Full Scale	Zero	−Full Scale
1000000000	Mid-scale −LSB	−LSB	+Full Scale
1111111111	Zero	−Full Scale	Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

Table I. Digital Input Codes

ACCURACY

Accuracy error of a D/A converter is the difference between the analog output that is expected when a given digital code is applied and the output that is actually measured with that code applied to the converter. Accuracy error can be caused by gain error, zero error, linearity error, or any combination of the three. Of these three specifications, the linearity error specification is the most important since it cannot be corrected for. The linearity error of the AD DAC100 is specified over its entire temperature range. This means that the analog output will not vary by more than ±½LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range (see Figures 1 and 2).

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1LSB means that the output voltage step sizes can range from 0LSB to 2LSB when the input changes from one adjacent input state to the next. Monotonicity over the full temperature range is guaranteed in the AD DAC100 to insure that the analog output will not decrease with increasing input digital codes.

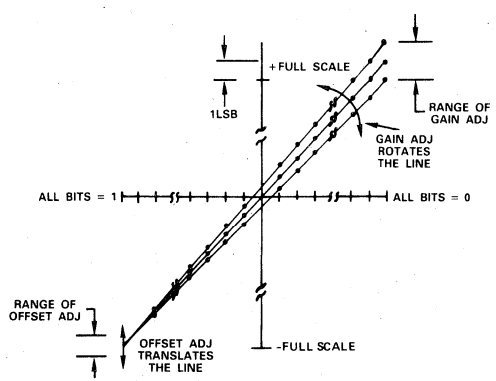


Figure 1. Relationship of OFFSET and GAIN Adjustments for a BIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)

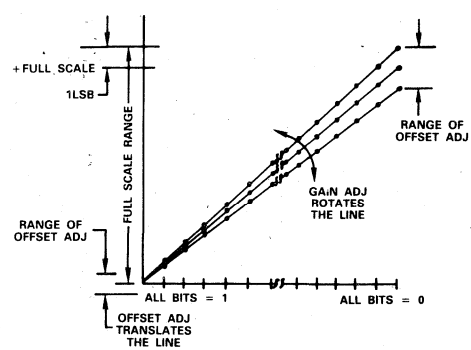
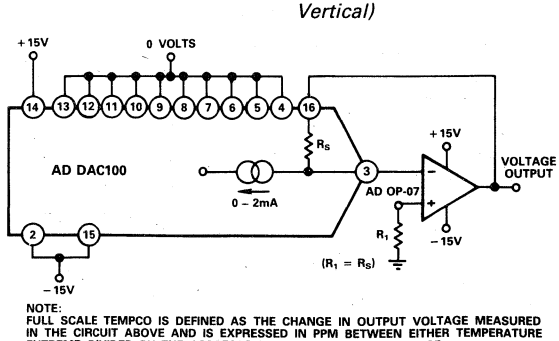


Figure 2. Relationship of OFFSET and GAIN Adjustments for a UNIPOLAR D/A Converter (Input, Horizontal; Output, Vertical)



NOTE:
FULL SCALE TEMPCO IS DEFINED AS THE CHANGE IN OUTPUT VOLTAGE MEASURED IN THE CIRCUIT ABOVE AND IS EXPRESSED IN PPM BETWEEN EITHER TEMPERATURE EXTREME DIVIDED BY THE CORRESPONDING TEMPERATURE CHANGE.

Figure 3. Full Scale Test Circuit

CONNECTING THE AD DAC100 FOR BUFFERED VOLTAGE OUTPUT

The standard current-to-voltage conversion connections using an operational amplifier are shown here with the preferred trimming techniques. If a low offset operational amplifier (AD544, AD547, AD509, AD510, AD741L) is used, excellent performance can be obtained in many situations without trimming. (A 5mV op amp offset is equivalent to ½LSB on a 10 volt scale).

The AD509 is recommended for buffered voltage-output applications which require a settling time to ±½LSB of one microsecond. The feedback capacitor is shown with the optimum value for each application; this capacitor is required to compensate for the 13 picofarad DAC output capacitance.

FIGURE 4. UNIPOLAR CONFIGURATION

This configuration will provide a unipolar 0 to +10 volt output range.

STEP I . . . ZERO ADJUST

Turn all bits HIGH and adjust op amp trimmer, R4, until the output reads 0.000 volts (1LSB = 9.76mV).

STEP II . . . GAIN ADJUST

Turn all bits LOW and adjust 200Ω gain trimmer, R2, until the output is 9.990 volts (Full scale is adjusted to 1LSB less than nominal full scale of 10.000 volts.)

FIGURE 5. BIPOLAR CONFIGURATION

This configuration will provide a bipolar output voltage from −5.000 to +4.990 volts, with positive full scale occurring with all bits LOW (all 0's).

STEP I . . . OFFSET ADJUST

Turn all bits HIGH, adjust 500Ω trimmer, R3, to give a reading of −5.000 volts.

STEP II . . . GAIN ADJUST

Turn MSB LOW, turn all other bits HIGH. Adjust 200Ω gain trimmer to give 0.000 output volts.

Please note that it is not necessary to trim the op amp to obtain full accuracy at room temperature. In most bipolar situations, the op amp trimmer is unnecessary unless the untrimmed offset drift of the op amp is excessive. If a FET-input op amp is used, R1 can generally be omitted.

9

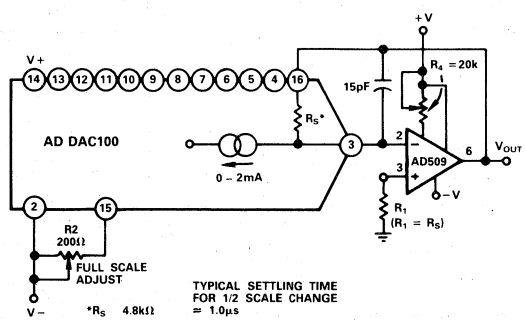


Figure 4. Unipolar Voltage Output Circuit

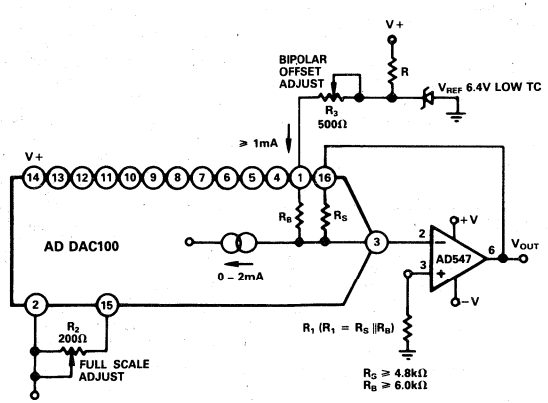


Figure 5. ±5V Bipolar Voltage Output Circuit

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy.

The AD DAC100 is designed to be operated with the output voltage near zero. Output voltage swings can affect linearity by causing improper switching of bits. Potentially damaging large voltage swings can be avoided by clamping the output within ±0.7 volts using a pair of back to back silicon diodes between the output and ground as shown in Figure 6.

INTERFACING WITH CMOS LOGIC

CMOS inputs may be used directly as long as the logic input voltages do not exceed 6.5V or V+ (the lesser of the two). If a +6 (±5%)V input supply is used, no interfacing components are required.

For CMOS levels between 6.5V and +15V, a method of interfacing is shown in Figure 7. The high level inputs are stepped down to TTL level inputs not exceeding 5V by using CMOS Hex buffer/converters. These buffer/converters not only provide level shifting but allow input coding flexibility since they are available as inverting (CD4049A) or noninverting (CD4050A) devices. The user can then choose betwen negative true and positive true binary coding.

REDUCED RESOLUTION APPLICATIONS

For applications requiring less than 10 bits of resolution, all unused logic inputs must be tied high for proper operation (see Figure 8).

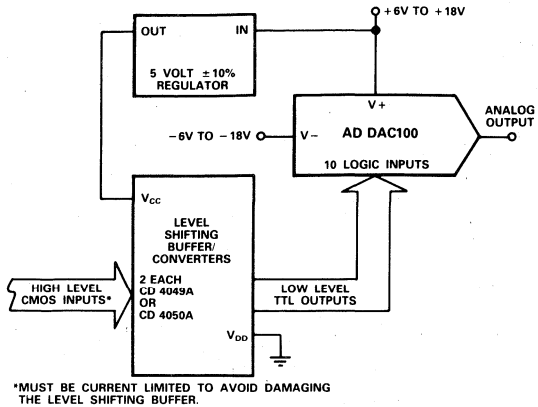


Figure 7. CMOS to AD DAC100 Interface

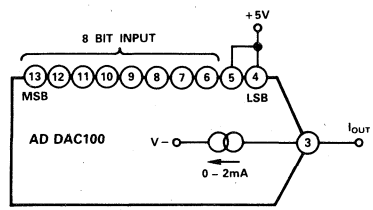


Figure 8. Reduced Resolution Application

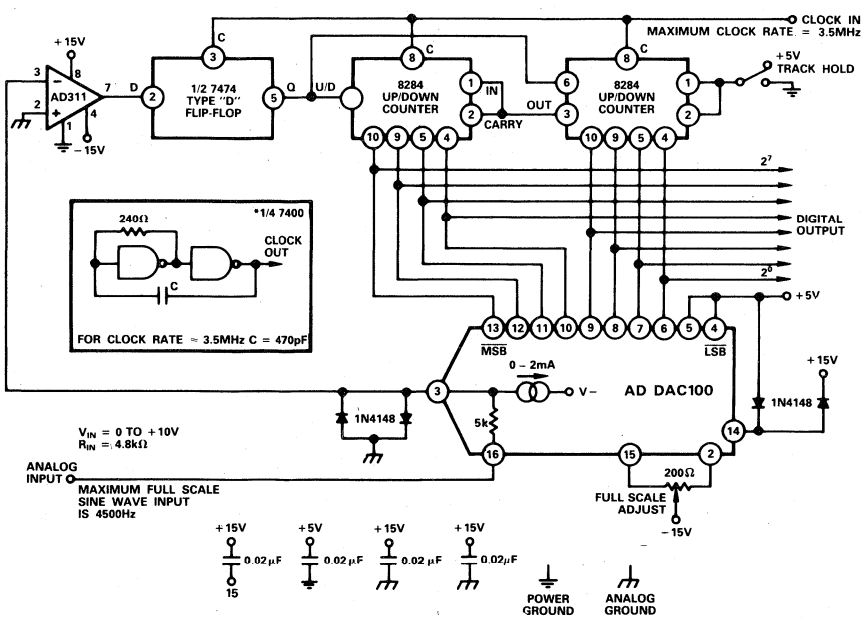


Figure 6. Tracking (Servo Type) A/D Converter

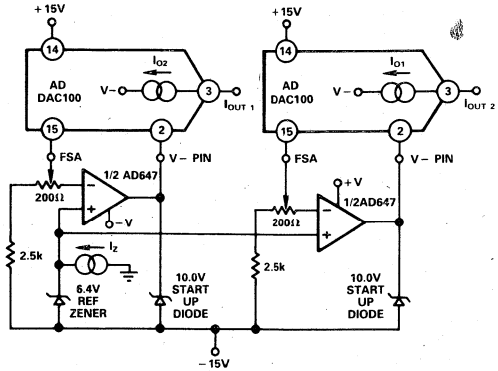


Figure 9. External Reference Connection

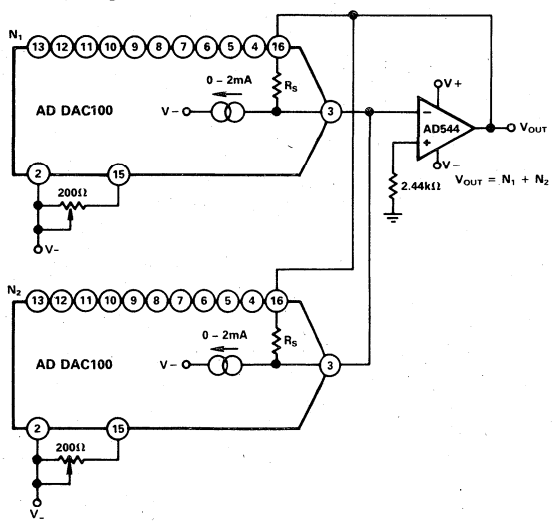


Figure 10. Analog Sum of Two Digital Numbers

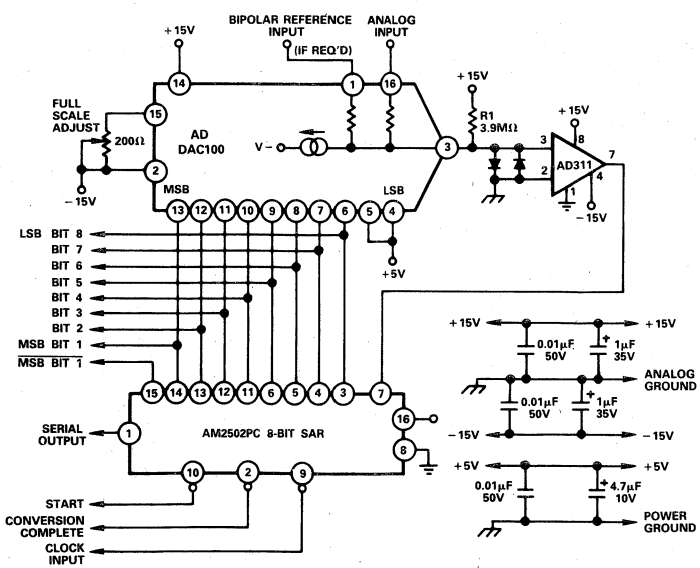


Figure 11. 8-Bit Successive Approximation A/D Converter

Hybrid Video Low Glitch D/A Converter

HDD Series

FEATURES

- Ultra Fast 10ns Settling Time to 0.2% (HDD-0810)
  15ns Settling Time to 0.1% (HDD-1015)
- Internal Monolithic Reference
- Low 200pV-sec Glitch Energy
- Single -5.2V Power Supply
- Available Screened to MIL-STD-883
- Designed for General Output Compatibility with EIA Standards RS-170 and RS-343, including 10% Brightness
- Complete Composite Inputs (HDD-0810C, HDD-1015C)

APPLICATIONS

- Raster Scan and Vector Graphic Displays
- TV Video Reconstruction
- Ultra Fast Current or Voltage Output DAC for Use in Analytical Instrumentation
- Digital VCOs

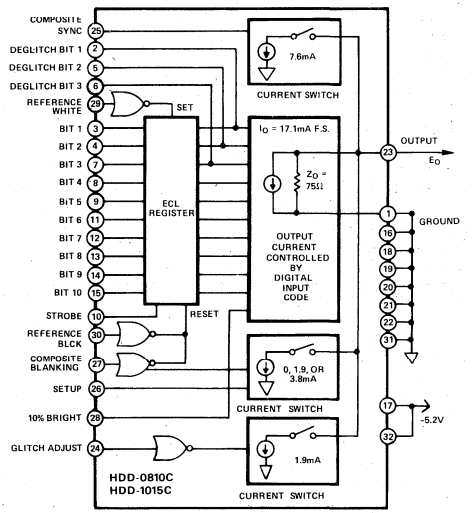
GENERAL DESCRIPTION

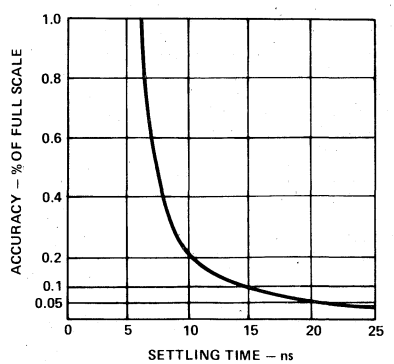
The HDD-0810 and HDD-1015 combine state-of-the-art technology with the latest active laser trimming techniques to achieve the world's fastest 8- and 10-bit voltage output digital-to-analog converters of their type.

Containing input registers and an ultra stable monolithic internal reference, the HDD-0810 8-bit D/A converter settles to within 0.2% in 10ns, while the 10-bit version HDD-1015 settles to within 0.1% in only 15ns. They are compatible with standard ECL logic levels. The 75Ω output impedance allows them to drive 75Ω cables or filters directly, without costly external output drivers. This feature assures that a full one volt is available at the load, since the D/A output is a minimum of 27mA (HDD-1015). Additionally, these D/As are monotonic over the full operating temperature range of -25°C to +85°C (metal case versions), or 0 to +70°C for the commercial style glass-ceramic package, and require only a single -5.2V supply for operation.

The HDD-0810C and HDD-1015C combine all of the above features with full composite input capability, which allows operation directly with raster scan/output video display systems. These controls include Composite Sync, Blanking, Setup and a 10% Brightness input which gives the user digital control of the picture's intensity. Further, the HDD Series D/A converters contain provisions for external adjustments to optimize differential phase and gain, critical considerations in composite color video applications.

HDD SERIES FUNCTIONAL BLOCK DIAGRAM





TIME IS MEASURED FROM 50% TRANSITION POINT OF THE STROBE WITH INPUT DATA LINES DESKEWED AND 75Ω LOAD. VOLTAGE OUTPUT. INHERENT DELAY OF INTERNAL REGISTER (3ns) HAS BEEN DISREGARDED.

HDD Series D/A Converters Accuracy vs. Settling Time

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 75Ω output load unless otherwise noted)

MODEL	UNITS	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
RESOLUTION FS = FULL SCALE	Bits	8	8	10	10
LSB WEIGHT (Current)	μA	106	67	27	17
LSB WEIGHT (Voltage)	mV	4	2.5	1	0.625
ACCURACY[1]	±% of FS	0.1		0.05	
	±% of GS		0.1		0.05
Linearity	±μA	26.5	17	13	8.5
Monotonicity		Guaranteed	*	*	*
Zero Offset (Initial)	mV	-1.4	*	*	*
TEMPERATURE COEFFICIENTS					
Linearity	ppm/°C	5	*	*	*
Zero Offset	ppm/°C	1	*	*	*
Gain	ppm/°C	80	*	*	*
STROBE INPUT					
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
(Positive Logic) "0" =	V	-1.7	*	*	*
Logic Loading		50pF and 5kΩ to -5.2V	*	*	*
Set-Up Time (Data)	ns	2.5 min	*	*	*
Hold Time (Data)	ns	1.5 min	*	*	*
Propagation Delay	ns	3	*	*	*
REFERENCE BLACK AND REFERENCE WHITE INPUTS[2]		See Note 2	*	*	*
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
"0" =	V	-1.7	*	*	*
Logic Loading		50pF and 5kΩ to -5.2V	5pF and 50kΩ *	50pF and 5kΩ *	5pF and 50kΩ *
DATA INPUTS					
Logic Compatibility		ECL	*	*	*
Logic Voltage Levels "1" =	V	-0.9	*	*	*
(Positive Logic) "0" =	V	-1.7	*	*	*
Logic Loading (Each Bit)		5pF and 50kΩ to -5.2V	*	*	*
Coding (See Table)		Complementary Binary (CBN)	*	*	*
COMPOSITE SYNC INPUT					
Logic Compatibility		N/A	ECL	N/A	ECL
Logic Voltage Levels "1" =	V	N/A	-0.9	N/A	-0.9
"0" =	V	N/A	-1.7	N/A	-1.7
Logic Loading for Logic "1"		N/A	5pF, +7.6mA	N/A	5pF, +7.6mA
Logic "0"		N/A	5pF, -50μA	N/A	5pF, -50μA
COMPOSITE BLANKING AND 10% BRIGHT INPUTS					
Logic Compatibility		N/A	ECL	N/A	ECL
Logic Voltage Levels "1"	V	N/A	-0.9	N/A	-0.9
"0"	V	N/A	-1.7	N/A	-1.7
Logic Loading		N/A	5pF and 50kΩ to -5.2V	N/A	5pF and 50kΩ to -5.2V
SETUP CONTROL					
Ground	mV	0 (0 IRE Units)	*	*	*
Open	mV	71 (10 IRE Units)	*	*	*
-5.2V	mV	142 (20 IRE Units)	*	*	*
OUTPUT[3]					
Current	mA	0 to -27.2	0 to -17	0 to -27.3	0 to -17.05
Voltage[4]	V (±1%)	0 to -1.020	0 to -0.6375	0 to -1.023	0 to -0.639375
Compliance	V	+1.1 to -1.1	*	*	*
Internal Impedance	Ω (±5%)	75	*	*	*
OUTPUT – COMPOSITE SYNC					
Current	mA (±5%)	N/A	0 or -7.6	N/A	0 or -7.6
Voltage	mV (±5%)	N/A	0 or -286	N/A	0 or -286
OUTPUT – 10% BRIGHT					
Current	mA (±5%)	N/A	0 or -1.9	N/A	0 or -1.9
Voltage	mV (±5%)	N/A	0 or -71	N/A	0 or -7.1
OUTPUT – COMPOSITE BLANKING[5]					
Current	mA (±1%)	N/A	0, -17.0, -18.9, or -20.8	N/A	0, -17.05, -18.95, or -20.85
Voltage	mV (±1%)	N/A	0, -637.5, -708.75 or -780	N/A	0, -639.4, -710.6, or -781.9

MODEL	UNITS	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
SPEED PERFORMANCE – FULL SCALE OR GRAY SCALE OUTPUT					
Settling Time (Voltage)[6]	ns (to % FS)	10 (0.2)		15 (0.1)	
	or (to % GS)		10 (0.2)		15 (0.1)
Slew Rate	V/μs	200	*	*	*
Update Rate[7]	MHz	100	100	67	67
Rise Time	ns	4	*	*	*
Glitch Energy[8]	pV-s	200	*	*	*
SPEED PERFORMANCE – CONTROL INPUTS					
Settling Time to 10% of Final Value for:					
Composite Sync	ns	N/A	10	N/A	10
Composite Blanking	ns	N/A	10	N/A	10
Reference White	ns	N/A	10	N/A	10
Reference Black	ns	N/A	10	N/A	10
10% Bright	ns	N/A	10	N/A	10
POWER REQUIREMENTS					
-5.2V ±0.25V	mA	380	390	450	450
Power Supply Sensitivity	%/%	0.04/1	*	*	*
Reference		Monolithic, Internal	*	*	*
TEMPERATURE RANGE					
Operating, Glass Case	°C Case	0 to +70	*	*	*
Operating, Metal Case ("M")	°C Case	-25 to +85	*	*	*
Storage	°C	-55 to +125	*	*	*
MTBF[9]					
Mean Time Between Failure	hours	>300,000			
PACKAGE OPTIONS[10]		HY32A		HY32C	

NOTES

[1] Accuracy is relative to full scale (FS) for binary versions, or relative to gray scale (GS) for Composite ("C") versions, and includes linearity.

[2] Reference White on models HDD-0810, -1015 a logic "1" on Pin 30 Reference Black will produce all "0" code 0 volts output; a logic "1" on Pin 29 Reference White will produce all "1" code -1 volt output.
On models HDD-0810C, 1015C a logic "0" on Pin 30 Reference Black will produce all "1" code 0 volts output; a logic "0" on Pin 29 Reference White will produce all "0" code -1 volt output.

[3] The output is shown for full scale (FS) for binary versions, and for full gray scale (GS) for Composite ("C") versions.

[4] The difference between the full-scale output of 637.5mV and 643mV shown elsewhere herein is due to the fact that we selected an LSB value of 2.5mV for ease of calibration. These differences are well within the output and EIA standard RS-170 tolerances.

[5] The three currents and voltages correspond to the three set-up levels of 0, 10, and 20 IRE units as externally selected.

[6] Worst case settling time includes FS and most significant bit (MSB) transitions. The inherent 3ns proposition delay through the input registers (50% point of Strobe to 50% point of register output) has been disregarded. Settling time to a percentage of FS is given for straight versions, and settling time to a percentage of maximum gray scale (GS) is given for composite video output ("C") versions.

[7] The update rates shown are limited by a full scale settling time that is useable for the number of bits of resolution. Both DACs may be operated up to 125MHz with settling time degradation. This is the limit of the logic switching speed.

[8] Reducible to less than 100pV-s with appropriate deskewing of digital inputs. See Applications Section.

[9] Calculated for HDD-1015CMB using MIL Handbook 217. Ground: Fixed Temperature Case = 60°C.

[10] See Section 19 for package outline information.

*Specifications same as for HDD-0810.

Specifications subject to change without notice.

ORDERING NOTE

1. To order devices with hermetically sealed metal cases, add "M" suffix to part number.

   Example: HDD-0810CMB

PIN DESIGNATIONS

PIN	FUNCTION
1	GROUND
2	DEGLITCH BIT 1
3	BIT 1 (MSB)
4	BIT 2
5	DEGLITCH BIT 2
6	DEGLITCH BIT 3
7	BIT 3
8	BIT 4
9	BIT 5
10	STROBE
11	BIT 6
12	BIT 7
13	BIT 8
14	BIT 9
15	BIT 10 (LSB)
16	GROUND
17	-5.2V
18	GROUND
19	GROUND
20	GROUND
21	GROUND
22	GROUND
23	OUTPUT
24	GLITCH ADJUST
25	COMPOSITE SYNC
26	SETUP
27	COMPOSITE BLANKING
28	10% BRIGHT
29	REFERENCE WHITE
30	REFERENCE BLACK
31	GROUND
32	-5.2V

ON THE HDD-0810 AND HDD-0810C, PINS 14 AND 15 ARE NOT USED, AND PIN 13 IS THE LSB. ON THE HDD-0810 AND HDD-1015, PINS 25, 27, AND 28 ARE NOT USED. ALL GROUND PINS (1, 16, 18-22, 31) ARE CONNECTED INTERNALLY.

APPLICATIONS INFORMATION

HIGH-SPEED LOW-GLITCH OPERATION SUGGESTIONS

The HDD Series D/As offer the highest available speed. However, with this speed performance, certain precautions and operation conditions should be considered.

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor mounted between the -5.2V supply line and ground near the D/A.
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 17 and 32 to ground (see Figure 1).
4. The threshold of the internal current switches can be optimized for low glitch energy by the addition of an external potentiometer connected to Pin 24 of the D/A (see Figure 1). This potentiometer is adjusted for minimum glitch energy as shown in Photo 2.

   If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 1 (C1-3). They are adjusted in conjunction with the glitch adjust pot for minimum glitch energy as shown in Photo 2.

   In composite television applications, C1-3 are adjusted for best differential phase performance, and the glitch adjust is adjusted for best differential gain performance. These may tend to interact, so going back and forth between adjustments may be required.
5. Standard 32-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/As should be soldered directly into the printed circuit board without sockets.

GAIN ADJUSTMENT

The HDD Series D/As are actively laser-trimmed to provide a voltage into exactly 75Ω which is an even binary multiple; i.e., the HDD-0810 has an LSB of 4mV and the HDD-1015 has an LSB of 1mV. This makes the full-scale output slightly greater than one volt. If an output of exactly one volt is required—such as for TV reconstruction—a 2k potentiometer may be placed across the output of the D/A for gain adjustment. For a one volt output, the adjusted value of this pot will be about 1500Ω (see Figures 1 and 5).

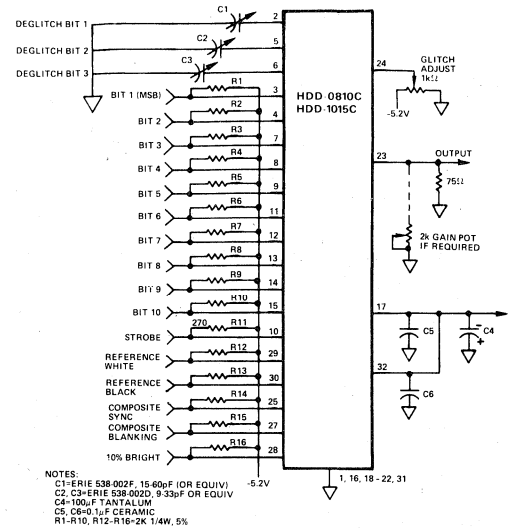


Figure 1. HDD-0810, HDD-1015C Typical Hook-Up Circuit

ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 2). The duration of the HDD Series D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch. The minimum acquisition time of the HTS-0025 for 0.1% accuracy is 30ns. This implies that the circuit of Figure 2 can be operated up to 22MHz and still maintain 10-bit accuracy. For 0.2% accuracy, the acquisition time for the T&H can be reduced to 25ns, allowing the circuit to operate to 25MHz. This discussion assumes that the D/A will be required to slew full scale (one volt) between adjacent samples. In practice, the sample-to-sample variation is less than full scale depending on the amount of oversampling. In a practical situation, therefore, 10-bit accuracy should be achievable at 25MHz update rates.

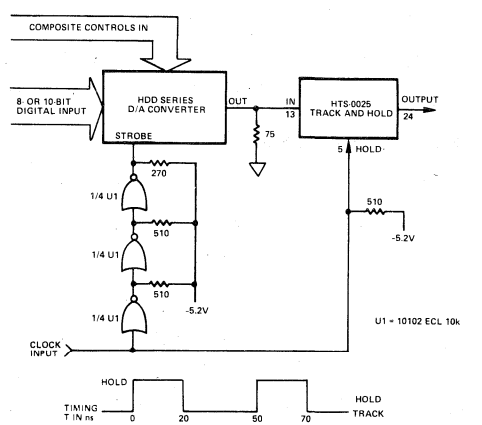


Figure 2. HTS-0025 Track and Hold Used as a Deglitcher (Update ≈ 20MHz)

CHARACTERISTICS OF HDD-1015C [0810C] VIDEO DACS

COMPOSITE VIDEO SIGNAL
1024 [256] gray levels plus blanking and sync levels

STEP SIZE
0.625mV [2.5mV]

GRAY SCALE RANGE
0.643V Peak to Peak

SETUP CONTROL
User programmable in three levels

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	71	10
3. Input @ -5.2V	142	20

REFERENCE WHITE LEVEL
0V Absolute
100 IRE Units (+0.714V relative to blanking level with standard setup; +0.643V relative to Reference Black)

DIGITAL INPUT FOR WHITE LEVEL
All ones (1111111111)

REFERENCE WHITE/BLACK CONTROLS[1]
Overrides Video Input Word
A logic 0 on Pin 30 (reference Black) will drive the output to reference black level of -643mV.
A logic 0 on Pin 29 (Reference White) will drive the output to reference white level of 0 volts absolute.

REFERENCE BLACK LEVEL
-0.643V Absolute; +71mV (10 IRE Units)
Relative to blanking level with standard setup.

DIGITAL INPUT FOR REFERENCE BLACK
All zeroes (0000000000)

COMPOSITE BLANKING LEVEL
-0.714V Absolute, (0 IRE Units) with standard setup.

COMPOSITE BLANKING INPUT - PIN 27[1]
Logic 0 on Pin 27 resets input register to 0000000000, and causes output voltage to go negative by the amount of setup voltage with respect to the all "0" output voltage.

COMPOSITE SYNC LEVEL
-1.0V Absolute with standard setup.
-0.286V (-40 IRE Units) relative to blanking level (Back Porch).

COMPOSITE SYNC INPUT - PIN 25
Logic 0 resets input register to 0000000000, and the output voltage goes negative by 0.286V.

10% BRIGHT - PIN 28
Logic "0" causes output voltage to go positive by 71mV.

STROBE - PIN 10
Logic "0" to Logic "1" transition clocks input register.

DEFINITION OF VIDEO TERMS

BLANKING LEVEL
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch of Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green, and Blue to produce color pictures within the usual spectrum. In RGB monitors, three HDD "C" Series DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)
The position of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
The discrete levels of video signal between Reference Black and Reference White levels. A 10-bit DAC contains 1,024 different levels, while an 8-bit DAC contains 256.

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and display images. This method is used in commercial television in the USA.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the Reference Black level and the blanking level. This should not be confused with setup as used with digital logic.

SYNC LEVEL
The peak level of the composite SYNC signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

NOTE
[1] Reference White (Pin 29) should not be activated at the same time as composite blanking (Pin 27) or Reference Black (Pin 30).

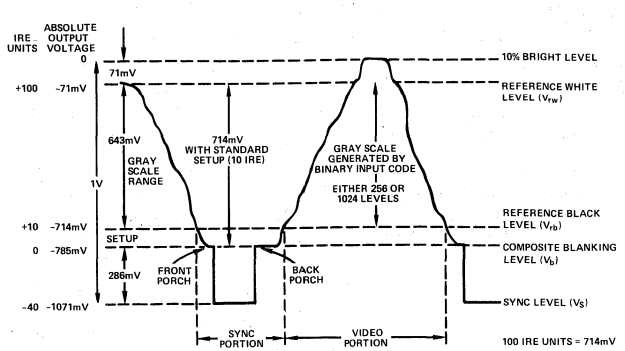


Figure 3. HDD-0810C, HDD-1015C Output Waveforms

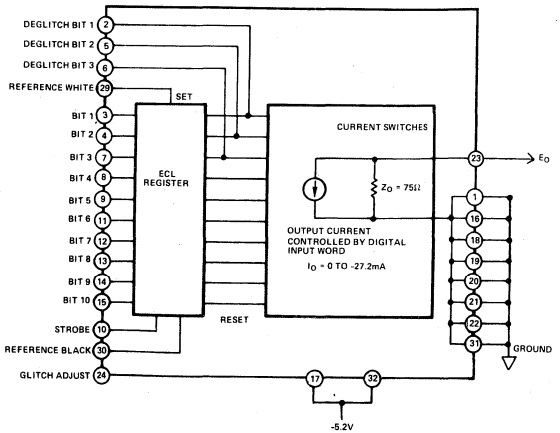


Figure 4. HDD-0810; HDD-1015 Block Diagram

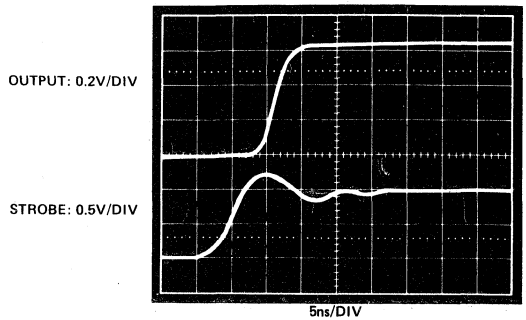


Photo 1. Full Scale Rise Time vs. Strobe

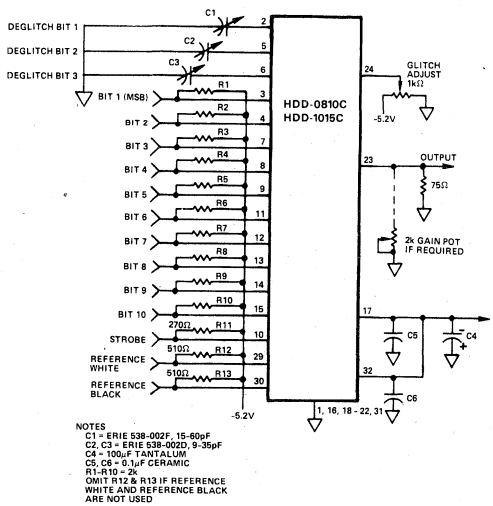


Figure 5. HDD-0810, HDD-1015 Typical Hook-Up Circuit

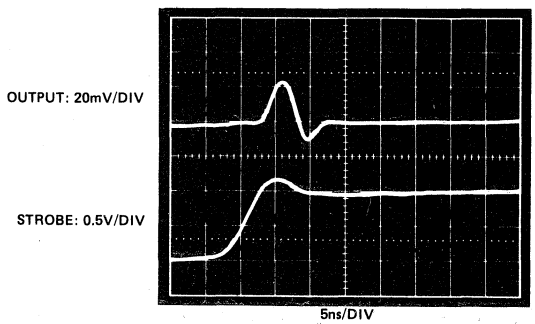


Photo 2. Midscale Glitch

HDD-0810C, HDD-1015C Output Waveform

ANALOG OUTPUT WITH 75Ω LOAD

Digital Input	HDD-0810	HDD-0810C	HDD-1015	HDD-1015C
111 . . . 111	0	0	0	0
111 . . . 110	-4mV	-2.5mV	-1mV	-0.625mV
110 . . . 000	-252mV	-157.5mV	-255mV	-159.375mV
101 . . . 111	-256mV	-160mV	-256mV	-160mV
100 . . . 111	-508mV	-317.5mV	-511mV	-319.375mV
011 . . . 111	-512mV	-320mV	-512mV	-320mV
010 . . . 000	-764mV	-477.5mV	-767mV	-479.375mV
001 . . . 111	-768mV	-480mV	-768mV	-480mV
000 . . . 001	-1016mV	-635mV	-1022mV	-638.75mV
000 . . . 000	-1020mV	-637.5mV	-1023mV	-639.375mV

Coding Table

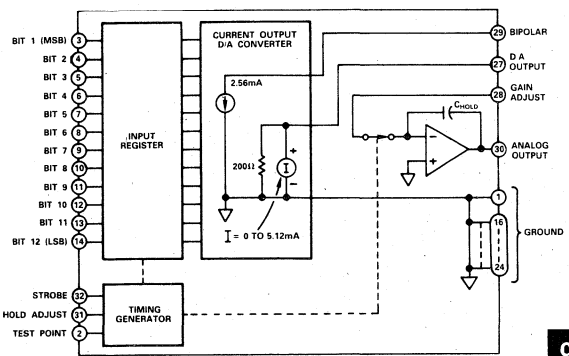
12-Bit Deglitched Voltage Out D/A Converter

HDD-1206

FEATURES
Registers, D/A, Amplifier in Single Hybrid
Deglitched Voltage Output
6MHz Update Rate

APPLICATIONS
Vector Scan Displays
Analytical Instrumentation
Digital VCOs
Military Systems

HDD-1206 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The Analog Devices HDD-1206 D/A converter combines innovative design techniques with remarkable hybrid construction to achieve deglitched voltage outputs at digital update rates as high as 6MHz.

Despite its small size and low power, the HDD-1206 provides the user with a complete solution to demanding applications which require the conversion of high-speed digital inputs into deglitched analog output voltages.

The unit is housed in an industry standard 32-pin hybrid and contains all the necessary circuit components to provide analog outputs at high update rates without the need for designing external circuits. Input registers, current-output D/A, deglitching circuits, and an output amplifier are all included inside the HDD-1206.

With the deglitching problem solved in a single package, the user of the HDD-1206 is able to incorporate the solution into his system with a minimum of design effort. User involvement is limited to the simple task of establishing the "hold" time for an optimum value by selecting the correct resistor value.

After that step is accomplished, the addition of a low-pass filter at the output of the D/A assures a "clean" voltage representation of the 12 bits of digital information applied to the inputs at video update rates.

The HDD-1206 is available in 32-pin dual in-line ceramic packages.

PIN DESIGNATIONS
HDD-1206

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	17	GROUND
2	TEST POINT	18	GROUND
3	BIT 1 (MSB)	19	GROUND
4	BIT 2	20	GROUND
5	BIT 3	21	GROUND
6	BIT 4	22	GROUND
7	BIT 5	23	GROUND
8	BIT 6	24	GROUND
9	BIT 7	25	+15V
10	BIT 8	26	−15V
11	BIT 9	27	D/A OUTPUT
12	BIT 10	28	GAIN ADJUST
13	BIT 11	29	BIPOLAR
14	BIT 12 (LSB)	30	OUTPUT
15	+5V	31	HOLD ADJUST
16	GROUND	32	STROBE

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 1kΩ output load unless otherwise noted)

Model	HDD-1206JW			HDD-1206SM			
Parameter	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
RESOLUTION		12			*		Bits
LSB WEIGHT (FS = 10.24V)		2.5			*		mV
ACCURACY (Linearity)			±0.0125			*	% FS
Differential Nonlinearity		±1/2			*		LSB
Zero Offset[1] (Initial)		±35	±50		*	*	mV
Monotonicity		Guaranteed			*		
TEMPERATURE COEFFICIENTS							
Linearity		5			*		ppm/°C
Gain		40			*		ppm/°C
Offset		100			*		ppm/°C
DYNAMIC CHARACTERISTICS[2]							
Settling Time to ½LSB							
±5.12V FS Change		2			*		µs
1LSB Change		60			*		ns
Internal Current D/A		50			*		ns
Slew Rate		25			*		V/µs
Gain		Adjustable			*		V/V
DIGITAL DATA INPUTS							
Logic Compatibility		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load (each bit)		One Standard			*		TTL Load
Coding (see Table on last page)		Complementary Binary (CBN); Complementary Offset Binary (COB)			*		
STROBE INPUT							
Logic Compatiblity		TTL			*		
Logic Levels							
"1"	+2.4		+5	*		*	V
"0"	0		+0.4	*		*	V
Load		One Standard			*		TTL Load
Risetime/Falltime (10%–90%)			15			*	ns
Width	50		.65/word rate	*		*	ns
Frequency (see chart below)			6			*	MHz
OUTPUT (see Coding Table)							
R_{FB} = 1,000Ω							
Bipolar Voltage[3]		±2.56			*		V
Unipolar Voltage		0 to −5.12			*		V
Current	8			*			mA
R_{FB} = 2,000Ω							
Bipolar Voltage		±5.12			*		V
Current	8			*			mA
Residual Glitch		50	100		*	*	mV
Output Impedance		0.1	1		*	*	Ω
Capacitive Loading		1,000			*		pF
POWER REQUIREMENTS							
+15V ± 3% Current		55	60		*	*	mA
−15V ± 3% Current		30	35		*	*	mA
+5V ± 5% Current		85	95		*	*	mA
Power Supply Rejection Ratio		2			*		mV/V
Power Dissipation		1.7	1.9		*	*	W
TEMPERATURE RANGE							
Operating[4]	0		+70	−55		+125	°C
Storage	−55		+125	*		*	°C
THERMAL RESISTANCE[5]							
Junction to Air, θja (free air)		32			*		°C/W
Junction to Case, θjc		13			*		°C/W
MTBF[6]							
Mean Time Between Failures					3.015×10^5		Hours
PACKAGE OPTION[7]		HY32A			HY32C		

NOTES
[1]Adjustable to zero.
[2]All dynamic characteristics are based on FS = ±5.12V; R_{FB} = 2,000Ω.
[3]With R_{FB} = 1k, analog output voltages are half those shown in Table on last page.
[4]Case Temperature.
[5]Maximum junction temperature is 150°C.
[6]Calculated per MIL-HDBK 217, Ground; Fixed; Case Temperature = 60°C.
[7]See Section 19 for package outline information.
*Specifications same as HDD-1206JW.
Specifications subject to change without notice.

Max Output Change (LSBs)	for	Update Rate (MHz)
2		6
4		5
6		4
15		3

THEORY OF OPERATION

The equivalent circuit for the for the HDD-1206 D/A converter is shown in functional block diagram.

The unit consists of input registers, fast-settling current output D/A, output amplifier, timing generator, and associated circuits.

The purpose of the input register circuits is to de-skew the input bits and assure their simultaneous arrival at the input of the current D/A. This is critical because time skew on the input data bits is a major contributor to discontinuities, or "glitches," in the analog output of a D/A.

The Timing Generator includes a Track & Hold circuit and generates the required internal pulses for operation whenever it receives a Strobe input pulse. See Figure 1, the HDD-1206 timing diagram.

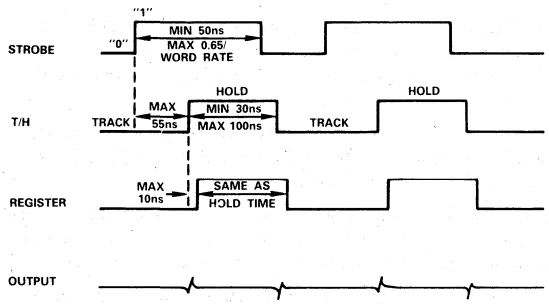


Figure 1. HDD-1206 Timing Diagram (Digital Inputs not Changing)

As shown, the Strobe pulse is a positive-going TTL pulse supplied by the user of the HDD-1206. Internal timing circuits establish the maximum 55ns delay from the leading edge of the Strobe pulse to the leading edge of the T/H (Track/Hold) pulse; and the maximum 10ns delay from the leading edge of the T/H pulse to the leading edge of the Register pulse. The data from the input registers are strobed into the current D/A at the end of this 65ns interval, so they must be valid by that time.

The user determines the width of the T/H pulse (and the Register pulse) by selecting the value of the R_{HOLD} resistor. See Figures 1 and 2. As shown, the width of the Hold pulse can vary from approximately 30ns to approximately 100ns by using resistor values from 1k to 5k, respectively.

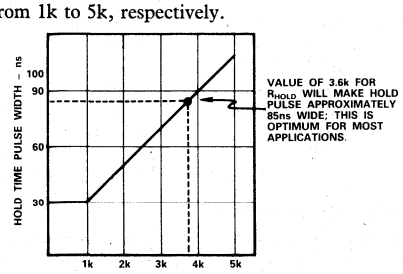


Figure 2. Hold Time vs. R_{HOLD}

For most applications, a value of 3.6kΩ and a pulse width of approximately 85ns is the optimum choice. This pulse width will "hold" the analog output of the HDD-1206 D/A until the "glitch" resulting from the most recent update has passed, without infringing on the word rate capabilities of the HDD-1206.

CURRENT-OUTPUT D/A CONVERTERS

A brief review of the salient characteristics of current D/A converters may be a useful approach to understanding the operation of the HDD-1206 unit.

Current-switching D/A converters are inherently faster than voltage-output types because of the absence of an output amplifier. This means current-switching converters have no slew rate limitation which can slow settling; nor are they subject to the overshoot and ringing problems often associated with feedback amplifiers.

Both current-switching and voltage-output converters display a discontinuity, or "glitch," in their analog outputs because of the basic characteristic of saturated logic (TTL is an example) which causes the propagation delay to be less for negative-going inputs than it is for positive-going inputs.

This difference in propagation delay manifests itself as a "worst case glitch" at the major carry point, or mid-scale, of the output range of the current converter. This is the point at which nearly equal and opposite currents are being switched within the converter.

The "glitch" at mid-scale, the switching point of the Most Significant Bit (MSB), will be halved at the ¼ and ¾ points; halved again at the ⅛ and ⅞ points, etc. The amplitude of the "glitch," therefore, is a function of signal dynamics and cannot be eliminated with filtering.

The variations in glitch amplitude caused by signal dynamics create a multitude of intermodulation (IM) products, some of which fall into the video pass-band as spurious signals, and increased noise level. These IM products are also relatively immune to elimination by filtering.

The amplitude of the glitch can be reduced by de-skewing the input bits; but no amount of de-skewing or filtering can negate the physics of saturated logic which cause the glitch to be generated initially.

The best solution, then, is to cause the glitch to remain a constant across the entire output range of the converter. The efficiencies of the circuit will be enhanced if the solution can also permit using the full drive capabilities of the current-output D/A in either unipolar or bipolar modes of operation.

The design approach used in the Analog Devices HDD-1206 D/A converter accomplishes these desired goals and provides voltage outputs at high update rates.

NOTES ON DEGLITCHING

Refer again to the equivalent circuit for the HDD-1206. The data bits are applied through the input register to the current-output D/A converter, which is capable of supplying up to 5.12mA of output current.

The output of the current D/A, in turn, is applied to the input of the output amplifier via strapping external to the HDD-1206. The Timing Generator supplies the necessary pulses and timing to apply signals to the current D/A and output amplifier after the initial glitch caused by the digital inputs has subsided.

The digital "1" (Hold) level of the T/H pulse causes the switch at the input of the amplifier to open, holding the last value of the current D/A converter. During this hold interval, the switching transients caused by updating digital inputs are masked from the amplifier, thereby avoiding HDD-1206 output discontinuities whose amplitude would be a function of signal dynamics.

Ten nanoseconds after the T/H pulse goes to the digital "1" level, the register pulse also changes state from "0" to "1".

This transition moves the output of the current D/A to the new value established by the most recent digital inputs applied to the HDD-1206.

Any change in the current D/A output has stablized by the time the T/H pulse returns to the digital "0" (Track) level. Re-establishing the track mode closes the switch at the input of the amplifier and the output of the HDD-1206 moves to the new analog value dictated by the digital input word.

As shown in Figure 1, the output of the HDD-1206 will contain switching transients associated with the T/H pulse. But these "glitches" will be constant in amplitude and duration and will occur at the update rate, since they are a function of the strobe pulse applied by the user.

These switching transients will settle out in approximately 500ns, and will have uniform amplitude over the complete analog output range of the D/A. For strobe rates of 2MHz and above, the settling interval switching from "hold" to "track", and vice versa, will produce a constant dc offset on the output. The HDD-1206 is not intended to get rid of all glitches per se; it is designed to provide a constant-amplitude glitch.

When the area under the transient curve is held constant, the frequency spectrum of the glitch is a fine line, i.e., a single-line spectrum at the sample rate frequencies, and harmonics of the sample frequency.

The HDD–1206 effectively eliminates the IM products discussed above. When it does, the signal-to-noise (S/N) ratio approaches that of an ideally-quantized signal, where the rms noise is $q/\sqrt{12}$, when frequencies above Nyquist are filtered out.

GLITCH VS. PEDESTAL

In addition to the "glitch" which is a characteristic of current D/As, the track & hold used in the HDD-1206 also contributes an anomaly to the output signal.

Refer to Figure 3. This diagram compares the "glitch" created by the HDD-1206 to the pedestal created by the internal T/H circuits.

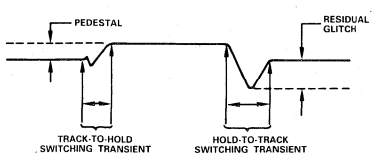


Figure 3. Pedestal/Glitch Relationship

As shown, the "glitch" is a transient signal which remains constant in width and amplitude over the entire output range, at all update rates. The pedestal, on the other hand, is an offset signal whose amplitude can vary (because of switching transient settling) as a function of hold time and word rate.

This pedestal is caused by charge transfer associated with the hold capacitor; the transfer occurs when the HDD-1206 circuits are switched from a "track" to "hold" condition. The pedestal is basically an offset error in the HDD-1206 output and can be compensated with the Offset Adjust when the unit is installed in the user's system.

Figure 3 is not drawn to scale; there is no attempt to imply the identified elements have precisely that relationship to one another. They are exaggerated for illustrative purposes.

Applications

Bipolar connections for the HDD-1206 D/A converter are shown in Figure 4. As indicated, a unipolar negative output is accomplished by connecting Bipolar Pin 29 to ground, instead of to Pins 27 and 28.

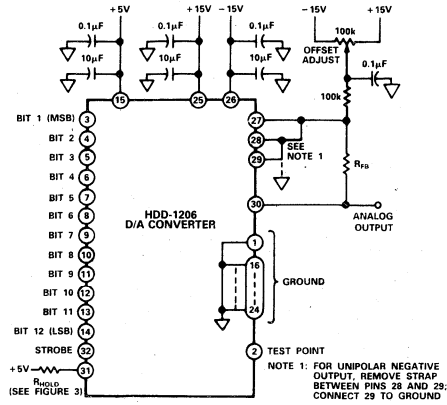


Figure 4. HDD-1206 Bipolar Connections

The output voltage swing is established by the value of feedback resistor R_{FB}. The table below indicates output levels for both unipolar and bipolar operation, with feedback resistors of either 1,000Ω or 2,000Ω.

Hold resistor R_{HOLD} connected between the +5V supply and Pin 31 sets the width of the Hold mode of the T/H pulse. Test Point Pin 2 is used for observing the pulse.

The Offset Adjust potentiometer is used to set the desired analog output of the HDD-1206 and can be used to help assure correct voltages are present when the D/A is installed in the system.

When operated in a unipolar mode with digital "0" applied to all inputs but no continuous strobe pulses applied, the Offset Adjust is set for an analog output of −5.12V less 1LSB, with 1k for the value of R_{FB}. (NOTE: At least one strobe pulse needs to be applied to latch the input data into the registers.)

If the HDD-1206 is installed in a system and the strobe pulse is applied continuously, the Offset Adjust is calibrated for the desired output value with a digital "0" applied to all input pins.

HDD-1206 ANALOG OUTPUT WITH 1kΩ LOAD

Digital Inputs	Complementary Offset Binary (COB) Bipolar Output R_{FB} = 2k	Complementary Binary (CBN) Unipolar Negative Output R_{FB} = 1k
111...111	+5.12 (+FS)	0.0000 (0)
111...110	+5.1175	− 0.00125 (+1LSB)
110...000	+2.5625 (+1/2FS)	− 1.27875
101...111	+2.56	− 1.28 (1/4)
100...000	+0.0025 (+1LSB)	− 2.55875
011...111	0.0000	− 2.56 (1/2)
010...000	−2.5575 (−1/2FS)	− 3.83875
001...111	−2.56	− 3.84 (3/4)
000...001	−5.1150	−5.1175
000...000	−5.1175 (−FS −1LSB)	−5.11875 (FS − 1LSB)

ORDERING INFORMATION

Model HDD-1206JW D/A converter is housed in a ceramic package, the model HDD-1206SM is a hermetically sealed version; outline dimensions are shown elsewhere.

Mating individual pin sockets are available from AMP. Part number 6-330808-0 are knockout end type; 6-330808-3 are open end type.

ANALOG DEVICES

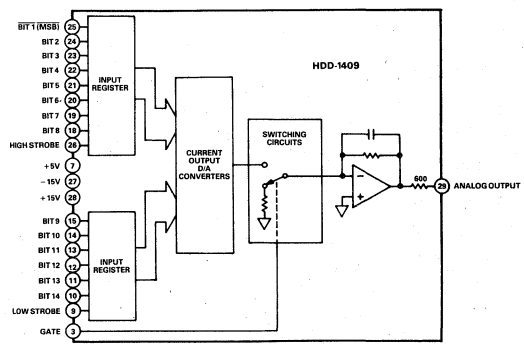
14-Bit, 200kHz Digital-to-Analog Converter

HDD-1409

FEATURES
14-Bit Resolution
200kHz Word Rates
RZ Gated Output
32-Pin DIP

APPLICATIONS
FDM/TDM Transmultiplexers
Digital Signal Processing
PCM Systems
Digital Audio

HDD-1409 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

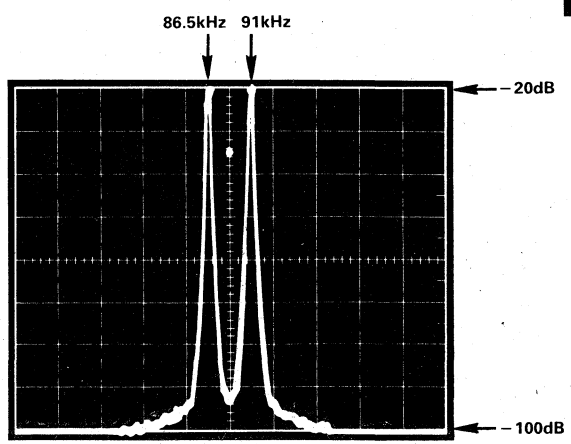
The HDD-1409KM D/A converter is a voltage-output, 32-pin hybrid digital-to-analog converter complete with input registers, current-output D/A, switching circuits, and output amplifier. The unit is capable of converting 14-bit digital inputs into gated analog output voltages at update rates from dc through 200kHz.

Monolithic ICs and hybrid microelectronic packaging have been combined in a grounded metal case hybrid which provides cost, space, and power savings for the system designer. The HDD-1409 is a complete solution for converting high-resolution digital data into "clean" analog voltages and accomplishes it with maximum power dissipation of only 600 milliwatts.

The HDD-1409 D/A has been characterized with a companion A/D converter, the HAS-1409KM, to emphasize the superior ac performance which makes the A/D – D/A combination especially attractive for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. But the design concepts and versatility which are incorporated into it also make the HDD-1409 useful in Pulse Code Modulation (PCM) and other digital signal processing applications.

The analog output voltage range is ±5V; output impedance is 600 ohms, ideal for filter matching. The D/A output operates in a return-to-zero (RZ) mode, which provides deglitching and allows selecting the optimum duty cycle for FDM/TDM and PCM applications.

Small size, low power, and multiple functions in a single package make the HDD-1409 D/A converter attractive for a wide range of data processing uses.



10dB/div Vertical; 5kHz/div Horizontal
Spectrum analyzer shows extremely low intermodulation (IM) products of back-to-back HAS-1409 A/D and HDD-1408 D/A
(See Page 9–308 for details)

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HDD-1409KM
RESOLUTION (FS = Full Scale)	Bits	14
LSB WEIGHT (FS = 10V; no load)	µV	610
ACCURACY (Linearity)	%FS	0.006
Differential Nonlinearity	LSB	1/2
Zero Offset (Initial)	mV	2
Monotonicity		Guaranteed
Gain Accuracy (−3dB)	dB	±0.01
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	10
Gain	ppm/°C	20
Offset	ppm/°C	10
DYNAMIC CHARACTERISTICS[1]		
Settling Time to 1/2LSB		
±5V FS Change	µs	5
1LSB Change	µs	1
Slew Rate	V/µs	5
Update Rate	kHz, max	200
Harmonics[2]	dB	−100
Intermodulation Products[2]	dB	−100
Noise Power Ratio (NPR)[3]	dB	68
Idle Noise/kHz[4]	dB	−104
Frequency Response[5]	dB	±0.2
DIGITAL DATA INPUTS		
Logic Compatability		TTL; CMOS
Logic Levels		
"0"	V	0 to +2.0
"1"	V	+3 to +5
Loading		
Each Bit	CMOS Load	5
STROBE (HIGH/LOW)	CMOS Load	5
GATE	TTL	1 Standard
Coding		Two's Complement (2SC)
		Offset Binary (OBN)
OUTPUT[6]		
Bipolar Voltage (No Load)	V	±5
Current	mA	4.2
Output Impedance	Ω (max %)	600 (±2)
Residual Glitch		(See Note 7)
POWER REQUIREMENTS		
+15V ±5%	mA	8
−15V ±5%	mA	20
+5V ±5%	mA	20
Power Supply Rejection Ratio	mV/V	1
Power Dissipation	W, max	0.6
TEMPERATURE RANGE[8]		
Operating	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[9]		
Junction to Air, θja		
(Free Air)	°C/W	38
Junction to Case, θjc	°C/W	18
MEAN TIME BETWEEN FAILURES[10] (MTBF)	Hours	4×10^6
PACKAGE OPTION[11]		HY32C

NOTES
[1]AC performance characteristics are based on back-to-back performance with HAS-1409 D/A converter. All signals are referenced to rms value of full-scale sinewave.
[2]Harmonics and intermodulation products measured at 112kHz encode rate, with input frequencies of 86.5kHz and 91kHz at −21dB (see Figure 4).
[3]60kHz to 108kHz white noise bandwidth with slot frequency of 70kHz; and encode rate of 112kHz (see Figure 5).
[4]Idle noise measured at 112kHz encode rate, with input frequency of 84kHz at −41dB (see Figure 6).
[5]Indicates flatness of response over frequency range of 60kHz to 108kHz.
[6]Output is 25% duty cycle high; Return-to-Zero (RZ) between samples.
[7]Not deglitched; designed for gated operation.
[8]Case Temperature.
[9]Maximum junction temperature = 150°C
[10]Calculated per MIL-HDBK 217; Ground; Benign; Case Temperature = 60°C.
[11]See Section 19 for package outline information.

Specifications subject to change without notice.

HDD-1409 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	SIGNAL	17	DIGITAL GROUND
2	$\overline{\text{SIGNAL}}$	18	BIT 8
3	GATE	19	BIT 7
4	DIGITAL GROUND	20	BIT 6
5	ANALOG GROUND	21	BIT 5
6	N/C	22	BIT 4
7	+5V	23	BIT 3
8	DIGITAL GROUND	24	BIT 2
9	LOW STROBE	25	$\overline{\text{BIT 1 (MSB)}}$
10	BIT 14 (LSB)	26	HIGH STROBE
11	BIT 13	27	−15V
12	BIT 12	28	+15V
13	BIT 11	29	ANALOG OUTPUT
14	BIT 10	30	ANALOG GROUND
15	BIT 9	31	ANALOG GROUND
16	DIGITAL GROUND	32	ANALOG GROUND

NOTES:
WHEN USING WITH HAS-1409 A/D, CONNECT $\overline{\text{BIT 1 (MSB)}}$ OF A/D (PIN 22) to $\overline{\text{BIT 1 (MSB)}}$ OF HDD-1409 D/A (PIN 25).

TO USE HDD-1409 D/A AS STAND-ALONE DEVICE WITH OFFSET BINARY INPUT, APPLY BIT 1 DIGITAL INPUT SIGNAL TO SIGNAL (PIN 1) AND CONNECT $\overline{\text{SIGNAL}}$ (PIN 2) TO $\overline{\text{BIT 1 (MSB)}}$ (PIN 25).

TO LOAD 14-BIT DATA FULLY PARALLEL, CONNECT HIGH STROBE (PIN 26) AND LOW STROBE (PIN 9) TOGETHER EXTERNALLY.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

THEORY OF OPERATION

Refer to the block diagram of the HDD-1409 D/A converter.

When the HDD-1409 D/A converter is operated with its companion HAS-1409 A/D converter, the 3-state digital logic inputs supplied by the HAS-1409 are applied to internal input registers.

For full 14-bit parallel operation, HIGH STROBE and LOW STROBE are operated simultaneously from an external STROBE signal and cause the outputs of the registers to be applied to the internal current output D/A converter.

The output of the converter, in turn, is applied to the output amplifier through switching circuits controlled by an external GATE signal. The timing of this GATE signal establishes the percentage of duty cycle during which the analog output will be at the voltage level indicative of the value of the digital inputs. During the time the GATE signal is at a digital "0" level, the voltage output of the HDD-1409 will be at ground.

The glitch from the internal D/A converter subsides during that period of time the analog output is connected to ground and never appears as a discontinuity in its voltage level. In effect, this technique accomplishes "deglitching" of the HDD-1409 D/A converter output by gating the output to be available only after internal settling times have been completed.

APPLICATIONS/TESTING

The testing and calibration of the HDD-1409 D/A converter are done in a back-to-back hookup with its companion HAS-1409 A/D converter. See Figure 1.

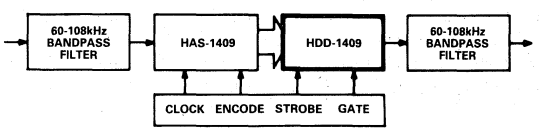


Figure 1. Basic Test Setup

The ac parameters of both converters have been optimized for operation at a word rate of 112kHz for reasons outlined in the detailed explanation of FDM/TDM Transmultiplexers included in the HAS-1409 A/D converter data sheet. This word rate is the one used in test and calibration of the units.

Analog signals in the frequency band of 60-108kHz are applied through a bandpass filter to the input of the HAS-1409 A/D converter. The output of the A/D is a digital representation of this signal and is applied to the HDD-1409 D/A converter as 3-state TTL-compatible digital inputs. After reconstruction, the analog output of the D/A is filtered through the same type of filter used ahead of the A/D and is applied to the test and measurement circuits.

CLOCK and $\overline{\text{ENCODE}}$ signals generated by the test setup are synchronized to one another and are timed for correct interaction with the STROBE and GATE signals applied to the HDD-1409.

The timing relationships among the digital inputs, STROBE, GATE, and analog output signals are shown in Figure 2.

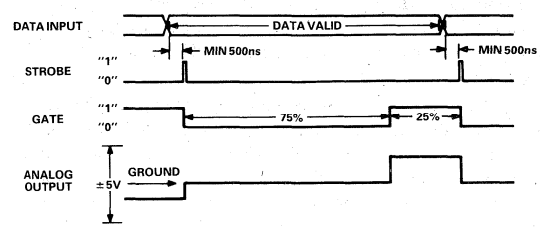


Figure 2. HAS-1409 Timing Diagram

The STROBE signal is shown as a single pulse for illustrative purposes to highlight that its positive-trigger leading edge establishes timing. In actual use, both LOW STROBE (pin 9) and HIGH STROBE (pin 26) signals are simultaneously applied to the HDD-1409 to latch the digital inputs into internal registers. This is easily accomplished through the simple expedient of connecting pins 9 and 26 together externally.

The GATE input shown in Figure 2 causes the analog output of the converter to be "on" for 25% of the duty cycle and "off" (connected to ground) for 75% of the duty cycle. This ratio makes the sin X/X compensation simpler when reconstructing

the digital inputs. If desired, the user could alter the timing of the GATE signal to allow the output to be "on" and/or "off" up to 50% of the duty cycle.

The type of testing which is done checks performance parameters for both the A/D and the D/A; as a result, it establishes the baseline performance for *both* units.

Refer to Figure 3 Intermodulation/Total Harmonic Distortion Test Circuit.

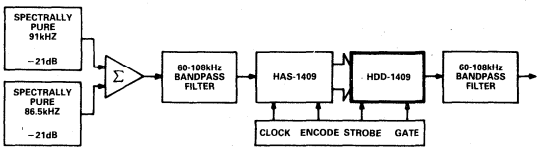


Figure 3. Intermodulation/Total Harmonic Distortion Test

To assure optimum performance in FDM/TDM transmultiplexer applications, the levels of harmonics and intermodulation (IM) products are both measured in the same way. The purpose of testing these parameters is to insure that "beat" frequencies which result from the interaction of two signals are far enough below those signals to avoid interfering with the carrier frequencies.

Spectrally pure sinewaves at frequencies of 91kHz and 86.5kHz are used because their interactions with one another will generate second and third-order harmonics which are easy to distinguish and measure. As in any sampling scheme, the generated frequencies are "folded" back into the passband of interest and their levels are a measure of converter performance.

Each test frequency is applied to a summation amplifier at a precise level 21dB below the rms value of a full-scale sinewave. After being digitized, reconstructed by the HDD-1409 D/A converter, and filtered, the amplitudes of the residual harmonics and IM products have typical levels of −100dB.

Refer to Figure 4 Noise Power Ratio Test Circuit.

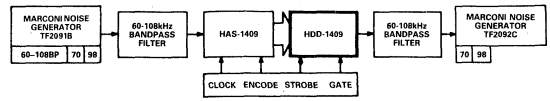


Figure 4. Noise Power Ratio Test Circuit

The measurement of noise power ratio (NPR) is a critical indicator of converter performance in telecommunications systems, and the test conditions must replicate the system environment to the maximum possible extent.

White noise in the frequency range of 60 to 108kHz is applied through the input filter, and the total power present in a narrow "slot" centered at 70kHz is computed. A bandstop filter 1kHz wide, also centered at 70kHz, is switched in and the total power still present in the "slot" is computed. The NPR is the ratio of these two readings and acceptable performance is typically 68dB.

Refer to Figure 5 Idle Noise Test Circuit.

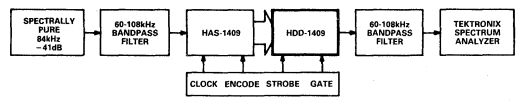


Figure 5. Idle Noise Test Circuit

As shown in Figure 5, a sinewave of 84kHz and good spectral purity is applied through the input filter to the A/D and D/A combination under test. As it is in the harmonics and IM distortion tests, the input level of the test signal is critical; for this measurement, it is at −41dB, referenced to the rms value of a full-scale sinewave.

The combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental 84kHz frequency and the idle noise components. The specification for acceptable performance requires that these components typically be at −104dB when using a 1kHz-bandwidth filter.

FDM/TDM TRANSMULTIPLEXERS

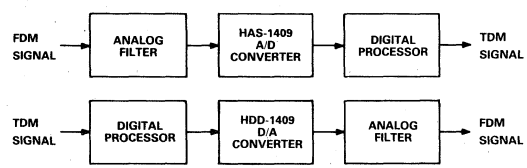
Two standard formats are used in telephony for multiplexing voice signals. The older of the two, frequency division multiplex (FDM), is used throughout the world for transmitting long distance telephone calls. In this scheme, voiceband signals are "stacked" into adjacent 4kHz channels in their assigned frequency domain by using single sideband (SSB) amplitude modulation.

In the newer time division multiplex, or TDM, each voice signal is digitized using pulse code modulation (PCM), at an 8kHz sample rate. As the name suggests, the resulting pulse streams are then interleaved in time and transmitted.

Digital toll switching offices, first installed in the United States in the latter part of the 1970s, continue to proliferate at a high rate. One of their major characteristics is that they switch signals exclusively in the TDM format within the office. But the need to operate also with the older FDM format means all incoming and outgoing signals must be converted to and from digital form.

The interface between the two standard signl multiplexing formats which is used to make this conversion is the FDM/TDM transmultiplexer system.

The application of digital signal processing (DSP) to the interface, as shown above, is extremely attractive since the frequency ranges of the signals which are involved make efficient use of available technology. In addition, the stringent interface specifications benefit from the precision which is inherent in a digital approach to the problem.



Digital FDM/TDM Translation

The analog filter shown in the upper portion of the diagram is used to remove undesirable out-of-band components from the FDM signal. The output of the filter is then applied to the HAS–1409 A/D converter whose output is a digital word stream. The individual channels within this stream are separated via a real-time processing algorithm in the block labeled Digital Processor. The resulting signal is now in the TDM format for switching and/or transmitting.

The lower portion of the diagram depicts the process of going from TDM to FDM, using the HDD-1409 D/A converter, in a procedure which is basically an inverse operation. The exception to that is the analog filter, which performs essentially the same function in both directions.

The reader is urged to consult the data sheet for the HAS-1409 A/D converter, which contains considerably more detail on the theory and application of FDM/TDM transmultiplexers.

ANALOG DEVICES

Hybrid Video Digital-to-Analog Converters

HDG SERIES

FEATURES
- Ultra Fast 7ns Settling Time to 0.4% (8ns Max)
- Low 50 pV-s Max Glitch Energy
- Operates from Single -5.2V Power Supply
- Complete Composite Inputs
- Designed for General Output Compatibility with EIA Standards RS-170 and RS-343, Including 10% Brightness
- Low Price

APPLICATIONS
- Raster Scan Graphics Displays
- TV Video Reconstruction
- Ultra Fast Current or Voltage Output DAC for Analytical Instrumentation
- Digital VCOs

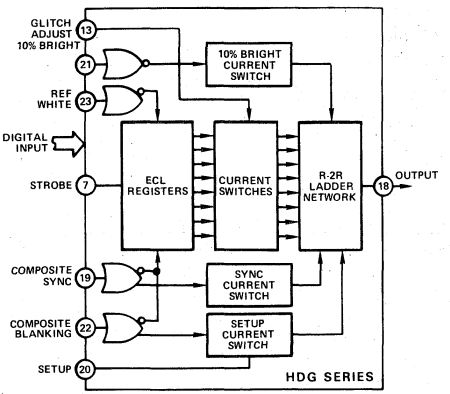
GENERAL DESCRIPTION

The HDG series digital-to-analog converters are the fastest D/As with full composite capabilities presently available. The units are available in three resolutions (levels) of Gray Scale. The HDG-0805 has 8 bits of resolution (256 levels) and typically settles in 7ns (8 max). The HDG-0605 has 6-bit resolution (64 levels) and typically settles in 5ns (6 max), while the HDG-0405 features 4-bit resolution (16 levels) and typically settles in less than 3ns (4 max). All three units are packaged in 24-pin metal hybrids and require only a single -5.2V power supply for operation.

All three units have complete composite controls including self-contained, digitally-controlled sync, blanking, and 10% bright, a unique feature not found on most composite D/A converters. A reference white control input is also provided, thus assuring compatibility with EIA Standards RS-170, RS-330, and RS-343A.

Absolute accuracies of the HDG-0805, HDG-0605 and HDG-0405 are ±0.19, 0.8, and 3.2% respectively. The output impedance is 75Ω and the full scale output current of -17mA is sufficient to develop 1V across a 75Ω video load. Operation of all three units is specified over the case temperature range of -25°C to +85°C. Monotonicity is guaranteed.

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



The HDG series D/A converters represent the most cost-effective high performance system solution for 8-bit raster scan D/A converter requirements. Older modular technology offers similar electrical performance but at much larger size and at a higher price. Monolithic technology has produced DACs at comparable speeds but without composite capabilities, thereby requiring external registers, sync and blanking circuits, and references for compatibility.

Model	Resolution	% of Gray Scale	Settling Time (max)
HDG-0805	8 Bits	0.4%	8ns
HDG-0605	6 Bits	1.6%	6ns
HDG-0405	4 Bits	6.4%	4ns

Table I. Accuracy vs. Settling Time

9

SPECIFICATIONS (typical @ +25°C with nominal power supplies and 75Ω output load unless otherwise noted)

Model[1]	Units	HDG-0405	HDG-0605	HDG-0805
RESOLUTION FS = FULL SCALE	Bits	4	6	8
LSB WEIGHT (Current)	μA	1072	268	67
LSB WEIGHT (Voltage)	mV	40	10	2.5
ACCURACY[2]				
Absolute	±% of GS	3.2	0.8	0.19
Linearity	±% of GS	3.2	0.8	0.19
Monotonicity		Guaranteed	*	*
Zero Offset (Initial)	mV	0.9	*	*
SPEED PERFORMANCE – GRAY SCALE OUTPUT				
Settling Time (Voltage) Max[3]	ns (to % GS)	4(6.4)	6(1.6)	8(0.4)
Slew Rate	V/μs	200	*	*
Update Rate[4]	MHz	100	*	*
Rise Time	ns	3	*	*
Glitch Energy[5]	pV-s	50	*	*
TEMPERATURE COEFFICIENTS				
Linearity	ppm/°C	16.0	*	*
Zero Offset	ppm/°C	6.0	*	*
Gain	ppm/°C	17.0	*	*
STROBE INPUT				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
Positive Logic) "0"	V	-1.7	*	*
Logic Loading		50pF and 5kΩ to -5.2V	*	*
Set-Up Time (Data)	ns	2.5 min	*	*
Hold Time (Data)	ns	1.5 min	*	*
Propagation Delay	ns	3	*	*
REFERENCE WHITE INPUT[6]				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
"0"	V	-1.7	*	*
Logic Loading		5pF and 50kΩ to -5.2V	*	*
DATA INPUTS				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
(Positive Logic) "0"	V	-1.7	*	*
Logic Loading (Each Bit)		5pF and 50kΩ to -5.2V	*	*
Coding (See Table)		Complementary Binary (CBN)	*	*
COMPOSITE SYNC, BLANKING, AND 10% BRIGHT INPUTS				
Logic Compatibility		ECL	*	*
Logic Voltage Levels "1"	V	-0.9	*	*
"0"	V	-1.7	*	*
Logic Loading		5pF and 50kΩ to -5.2V	*	*
SETUP CONTROL				
Ground	mV	0 (0 IRE Units)	*	*
Open	mV	71 (10 IRE Units)	*	*
-5.2V	mV	142 (20 IRE Units)	*	*
OUTPUT				
Current	mA	0 to -17	*	*
Voltage[7]	V (±1%)	0 to -0.600	0 to -0.630	0 to -0.6375
Compliance	V	+1.1 to -1.1	*	*
Internal Impedance	Ω (±5%)	75	*	*
OUTPUT – COMPOSITE SYNC				
Current	mA (±5%)	0 or -7.6	*	*
Voltage	mV (±5%)	0 or -286	*	*

Model	Units	HDG-0405	HDG-0605	HDG-0805
OUTPUT – 10% BRIGHT				
Current	mA (±5%)	0 or -1.9	*	*
Voltage	mV (±5%)	0 or -71	*	*
OUTPUT – COMPOSITE BLANKING[8]				
Current	mA (±1.5%)	0, -17.0, -18.9, or -20.8	*	*
Voltage	mV (±1.5%)	0, -637.5, -708.75 or -780	*	*
SPEED PERFORMANCE – CONTROL INPUTS				
Settling Time to 10% of Final Value for:				
Composite Sync	ns	8	*	*
Composite Blanking	ns	8	*	*
Reference White	ns	8	*	*
Reference Black	ns	8	*	*
10% Bright	ns	8	*	*
POWER REQUIREMENTS				
-5.2V ±0.25V[9]	mA	200	260	320
Power Supply Sensitivity	%/%	1/1	*	*
TEMPERATURE RANGE				
Operating, Metal Case	°C Case	-25 to +85	*	*
Storage	°C	-55 to +125	*	*
MTBF[10]				
Mean Time Between Failure	hours			560,900
PACKAGE OPTIONS[11]		HY24G		HY24E

NOTES
[1] HDG-XXXXW specs same as HDG-XXXX.
[2] Accuracy is relative to Gray Scale and includes linearity.
[3] Worst case settling to a percentage of maximum Gray Scale is given, and includes FS and MSB transitions. The inherent 3ns propagation dea
propagation delay through the input registers (50% points) has been disregarded.
[4] The update rates shown are limited by a full-scale settling time that is useable for the number of bits of resolution. The DACs may be updated to a maximum of 125MHz with some settling time degradation.
[5] Reducible to less than 25p V-s with glitch adjustment.
[6] A Logic "0" on Pin 29, Reference White will drive the output to the Reference White level regardless of digital input.
[7] The diffrence between the full-scale output of 637.5mV and 643mV shown elsewhere herein (HDG-0805) is due to the fact that we selected an LSB value of 2.5mV for ease of calibration. These differences are well within the output and EIA Standard RS-170 tolerances.
[8] The three currents and voltages correspond to the three set-up levels of 0, 10, and 20 IRE units as externally selected.
[9] Power Supply must have less than 5mV p-p ripple.
[10] Calculated for HDG-0805 using MIL Handbook 217. Ground: Fixed; Ambient Temperature 25°C.
[11] See Section 19 for package outline information.

*Specifications same as HDG-0405.
Specifications subject to change without notice.

9

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	13	GLITCH ADJUST
2	-5.2V	14	GROUND
3	BIT 1 (MSB)	15	GROUND
4	BIT 2	16	GROUND
5	BIT 3	17	GROUND
6	BIT 4	18	ANALOG OUTPUT
7	CLOCK	19	COMPOSITE SYNC
8	BIT 5	20	SETUP
9	BIT 6	21	10% BRIGHT
10	BIT 7	22	COMPOSITE BLANKING
11	BIT 8 (LSB)	23	REFERENCE WHITE
12	GROUND	24	-5.2V

NOTES: FOR HDG-0605 PIN 9 IS LSB AND PINS 10 AND 11 ARE PRESENT BUT NOT USED.
FOR HDG-0405 PIN 6 IS LSB AND PINS 8, 9, 10 AND 11 ARE PRESENT BUT NOT USED.

Typical Applications

A typical raster scan graphics display system is depicted in Figure 1. The system consists of a MOS RAM memory buffer for storing the data to be displayed, one or more memory controllers for display updating and CRT refresh, and a programmable μP for graphics generation and image manipulation. The system acts as an intelligent peripheral to the host CPU, and drives standard television monitors via the built-in DAC circuitry.

The D/A converter controls the Z axis of the CRT modulating the brightness of the raster scan beam. A typical raster scan system requires resolution anywhere from 4 to 8 bits, which represents 16 to 256 levels of Gray Scale. For color displays three DACs are required—one each for the red, green, and blue color guns.

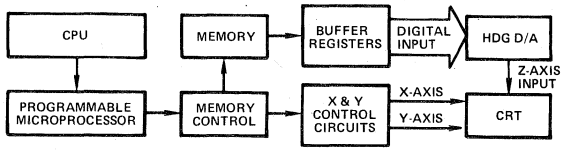


Figure 1. Typical Raster Scan Display System

APPLICATIONS INFORMATION

The HDG series D/A converters feature the fastest 8-bit settling times presently available. To insure maximum performance at these speeds the following guidelines should be followed:

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor mounted between the -5.2V supply line and ground near the D/A.
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 2 and 24 to ground (see Figure 2).

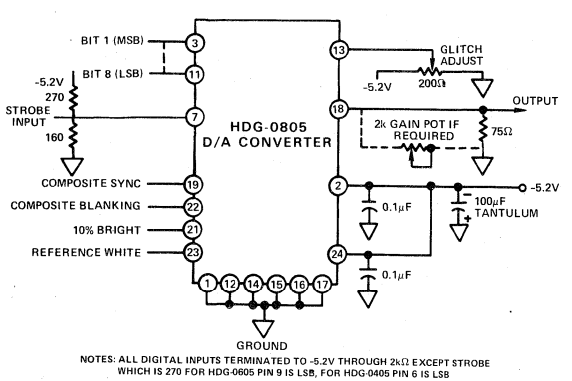


Figure 2. HDG-0805 Typical Connection Diagram

4. The threshold of the internal current switches can be optimized for low glitch energy by the addition of an external potentiometer connected to Pin 13 of the D/A (see Figure 2). This potentiometer is adjusted for minimum glitch energy as shown in Photo 2.
5. Standard 24 pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/As should be soldered directly into the printed circuit board without sockets.
6. Microstrip techniques are recommended for routing digital and strobe inputs to the DAC for distances greater than 1" (2.54mm).

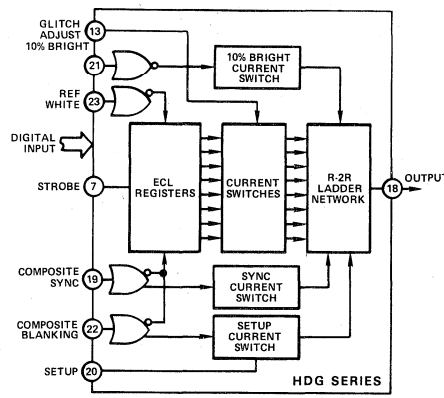


Figure 3. Block Diagram HDG-Series DAC

POWER SUPPLY SENSITIVITY — PRECISION -5.2V SUPPLY

As shown in the Specifications section, the power supply sensitivity is 1/1. This means a 1% change in power supply voltage will cause a 1% change in the full scale output.

As an example, a change of 52mV (1%) in the -5.2V power supply will cause 11mV (1%) change in the full scale output level (75Ω load).

If a "clean" (less than 5mV p-p ripple) -5.2V power supply is not readily available, it can be derived by using a MC7905.2 or LM120 or equivalent 3-terminal negative regulator. This is particularly important when using the HDG-0805; on the HDG-0405 and HDG-0605, even 5mV ripple is less than 1/2LSB.

Well-regulated, precise -5.2V may be desirable to help counteract the effects of time and temperature on D/A performance. A circuit to supply -5.2V is shown in Figure 4; it uses AD584 and AD OP-07 components to achieve an ultra stable D/A power supply voltage.

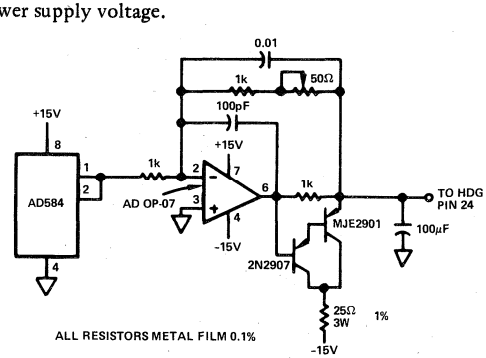


Figure 4. Precision -5.2V Supply

TESTING THE HDG SERIES DACs

Settling Time

Measuring the full-scale settling time of an 8ns DAC presents a significant challenge even under perfect conditions. The only practical solution using oscilloscopes is to extrapolate the settling time from a rise-time measurement. This is because the vertical amplifier of the scope will undoubtedly be overdriven when the required gain is achieved.

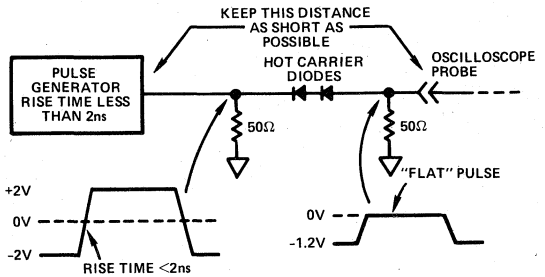


Figure 5. Flat Pulse Generator

Using the circuit of Figure 5, a pulse generator with rise times of less than 2ns is a must. The scope probe is calibrated using the resistor/diode scheme shown, which results in a "flat pulse." The rise time (10% to 90%) of the all "0s" to all "1s" transition, t_r, is measured using a sampling oscilloscope having a bandwidth of 500MHz minimum. The associated time constant, τ, is related to t_r by the following:

$$t_r = 2.2\tau$$

Assuming an exponential function, the D/A output, V, is given by:

$$V = (1 - e^{-t/\tau})\, V_O$$

The settling time required, t_s, to reach a percentage of the final output, V_O is given by the following table:

Resolution	% of Full Scale	Settling Time
8	0.4	2.5 t_r
7	0.5	2.2 t_r
6	1.6	1.9 t_r
5	3.2	1.5 t_r
4	6.4	1.2 t_r

It can then be seen that using the HDG rise time of 3ns results in settling times of 3.6, 5.7, and 7.5ns for the HDG-0405, 0605, and 0805 respectively.

Photo 1 shows an actual full-scale output signal measured using the above procedure indicating a rise time of 2.5ns. The corresponding settling time to 8-bit accuracy would thus be 6.3ns.

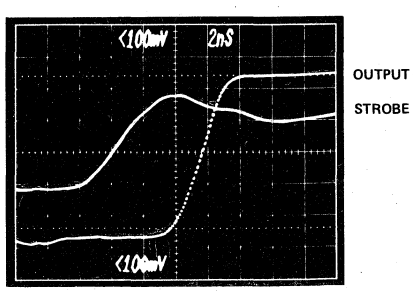


Photo 1. Full Scale Output — Rise Time

Glitch Energy

The glitch amplitude of the HDG series DACs at the major carry point is typically less than 100mV. This allows the user to measure it directly since there is little danger of overdriving the oscilloscope's vertical amplifier. Distances from the DAC output to the scope input should be minimal (no more than a few inches). Photo 2 shows an actual HDG-0805 mid-scale glitch measured using the 50Ω input of the sampling scope as termination for the D/A. The D/A test set output was connected directly to the scope using the appropriate BNC fittings. Positive and negative glitch energy in the photo is less than 30 picovolt-seconds. Net glitch energy is approximately zero. Note that glitch settling is less than 6ns.

In the rare case that positive and negative glitch excursions are unequal the glitch adjust input (Pin 13) may be used as shown in Figure 2 to minimize the net glitch energy.

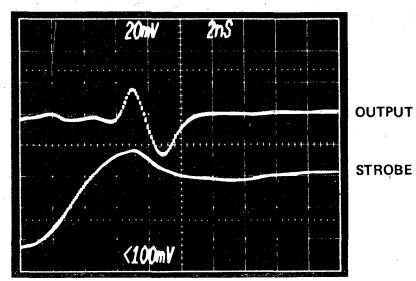


Photo 2. Midscale Glitch

CHARACTERISTICS OF HDG-0805, [-0605], [-0405] VIDEO DACs

COMPOSITE VIDEO SIGNAL
256 gray levels plus blanking and sync levels [64] [16]

STEP SIZE
2.5 [10] [40] mV

GRAY SCALE RANGE
0.643V Peak to Peak

SETUP CONTROL
User programmable in three levels

	mV	IRE Units
1. Input Grounded	0	0
2. Input Open	71	10
3. Input to -5.2V	142	20

REFERENCE WHITE LEVEL
0V Absolute
100 IRE Units (+0.714V relative to blanking level with standard setup; +0.643V relative to Reference Black)

DIGITAL INPUT FOR WHITE LEVEL
All ones (11111111)

REFERENCE WHITE CONTROLS[1]
Overrides Video Input Word
A Logic "0" on Pin 23 will drive the output to the Reference White Level.

REFERENCE BLACK LEVEL
-0.643V Absolute; +71mV (10 IRE Units)
Relative to blanking level with standard setup.

DIGITAL INPUT FOR REFERENCE BLACK
All zeroes (00000000)

COMPOSITE BLANKING LEVEL
-0.714V absolute, (0 IRE Units) with standard setup.

COMPOSITE BLANKING INPUT – PIN 22
Logic "0" on Pin 22 resets input register to 00000000, and causes output voltage to go negative by the amount of setup voltage with respect to the all "0" output voltage.

COMPOSITE SYNC LEVEL
-1.0V absolute with standard setup.
-0.286V (-40 IRE Units) relative to blanking level (Back Porch).

COMPOSITE SYNC INPUT – PIN 19
Logic "0" resets input register to 00000000, and the output voltage goes negative by 0.286V.

10% BRIGHT – PIN 21
Logic "0" causes output to go positive by 71mV.
Note: The most positive output voltage is still 0 volts absolute. All other levels are shifted down by 71mv; i.e., Sync Level (-40 IRE) becomes -1.071V.

STROBE – PIN 7
Logic "0" to Logic "1" transition clocks input register.

DEFINITION OF VIDEO TERMS

BLANKING LEVEL
The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
This usually refers to the technique of combining the three primary colors of Red, Green, and Blue to produce color pictures within the usual spectrum. In RGB monitors, three HDG "C" Series DACs would be required, one for each color.

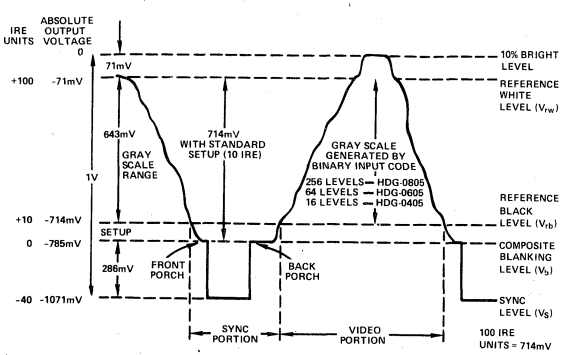


Figure 6. HDG-0805 Composite Output Waveform

COMPOSITE SYNC SIGNAL (SYNC)
The portion of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
The discrete levels of video signal between Reference Black and Reference White levels. A 10-bit DAC contains 1,024 different levels, while an 8-bit DAC contains 256 (2^N).

RASTER SCAN
The most basic method of sweeping a CRT one line at a time to generate and display images. This method is used in commercial television in the USA.

REFERENCE BLACK LEVEL
The maximum negative polarity amplitude of the video signal.

REFERENCE WHITE LEVEL
The maximum positive polarity amplitude of the video signal.

SETUP
The difference between the Reference Black level and the blanking level. This should not be confused with setup as used with digital logic.

SYNC LEVEL
The peak level of the composite SYNC signal.

VIDEO SIGNAL
That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

NOTE
[1] Reference White (Pin 23) should not be activated at the same time as composite blanking (Pin 22).

ORDERING GUIDE

Model	Resolution	Settling Time (max)
HDG-0805 HDG-0805W	8 Bits	8ns
HDG-0605 HDG-0605W	6 Bits	6ns
HDG-0405 HDG-0405W	4 Bits	4ns

ANALOG DEVICES

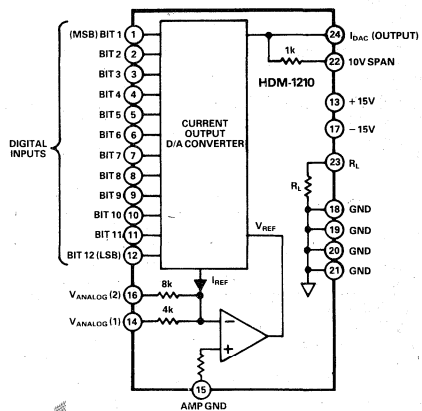
Ultra High Speed Multiplying D/A Converter

HDM-1210

FEATURES
Small Size: 24-Pin DIP
12-Bit Multiplying Accuracy
Good Drive: 10.24mA
Highest Speed Available

APPLICATIONS
CRT Displays
Waveform Generation
Vector Generation
MHz-Rate Digital Attenuators

HDM-1210 FUNCTIONAL BLOCK DIAGRAM



9

GENERAL DESCRIPTION

The HDM-1210 converter is an ultra-high-speed current output multiplying converter which offers circuit designers a chance to obtain high speed, good drive, and flexible design parameters in a DIP package. It can accept 12 bits of digital input data and combine them with two analog inputs into a multiplied output for use in a wide variety of applications.

Typical analog settling time to 12 bits of accuracy is only 175ns; and 3dB analog bandwidth is 10MHz. Digital settling time to 1/2LSB accuracy at the major carry transition is an incredible 65ns, making the HDM-1210 D/A extremely attractive for a range of high-speed multiplying functions.

In one mode of operation, its output current is precisely proportional to the analog input signal, multiplied by the digital input code. The analog signal being multiplied can be a sine wave, triangle wave, sawtooth, or any one of a variety of complex waveforms. The output is an accurate scaled version of the input, with the digital input used as the scale factor.

In another mode of operation, the analog input voltage can be used as the scale factor for the digital input code. In addition to this kind of flexibility, the HDM-1210 also has various offsetting capabilities which allow the analog input, digital input, analog output, and/or an external amplifier to be combined. With these features, the HDM-1210 can be used to accommodate unipolar or bipolar operation; and provide either one-quadrant or two-quadrant multiplication.

SPECIFICATIONS (typical @ +25°C with nominal power supplies; V_{ANALOG} (1) = −5V; and V_{ANALOG} (2) = 0V unless otherwise noted)

Parameter	HDM-1210BD	Units
RESOLUTION	12	Bits
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Current	2.5	μA
LINEARITY		
Differential	±1/2	LSB
Integral	±1/2	LSB
Monotonicity	Guaranteed	
TEMPERATURE COEFFICIENTS		
Differential Linearity	±2	ppm/°C
Integral Linearity	±2	ppm/°C
Full-Scale Gain	±20	ppm/°C
DYNAMIC CHARACTERISTICS		
Digital Settling Time		
(To 1/2LSB; Major Carry Transition)	65	ns
DIGITAL DATA INPUTS		
Logic Compatability	TTL	
Logic Levels		
"1"	+2.4 to +5.0	V
"0"	0 to +0.4	V
Coding		
Unipolar	Binary (BIN)	
Bipolar	Offset Binary (OBN)	
All "1's" Input	Maximum Positive Output	
All "0's" Input	Maximum Negative Output	
OUTPUT[1] (FS = Full Scale)		
Current Range[2] (±0.1% Accurate @ FS)	0 to +10.24 FS	mA
Voltage Range[3,4] (±0.5% Accurate @ FS)	0 to +1.024 FS	V
Zero Offset[3]	10	μV
Voltage Noise, rms (0.1Hz to 15MHz)	13	μV
Compliance	+1.5; −2	V
Resistance[4]	100 (0.5)	Ω (±)
MULTIPLYING CHARACTERISTICS[5]		
V_{ANALOG} (1) Input Resistance	4	kΩ
V_{ANALOG} (2) Input Resistance	8	kΩ
V_{ANALOG} (1) Input Range (Pin 14):		
V_{ANALOG} (2) = 0V to	0 to −5 FS to	V
V_{ANALOG} (2) = −5V to	+2.5 to −2.5 FS to	V
V_{ANALOG} (2) = −10V	+5 to 0 FS	V
V_{ANALOG} (2) Input Range (Pin 16):		
V_{ANALOG} (1) = 0V to	0 to −10 FS to	V
V_{ANALOG} (1) = −2.5V to	+5 to −5 FS to	V
V_{ANALOG} (1) = −5V	+10 to 0 FS	V
Analog Feedthrough at I_{DAC}	1	LSB
(V_{ANALOG} (1) = 5V p-p, 200kHz; All Digital Inputs @ "0")		
Analog Settling to ±0.025% FS	175	ns
(V_{ANALOG} (1) = 0V to −5V Step; All Digital Inputs @ "1")		
FS Analog bandwidth (3dB)	10	MHz
POWER REQUIREMENTS		
+15V ±5%	60	mA
−15V ±5%	25	mA
Power Supply		
Rejection Ratio	0.05	%/V
TEMPERATURE RANGE		
Operating (Case)	−25 to +85	°C
Storage	−55 to +125	°C
PACKAGE OPTION[6]	D24B	

NOTES
[1]FS accuracies are ±1% when using V_{ANALOG} (2) input.
[2]Current output into short circuit.
[3]Voltage output into open circuit.
[4]R_L (Pin 23) connected to I_{DAC} (Pin 24).
[5]Two-quadrant multiplying requires external op amp operating in bipolar mode.
[6]See Section 19 for package outline information.

Specifications subject to change without notice.

HDM-1210 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	13	+15V
2	BIT 2	14	V_{ANALOG} (1)
3	BIT 3	15	AMPLIFIER GROUND
4	BIT 4	16	V_{ANALOG} (2)
5	BIT 5	17	−15V
6	BIT 6	18	GROUND
7	BIT 7	19	GROUND
8	BIT 8	20	GROUND
9	BIT 9	21	GROUND
10	BIT 10	22	10V SPAN
11	BIT 11	23	R_L
12	BIT 12 (LSB)	24	I_{DAC} (OUTPUT)

NOTE
PINS 15, 18, 19, 20 AND 21 NEED TO BE CONNECTED TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

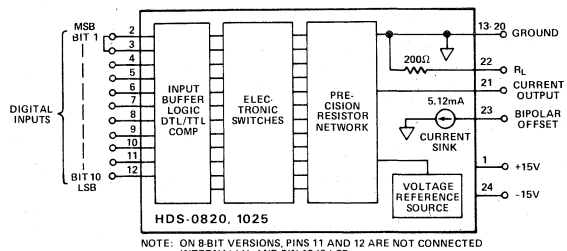
8-, 10-, 12-Bit Video Speed Hybrid Current & Voltage Out D/A Converter

HDS-0820, -1025, -1250/HDH-0802, -1003, -1205

FEATURES
- 25ns Current Settling to 0.1% (HDS)
- 200ns Voltage Settling to 0.1% (HDH)
- 10mA Current Out (HDS)
- Guaranteed Monotonicity Over Temperature
- No External Parts Required
- Reliable Hybrid Construction

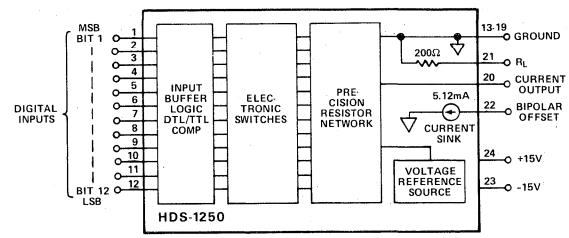
APPLICATIONS
- CRT Vector Displays
- TV Video Reconstruction
- Analytical and Medical Instruments

HDS-0820, HDS-1025 FUNCTIONAL BLOCK DIAGRAM

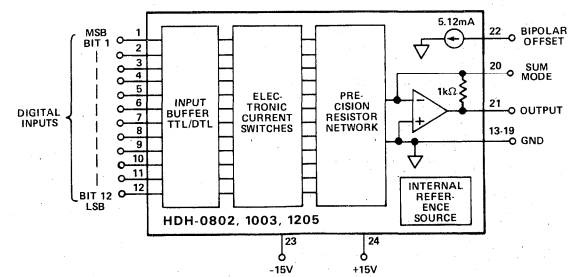


NOTE: ON 8-BIT VERSIONS, PINS 11 AND 12 ARE NOT CONNECTED INTERNALLY, AND PIN 10 IS LSB.

HDS-1250 FUNCTIONAL BLOCK DIAGRAM



HDH-0802, HDH-1003 AND HDH-1205 FUNCTIONAL BLOCK DIAGRAM



NOTE: ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

GENERAL DESCRIPTION

The HDS/HDH series of digital-to-analog converters are among the fastest precision settling current and voltage DACs available. They can be processed to guarantee monotonic over their operating temperature range. The current output models provide 10mA full scale allowing direct drive of capacitive loads and transmission lines. All versions have a precision reference and are active laser trimmed to specified accuracy, so no external adjustment pots or other components are required.

With six units available, engineering trade-offs can be made among resolution, speed, current or voltage output, and price. To facilitate this comparison major specifications are summarized in Table I.

Other general specifications that apply to all devices include TTL logic; ceramic or hermetic metal package; unipolar or bipolar operation with internal offsetting reference.

The HDH voltage output devices provide access to the op amp summing point so that reduced full-scale output voltage swing can be provided. Operation with an external resistor shunting the internal 1k resistor will reduce the already low op amp offset drift.

Model	Resolution	Full Scale Step Settling Time
Current Output		10mA Step
HDS-0820	8 Bits	20ns to 0.4%
HDS-1025	10 Bits	25ns to 0.1%
HDS-1250	12 Bits	35ns to 0.025%
Voltage Output		10V Step
HDH-0802	8 Bits	200ns to 0.4%
HDH-1003	10 Bits	300ns to 0.1%
HDH-1205	12 Bits	500ns to 0.125%

Table I

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

		CURRENT OUT			VOLTAGE OUT		
MODEL	UNITS	HDS-0820	HDS-1025	HDS-1250	HDH-0802	HDH-1003	HDH-1205
RESOLUTION FS = Full Scale	Bits	8	10	12	8	10	12
LSB WEIGHT		40μA	10μA	2.5μA	40mV	10mV	2.5mV
ACCURACY (Relative to FS Including Linearity)	±% FS	0.1	0.05	0.0125	0.1	0.05	0.0125
Linearity		±10μA	±5μA	±1.25μA	±10mV	±5mV	±1.25mV
	LSB	±1/4	±1/2	±1/2	±1/4	±1/2	±1/2
Monotonicity		Guaranteed Over Operating Temperature Range					
Zero Offset (Initial)		15nA max	*	*	10mV typ 50mV max	*	*
TEMPERATURE COEFFICIENTS							
Linearity	ppm/°C	3	*	*	*	*	*
Gain	ppm/°C	30	*	*	*	*	*
Unipolar Offset	ppm/°C	3	*	*	*	*	*
Bipolar Offset	ppm/°C	15	*	*	*	*	*
DATA INPUTS							
Logic Compatibility		TTL and 5V CMOS					
Logic Voltage Levels Positive Logic "1" =	V	+2 to +7	*	*	*	*	*
"0" =	V	0 to +0.8	*	*	*	*	*
Logic Loading (Each Bit) "1" =	μA	40	*	*	*	*	*
"0" =	mA	-2.6	*	*	*	*	*
Codes		BIN, OBN			BIN,OBN		
OUTPUT							
Current Range FS							
Unipolar	mA	+10.24	*	+10.24 ±0.2% (max)	±25 max	**	**
Bipolar	mA	±5.12	*	±5.12 ±0.2% (max)	±25 max	**	**
Voltage Out FS[1,2]							
Unipolar HDS with 200Ω Internal Connected R_L	V	+1.024	*	+1.024 ±0.05%	-10.24 ±0.1%	**	**
Bipolar	V	±0.512	*	±0.512 ±0.025%	∓5.12 ±0.05%	**	**
Compliance	V	+1.5, -2	*	*	N/A	**	**
Impedance, Internal (See Figure 1)	Ω	200	*	*	0.1 max	**	**
SETTLING TIME							
Current	ns to % FS	20 to 0.4	25 to 0.1	35 to 0.025	N/A	N/A	N/A
Voltage[2]							
Unipolar or Bipolar Out, 75Ω Load, 0.56V p-p	ns to % FS	30 to 0.4	35 to 0.1	50 to 0.025	N/A	N/A	N/A
Unipolar or Bipolar Out, Internal 200Ω Load, 1.024V p-p	ns to % FS	45 to 0.4	50 to 0.1	60 to 0.025	N/A	N/A	N/A
10V Output Step	ns to % FS	N/A	N/A	N/A	200 to 0.4	300 to 0.1	500 to 0.025
5V Output Step	ns to % FS	N/A	N/A	N/A	150 to 0.4	200 to 0.1	350 to 0.025
POWER REQUIREMENTS							
+14.5V to +15.5V	mA max	42	*	55	70	**	**
-12V to -16V	mA max	14	*	18	40	**	**
Power Supply Rejection (+15V)	%/%	0.06	*	*	*	*	*
Power Supply Rejection Ration (-15V)	%/%	0.04	*	*	*	*	*
TEMPERATURE RANGE							
Operating – Glass Package	°C	0 to +70	*	*	*	*	*
Operating – "M" Metal Case[3]	°C	-55 to +125	*	*	*	*	*
Storage	°C	-55 to +125	*	*	*	*	*
PACKAGE OPTIONS[4]		HY24E			HY24G		

NOTES

[1] Other voltages may be obtained with external resistor.

[2] For HDS series, $V_{OUT} = I_{OUT} \times R_{equivalent}$ which is the value of the 200Ω internal impedance in parallel with the external load resistance. Thus, by correct selection of external R1 V_{OUT} can be any magnitude up to the + or - compliance voltage. See Figures 1 and 2.

[3] Contact factory or local Analog Devices sales office for "M" Metal Case device specifications and prices.

[4] See Section 19 for package outline information.

*Specifications same as HDS-0820.

**Specifications same as HDH-0802.

Specifications subject to change without notice.

PIN DESIGNATIONS
HDS-0820, HDS-1025

PIN	FUNCTION
1	+15V
2,3*	BIT 1 (MSB)
4	BIT 2
5	BIT 3
6	BIT 4
7	BIT 5
8	BIT 6
9	BIT 7
10	BIT 8
11	BIT 9 (HDS-1025)
12	BIT 10
13-20	GND
21	OUTPUT (I_O)
22	R_L 200Ω
23	BIPOLAR OFFSET
24	-15V

*PINS 2 AND 3 MUST BE CONNECTED TOGETHER EXTERNALLY.

PIN DESIGNATIONS
HDS-1250

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GND
20	OUTPUT (I_O)
21	R_L 200Ω
22	BIPOLAR OFFSET
23	-15V
24	+15V

PIN DESIGNATIONS
HDH SERIES

PIN	FUNCTION
1	BIT 1 (MSB)
2	BIT 2
3	BIT 3
4	BIT 4
5	BIT 5
6	BIT 6
7	BIT 7
8	BIT 8
9	BIT 9
10	BIT 10
11	BIT 11
12	BIT 12
13-19	GROUND
20	SUM NODE
21	OUTPUT
22	BIPOLAR OFFSET
23	-15V
24	+15V

ON HDH-0802 DEVICES, GROUND PINS 9, 10, 11 AND 12.
ON HDH-1003 DEVICES, GROUND PINS 11 AND 12.

9

Analog Output, ±5.12mA	Offset Binary
+5.11mA (1LSB)	111.....1
+2.56mA	110.....0
0mA	100.....0
-2.56mA	010.....0
-5.12mA	000.....0
Analog Output, 0 to +10.24mA	**Straight Binary**
+10.23mA	111.....1
+7.68mA	110.....0
+5.12mA	100.....0
+2.56mA	010.....0
0mA	000.....0

Table II. Coding HDS Series

Analog Output, ±5.12V	Complement Offset Binary
-5.1175V	111.....1
-2.56V	110.....0
0V	100.....0
+2.56V	010.....0
+5.12V	000.....0
Analog Output, 0 to +10.24V	**Complement Binary**
-10.2375V	111.....1
-7.68V	110.....0
-5.12V	100.....0
-2.56V	010.....0
0V	000.....0

Table III. Coding HDH Series

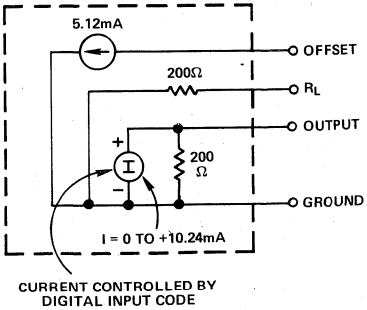


Figure 1. HDS Current Equivalent Circuit

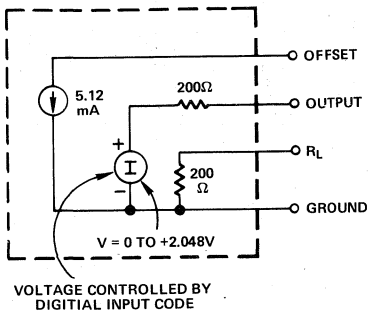


Figure 2. HDS Voltage Equivalent Circuit

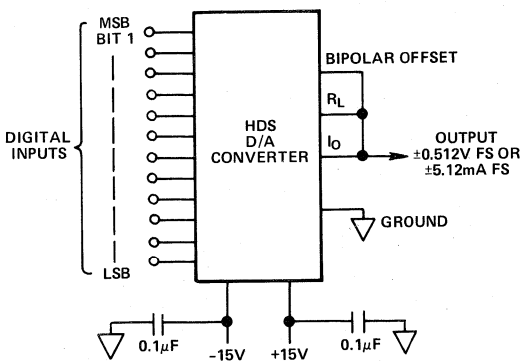


Figure 3. Bipolar Current Output

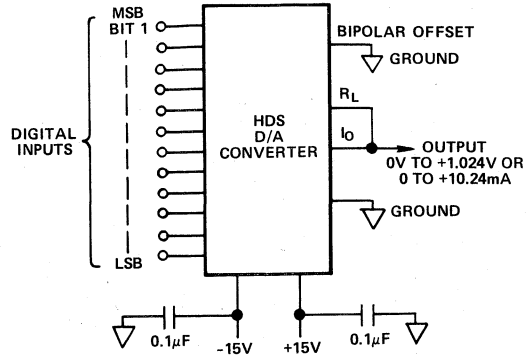


Figure 4. Unipolar Current Output

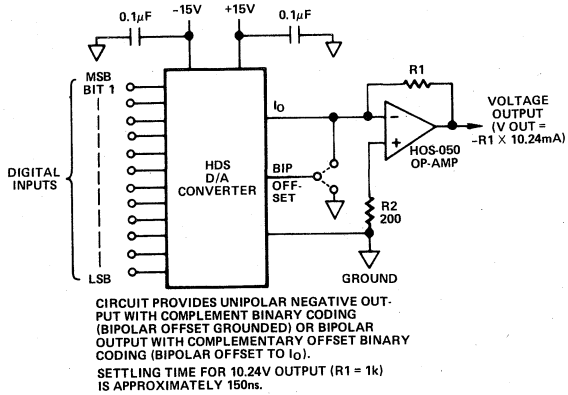


Figure 5. Inverting Unipolar or Bipolar Voltage Output

ORDERING INFORMATION

Order model number HDS-0820, HDS-1025, HDS-1250, HDH-0802, HDH-1003, HDH-1205. Models with extended operating temperature range, hermetically-sealed metal-case construction (M versions). Consult factory or local Analog Devices sales office for further information.

ANALOG DEVICES

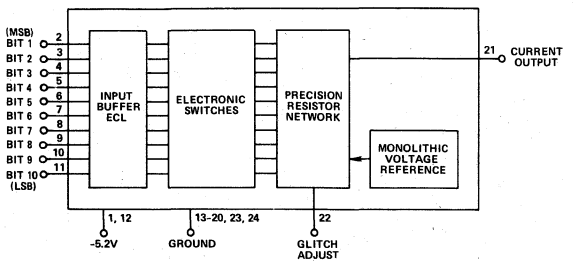
Ultra High Speed ECL Hybrid D/A Converter

HDS-0810E - HDS-1015E

FEATURES
Settling Times to 10ns
Low Glitch Energy — 200pV-sec.
100MHz Update Rates
8- & 10-Bit Versions Available
Low Power < 1 Watt

APPLICATIONS
Raster Scan & Vector Graphic Displays
TV Video Reconstruction
Digital VCO's
High-Frequency Waveform Generators
Analytical & Medical Instrumentation

HDS-0810E, HDS-1015E FUNCTIONAL BLOCK DIAGRAM



ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY

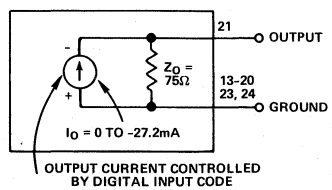
9

PRODUCT DESCRIPTION

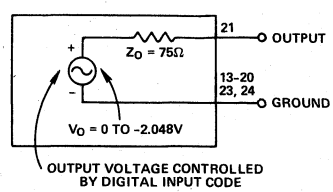
The HDS-0810E and HDS-1015E represent the state-of-the-art in ultra-high-speed hybrid D/A converters. They are designed to be input compatible with standard ECL logic families, and feature internal high-precision monolithic voltage reference, active laser-trimmed resistor network, and 75Ω output impedance — allowing them to be used to drive 75Ω cable directly without external driver amplifiers. This feature assures that a full 1 volt is available at the load, since the D/A output is a full 27mA. In addition, these D/A's are monotonic over the full operating temperature range and require only one power supply (-5.2V) for operation.

Packaged in an industry standard size 24-pin double width dual in-line case, the HDS-E Series D/A's are available in either ceramic cases (commercial) or hermetically sealed metal cases (extended).

The HDS-E D/A's are ideally suited for use in a wide variety of applications, including graphic CRT displays, since they feature very low glitch energy and extremely fast settling time.



Current Equivalent Circuit



Voltage Equivalent Circuit

SPECIFICATIONS (typical @25° C with nominal power supplies and with 75Ω output load unless otherwise noted)

MODEL	UNITS	HDS-0810E	HDS-1015E
RESOLUTION FS = Full Scale	Bits	8	10
LSB WEIGHT (Current)	μA	106	27
LSB WEIGHT (Voltage)	mV	4	1
ACCURACY[1]	±% FS	0.1	0.05
Linearity	±μA	26.5	13
Monotonicity		Guaranteed	*
Zero Offset (Initial)	μA	5	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C	5	*
Zero Offset	ppm/°C	1	*
Gain	ppm/°C	80	*
DATA INPUTS			
Logic Compatibility		ECL	*
Logic Voltage Levels "1" =	V	-0.9	*
(Positive Logic) "0" =	V	-1.7	*
Logic Loading "1" =	mA	+13.6	*
(Each Bit) "0" =	μA	-50	*
Coding (See Coding Table)		BIN	*
OUTPUT			
Current Range (Unipolar) FS	mA	0 to -27.2	0 to -27.3
Voltage with 75Ω Ext. Load	V (±1%)	0 to -1.020	0 to -1.023
Compliance	V	-1.1 to +1.1	*
Impedance, Internal	Ω (±5%)	75	*
SPEED PERFORMANCE			
Settling Time (Voltage)[2]	ns (to % FS)	10 (0.2)	15 (0.1)
Slew Rate	V/μs	200	*
Update Rate[3]	MHz	100	67
Rise Time	ns	4	4
Glitch Energy[4]	pV-sec	200	*
POWER REQUIREMENTS			
-5.2V ±0.25V	mA	155	180
Power Supply Rejection Ratio	%/%	0.04	*
Reference		Monolithic, Internal	*
TEMPERATURE RANGE			
Operating; Glass Case	°C	0 to +70	*
Operating; "M" Metal Case	°C	-55 to +125	*
Storage	°C	-55 to +125	*
PACKAGE OPTIONS[5]		HY24E	HY24G

NOTES
[1] Relative to FS, including linearity.
[2] Worst case settling time. Includes FS and MSB transitions.
[3] Limited only by D/A settling time.
[4] Reducible to less than 100pV-sec with appropriate deskewing of digital inputs.
[5] See Section 19 for package outline information.
*Specifications same as HDS-0810E.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1, 12	-5.2V
2	BIT 1 (MSB)
3	BIT 2
4	BIT 3
5	BIT 4
6	BIT 5
7	BIT 6
8	BIT 7
9	BIT 8
10	BIT 9
11	BIT 10 (LSB)
13-20	GROUND
21	OUTPUT
22	GLITCH ADJUST
23, 24	GROUND

ON THE HDS-0810E, PINS 10 AND 11 ARE NOT CONNECTED INTERNALLY, AND PIN 9 IS THE LSB. ALL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY.

ANALOG DEVICES

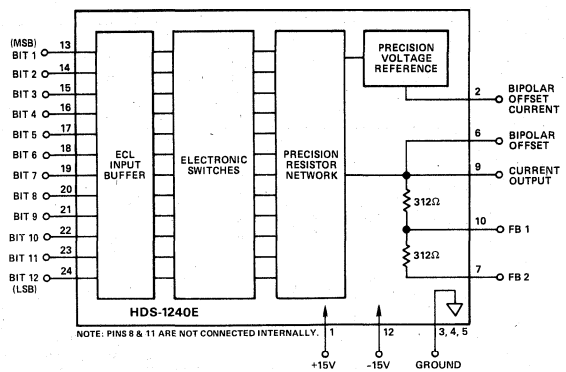
Ultra High Speed ECL Hybrid D/A Converter

HDS-1240E

FEATURES
12-Bit Settling Time to 40ns
Low Glitch Energy
ECL Compatible
Replacement for ADH-030, DA-4000, DAC397

APPLICATIONS
Graphic Displays - Random Scan
Digital VCO's
Waveform Generation
High-Speed ADC's

HDS-1240E FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDS-1240E is a 12-bit high current output hybrid IC D/A converter which has an output settling time of 40ns. Its inputs are compatible with standard ECL (emitter coupled logic), and it features an actively trimmed resistor ladder network for high accuracy. The HDS-1240E can be operated connection. For voltage output applications, the feedback resistors required for use with an external op-amp are built in to allow various voltage ranges without the need for external components. Additionally, the HDS-1240E features practically glitch-free operation without the need for external adjustments, and it operates on standard ±15 volt power supplies.

PIN DESIGNATIONS
HDS-1240E

PIN	FUNCTION	PIN	FUNCTION
1	+15 VOLTS	13	BIT 1 (MSB) INPUT
2	BIPOLAR OFFSET CURRENT	14	BIT 2 INPUT
3	GROUND	15	BIT 3 INPUT
4	GROUND	16	BIT 4 INPUT
5	GROUND	17	BIT 5 INPUT
6	BIPOLAR OFFSET	18	BIT 6 INPUT
7	FB 2	19	BIT 7 INPUT
8	N.C.	20	BIT 8 INPUT
9	OUTPUT	21	BIT 9 INPUT
10	FB 1	22	BIT 10 INPUT
11	N.C.	23	BIT 11 INPUT
12	-15 VOLTS	24	BIT 12 (LSB) INPUT

SPECIFICATIONS (typical @ +25°C with nominal power supply voltages unless otherwise noted)

Model	Units	HDS-1240E
RESOLUTION FS = Full Scale	Bits	12
LSB WEIGHT	μA	3.9
ACCURACY (Relative to FS)		
Linearity	% FS	±0.0125 max
Differential Linearity	% FS	±0.0125 max
Gain	% FS	±0.05 max
Zero Offset - Unipolar	μA	1
Zero Offset - Bipolar	μA	4
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C	±3 typ; ±5 max
Differential Linearity	ppm/°C	±3 typ; ±5 max
Gain	ppm/°C	25
Zero Offset	ppm/°C	10
DATA INPUTS		
Logic Compatibility		
Logic "1"		
Voltage Range (Operating)	V	-0.81 to -0.96
Voltage Range (Absolute max)	V	0
Current	mA	10 max
Logic "0"		
Voltage Range (Operating)	V	-1.65 to -1.85
Voltage Range (Absolute min)	V	-6
Current	μA	1 max
Coding		Complementary Binary (CBN) for Unipolar; Complementary Offset Binary (COB) for Unipolar
OUTPUT		
Current - Unipolar	mA	0 to -16
Current - Bipolar	mA	±8
Compliance	V	+0.5V to -1.1V
Impedance	Ω	200
Capacitance	pF	25
SPEED PERFORMANCE		
Settling Time[1]		
For FS Input Change		
to 1% of FS	ns	20 typ; 30 max
to 0.1% of FS	ns	35 typ; 50 max
to 0.0125% of FS	ns	40 typ
For 1LSB Change from 011...11 to 100...00 to 0.0125%	ns	30 typ; 35 max
Internal Skewing Time	ps	400 typ; 800 max
Output Time Constant	ps	3 into 100Ω load
Glitch Energy (with 100Ω Load)	pV-s	150
	mA-ns	2.5
POWER REQUIREMENTS		
Voltage - Operating	V	+15 ±10%: -15 ±10%
Voltage - Absolute Limit	V	+18, -18
Current	mA	20 typ; 30 max: 60 typ; 80 max
Rejection Ratio	%/V	0.02 max
TEMPERATURE RANGE (Case)		
Operating		
HDS-1240E	°C	0 to +70
HDS-1240EM, HDS-1240EMB	°C	-55 to +100
Storage	°C	-55 to +125
THERMAL RESISTANCE[2]		
Junction to Air, θja (free air)		
HDS-1240E	°C/W	38
HDS-1240EM, HDS-1240EMB	°C/W	45
Junction to Case, θjc		
HDS-1240E	°C/W	15
HDS-1240EM, HDS-1240EMB	°C/W	12
MTBF[3]		
Mean Time Between Failure		
Calculated Using MIL Handbook-217	hours	$>1.356 \times 10^6$
PACKAGE OPTIONS[4]		HY24E, HY24G

NOTES
[1] Measured with output loaded with 100Ω.
[2] Maximum junction temperature is 150°C.
Specifications subject to change without notice.
[3] HDS-1240EMB calculated using MIL Handbook-217 Ground: Fixed Temperature Case = 60°C.
[4] See Section 19 for package outline information.

APPLICATIONS

The HDS-1240E is a current output D/A converter which is input compatible with standard ECL (emitter coupled logic). Each digital input controls an internal switch, which through a precision binary weighted resistor network, sets the output current of the device. Starting with the most significant bit (MSB) and proceeding toward the least significant bit (LSB), each lesser bit controls one-half the current value of the preceeding bit. Therefore, the MSB (Bit 1) controls 8mA, Bit 2 controls 4mA, and so on until the LSB is reached which has a weight of 3.9μA. Thus, the output of the D/A varies from 0 with all digital inputs at a logic "1" state to -16mA with all inputs at a logic "0" state. This operating condition is called unipolar. For bipolar operation, an 8mA current source is provided. When this current source is connected to the output, it will then swing from -8mA to +8mA. See Figures 1 and 2 for this hook-up.

Transfer Characteristics

With the DAC hooked-up as shown in Figure 1, the output will be 0 to -16mA. Since the output compliance is +0.5V to -1.1V, care must be taken not to let the output voltage exceed these limits. The input/output relationships are shown in the table below.

Analog Output		Digital Input Code
Unipolar	**Bipolar**	
0	+FS	111...11
-1/2LSB	+FS -1LSB	111...10
-1/4FS	+1/2 FS	100...00
-1/2 FS +1LSB	+1LSB	100...00
-1/2FS	0	011...11
-1/2 FS -1LSB	-1LSB	011...10
-3/4 FS	-1/2LSB	001...11
-FS +1LSB	-FS -1LSB	000...00

Table I. Coding Table

ANALOG OUTPUT

A. Normal Operation Without Amplification

The HDS-1240E is a current output D/A converter. However, the wide voltage compliance of +0.5V to -1.1V allows it to be used to generate an output voltage within this range which is proportional to the digital input code and the load impedance. When the DAC is operated in this mode the following formulae apply:

$$V_O = -0.016\ [R_t]$$

$$R_t = \frac{R_i \times R_L}{R_i + R_L} = \frac{200\ (R_L)}{200 + R_L}$$

Where: R_i = the internal resistance of the DAC (200Ω)
R_L = the external load resistance loading the DAC
R_t = the total resistance seen by the DAC output current, i.e., R_i in parallel with R_L.

In general, the output voltage of DAC is limited to 1V p-p. In this instance, from the above formulae, it can be determined that the maximum external load resistance will be about 90Ω. Since the bipolar offsetting provision is a true current source, this calculation does not differ even when the DAC is used in the bipolar mode. Full-scale gain may be adjusted by varying R_L (see Figure 4).

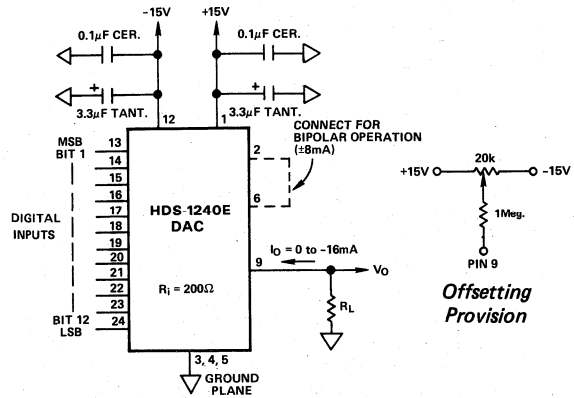


Figure 1. Current Output Operation

B. Operation with Voltage Amplification

There are certain applications that require more than the 1V p-p that is directly obtainable with the DAC output. In these circumstances, the use of an ultra-high speed operational amplifier is required. Figure 2 shows such an application utilizing the ADI Model HOS-050 op amp. The HDS-1240E DAC has built-in feedback resistors which are actively laser trimmed, and which eliminate the need for extra components. A variety of connections of these resistors allows various output voltages as shown in the table below. Care should be taken to keep all leads as short as possible, as the bandwidths encountered in these type circuits are quite high, and parasitics can be a very real problem. The power supply bypassing arrangement shown in Figure 1 should be used.

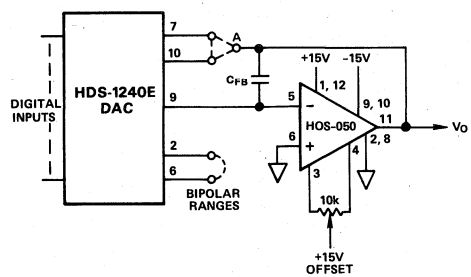


Figure 2. Voltage Output Operation

Voltage Range	Jumper Connections
±1.25V	7 to 9, 10 to A, 2 to 6
±2.5V	10 to A, 2 to 6
±5V	7 to A, 2 to 6
0 to +2.5V	7 to 9, 10 to A
0 to +5V	10 to A
0 to +10V	7 to A

Table II. Output Voltage Connections

NOTE: The value of Cfb should be optimized for best settling time without overshoot. If absolute accuracy of gain is required, a large value of resistance can be introduced in parallel with Pins 7 and 9 of the DAC.

High-Speed Low-Glitch Operation Suggestions

The HDS-1240E D/A offers the highest available speed. However, with this speed performance, certain precautions and operating conditions should be considered. You are now in the RF world.

1. The D/A converter should be provided with a very low impedance grounding system to very high frequencies. A large ground plane is a must.
2. Low frequency bypassing should be provided with 1μF (or larger) tantalum capacitors mounted between the ±15V supply lines and ground near the D/A (see Figure 1).
3. High frequency bypassing should be provided by ceramic capacitors of 0.1μF or larger mounted within 0.25 inches of Pins 1 and 12 to ground (see Figure 1).
4. The D/A converter should be driven with ECL registers as physically close to the D/A as possible. The 10176 HEX "D" Master-slave flip-flop is recommended. The six most significant bits should come from the same package as shown in Figure 4. The six least significant bits should come from a second package.
5. Each digital input should be terminated with a 510Ω resistor connected between the input and -5.2V (see Figure 4).
6. If required, variable capacitors can be added to "deskew" the most significant bits for lowest glitch—although this is not usually required in many applications. These capacitors are added as shown in Figure 4 (C1-4), and are adjusted for minimum glitch energy.
7. Standard 24-pin sockets should be avoided. Individual "pin sockets" are most suited for evaluating devices, as lead inductance is reduced. In final designs, the D/A's should be soldered directly into the printed circuit board without sockets.

ULTRA-LOW GLITCH OPERATION

For extremely low glitch requirements (<50 - 100pV-s), an HTS-0025 Track-and-Hold is recommended as a deglitcher (see Figure 3). The duration of the HDS-1240E D/A glitch is approximately 10ns. The hold time of the HTS-0025 should be at least 15ns to "mask out" the glitch.

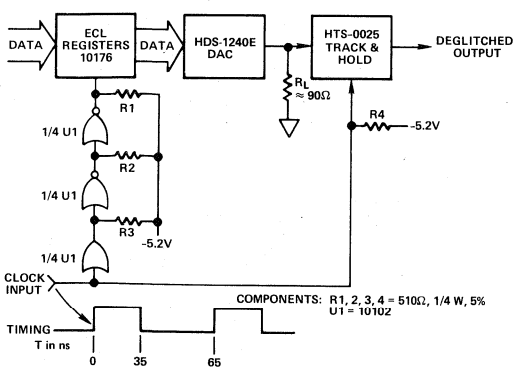
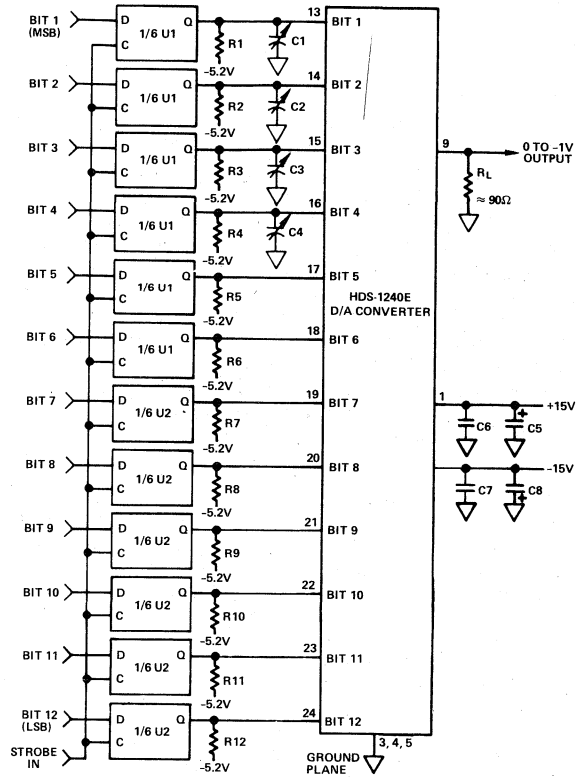


Figure 3. HTS-0025 Track & Hold Used with HDS-1240E D/A as Deglitcher @ 20MHz Update Rate



NOTES:
1. R1-1 = 510Ω, 1/4 W, 5%; R1 = OUTPUT LOAD; ADI P/N 79PR1K; C1 - ERIE 538-002F, 15-60pF, OR EQUIVALENT; C2, 3, 4 = ERIE 538-002D, 9-35pF, OR EQUIVALENT; C5, 8 = 3.3μF TANTALUM; C6, 7 = 0.1μF CERAMIC; U1, 2 = 10176, 10K ECL TYP "D" F-F.
2. THE FIRST SIX MOST SIGNIFICANT BITS (BITS 1-6) SHOULD ALWAYS BE ROUTED THROUGH ONE 10176 FOR CONSISTENCY IN TIMING AND REDUCED DATA SKEW.
3. R_L IS ADJUSTED FOR ABSOLUTE GAIN (FULL-SCALE) ACCURACY.

Figure 4. HDS-1240E — Typical Hook-Up and Test Circuit

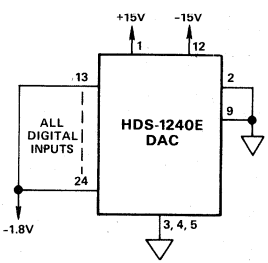


Figure 5. Recommended Burn-In Circuit

ORDERING INFORMATION

For commercial environment applications (0 to +70°C), order HDS-1240E. For extreme environment applications (-55°C to +100°C), order HDS-1240EM.

Analog-to-Digital Converters

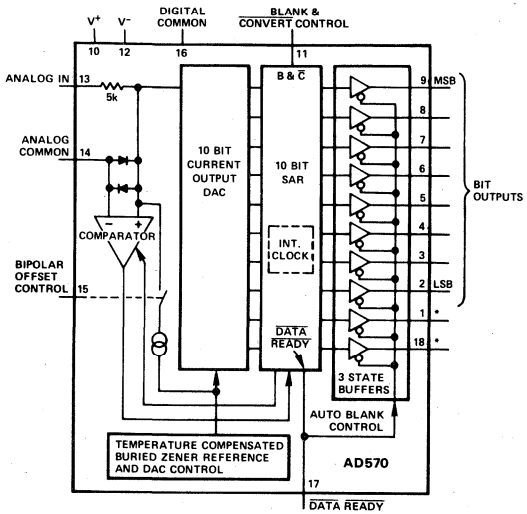
Contents

•New products since publication of *1982–1983 Databook Update.*

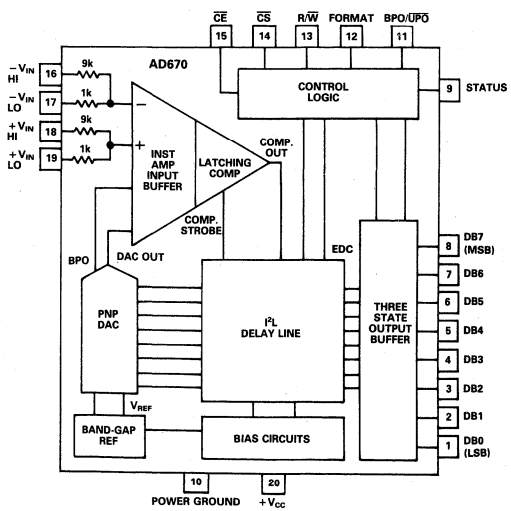
10

Selection Guide
Analog-to-Digital Converters

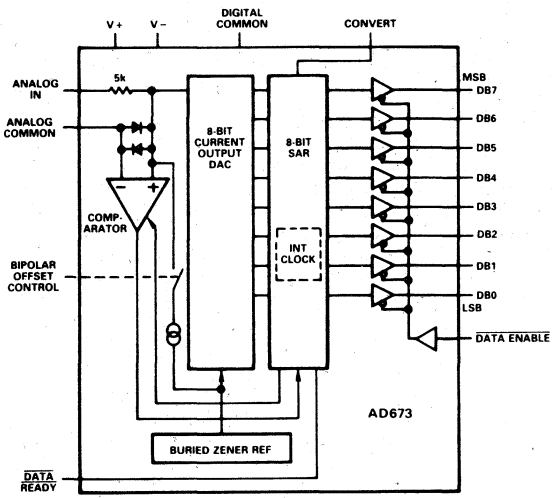
8-Bit A/D Converters



AD570



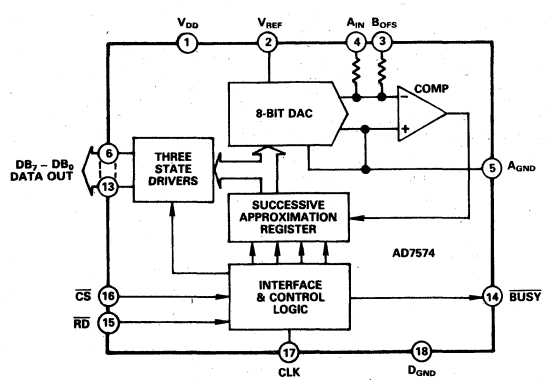
AD670



AD673

Page

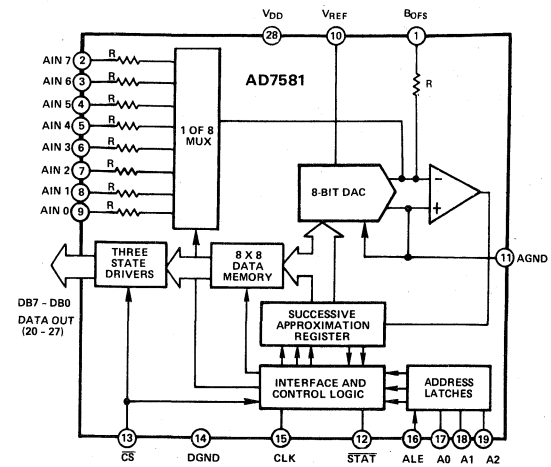
- **Complete 8-Bit A/D Converter with Reference, Clock and Comparator** Vol. I 10–95
- **Full Microprocessor Bus Interface**
- **Fast Successive Approximation Conversion – 20μs**
- **No Missing Codes Over Temperature**
- **Operates on +5V and −12V to −15V Supplies**



AD7574

- **No Missed Codes Over Full Temperature Range** Vol. I 10–151
- **Fast Conversion Time: 15μs**
- **Interfaces to μP like RAM, ROM or Slow Memory**
- **Low Power Dissipation: 30mW**
- **Ratiometric Capability**
- **Single +5V Supply**

Selection Guide
Analog-to-Digital Converters
8-Bit A/D Converters

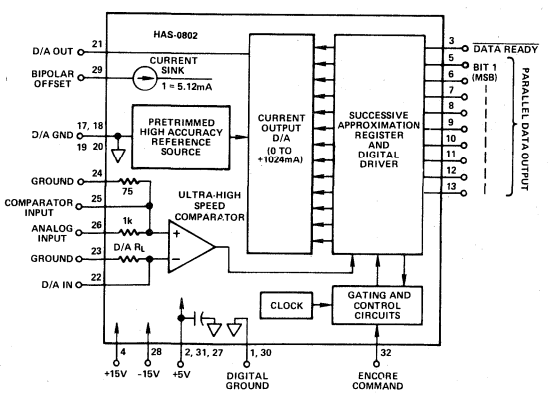


AD7581

Page

Vol. I
10–159

8-Bit Resolution
On-Chip 8×8 Dual-Port Memory
No Missed Codes Over Full Temperature Range
Interfaces Directly to Z80/8085/6800
CMOS, TTL Compatible Digital Inputs
Three-State Data Drivers
Ratiometric Capability
Interleaved DMA Operation
Fast Conversion
A/D Process Totally Transparent to μP

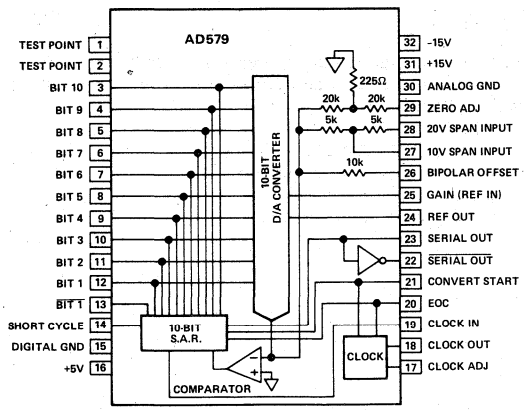


HAS-0802

Vol. I
10–201

Conversion Times as Low as 1.2μs
Resolution: 8 Bits
Exceptional Accuracy: 0.012% of F.S.
Low Power
Contained in Glass or Metal 32-Pin DIP
Adjustment-Free Operation

10-Bit A/D Converters



AD579

Page

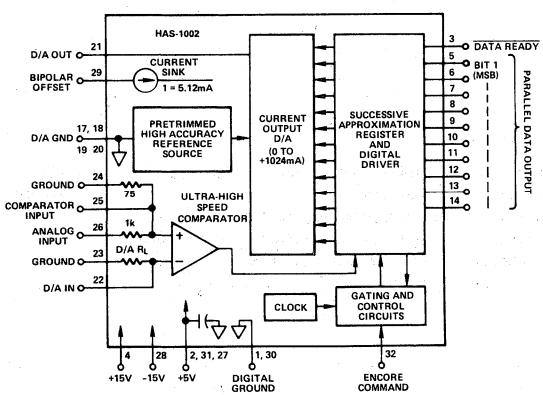
Complete 10-Bit A/D Converter with Reference and Clock Vol. I 10–79

Fast Successive Approximation Conversion: 1.8μs

Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max

Max Nonlinearity: <±0.048%

Low Power: 775mW



HAS-1002

Conversion Times as Low as 1.7μs Vol. I 10–201

Resolution: 10 Bits

Exceptional Accuracy: 0.012% of F.S.

Low Power

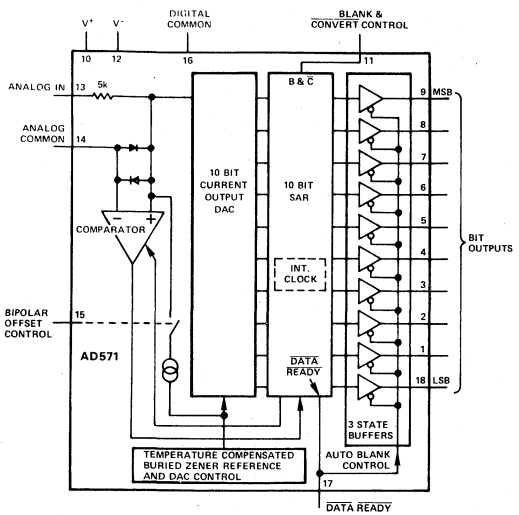
Contained in Glass or Metal 32-Pin DIP

Adjustment-Free Operation

10

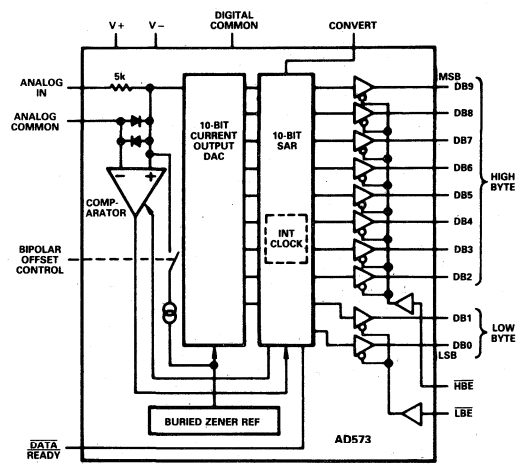
Selection Guide
Analog-to-Digital Converters

10-Bit A/D Converters



AD571

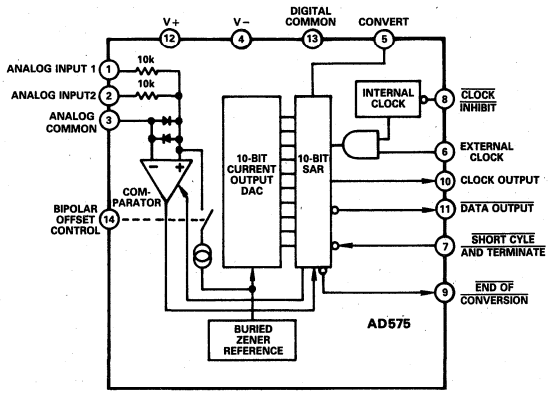
Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
0 to +70°C – AD571K
−55°C to +125°C – AD571S
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction



AD573

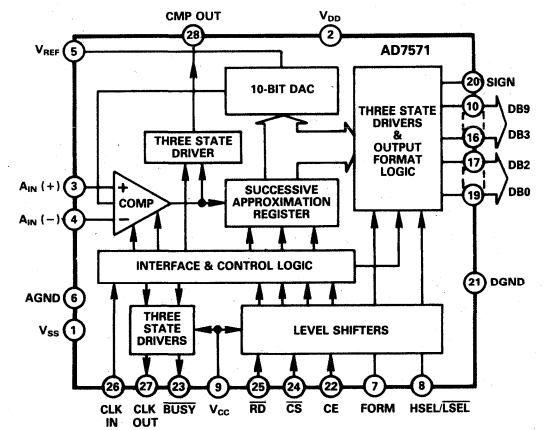
Complete 10-Bit A/D Converter with Reference, Clock and Comparator

Full 8- or 16-Bit Microprocessor Bus Interface
Fast Successive Approximation Conversion – 15μs
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies



AD575

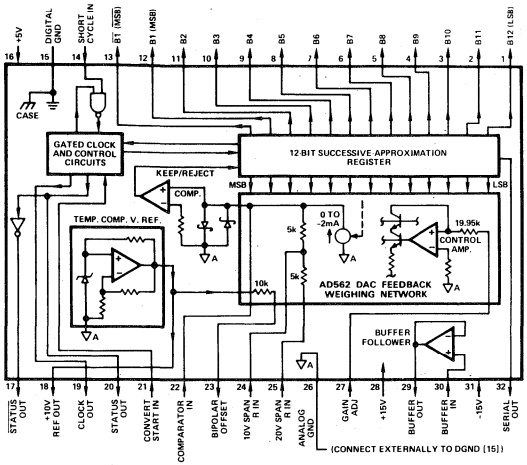
Complete 10-Bit A/D Converter with Reference Clock and Comparator Vol. I 10–67
Serial Output
Fast Successive Approximation Conversion – 20μs typ
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction



AD7571

10-Bit Plus Sign Resolution Vol. I 10–139
No Missed Codes Over Full Temperature Range
Conversion Time 80μs
Differential Analog Voltage Inputs, ±10V Range
Serial and Parallel Data Outputs
Easy Interface to Most Microprocessors
Internal Clock Oscillator
Single Supply Operation for Positive-Only Signals
Monolithic Construction

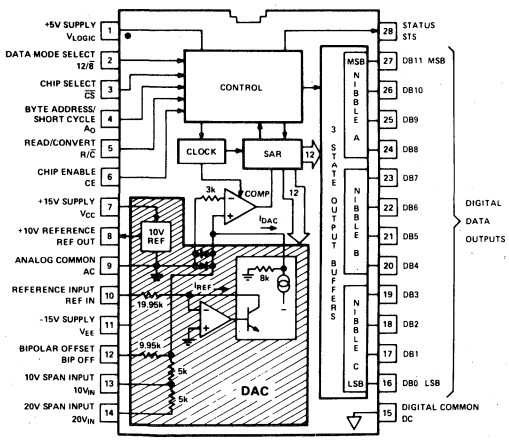
Selection Guide
Analog-to-Digital Converters
12-Bit A/D Converters



AD572

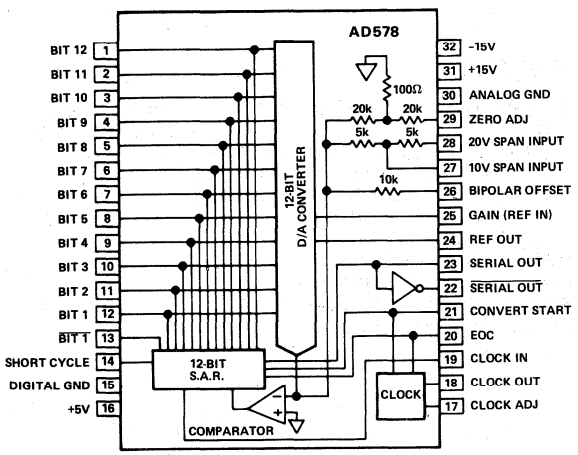
Page

True 12-Bit Operation: Max Nonlinearity $< \pm 0.012\%$ — Vol. I 10–39
Low Gain T.C.: $< \pm 15$ppm/°C (AD572B)
Low Power: 900mW
Fast Conversion Time: $<25\mu s$
Monotonic Feedback DAC Guarantees No Missing Codes



AD574A

Complete 12-Bit A/D Converter with Reference and Clock — Vol. I 10–55
Full 8- or 16-Bit Microprocessor Bus Interface
250ns Bus Access Time
Guaranteed Linearity Over Temperature
0 to +70°C – AD574AJ, AK, AL
−55°C to +125°C – AD574AS, AT, AU
No Missing Codes Over Temperature
Fast Successive Approximation Conversion – 25μs
Buried Zener Reference for Long-Term Stability and Low Gain T.C.
10ppm/°C max AD574AL
12.5ppm/°C max AD574AU
Low Profile 28-Pin Ceramic DIP
Low Power: 390mW



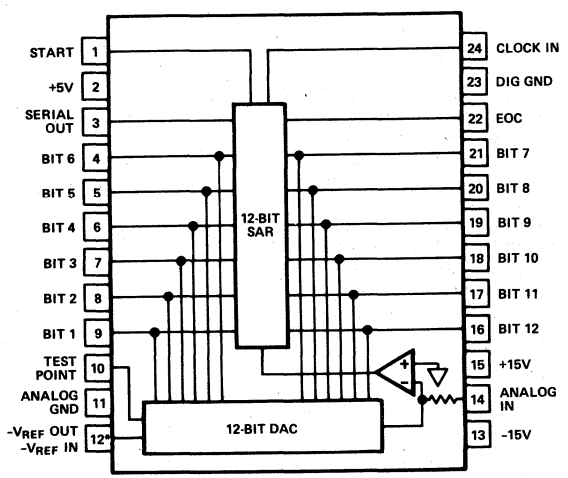
AD578

Page

Complete 12-Bit A/D Converter with Reference and Clock — Vol. I 10–73

Fast Conversion: 3μs (max)
Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max
Max Nonlinearity: <±0.012%
Low Power: 775mW
Hermetic Package Available
Positive-True Parallel or Serial Logic Outputs
Short Cycle Capability
Precision +10V Reference for External Applications
Adjustable Internal Clock
"Z" Models for ±12V Supplies

10

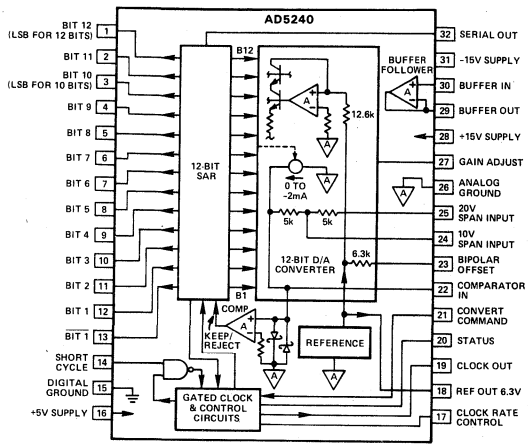


AD5200 SERIES

AD5200: 50μs Conversion Time — Vol. I 10–105
AD5210: 13μs Conversion Time

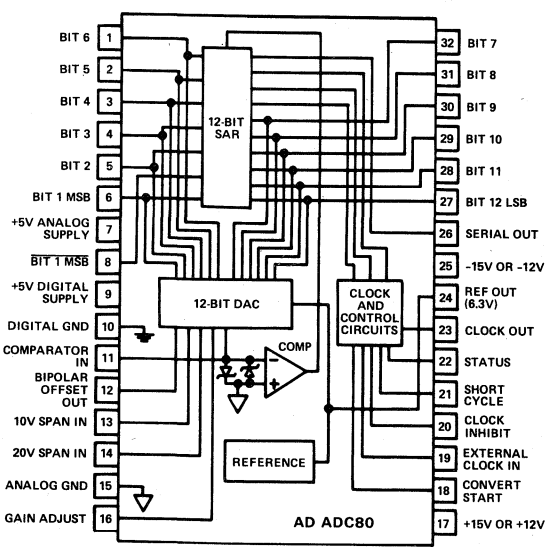
True 12-Bit Operation: ±1/2LSB max Nonlinearity
Totally Adjustment-Free
Guaranteed No Missing Codes Over the Specified Temperature Range
Hermetically-Sealed Package
Standard Temperature Range: +25°C to +85°C
Extended Temperature Range: −55°C to +125°C
Serial and Parallel Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count for High Reliability
Industry Standard Pin Out
Small 24-Pin DIP

Selection Guide
Analog-to-Digital Converters
12-Bit A/D Converters



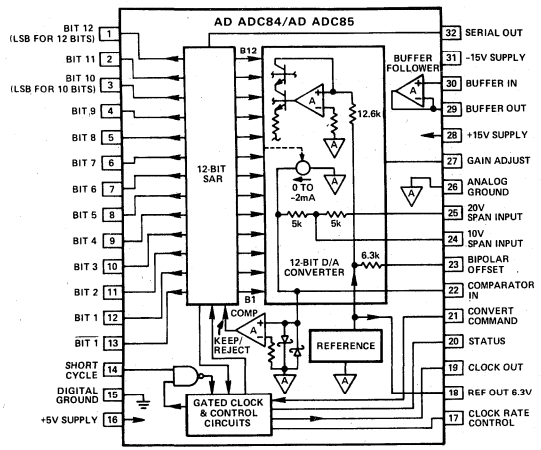
AD5240

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Fast Successive Approximation Conversion: 5μs**
- **Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C**
- **Max Nonlinearity: <±0.012%**
- **Low Power: 775mW Typical**
- **Hermetic Package Available**
- **Low Chip Count – High Reliability**
- **Pin Compatible with AD ADC84/AD ADC85**
- **"Z" Models for ±12V Supplies**



AD ADC80

- **True 12-Bit Operation: Max Nonlinearity ±0.012%**
- **Low Gain T.C.: ±30ppm/°C max**
- **Low Power: 800mW**
- **Fast Conversion Time: 25μs**
- **Precision 6.3V Reference for External Application**
- **Short-Cycle Capability**
- **Serial or Parallel Data Outputs**
- **Monolithic DAC with Scaling Resistors for Stability**
- **Low Chip Count – High Reliability**
- **Industry Standard Pin Out**
- **"Z" Models for ±12V Supplies**



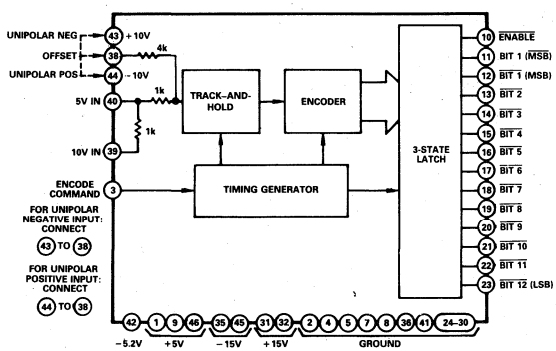
AD ADC84/AD ADC85

Page

Vol. I
10-191

Complete 12-Bit A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 10μs
Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
Max Nonlinearity: $< \pm 0.012\%$
Low Power: 880mW Typical
Hermetic Package Available
Low Chip Count – High Reliability
Industry Standard Pin Out
"Z" Models for ±12V Operation Available

10



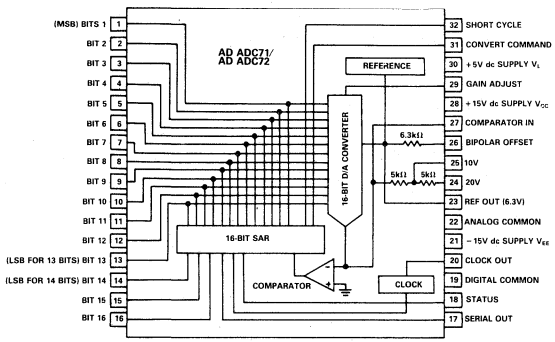
HAS-1201

Vol. I
10-205

12-Bit Resolution
1MHz Word Rate
T/H and Timing Circuits Included
Single Hybrid Package

APPLICATIONS
Radar Systems
Medical Instrumentation
Electro-Optics Systems
Test Systems

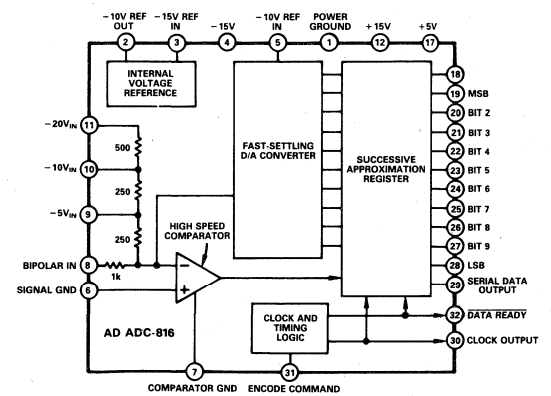
Selection Guide
Analog-to-Digital Converters
High Resolution A/D Converters



AD ADC71/AD ADC72

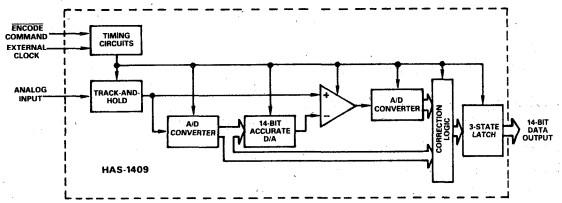
Page

Complete 16-Bit Converter with Reference and Clock — Vol. I 10–175
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 45μs (14 Bit)
Short Cycle Capability
Parallel or Serial Logic Outputs



AD ADC-816

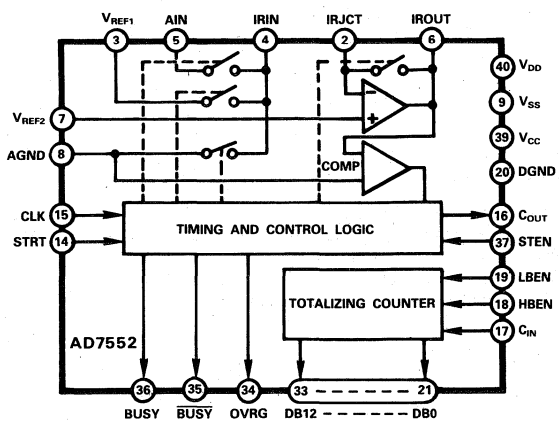
10-Bit Resolution — Vol. I 10–199
800ns Conversion Time
Six Input Ranges
Unipolar and Bipolar Operation



HAS-1409

14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP

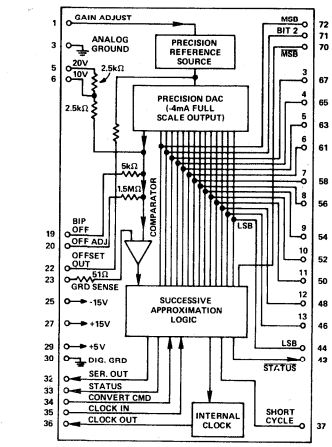
APPLICATIONS
FDM/TDM Transmultiplexers
CAT/NMR Scanners
PCM Systems
Digital Audio



AD7552

12-Bit Binary with Polarity and Overrange
Accuracy ±1LSB
Microprocessor Compatible
Ratiometric Operation
Low Power Dissipation

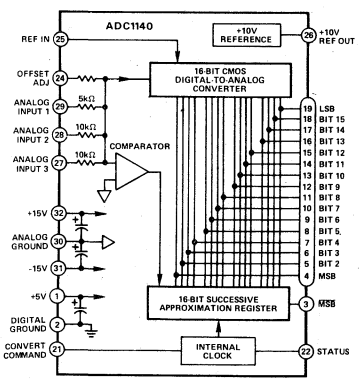
Selection Guide
Analog-to-Digital Converters
High Resolution A/D Converters



ADC1130/ADC1131

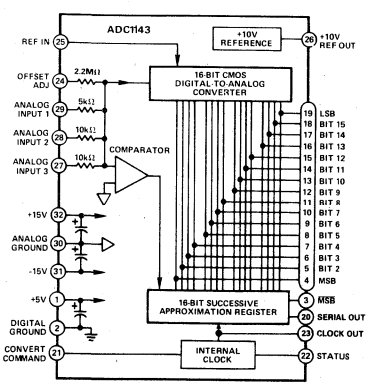
Page

14-Bit Resolution and Accuracy — Vol. II 11-27
Fast 12μs Conversion Time (ADC1131J/K)
Low 10ppm/°C Maximum Gain TC
User Choice of Input Range
No Missing Codes



ADC1140

Low Cost 16-Bit A/D Converter — Vol. II 11-31
Guaranteed Nonlinearity: ±0.003% FSR max
35μs Maximum Conversion Time
Small Size 2″ × 2″ × 0.4″
Wide Power Supply Operation: ±12V to ±17V



ADC1143

High Performance 16-Bit A/D Converter — Vol. II 11-35
Low Power Consumption:
- **175mW max, V_S = ±15V**
- **150mW max, V_S = ±12V**

Guaranteed Nonlinearity:
- **±0.006% FSR max (ADC1143J)**
- **±0.003% FSR max (ADC1143K)**

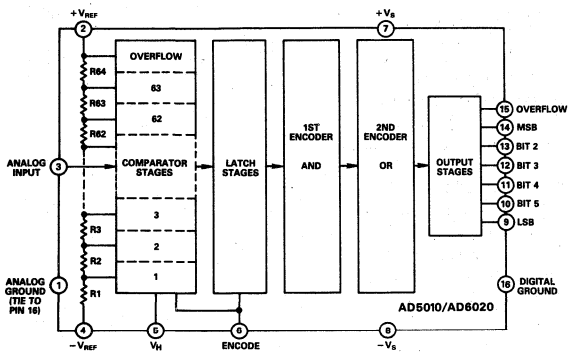
Guaranteed Differential Nonlinearity:
- **±0.006% FSR max (ADC1143J)**
- **±0.003% FSR max (ADC1143K)**

Low Differential Nonlinearity T.C.:
- **±2ppm/°C max (ADC1143J)**
- **±1ppm/°C max (ADC1143K)**

Fast Conversion Time:
- **70μs max (ADC1143J)**
- **100μs max (ADC1143K)**

Wide Power Supply Operation:
- **V_S = ±11.4V to ±18.0V**
- **V_D = +3.0V to +18.0V**

Video A/D Converters

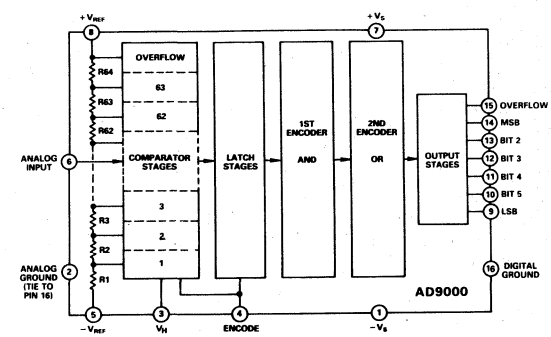


AD5010/AD6020

Scan Frequency to 100MHz (AD5010KD)
Low 450mW Power Dissipation
±1/4LSB Linearity
ECL Logic Compatible
No Sample & Hold Required
Overflow Output for Extended Resolution

APPLICATIONS
Video Data Conversion
High Speed Data Acquisition
Radar/Sonar Data Conversion

10



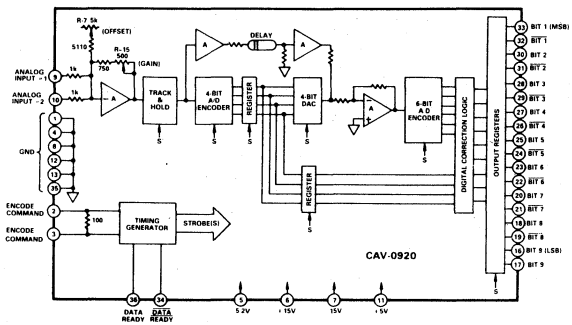
9000 SERIES

6-Bit, 75MHz Minimum Word Rates
No T/H Required
−55°C to +125°C Temperature
Overflow Bit for Cascading Units

APPLICATIONS
Image Processing
Video Digitizing
Radar Digitizing
Military Systems

Selection Guide
Analog-to-Digital Converters

Video A/D Converters



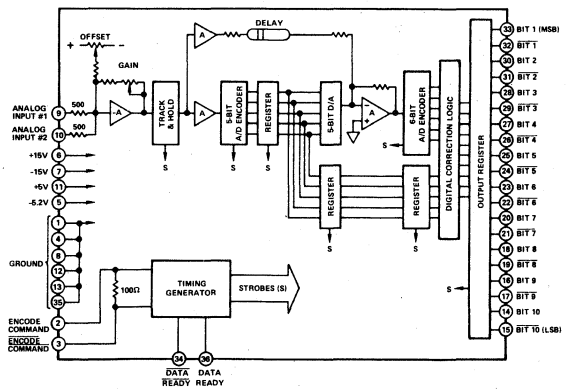
CAV-0920

Page

Vol. II
11–39

9-Bit Resolution
20MHz Word Rate
Single 35-In^2 PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Television Digitizing
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis

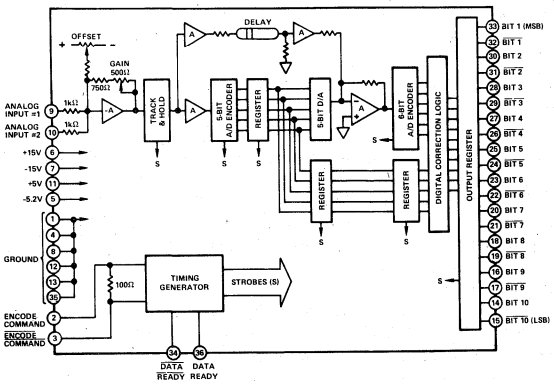


CAV-1040

Vol. II
11–43

10-Bit Resolution
40MHz Word Rate
Single 35-In^2 PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis

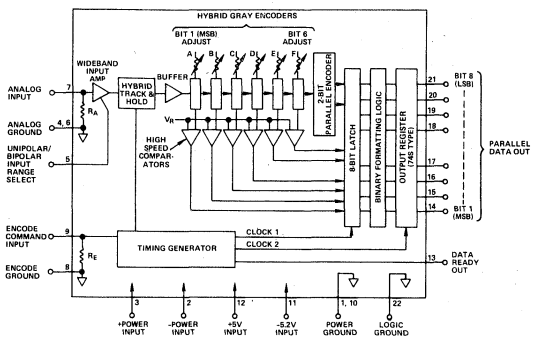


CAV-1210

12-Bit Resolution
10MHz Word Rate
Single 35-In^2 PC Board
ECL Compatible
No External Circuits Required

APPLICATIONS
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis

Selection Guide
Analog-to-Digital Converters
Video A/D Converters



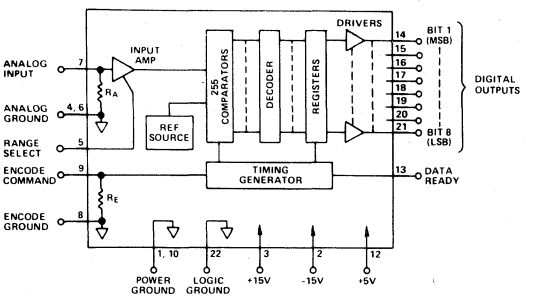
MATV-0811/MATV-0816

MATV-0811: 11MHz Word Rates
MATV 0816: 16MHz Word Rates

Page

8-Bit Accuracy – Guaranteed Monotonic Vol. II
Most Economical Video A/D 11-57
Smallest Available Complete A/D – 5.5″ × 4.38″ × 0.85″
Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

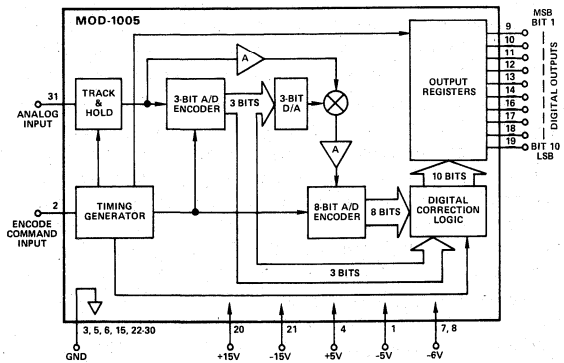
APPLICATIONS
Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
Video Time Base Correction and Frame Synchronization
Radar Signal Processing
Real Time Transient and Continuous Spectrum Analysis



MATV-0820

8-Bit Accuracy – Guaranteed Monotonic Vol. II
Ultra-High Speed – dc to 20MHz Word Rates 11-57
Most Economical Video A/D
Smallest Available Complete A/D – 5.5″ × 4.38″ × 0.85″
Self Contained – Includes Input Buffer, Encoder, Reference, Timing, and Buffered Parallel Output

APPLICATIONS
Digitize Color Television at Up to Three or Four Times NTSC or PAL Color Subcarrier Frequencies
Video Time Base Correction and Frame Synchronization
Radar Signal Processing
Real Time Transient and Continuous Spectrum Analysis

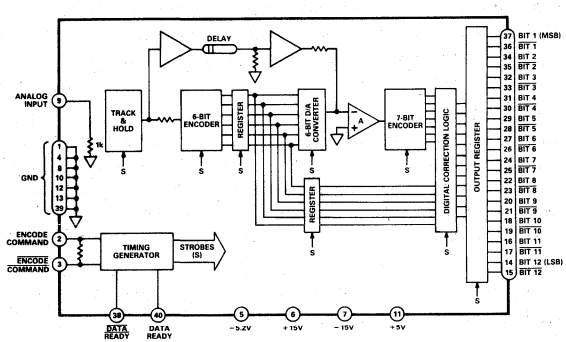


MOD-1005

Page

10 Bits @ 5MHz Word Rate Vol. II
One-27 Sq. In. PC Board 11-61
Built-In Track-and-Hold – 25ps Aperture Uncertainty
20MHz Analog Input Bandwidth
TTL Compatible
Low (10-Watt) Power Dissipation
Signal-to-Noise Ratio Greater Than 58dB
Noise Power Ratio Greater Than 49dB
Completely Repairable

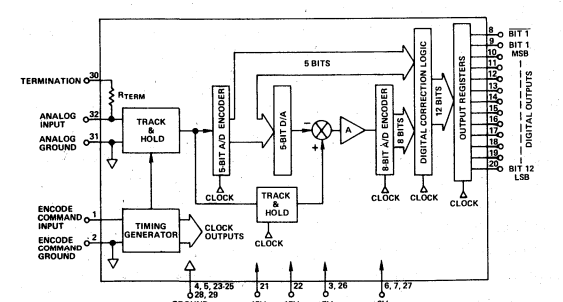
APPLICATIONS
Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
High Resolution TV



MOD-1020

10 Bits @ 20MHz Word Rates Vol. II
One-35 Sq. In. PC Board 11-65
Built-In Track-and-Hold – 25ps Aperture
15MHz Large-Signal Input Bandwidth
ECL Compatible
Signal-to-Noise Ratio Greater Than 56dB
Noise Power Ratio Greater Than 45dB

APPLICATIONS
Television Digitizing
Radar Digitizing
Medical Instrumentation
Digital Communications
Spectrum Analysis
Sonar Digitizing



MOD-1205

12 Bits @ 5MHz Word Rate Vol. II
One-27 Sq. In. PC Board 11-69
Built-In Track-and-Hold – 25ps Aperture Uncertainty
15MHz Analog Input Bandwidth
TTL Compatible
Low (13-Watt) Power Dissipation
Signal-to-Noise Ratio Greater Than 66dB
Noise Power Ratio Greater Than 56dB
Completely Repariable

APPLICATIONS
Radar Digitizing
Digital Communications
Real Time Spectrum Analysis
Signature Analysis

Orientation
Analog-to-Digital Converters

FACTORS IN CHOOSING AN A/D CONVERTER

In the two volumes of this catalog, there are listed some 34 different families of analog-to-digital converters (ADCs). If one were to consider all the variations, there would be considerably more than 92 different types to choose among. The reason for so many different types is the number of degrees of freedom in selection—technological, functional, performance, and package. Complete information on converters may be found in the 250-page book, *Analog-Digital Conversion Notes*, published by Analog Devices and available for $5.95 from P.O. Box 796, Norwood, MA 02062.

FUNCTIONAL CHARACTERISTICS

Block diagrams illustrating the various conversion techniques appear on individual data sheets.

The moderate-speed converters described in this catalog (<1MHz) employ two fundamental techniques—*successive approximations*, for moderate-to-high resolution at moderate-to-high speed, and *integration*, for high resolution at modest speeds. The AD574A and ADC1143 are examples of the former, the AD7552 the latter.

Like a chemist's balance with binary weights (1/2, 1/4, 1/8, etc.), the *successive-approximation* converter compares the unknown input with sums of accurately-known binary fractions of full scale, starting with the largest (2^{-1}), and rejecting any that change the comparator's state ("tip the scale"). At the end of conversion (EOC), the output of the converter is a digital word, representing the ratio of the input to full scale by a fractional-binary code.

Integrating types count pulses for a period proportional to the input. Most-frequently used are *dual slope* types, which count off the period required for the integral of the reference to become equal to the average value of the input (over a fixed period). Integrating types can be made insensitive to drift by storing errors during an error-correcting cycle and subtracting them during the input-measuring cycle. This correction can be performed in analog fashion, using capacitance for storage, or digitally—using the information stored in a counter for correction (AD7552).

The video converters described here (MATV, MOD-1205, etc.) employ two basic encoding techniques: simultaneous, or *flash* conversion, and serial-Gray-Code conversion. High resolution and high speed are obtained by *subranging*, i.e., by performing an n-bit conversion in two steps; Analog Devices has perfected a form of subranging, known as DSC—*digitally corrected subranging*—which permits accurate resolutions of 12 bits and more.*

In *flash* conversion, the analog signal is compared against $2^n - 1$ graded voltage levels, using as many comparators, and the comparator output logic levels are processed by a priority encoder, which converts the "thermometer" output to a binary (or Gray) code. Since the whole conversion occurs essentially simultaneously, it is the fastest means of conversion, but it requires many accurate comparators and large numbers of gates.

In *serial*-analog-parallel-digital conversion, there are a number of cascaded stages, each having a gain of +2 for signals less than one-half the reference, and a gain of −2 for signals between one-half the reference and full scale. At each stage, a decision is made as to whether the signal is larger (1) or smaller (0) than one-half the reference; the stage's analog output becomes the input to the next stage. The complete time for one conversion is determined by the propagation delay of the analog signal through all stages; however, since the decision of each stage can be latched as soon as the stage has settled (and a new conversion can, in principle, be started as soon as the first bit has been latched), the rate at which conversions come out of the pipeline is considerably faster than the time for one sample to go through the conversion process. Though fast, this process is difficult to implement accurately for more than a few bits, because of the compounding of gain (hence errors).

A *subranging* converter digitizes to a group of more-significant bits, and stores them in a latch. A fast, very-high-accuracy D/A converter converts them to an analog signal, which is then subtracted from the input. The difference, or residue, is amplified and digitized, and (in DCS) the result is combined digitally in such a way as to correct for mid-scale conversion errors.

Whatever the technique, these A/D converters comprise several essential functions: an analog section, a digital data-generating section, data outputs, and digital controls.

Analog Section

This section requires a reference, one or more high-gain comparators, and either a D/A converter (successive approximations) or a controllable integrator. The reference may be internal or external, fixed or variable, and of a specified polarity/sense in relation to the analog input. In ratiometric conversion, the reference is usually external and variable.

In successive-approximation converters the comparator is generally used in the *current-summing* mode; that is, the current output of the DAC is summed with the current developed in the DAC's "feedback resistor" by the input voltage (of opposite polarity), and the balancing action of the converter tends to bring the summing junction towards a voltage null (much like that of an op amp) at the end of conversion. The typical DAC feedback options, when applied in an ADC, provide input-scaling choices. When the bipolar-offset connection is jumpered to the summing point, input signals of both polarities can be handled. The current-switching action of the DAC, at the typically fast clock-rates used in successive-approximation converters, can disturb the output of the analog signal source, especially if it is a slow high-precision op amp. In such cases, buffering may be necessary.

*A considerable amount of useful information about the differences between video conversion and moderate-speed conversion can be found in the article "Very High Speed Data Acquisition," by Ed Graves, in *Analog Dialogue* 13-2, available upon request.

Digital Data-Generating Section
In successive-approximation types, this section consists of a discrete or integrated successive-approximations register (SAR), its controls, and inputs from the comparator and clock (which is on-board, but in many cases permits external clock pulses, frequency adjustment, and/or control). In integrating types, this section consists of the clock-pulse generator, the counter(s), the input from the comparator, and the associated controls. Often, provisions are made for the pulse-train to be jumpered to the counter externally, so that the pulse train can be operated on externally, or can transmit its train of pulses to a remote counter. In a few types there are no on-board counters or registers; the pulse train, magnitude, overrange, and control terminals are intended to communicate with external counters and registers.

Data Outputs
Factors to consider here include coding, resolution, overrange information, levels, format, validity, and timing. *Coding* is usually binary, including jumper-connected offset-binary and/or two's complement for bipolar input signals. For some types, BCD is available, with sign-magnitude for bipolar inputs. Output coding specs should always be checked for digital polarity (positive- or negative-true) of both magnitude and sign information. The *resolution* (number of output bits) must be sufficient for the application; in addition, the specifications must be checked to ascertain that not only will all 2^n (binary) output codes be present (no missing codes), but they must all be present at any temperature in the operating range and related to the input with sufficient accuracy. Integrating types generally have no problems with missing codes (except sometimes at zero, with sign-magnitude coding); nevertheless, nonlinear integration can cause the conversion relationship to become nonlinear. Successive-approximation types have no way of determining *overrange;* they simply fill up. However, counter types roll over and put out a carry flag to signal overrange.

The *data levels* available at the converter output must be checked (TTL, low-voltage CMOS, high-voltage CMOS, ECL), as must the load-driving capability and fanout, and the supply conditions under which appropriate output levels will be furnished. The available choice of output *formats* must also be as desired—parallel, serial, byte-serial, and/or pulse-train. If the converter is intended to communicate directly with an 8-bit data bus, the output should have three-state capability, and parallel outputs must be enabled in bytes of 8 or fewer lines (AD573, AD574A). If the output is serial, it is usually NRZ (non-return-to-zero) and should be accompanied by a set of synchronized clock-pulses.

A *status* (or *busy* or *EOC*) output changes state to indicate when the data becomes *valid*. The exact nature of this transition should be specified—polarity, timing, levels, etc. For serial data, the exact relationship between the data and the synchronizing clock should be specified, to indicate when each bit becomes valid, and for how long. In general, the *timing* of the whole conversion process must be clearly understood, especially if high speeds are necessary, either for conversion, or for communication with a processor (or both). The timing diagrams on specification sheets are usually accompanied by adequate descriptions of the conversion process and specifications of the critical interface parameters.

Controls
The functions, action (levels or edges), polarity, and timing of all control inputs and outputs should be clearly understood, as well as their loading characteristics and dependence on the supply. In addition to the essential *start-conversion-command* input and a *status* output, various control commands may be available, such as *clock inhibit, high (low)-byte enable, status enable*, and—for speeding up conversion at the cost of resolution in successive-approximation converters—*short-cycle.*

Power Supplies
Appropriate power supplies should be made available, considering the logic levels and analog input signals to be employed in the system. The appropriate degree of power-supply stability to meet the accuracy specifications should be provided. Any recommended external protection circuitry should be planned for. In many cases, separate analog and digital grounds are required; ground wiring should follow best practice to minimize digital interference with high-accuracy analog signals, while ensuring that a connection between grounds can always exist at one point, even if the "mecca" point is inadvertently unplugged from the system.

Application Checklist
The designer will generally require specific information in the following categories, before proceeding to the selection process:

- Accurate description of input and output
  1. analog signal range and source or load impedance
  2. digital code needed — binary, offset binary, 2's complement, BCD, etc.
  3. logic level system, i.e., TTL/DTL compatible
- What is the needed data throughput rate?
- What are the control interface details?
- What does the system error budget allow for the converter?
- What are environmental conditions — temperature range, time, supply voltage — over which the converter should operate to the desired accuracy?

For A/D converters, the following considerations are typical.

- What is the analog input voltage range, and to what resolution must the signal be measured?

- What is the requirement for linearity error (or relative accuracy error)?
- To what extent must the various sources of error be minimized as environmental temperature changes?
- How much time can be allowed in the system for each complete conversion? What aperture uncertainty and acquisition time are needed for the sample-hold?
- How stable is the system power supply? What errors will result from power supply terminal voltage variations of this order?
- Can the system tolerate missed codes under any conditions?
- What is the character of the input signal? Is it noisy, sampled, filtered, rapidly-varying, slowly-varying? What kind of pre-processing is to be (or can be) done that will affect the choice (and cost) of the converter? Is aliasing a potential problem?

SPECIFICATIONS & TERMS

Definitions of performance specifications, and related information, are to be found on the following pages, in alphabetical order.*

Accuracy, Absolute

The error of an A/D converter at a given output code is the difference between the theoretical and the actual analog input voltages required to produce that code. Since the code can be produced by any analog voltage in a finite band (see Quantizing Uncertainty), the "input required to produce that code" is defined as the midpoint of the band of inputs that will produce the code. For example, if 5 volts (±1.2mV) will theoretically produce a 12-bit half-scale code of 100000000000, then a converter for which any voltage from 4.997V to 4.999V will produce that code will have absolute error of 1/2(4.997 + 4.999) – 5 volts = –2mV.

Absolute error comprises gain error, zero error, and nonlinearity, together with noise, Absolute-accuracy measurements should be made under a set of standard conditions with sources and meters traceable to an internationally accepted standard.

Accuracy, Relative

Relative accuracy error, expressed in %, ppm, or fractions of an LSB, is the deviation of the analog value at any code (relative to the full analog range of the device transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range (FSR) has been calibrated.

Since the discrete points on the theoretical transfer characteristic lie on a straight line, this deviation can also be interpreted as a measure of nonlinearity (see Linearity).

The "discrete points" of an A/D transfer characteristic are the midpoints of the quantization bands at each code (see Accuracy, Absolute).

Aperture Time

This is the interval between the application of the *hold* command to a sample/track-hold and the actual opening of the switch. The aperture time consists of a delay (which depends on the logic and the switching device—50ns for SHA1144) and an uncertainty (due to jitter—20ps max rms for HTS-0025). When a sample-hold is used in an application where timing is critical, the timing of the hold command can be advanced to compensate for the known component of aperture delay. The jitter, however, imposes the ultimate limitation on timing accuracy. When a sample-hold is used with an ADC, the timing uncertainty of the conversion process is reduced by the ratio of aperture jitter to the conversion time, i.e., the maximum frequency which can be handled with less than 1LSB error due to timing is $2^{-n}/(\pi\,\tau_{au})$ instead of $2^{-n}/(\pi\,\tau_c)$, where τ_{au} is the aperture uncertainty and τ_c is the conversion time.

Common Mode Rejection (CMR)

The ability of a device to reject the effect of voltage applied to both input terminals simultaneously. Usually expressed as the log of a "common-mode rejection ratio," e.g., 1,000,000:1 (CMRR) or 120dB (CMR). A CMRR of 1,000,000 to 1 means that a 1V common-mode voltage passes through the amplifier as through it were a differential signal of one microvolt at the input.

Conversion Time and Conversion Rate

The time required for a complete measurement by an ADC is called *conversion time*. For most converters (assuming no significant additional systemic delays), this is identical to the inverse of *conversion rate*. However, in some high-speed converters, because of pipelining, new conversions are initiated before the results of prior conversions have been determined; thus, for example, the MOD-1205 can provide 12-bit output data at a 5MHz word rate (200ns/conversion), even though the time for any one conversion, from start to finish, is two clock periods plus 275ns, or 675ns, at 5MHz.

Dual-Slope Converter

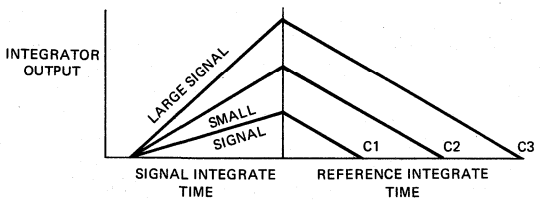
An integrating analog-to-digital converter in which the unknown signal is converted to a proportional time interval, which is then measured digitally. This is done by integrating the unknown for a predetermined time. Then a reference input is switched to the integrator, and integrates "down" from the level determined by the unknown until a "zero" level is reached. The time for the second integration process is proportional to the average of the unknown signal level over the predetermined integrating period. A digital time-interval meter (i.e., counter) is generally used as the output indicator.

*For video converters, there are a number of additional application-oriented specifications pertaining to the device's use in a system (e.g., *noise power ratio*, *differential phase*, *differential gain*, *signal-to-noise ratio*). Some useful references for understanding such specifications can be found in the following publications, available from Analog Devices, Computer Labs Division, 7810 Success Road, Greensboro, NC 27409.

Kester, W. A., "PCM Signal Codecs for Video Applications", *SMPTE Journal*, Volume 88, November 1979, pp 770-778.

Pratt, W. J., "Test A/D Converters Digitally", *Electronic Design*, December 6, 1975

Smith, B.F. and Pratt, W.J., "Understanding High-Speed A/D Converter Specifications", Computer Labs, 1974



Feedthrough
Undesirable signal-coupling around switches or other devices that are supposed to be turned off or provide isolation, e.g., *feedthrough error* in a multiplexer. It is variously specified in %, ppm, fractions of 1 LSB, or fractions of 1 volt, with a given set of inputs, at a specified frequency.

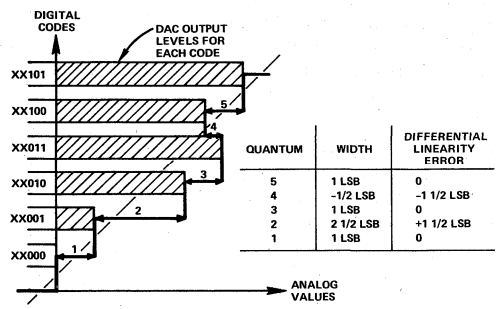
"Flash" Converter
A converter in which all the bit choices are made at the same time. It requires $2^n - 1$ voltage-divider taps and comparators, and a comparable amount of priority encoding logic. An extremely fast scheme, it requires large numbers of precision components. Flash converters are often used for partial conversions in *subranging converters*.

Gain Adjustment
The "gain" of a converter is that analog scale factor setting that provides the nominal conversion relationship, e.g., 10V full scale, in a fixed-reference converter, or 100% of full-scale in a ratiometric converter. Gain- and zero-adjustment principles are discussed under *zero*.

Least Significant Bit (LSB)
In a system in which a numerical magnitude is represented by a series of binary (i.e., two-valued) digits, the "least significant bit" is that digit (or "bit") that carries the smallest value or weight. For example, in the natural binary number 1101 (decimal 13, or $2^3 + 2^2 + 0 + 2^0$), the rightmost "1" is the LSB. Its analog weight, relative to full scale, is 2^{-n}, where n is the number of binary digits. It represents the smallest change that can be resolved by an n-bit converter.

Linearity Error
Linearity error of a converter, expressed in percent or parts-per-million of full-scale range, or fractions of a least-significant bit, is the deviation of the analog values from a straight line, in a plot of the measured conversion relationship. The straight line can be either a "best straight line," determined empirically by manipulation of the gain and/or offset to equalize maximum positive and negative deviations of the actual transfer characteristic from this straight line; or, it can be a straight line passing through the end points of the transfer characteristic after they have been calibrated. Sometimes referred to as "end-point" nonlinearity, the latter is both a more conservative measure and is much easier to verify in actual practice. "End-point" nonlinearity is similar to relative accuracy error (see Accuracy, Relative). Linearity has two components—*differential* and *integral* nonlinearity.

Linearity, Differential and Integral
A digital output code should correspond to a quantum of analog input values exactly 1 LSB in width (2^{-n} of full scale, for an n-bit converter). Any deviation of the measured "step" from the ideal width is called Differential Nonlinearity. It is an important specification, because a differential nonlinearity error greater than 1 LSB can lead to nonmonotonic behavior of of a D/A converter, and missed codes in an A/D converter employing such a DAC. A flagrant example of differential nonlinearity is shown here.



QUANTUM	WIDTH	DIFFERENTIAL LINEARITY ERROR
5	1 LSB	0
4	-1/2 LSB	-1 1/2 LSB
3	1 LSB	0
2	2 1/2 LSB	+1 1/2 LSB
1	1 LSB	0

In the illustration, the horizontal bars represent the measured DAC output values corresponding to 6 adjacent digital codes. The DAC is nonlinear, in that the next-least-significant bit (XX010) is 1½ LSB too large. Thus, instead of the five quanta, or steps, being all equal (= 1 LSB), quantum 2 is 2½ LSB and quantum 4 is -½ LSB. The differential linearity error, the difference between the actual quantum width and the ideal 1 LSB, is +1½ LSB for quantum 2 and -1½ LSB for quantum 4.

When this DAC is used in successive-approximations conversion, it will lead to a missed code. Analog inputs slightly larger than the value of XX100 will be converted to XX100, and analog inputs slightly less than the value of XX100 will be converted to XX010. The code XX011 will not exist; it will be a *missed code*.

Often, instead of a maximum differential nonlinearity specification, there will be a simple specification of "no missed codes", which implies a differential nonlinearity less than 1 LSB.

While differential nonlinearity deals with errors in step size, *integral nonlinearity* has to do with deviations of the overall shape of the conversion response. Even converters that are not subject to differential linearity errors (e.g., integrating types) have integral linearity (sometimes just "linearity") errors.

Power-Supply Sensitivity
The sensitivity of a converter to dc changes in power-supply voltages is normally expressed in terms of percentage change in analog input value (or fractions of the analog equivalent of 1 LSB), corresponding to a given code, for a 1% dc change

in the power supply, e.g., 0.05%/%ΔV_S). Power-supply sensitivity may also be expressed in relation to a specified dc shift of the supply voltage. High-accuracy ADCs intended for battery operation require excellent rejection of large supply-variations.

Quad-Slope Converter
This is an integrating analog-to-digital converter that goes through two cycles of *dual-slope* conversion, once with zero input and once with the analog input being measured. The errors determined during the first cycle are subtracted digitally from the result in the second cycle. The scheme results in an extremely accurate converter. For example, the 13-bit single-chip AD7550 is a CMOS quad-slope A/D converter with typical tempcos (gain and zero temperature coefficients) of 1ppm/°C.

Quantizing Uncertainty (or "Error")
The analog continuum is partitioned into 2^n discrete ranges for n-bit conversion. All analog values within a given range are represented by the same digital code, usually assigned to the nominal midrange value. There is, therefore, an inherent quantization uncertainty of ±½ LSB, in addition to the actual conversion errors. In integrating converters, this "error" is often expressed as "±1 count."

Ratiometric Converter
The output of an A/D converter is a digital number proportional to the ratio of (some measure of) the input to a reference. Most requirements for conversions call for an absolute measurement, i.e., against a fixed reference. In some cases, where the measurement is affected by a changing reference voltage (e.g., the voltage applied to a bridge), it is advantageous to use that same reference as the reference for the conversion, to eliminate the effect of variation. Ratiometric conversion can also serve as a substitute for analog signal division (where the denominator changes but little during the conversion).

Stability
Stability of a converter, usually applies to the insensitivity of its characteristics with time, temperature, etc. All measurements of stability are difficult and time consuming, but stability vs. temperature is sufficiently critical in most applications to warrant universal inclusion in tables of specifications (see "Temperature Coefficients").

Subranging Converters
In this type of converter, an extremely fast conversion produces the most-significant portion of the output word. This portion is converted back to analog with a fast high-accuracy D/A converter and subtracted from the input. The resulting residue is converted to digital at high speed and combined with the results of the earlier conversion to form the output word. In *digitally corrected subranging* (DCS), the two bytes are combined in a manner that corrects for the error of the LSB of the most-significant byte. For example, using 8-bit and 5-bit conversion, and this proprietary technique, a full-accuracy high-speed 12-bit converter can be built.

Successive Approximations
Successive approximations is a high speed method of comparing an unknown against a group of weighted references. The operation of a successive approximations A/D converter is generally similar to the orderly weighing of an unknown quantity on a precision chemical balance, using a set of weights such as: 1 gram, 1/2 gram, 1/4 gram, 1/8 gram, 1/16 gram, etc. The weights are tried in order, starting with the largest. Any weight that tips the scale is removed. At the end of the process, the sum of the weights remaining on the scale will be within one LSB of the actual weight (±½ LSB, if the scale is properly biased – see *zero*).

Temperature Coefficients
In general, temperature instabilities are expressed in %/°C, ppm/°C, as fractions of 1 LSB/°C, or as a change in a parameter over a specified temperature range. Measurements are usually made at room temperature and at the extremes of the specified range, and the temperature coefficient (tempco, T.C.) is defined as the change in the parameter, divided by the corresponding temperature change. Parameters of interest include *gain, linearity, offset* (bipolar), and *zero.* The last three are expressed in % or ppm of full-scale range per Celsius degree.

Gain Tempco: Two factors principally affect converter gain instability with temperature:

a) In fixed-reference converters, the reference source will vary with temperature. For example, the tempco of an AD581L is typically 5ppm/°C.
b) The ratiometric circuitry has a sensitivity to temperature.

Linearity Tempco: Sensitivity of linearity to temperature over the specified range. To avoid missed codes, it is sufficient that the differential nonlinearity error be less than 1 LSB at any temperature in the range of interest. The *differential nonlinearity temperature coefficient* may be expressed as a ratio, as a maximum change over a specified temperature range, and/or implied by a statement that there are no missed codes when operating within a specified temperature range.

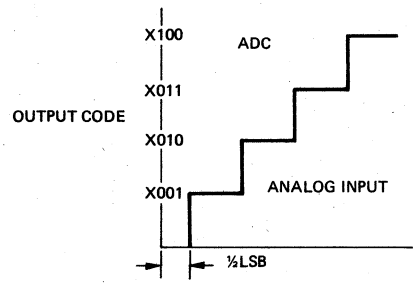
Offset Tempco The temperature coefficient of the all-DAC-switches-off (minus full-scale) point, of a bipolar successive-approximations converter, is dependent on three variables:

1) The tempco of the reference source
2) The voltage stability of the input buffer and the comparator
3) The tracking capability of the bipolar-offset resistors and the gain resistors.

Unipolar Zero The zero tempco of an ADC is dependent only on the zero stability of the integrator and/or the input buffer and the comparator. It may be expressed in μV/°C, or in percent or ppm of full-scale per degree C.

Zero- and Gain-Adjustment Principles

The zero adjustment of a unipolar ADC is set so that the transition from all-bits-off to LSB-on occurs at $\frac{1}{2} \times 2^{-n}$ of nominal full-scale. The gain is set for the final transition to all-bits-on to occur at F.S. $(1 - \frac{3}{2} \times 2^{-n})$. The "zero" of an offset-binary bipolar ADC is set so that the first transition occurs at -F.S. $(1 - 2^{-n})$ and the last transition at +F.S. $(1 - 3 \times 2^{-n})$. The data sheet instructions should be followed.



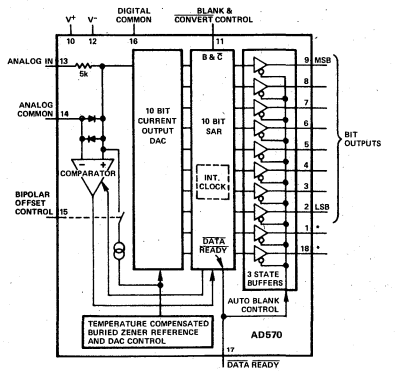
Low Cost, Complete IC 8-Bit A-to-D Converter

AD570*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
0 to +70°C – AD570J
-55°C to +125°C – AD570S
Digital Multiplexing – 3 State Outputs
18-Pin DIP
Low Cost Monolithic Construction

AD570 FUNCTIONAL BLOCK DIAGRAM



18-PIN DUAL IN LINE PACKAGE

PRODUCT DESCRIPTION

The AD570 is an 8-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 25μs.

The AD570 incorporates the most advanced integrated circuit design and processing technology available today. I^2L (integrated injection logic) processing in the fabrication of the SAR function along with laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) and a temperature compensated, subsurface Zener reference insures full 8-bit accuracy at low cost.

Operating on supplies of +5V and -15V, the AD570 will accept analog inputs of 0 to +10V unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD570 executes a true 8-bit conversion with no missing codes in approximately 25μs.

The AD570 is available in two versions; the AD570J is specified for the 0 to 70°C temperature range, the AD570S for -55°C to +125°C. Both guarantee full 8-bit accuracy and no missing codes over their respective temperature ranges. The AD570J is also offered in an 18-pin plastic DIP.

*Protected by Patent Nos. 3940760, 4213806 and 4136349.

PRODUCT HIGHLIGHTS

1. The AD570 is a complete 8-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.8% (2LSB of 8 bits) is achieved without external trims.
2. The AD570 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD570 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V supplies. The device will also operate with a -12V supply.

10

SPECIFICATIONS (T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD570J Min	AD570J Typ	AD570J Max	AD570S Min	AD570S Typ	AD570S Max	Units
RESOLUTION[1]		8			8		Bits
RELATIVE ACCURACY, T_A[1,2,3]			±1/2			±1/2	LSB
T_{min} to T_{max}			±1/2			±1/2	LSB
FULL SCALE CALIBRATION[3,4]		±2			±2		LSB
UNIPOLAR OFFSET[3]			±1/2			±1/2	LSB
BIPOLAR OFFSET[3]			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY, T_A		8		8			Bits
T_{min} to T_{max}		8		8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS[3]							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full Scale Calibration[2]			±2			±2	LSB
POWER SUPPLY REJECTION[3]							
Positive Supply							
+4.5≤V+≤+5.5V			±2			±2	LSB
Negative Supply							
−16.00V≤V−≤−13.5V			±2			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			mA
Output Source Current[6]							
(V_{OUT} = 2.4V max, T_{min} to T_{max})	**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**	μA
LOGIC INPUTS							
Input Current			**±40**			**±40**	μA
Logic "1"	**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**	V
CONVERSION TIME, T_A and							
T_{min} to T_{max}	15	25	40	15	25	40	μs
POWER SUPPLY							
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+7.0**	V
V−	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	V
OPERATING CURRENT							
V+		2	**10**		2	**10**	mA
V−		9	**15**		9	**15**	mA
PACKAGE[7]							
Ceramic DIP		N18A			N18A		mA
Plastic DIP		D18A			D18A		mA

NOTES

[1]The AD570 is selected version of the AD571 10-bit A to D converter. As such, some devices may exhibit 9 or 10 bits of relative accuracy or resolution, but that is neither tested nor guaranteed. Only TTL logic inputs should be connected to pins 1 and 18 (or no connection made) or damage may result.

[2]Relative accuracy is defined as the deviation of the code transition points from the ideal transer point on straight line from the zero to the full scale of the device.

[3]Specifications given in LSB's refer to the weight of a least significant bit at the 8-bit level, which is 0.39% of full scale.

[4]Full scale calibration is guaranteed trimmable to zero with an external 200Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB or 9.961 volts.

[5]Full Scale Calibration Temperature Coefficient includes effects of unipolar offset drift as well as gain drift.

[6]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[7]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . .0 to +7V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . 0 to V+
Power Dissipation. 800mW

AD570 ORDERING GUIDE

Model	Package Number[1]	Temperature Range
AD570JN	18-Pin Plastic DIP (N18A)	0 to +70°C
AD570JD	18-Pin Ceramic DIP (D18A)	0 to +70°C
AD570SD	18-Pin Ceramic DIP (D18A)	-55°C to +125°C

[1] See Section 19 for package outline information.

CONNECTING THE AD570 FOR STANDARD OPERATION

The AD570 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 1.

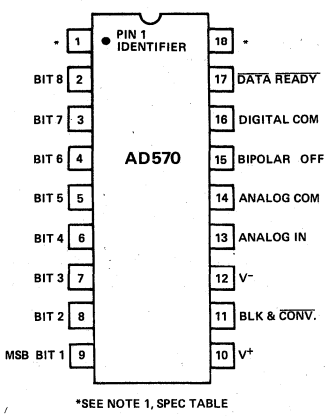


Figure 1. AD570 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.961 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be about ±2LSB or ±0.8%. If a more precise calibration is desired a 200Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 11111110 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 40.00mV), a 50Ω resistor in series with a 200Ω trimmer (or a 500Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

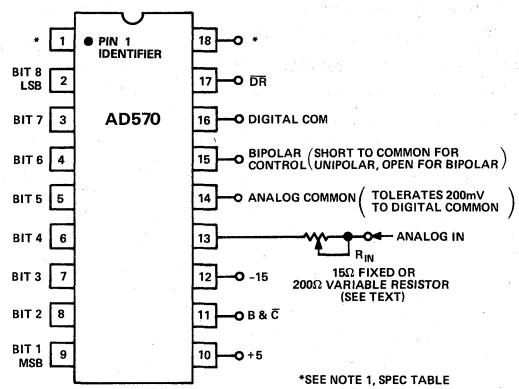


Figure 2. Standard AD570 Connections

BIPOLAR CONNECTION

To obtain the bipolar -5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A -5.00 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 3.

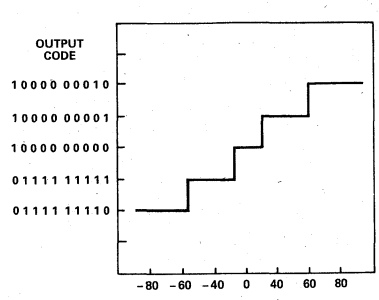


Figure 3. AD570 Transfer Curve – Bipolar Operation

NOTE: That in the bipolar mode, the code transitions are offset 1/2LSB such that an input voltage of 0 volts ±20mV yields the code representing zero (10000000 00). Each output code is then centered on its nominal input voltage.

Full Scale Calibration
Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.99 volts.

Negative Full Scale Calibration
The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally -5V) which results in the 00000000 00 code. R2 should be omitted to obtain a symmetrical range.

ZERO OFFSET
The apparent zero point of the AD570 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 4 illustrates two methods of providing this offset. Figure 4A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

Figure 4B shows how to offset the zero code by 1/2LSB to provide a code transition between the nominal bit weights.

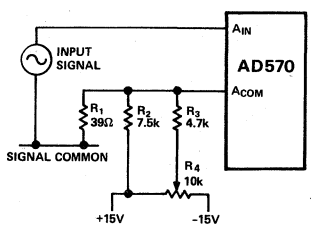


Figure 4A.

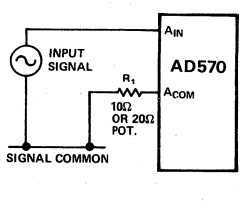


Figure 4B.

CONTROL AND TIMING OF THE AD570
There are several important timing and control features on the AD570 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 5.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

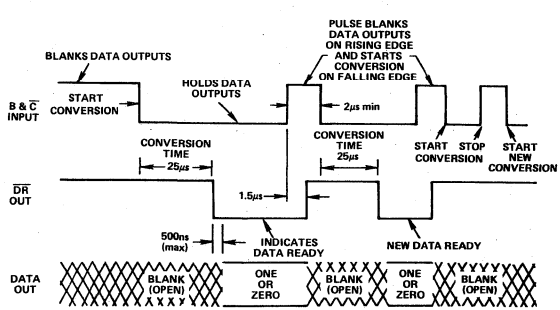


Figure 5. AD570 Timing and Control Sequence

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$
The timing sequence of the AD570 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 6 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse.

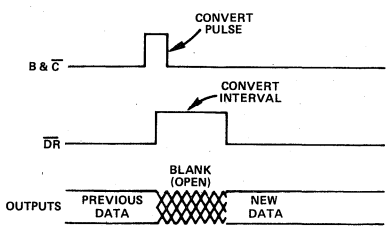


Figure 6. Convert Pulse Mode

Multiplex Mode — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 7.

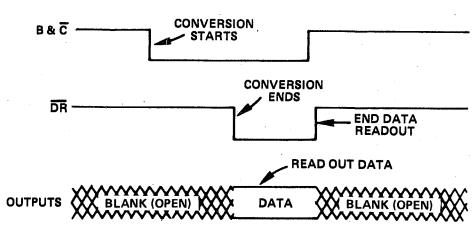


Figure 7. Multiplex Mode

This operating mode allows multiple AD570 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD570 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 8-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD570's are multiplexed in sequence, a new conversion may be started in one AD570 while data is being read from another. As long as the data is read and the first AD570 is cleared within 15μs after the start of conversion of the second AD570, no data overlap will occur.

ANALOG DEVICES

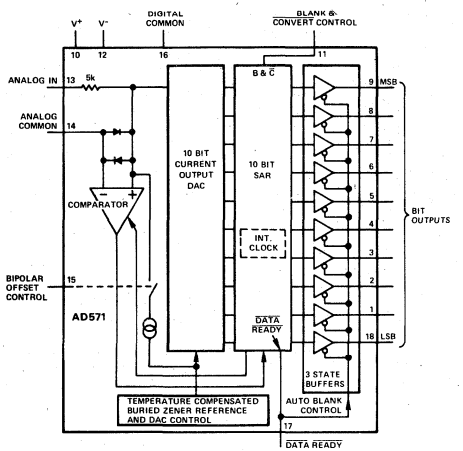
Integrated Circuit 10-Bit Analog-to-Digital Converter

AD571*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion – 25μs
No Missing Codes Over Temperature
0 to +70°C – AD571K
-55°C to +125°C – AD571S
Digital Multiplexing – 3 State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction

AD571 FUNCTIONAL BLOCK DIAGRAM



18-PIN DIP

PRODUCT DESCRIPTION

The AD571 is a 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers – all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 25μs.

The AD571 incorporates the most advanced integrated circuit design and processing technology available today. It is the first complete converter to employ I^2L (integrated injection logic) processing in the fabrication of the SAR function. Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated, subsurface Zener reference.

Operating on supplies of +5V to +15V and -15V, the AD571 will accept analog inputs of 0 to +10V, unipolar or ±5V bipolar, externally selectable. As the BLANK and $\overline{\text{CONVERT}}$ input is driven low, the three state outputs will be open and a conversion will commence. Upon completion of the conversion, the $\overline{\text{DATA READY}}$ line will go low and the data will appear at the output. Pulling the BLANK and $\overline{\text{CONVERT}}$ input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in approximately 25μs.

The AD571 is available in two versions for the 0 to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from -55°C to +125°C.

***Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.**

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction.
3. The AD571 accepts either unipolar (0 to +10V) or bipolar (-5V to +5V) analog inputs by simply grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with -15V and +5V to +15V supplies. The device will also operate with a -12V supply.

10

SPECIFICATIONS (T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY, T_A[1]			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2			±2		LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	**10**			**10**			**10**			Bits
T_{min} to T_{max}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5V≤V+≤+16.5V	–	–	–	–		±1	–	–	–	LSB
TTL Positive Supply										
+4.5V≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−16.0V≤V−≤−13.5V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[3]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			±40			±40			±40	µA
LOGIC INPUTS										
Input Current			±100			±100			±100	µA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME, T_A and										
T_{min} to T_{max}	**15**	25	**40**	**15**	25	**40**	**15**	25	**40**	µs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	+5.0	**+16.5**	**+4.5**	+5.0	**+7.0**	V
V−	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	**−12.0**	−15	**−16.5**	V
OPERATING CURRENT										
V+		15	**25**		15	**25**		15	**25**	mA
V−		9	**15**		9	**15**		9	**15**	mA
PACKAGE[4]										
Ceramic DIP		D18A			D18A			D18A		
Plastic DIP		N18A			N18A					

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor.

Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[4]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common AD571J, S . . . . . .0 to +7V
AD571K. . . . . 0 to +16.5V
V– to Digital Common . . . . . .0 to –16.0V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . .0 to V+
Power Dissipation. 800mW

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown in Figure 1. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±½LSB (0.05%).

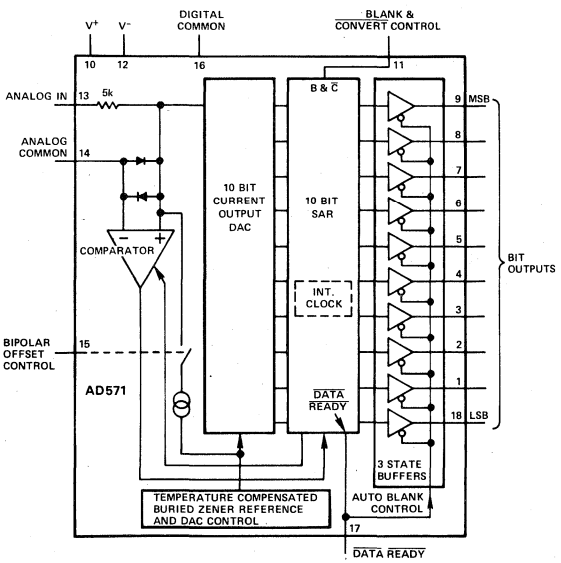


Figure 1. AD571 Functional Block Diagram

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given further.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5V and −15V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 2. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply current variations are shown in Figure 3. The supply currents change only moderately over temperature as shown in Figure 7.

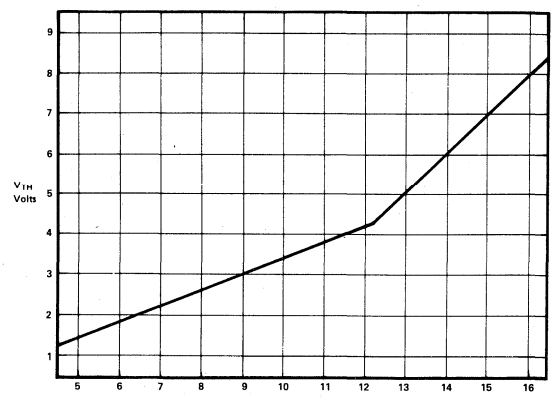


Figure 2. Logic Threshold (AD571K Only)

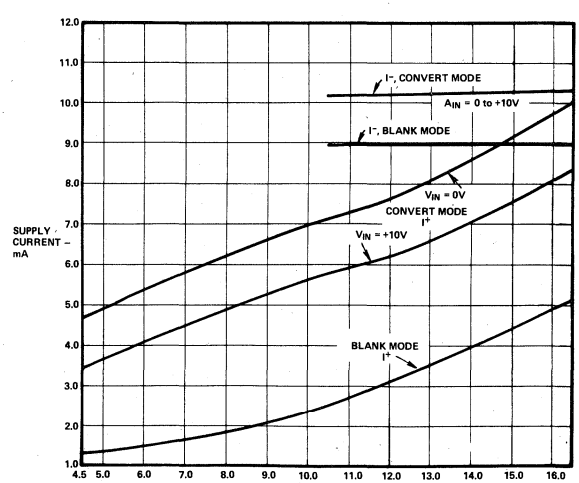


Figure 3. Supply Currents vs. Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. Thus, for most situations, all that is necessary is connection of the power supply (+5 and -15), the analog input, and the conversion start pulse. But, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 4.

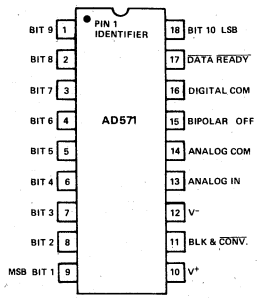


Figure 4. AD571 Pin Connections

FULL SCALE CALIBRATION

The 5kΩ thin-film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC—plus about 0.3%—when a full scale analog input voltage of 9.990 volts (10 volts − 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 13. Typical full scale calibration error will then be about ±2LSB or ±0.2%. If the more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have weight of exactly 10.00mV), a 100Ω resistor in series with a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ.

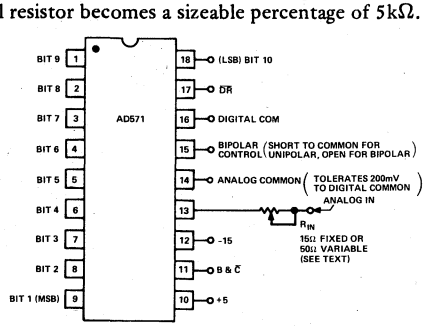


Figure 5. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a -5V to +5V range with an offset binary output code. (-5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yeilds the 1111111111 code). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 6.

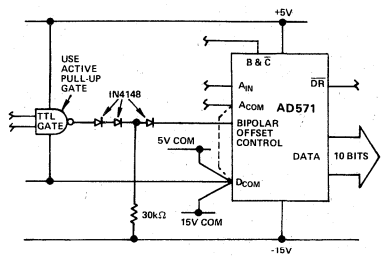


Figure 6. Bipolar Offset Controlled by Logic Gate

Gate Output = 1 Unipolar 0 - 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

10

COMMON MODE RANGE

The AD571 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition, a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. An additional 1mA will flow in during a blank interval with zero analog input. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend the connection of a parallel pair of back-to-back protection diodes between the commons if they are not connected locally.

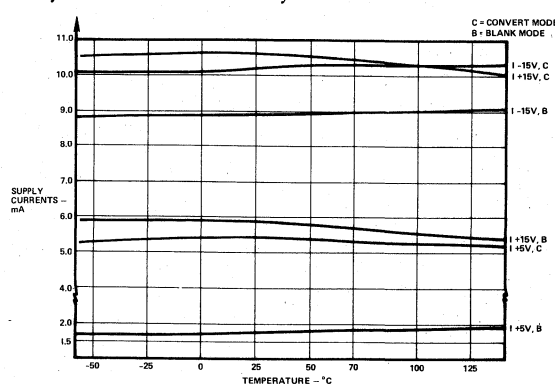


Figure 7. AD571 Power Supply Current vs. Temperature

ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the Analog Common of the device and the actual signal return or signal common. Figure 8 illustrates two methods of providing this offset. Figure 8A shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

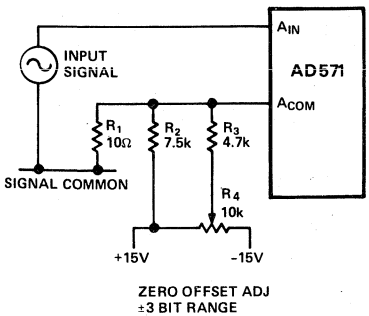


Figure 8. (A)

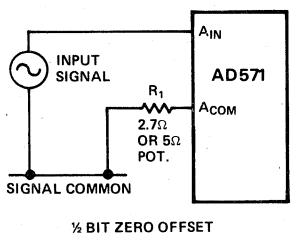


Figure 8. (B)

Figure 9 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 8B. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common, should go to the signal input side of the resistive offset network.

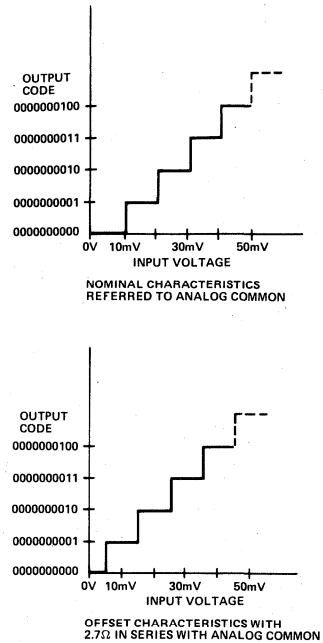


Figure 9. AD571 Transfer Curve - Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~9.766mV)

BIPOLAR CONNECTION

To obtain the bipolar -5V to +5V range with an offset binary output code the bipolar offset control pin is left open.

A -5.0 volt signal will give a 10-bit code of 00000000 00; an input of 0.00 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 10.

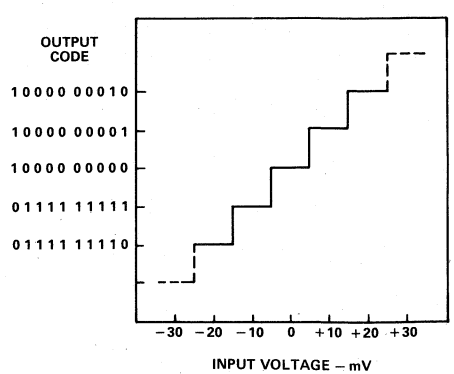


Figure 10. AD571 Transfer Curve — Bipolar Operation

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 11.

The normal stand-by situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and Data lines do not change state. When the conversion cycle is complete (typically 25μs), the $\overline{\text{DR}}$ line goes low, and within 500ns, the Data lines become active with the new data.

About 1.5μs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the Data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2μs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and Data lines will not change. If a 2μs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

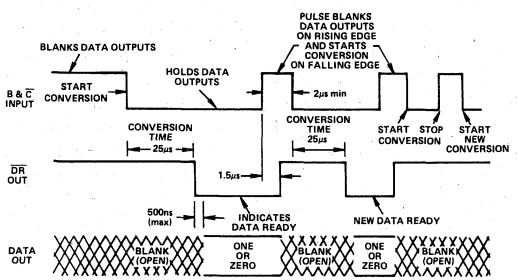


Figure 11. AD571 Timing and Control Sequences

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode, and the Multiplex Mode, are illustrated here.

Convert Pulse Mode — In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 12 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 15 in which μP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode — In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 13. A typical AD571 multiplexing application is shown in Figure 16.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571's are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15μs after the start of conversion of the second AD571, no data overlap will occur.

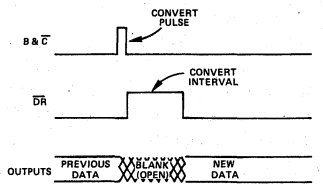


Figure 12. Convert Pulse Mode

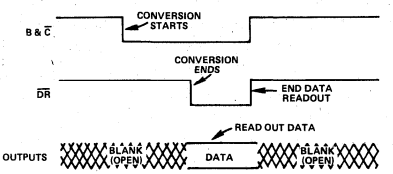


Figure 13. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 14 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the

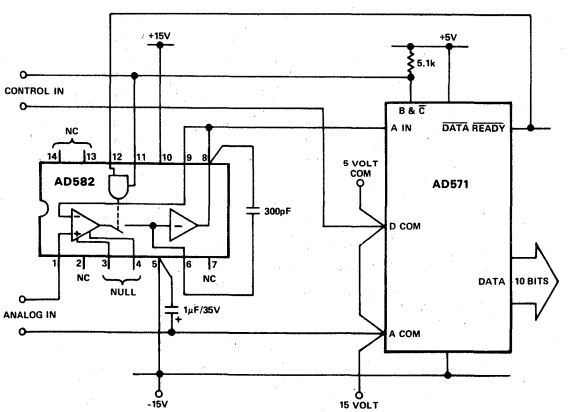


Figure 14. Sample-Hold Interface to the AD571

first comparator decision inside the AD571). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle to give the most accurate measurements.

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12-or 16-bit) with a minimum of additional control components. The configuration shown in Figure 15 is designed to operate with 8-bit bus and standard 8080 control signals.

The input control circuitry shown is required to insure that the AD571 receives a sufficiently long B & $\overline{\text{C}}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{\text{C}}$ line is low, and $\overline{\text{DR}}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{\text{WR}}$. The B & $\overline{\text{C}}$ line will now go high, followed about 1.5μs later by $\overline{\text{DR}}$. This resets the external flip-flop and brings B & $\overline{\text{C}}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DR}}$ line goes low, the data outputs will become active with the new data and the control lines will return to the stand-by state. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{\text{RD}}$ line goes low. This arrangement presents data to the bus "left-justified," with highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{\text{DR}}$ line, as shown. In this configuration, there is no need for additional buffer register storage since the data can be held indefinitely in the AD571, since the B & $\overline{\text{C}}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 16 is a straighforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs, hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{\text{DATA READY}}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{\text{DR}}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2-bits from the other port and programmed as a 10-bit input port. The remaining 6-bits of the second port are programmed as outputs and along with the 2 control bits (which act as outputs), are used to control the 8 AD571's. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADC's are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers. See the Motorola MC6821 data sheet for more application detail.

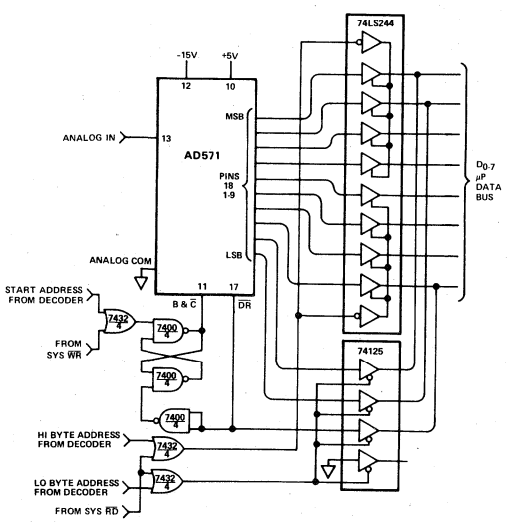


Figure 15. Interfacing AD571 to an 8-bit Bus (8080 Control Structure)

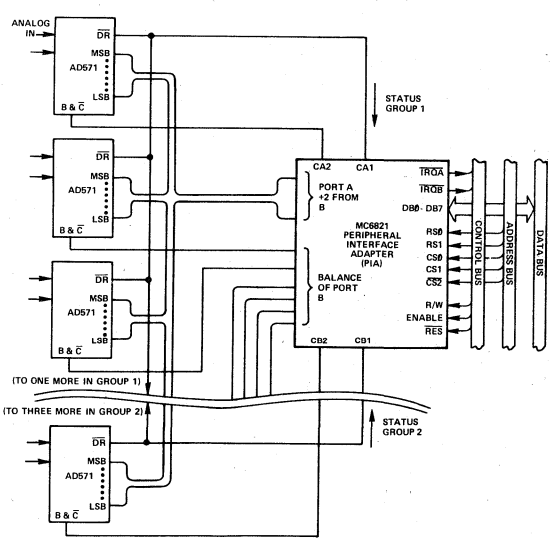


Figure 16. Multiplexing 8 AD571s Using Single PIA for µP Interface. No Other Logic Required (6800 Control Structure).

ANALOG DEVICES

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

- True 12-Bit Operation: Max Nonlinearity < ±0.012%
- Low Gain T.C.: < ±15ppm/°C (AD572B)
- Low Power: 900mW
- Fast Conversion Time: < 25μs
- Monotonic Feedback DAC Guarantees No Missing Codes

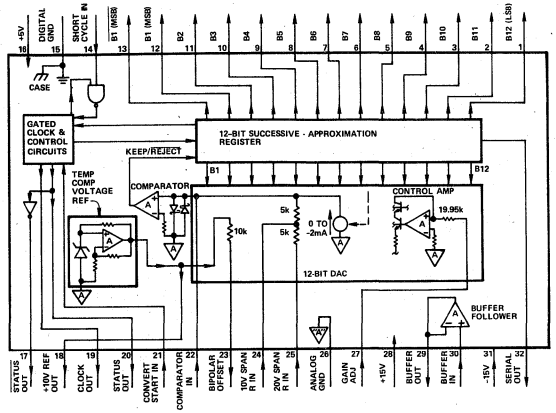
Versatility

- Aerospace Temperature Range: -55°C to +125°C (AD572S)
- Positive-True Serial or Parallel Logic Outputs
- Short-Cycle Capability

Value

- Precision +10V Reference for External Application
- Internal Buffer Amplifier
- High Reliability Package

AD572 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide superior performance, flexibility and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 900mW, and conversion time of less than 25μs. Of considerable significance in aerospace applications is the guaranteed performance from -55°C to +125°C of the AD572S. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5.0, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +10V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The new ceramic AD572 package reduces the predicted failure rate by a factor of two. The new package integrates the device substrate and package in a single ceramic element to eliminate a number of bond wires and interconnections.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25°C to +85°C, and the "S" from -55°C to +125°C.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar circuit elements:

1. 12-bit successive-approximation register
2. 12-bit DAC
3. low-drift comparator
4. temperature-compensated precision +10V reference
5. high-impedance buffer follower
6. gated clock and digital control circuits

10

AD572 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes	Package Outline[1]
AD572AD	-25°C to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C	HY32G
AD572BD	-25°C to +85°C	±15ppm/°C	±10ppm/°C	-25°C to +85°C	HY32G
AD572SD	-55°C to +125°C	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)	±20ppm/°C	-55°C to +125°C	HY32G

NOTE: [1] See Section 19 for package outline information.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	5.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time			
to 0.01% of FSR for 20V step	2μs	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25°C to +85°C	Guaranteed: -55°C to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/%ΔV_S	*	*
±5V	±0.001% FSR/%ΔV_S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C)	±15ppm/°C (-25°C to +85°C) ±25ppm/°C (-55°C to +125°C)
Unipolar Offset	±3ppm FSR/°C	±5ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μs	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
$\overline{\text{Status}}$	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV typ	*	*
Max External Current	±1mA	*	*
Voltage Temperature Coefficient (max)	±20ppm/°C	±10ppm/°C	*
POWER REQUIREMENTS			
Supply Voltages/Currents	+15V, ±5% @ +25mA (40 max)	*	*
	-15V, ±5% @ -20mA (35 max)	*	*
	+5V, ±5% @ +80mA (150 max)	*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-55°C to +150°C	*	*

NOTES
*Same specification as AD572AD.
**Same specification as AD572BD.

Specifications subject to change without notice.

Note 1 Positive pulse 200ns wide (min). Leading edge ("0" to "1") resets registers. Trailing edge ("1" to "0") initiates conversion.

Note 2 With 50Ω, 1% fixed resistor in place of Gain Adjust pot; see Figures 4 and 5.

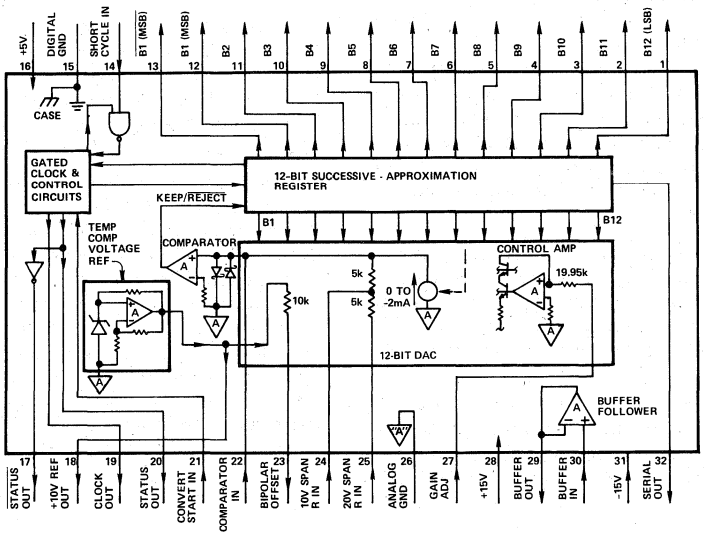


Figure 1. AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T.C. zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, ±10mV by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC chip uses 12 precision, high speed bipolar current steering switches, a control amplifier and a laser-trimmed thin film resistor network to produce a very fast, high accuracy analog output current. The DAC is laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through

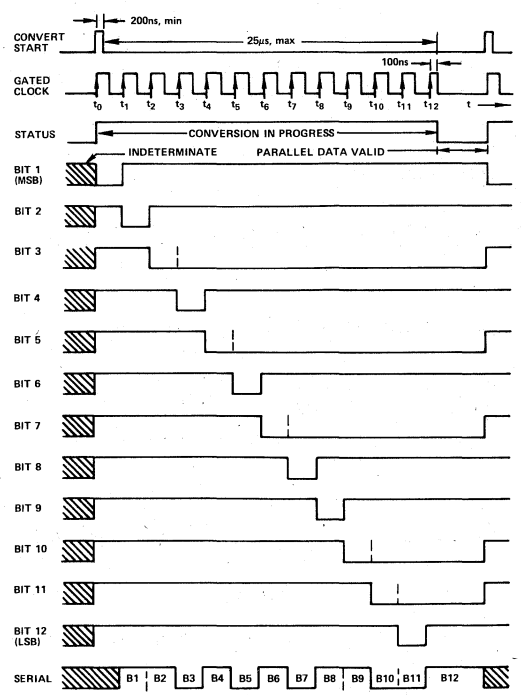


Figure 2. Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 100ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 100ns delay period guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_o = B_1\ B_2\ B_3 \ldots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 + \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{in}}{FSR} \qquad (1)$$

. . .where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes:

$$\frac{B_1\,2^{11} + B_2\,2^{10} + B_3\,2^9 + \ldots + B_{12}\,2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \qquad (2)$$

Expressions (1) and (2) can be put in an alternate form:

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR = E_{in} \qquad (3)$$

Unipolar (Binary Coding)

...and...

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \ldots + \frac{B_{12}}{4096}\right) FSR - \frac{FSR}{2} = E_{in} \qquad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

0 TO +10V INPUT RANGE

Assume FSR = 10V and $B_1\ B_2\ B_3\ .\ .B_{12}$ = 110001000001, then from (3), E_{in} = +5V +2.5V +0.1563V + 0.0024V = +7.6587V.

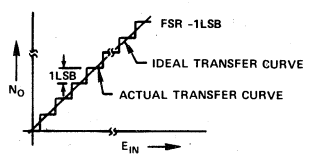
-5V TO +5V INPUT RANGE

Assume FSR = 10V as above, but that the bipolar offset is connected and $B_1\ B_2\ B_3\ .\ .B_{12}$ = 0110000000001. Then from (4), E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V.

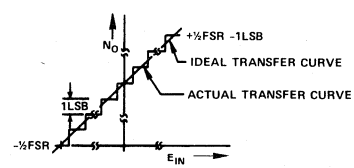
-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), E_{in} = (+5V +2.5V +0.0049V) -10V = -2.4951V, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the 2^{12} = 4096 quantization levels between 0 and FSR (or -FSR/2 and +FSR/2). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight-line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly ±½LSB at the end of each quantization interval, giving rise to the fundamental ±½LSB quantization error inherent in the digitizing process.



(A) Unipolar Range (Binary Coding)



(B) Bipolar Range (Offset Binary Coding)

Figure 3. Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust: Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open-circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9MΩ resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of 8 x 244 x 10^{-6} x 1200ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

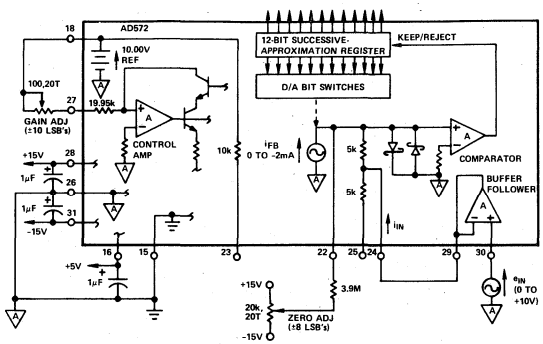


Figure 4. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

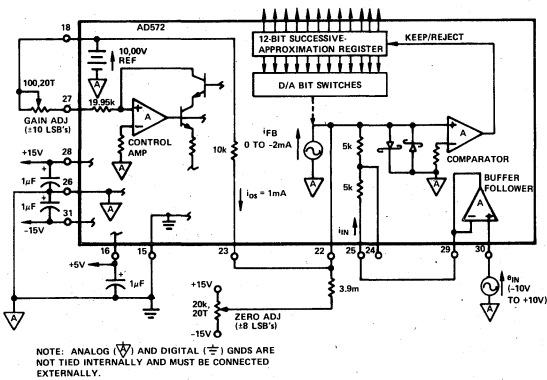


Figure 5. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6.

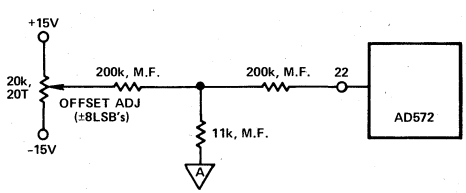


Figure 6. Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pick-up.

Gain Adjust: The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types; 20T cermet (tempco = 100ppm/°C max) types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to ±0.1% of FSR is guaranteed.

Grounding: Analog and digital power supply grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -½FSR for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table I. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table I. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table II.

Range	Buffer Follower	Connect Analog Input To Pin:	Connect Span Pin:	Connect Bipolar Pin 23 To:
0 to +5V	Used	30, and 29 to 24	25 to 22	—
	Not Used	24		
0 to +10V	Used	30, and 29 to 24	—	
	Not Used	24		
-2.5 to +2.5V	Used	30, and 29 to 24	25 to 22	22
	Not Used	24		
-5 to +5V	Used	30, and 29 to 24	—	
	Not Used	24		
-10 to +10V	Used	30, and 29 to 25	—	
	Not Used	25		

Table II. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical r_{on} = 200Ω which has a 3000ppm/°C tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5kΩ input impedance, nominal), this r_{on} would introduce a 4% gain scale-factor loading error, which is well beyond the normal ±0.25% FSR external gain adjustment range, and a tempco of approximately 3000ppm/°C x 4% = 120ppm/°C. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage I_{BIAS} R_{SOURCE} can be kept negligible, even though the buffer amplifier dynamic input impedance ⩾ 100MΩ. The buffer amplifier has a 2μs settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

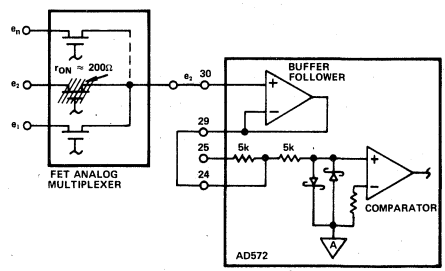


Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 14 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +100ns in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table III.

Connect Short Cycle Pin 14 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at: (Figure 2)
16	12	0.024	25	t_{12} + 100ns
2	10	0.10	21	t_{10} + 100ns
4	8	0.39	17	t_8 + 100ns

Table III. Short Cycle Connections

(One should note that the calibration voltages listed in Table I are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary

or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 200ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than ½LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The $\overline{\text{STATUS}}$ output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the $\overline{\text{STATUS}}$ flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\ S\text{-}H}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the $\overline{\text{STATUS}}$ flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\ S\text{-}H}$ again tracks the analog signal voltage $e_{in\ S\text{-}H}$ (after the signal acquisition transient has subsided).

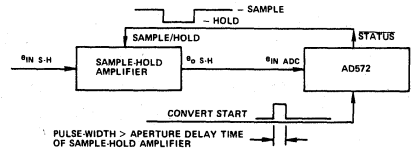


Figure 9. Sample-Hold Amplifier – AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\ S\text{-}H}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.

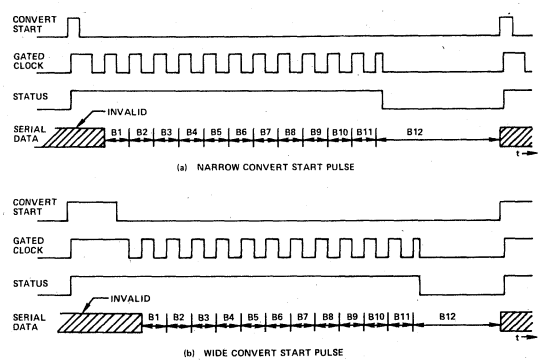


Figure 10. Effect of Convert Start Pulse-Width on Timing

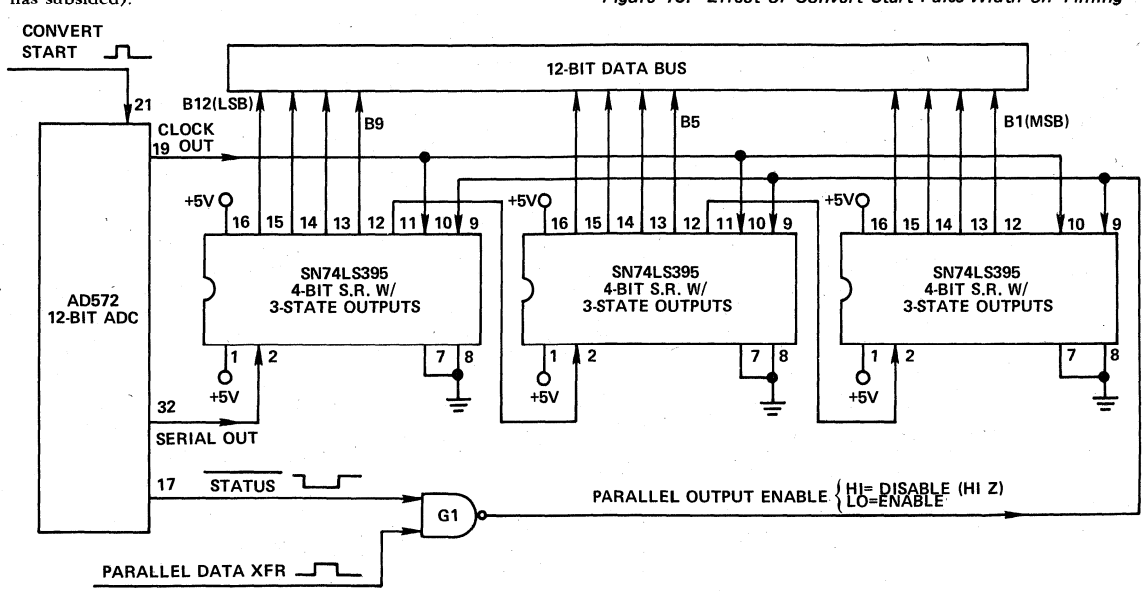


Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Bus

Digital Gain Control: Figure 11 shows a method of varying the AD572 gain digitally, using an 8-bit DAC. The 100Ω GAIN ADJ potentiometer is replaced by a 15Ω fixed resistor. This biases full-scale high by approximately 35Ω/20,000Ω = +0.18% of FSR. The AD559 has a large positive compliance voltage which permits its Current Output pin 4 to be connected directly to the AD572 Reference Input pin 27. The AD559 2.5mA output current is established by the AD580 +2.5V voltage reference connected through a 1kΩ resistor to Reference Current Input pin 14. The 2.5mA DAC full-scale output current removed from the AD572 pin 27 node changes the pin 27 input current -2.5mA x 15Ω/20kΩ = -1.88μA, or

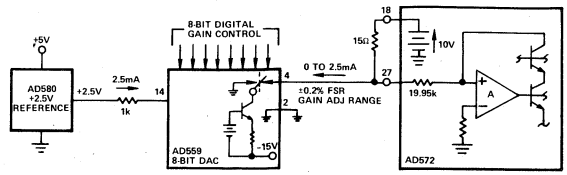


Figure 11. Digital Gain Control Using 8-Bit DAC

-1.88μA/500μA = -0.38% of FSR; this permits a digital gain adjustment range of approximately ±0.2% FSR from nominal.

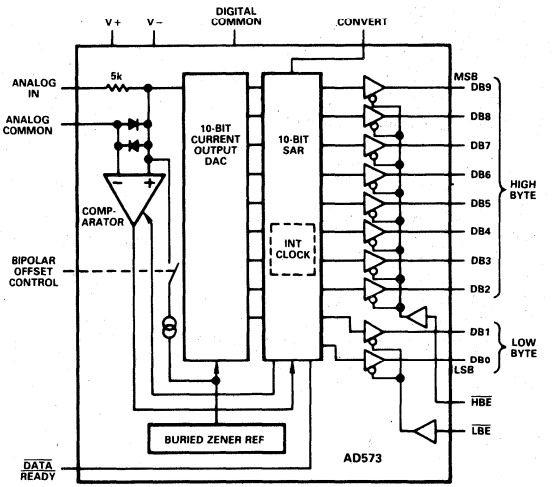
Fast, Complete 10-Bit A/D Converter with Microprocessor Interface

AD573*

FEATURES

- Complete 10-Bit A/D Converter with Reference, Clock and Comparator
- Full 8- or 16-Bit Microprocessor Bus Interface
- Fast Successive Approximation Conversion – 20μs typ
- No Missing Codes Over Temperature
- Operates on +5V and −12V to −15V Supplies
- Low Cost Monolithic Construction

AD573 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD573 is a complete 10-bit successive approximation analog to digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

The AD573 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD573 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion. $\overline{\text{HIGH BYTE ENABLE}}$ ($\overline{\text{HBE}}$) and $\overline{\text{LOW BYTE ENABLE}}$ ($\overline{\text{LBE}}$) control the 8-bit and 2-bit three state output buffers.

The AD573 is available in two versions for the 0 to +70°C temperature range, the AD573J and AD573K. The AD573S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD573J and AD573K are also available in a 20-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD573 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The AD573 interfaces to many popular microprocessors without external buffers or peripheral interface adapters. The 10 bits of output data can be read as a 10-bit word or as 8- and 2-bit words.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD573 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.

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*Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690

SPECIFICATIONS (T_A=25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD573J Min	AD573J Typ	AD573J Max	AD573K Min	AD573K Typ	AD573K Max	AD573S Min	AD573S Typ	AD573S Max	Units
RESOLUTION		10			10			10		Bits
RELATIVE ACCURACY[1]			±1			±1/2			±1	LSB
$T_A = T_{min}$ to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2				±2	LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY[3]	10			10			10			Bits
$T_A = T_{min}$ to T_{max}		9			10				10	Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS[4]										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
Positive Supply										
+4.5≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	−5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[5]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
Output Leakage			±40			±40			±40	µA
LOGIC INPUTS										
Input Current			±100			±100			±100	µA
Logic "1"	2.0			2.0			2.0			V
Logic "0"			0.8			0.8			0.8	V
CONVERSION TIME										
$T_A = T_{min}$ to T_{max}	10	20	30	10	20	30	10	20	30	µs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−11.4	−15	−16.5	+11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT										
V+		15	25		15	25		15	25	mA
V−		9	15		9	15		9	15	mA
PACKAGE[6]										
Ceramic DIP		D20A			D20A			D20A		
Plastic DIP		N20A			N20A					

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor.
Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]Change from +25°C value from +25°C to T_{min} or T_{max}.

[5]The data output lines have active pull-ups to source 0.5mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

[6]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD573 ORDERING GUIDE

Model	Package Option	Temperature Range	Relative Accuracy
AD573JN	20-Pin Plastic DIP	0 to +70°C	±1LSB max
AD573KN	20-Pin Plastic DIP	0 to +70°C	± 1/2LSB max
AD573JD	20-Pin Ceramic DIP	0 to +70°C	±1LSB max
AD573KD	20-Pin Ceramic DIP	0 to +70°C	± 1/2LSB max
AD573SD	20-Pin Ceramic DIP	−55°C to +125°C	±1LSB max

FUNCTIONAL DESCRIPTION

A block diagram of the AD573 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5μs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ½LSB (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{HBE}$ and $\overline{LBE}$ can then be activated to enable the upper 8-bit and lower 2-bit buffers as desired. $\overline{HBE}$ and $\overline{LBE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

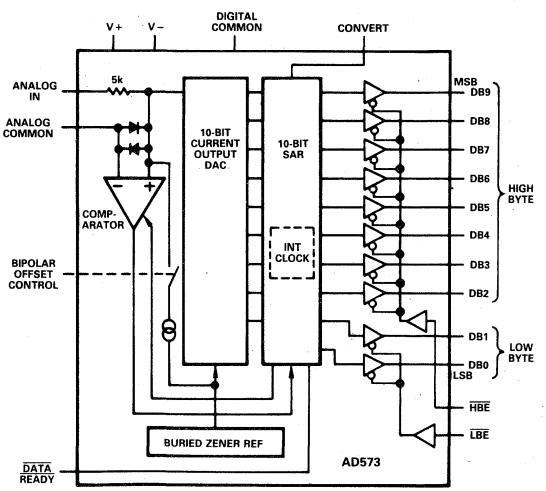


Figure 1. AD573 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD573 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

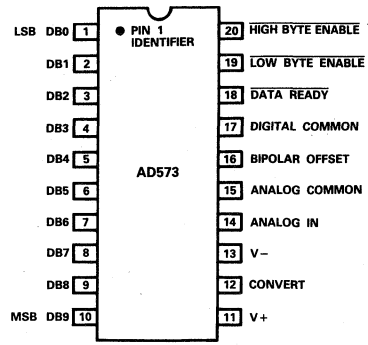


Figure 2. AD573 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.990 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.2%. If more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 11111111 10 and 11111111 11. Each LSB will then have a weight of 9.766mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 10.00mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

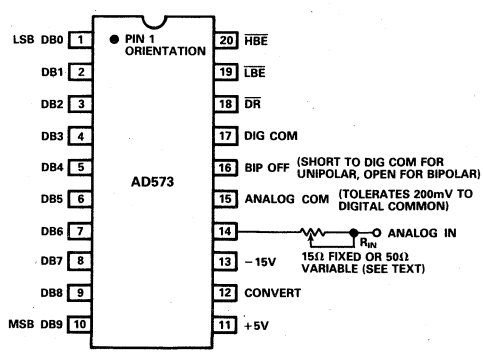


Figure 3. Standard AD573 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1LSB for all versions of the AD573, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

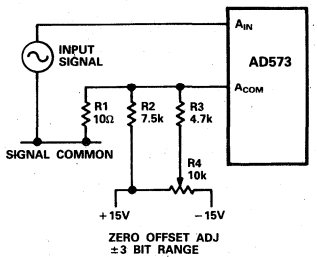


Figure 4a.

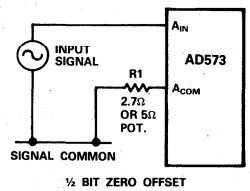


Figure 4b.

Figure 5 shows the nominal transfer curve near zero for an AD573 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

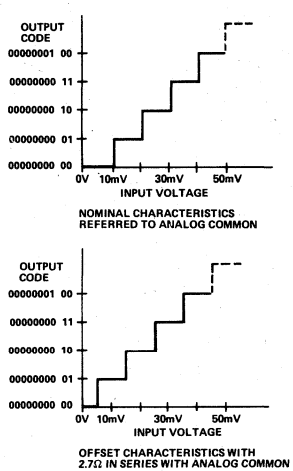


Figure 5. AD573 Transfer Curve – Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.000 volt signal will give a 10-bit code of 00000000 00; an input of 0.000 volts results in an output code of 10000000 00 and +4.99 volts at the input yields the 11111111 11 code. The nominal transfer curve is shown in Figure 6.

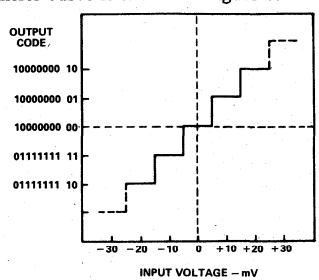


Figure 6. AD573 Transfer Curve – Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ½LSB such that an input voltage of 0 volts ±5mV yields the code representing zero (10000000 00). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.985 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 00000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

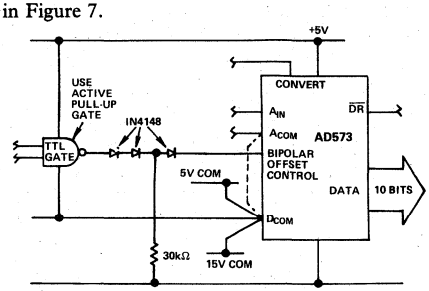


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0 – 10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD573

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a

signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD573, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD573 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

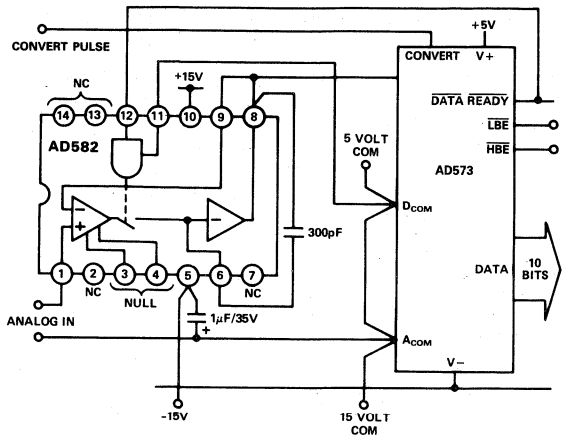


Figure 8. Sample-Hold Interface to the AD573

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD573 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD573).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

GROUNDING CONSIDERATIONS

The AD573 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD573

The operation of the AD573 is controlled by three inputs: CONVERT, $\overline{HBE}$ and $\overline{LBE}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{DR}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{DR}$ returns low. During the conversion cycle, $\overline{HBE}$ and $\overline{LBE}$ should be held high. If $\overline{HBE}$ or $\overline{LBE}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

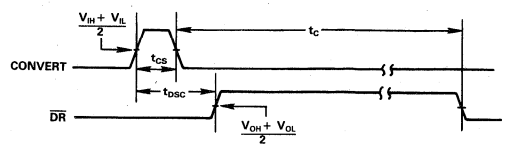


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers are enabled by $\overline{HBE}$ and $\overline{LBE}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

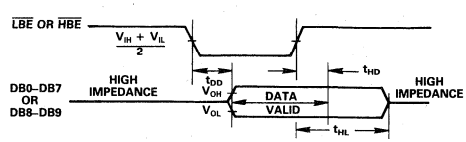


Figure 10. Read Timing

TIMING SPECIFICATIONS (All grades, T_A = T_{min} – T_{max})

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{DR}$ Delay from CONVERT	t_{DSC}	–	1	1.5	μs
Conversion Time	t_C	10	20	30	μs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{HBE}$/$\overline{LBE}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD573 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD573 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD573, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing. In 8-bit bus systems, the 10-bit AD573 will occupy two locations when data is to be read; therefore, two (usually consecutive) addresses must be decoded. One of the addresses can also be used as the address which produces the CONVERT signal during WR operations.

Figure 11 shows a generalized diagram of the control logic for

an AD573 interfaced to an 8-bit data bus, where two addresses (ADC ADDR and ADC ADDR + 1) have been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations. ADC ADDR + 1 performs no function during write operations, but contains the low byte data during read operations.

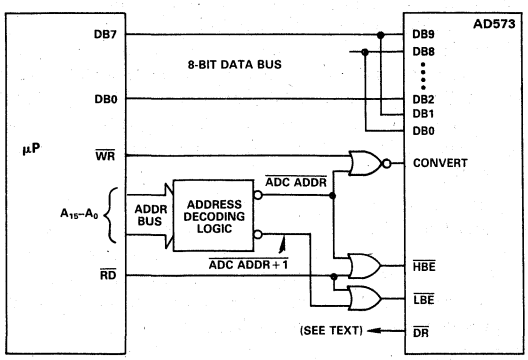


Figure 11. General AD573 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

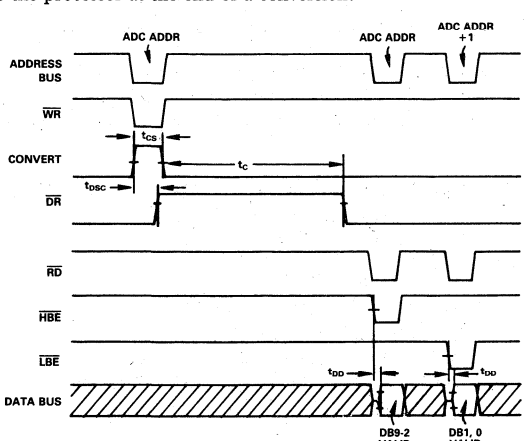


Figure 12. Typical AD573 Interface Timing Diagram

CONVERT Pulse Generation

The AD573 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD573.

In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

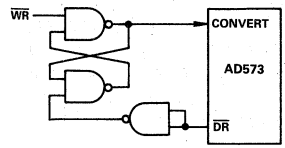


Figure 13a. Using 74LS00

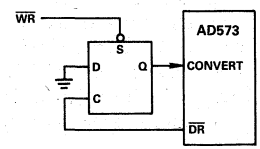


Figure 13b. Using 1/2 74LS74

Output Data Format

The AD573 output data is presented in a left-justified format. The 8 MSBs (DB9–DB2, pins 10 through 3) are enabled by $\overline{HBE}$ (pin 20) and the 2 LSBs (DB1, DB0 – pins 2 and 1) are enabled by $\overline{LBE}$ (pin 19). This allows simple interface to 8-bit system buses by overlapping the 2 MSBs and the 2 LSBs. The organization of the data is shown in Figure 14.

When the least significant bits are read ($\overline{LBE}$ brought low), the six remaining bits of the byte will contain meaningless data. These unwanted bits can be masked by logically ANDing the byte with 11000000 (C0 hex), which forces the 6 lower bits to logic 0 while preserving the two most significant bits of the byte.

Note that it is not possible to reconfigure the AD573 for right justified data.

$\overline{HBE}$	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
$\overline{LBE}$	DB1	DB0	X	X	X	X	X	X

Figure 14. AD573 Output Data Format

In systems where all 10 bits are desired at the same time, $\overline{HBE}$ and $\overline{LBE}$ may be tied together. This is useful in interfacing to 16-bit bus systems. The resulting 10-bit word can then be placed at the high end of the 16-bit bus for left justification or at the low end for right justification.

It is also possible to use the AD573 in a "stand-alone" mode, where the output data buffers are automatically enabled at the end of a conversion cycle. In this mode, the $\overline{DR}$ output is wired to the $\overline{HBE}$ and $\overline{LBE}$ inputs. The outputs thus are forced into the high-impedance state during the conversion period, and valid data becomes available approximately 500ns after the $\overline{DR}$ signal goes low at the end of the conversion. The 500ns delay allows propagation of the least significant bit through the internal logic.

This mode is particularly useful for bench-testing of the AD573, and in applications where dedicated I/O ports of peripheral interface adapter chips are available.

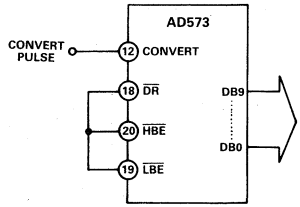


Figure 15. AD573 in "Stand-Alone" Mode (Output Data Valid 500ns After DR Goes Low)

Apple II Microcomputer Interface

The AD573 can provide a flexible, low-cost analog interface for the popular Apple II microcomputer. The Apple II, based on a 1MHz 6502 microprocessor, meets all timing requirements for the AD573. Only a few TTL gates are required to decode the signals available on the Apple II's peripheral connector. The recommended connections are shown in Figure 16.

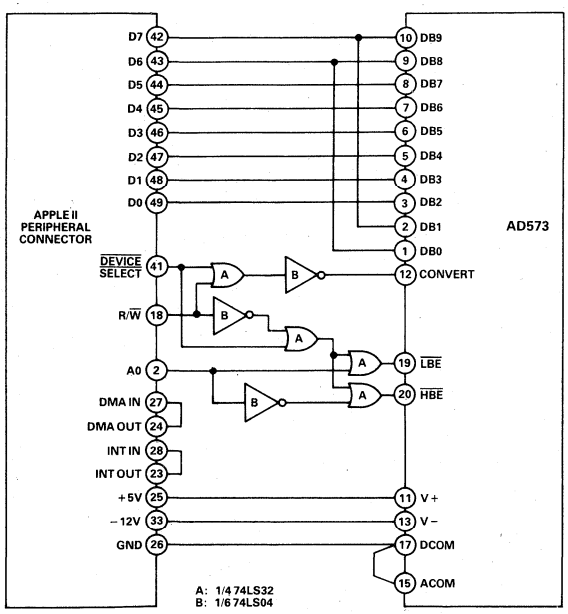


Figure 16. AD573 Interface to Apple II

The BASIC routine listed here will operate the AD573 circuit shown in Figure 16. The conversion is started by POKEing to the location which contains the AD573. The relatively slow execution speed of BASIC eliminates the need for a delay routine between starting and reading the converter. This routine assumes that the AD573 is connected for a ±5 volt input range. Variable I represents the integer value (from 0 to 1023) read from the AD573. Variable V represents the actual value of the input signal (in volts).

```
100 PRINT "WHICH SLOT IS THE A/D IN";:INPUT S
110 A= 49280+16*S
120 POKE A,0
130 L=PEEK(A) :H=PEEK(A+1)
140 I=(4*H)+INT(L/64)
150 V=(I/1024)*10-5
160 PRINT "THE INPUT SIGNAL IS ";V;"VOLTS."
```

It is also possible to write a faster-executing assembly-language routine to control the AD573. Such a routine will require a delay between starting and reading the converter. This can be easily implemented by calling the Apple's WAIT subroutine (which resides at location $FCA8) after loading the accumulator with a number greater than or equal to two.

8085-Series Microprocessor Interface

The AD573 can also be used with 8085-series microprocessors. These processors use separate control signals for RD and WR, as opposed to the single R/$\overline{W}$ control signal used in the 6800/6500 series processors.

There are two constraints related to operation of the AD573 with 8085-series processors. The first problem is the width of the CONVERT pulse. The circuit shown in Figure 17 (essentially the same as that shown in Figure 13) will produce a wide enough CONVERT pulse when the 8085 is running at 5MHz. For 8085 systems running at slower clock rates (3MHz), the flip-flop-based circuit can be eliminated since the $\overline{WR}$ pulse will be approximately 500ns wide.

The other consideration is the access time of the AD573's three-state output data buffers, which is 250ns maximum. It may be necessary to insert wait states during RD operations from the AD573. This will not be a problem in systems using memories with comparable access times, since wait states will have already been provided in the basic system design.

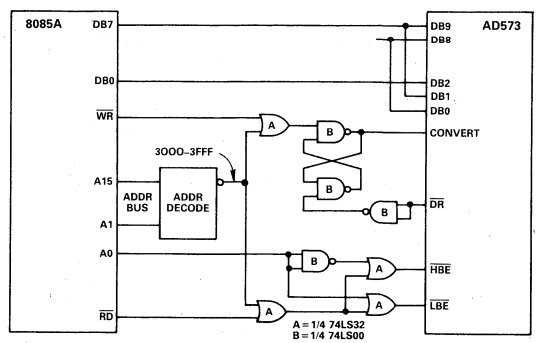


Figure 17. AD573–8085A Interface Connections

The following assembly-language subroutine can be used to control an AD573 residing at memory locations 3000_H and 3001_H. The 10 bits of data are returned (left-justified) in the DE register pair.

```
ADC:  LXI  H,3000  ;LOAD HL WITH AD573 ADDRESS
      MOV M,A      ;START CONVERSION
      MVI  B,06    ;LOAD DELAY PERIOD
LOOP: DCR  B       ;DELAY LOOP
      JNZ  LOOP    ;
      MOV A,M      ;READ LOW BYTE
      ANI  C0      ;MASK LOWER 6 BITS
      MOV E,A      ;STORE CLEAN LOW BYTE IN E
      INR  L       ;LOAD HIGH BYTE ADDRESS
      MOV D,M      ;MOVE HIGH BYTE TO D
      RET          ;EXIT
```

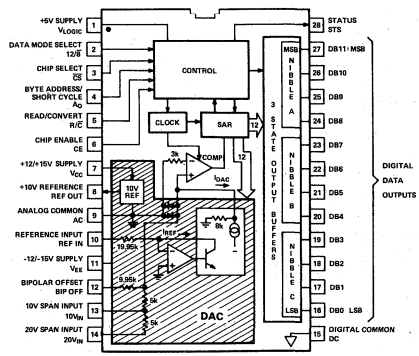
Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

FEATURES

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Full 8- or 16-Bit Microprocessor Bus Interface**
- **250ns Bus Access Time**
- **Guaranteed Linearity Over Temperature**
  - **0 to +70°C – AD574AJ, AK, AL**
  - **−55°C to +125°C – AD574AS, AT, AU**
- **No Missing Codes Over Temperature**
- **Fast Successive Approximation Conversion – 25μs**
- **Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL 12.5ppm/°C max AD574AU**
- **Low Profile 28-Pin Ceramic DIP**
- **Low Power: 390mW**

AD574A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12-or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the proven LCI (linear-compatible integrated injection logic) process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, AT, and AU are specified for the −55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD574A interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.

10

SPECIFICATIONS (@ = 25°C with V_{CC} = +15V, V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise indicated)

Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR										
25°C (max)			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minumum resolution for which no missing codes are guaranteed)										
25°C	11			12			12			Bits
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)			±10			±4			±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT TO REF IN)										
(Adjustable to zero) 25°C (max)			0.25			0.25			0.25	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)		0.47			0.37			0.30		% of F.S.
(With Initial Adjustment)		0.22			0.12			0.05		% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2			±1			±1	LSB
			10			5			5	ppm/°C
Bipolar Offset			±2			±1			±1	LSB
			10			5			5	ppm/°C
Full Scale Calibration			±9			±5			±2	LSB
			50			27			10	ppm/°C
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
$+13.5 \le V_{CC} \le +16.5V$ or $+11.4V \le V_{CC} \le +12.6V$			±2			±1			±1	LSB
$+4.5 \le V_{LOGIC} \le +5.5V$			±1/2			±1/2			±1/2	LSB
$-16.5 \le V_{EE} \le -13.5V$ or $-12.6V \le V_{EE} \le -11.4V$			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar		−5 to +5			−5 to +5			−5 to +5		Volts
		−10 to +10			−10 to +10			−10 to +10		Volts
Unipolar		0 to +10			0 to +10			0 to +10		Volts
		0 to +20			0 to +20			0 to +20		Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
V_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads) (External load should not change during conversion)			1.5[1]			1.5[1]			1.5[1]	mA
PACKAGE OPTION[2] (D28A)–Ceramic DIP		AD574AJD			AD574AKD			AD574ALD		

NOTES

[1]The reference should be buffered for operation on ± 12V supplies.

[2]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR										
25°C (max)			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minumum resolution for which no missing codes are guaranteed)										
25°C	11			12			12			Bits
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)			±10			±4			±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT TO REF IN)										
(Adjustable to zero) 25°C (max)			0.25			0.25			0.25	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)		0.75			0.5			0.37		% of F.S.
(With Initial Adjustment)		0.5			0.25			0.12		% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference)										
T_{min} to T_{max}										
Unipolar Offset			±2			±1			±1	LSB
			5			2.5			2.5	ppm/°C
Bipolar Offset			±4			±2			±1	LSB
			10			5			2.5	ppm/°C
Full Scale Calibration			±20			±10			±5	LSB
			50			25			12.5	ppm/°C
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
$+13.5 \le V_{CC} \le +16.5V$ or $+11.4V \le V_{CC} \le +12.6V$			±2			±1			±1	LSB
$+4.5 \le V_{LOGIC} \le +5.5V$			±1/2			±1/2			±1/2	LSB
$-16.5 \le V_{EE} \le -13.5V$ or $-12.6V \le V_{EE} \le -11.4V$			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar		−5 to +5			−5 to +5			−5 to +5		Volts
		−10 to +10			−10 to +10			−10 to +10		Volts
Unipolar		0 to +10			0 to +10			0 to +10		Volts
		0 to +20			0 to +20			0 to +20		Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
V_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads) (External load should not change during conversion)			1.5[1]			1.5[1]			1.5[1]	mA
PACKAGE OPTION[2] D (D28A) – Ceramic DIP	AD574ASD			AD574ATD			AD574AU			

NOTES
[1]The reference should be buffered for operation on ±12V supplies.
[2]See Section 19 for package outline information.

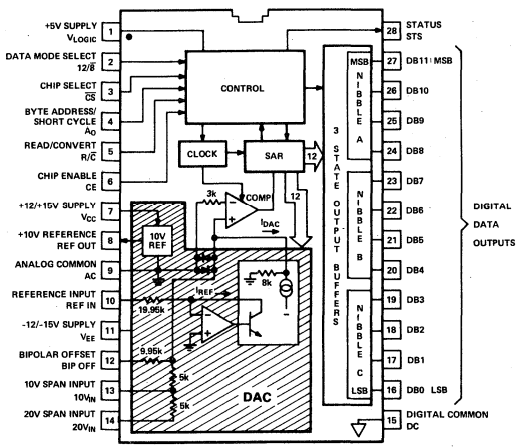
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

DIGITAL CHARACTERISTICS[1] (All grades, T_{min} – T_{max})

	Min	Typ	Max	
Logic Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)				
Voltages				
Logic "1"	+2.0V		+5.5V	
Logic "0"	−0.5V		+0.8V	
Current	−50μA		+50μA	
Capacitance		5pF		
Logic Outputs (DB11–DB0, STS)				
Logic "0"			+0.4V	$I_{SINK} \leq 1.6mA$
Logic "1"	2.4V			$I_{SOURCE} \leq 500\mu A$
Leakage (When in high-Z state)	−40μA		+40μA	DB11 – DB0 Only
Capacitance		5pF		

[1]Detailed Timing Specifications appear in the Digital Interface Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard-wired to V_{LOGIC} or DIGITAL COMMON.



AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common . . . . . ±16.5V
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) . . . . . 100°C
(S, T, U grades) . . . . . 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec.
Storage Temperature . . . . . −65°C to +150°C
Thermal Resistance, θ_{JA} . . . . . 60°C/W

AD574A ORDERING GUIDE

Model	Temp. Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJD	0 to +70°C	±1LSB	11 Bits	50.0
AD574AKD	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574ALD	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574ASD	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574ATD	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AUD	−55°C to +125°C	±1LSB	12 Bits	12.5

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR
Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)
A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET
The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET
Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY
Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT–JUSTIFIED DATA
The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL SCALE CALIBRATION ERROR
The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS
The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION
The standard specifications for the AD574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH
A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

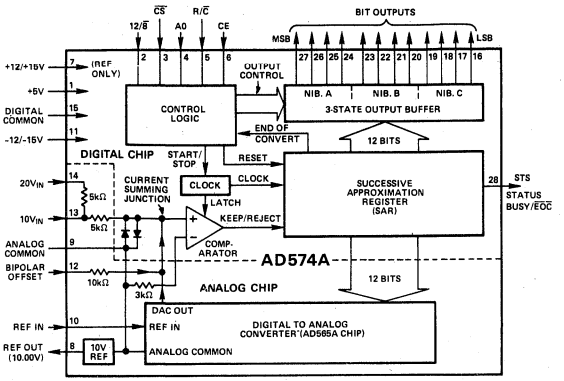


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ±15V supplies. If the AD574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574A ANALOG INPUT

The AD574A is a successive-approximation type analog-to-digital converter. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 500kHz rate. Thus it is important to recognize that the signal source driving the AD574A must be capable of holding a constant output voltage under dynamically–changing load conditions.

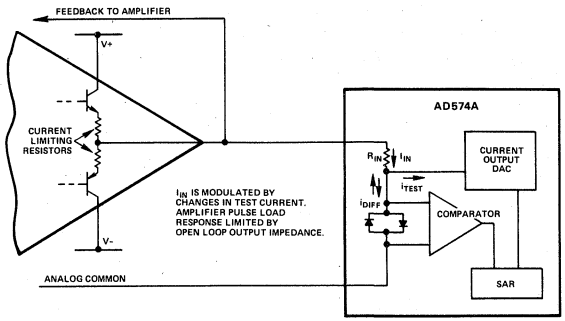


Figure 2. Op Amp – AD574A Interface

The closed loop output impedance of an op amp is equal to the open loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving an AD574A must either have sufficient loop gain at 500kHz to reduce the closed loop output impedance to a low value or have low open loop output impedance.

This can be accomplished either by using a wideband op amp or by placing a discrete-transistor or integrated buffer inside the amplifier's feedback loop.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $+V_{CC}$ and $-V_{EE}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 47μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

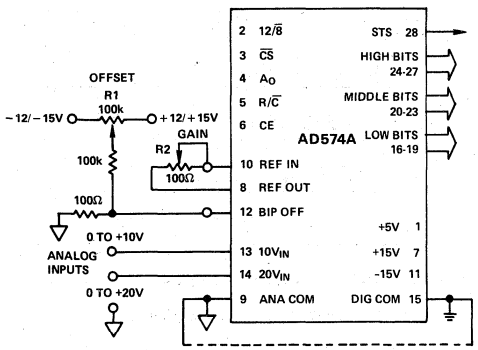


Figure 3. Unipolar Input Connections

All of the thin film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±2LSB max zero offset error and ±0.25% (10LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14.

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal ½LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

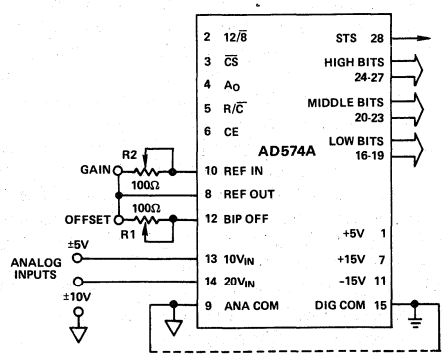


Figure 4. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

CONVERSION START/DATA READ CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 5 shows the internal logic circuitry of the AD574A.

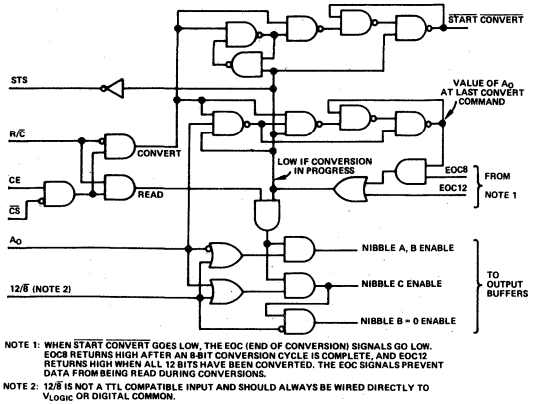


Figure 5. AD574A Control Logic

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. The A_0 line is usually tied to the least significant bit of the address bus. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to VLOGIC). The 12/$\overline{8}$ pin is not TTL-compatible and must be hard-wired to either VLOGIC or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that A_0 change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4LSBs + 4 Trailing Zeroes

Table I. AD574A Truth Table

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the AD574A control signals will provide the system designer with useful insight into the operation of the device.

Figure 6 shows a complete timing diagram for the AD574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion. As shown in Figure 6,

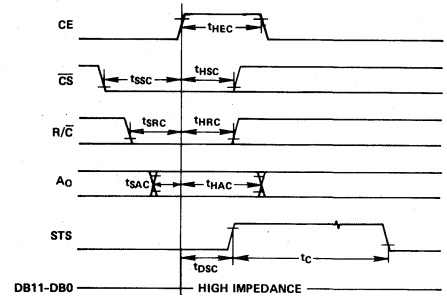


Figure 6. Convert Start Timing

CE is used. If $\overline{CS}$ is used to trigger conversion or if the specified set-up times are not met, appropriately longer pulses are necessary (to provide at least 200ns when R/$\overline{C}$, CE, and $\overline{CS}$ are all valid). Note that CE includes one less propagation delay than $\overline{CS}$ and is therefore the faster input.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			300	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{CS}$ to CE Setup	300			ns
t_{HSC}	$\overline{CS}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	200			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs

Figure 7 shows the timing for data read operations. The AD574A differs from the original AD574 design in that the three-state output buffers feature faster access time and shorter data latency

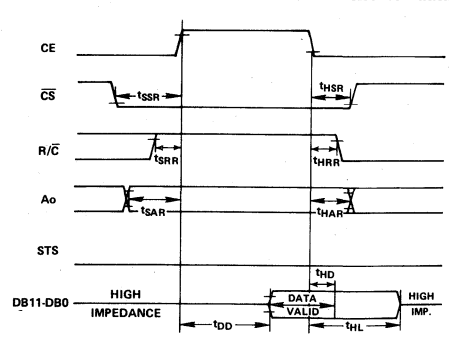


Figure 7. Read Cycle Timing

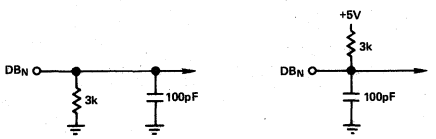
times. This speed improvement simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ is used to enable the device, access time is extended by 100ns.

In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0, must be stable at least 150ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

READ TIMING – FULL CONTROL MODE

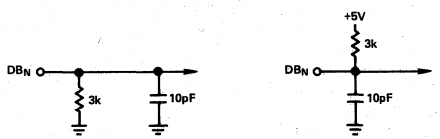
Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)		210	250	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay		110	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

[1] t_{DD} is measured with the load circuit of Figure 8 and defined as the time required for an output to cross 0.4V or 2.4V.
[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 9.



a. High-Z to Logic 1 *b. High-Z to Logic 0*

Figure 8. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*

Figure 9. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals–a high pulse or a low pulse. Operation with a low pulse is shown in Figure 10. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 500ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

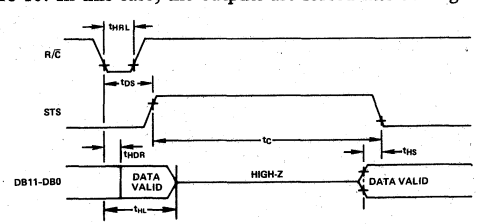


Figure 10. Low Pulse for R/$\overline{C}$ – Outputs Enabled After Conversion

If conversion is initiated by a high pulse as shown in Figure 11, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

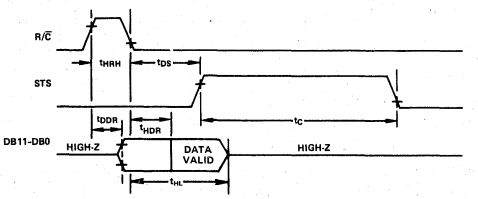


Figure 11. Low Pulse for R/$\overline{C}$ – Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			500	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HL}	Output Float Delay		110	150	ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	250			ns
t_{DDR}	Data Access Time			250	ns

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

Analog-to-digital converters, like any I/O device, may be interfaced to microprocessors by several methods. These methods include (but are not limited to) direct memory access, isolated or accumulator I/O, and memory-mapped I/O. Direct memory access (DMA) is the fastest, since conversions occur automatically and data updates into memory are transparent to the processor. DMA logic is very processor-dependent and makes use of dedicated specialized hardware.

Memory-mapped and accumulator I/O are more often used and somewhat easier to understand. Memory-mapped I/O assigns the I/O device to one or more locations in the memory space of the microprocessor. This technique has the advantage that the full range of memory reference instructions may be used to operate on the data. The potential disadvantages include limiting the memory space available for program and data memory, somewhat more complex address decoding and more difficult isolation of device select pulses for system debugging. Many processors offer only memory-mapped I/O.

Accumulator I/O uses a set of control signals which are distinct and different from the memory control signals. These control signals, combined with the address bus, serve to define a totally

separate I/O address space. This architecture is simpler from a hardware standpoint, since address decoding requirements are less severe and distinct I/O read and write pulses are more easily located for system debugging purposes. However, processors using accumulator I/O generally can only send data to an output device from the accumulator. This can make the software more cumbersome, since processor-controlled transfers of I/O device data to a memory location cannot be accomplished in a single instruction.

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the converter is done with its cycle, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8MSBs (DB11 through DB4). The odd address (A0 high) contains the 4LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

	D7							D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX1 (ODD ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

Figure 12. AD574A Data Format for 8-Bit Bus

It is not possible to rearrange the AD574A data lines for right-justified 8-bit bus interface.

The AD574A three-state buffers feature access times and data latency times comparable to presently-available memory devices. Therefore, the AD574A can interface directly to many processor buses without the need for wait states or external data buffers.

SPECIFIC PROCESSOR INTERFACE EXAMPLES

6800/6502–Type Systems

The control signals and bus architecture of the 6800 series and 6502 series microprocessors are very similar. In each, the state of the R/$\overline{W}$ signal at the rising edge of the Ø2 (or equivalent) clock establishes whether a memory read or write is in progress. The memory address being exercised is signaled by decoding the address bits to (usually) an active low signal.

This control structure is directly compatible with the AD574A. The R/$\overline{W}$ line can be used for R/$\overline{C}$, the active-low decoded base address (the AD574A occupies two memory locations) is applied to $\overline{CS}$, and Ø2 is used for CE. The least-significant address line ties to the AD574A A0 input.

In this interface, the processor can write to one address (A0 low) to start a full 12-bit conversion or another address (A0 high) to start a short 8-bit conversion. The contents of the data bus are meaningless during these writes. After sufficient time has passed for the conversion to complete, the processor can read the data in the two memory locations occupied by the AD574A. The even location (A0 low) contains the eight MSBs and the odd location contains the four LSBs and four trailing zeroes.

The AD574A may be used directly with 6800 series processors running at clock speeds up to 1.5MHz.

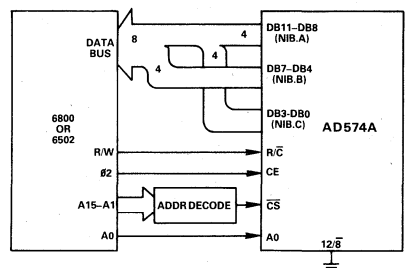


Figure 13. AD574A–6800/6502 Interface Connections

8085A Interface

The 8085A microprocessor uses a multiplexed address/data bus. At the beginning of a machine cycle, this bus contains the low byte of the address being exercised. The ALE output signal is available to strobe a latch to hold the low address byte. For the rest of the machine cycle, this bus carries data to or from the CPU.

The 8085A can use either accumulator I/O or memory-mapping for I/O devices. The system $\overline{RD}$ and $\overline{WR}$ are gated with IO/$\overline{M}$ to provide distinct I/O read and write signals and memory read and write signals. The control signals required for the AD574A are easily derived from the 8085A control bus. $\overline{CS}$ is taken from an address decoder on the high-order address bits. R/$\overline{C}$ can be taken from $\overline{WR}$ (either I/O write or memory write), A0 is tied to the LSB of the address bus, and CE is taken from the output of a NAND gate driven from $\overline{RD}$ and $\overline{WR}$. All bus access and float delay requirements are met for direct bus interface for 8085A clock rates up to 3MHz.

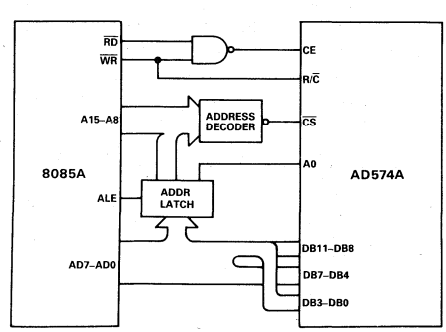


Figure 14. AD574A–8085A Direct Bus Interface

In 8085A systems running at high clock frequencies some external circuitry is required. First, the AD574A delay from CE going low to the data lines going into three-state will cause a bus conflict when the 8085A sends out the low byte of the next instruction address. This conflict will occur if the AD574A data outputs are tied directly to the 8085A bus. In systems where bus transceivers (e.g., 74LS245, 8286, etc.) are used to separate the address and data lines, the conflict is eliminated. The transceivers are disabled at the end of the read cycle and thus isolate the AD574A from the 8085A bus. Since most systems incorporate such buffers, this does not add to system complexity.

A second consideration when interfacing to higher speed 8085A systems is the width of the convert start pulse. The $\overline{WR}$ pulse from a 5MHz 8085A is only guaranteed to be 230 nanoseconds wide and is thus not long enough to initiate a conversion. There are two solutions to this problem. One possibility is to use a dual D-type flip-flop connected as shown in Figure 15 to insert a single wait state in read and write operations directed towards the AD574A. Another solution is to substitute the earlier-occurring S1 and S0 outputs from 8085A for $\overline{RD}$ and $\overline{WR}$ in the circuit of Figure 14 to generate the required control signals. It is important that bus transceivers be employed if S1 and S0 are used for control signals since these signals remain active longer than $\overline{RD}$ and $\overline{WR}$, enabling the AD574A output buffers in read operations for too long, causing potential bus conflicts.

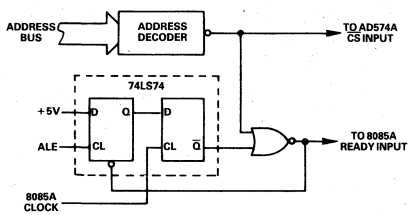


Figure 15. Wait State Generator for 5MHz 8085A Interface

Z-80 System Interface

The Z-80 series of 8-bit microprocessors, like the 8085A, offers both memory-mapped and accumulator I/O capability. While the 8085A only includes two instructions for accumulator I/O (IN and OUT), the Z-80 I/O instruction set is considerably more extensive.

The control signals available on the Z-80 include $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$. The $\overline{RD}$ and $\overline{WR}$ signals indicate direction of data flow while $\overline{MREQ}$ and $\overline{IORQ}$ determine whether the read or write cycle in progress is a memory or I/O cycle. During I/O reads and writes, only 8 address lines are active (as in the 8085A). An interesting feature of the Z-80 is that I/O read and write cycles are automatically extended by one clock cycle (one wait state is inserted) and are thus slower. The Z-80 control signal connections to the AD574A are identical to the 8085A connections.

The AD574A can be interfaced to Z-80 series processors with clock speeds up to 2.5MHz in the memory address space using the $\overline{MWR}$ and $\overline{MRD}$ signals. At higher clock rates (4 and 6MHz), the memory write pulse is not wide enough to properly start a conversion. The extra wait state added during I/O write operations will extend this pulse to a suitable width at clock rates up to 6MHz so that accumulator I/O is possible.

INTERFACING THE AD574A TO THE APPLE II COMPUTER

The AD574A can be used to provide a low-cost precision analog input port for the Apple II microcomputer without the need for additional power supplies or extensive digital interface logic. The AD574A can be mounted on a hobby card designed to plug into an Apple II I/O slot.

Hardware

All required supply voltages and control signals are available on the Apple's peripheral connectors. Each connector contains, on pin 41, a $\overline{DEVICE\ SELECT}$ output which is active when the address bus holds a hexadecimal address between C0n0 and C0nF, where n is equal to the slot number plus 8. This signal can be connected to pin 3 ($\overline{CS}$) of the AD574A. The Φ0 clock on pin 40 of the peripheral connector can be used for the AD574A CE input (pin 6). The AD574A R/$\overline{C}$ input (pin 5) can be driven directly by the R/$\overline{W}$ output available on peripheral connector pin 18. Pin 2 of the peripheral connector, A0, connects directly to the AD574A pin 4. The connections between the peripheral connector and the AD574A are shown in Figure 16.

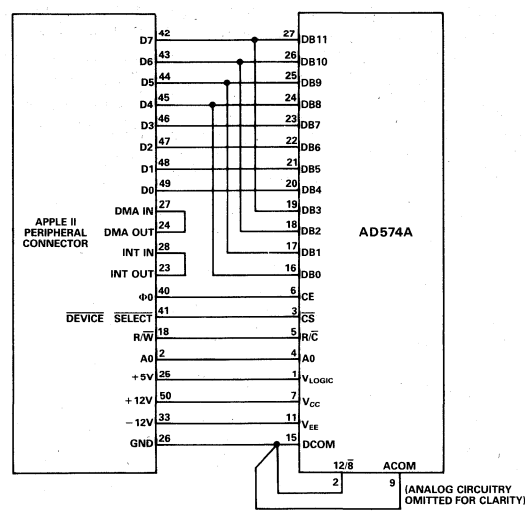


Figure 16. AD574A Connections to Apple II Peripheral Connector

The Apple II represents a relatively hostile electrical environment to the AD574A. The high frequency clocks radiate a large amount of noise which can be inadvertently coupled into analog signal lines. Furthermore, the switching power supply in the Apple is noisy, and this noise will often pollute the analog signals. It is possible, however, by judicious bypassing, decoupling, and ground management, to achieve a data acquisition system with only occasional flicker. A suggested grounding and decoupling scheme is shown in Figure 17.

It is recommended that any signal preamplification used in such a system be physically located outside the Apple cabinet. A full-scale signal range is less susceptible to electromagnetically coupled interference than a smaller signal range would be. Thus, the preferred method is to deliver a buffered, high-level signal to the AD574A through a shielded cable. The ±5V or ±10V

range is suggested. Full-scale and offset trims, if desired, are performed as shown on page 7.

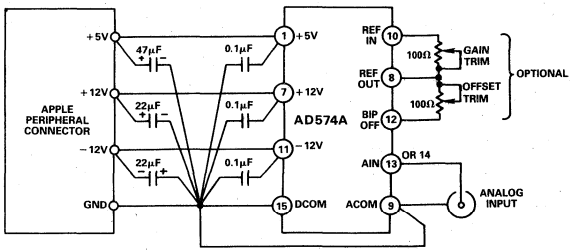


Figure 17. Recommended Grounding Procedure

Software

In this discussion, the AD574A is assumed to be located in I/O slot 2 of the Apple II and be the only device in that slot. The AD574A thus occupies the sixteen locations from $C0A0 through $C0AF, even though only two locations are actually required.

It is possible to operate the AD574A from either machine language or a high-level language. In machine language, the converter is started by writing data to either $C0A0 or $C0A1, using a STA instruction. Writing to $C0A0 will start a full 12-bit conversion cycle; writing to $C0A1 starts an 8-bit cycle. Accumulator contents are unimportant during convert start operations. It is then necessary to wait for the AD574A to finish converting before attempting to read the data. This can be accomplished by loading the accumulator with the value 02 and calling the WAIT subroutine located at $FCA8 in the Apple Monitor.

When data is read, it can be read only 8 bits at a time, as explained on page 10. The sample subroutine below starting at location $4000 performs the control for the AD574A and returns the result in RAM locations $0300 and $0301.

```
4000   A9 02       LDA   #$02
4002   8D A0 C0    STA   $C0A0
4005   20 A8 FC    JSR   $FCA8
4008   AD A0 C0    LDA   $C0A0
400B   8D 00 03    STA   $0300
400E   AD A1 C0    LDA   $C0A1
4012   8D 01 03    STA   $0301
4015   60          RTS
```

Figure 18. Assembly-Language AD574A Control Subroutine

Programs written in Applesoft Basic can also operate the AD574A. Conversion is started by POKEing into location 49312 decimal for a 12-bit conversion (or location 49313 for an 8-bit conversion). Basic executes slowly enough that no delay routines are needed. The output of the AD574A is read by PEEKing into those locations. In order to compute the actual analog voltage, it is necessary to establish the proper weighting for the two bytes read.

The Basic subroutine shown in Figure 19 will accomplish this arithmetic. This routine assumes a ±5V analog signal range and returns the value of actual analog signal voltage in the variable V.

```
100   POKE (49312)
110   A = PEEK (49312): B = PEEK (49313): C = 256
120   A = (A + B/C)/C
130   V = A*10 − 5
140   RETURN
```

Figure 19. Applesoft II Basic Subroutine for AD574A Control

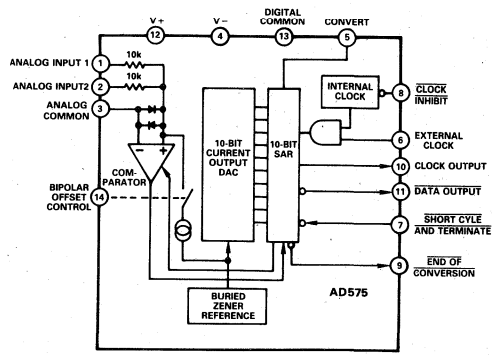
Fast, Complete, 10-Bit A/D Converter with Serial Output

AD575*

FEATURES

- **Complete 10-Bit A/D Converter with Reference, Clock and Comparator**
- **Serial Output**
- **Fast Successive Approximation Conversion – 20μs**
- **No Missing Codes Over Temperature**
- **Operates on +5V and −12V to −15V Supplies**
- **Low Cost Monolithic Construction**
- **Internal/External Clock Option**
- **Triggered or Continuous Conversions**
- **Automatic Short Cycle Option**

AD575 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD575 is a complete 10-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and serial interface–all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 20μs.

The AD575 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface zener reference.

Operating on supplies of +5V and −12V to −15V, the AD575 will accept analog inputs of 0V to +10V, 0V to +20V, −5V to +5V or −10V to +10V. The rising edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. Eleven clock pulses will appear at the CLOCK OUTPUT pin with data valid on the falling edges of the clock waveform. The data is presented serially at DATA OUTPUT beginning with the MSB which is valid on the falling edge of the second clock pulse. The part may be programmed to perform 8-bit conversions or short cycled to any desired data word width below 10-bits using the SHORT CYCLE AND TERMINATE line. END OF CONVERSION indicates the completion of the conversion. The AD575 may also be operated with an external clock if desired.

The AD575 is available in two versions for the 0 to +70°C temperature range, the AD575J and AD575K. The AD575S guarantees ±1LSB relative accuracy and no missing codes from −55°C to +125°C.

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

Two package configurations are offered. All versions are offered in a 14-pin hermetically sealed ceramic DIP. The AD575J and AD575K are also available in a 14-pin plastic DIP.

10

PRODUCT HIGHLIGHTS

1. The AD575 is a complete 10-bit A/D converter. No external components or control signals are required to perform a conversion.
2. The serial output of the AD575 allows a wide range of microprocessor interfacing and data transmission possibilities.
3. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD575 adapts to either unipolar or bipolar analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.

SPECIFICATIONS (T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD575J			AD575K			AD575S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION			10			10			10	Bits
RELATIVE ACCURACY, T_A[1]			±1			±1/2			±1	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
FULL SCALE CALIBRATION[2]		±2			±2				±2	LSB
UNIPOLAR OFFSET			±1			±1/2			±1	LSB
BIPOLAR OFFSET			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY, T_A	10			10			10			Bits
T_{min} to T_{max}	9			10			9			Bits
TEMPERATURE RANGE	0		+70	0		+70	−55		+125	°C
TEMPERATURE DRIFT ERRORS										
Unipolar Offset			±2			±1			±2	LSB
Bipolar Offset			±2			±1			±2	LSB
Full Scale Calibration[2]			±4			±2			±5	LSB
POWER SUPPLY REJECTION										
Positive Supply										
+4.5≤V+≤+5.5V			±2			±1			±2	LSB
Negative Supply										
−15.75V≤V−≤−14.25V			±2			±1			±2	LSB
−12.6V≤V−≤−11.4V			±2			±1			±2	LSB
ANALOG INPUT IMPEDANCE										
Pins 1 and 2	6	10	14	6	10	14	6	10	14	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
	0		+20	0		+20	0		+20	V
Bipolar	−5		+5	−5		+5	−5		+5	V
	−10		+10	−10		+10	−10		+10	V
OUTPUT CODING										
Unipolar	Negative True Binary			Negative True Binary			Negative True Binary			
Bipolar	Negative True Offset Binary			Negative True Offset Binary			Negative True Offset Binary			
LOGIC OUTPUTS										
Output Sink Current										
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			3.2			mA
Output Source Current[3]										
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			0.5			mA
LOGIC INPUTS										
Input Current			±100			±100			±100	μA
V_{INH}	2.0			2.0			2.0			V
V_{INL}			0.8			0.8			0.8	V
CONVERSION TIME[4]										
T_A and T_{min} to T_{max}	10	20	30	10	20	30	10	20	30	μs
POWER SUPPLY										
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	−11.4	−15	−16.5	+11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT										
V+		15	25		15	25		15	25	mA
V−		9	15		9	15		9	15	mA
PACKAGE[5]										
Ceramic DIP		D14A			D14A			D14A		
Plastic DIP		N14A			N14A					

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is specified with a 15Ω fixed resistor in series with the 10V input (Pins 1 and 2 tied together) or a fixed 30Ω resistor in series with the 20V input (either Pin 1 or 2 with the unused pin tied to analog common). Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω/30Ω resistor mentioned above. Full scale is defined as 10V for ±5V and 10V ranges and 20V for the ±10V and 0, 20V ranges.

[3]The data output lines have active pull-ups to source 0.5mA.

[4]Internally clocked mode.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Inputs to Analog Common	±22V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD575 ORDERING GUIDE

Model	Package Option	Temperature Range	Relative Accuracy
AD575JN	14-Pin Plastic DIP	0 to +70°C	±1LSB max
AD575KN	14-Pin Plastic DIP	0 to +70°C	± 1/2LSB max
AD575JD	14-Pin Ceramic DIP	0 to +70°C	±1LSB max
AD575KD	14-Pin Ceramic DIP	0 to +70°C	± 1/2LSB max
AD575SD	14-Pin Ceramic DIP	−55°C to +125°C	±1LSB max

FUNCTIONAL DESCRIPTION

A block diagram of the AD575 is shown in Figure 1. The positive convert pulse must be at least 300ns wide. $\overline{EOC}$ goes high within 300ns indicating that a conversion has started. The internal 10-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 10kΩ input resistor(s). The comparator determines whether the addition of each successively-weighted bit current causes the DAC current to sum to be greater or less than the input current, if the sum is less the bit is left on, ($\overline{DO}$ set low). If the sum is more, the bit is turned off ($\overline{DO}$ set high). The result of each bit decision is passed to $\overline{DO}$ as it is made with synchronizing information provided at CO.

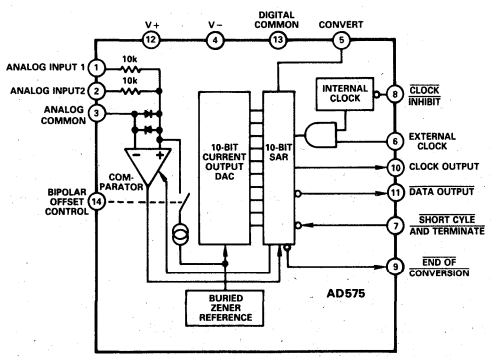


Figure 1. AD575 Functional Block Diagram

After testing all bits, the DAC output current will match the input signal current to within 0.05% (1/2LSB). The $\overline{EOC}$ returns low after the final bit decision to indicate that the AD575 has been reset and is ready to perform a new conversion. The output data stream can be synchronized to an external clock using the XCL input and short cycled to any desired word length using the $\overline{SCAT}$ line.

UNIPOLAR CONNECTION

The AD575 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), and the analog input. However, there are some features and special connections which are available to match a variety of applications and problems. The functional pinout is shown in Figure 2.

The unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 14) to digital common (pin 13), and applying the input signal to the parallel combination of the input resistors (Pins 1 and 2). The unipolar 0 to +20V input range is achieved by applying the input signal to Pin 1 and tying the unused input (Pin 2) to Analog Common (Pin 3).

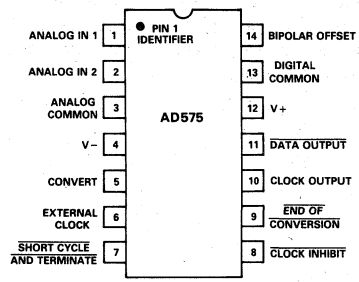


Figure 2. AD575 Pin Connections

Full Scale Calibration

The 10kΩ thin-film input resistors are laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.990 volts (10 volts – 1LSB) is applied to both inputs. The input resistors are trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the

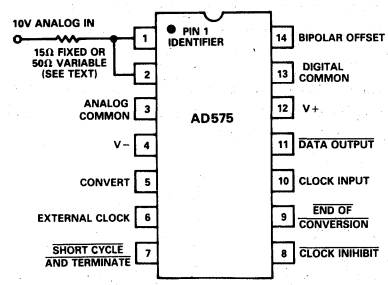


Figure 3. AD575 Pin Connections for 10V Full Scale Range

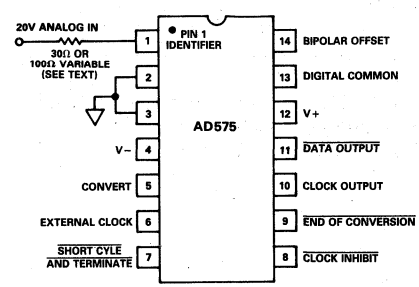


Figure 4. AD575 Pin Connections for 20V Full Scale Range

input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 10V and 20V full scale ranges can be achieved to sufficient accuracy by simply inserting a 15/30Ω resistor in series with the analog inputs. Typical full scale calibration error will then be within ±2LSB or ±0.2%. If more precise calibration is desired, a 50/100Ω trimmer should be used instead. Set the analog input at 9.990/19.980 volts, and set the trimmer so that the output code is just at the transition between (0000000001) and (0000000000).

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V or −10V to +10V input ranges with an offset binary output code, the bipolar offset control pin is left open. The nominal transfer curve is shown in Figure 5. Note that in the bipolar mode, the code transitions are offset by 1/2LSB such that an input voltage of 0V + 1/2LSB yields the code representing zero. Each output code is then centered on its nominal input range.

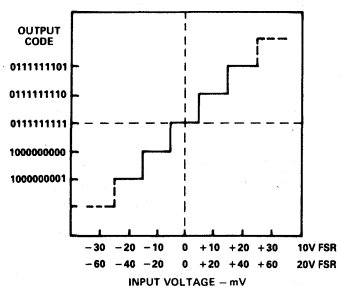


Figure 5. AD575 Transfer Curve Bipolar Operation

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.985 volts for −5V to +5V range or +9.990 volts for −10V to +10V range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 6.

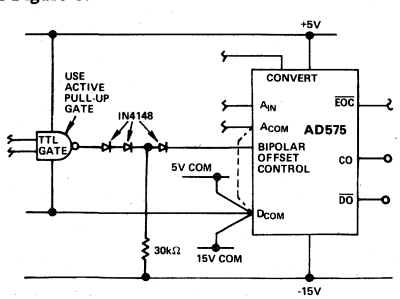


Figure 6. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar
Gate Output = 0 Bipolar

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD575

Many situations in high-speed data acquisition systems for digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD575, a SHA can also serve as a high input impedance buffer.

Figure 7 shows the AD575 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

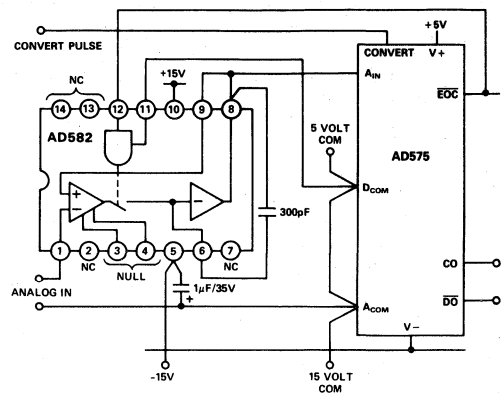


Figure 7. Sample-Hold Interface to the AD575

$\overline{EOC}$ goes high after the conversion is initiated to indicate that conversion is underway. In Figure 7 it is also used to put the AD582 into the hold mode while the AD575 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD575).

$\overline{EOC}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 7, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

GROUNDING CONSIDERATIONS

The AD575 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

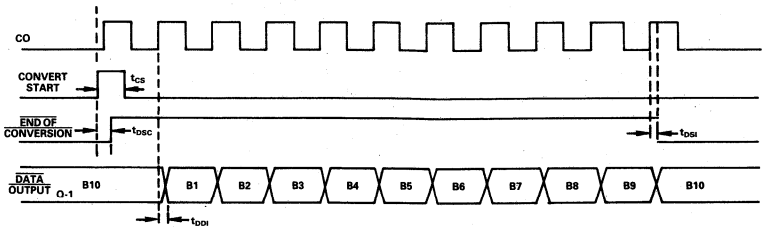


Figure 8a. AD575 Timing Diagram (Internal Clock)

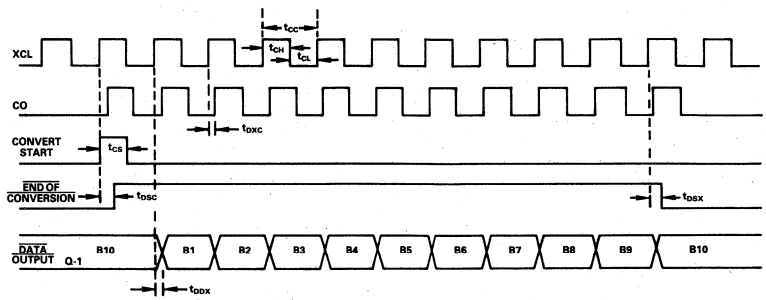


Figure 8b. AD575 Timing Diagram (External Clock)

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CONTROL AND TIMING OF THE AD573

The AD575 is controlled through four inputs: CONVERT, $\overline{\text{CLI}}$, XCL, and $\overline{\text{SCAT}}$.

The CONVERT line is used to initiate the conversion cycle. The SAR in the AD575 is reset at the end of each conversion cycle. A positive going pulse on the CONVERT line of at least 300ns duration will initiate a conversion. The $\overline{\text{CLI}}$ or clock inhibit line is tied low to inhibit the operation of the internal clock when an external clock (XCL) is to be used. The XCL line should be tied to +V (Pin 12) along with $\overline{\text{CLI}}$ if the internal clock is to be used.

The $\overline{\text{SCAT}}$ or the $\overline{\text{SHORT CYCLE AND TERMINATE}}$ line has two uses. If it is kept low for the duration of a conversion, the cycle will terminate at 8 bits. If it is held high at the beginning of a conversion, the cycle will end when $\overline{\text{SCAT}}$ is driven low.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 300ns wide. The rising edge of this pulse sets the $\overline{\text{EOC}}$ line high and starts the internal clock (or gates the external clock if used). Eleven clock pulses will be output from CO following a rising edge input on the CONVERT line. The least signficiant data bit from the previous conversion will remain at $\overline{\text{DO}}$ during the first clock pulse. The data is output in serial fashion at DO beginning with MSB which becomes valid 120ns after the rising edge of the second clock pulse. $\overline{\text{ECO}}$ is reset 120ns after the rising edge of the eleventh CO clock pulse. The SAR is reset as well preparing the converter for the next conversion. The least significant bit remains latched at $\overline{\text{DO}}$ following the conversion as noted earlier.

AD575 TIMING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	300	–	–	ns
CONVERT to $\overline{\text{EOC}}$ Delay	t_{DSC}	–	150	300	µs
Conversion Time	t_C	10	20	30	µs
Internal Clock Timing					
CO to $\overline{\text{DO}}$ Output Delay	t_{DDI}	–	70	120	ns
CO to $\overline{\text{EOC}}$ Reset Delay	t_{DSI}	–	70	120	ns
External Clock Timing					
XCL Period	t_{CC}	2.5	–	–	µs
XCL High	t_{CH}	500	–	–	ns
XCL Low	t_{CL}	500	–	–	ns
XCL to CO Output Delay	t_{DXC}	–	50	100	ns
XCL to $\overline{\text{DO}}$ Output Delay	t_{DDX}	–	150	300	ns
XCL to $\overline{\text{EOC}}$ Reset Delay	t_{DSI}	–	150	300	ns

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

FEATURES

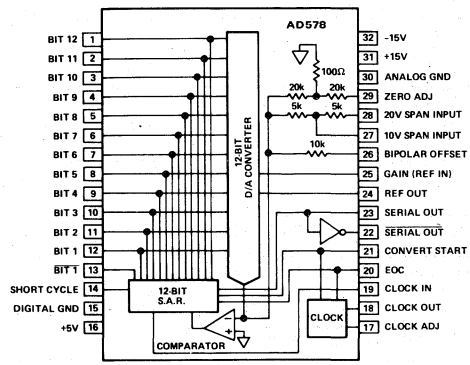
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Conversion: 3μs (max)
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max
- Max Nonlinearity: <±0.012%
- No Missing Codes Over Temperature
- Low Power: 875mW
- Hermetic Package Available

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12V Supplies

AD578 FUNCTIONAL BLOCK DIAGRAM



32 PIN DIP

10

GENERAL DESCRIPTION

The AD578 is a high speed 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 875mW and maximum conversion time of 3μs.

The fast conversion speeds of 3μs (L grade) 4.5μs (K grade) and 6μs (J grade) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 333kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available with either the polymer seal (N) for use in benign environmental applications or hermetic solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital signal processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typical T.C. The reference is available for external use and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The component count is minimized, resulting in low bond wire and chip count and high MTBF.
6. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
7. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Model	AD578J	AD578K	AD578L
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ	*	*
±10V, 0 to +20V	10kΩ	*	*
DIGITAL INPUTS			
Convert Command[1]	1LSTTL Load	*	*
Clock Input	1LSTTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR, ±0.25% FSR max	*	*
Unipolar Offset[3]	±0.1% FSR, ±0.25% FSR max	*	*
Bipolar Error[3,4]	±0.1% FSR, ±0.25% FSR max	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
DIFFERENTIAL LINEARITY ERRORS (Minimum resolution for which no missing codes are guaranteed)			
+25°C	12 Bits	*	*
T_{min} to T_{max}	12 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15V ±10%	0.005%/%ΔV_S max	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*
+5V ±10%	0.001%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±15ppm/°C typ	*	*
	±30ppm/°C max	*	*
Unipolar Offset	±3ppm/°C typ	*	*
	±10ppm/°C max	*	*
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	*	*
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5,6,7](max)	6.0μs	4.5μs	3μs
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10mV	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS[8]			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Supply Current +15V	3mA typ, 8mA max	*	*
−15V	22mA typ, 35mA max	*	*
+5V	100mA typ, 150mA max	*	*
Power Dissipation	875mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	*
Storage	−55°C to +150°C	*	*

NOTES

[1]Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2]With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3]Adjustable to zero.

[4]With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[5]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[6]Each grade is specified at the conversion speed shown.

[7]Externally adjustable by a resistor or capacitor (see Figure 7).

[8]For "Z" models order AD578ZJ, ZK, ZL (±11.6V to ±16.5V).

*Specifications same as AD578J.

Specifications subject to change without notice.

THEORY OF OPERATION

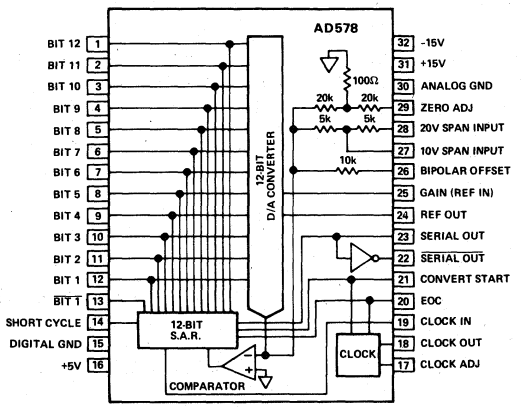


Figure 1. AD578 Functional Diagram and Pinout

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The parallel data bits become valid on the rising edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within $\pm$1/2LSB.

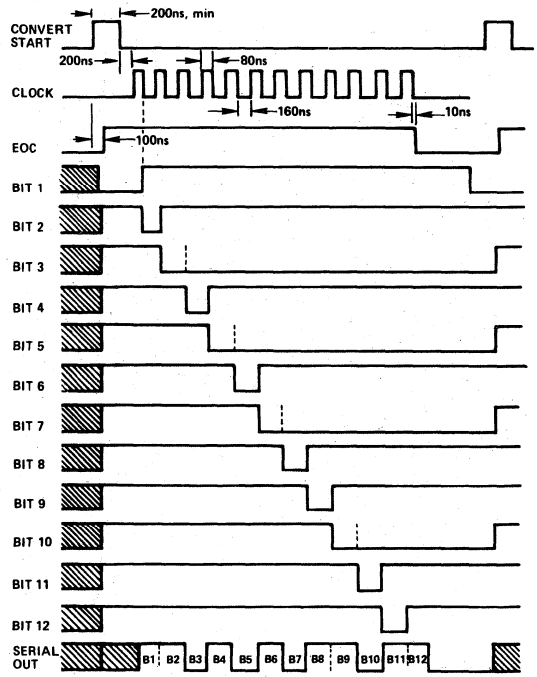
The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts $\pm$0.1%, it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately $\pm$25mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963V for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2. AD578 3μs Timing Diagram

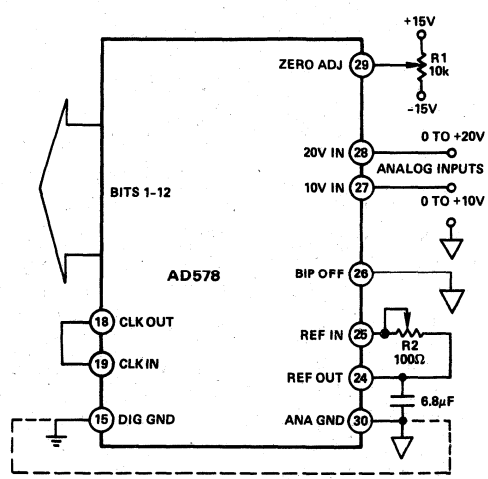


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (−4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

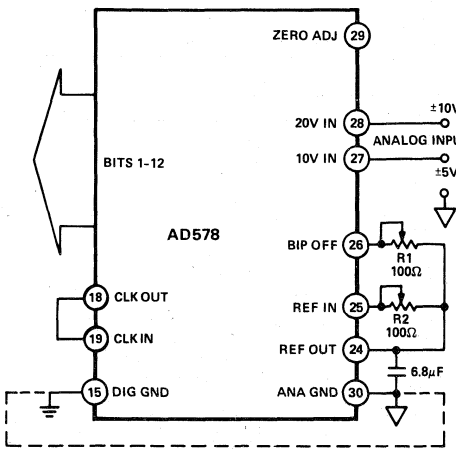


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD578's supply terminals should be capacitively decoupled as close to the AD578 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

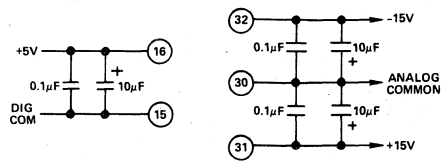


Figure 5. Basic Grounding Practice

To minimize noise the reference output (pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 6 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table II.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	−5V to +5V Range	−10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

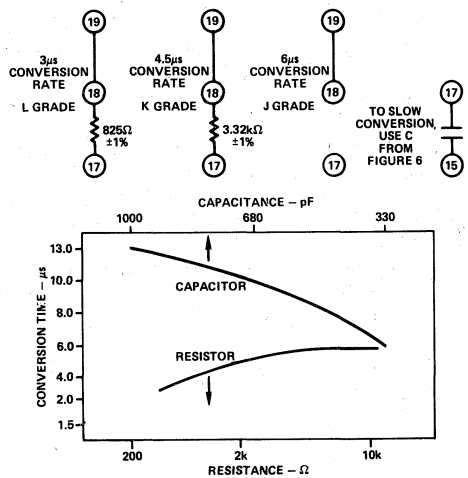


Figure 6. Conversion Times vs. R or C Values

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier – In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD507 should be used.

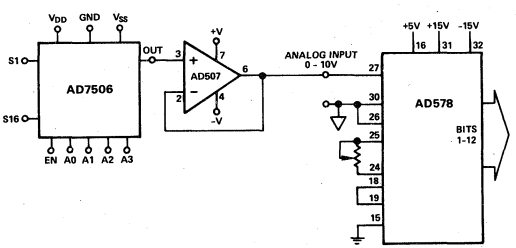


Figure 7. Input Buffer

MICROPROCESSOR INTERFACING

The 3μs conversion times of the AD578 suggests several different methods of interface to microprocessors. In systems where the AD578 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

In many multichannel data acquisition systems, the processor spends a good deal of time waiting for the ADC to complete its cycle. Converters with total conversion times of 25μs to 100μs are not slow enough to justify use of interrupts, nor fast enough to finish converting during one instruction and are usually timed out with loops, or continuously polled for status. The AD578 allows the microprocessor to time out the converter with just a few dummy instructions. For example, an 8085 system running at a 5MHz clock rate will time out an AD578 by pushing a register pair onto the stack and popping the same pair back off the stack. Such a time-out routine only occupies two bytes of program memory but requires 22 clock cyles (4.4μs). The time saved by not having to wait for the converter allows the processor to run much more efficiently particularly in multichannel systems.

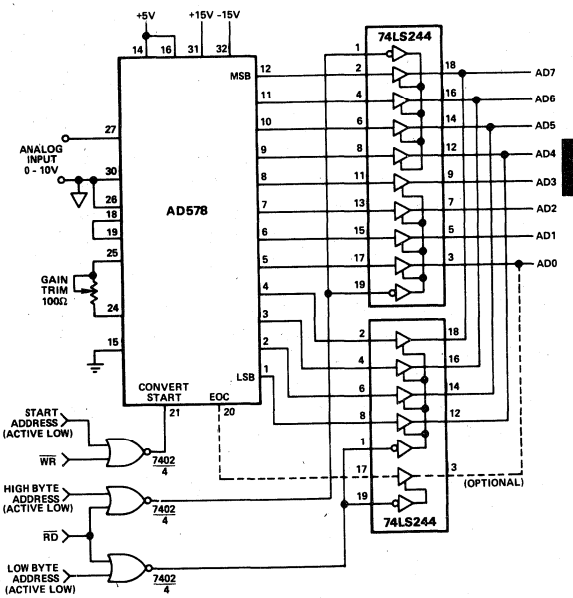


Figure 8. AD578–8085A Interface Connections

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSBs in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 8 shows a typical connection to an 8085-type bus, using left-justified data format for unipolar inputs. Status polling is

optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD578 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs ($\pm 5V$, $\pm 10V$ ranges), using the MSB directly yields an offset binary-coded output. If two's complement coding is desired, it can be produced by substituting $\overline{MSB}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

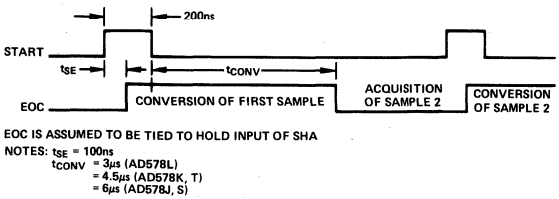


Figure 9. Start/EOC Timing for Sampled Data System

SAMPLED DATA SYSTEMS

The conversion speed of the AD578 allows accurate digitization of high frequency signals and high throughput rates in multi-channel data acquisition systems. The AD578LD, for example, is capable of a full accuracy conversion in 3μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 4μs. This means a sample rate of 250kHz can be realized, allowing a signal with no frequency components above 125kHz to be sampled with no loss of information. Note that the EOC signal from the AD578 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

AD578 ORDERING GUIDE*

	Conversion Speed	Temperature Range	Package	Option[1]
AD578JN(JD)	6.0μs	0 to +70°C	Polymer (Solder) Seal	HY32H
AD578KN(KD)	4.5μs	0 to +70°C	Polymer (Solder) Seal	HY32H
AD578LN(LD)	3.0μs	0 to +70°C	Polymer (Solder) Seal	HY32H

*For $\pm 12V$ operation "Z" version order: AD578ZJN, . . .

[1]See Section 19 for package outline information.

ANALOG DEVICES

Very Fast, Complete 10-Bit A/D Converter

AD579

FEATURES

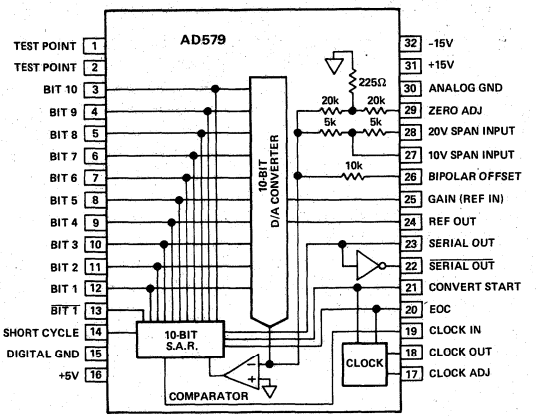
Performance

- Complete 10-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 1.8μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±40ppm/°C max
- Max Nonlinearity: <±0.048%
- Low Power: 775mW

Versatility

- Positive-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +10V Reference for External Applications
- Adjustable Internal Clock
- "Z" Models for ±12V Supplies

AD579 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD579 is a high speed low cost 10-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 10-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD579 include a maximum linearity error at +25°C of ±0.048%, maximum gain temperature coefficient of ±40ppm/°C, typical power dissipation of 775mW and maximum conversion time of 1.8μs.

The fast conversion speeds of 1.8μs (K and T grades) and 2.2μs (J grade) make the AD579 an excellent choice in a variety of applications where system throughput rates from 454kHz to 555kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD579 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD579 is available with either the polymer seal (N) for use in benign environmental applications or solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD579 is a complete 10-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD579 makes it an excellent choice for high speed data acquisition on systems requiring high throughput rate.
3. The internal buried zener reference is laser trimmed to 10.00V ±0.1% and ±15ppm/°C typ T.C. The reference is available externally and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
6. The integrated package construction provides high quality and reliability with small size and weight.

10

AD579 ORDERING GUIDE

Model	Conversion Speed	Package	Temperature Range	Power Supply Range	Package Outline[1]
AD579JN	2.2μs	Polymer-Seal	0 to +70°C	±15V ±10%	HY32H
AD579KN	1.8μs	Polymer-Seal	0 to +70°C	±15V ±10%	HY32H
AD579TD	1.8μs	Hermetic-Seal	-55°C to 125°C	±15V ±10%	HY32H
AD579ZJN	2.2μs	Polymer-Seal	0 to +70°C	±12V ±5%	HY32H
AD579ZKN	1.8μs	Polymer-Seal	0 to +70°C	±12V ±5%	HY32H
AD579ZTD	1.8μs	Hermetic-Seal	-55°C to +125°C	±12V ±5%	HY32H

[1] See Section 19 for package outline information.

SPECIFICATIONS (typical @ +25°C; ±15V, and +5V power supplies unless otherwise noted)

Model	AD579JN	AD579KN	AD579TD
RESOLUTION	10 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±5.0V, ±10V	*	*
Unipolar	0 to +10V, 0 to +20V	*	*
Input Impedance			
0 to +10V, ±5V	5kΩ (±20%)	*	*
±10V, 0 to +20V	10kΩ (±20%)	*	*
DIGITAL INPUTS			
Convert Command[1]	1LS TTL Load	*	*
Clock Input	1LS TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error[2,3]	±0.1% FSR (±0.25% FSR max)	*	*
Unipolar Offset[3]	±0.1% FSR (±0.25% FSR max)	*	*
Bipolar Offset[3,4]	±0.1% FSR (±0.25% FSR max)	*	*
Linearity Error			
+25°C	±1/2LSB max	*	*
T_{min} to T_{max}	±3/4LSB max	*	*
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)			
+25°C	10 Bits	*	*
T_{min} to T_{max}	10 Bits	*	*
POWER SUPPLY SENSITIVITY			
+15V ±10%	0.005%/%ΔV_S max	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*
+5V ±10%	0.001%/%ΔV_S max	*	*
"Z" Versions			
+12V ±5%	0.007%/%ΔV_S max	*	*
−12V ±5%	0.007%/%ΔV_S max	*	*
TEMPERATURE COEFFICIENTS			
Gain	±25ppm/°C typ	*	*
	±40ppm/°C max	*	*
Unipolar Offset	±5ppm/°C typ	*	*
	±15ppm/°C max	*	*
Bipolar Offset	±8ppm/°C typ	*	*
	±20ppm/°C max	*	*
Differential Linearity	±2ppm/°C typ	*	*
CONVERSION TIME[5,6] (max)	2.2μs	1.8μs	**
Conversion Time T_{min} to T_{max}	2.4μs	2.0μs	**
PARALLEL OUTPUTS			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2LSTTL Loads	*	*
SERIAL OUTPUTS (NRZ FORMAT)			
Unipolar Code	Binary/Complementary Binary	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*
Output Drive	2LSTTL Loads	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*
Output Drive	8LSTTL Loads	*	*
INTERNAL CLOCK[7]			
Output Drive	2LSTTL Loads	*	*
INTERNAL REFERENCE			
Voltage	10.000 ±10mV typ	*	*
Temperature Coefficient	15ppm/°C	*	*
External Current	±1mA max	*	*
POWER SUPPLY REQUIREMENTS			
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*
Supply Current +15V	3mA typ, 8mA max	*	*
−15V	22mA typ, 35mA max	*	*
+5V	100mA typ, 150mA max	*	*
Power Dissipation	775mW typ	*	*
TEMPERATURE RANGE			
Operating	0 to +70°C	*	−55°C to +125°C
Storage	−55°C to +150°C	*	*

NOTES

[1] Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[2] With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[3] Adjustable to zero.

[4] With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[5] Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[6] Each grade is specified at the conversion speed shown. See Figure 7 for appropriate connections.

[7] Externally adjustable by a resistor or capacitor.

[8] For "Z" models order AD579ZJN, AD579ZKN or AD579ZTD.

*Specifications same as AD579JN.

**Specifications same as AD579KN.

Specifications subject to change without notice.

THEORY OF OPERATION

The AD579 is a complete 10-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD579 is shown in Figure 1.

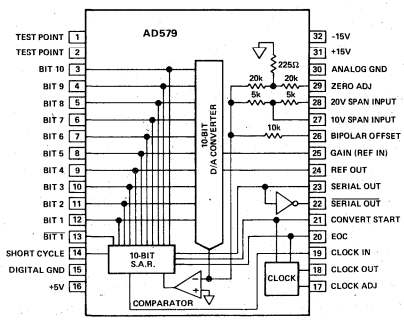


Figure 1. AD579 Functional Diagram and Pinout

On receipt of a CONVERT START command, the AD579 converts the voltage at its analog input into an equivalent bit binary number. This conversion is accomplished as follows: the 10-bit successive-approximation register (SAR) has its 10-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±0.1%; it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 10 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{10} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until Bit 10 (LSB) decision (keep) is made at t_{10}. After a 15ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to Logic "0" state.

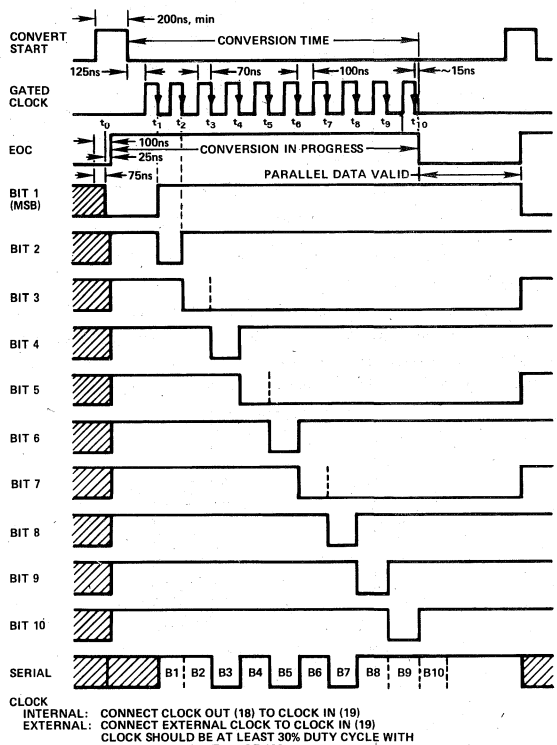


Figure 2. AD579 Timing Diagram

Serial data does not change and is guaranteed valid on negative-going clock edges, therefore; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 2).

Incorporation of this 15ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

UNIPOLAR CALIBRATION

The AD579 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 00 to 0000 0000 01) will occur for an input level of +1/2LSB (4.88mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±50mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.985V for a 10V range). Trim R2 to give the last transition (1111 1111 10 to 1111 1111 11).

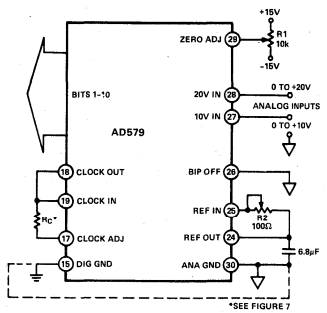


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (-4.9957V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 00 to 0000 0000 01). Then, a signel 1 1/2LSB below positive full scale (+4.9853V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 10 to 1111 1111 11).

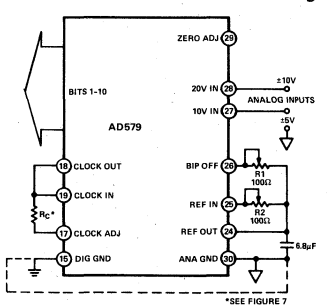


Figure 4. Bipolar Input Connections

ERROR SOURCES

The analog continuum is partitioned into 2^{10} discrete ranges for 10-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection.

The matching and tracking errors in the AD579 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR typical. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 3 and 4. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can having missing codes; the AD579TD is specified as having no missing codes from -55°C to +125°C and thus is monotonic.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

Analog Input — Volts (Center of Quantization Interval)				Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	-5V to +5V Range	-10V to +10V Range	B1 (MSB) B10 (LSB)
+9.9902	+19.9804	+4.9902	+9.9804	1111111111
+9.9804	+19.9609	+4.9804	+9.9609	1111111110
•	•	•	•	•
•	•	•	•	•
+5.0097	+10.0195	+0.0097	+0.0195	1000000001
+5.0000	+10.0000	+0.0000	+0.0000	1000000000
•	•	•	•	•
•	•	•	•	•
+0.0097	+0.0195	-4.9902	-9.9804	0000000001
+0.0000	+0.0000	-5.0000	-10.0000	0000000000

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

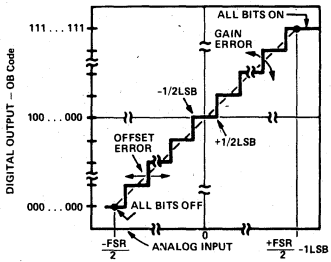


Figure 5. Transfer Characteristic for an Ideal Bipolar A/D

LAYOUT CONSIDERATIONS

Many data acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD579. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD579's supply terminals should be capacitively decoupled as close to the AD579 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

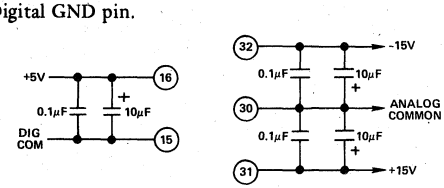


Figure 6. Basic Grounding Practice

To minimize noise the reference output (Pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 4.8μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

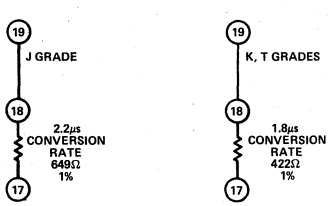


Figure 7. Clock Rate Control Connection

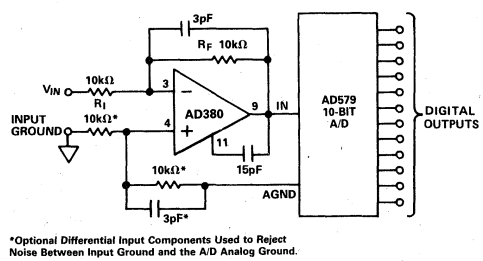
Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 10-bit resolution. Short cycle pin connections and associated maximum 10- and 8-bit conversion times are summarized in Table II.

Resolution (Bits)	10	8
Connect Pin 14 to Pin	2	4
Conversion Speed (μs)	1.8	1.5

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle.

External Buffer Amplifier – In applications where the AD579 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD380 should be used.



*Optional Differential Input Components Used to Reject Noise Between Input Ground and the A/D Analog Ground.

Figure 8. Input Buffer

SAMPLED DATA SYSTEMS

The conversion speed of the AD579 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD579TD, for example, is capable of a full accuracy conversion in 1.8μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 2.5μs. This means a sample rate of 400kHz can be realized, allowing a signal with no frequency components above 200kHz to be sampled with no loss of information. Note that the EOC signal from the AD579 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

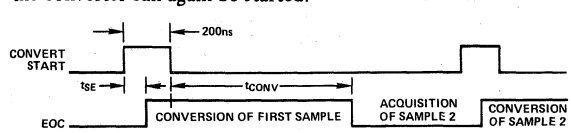


Figure 9. Start/EOC Timing for Sampled Data System

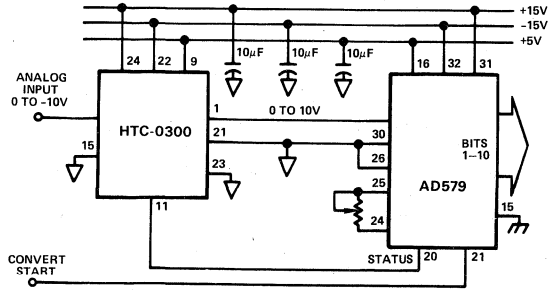


Figure 10. 400kHz – 10-Bit, A/D Conversion System

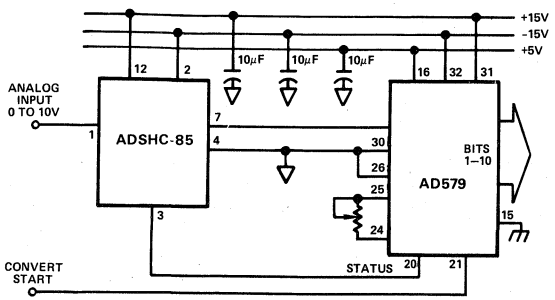


Figure 11. 154kHz – 10-Bit, A/D Conversion System

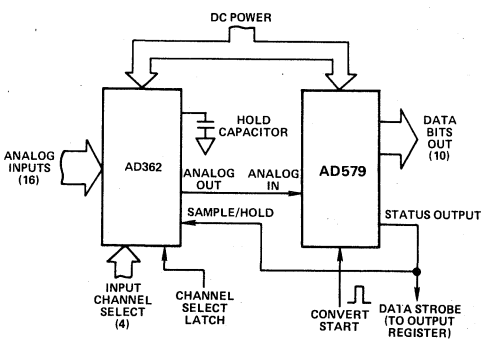


Figure 12. High Speed 10-Bit DAS

A fast (85kHz) 10-bit DAS can be configured using the AD362 and the AD579. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

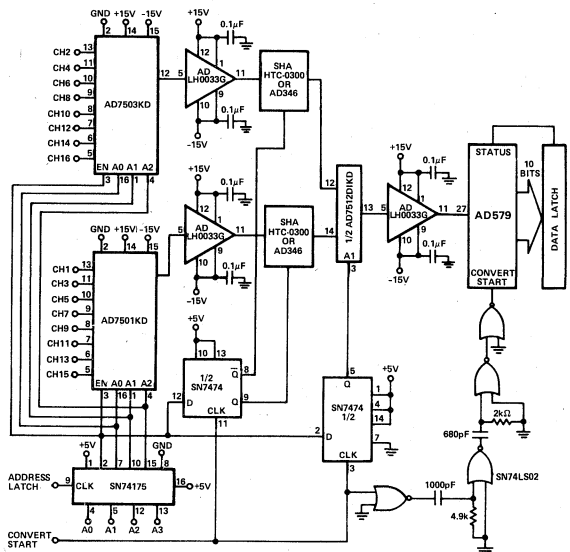


Figure 13. High Speed–165kHz–10-Bit DAS

A high speed 10-bit DAS with a throughput rate of 165kHz can be built around an AD579. The DAS of Figure 13 "Ping Pongs" two sample and hold amplifiers to eliminate the effects of the acquisition time of the sample and hold amplifiers. By applying sequential channel address the AO of the address enables one of the two multiplexers. The incorporation of the flip-flops on the SHA mode controls and the switch address allows a new channel address to be latched in while a conversion is in progress.

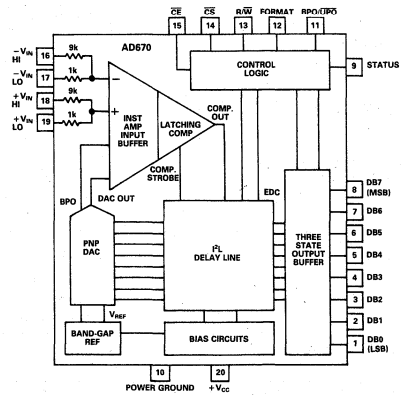
Low Cost Signal Conditioning 8-Bit ADC

AD670

FEATURES

Complete 8-Bit Signal Conditioning A/D Converter Including Instrumentation Amp, Reference, Comparator
Full Microprocessor Bus Interface
10μs Conversion Speed
Flexible Input Stage: Instrumentation Amp Front End Provides Differential Inputs and High Common-Mode Rejection
No User Trims Required
No Missing Codes Over Temperature
Single +5V Supply Operation
Convenient Input Ranges
Small 20-Pin Package
Low Cost Monolithic Construction

AD670 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD670 analog-to-digital converter is a complete 8-bit signal conditioning successive approximation analog-to-digital converter. It consists of an instrumentation amplifier front end along with a DAC, comparator, successive approximation register (SAR), precision voltage reference, and a three-state output buffer on a single monolithic chip. No external components or user trims are required to interface, with full accuracy, an analog system to an 8-bit data bus. The AD670 will operate off of the +5V system supply. The input stage provides differential inputs with excellent common-mode rejection and allows direct interface to a variety of transducers.

The device is configured with input scaling resistors to permit four input ranges: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB). The AD670 can be configured for both unipolar and bipolar inputs over these ranges. The voltage to current conversion on the input is completed by using the on-board instrumentation amplifier. The differential inputs and common-mode rejection of this front end are useful in applications such as amplification of transducer signals superimposed on common-mode voltages.

The AD670 incorporates advanced circuit design and proven processing technology. The successive approximation function is implemented with I^2L (integrated injection logic). Thin-film SiCr resistors provide the stability required to prevent missing codes over the entire operating temperature range while laser wafer trimming of the resistor ladder permits calibration of the device to within ±1LSB. Thus, no user trims for gain or offset are required. Conversion time of the device is 10μs.

The AD670 is available in two package types and five grades: the AD670JN and AD670KN, in 20-pin plastic DIP packages are specified over 0 to +70°C while the AD670AD and AD670BD (−25°C to +85°C) are in 20-pin ceramic packages. A military grade designated as the AD670SD and specified over the −55°C to +125°C temperature range is available in the 20-pin ceramic package.

10

PRODUCT HIGHLIGHTS

1. The AD670 is a complete 8-bit A/D including three-state outputs and microprocessor control for direct connection to 8-bit data buses. No external components are required to perform a conversion.
2. The flexible input stage features a differential instrumentation amp input with excellent common-mode rejection. This allows direct interface to a variety of transducers without preamplification.
3. No user trims are required for 8-bit accurate performance.
4. Operation from a single +5V supply allows the AD670 to run off of the microprocessor's supply.
5. Four convenient input ranges are available through internal scaling resistors: 0 to 255mV (1mV/LSB) and 0 to 2.55V (10mV/LSB).
6. Software control of the output mode is provided. The user can easily select unipolar or bipolar inputs and binary or 2's complement output codes.

SPECIFICATIONS (@ V_{CC} = +5V and +25°C unless otherwise noted)

Model	AD670J Min	AD670J Typ	AD670J Max	AD670K Min	AD670K Typ	AD670K Max	Units
OPERATING TEMPERATURE RANGE	0		+70	0		+70	°C
RESOLUTION	8			8			Bit
CONVERSION TIME – T_{min} to T_{max}			**10**			**10**	µs
RELATIVE ACCURACY							
T_{min} to T_{max}			**±1/2**			**±1/4**	LSB
DIFFERENTIAL LINEARITY ERROR							
T_{min} to T_{max}			**GUARANTEED NO MISSING CODES ALL GRADES**				
FULL SCALE ACCURACY							
@ +25°C			**±1.5**			**±0.5**	LSB
T_{min} to T_{max}			±2.5			±1.0	LSB
UNIPOLAR ZERO ERROR							
@ +25°C			**±1.0**			**±0.5**	LSB
T_{min} to T_{max}			±2.0			±1.0	LSB
BIPOLAR ZERO ERROR[1]							
@ +25°C			**±1.0**			**±0.5**	LSB
T_{min} to T_{max}			±2.0			±1.0	LSB
ANALOG INPUT RANGES							
All Grades		0 to +255			0 to +255		mV
		−128 to +127			−128 to +127		mV
		0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27		V
BIAS CURRENT (255mV RANGE)							
T_{min} to T_{max}		200	**500**		200	**500**	nA
OFFSET CURRENT (255mV RANGE)							
T_{min} to T_{max}		20	**100**		20	**100**	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH							
+ AND − INPUT		±1/2			±1/2		LSB
COMMON-MODE RANGE (V_{CC} = 4.5V)							
255mV RANGE							
@ +25°C	**−0.2**		**+1.4**	**−0.2**		**+1.4**	V
T_{min} to T_{max}	**0**		**+1.0**	**0**		**+1.0**	V
COMMON-MODE REJECTION							
RATIO (255mV RANGE)			**1**			**1**	LSB
COMMON-MODE REJECTION							
RATIO (2.55V RANGE)			**1**			**1**	LSB
POWER SUPPLY							
Operating Range	**4.5**		**5.5**	**4.5**		**5.5**	V
Current I_{CC}		30	**45**		30	**45**	mA
Rejection Ratio			**0.015**			**0.015**	% of FS/%
DIGITAL OUTPUT (V_{OUT} = 0.4V)							
SINK CURRENT							
@ +25°C	**1.6**			**1.6**			mA
T_{min} to T_{max}	**1.6**			**1.6**			mA
SOURCE CURRENT (V_{OUT} = 2.4V)							
@ +25°C	**0.5**			**0.5**			mA
T_{min} to T_{max}	**0.5**			**0.5**			mA
THREE-STATE LEAKAGE CURRENT			**±40**			**±40**	µA
OUTPUT CAPACITANCE		5			5		pF
DIGITAL INPUT VOLTAGE							
V_{INL}			**0.8**			**0.8**	V
V_{INH}	**2.0**			**2.0**			V
INPUT CURRENT ($0 \le V_{IN} \le +5V$)							
I_{INL}	**−100**			**−100**			µA
I_{INH}			**+100**			**+100**	µA
INPUT CAPACITANCE		10			10		pF

NOTES

[1]Refer to Figure 5 for characterization.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD670A			AD670B			AD670S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OPERATING TEMPERATURE RANGE	−25		+85	−25		+85	−55		+125	°C
RESOLUTION	8			8			8			Bit
CONVERSION TIME – T_{min} to T_{max}			10			10			10	µs
RELATIVE ACCURACY										
T_{min} to T_{max}			±1/2			±1/4		±1/4	±1/2	LSB
DIFFERENTIAL LINEARITY ERROR										
T_{min} to T_{max}	GUARANTEED NO MISSING CODES ALL GRADES									
FULL SCALE ACCURACY										
@ +25°C			±1.5			±0.5			±0.5	LSB
T_{min} to T_{max}			±2.5			±1.0			±2.0	LSB
UNIPOLAR ZERO ERROR										
@ +25°C			±1.0			±0.5			±0.5	LSB
T_{min} to T_{max}			±2.0			±1.0			±1.0	LSB
BIPOLAR ZERO ERROR[1]										
@ +25°C			±1.0			±0.5			±0.5	LSB
T_{min} to T_{max}			±2.0			±1.0			±1.0	LSB
ANALOG INPUT RANGES										
All Grades		0 to +255			0 to +255			0 to +255		mV
		−128 to +127			−128 to +127			−128 to +127		mV
		0 to +2.55			0 to +2.55			0 to +2.55		V
		−1.28 to +1.27			−1.28 to +1.27			−1.28 to +1.27		V
BIAS CURRENT (255mV RANGE)										
T_{min} to T_{max}		200	500		200	500		200	500	nA
OFFSET CURRENT (255mV RANGE)										
T_{min} to T_{max}		20	100		20	100		20	100	nA
2.55V RANGE INPUT RESISTANCE	8.0		12.0	8.0		12.0	8.0		12.0	kΩ
2.55V RANGE FULL SCALE MATCH										
+ AND − INPUT		±1/2			±1/2			±1/2		LSB
COMMON-MODE RANGE (V_{CC} = 4.5V)										
255mV RANGE										
@ +25°C	−0.2		+1.4	−0.2		+1.4	−0.2		+1.4	V
T_{min} to T_{max}	0		+1.0	0		+1.0	0		+1.0	V
COMMON-MODE REJECTION										
RATIO (255mV RANGE)			1			1			1	LSB
COMMON-MODE REJECTION										
RATIO (2.55V RANGE)			1			1			1	LSB
POWER SUPPLY										
Operating Range	4.5		5.5	4.5		5.5	4.5		5.5	V
Current I_{CC}		30	45		30	45		30	45	mA
Rejection Ratio			0.015			0.015			0.015	% of FS/%
DIGITAL OUTPUT (V_{OUT} = 0.4V)										
SINK CURRENT	1.6			1.6			1.6			mA
T_{min} to T_{max}	1.6			1.6			1.6			mA
SOURCE CURRENT (V_{OUT} = 2.4V)										
@ +25°C	0.5			0.5			0.5			mA
T_{min} to T_{max}	0.5			0.5			0.5			mA
THREE-STATE LEAKAGE CURRENT			±40			±40			±40	µA
OUTPUT CAPACITANCE		5			5			5		pF
DIGITAL INPUT VOLTAGE										
V_{INL}			0.8			0.8			0.7	V
V_{INH}	2.0			2.0			2.0			V
INPUT CURRENT (0≤V_{IN}≤+5V)										
I_{INL}	−100			−100			−100			µA
I_{INH}			+100			+100			+100	µA
INPUT CAPACITANCE		10			10			10		pF

NOTES

[1]Refer to Figure 5 for characterization.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

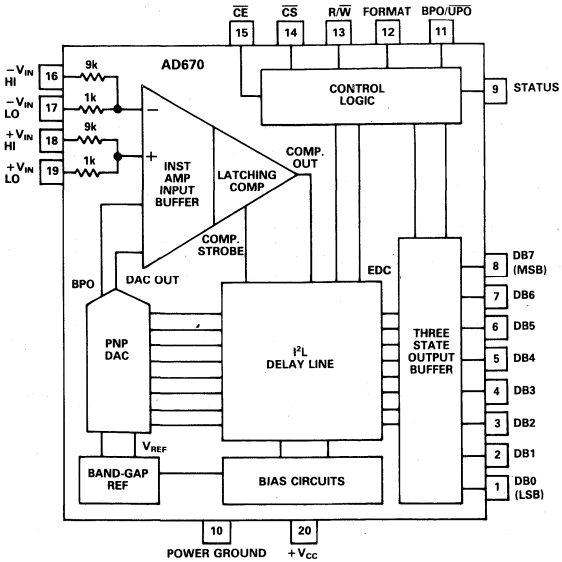


Figure 1a. AD670 Block Diagram

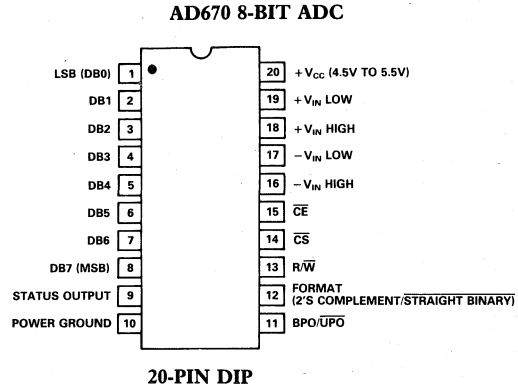


Figure 1b. AD670 Pin Connections

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Ground . . . . . 0V to +7.5V
Digital Inputs (Pins 11-15) . . . . . −0.5V to V_{CC} +0.5V
Digital Outputs (Pins 1-9) . Momentary Short to V_{CC} or Ground
Analog Inputs (Pins 16-19) . . . . . −30V to +30V
Power Dissipation 450mW
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . +300°C

AD670 ORDERING GUIDE

Model	Temperature Range	Relative Accuracy Max (T_{min} to T_{max})	Full Scale Accuracy (T_{min} to T_{max})	Package[1] Type
AD670JN	0 to +70°C	±1/2LSB	±2.5LSB	Plastic DIP (N20A)
AD670KN	0 to +70°C	±1/4LSB	±1.0LSB	Plastic DIP (N20A)
AD670AD	−25°C to +85°C	±1/2LSB	±2.5LSB	Ceramic DIP (D20A)
AD670BD	−25°C to +85°C	±1/4LSB	±1.0LSB	Ceramic DIP (D20A)
AD670SD	−55°C to +125°C	±1/2LSB	±2.0LSB	Ceramic DIP (D20A)

[1]See Section 19 for package outline information.

CIRCUIT OPERATION/FUNCTIONAL DESCRIPTION

The AD670 is a functionally complete 8-bit signal conditioning A/D converter with microprocessor compatibility. A block diagram and pin out are shown in Figures 1a. and 1b. The input section uses an instrumentation amplifier to accomplish the voltage to current conversion. This front end provides a high impedance, low bias current differential amplifier. The ground inclusive common-mode range allows the user to directly interface the device to a variety of transducers.

The A/D is signaled to begin a conversion using the three input signals, R/$\overline{W}$, $\overline{CS}$, and $\overline{CE}$. The R/$\overline{W}$ line directs the converter to read or start a conversion. A minimum write/start pulse of 300ns is required on either $\overline{CE}$ or $\overline{CS}$. The conversion thus begun, the internal 8-bit DAC is sequenced from MSB to LSB using a novel successive approximation technique. In conventional designs, the DAC is stepped through the bits by a clock. This can be thought of as a static design since the speed at which the DAC is sequenced is determined solely by the clock. No clock is used in the AD670. Instead, a "dynamic SAR" is created consisting of a string of inverters with taps along the delay line. Sections of the delay line between taps act as one shots. The pulses are used to set and reset the DAC's bits and strobe the comparator. When strobed, the comparator then determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current. If the sum is less, the bit is turned off. After all bits are tested, the SAR holds an 8-bit code representing the input signal to within 1/2LSB accuracy. Ease of implementation and reduced dependence on process related variables make this an attractive approach to a successive approximation design.

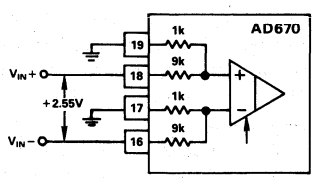
The SAR provides an end-of-conversion signal to the control logic which then brings the STATUS line low. Data outputs remain in a high impedance state until edge-triggered by a signal sent to the R/$\overline{W}$ line; R/$\overline{W}$ is then brought high with $\overline{CE}$ and $\overline{CS}$ low and allows the converter to be read. Bringing $\overline{CE}$ or $\overline{CS}$ high during the valid data period ends the read cycle. The output buffers cannot be enabled during a conversion. Any convert start commands will be ignored until the conversion cycle is completed; once a conversion cycle has been started it cannot be stopped or restarted.

The AD670 provides the user with a great deal of flexibility by offering two input spans and formats and a choice of output codes. Input format and input range can each be selected. The BPO/$\overline{\text{UPO}}$ pin controls a switch which injects a bipolar offset current of a value equal to the MSB less 1/2LSB into the summing node of the comparator to offset the DAC output. Two precision 10 to 1 attenuators are included on board to provide input range selection of 0 to 2.55V or 0 to 255mV. Additional ranges of −1.28 to 1.27V and −128 to 127mV are possible if the BPO/$\overline{\text{UPO}}$ switch is high when the conversion is started. Finally, output coding can be chosen using the FORMAT pin when the conversion is started. In the bipolar mode and a logic 1 on FORMAT, the output is in two's complement; with a logic 0, the output is offset binary.

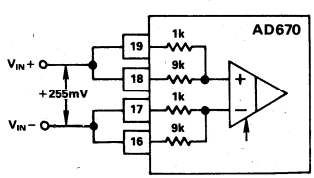
CONNECTING THE AD670

The AD670 has been designed for ease of use. All active components required to perform a complete A/D conversion are on board and are connected internally. In addition, all calibration trims are performed at the factory assuring specified accuracy without user trims. There are, however, a number of options and connections that should be considered to obtain maximum flexibility from the part.

Standard connections are shown in the figures that follow. An input range of 0 to 2.55V may be configured as shown in Figure 2a. This will provide a one LSB change for each 10mV of input change. The input range of 0 to 255mV is configured as shown in Figure 2b. In this case, each LSB represents 1mV of input change. As in Figure 2, when unipolar input signals are used, Pin 11, BPO/$\overline{\text{UPO}}$, should be grounded. Pin 11 selects the input format for either unipolar or bipolar signals. Figures 3a and 3b show the input connections for bipolar signals. Pin 11 should be tied to $+V_{CC}$ for bipolar inputs.



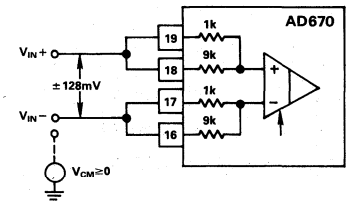
2a. 0 to 2.55V (10mV/LSB)



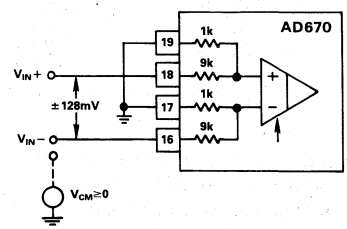
2b. 0 to 255mV (1mV/LSB)

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE HIGH WHEN CONVERSION IS STARTED.

Figure 2. Unipolar Input Connections



3a. ±1.28V Range



3b. ±128mV Range

NOTE: PIN 11, BPO/$\overline{\text{UPO}}$ SHOULD BE LOW WHEN CONVERSION IS STARTED.

Figure 3. Bipolar Input Connections

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Although the instrumentation amplifier has a differential input, there must be a return path to ground for the bias currents. If it is not provided, those currents will charge stray capacitances and cause the output to drift uncontrollably or saturate. Such a return path is provided in Figures 2a and 3a (the larger input ranges) since the 1k register leg is tied to ground. This is not the case for Figures 2b and 3b (the lower input ranges). Therefore, when amplifying outputs of floating sources, such as transformers and ac-coupled sources, there must still be a dc path from each input to common.

Input/Output Options

Data output coding (2's complement vs. straight binary) is selected using the FORMAT pin. The selection of input format (bipolar vs. unipolar) is controlled using Pin 11, BPO/$\overline{\text{UPO}}$. Prior to a write/convert, the state of FORMAT and BPO/$\overline{\text{UPO}}$ should be available to the converter. These lines may be tied to the data bus and may be changed with each conversion if desired. BPO/$\overline{\text{UPO}}$ controls the bipolar offset current. A logic 0 on this input sets up the AD670 for a unipolar input range and a logic 1 sets up the bipolar range. These choices are shown in Table I.

BPO/$\overline{\text{UPO}}$	FORMAT	INPUT FORMAT/OUTPUT CODE
0	0	Unipolar/Straight Binary
1	0	Bipolar/Offset Binary
0	1	Unipolar/2's Complement
1	1	Bipolar/2's Complement

Table I. AD670 Input Selection/Output Format Truth Table

An output signal, STATUS, indicates the status of the conversion. STATUS goes high at the beginning of the conversion and returns low when the conversion cycle has been completed.

Output coding can be selected for the AD670 by using Pin 12, the FORMAT pin. Holding FORMAT high when starting a conversion will give a 2's complement output. Holding FORMAT low will give an offset binary output. Coding for each of these outputs is shown in Figures 4a and 4b.

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	STRAIGHT BINARY (FORMAT = 0, BPO/$\overline{UPO}$ = 0)
0	0	0	0000 0000
128mV	0	128mV	1000 0000
255mV	0	255mV	1111 1111
255mV	255mV	0	0000 0000
128mV	127mV	1mV	0000 0001

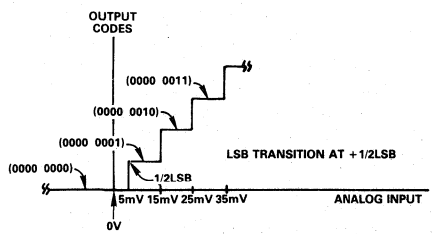
Figure 4a. Unipolar Output Codes

$+V_{IN}$	$-V_{IN}$	DIFF V_{IN}	OFFSET BINARY (FORMAT = 0, BPO/$\overline{UPO}$ = 1	2's COMPLEMENT (FORMAT = 1, BPO/$\overline{UPO}$ = 1
0	0	0	1000 0000	0000 0000
128mV	0	128mV	1111 1111	0111 1111
255mV	127mV	128mV	1111 1111	0111 1111
255mV	255mV	0	1000 0000	0000 0000
128mV	127mV	1mV	1000 0001	0000 0001
127mV	128mV	−1mV	0111 1111	1111 1111
127mV	255mV	−128mV	0000 0000	1000 0000

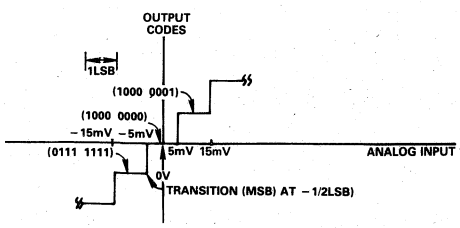
Figure 4b. Bipolar Output Codes

Calibration

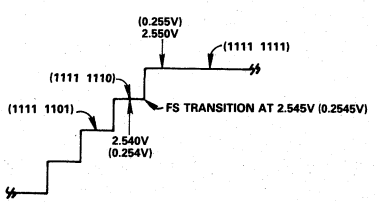
Because of its precise factory calibration, the AD670 is intended to be operated without user trims for gain and offset; therefore, no provisions have been made for such user-trims. Figures 5a, 5b, and 5c show the transfer curves at zero and full scale for the unipolar and bipolar modes. The code transitions are positioned so that the desired value is centered at that code. The first LSB transition for the unipolar mode occurs for an input of +1/2LSB (5mV or 0.5mV). Similarly, the MSB transition for the bipolar mode is set at −1/2LSB (−5mV or −0.5mV). The full scale transition is located at the full scale value −1 1/2LSB. These values are 2.545V and 254.5mV.



a. Unipolar Offset



b. Bipolar Offset



c. Full Scale

Figure 5. Transfer Curves

CONTROL AND TIMING OF THE AD670

Control Logic

The AD670 contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 6 shows the internal logic circuitry of the AD670. The control signals, $\overline{CE}$, $\overline{CS}$, and R/$\overline{W}$ control the operation of the converter. The read or write function is determined by R/$\overline{W}$ when both $\overline{CS}$ and $\overline{CS}$ are low as shown in Table II. If all three control inputs are held low longer than the conversion time, the device will continuously convert until one input, $\overline{CE}$, $\overline{CS}$, or R/$\overline{W}$ is brought high. The relative timing of these signals is discussed later in this section.

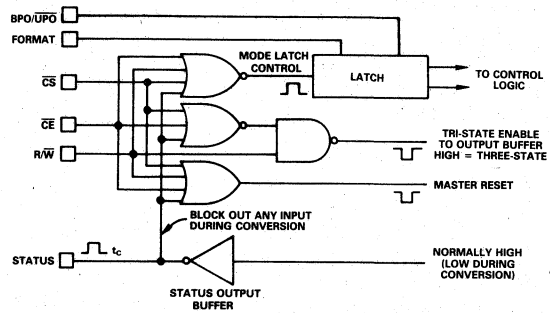


Figure 6. Control Logic Block Diagram

R/$\overline{W}$	$\overline{CS}$	$\overline{CE}$	OPERATION
0	0	0	WRITE/CONVERT
1	0	0	READ
X	X	1	NONE
X	1	X	NONE

Table II. AD670 Control Signal Truth Table

Timing

The AD670 is easily interfaced to a variety of microprocessors and other digital systems. Discussion of the timing requirements of the AD670 control signals will provide the designer with useful insight into the operation of the device.

Write/Convert Start Cycle

Figure 7 shows a complete timing diagram for the write/convert start cycle. $\overline{CS}$ (chip select) and $\overline{CE}$ (chip enable) are active low and are interchangeable signals. Both $\overline{CS}$ and $\overline{CE}$ must be low for the converter to read or start a conversion. The minimum pulse width, t_W, on either $\overline{CS}$ or $\overline{CE}$ is 300ns to start a conversion.

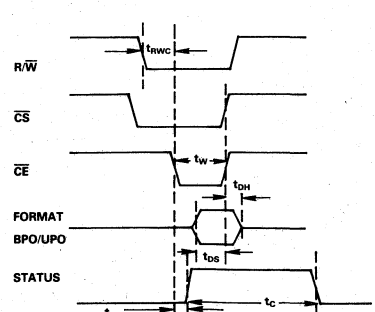


Figure 7. Write/Convert Start Timing

The R/$\overline{W}$ line is used to direct the converter to start a conversion (R/$\overline{W}$ low) or read data (R/$\overline{W}$ high). The relative sequencing of the three control signals (R/$\overline{W}$, $\overline{CE}$, $\overline{CS}$) is unimportant. However, when all three signals remain low for at least 300ns (t_W), STATUS will go high to signal that a conversion is taking place.

Once a conversion is started and the STATUS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffer cannot be enabled during a conversion.

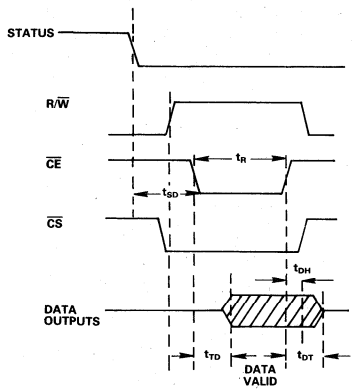


Figure 8. Read Cycle Timing

Read Cycle

Figure 8 shows the timing for the data read operation. The data outputs are in a high impedance state until a read cycle is initiated. To begin the read cycle, R/$\overline{W}$ is brought high. During a read cycle, the minimum pulse length for $\overline{CE}$ and $\overline{CS}$ is a function of the length of time required for the output data to be valid. The data becomes valid and is available to the data bus in a maximum of 250ns. This delay between the high impedance state and valid data is the maximum bus access time or t_{TD}. Bringing $\overline{CE}$ or $\overline{CS}$ high during valid data ends the read cycle. The outputs remain valid for a minimum of 10ns (t_{DH}) and return to the high impedance state after a delay, t_{DT}, of 150ns maximum.

STAND-ALONE OPERATION

The AD670 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available. Two typical conditions are described and illustrated by the timing diagrams which follow.

Single Conversion, Single Read

When the AD670 is used in a stand-alone mode, $\overline{CS}$ and $\overline{CE}$ should be tied together. Conversion will be initiated by bringing R/$\overline{W}$ low. Within 700ns, a conversion will begin. The R/$\overline{W}$ pulse should be brought high again once the conversion has started so that the data will be valid upon completion of the conversion. Data will remain valid until $\overline{CE}$ and $\overline{CS}$ are brought high to indicate the end of the read cycle. The timing diagram is shown in Figure 9.

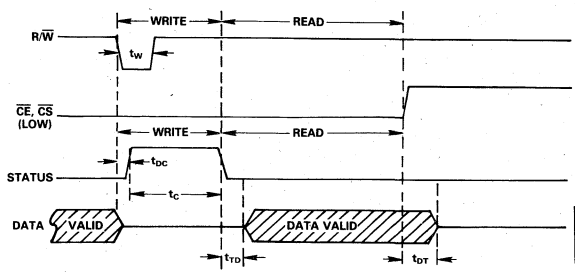


Figure 9. Stand-Alone Mode Single Conversion/ Single Read

Continuous Conversion, Single Read

A variety of applications may call for the A/D to be read after several conversions. In process control systems, this is often the case where a reading from a sensor may only need to be updated every few conversions. Figure 10 shows the timing relationships.

Once again, $\overline{CE}$ and $\overline{CS}$ should be tied together. Conversion will begin when the R/$\overline{W}$ signal is brought low. The device will convert repeatedly as indicated by the status line. A final conversion

AD670 TIMING SPECIFICATIONS

(Guaranteed Over the Full Operating Temperature Range, Unless Otherwise Noted)
Boldface indicates parameters tested 100% – See note on Specifications page.

Symbol	Parameter	Min	Typ	Max	Units
WRITE/CONVERT START MODE					
t_W	Write/Start Pulse Width	300			ns
t_{DS}	Input Data Setup Time	200			ns
t_{DH}	Input Data Hold	10			ns
t_{RWC}	Read/Write Setup Before Control	0			ns
t_{DC}	Delay to Convert Start			700	ns
t_C	**Conversion Time**			**10**	µs
READ MODE					
t_{SD}	Delay from Status Low to Data Read	0		250	ns
t_{TD}	**Bus Access Time**		200	**250**	ns
t_{DH}	Data Hold Time	25			ns
t_{DT}	**Output Float Delay**			**150**	ns

will take place once the R/$\overline{W}$ line has been brought high. The rising edge of R/$\overline{W}$ must occur while STATUS is high. R/$\overline{W}$ should not return high while STATUS is low since the circuit is in a reset state prior to the next conversion. Since the rising edge of R/$\overline{W}$ must occur while STATUS is high, R/$\overline{W}$'s length must be high per a minimum of 10.25μs ($t_C + t_{TD}$). Data becomes valid upon completion of the conversion and will remain so until the $\overline{CE}$ and $\overline{CS}$ lines are brought high indicating the end of the read cycle or R/$\overline{W}$ goes high initiating a new series of conversions.

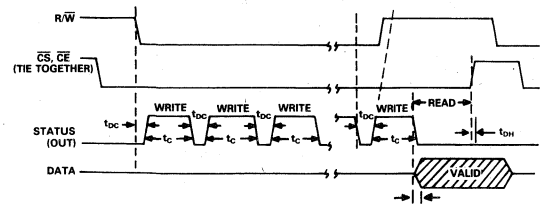


Figure 10. Stand-Alone Mode Continuous Conversion/ Single Read

APPLYING THE AD670

The AD670 has been designed for ease of use, system compatibility, and minimization of external components. Transducer interfaces generally require signal conditioning and preamplification before the signal can be converted. The AD670 will reduce and even eliminate this excess circuitry in many cases. To illustrate the flexibility and superior solution that the AD670 can bring to a transducer interface problem, the following discussions are offered.

Temperature Measurements

Temperature transducers are one of the most common sources of analog signals in data acquisition systems. These sensors require circuitry for excitation and preamplification/buffering. The instrumentation amplifier input of the AD670 eliminates the need for this signal conditioning. The output signals from temperature transducers are generally sufficiently slow that a sample/hold amplifier is not required. Figure 11 shows the AD590 IC temperature transducer interfaced to the AD670. The AD580 voltage reference is used to offset the input for 0°C calibration. The current output of the AD590 is converted into a voltage by R1. The high impedance unbuffered voltage is applied directly to the AD670 configured in the −128mV to 127mV bipolar range. The digital output will have a resolution of 1°C.

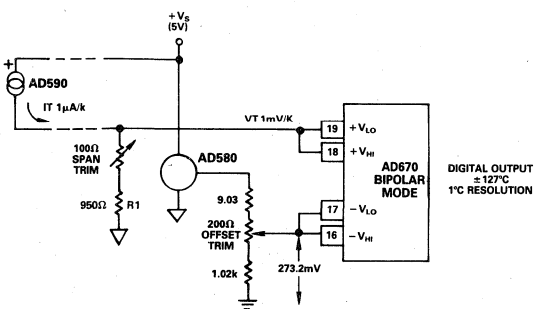


Figure 11. AD670 Temperature Transducer Interface

Platinum RTDs are also a popular, temperature transducer. Typical RTDs have a resistance of 100Ω at 0°C and change resistance of 0.4Ω per °C. If a constant excitation current is caused to flow in the RTD, the change in voltage drop will be a measure of the change in temperature. Figure 12 shows such a method and the required connections to the AD670. The AD580 2.5V reference provides the accurate voltage for the excitation current and range offsetting for the RTD. The op-amp is configured to force a constant 2.5mA current through the RTD. The differential inputs of the AD670 measure the difference between a fixed offset voltage and the temperature dependent output of the op-amp which varies with the resistance of the RTD. The RTD change of approximately 0.4Ω/°C results in a 1mV/°C voltage change. With the AD670 in the 1mV/LSB range, temperatures from 0 to 255°C can be measured.

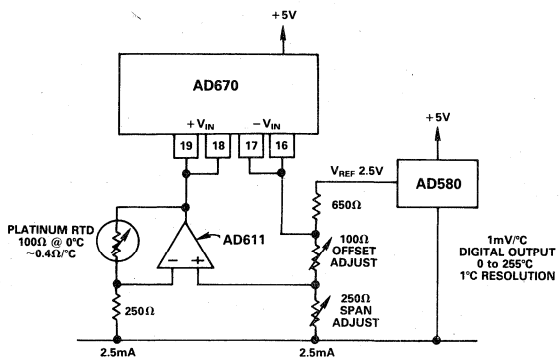


Figure 12. Low Cost RTD Interface

Differential temperature measurements can be made using an AD590 connected to each of the inputs as shown in Figure 13. These configurations will allow the user to measure the relative temperature difference between two points with a 1°C or 1/9°C resolution. Although the internal 1k and 9k resistors on the inputs have ±20% tolerance, trimming the AD590 is unnecessary as most differential temperature applications are concerned with the relative differences between the two.

However the user may see up to a 20% scale factor error in the differential temperature to digital output transfer curve.

This scale factor error correction can be accomplished through software correction. Offset corrections can be made by adjusting for any difference that results when both sensors are held at the same temperature. A span adjustment can then be made by immersing one AD590 in an ice bath and one in boiling water and eliminating any deviation from 100°C. For a low cost version of this setup, the plastic AD592 can be substituted for the AD590.

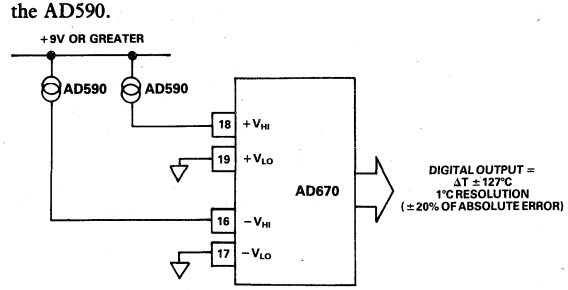


Figure 13a. Differential Temperature Measurement Using the AD590

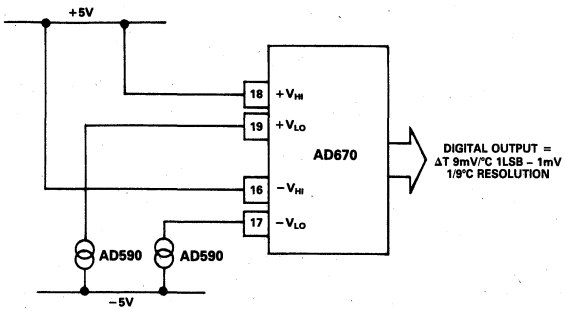


Figure 13b. Differential Temperature Measurement Using the AD590

STRAIN GAUGE MEASUREMENTS

Many semiconductor-type strain gauges, pressure transducers, and load cells may also be connected directly to the AD670. These types of transducers typically produce 30 millivolts full-scale per volt of excitation. In the circuit shown in Figure 14, the AD670 is connected directly to a Data Instruments model JP-20 load cell. The AD584 programmable voltage reference is used along with an AD741 op-amp to provide the ±2.5V excitation for the load cell. The output of the transducer will be ±150mV for a force of ±20 pounds. The AD670 is configured for the ±128 millivolt range. The resolution is then approximately 2.1 ounces per LSB over a range of ±17 pounds. Scaling to exactly 2 ounces per LSB can be accomplished by trimming the reference voltage which excites the load cell.

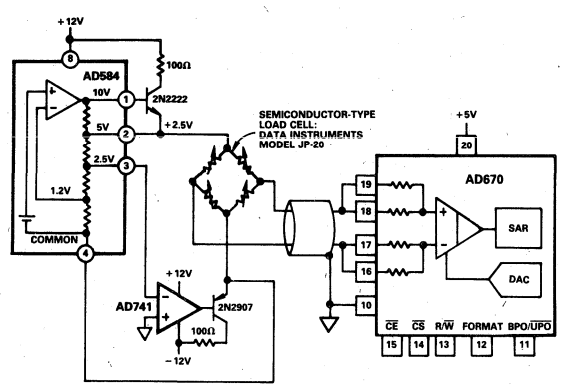


Figure 14. AD670 Load Cell Interface

INTERFACING THE AD670 TO MICROPROCESSOR DATA BUSES

The control logic of the AD670 allows it to be interfaced with many popular microcomputers and microprocessors with few or no additional components. For example Figure 15 shows how the AD670 can be interfaced to an APPLE II microcomputer.

The DEVICE SELECT signal available on the APPLE's peripheral connector can serve as the $\overline{CS}$ for the AD670. The $\overline{CE}$ line can be connected to the APPLE's phase 1 clock, and R/$\overline{W}$ can be connected directly to the APPLE's R/$\overline{W}$ line. The BPO/$\overline{UPO}$ and FORMAT controls can be latched into the AD670 from the data bus.

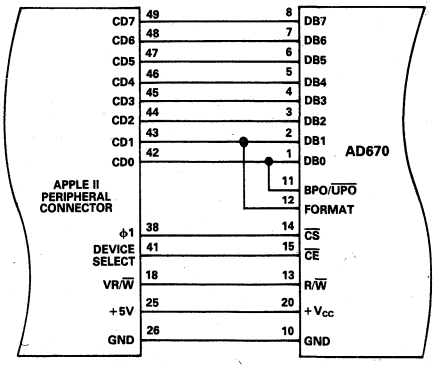


Figure 15. APPLE II Interface

The program shown in Figure 16 is used in interfacing the AD670 to the JP-20 load cell. The load cell output is ±150mV for ±20 pounds and a ±2.5V input to the AD670. This routine determines the weight of the object, averages 100 readings and provides an answer in pounds. The AD670 is interfaced to an APPLE II computer as in Figure 15.

```
1  PR# 1: PRINT  CHR$ (9);"52N": LIST : PR#
   0: END : REM  HARDCOPY OF LIST
2  REM   PROGRAM IN APPLESOFT TO INTER-
3  REM   FACE AD670 8-BIT ADC TO DATA
4  REM   INSTRUMENTS MODEL JP-20 LOAD
5  REM   CELL WHICH HAS +/-150 MV
6  REM   OUTPUT FOR +/-20 POUNDS AND
7  REM   +/-2.5 VOLT INPUT.
10  PRINT : PRINT : PRINT : PRINT
20  PRINT "TARE (T) OR WEIGH (W)? ";
30  INPUT A$
40  IF A$ <  > "T" THEN  GOTO 100
50  PRINT : PRINT "CLEAR SCALE NOW"
60  FOR I = 1 TO 1000: NEXT I
70 TARE = W
80  PRINT "TARE IS ";TARE;" POUNDS"
90  PRINT : PRINT : PRINT
95  GOTO 20
100  REM   ACTUAL WEIGHT ROUTINE
105  PRINT "PUT THE OBJECT ON THE SCALE."
110  GOSUB 670
120 NETWT = W - TARE
125  PRINT : PRINT : PRINT : PRINT
130  PRINT "NET WEIGHT IS ";NTWT;" POUNDS."
140  PRINT : PRINT : PRINT
150  GOTO 110
670  REM   THIS ROUTINE INTERFACES THE
671  REM   AD670 TO THE APPLE AND
672  REM   AVERAGES 100 READINGS, THEN
673  REM   CONVERTS THE ANSWER TO POUNDS.
675 W = 0
680  FOR I = 1 TO 100
681  POKE 49360,2 REM   THE '2' SETS THE
682  REM   AD670 FOR OFFSET
683  REM   BINARY OPERATION
684  REM  AND BIPOLAR INPUT
690 X =  PEEK (49360) REM  TO READ OUTPUT
691  REM  AFTER CONVERSION
695 X = X - 128
700 X = (X / 150) * 20
710 W = W + X
720  NEXT I
730 W =  INT ((W / 10) + 0.5)
740 W = W / 10
750  RETURN
1000  END
```

Figure 16. APPLE II Software for AD670 Interface

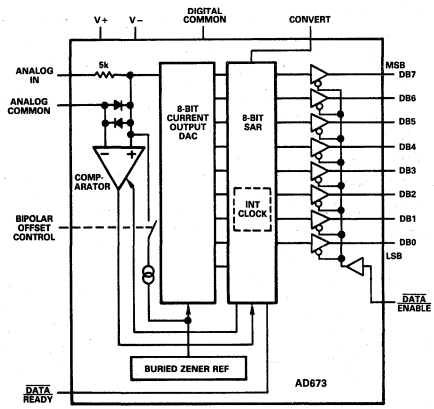
Fast, Complete, 8-Bit A/D Converter with Microprocessor Interface

AD673*

FEATURES

Complete 8-Bit A/D Converter with Reference, Clock and Comparator
Full 8- or 16-Bit Microprocessor Bus Interface
Fast Successive Approximation Conversion – 20μs
No Missing Codes Over Temperature
Operates on +5V and −12V to −15V Supplies
Low Cost Monolithic Construction

AD673 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD673 is a complete 8-bit successive approximation analog-to-digital converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register (SAR) and 3 state output buffers–all fabricated on a single chip. No external components are required to perform a full accuracy 8-bit conversion in 20μs.

The AD673 incorporates the most advanced integrated circuit design and processing technology available today. The successive approximation function is implemented with I^2L (integrated injection logic). Laser trimming of the high stability SiCr thin film resistor ladder network at the wafer stage (LWT) insures high accuracy, which is maintained with a temperature compensated sub-surface Zener reference.

Operating on supplies of +5V and −12V to −15V, the AD673 will accept analog inputs of 0 to +10V or −5V to +5V. The trailing edge of a positive pulse on the CONVERT line initiates the 20μs conversion cycle. $\overline{\text{DATA READY}}$ indicates completion of the conversion.

The AD673 is available in two versions. The AD673J as specified over the 0 to +70°C temperature range and the AD673S guarantees ±½LSB relative accuracy and no missing codes from −55°C to +125°C.

Two package configurations are offered. All versions are also offered in a 20-pin hermetically sealed ceramic DIP. The AD673J is also available in a 20-pin plastic DIP.

PRODUCT HIGHLIGHTS

1. The AD673 is a complete 8-bit A/D converter. No external components are required to perform a conversion.
2. The AD673 interfaces to many popular microprocessors without external buffers or peripheral interface adapters.
3. The device offers true 8-bit accuracy and exhibits no missing codes over its entire operating temperature range.
4. The AD673 adapts to either unipolar (0 to +10V) or bipolar (−5V to +5V) analog inputs by simply grounding or opening a single pin.
5. Performance is guaranteed with +5V and −12V or −15V supplies.

10

***Protected by U.S. Patent Nos. 3,940,760; 4,213,806; 4,136,349; 4,400,689; and 4,400,690**

SPECIFICATIONS (T_A = 25°C, V+ = +5V, V− = −12V or −15V, all voltages measured with respect to digital common, unless otherwise indicated)

Model	AD673J Min	AD673J Typ	AD673J Max	AD673S Min	AD673S Typ	AD673S Max	Units
RESOLUTION		8			8		Bits
RELATIVE ACCURACY,[1]			±1/2			±1/2	LSB
$T_A = T_{min}$ to T_{max}			±1/2			±1/2	LSB
FULL SCALE CALIBRATION[2]		±2			±2		LSB
UNIPOLAR OFFSET			±1/2			±1/2	LSB
BIPOLAR OFFSET			±1/2			±1/2	LSB
DIFFERENTIAL NONLINEARITY,[3]	8			8			Bits
$T_A = T_{min}$ to T_{max}	8			8			Bits
TEMPERATURE RANGE	0		+70	−55		+125	°C
TEMPERATURE COEFFICIENTS							
Unipolar Offset			±1			±1	LSB
Bipolar Offset			±1			±1	LSB
Full Scale Calibration[2]			±2			±2	LSB
POWER SUPPLY REJECTION							
Positive Supply							
+4.5≤V+≤+5.5V			±1			±2	LSB
Negative Supply							
−15.75V≤V−≤−14.25V			±1			±2	LSB
−12.6V≤V−≤−11.4V			±1			±2	LSB
ANALOG INPUT IMPEDANCE	3.0	5.0	7.0	3.0	5.0	7.0	kΩ
ANALOG INPUT RANGES							
Unipolar	0		+10	0		+10	V
Bipolar	−5		+5	−5		+5	V
OUTPUT CODING							
Unipolar	Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT							
Output Sink Current							
(V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2			3.2			mA
Output Source Current[4]							
(V_{OUT} = 2.4V max, T_{min} to T_{max})	0.5			0.5			mA
Output Leakage			±40			±40	μA
LOGIC INPUTS							
Input Current			±100			±100	μA
Logic "1"	2.0			2.0			V
Logic "0"			0.8			0.8	V
CONVERSION TIME, T_A and							
T_{min} to T_{max}	10	20	30	10	20	30	μs
POWER SUPPLY							
V+	+4.5	+5.0	+7.0	+4.5	+5.0	+7.0	V
V−	+11.4	−15	−16.5	−11.4	−15	−16.5	V
OPERATING CURRENT							
V+		15	25		15	25	mA
V−		9	15		9	15	mA
PACKAGE[5]							
Ceramic DIP		D20A			D20A		
Plastic DIP		N20A					

NOTES

[1]Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[2]Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor.
Full scale is defined as 10 volts minus 1LSB, or 9.961 volts.

[3]Defined as the resolution for which no missing codes will occur.

[4]The data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

[5]See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common	0 to +7V
V− to Digital Common	0 to −16.5V
Analog Common to Digital Common	±1V
Analog Input to Analog Common	±15V
Control Inputs	0 to V+
Digital Outputs (High Impedance State)	0 to V+
Power Dissipation	800mW

AD673 ORDERING GUIDE

Model	Package Option	Temperature Range	Relative Accuracy
AD673JN	20-Pin Plastic DIP	0 to +70°C	±1/2LSB max
AD673JD	20-Pin Ceramic DIP	0 to +70°C	±1/2LSB max
AD673SD	20-Pin Ceramic DIP	−55°C to +125°C	±1LSB max

FUNCTIONAL DESCRIPTION

A block diagram of the AD673 is shown in Figure 1. The positive CONVERT pulse must be at least 500ns wide. $\overline{DR}$ goes high within 1.5µs after the leading edge of the convert pulse indicating that the internal logic has been reset. The negative edge of the CONVERT pulse initiates the conversion. The internal 8-bit current output DAC is sequenced by the integrated injection logic (I^2L) successive approximation register (SAR) from its most significant bit to least significant bit to provide an output current which accurately balances the input signal current through the 5kΩ resistor. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is more, the bit is turned off. After testing all bits, the SAR contains a 8-bit binary code which accurately represents the input signal to within (0.05% of full scale).

The SAR drives $\overline{DR}$ low to indicate that the conversion is complete and that the data is available to the output buffers. $\overline{DATA\ ENABLE}$ can then be activated to enable the 8-bits of data desired. $\overline{DATA\ ENABLE}$ should be brought high prior to the next conversion to place the output buffers in the high impedance state.

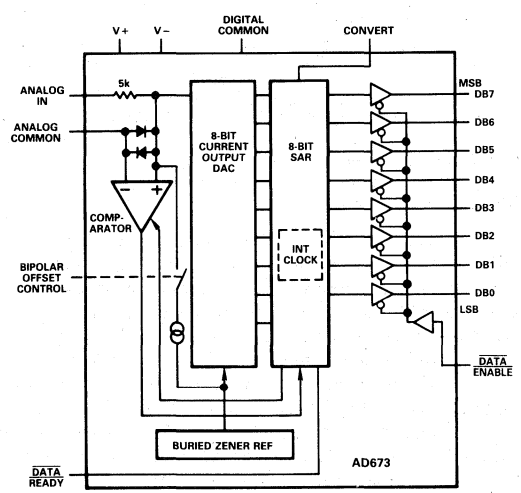


Figure 1. AD673 Functional Block Diagram

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and ensures excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less ½LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 to +10V unipolar input range becomes a −5V to +5V range. The 5kΩ thin film input resistor is trimmed so that with a full scale input signal, an input current will be generated which exactly matches the DAC output with all bits on.

UNIPOLAR CONNECTION

The AD673 contains all the active components required to perform a complete A/D conversion. Thus, for many applications, all that is necessary is connection of the power supplies (+5V and −12V to −15V), the analog input and the convert pulse. However, there are some features and special connections which should be considered for achieving optimum performance. The functional pin-out is shown in Figure 2.

The standard unipolar 0 to +10V range is obtained by shorting the bipolar offset control pin (pin 16) to digital common (pin 17).

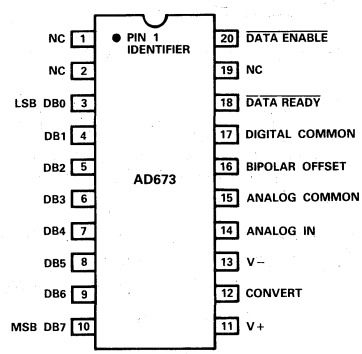


Figure 2. AD673 Pin Connections

Full Scale Calibration

The 5kΩ thin film input resistor is laser trimmed to produce a current which matches the full scale current of the internal DAC–plus about 0.3%–when an analog input voltage of 9.961 volts (10 volts – 1LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full scale input voltage can be trimmed down to match the DAC full scale current as precisely as desired. However, for many applications the nominal 9.961 volt full scale can be achieved to sufficient accuracy by simply inserting a 15Ω resistor in series with the analog input to pin 14. Typical full scale calibration error will then be within ±2LSB or ±0.8%. If more precise calibration is desired, a 50Ω trimmer should be used instead. Set the analog input at 9.961 volts, and set the trimmer so that the output code is just at the transition between 111111 10 and 11111111. Each LSB will then have a weight of 39.06mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a weight of exactly 40.0mV), a 100Ω resistor and a 100Ω trimmer (or a 200Ω trimmer with good resolution) should be used. Of course, larger full scale ranges can be arranged by using a larger input resistor, but linearity and full scale temperature coefficient may be compromised if the external resistor becomes a sizeable percentage of 5kΩ. Figure 3 illustrates the connections required for full scale calibration.

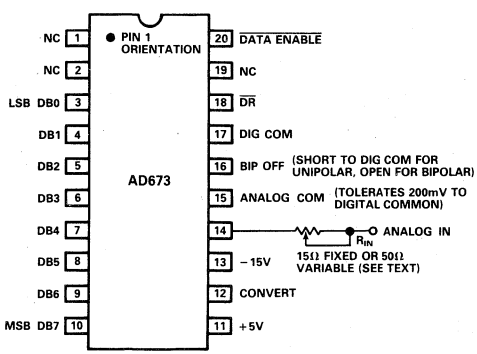


Figure 3. Standard AD673 Connections

Unipolar Offset Calibration

Since the Unipolar Offset is less than ±1/2LSB for all versions of the AD673, most applications will not require trimming. Figure 4 illustrates two trimming methods which can be used if greater accuracy is necessary.

Figure 4a shows how the converter zero may be offset to correct for initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode.

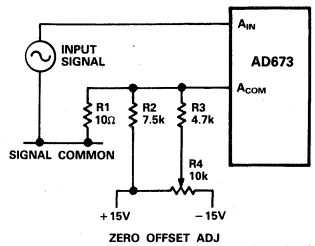


Figure 4a.

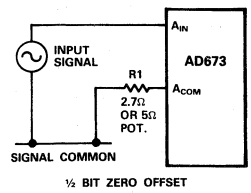


Figure 4b.

Figure 5 shows the nominal transfer curve near zero for an AD673 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics.

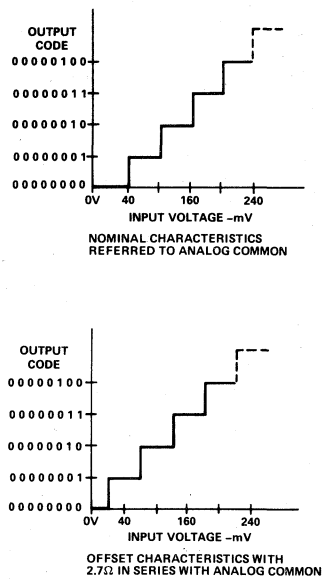


Figure 5. AD673 Transfer Curve – Unipolar Operation (Approximate Bit Wedights Shown for Illustration, Nominal Bit Weights ~ 39.06mV)

This offset can easily be accomplished as shown in Figure 4b. At balance (after a conversion) approximately 2mA flows into the Analog Common terminal. A 2.7Ω resistor in series with this terminal will result in approximately the desired ½ bit offset of the transfer characteristics. The nominal 2mA Analog Common current is not closely controlled in manufacture. If high accuracy is required, a 5Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full scale transition point will also move. Thus, if an offset of ½LSB is introduced, full scale trimming as described on the previous page should be done with an analog input of 9.941 volts.

NOTE: During a conversion, transient currents from the Analog Common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle appropriately during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion

errors. Power supply decoupling, which returns to analog signal common, should go to the signal input side of the resistive offset network.

BIPOLAR CONNECTION

To obtain the bipolar −5V to +5V range with an offset binary output code, the bipolar offset control pin is left open.

A −5.00 volt signal will give a 10-bit code of 00000000; an input of 0.00 volts results in an output code of 10000000 and +4.61 volts at the input yields the 11111111 code. The nominal transfer curve is shown in Figure 6.

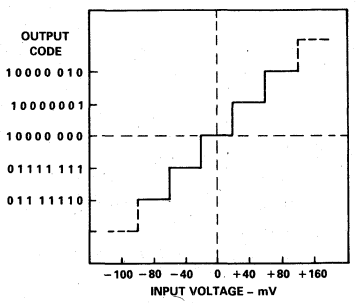


Figure 6. AD673 Transfer Curve–Bipolar Operation

Note that in the bipolar mode, the code transitions are offset ¼LSB such that an input voltage of 0 volts ±5mV yields the code representing zero (10000000). Each output code is then *centered* on its nominal input voltage.

Full Scale Calibration

Full Scale Calibration is accomplished in the same manner as in Unipolar operation except the full scale input voltage is +4.61 volts.

Negative Full Scale Calibration

The circuit in Figure 4a can also be used in Bipolar operation to offset the input voltage (nominally −5V) which results in the 000000 00 code. R2 should be omitted to obtain a symmetrical range.

The bipolar offset control input is not directly TTL compatible but a TTL interface for logic control can be constructed as shown in Figure 7.

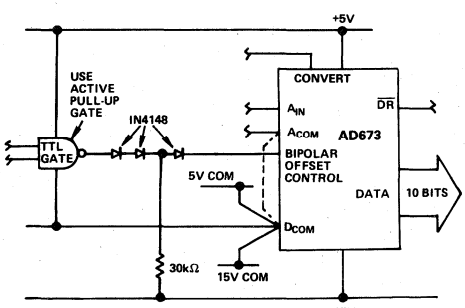


Figure 7. Bipolar Offset Controlled by Logic Gate
Gate Output = 1 Unipolar 0–10V Input Range
Gate Output = 0 Bipolar ±5V Input Range

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD673

Many situations in high-speed acquisition systems or digitizing rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD673, a SHA can also serve as a high input impedance buffer.

Figure 8 shows the AD673 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10μs with a droop rate less than 100μV/ms.

$\overline{DR}$ goes high after the conversion is initiated to indicate that reset of the SAR is complete. In Figure 8 it is also used to put the AD582 into the hold mode while the AD673 begins its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD673).

$\overline{DR}$ goes low when the conversion is complete placing the AD582 back in the sample mode. Configured as shown in Figure 8, the next conversion can be initiated after a 10μs delay to allow for signal acquisition by the AD582.

Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimize ground noise and interference during the conversion cycle.

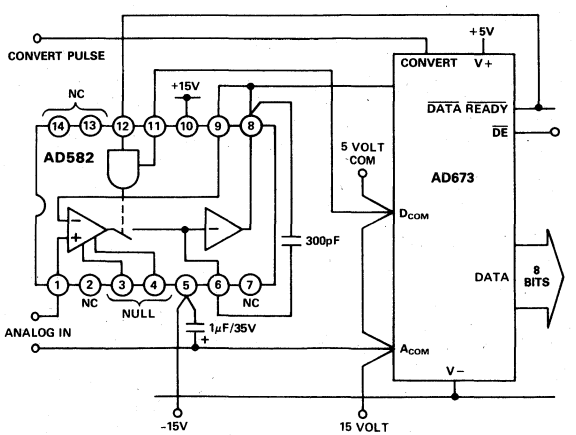


Figure 8. Sample-Hold Interface to the AD673

GROUNDING CONSIDERATIONS

The AD673 provides separate Analog and Digital Common connections. The circuit will operate properly with as much as ±200mV of common mode voltage between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation, the Analog Common terminal may generate transient currents of up to 2mA during a conversion. In addition a static current of about 2mA will flow into Analog Common in the unipolar mode after a conversion is complete. The Analog Common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. It is recommended that a parallel pair of back-to-back protection diodes be connected between the commons if they are not connected locally.

CONTROL AND TIMING OF THE AD673

The operation of the AD673 is controlled by two inputs: CONVERT and $\overline{\text{DATA ENABLE}}$.

Starting a Conversion

The conversion cycle is initiated by a positive-going CONVERT pulse at least 500ns wide. The rising edge of this pulse resets the internal logic, clears the result of the previous conversion, and sets $\overline{\text{DR}}$ high. The falling edge of CONVERT begins the conversion cycle. When conversion is completed $\overline{\text{DR}}$ returns low. During the conversion cycle, $\overline{\text{DE}}$ should be held high. If $\overline{\text{DE}}$ goes low during a conversion, the data output buffers will be enabled and intermediate conversion results will be present on the data output pins. This may cause bus conflicts if other devices in a system are trying to use the bus.

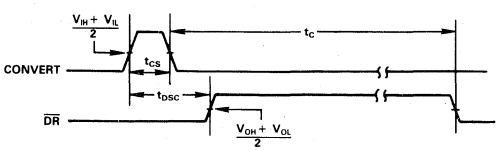


Figure 9. Convert Timing

Reading the Data

The three-state data output buffers is enabled by $\overline{\text{DE}}$. Access time of these buffers is typically 150ns (250 maximum). The Data outputs remain valid until 50ns after the enable signal returns high, and are completely into the high-impedance state 100ns later.

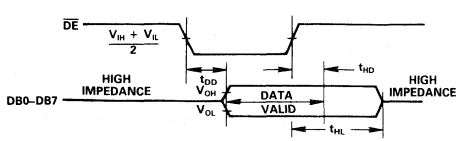


Figure 10. Read Timing

TIMING SPECIFICATIONS

Parameter	Symbol	Min	Typ	Max	Units
CONVERT Pulse Width	t_{CS}	500	–	–	ns
$\overline{\text{DR}}$ Delay from CONVERT	t_{DSC}	–	1	1.5	µs
Conversion Time	t_C	10	20	30	µs
Data Access Time	t_{DD}	0	150	250	ns
Data Valid after $\overline{\text{DE}}$ High	t_{HD}	50	–	–	ns
Output Float Delay	t_{HL}	–	100	200	ns

MICROPROCESSOR INTERFACE CONSIDERATIONS – GENERAL

When an analog-to-digital converter like the AD673 is interfaced to a microprocessor, several details of the interface must be considered. First, a signal to start the converter must be generated; then an appropriate delay period must be allowed to pass before valid conversion data may be read. In most applications, the AD673 can interface to a microprocessor system with little or no external logic.

The most popular control signal configuration consists of decoding the address assigned to the AD673, then gating this signal with the system's WR signal to generate the CONVERT pulse, and gating it with RD to enable the output buffers. The use of a memory address and memory WR and RD signals denotes "memory-mapped" I/O interfacing, while the use of a separate I/O address space denotes "isolated I/O" interfacing.

Figure 11 shows a generalized diagram of the control logic for an AD673 interfaced to an 8-bit data bus, where an address ADC ADDR has been decoded. ADC ADDR starts the converter when written to (the actual data being written to the converter does not matter) and contains the high byte data during read operations.

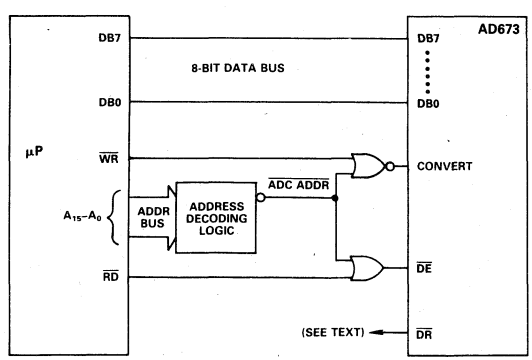


Figure 11. General AD673 Interface to 8-Bit Microprocessor

In systems where this read-write interface is used, at least 30 microseconds (the maximum conversion time) must be allowed to pass between starting a conversion and reading the results. This delay or "timeout" period can be implemented in a short software routine such as a countdown loop, enough dummy instructions to consume 30 microseconds, or enough actual useful instructions to consume the required time. In tightly-timed systems, the $\overline{DR}$ line may be read through an external three-state buffer to determine precisely when a conversion is complete. Higher-speed systems may choose to use $\overline{DR}$ to signal an interrupt to the processor at the end of a conversion.

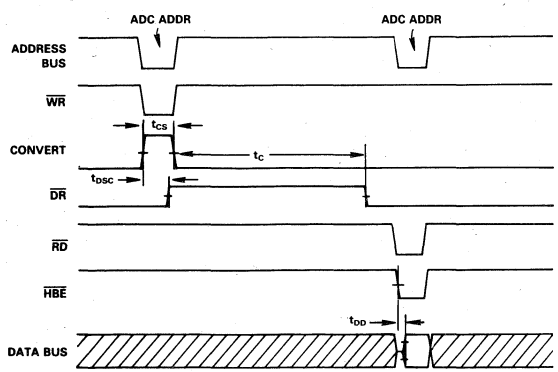


Figure 12. Typical AD673 Timing Diagram

CONVERT Pulse Generation

The AD673 is tested with a CONVERT pulse width of 500ns and will typically operate with a pulse as short as 300ns. However, some microprocessors produce active WR pulses which are shorter than this. Either of the circuits shown in Figure 13 can be used to generate an adequate CONVERT pulse for the AD673. In both circuits, the short low-going WR pulse sets the CONVERT line high through a flip-flop. The rising edge of $\overline{DR}$ (which signifies that the internal logic has been reset) resets the flip-flop and brings CONVERT low, which starts the conversion.

Note that t_{DSC} is slightly longer when the result of the previous conversion contains a logic 1 on the LSB. This means that the actual CONVERT pulse generated by the circuits in Figure 13 will vary slightly in width.

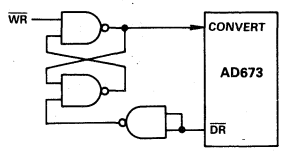


Figure 13a. Using 74LS00

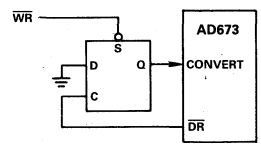


Figure 13b. Using 1/274LS74

10

50/100MHz, 6-Bit Monolithic ADC's

AD5010KD/AD6020KD

FEATURES

Scan Frequency to 100MHz (AD5010KD)
Low 450mW Power Dissipation
±1/4LSB Linearity
ECL Logic Compatible
No Sample & Hold Required
Overflow Output for Extended Resolution

APPLICATIONS

Video Data Conversion
High Speed Data Acquisition
Radar/Sonar Data Conversion

GENERAL DESCRIPTION

The AD6020KD is a 6-bit monolithic analog-to-digital converter capable of performing at conversion rates up to 50MHz. Packaged in a 16-pin hermetic ceramic dip, it performs true 6-bit A/D conversions with ±1/4LSB max linearity error. The extremely high scanning rate is ideal for video and other data acquisition applications that require digitizing of high frequency signals.

For other applications where even higher speed can be traded off against price, the AD5010KD represents the latest in state-of-the-art monolithic technology. Capable of performing true 6-bit conversions at rates up to 100MHz, the AD5010KD represents the ultimate in conversion speeds currently available in monolithic form. It is ideal for applications such as radar and X-ray equipment, medical systems such as ultra-sound, and measurement instruments such as digital storage oscilloscopes and transient recorders.

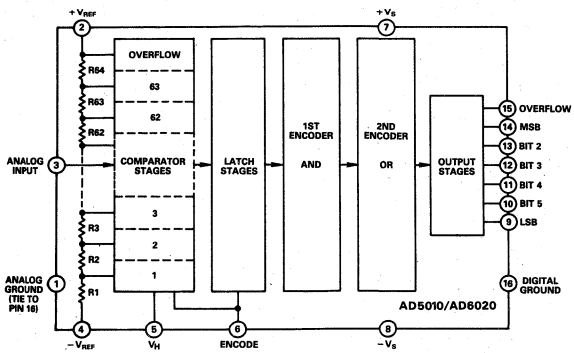
A unique feature of both units is the overflow output which allows the user to cascade two units to achieve 7-bit resolution, or four units for 8-bit resolution. Another salient feature is the power dissipation specification of only 450mW which is almost 50% less than the nearest competitive product.

THEORY OF OPERATION

The low linearity and ultra-high conversion rates are achieved by combining ECL logic and the parallel or "Flash" method of conversion. This consists of 64 comparator stages whose reference is set from an external voltage reference by a linear resistive voltage divider (see Block Diagram). The results of the comparator stage are then transferred to the 64 latches.

This comparison and transfer occurs when the encode input is at a "low" logic level. When the encode input goes "high", the latches are separated from the comparators and their contents encoded and brought to the output as a digital word. Since the latches are separated from the comparators during this cycle, the analog signal is always present at the input which eliminates the need for a track-and-hold.

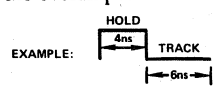
AD5010KD/AD6020KD FUNCTIONAL BLOCK DIAGRAM



TYPICAL CIRCUIT FOR 6-BIT OPERATION

The circuit of Figure 1 may be used for either the AD6020KD or AD5010KD. When the analog input equals or exceeds $+V_{REF}$, the overflow bit goes "high" and bits 1–6 go "low". If it is desirable to latch all bits high in this condition configure a 10197 (or equivalent) as shown to hold all bits including the overflow "high", as long as long as A_{IN} equals or exceeds $+V_{REF}$.

For applications at lower scan frequencies (below ≈ 50MHz), hysteresis control (V_H) may be left floating. At frequencies approaching 100MHz, the use of a nonsymmetrical encode pulse may enhance the overall performance.



Because of the high frequencies involved, attention to detail becomes most important (circuit layout, power supply decoupling, timing, etc.). A large ground plane is mandatory.

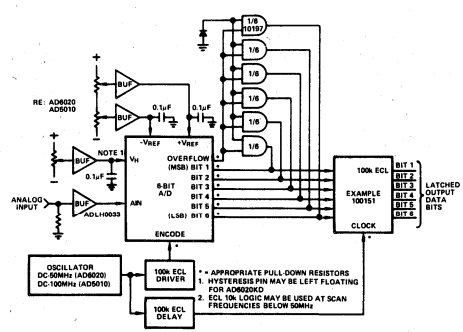


Figure 1. Typical Circuit – 6-Bit Operation

SPECIFICATIONS (typical at +25°C and nominal power supply unless otherwise noted)

PARAMETER	AD6020KD MIN	AD6020KD TYP	AD6020KD MAX	AD5010KD MIN	AD5010KD TYP	AD5010KD MAX	UNITS
RESOLUTION		6			*		Bits
INPUT RANGE			±2.5			*	V
LINEARITY ERROR[1]		1/4[2]			1/4[3]		LSB
INPUT CURRENT							
Hold	-10		+10	*		*	μA
Sample[4]		200	800		150	500	μA
INPUT CAPACITANCE[5]		35			*		pF
DYNAMIC							
Conversion Time		20			10		ns
Aperture Time (T_D)		2			*		ns
Aperture Jitter (Uncertainty)		25			*		ps
T_{ENCODE}	15	8		10	5		ns
Scan Frequency		50			100		MHz
Signal Transition Time							
T_{HLQ}		12	20		8	15	ns
T_{LHQ}		12	20		8	15	ns
Recovery Time (1V Step)		5			*		ns
DATA INPUTS							
Logic Compatibility		ECL			*		
Encode							
Logic Level "1"	-1.1	-0.9	-0.6	*	*	*	V
Logic Level "0"	-2.0	-1.7	-1.5	*	*	*	V
Encode Current "1"	5	30	100	*	*	*	μA
Encode Current "0"	5	30	100	*	*	*	μA
REFERENCE INPUTS							
Positive Reference Voltage	-2.0		+2.5	*		*	V
Negative Reference Voltage	-2.5		+2.0	*		*	V
Reference Resistance	96	128	256	*	*	195	Ω
DATA OUTPUTS[6]							
Logic Compatibility		ECL			*		
Logic Level "1"	-1.1	-0.9	-0.7	*	*	*	V
Logic Level "0"	-2.0	-1.7	-1.5	*	*	*	V
POWER SUPPLY REQUIREMENTS							
$+V_S$	4.75	5.0	5.25	*	*	*	V
$-V_S$	-5.46	-5.2	-4.94	*	*	*	V
CURRENT[7]							
$+V_S$ = +5.0V		30	60		*	*	mA
$-V_S$ = -5.2V		55	80		*	*	mA
POWER DISSIPATION		450			*		mW
TEMPERATURE RANGE (Ambient)	0		70	*		*	°C

NOTES
[1] Measured with 2V, 1kHz triangular input.
[2] 15ns T_{ENCODE}.
[3] 10ns T_{ENCODE}.
[4] Measured with AIN = $+V_{REF}$ in sample mode.
[5] Measured with AIN > $-V_{REF}$.
[6] Data Outputs terminated to -2V through 100Ω.
[7] $-V_{REF} \leq AIN \leq +V_{REF}$.
*Specifications same as AD6020.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter		Lower Limit	Upper Limit	Unit
Supply Voltage	$+V_S$	-0.3	+6.0	Volts
	$-V_S$	-6.0	+0.3	Volts
Input Voltages				
AIN $+V_{REF}$ $-V_{REF}$		-3.0	+3.0	Volts
Encode		$-V_S$	0.0	Volts
Hysterisis Control		>0	+3.0	Volts
Temperature				
Operating		0	+70	°C
Storage		-55	+125	°C
Lead, Soldering (10sec)			+300	°C

EVALUATION BOARD

An evaluation board is available. The AD6020KD/PCB contains everything needed to verify the performance of the ADC. The effects of changes in the analog input, $+V_{REF}$, $-V_{REF}$, hysteresis, and encode can be monitored by an on-board DAC. Each card is shipped with the ADC and a complete instruction set. The only user requirement is to supply power to the board: +5 ±2% @ 100mA; -5.2 ±2% @ 2000mA; ±15 ±1% @ 100mA each.

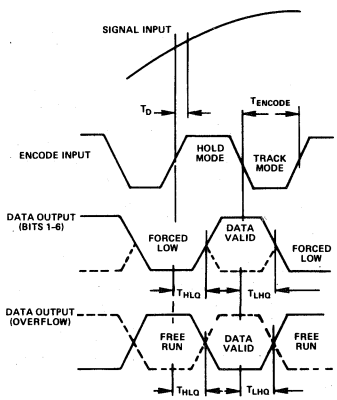
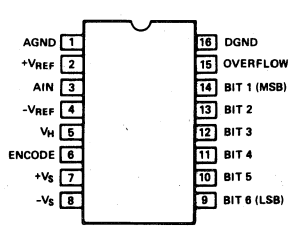


Figure 3. Timing Diagram

ORDERING INFORMATION

Model	Description	Package Option[1]
AD6020KD	6 Bits, 50MHz	D16B
AD6020KD/PCB	AD6020KD ADC with Evaluation Board	D16B
AD5010KD	6 Bits, 100MHz	D16B

[1] See Section 19 for package outline information.



PIN	SYMBOL	FUNCTION
1	GND	GROUND (ANALOG)
2	$+V_{REF}$	POSITIVE VOLTAGE REFERENCE
3	AIN	ANALOG INPUT
4	$-V_{REF}$	NEGATIVE VOLTAGE REFERENCE
5	V_H	HYSTERESIS CONTROL
6	ENCODE	ENCODE INPUT
7	$+V_S$	POSITIVE SUPPLY VOLTAGE
8	$-V_S$	NEGATIVE SUPPLY VOLTAGE
9	BIT 6	LEAST SIGNIFICANT BIT OUTPUT
10	BIT 5	BIT 5 OUTPUT
11	BIT 4	BIT 4 OUTPUT
12	BIT 3	BIT 3 OUTPUT
13	BIT 2	BIT 2 OUTPUT
14	BIT 1	MOST SIGNIFICANT BIT OUTPUT
15	OVERFLOW	OVERFLOW OUTPUT
16	GND	GROUND (DIGITAL)

NOTE: GND PINS (1, 16) SHOULD BE TIED TOGETHER AS CLOSE TO THE UNIT AS POSSIBLE.

Figure 2. Outline & Pin Designations

ANALOG DEVICES

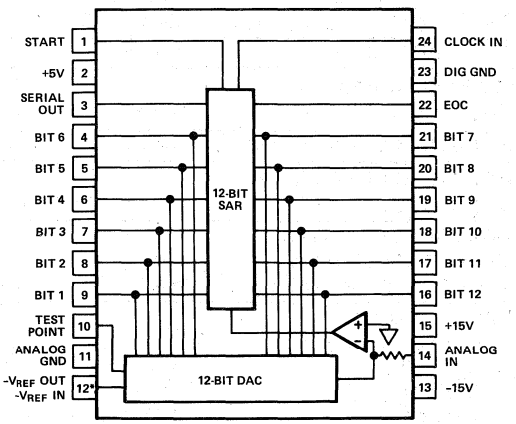
12-Bit Successive Approximation High Accuracy A/D Converter

AD5200/AD5210 SERIES

FEATURES

- True 12-Bit Operation: ±1/2LSB max Nonlinearity
- Totally Adjustment-Free
- Guaranteed No Missing Codes Over the Specified Temperature Range
- Hermetically-Sealed Package
- Standard Temperature Range: -25°C to +85°C
- Extended Temperature Range: -55°C to +125°C
- Serial and Parallel Outputs
- Monolithic DAC with Scaling Resistors for Stability
- Low Chip Count for High Reliability
- Industry Standard Pin Out
- Small 24-Pin DIP

AD5200/AD5210 FUNCTIONAL BLOCK DIAGRAM



*PIN 12 FUNCTION: -VREF OUT – AD52X1, AD52X2
-VREF IN – AD52X4, AD52X5

GENERAL DESCRIPTION

The AD52XX series devices are 12-bit successive approximation analog-to-digital converters. The hybrid design utilizes MSI digital, linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide a totally adjustment free converter—no potentiometers are required for calibration.

The innovative design of the AD52XX series devices incorporates a monolithic 12-bit feedback DAC for reduced chip count and higher reliability. The exceptional temperature coefficients of the monolithic DAC guarantees ±1/2LSB linearity over the entire operating temperature range of -25°C to +85°C for the BD grade and -55°C to +125°C for the TD grade.

The AD52XX series converters are available in 2 input voltage ranges: ±5V (AD521X1/AD52X4) and ±10V (AD52X2/AD52X5). The converters are available either complete with an internal buried zener reference or with the option of an external reference for improved absolute accuracy.

The AD52XX series converters are available in two performance grades; the "B" is specified from -25°C to +85° and the "T" is specified from -55°C to +125°C. All units are available in a 24-pin hermetically sealed ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD52XX series devices are laser trimmed at the factory to provide a totally adjustment free converter—no potentiometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The AD52XX series directly replaces other devices of this type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5210 series makes it an excellent choice for applications requiring high system throughput rates.

10

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

INPUT RANGE[1]	INPUT IMPEDANCE				
-5V to +5V -10V to +10V	5.0kΩ 10.0kΩ	AD52X1B AD52X2B	AD52X1T AD52X2T	AD52X4B AD52X5B	AD52X4T AD52X5T
REFERENCE		Internal	*	External -10.000V	***
RESOLUTION		12 Bits	*	*	*
LINEARITY ERROR, MAX		±1/2LSB	*	*	*
No Missing Codes T_{min} to T_{max}		Guaranteed	*	*	*
ZERO ERROR, MAX		±1LSB	*	*	*
ZERO ERROR, MAX T_{min} to T_{max}		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX		±2LSB	*	*	*
ABSOLUTE ACCURACY, MAX T_{min} to T_{max}		±0.4% of FSR[2]	*	±0.1% of FSR[2]	***
CONVERSION TIME, MAX					
Clock = 1MHz (5210 Series)		13μs	*	*	*
Clock = 260kHz (5200 Series)		50μs	*	*	*
LOGIC RATINGS					
Input Logic Commands					
Logic "0"		0.8V max	*	*	*
Logic "1"		+2.0V min	*	*	*
Loading		0.5TTL Load	*	*	*
CLOCK INPUT PULSE WIDTH		100ns min	*	*	*
OUTPUT LOGIC					
Logic "0"		0.4V max	*	*	*
Logic "1"		3.6V (2.4 min)	*	*	*
FANOUT - HIGH		8TTL Loads	*	*	*
FANOUT - LOW		2TTL Loads	*	*	*
POWER SUPPLY REQUIREMENTS					
V_{LOGIC}		+5V ±10%	*	*	*
V_{CC}		+15V ±10%	*	*	*
V_{DD}		-15V ±10%	*	*	*
OPERATING CURRENT					
V_{LOGIC}		25mA (42mA max)	*	*	*
V_{CC}		10mA (16mA max)	*	*	*
V_{DD}		20mA (28mA max)	*	*	*
V_{REF}				0.5mA	***
POWER SUPPLY REJECTION					
V_{CC}		±0.005%/% (±0.02%/% max)	*	*	*
V_{DD}		±0.005%/% (±0.02%/% max)	*	*	*
POWER CONSUMPTION		575mW (870mW max)	*	575mW (875mW max)	***
OPERATING TEMPERATURE RANGE		-25°C to +85°C	-55°C to +125°C	*	**

NOTES
*Same specifications as AD52X1/X2B.
**Same specifications as AD52X1/X2T.
***Same specifications as AD52X4/X5B.
[1] Other input ranges are available, consult factory.
[2] FSR is Full Scale Range and is equal to the peak to peak input signal.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Positive Supply	+18V
Negative Supply	−18V
Logic Supply	−0.5V to +7V
Analog Input	±25V
Digital Outputs	Logic Supply
Digital Inputs	+5.5V
Reference Supply	−15V

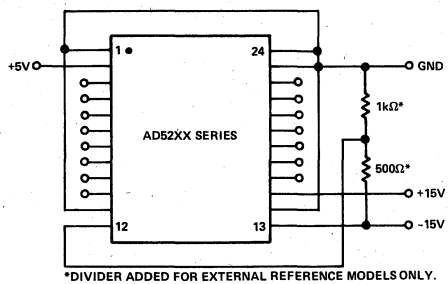


Figure 1. Burn In Circuit

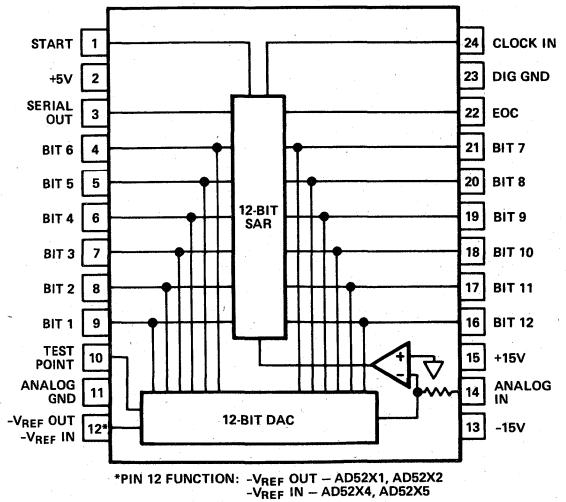


Figure 2. Pin Designations

10

AD52XX SERIES ORDERING GUIDE

Model	Linearity	Absolute Accuracy	Temperature Range	Conversion Time
AD521*BD	1/2LSB	2LSB	−25°C to +85°C	13μs
AD521*TD	1/2LSB	2LSB	−55°C to +125°C	13μs
AD520*BD	1/2LSB	2LSB	−25°C to +85°C	50μs
AD520*TD	1/2LSB	2LSB	−55°C to +125°C	50μs

*Insert number according to desired input voltage range as shown in Table II.
Package is HY24C or HY24D at the option of Analog Devices, Inc.
See Section 19 for package outline information.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD52XX converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 3. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high. At time t_0, B_1 is reset and B_2–B_{12} are set unconditionally. At t_1 the Bit 1 decision is made and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. The STATUS flag is reset at time t_{12} indicating that the conversion is complete and that the parallel output data is valid.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 3). An external clock of 1MHz (AD5210) will yield 13μs conversion time. An external clock of 260kHz (AD5200) will yield 50μs conversion time.

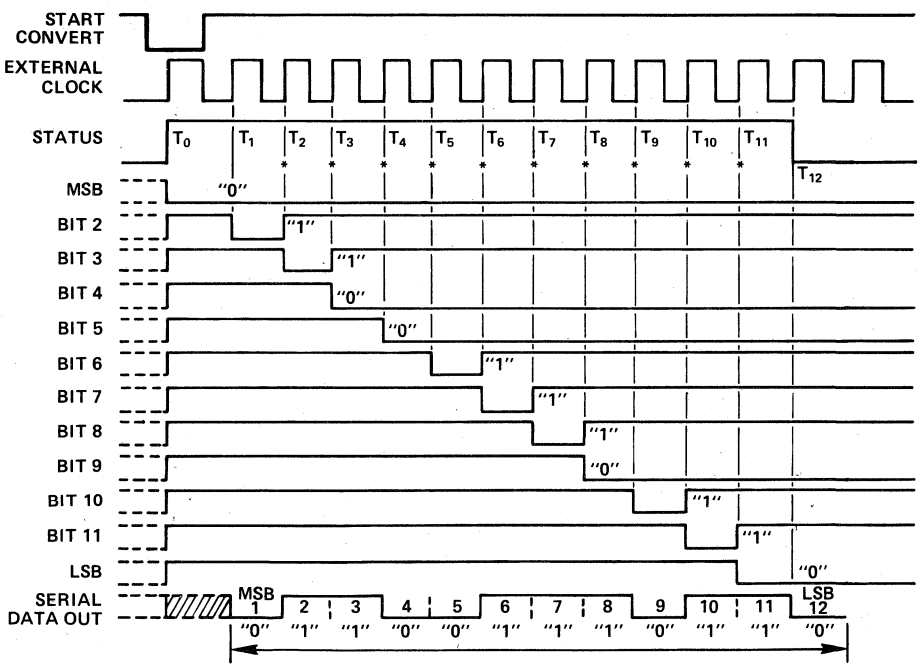


Figure 3. Timing Diagram

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors have been internally trimmed to provide an absolute accuracy of ±0.05%. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD52XX is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

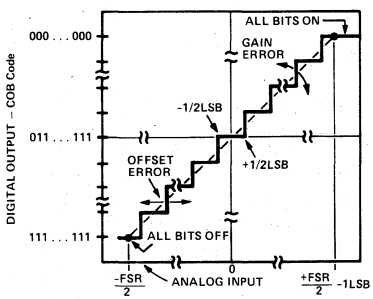


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Digital Ground and Analog Ground (Analog Power Return). These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD52XX. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

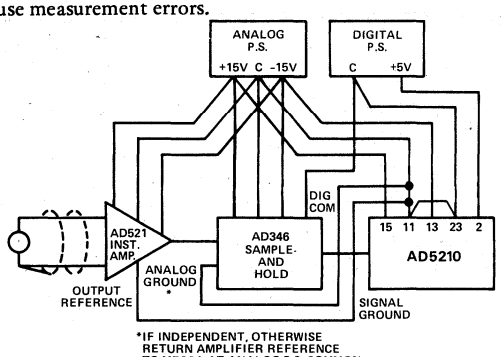


Figure 5. Basic Grounding Practice

Each of the AD52XX's supply terminals should be capacitively decoupled as close to the AD52XX as possible. A large value capacitor such as 1μF in parallel with 0.01μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Ground pin and the logic supply is bypassed to the Digital Ground pin.

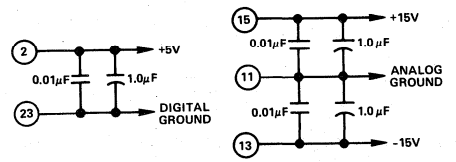


Figure 6. Power Supply Decoupling

SAMPLED DATA SYSTEMS

The conversion speed of the AD52XX allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD52XX capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 7 and 8 show the use of an AD346 and ADSHC-85 as sample and holds in combination with the AD52XX.

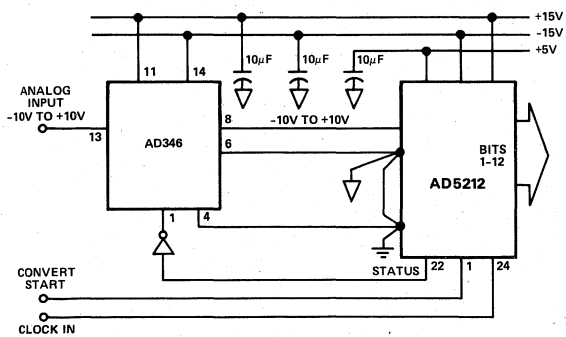


Figure 7. 66.6kHz–12 Bit, A/D Conversion System

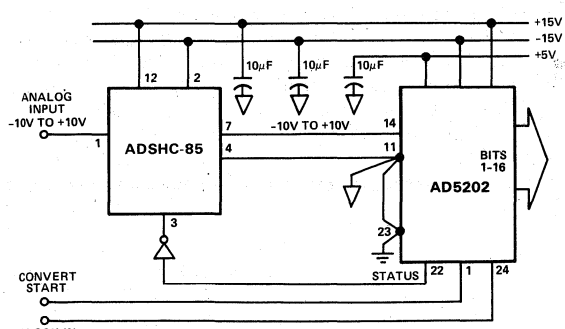


Figure 8. 18.3kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy and corresponding resolution of the converter.

The resolution of an AD5210 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)(\text{Aperture Uncertainty})}$$

$$F_{MAX}/AD346 = \frac{1}{(2\pi)\,(4096)\,(4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/ADSHC\text{-}85 = \frac{1}{(2\pi)\,(4096)\,(5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 9.

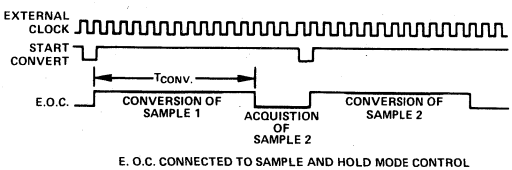


Figure 9. START/E.O.C. Timing for Sampled Data System

When using an AD346 with an AD5212 the throughput rate is, 2.0μs acquisition time plus 13μs conversion time, 66.6kHz. The ADSHC-85 used in combination with an AD5202 is, 4.5μs acquisition time plus 50μs conversion time, 18.3kHz. To meet the requirements of the Nyquist sampling criteria, the AD346 and AD5210 combination can be used for input frequencies from dc through 33.3kHz; the ADSHC-85 and AD5210 combination for inputs from dc through 9.2kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

A fast (32kHz) 12-bit DAS can be configured using the AD362 and the AD521X. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

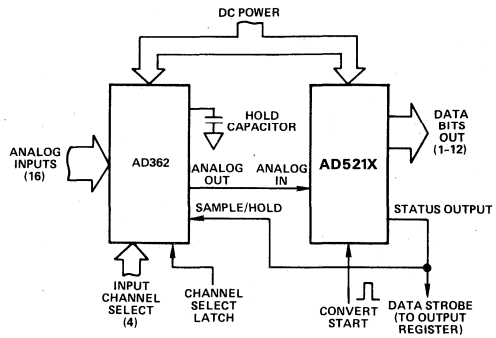


Figure 10. High Speed 12-Bit DAS

CONVERT START USING A POSITIVE EDGE

In some systems it may be inconvenient to generate a negative going start convert pulse of the proper width. The circuit of Figure 11 can be used to start a conversion on the AD521X series of A/Ds with a positive going edge. To perform a conversion both the convert start signal and the E.O.C. must be low. The output of the inverter and nand gate will then be in the high state. The converter will reset on the next rising clock edge. Resetting brings the E.O.C. to a high state; the inverter goes low; the convert start is still high so the output of the nand gate goes high allowing the conversion to continue immediately. The convert start line has only to be brought back down before the conversion is complete.

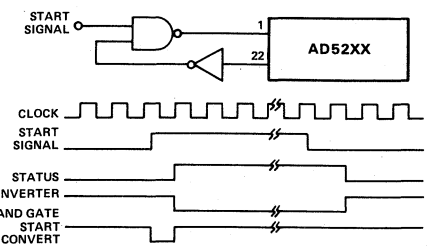


Figure 11. Convert Start Using a Positive Edge

Input Range	Speed	Internal Reference	External Reference
-5V to +5V	50μs	AD5201	AD5204
	13μs	AD5211	AD5214
-10V to +10V	50μs	AD5202	AD5205
	13μs	AD5212	AD5215

i.e., — the 13μs conversion time, ±10V input, external reference, extended temperature unit is the AD5215TD.

Table II.

ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD5240

FEATURES

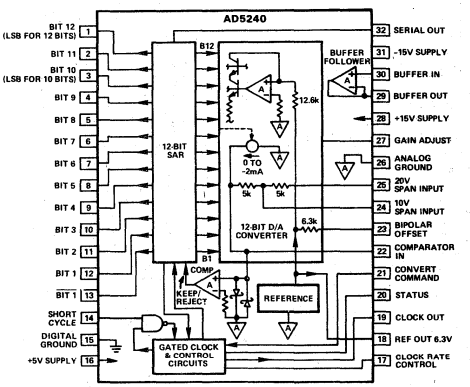
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 5μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
- Max Nonlinearity: <±0.012%
- Low Power: 775mW Typical
- Hermetic Package Available
- Low Chip Count – High Reliability
- Pin Compatible with AD ADC84/AD ADC85
- "Z" Models for ±12V Operation Available
- Extended Temperature Range -25°C to +85°C

Versatility

- Negative-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +6.3V Reference for External Applications

AD5240 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD5240 is a high speed low cost 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD5240 include a maximum linearity error at +25°C of 0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 775mW, and conversion time of less than 5μs for 12-bit conversions. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C (K grade) and -25°C to +85°C (B grade).

The design of the AD5240 includes scaling resistors that provide analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V, or 0 to +10V. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD5240K is specified for operation over the 0 to +70°C temperature range and the AD5240B is specified for the -25°C to +85°C range.

PRODUCT HIGHLIGHTS

1. The AD5240 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The AD5240 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rate of the AD5240 makes it an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and 10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and high reliability.

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SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD5240KD	AD5240BD
RESOLUTION	12 Bits	12 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	•
Unipolar	0V to +5V, 0V to +10V	•
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ(±20%)	•
0V to +10V, ±5V	5kΩ(±20%)	•
±10V	10kΩ(±20%)	•
Buffer Amplifier[1]		
Impedance (min)	100MΩ	•
Bias Current	50nA	•
Offset Voltage	6mV	
Settling Time		
To 0.01% for 20V Step	2μs	•
DIGITAL INPUTS[2]		
Convert Command	Positive Pulse 50ns min Trailing Edge Initiates Conversion	•
Logic Loading	1TTL Load	•
TRANSFER CHARACTERISTICS		
Gain Error[3]	±0.2%	•
Offset Error[3]	Adjustable to Zero	•
Unipolar	±0.1% of FSR[4]	•
Bipolar[5]	±0.2% of FSR[4]	•
Linearity Error (max)[6] T_{min} to T_{max}	±0.012% FSR	•
Inherent Quantization Error	±0.012% FSR	•
Differential Linearity Error	±1/2LSB	•
No Missing Codes Temperature Range	0 to +70°C	-25°C to +85°C
Power Supply Sensitivity		
±15V	±0.004% of FSR/% V	•
+5V	±0.001% of FSR/% V	•
DRIFT		
Specification Temperature Range	0 to +70°C	-25°C to +85°C
Gain (max)	±30ppm/°C	±25ppm/°C
Offset		
Unipolar	±3ppm/°C	•
Bipolar (max)[5]	±15ppm/°C	±7ppm/°C
Linearity (max)	±2ppm/°C	•
Monotonicity	GUARANTEED	•
CONVERSION SPEED (MAX)	5μs	•
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[7]		
Unipolar	CSB	•
Bipolar	COB, CTC	•
Output Drive	2TTL Loads	•
Serial Data Codes (NRZ)	CSB, COB	•
Output Drive	2TTL Loads	•
Status	Logic "1" during Conversion	•
Status Output Drive	2TTL Loads	•
Internal Clock		
Clock Output Drive	2TTL Loads	•
Frequency[8]	2.6MHz	•
INTERNAL REFERENCE VOLTAGE	6.3V/±15mV max	•
Max. External Current (with no degradation of specifications)	1.0mA	•
Tempco of Reference	±10ppm/°C	•
POWER REQUIREMENTS		
Rated Voltages	+5V, ±15V	•
Range for Rated Accuracy	4.75V to 5.25V and ±13.5V to ±16.5V	•
Z Models[9]	4.75V to 5.25V and ±11.4V to ±16.5V	•
Supply Drain +15V	15mA max	•
-15V	35mA max	•
+5V	100mA max	•
Total Power Dissipation	1100mW max	•
TEMPERATURE RANGE		
Specification	0 to +70°C	-25°C to +85°C
Operating (Derated Specs)	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	•
PACKAGE	Hermetic Ceramic	Hermetic Ceramic

NOTES
[1] Buffer Settling time adds to conversion speed when buffer is connected to input.
[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital input, Logic "0" = 0.4V max, Logic "1" = 2.4V min, digital output.
[3] Adjustable to zero.
[4] FSR means Full Scale Range.
[5] Guaranteed at V_{IN} = 0 volts.
[6] Error shown is the same as ±1/2LSB max error in % of FSR.
[7] See Table I.
[8] Pin 17 tied to +5V.
[9] For ±12V operaton add "Z" to model number. Input range limited to a maximum of ±5V when input buffer is used.
• Specifications same as AD5240KD.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Power Requirements	Temperature Range	Package[1]
AD5240KD	±15V	0 to +70°C	HY32F
AD5240ZKD	±12V	0 to +70°C	HY32F
AD5240BD	±15V	-25°C to +85°C	HY32F
AD5240ZBD	±12V	-25°C to +85°C	HT32F

[1] See Section 19 for package outline information.

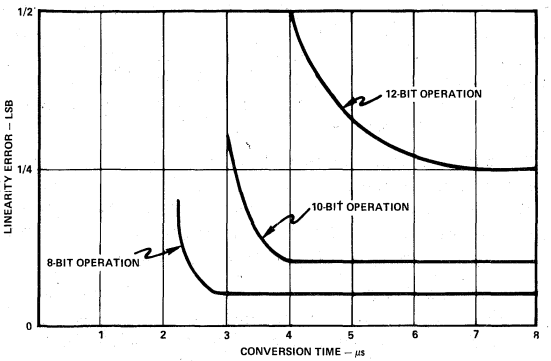


Figure 1. Linearity Error vs. Conversion Speed

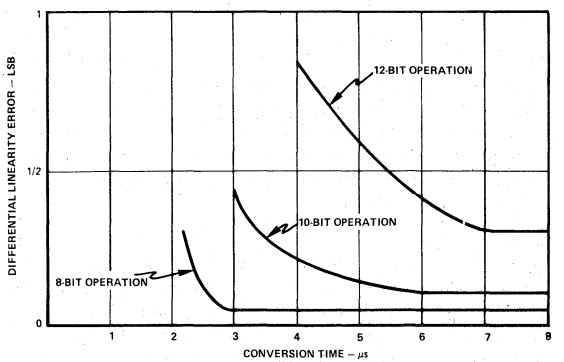


Figure 2. Differential Linearity Error vs. Conversion Speed

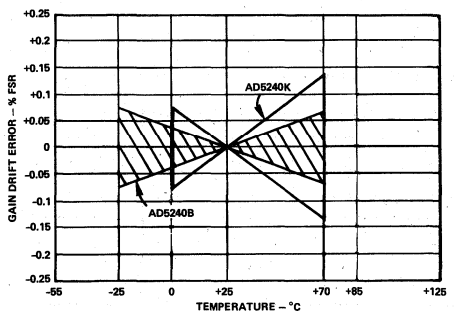


Figure 3. Gain Drift Error (% FSR) vs. Temperature

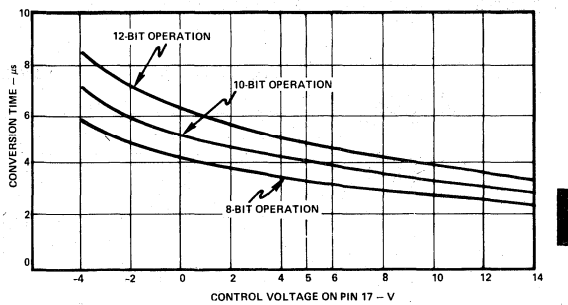


Figure 4. Conversion Speed vs. Control Voltage

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.2% FSR for gain and ±0.1% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 10 and 12. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD5240 is specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

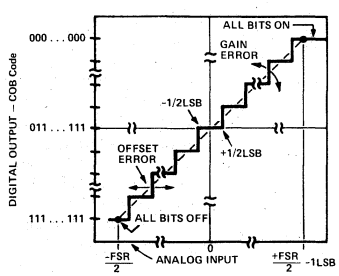


Figure 5. Transfer Characteristics for an Ideal Bipolar A/D

THEORY OF OPERATION

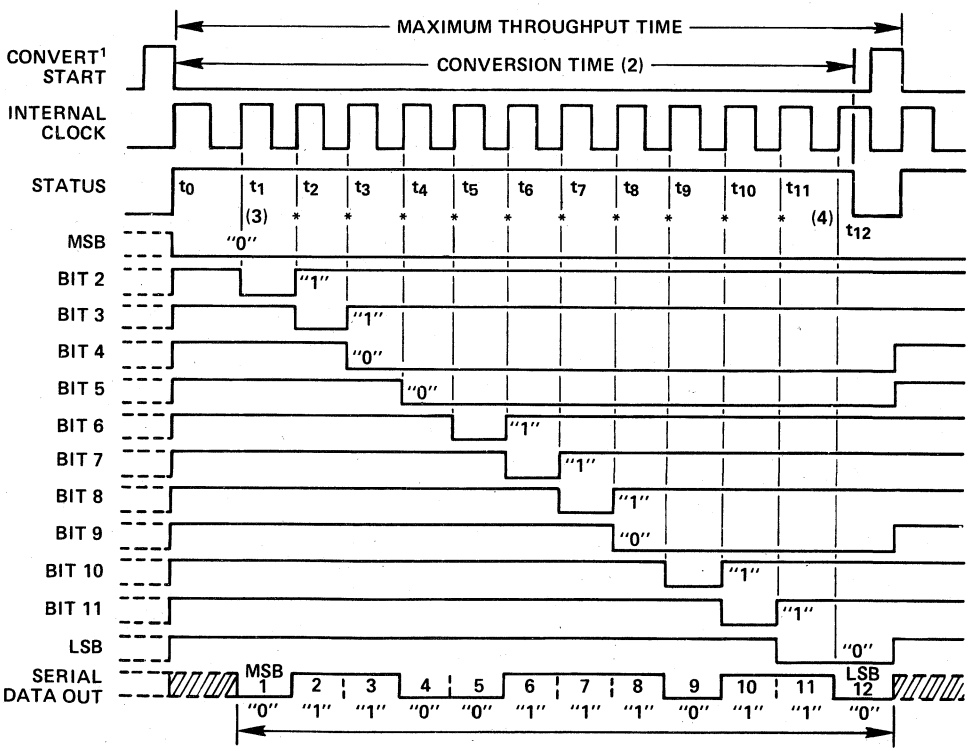
On receipt of a CONVERT START command, the AD5240 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simple by clocking it into a receiving shift register on these edges (see Figure 6).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 5μs FOR 12 BITS AND 4.2μs FOR 10 BITS (MAX – PIN 17 TIED TO +5V)
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 6. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 6. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 6. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 6). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in the table below.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	16	12	0.024	5.0	t_{12} +40ns
2	16	10	0.100	4.1	t_{10} +40ns
4	16	8	0.390	3.3	t_8 +40ns

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiometer with a TCR of ±100ppm/°C or less as shown in Figures 7 and 8.

If the potentiometer is connected to −15V, conversion time can be increased as shown in Figure 6. If these adjustments are used, delete the connections shown in the previous table for pin 17. See Figure 1 for linearity error vs. conversion speed and Figure 4 for the effect of the control voltage on clock speed.

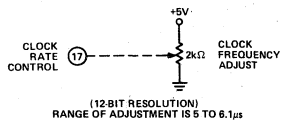


Figure 7. 12-Bit Clock Rate Control Optional Fine Adjust

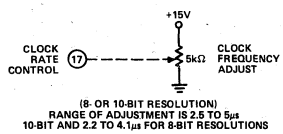


Figure 8. 8-Bit Clock Rate Control Optional Fine Adjust

INPUT SCALING

The AD5240 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

10

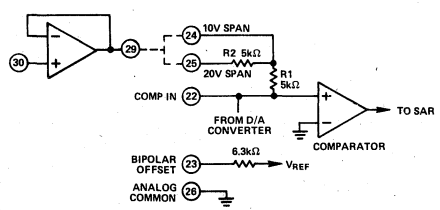


Figure 9. AD5240 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. Input Scaling Connections

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	−Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES:
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table I. Input Voltage Range and LSB Values

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 10 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a −1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

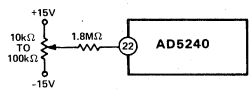


Figure 10. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 11.

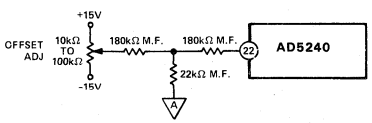


Figure 11. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 12.

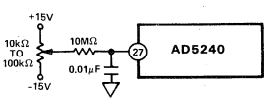


Figure 12. Gain Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 13.

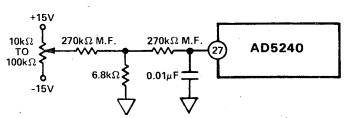


Figure 13. Low Tempco Gain Adjustment Circuit

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 10 and 12, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

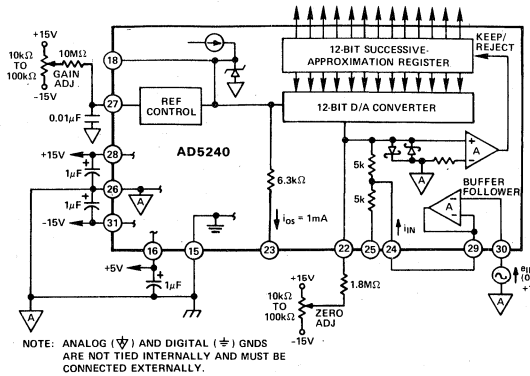


Figure 14. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

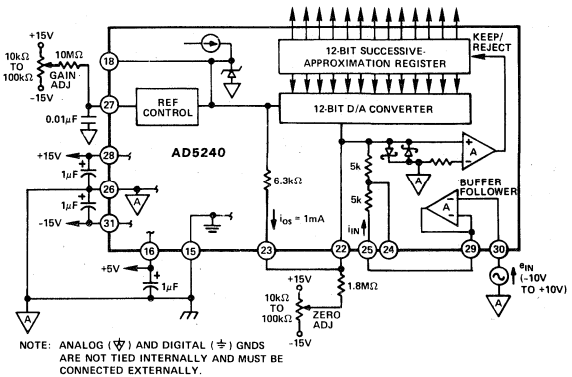


Figure 15. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR −2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

−10V to +10V Range: Set analog input to −9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD5240. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD5240's supply terminals should be capacitively decoupled as close to the AD5240 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

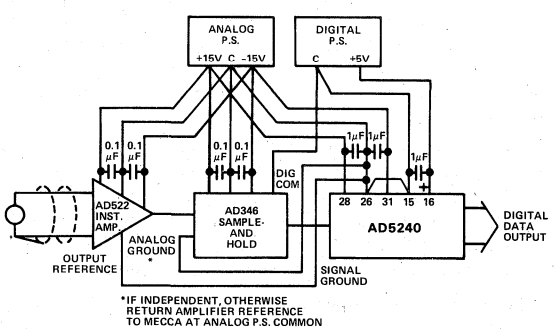


Figure 16. Basic Grounding Practice

SAMPLED DATA SYSTEMS

The conversion speed of the AD5240 allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD5240 capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or ADSHC-85 is required. Figures 16 and 17 show the use of an AD346 and ADSHC-85 as sample and hold's in combination with the AD5240.

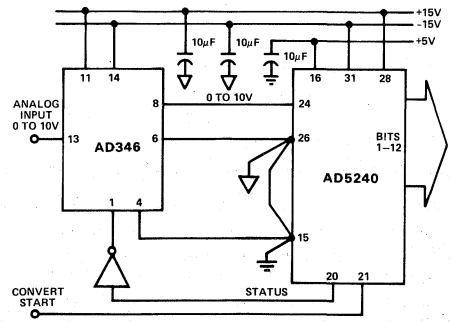


Figure 17. 142.8kHz–12-Bit, A/D Conversion System

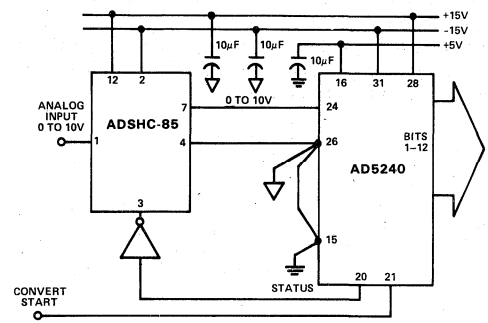


Figure 18. 105kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.

B. The desired accuracy, and corresponding resolution of the converter.

The resolution of an AD5240 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

$$F_{MAX}/ = \frac{2^{-N}}{(2\pi)\,(\text{Aperture Uncertainty})}$$

$$F_{MAX}/\text{AD346} = \frac{1}{(2\pi)\,(4096)\,(4 \times 10^{-10})} = 97.1\text{kHz}$$

$$F_{MAX}/\text{ADSHC-85} = \frac{1}{(2\pi)\,(4096)(5 \times 10^{-10})} = 77.7\text{kHz}$$

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 19.

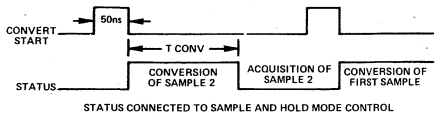


Figure 19. Start/Status Timing for Sampled Data System

When using an AD346 with an AD5240 the throughput rate is, 2.0μs acquisition time plus 5μs conversion time, 142.8kHz. The ADSHC-85 used in combination with an AD5240 is, 4.5μs acquisition time plus 5μs conversion time, 105.3kHz. To meet the requirements of the nyquist sampling criteria, the AD346 and AD5240 combination can be used for input frequencies from dc through 71kHz; the ADSHC-85 and AD5240 combination for inputs from dc through 52kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

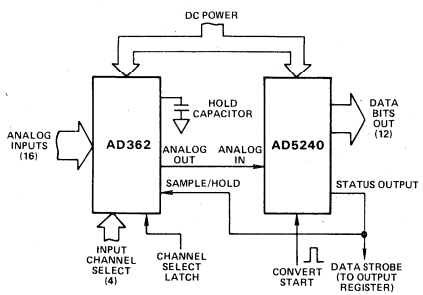


Figure 20. High Speed 12-Bit DAS

A fast (43.5kHz) 12-bit DAS can be configured using the AD362 and the AD5240. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hardwire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

MICROPROCESSOR INTERFACING

The 5μs conversion time of the AD5240 suggests several differential methods of interface to microprocessors. In systems where the AD5240 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is use-

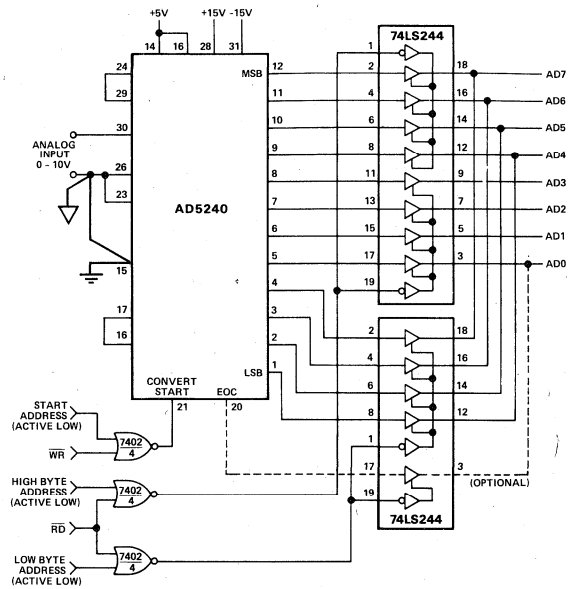


Figure 21. AD5240 Interface Connections

ful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 21 shows a typical connection to an 8085-type bus, using a left justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD5240 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{\text{MSB}}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

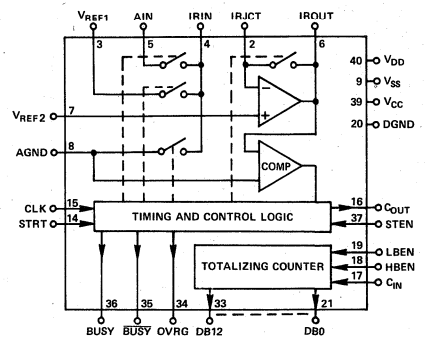
ANALOG DEVICES

CMOS 13-Bit Monolithic A/D Converter

AD7550

FEATURES
- **Resolution: 13 Bits, 2's Complement**
- **Relative Accuracy: ±1/2 LSB**
- **"Quad Slope" Precision**
  - **Gain Drift: 1ppm/°C**
  - **Offset Drift: 1ppm/°C**
- **Microprocessor Compatible**
- **Ratiometric**
- **Overrange Flag**
- **Very Low Power Dissipation**
- **TTL/CMOS Compatible**
- **CMOS Monolithic Construction**

AD7550 FUNCTIONAL BLOCK DIAGRAM



40-PIN DIP

GENERAL DESCRIPTION

The AD7550 is a 13-bit (2's complement) monolithic CMOS analog-to-digital converter on a 118 x 125 mil die packaged in a 40-pin ceramic DIP. Outstanding accuracy and stability (1ppm/°C) is obtained due to its revolutionary integrating technique, called "Quad Slope" (Analog Devices patent No. 3872466). This conversion consists of four slopes of integration as opposed to the traditional dual slope and provides much higher precision.

The AD7550 parallel output data lines have three-state logic and are microprocessor compatible through the use of two enable lines which control the lower eight LSB's (low byte enable) and the five MBS's (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

The AD7550 conversion time is about 40ms with a 1MHz clock. Clock can be externally controlled or internally generated by simply connecting a capacitor to the clock pin. A positive start pulse can be self-generated by having a capacitor on the start pin or can be externally applied.

PACKAGE IDENTIFICATION[1]

Suffix "D" – Ceramic DIP (D40A)

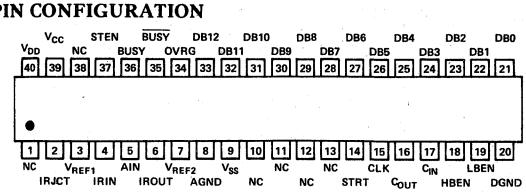
NOTE
[1] See Section 19 for package outline information.

For most applications, the AD7550 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

A wide range of power supply voltages (±5V to ±12V) with minuscule current requirements make the AD7550 ideal for low power and/or battery operated applications. Selection of the logic (V_{CC}) supply voltage (+5V to V_{DD}) provides direct TTL or CMOS interface on the digital input/output lines.

The AD7550 uses a high density CMOS process featuring double layer metal and silicon nitride passivation to ensure high reliability and long-term stability.

PIN CONFIGURATION



TOP VIEW

SPECIFICATIONS (V_{DD} = +12V, V_{SS} = -5V, V_{CC} = +5V, V_{REF1} = +4.25V unless otherwise noted)[1]

PARAMETER	TA = +25°C	OVER SPECIFIED TEMPERATURE RANGE	TEST CONDITIONS
ACCURACY			
Resolution		13 Bits 2's Comp min	
Relative Accuracy	±1LSB max	±1 LSB max	f_{CLK} = 500kHz, R_1 = 1MΩ,
Gain Error	±1LSB max		C_1 = 0.01μF, IRJCT Voltage
Gain Error Drift	1ppm/°C typ		Adjusted to $\frac{V_{REF1}}{2}$ ±0.6%
Offset Error	±0.5LSB max		
Offset Error Drift	1ppm/°C typ		
ANALOG INPUTS			
AIN Input Resistance[2]	R1MΩ min		
V_{REF1} Input Resistance[2]	R1MΩ min		
V_{REF2} Leakage Current	10pA typ		
DIGITAL INPUTS			
CIN, LBEN, HBEN, STEN			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+2.4V min	+2.4V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}, I_{INH}	5nA typ		
START			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V to V_{DD}
V_{INH}	+3.0V min	+3.0V min	
I_{INL}	-1μA typ		V_{CC} = +5V to V_{DD}, BUSY = Low
I_{INH}	+150μA typ		V_{CC} = +5V to V_{DD}, BUSY = High
CLOCK			
V_{INL}	+0.8V max	+0.8V max	V_{CC} = +5V
V_{INH}	+3V min	+3V min	
V_{INL}	+1.2V max	+1.2V max	V_{CC} = +12V
V_{INH}	+10.8V min	+10.8V min	
I_{INL}	-100μA typ		V_{IN} = V_{INL}; V_{CC} = +5V to +12V
I_{INH}	+100μA typ		V_{IN} = V_{INH}; V_{CC} = +5V to +12V
DIGITAL OUTPUTS			
V_{OUTL}	+0.5V max	+0.8V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OUTH}	+2.4V min	+2.4V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OUTL}	+1.2V max	+1.2V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OUTH}	+10.8V min	+10.8V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance (Floating State)	5pF typ		
(OVRG, BUSY, $\overline{BUSY}$, and DB0-DB12			
I_{LKG} (Floating State) (OVRG, $\overline{BUSY}$, BUSY, and DB0–DB12)	±5nA typ		V_{CC} = +5V to +12V V_{OUT} = 0V and V_{CC}
DYNAMIC PERFORMANCE			
Conversion Time	90ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 500kHz
	40ms typ		$V_{IN(CLK)}$ = 0 to +3V, f_{CLK} = 1MHz
STEN, HBEN, LBEN Propagation Delay t_{ON}, t_{OFF}	250ns typ, 500ns max		V_{IN}(STEN, HBEN, LBEN) 0 to +3V
External STRT Pulse Duration	800ns min		$V_{IN(STRT)}$ = 0 to +3V
POWER SUPPLIES			
V_{DD} Range	+10V min, +12V max		
V_{SS} Range	-5V min, -12V max		
V_{CC} Range	+5V min, V_{DD} max		
I_{DD}	0.6mA typ, 2mA max		
I_{SS}	0.3mA typ, 2mA max		f_{CLK} = 1MHz
I_{CC}	0.06mA typ, 2mA max		

NOTES

[1] Full Scale Voltage = ±V_{REF1} ÷ 2.125. For V_{REF1} = +4.25V, FS voltage is ±2.000V.

[2] The equivalent input circuit is the integrator resistor R_1 (1MΩ min, 10MΩ max) in series with a voltage source $\frac{V_{REF1}}{2}$, (see Figure 1).

Specifications subject to change without notice.

ORDERING INFORMATION

Model	Temperature Range	Package
AD7550BD	−25°C to +85°C	Ceramic

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.
2. V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND . . . . . 0V, +14V
V_{DD} to DGND . . . . . 0V, +14V
V_{SS} to AGND . . . . . 0V, −14V
V_{SS} to DGND . . . . . 0V, −14V
AGND to DGND . . . . . 0V, +14V
V_{CC} to DGND . . . . . 0V, V_{DD}
V_{REF1} . . . . . V_{SS}, V_{DD}
V_{REF2} . . . . . AGND, V_{DD}
AIN . . . . . V_{SS}, V_{DD}
IRIN . . . . . V_{SS}, V_{DD}
IRJCT . . . . . AGND, V_{DD}
IROUT . . . . . V_{SS}, V_{DD}
Digital Input Voltage
HBEN, LBEN, STEN, C_{IN} . . . . . DGND, (DGND +27V)
CLK, START . . . . . DGND, V_{DD}
Digital Output Voltage
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT} . . . DGND, V_{CC}
Power Dissipation (Package)
Up to +50°C 1000mW
Derates above +50°C by . . . . . 10mW/°C
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature . . . . . −25°C to +85°C

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input
4	IRIN	IntegratoR INput. External integrator input R is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Fullscale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C_1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (-5V to -12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1," the AD7550's digital logic is set up and BUSY is latched "high." When STRT returns "low," conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 800 nanoseconds to ensure proper set-up of the AD7550 logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $N = \left[\frac{AIN}{V_{REF1}} \; 2.125 + 1\right] \; 4096$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8-DB12 data outputs. When HBEN is low, the DB8—DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0—DB7. When LBEN is "low," DB0—DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRange indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2 LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

PRINCIPLES OF OPERATION

BASIC OPERATION

The essence of the quad slope technique is best explained through Figures 1 and 2.

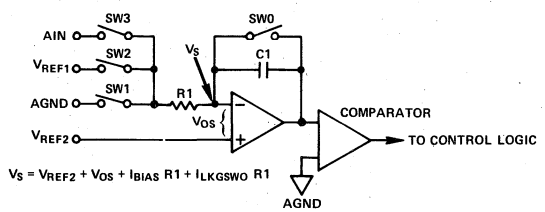


Figure 1. Quad Slope Integrator Circuit

The inputs AGND (analog ground), V_{REF1} and AIN (analog input) are applied in sequence to an integrator (Figure 1), creating four slopes (phases 1 through 4, Figure 2) at the integrator output. Voltage V_S is ideally equal to $\frac{V_{REF1}}{2}$, but if not, will create an error count "n" that will be minimized by the "quad-slope" conversion process. V_{REF1} and V_{REF2} must be positive voltages.

The equivalent integrator input voltages and their integration times are shown in Table I.

TABLE I.
INTEGRATOR EQUIVALENT INPUT VOLTAGES AND INTEGRATION TIMES

Phase	Input Voltage	Integration Time
1	AGND−V_S	$t_1 = K_1 t$
2	V_{REF1}−V_S	$t_2 = (K_1 + n)t$
3	AIN−V_S	$t_3 = (2K_1 - n)t$
4	V_{REF1}−V_S	$t_4 = (K_3 - 2K_1 + n - 2N)t$

NOTE: Ideally $V_S = V_{REF2} = 1/2\ V_{REF1}$

where:
t = The CLK period
n = System error count
K_1 = A fixed count equal to 4352 counts
K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
K_3 = A fixed count equal to 25600 counts
N = Digital output count corresponding to the analog input voltage, AIN

PHASE 0
After the start pulse is applied, switch SW2 is closed (all other switches open) and the integrator output is ramped to comparator zero crossing. Phase 0 can be considered the reset phase of the converter, and always has a duration $t_0 = R_1C_1$ (integrator time constant). Upon zero crossing, counters K_1 and K_2 are started, switch SW2 is opened and SW1 is closed.

PHASE 1
Phase 1 integrates (AGND − V_S) for a fixed period of time (by counter K_1) equal to $t_1 = K_1 t$. At the end of phase 1, switch SW1 is opened and SW2 is closed.

PHASE 2
The integrator input is switched to (V_{REF1} − V_S) and the output ramps down until zero crossing is achieved. The integration time $t_2 = (K_1 + n)t$ includes the error count "n" due to offsets, etc. At the end of phase 2, switch SW2 is opened, SW3 is closed, and a third counter (K_3) is started.

PHASE 3
Phase 3 integrates the analog input (AIN − V_S) until counter K_2 counts $4K_1 t$. At this time SW3 is opened and SW2 is closed again.

PHASE 4
Phase 4 integrates (V_{REF1} − V_S) and the comparator output ramps down until zero crossing once again is achieved. Since the comparator always approaches zero crossing from the same slope, propagation delay is constant and hysteresis effect is eliminated.

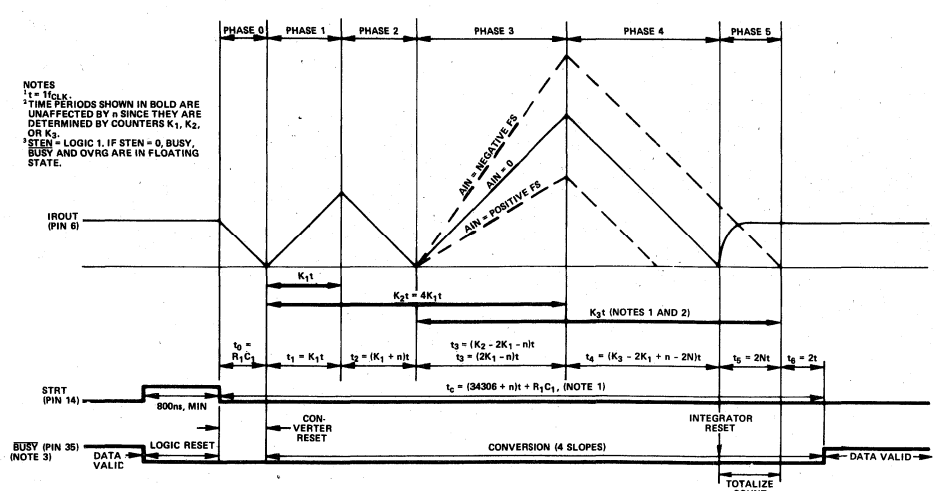


Figure 2. Quad Slope Timing Diagram

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal transfer function}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right) \cdot \left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right] \cdot 2K_1}_{\text{error term}}$$

where:

$$\alpha = \frac{2V_S - V_{REF1}}{V_{REF1}}$$

The ideal case assumes:

AGND = 0V

$V_S = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{V_{FS}} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

V_{FS} = full scale input voltage = $\frac{V_{REF1}}{2.125}$

The parallel output (DB0–DB12) of the AD7550 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

TABLE II
OUTPUT CODING (Bipolar 2's Complement)

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)			
		OVRG	DB12		DB0
+Overrange	–	1	0	1111 1111 1111	
+VFS ($1-2^{-12}$)	8191	0	0	1111 1111 1111	
+VFS (2^{-12})	4097	0	0	0000 0000 0001	
0	4096	0	0	0000 0000 0000	
-VFS (2^{-12})	4095	0	1	1111 1111 1111	
-VFS	0	0	1	0000 0000 0000	
-Overrange	–	1	1	0000 0000 0000	

Notes
1 $V_{FS} = \frac{V_{REF1}}{2.125}$
2 N = number of counts at C_{OUT} pin
3 C_{OUT} strapped to C_{IN}; LBEN, HBEN and STEN = Logic 1

ERROR ANALYSIS

Equation 1 shows that only α and AGND generate error terms. Their impact can be analyzed as follows:

Case 1: AGND = 0, $\alpha \neq 0$

Error sources such as capacitor-leakage (I_L) and op amp offset (e) cause α to be different from zero.

Under this condition,

$$\alpha = \frac{2(e + I_L R_1)}{V_{REF1}}$$

where $I_L R_1$ is the equivalent error voltage generated by leakage I_L.

The evaluation of this error term is best demonstrated through the following example:

Assume:

e = 5mV, I_L = 5nA, R_1 = 1MΩ and V_{REF1} = 4.25V.

Then:

$\alpha = 4.7 \times 10^{-3}$

and:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \times 8704 + 12800 - \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \times 22.1 \times 10^{-6} \times 8704}_{\text{error term } N_\epsilon}$$

Therefore, the error count N_ϵ is as follows:

For AIN = $-V_{FS}$: N_ϵ = 0.28 counts = 0.28LSB
AIN = 0: N_ϵ = 0.19 counts = 0.19LSB
AIN = $+V_{FS}$: N_ϵ = 0.09 counts = 0.09LSB

The above example shows the strong reduction of the circuit errors because of the α^2 term in (EQN 1). Another consequence of this effect is that N_ϵ is always positive, regardless of the polarity of the circuit errors.

Case 2: AGND $\neq 0$, $\alpha = 0$

When AGND is different from the signal ground, then this error will come through on a first-order basis. Indeed:

$$N = \left[\frac{AIN}{V_{REF1}} - 1\right] \cdot 8704 + 12800 + \underbrace{\left[\frac{AIN}{V_{REF1}} - 1\right] \cdot \frac{AGND}{V_{REF1}}}_{\text{error term } N_\epsilon}$$

The following example demonstrates the impact of AGND.

Let AGND = 1mV and V_{REF1} = 4.25V.

For AIN = $-V_{FS}$, then N_ϵ = 3.01 counts
AIN = 0, then N_ϵ = 2.05 counts
AIN = + V_{FS}, then N_ϵ = 1.08 counts

Therefore, ground loops should be minimized because a 330μV difference between AGND and signal ground will cause 1 count (1 LSB) of error when the analog input is at minus full scale. An optimized ground system is shown in Figure 7.

OPERATING GUIDELINES

The following steps, in conjunction with Figure 3, explain the calculations of the component values required for proper operation.

1. DETERMINATION OF V_{REF1}

When the full scale voltage requirement (VFS) has been ascertained, the reference voltage can be calculated by:

$V_{REF1} = 2.125\ (V_{FS})$

V_{REF1} must be positive for proper operation.

2. SELECTION OF C_3 (INTERNAL CLOCK OPERATION)

For internal clock operation, connect capacitor C_3 to the clock pin as shown in Figure 3. The clock frequency versus capacitor C_3 is shown in Figure 4.

The clock frequency must be limited to 1.3MHz for proper operation.

3. SELECTION OF INTEGRATOR COMPONENTS (R_1 AND C_1)

To ensure that the integrator's output doesn't saturate to its bound (V_{DD}) during the phase (3) integration cycle, the integrator time constant (R_1C_1) should be approximately equal to:

$$\tau = R_1C_1 = \frac{V_{REF1}\ (9 \times 10^3)}{f_{CLK}\ (V_{DD} - 4V)}$$

The integrator components R_1 and C_1 can be selected by referring to Figure 5 and/or Figure 6. Figure 5 plots the time constant (R_1C_1) versus clock frequency for different reference voltages. Figure 6 is a direct plot of the required C_1 versus f_{CLK} for R_1 values of 1MΩ and 10MΩ.

R_1 can be a standard 10% resistor, but must be selected between 1MΩ to 10MΩ.

The integrating capacitor "C_1" must be a low leakage, low dielectric absorption type such as teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C_1 must be connected to IR_{OUT}.

4. CONVERSION TIME

As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

$$t_{convert} = t_{STRT} + \frac{34306}{f_{CLK}} + R_1C_1$$

where:

t_{STRT} = STRT pulse duration
R_1C_1 = Integrator Time Constant
f_{CLK} = CLK Frequency

For example, if $V_{EEF1} = 4.25V$, $R_1 = 1M\Omega$, $C_1 = 4{,}000pF$ and CLK = 1MHz, the conversion time (not including t_{STRT}, which is normally only microseconds in duration) is approximately 40 milliseconds.

5. EXTERNAL OR AUTO STRT OPERATION

The STRT pin can be driven externally, or with the addition of C_2, made to self-start.

The size of C_2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

$$t_{DAV} \approx (1.7 \times 10^6\Omega)\ C_2 + 20\mu s$$

When first applying power to the AD7550, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation.

6. INITIAL CALIBRATION

Trim R_4 (Figure 3) so that pin 2 (IRJCT) equals 1/2 V_{REF1} ±0.6%. When measuring the voltage on IRJCT, apply a Logic "1" to the STRT terminal.

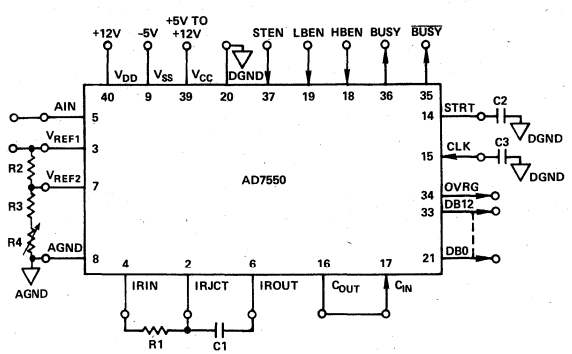


Figure 3. Operation Diagram

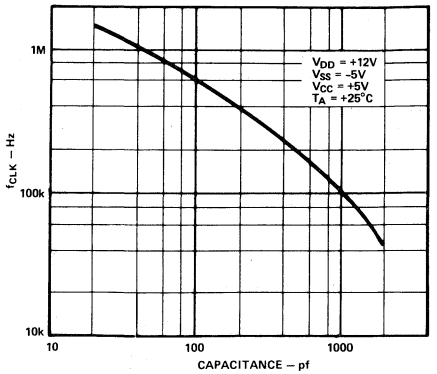


Figure 4. f_{CLK} vs. C_3

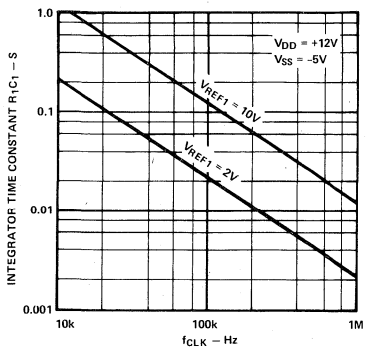


Figure 5. Integrator Time Constant (R_1C_1) vs. f_{CLK} for Different Reference Voltages

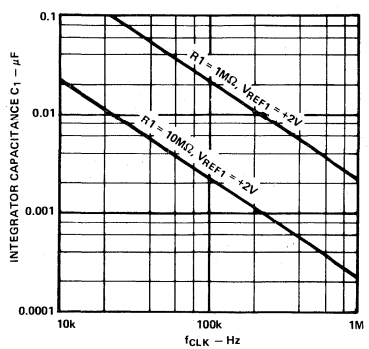


Figure 6. Integrator Capacitance (C_1) vs. f_{CLK} for Different Integrator Resistances (R_1)

APPLICATION HINTS

When operating at f_{CLK} greater than 500kHz, the following steps are recommended to minimize errors due to noise coupling (see Figure 7).

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01µF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R_1 and C_1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C_1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying STEN to the 1 state and driving HBEN and LBEN with BUSY. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.

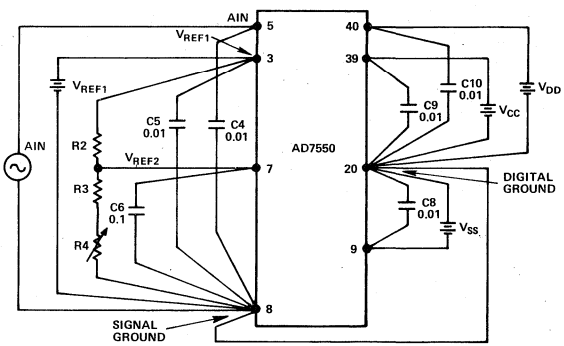


Figure 7. Ground System

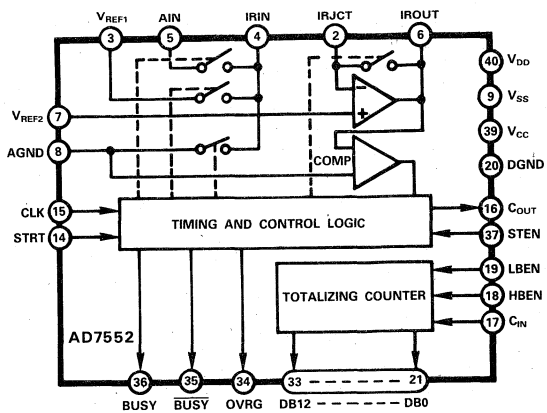
CMOS 12-Bit Plus Sign Monolithic A/D Converter

AD7552

FEATURES

12-Bit Binary with Polarity and Overrange
Accuracy ±1LSB
Microprocessor Compatible
Ratiometric Operation
Low Power Dissipation
Low Cost

AD7552 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7552 is a 12-bit plus sign and overrange monolithic CMOS analog to digital converter. The "Quad Slope" conversion algorithm (Analog Devices patent No. 3872466) converts any offset voltages due to the integrator, comparator etc. to a digital number and subsequently reduces the total system drift error to a second order effect.

The AD7552 parallel output data lines have three-state logic and are microprocessor compatible. Separate enable lines control the lower eight LSBs (low byte enable) and the five MSBs (high byte enable). An overrange flag is also available which together with the BUSY and $\overline{\text{BUSY}}$ flags can be interrogated through the STATUS ENABLE providing easy microprocessor interface.

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N40A)

[1]See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The output data (12-bits plus sign) may be directly accessed under control of two byte enable signals for a simple parallel bus interface. The overrange and converter busy signals are accessed by a status enable signal.
2. The AD7552 conversion time is approximately 160ms with a 250kHz clock.
3. Serial count out available for isolated A/D conversion via opto-isolators.
4. A conversion start can be controlled by an externally applied signal or, with the addition of a capacitor, the converter can be made to self start.
5. For most applications, the AD7552 needs only three resistors, one capacitor, and a reference voltage since the integrating amplifier, comparator, switches and digital logic are all on the CMOS chip.

10

SPECIFICATIONS (V_{DD} = +12V, V_{CC} = +5V, V_{SS} = −5V, V_{REF1} = +4.25V unless otherwise noted)[1]

Parameter	T_A = +25°C	T_A = 0 to +70°C	Units	Conditions/Comments
ACCURACY				
Resolution	12-bits plus sign	12-bits plus sign		Binary 2's complement coding
Accuracy of Reading (Including Noise)	±1	±1	Counts max	f_{CLK} = 250kHz, R1 = 1.8MΩ. C1 = 0.01μF 95% of conversions meet this specification
Noise (Flicker)	±1	±1	Counts max	From nominal reading, not exceeded 95% of time
	±2	±2	Counts max	From nominal reading, not exceeded 99% of time
ANALOG INPUTS				
AIN (pin 5) Input Resistance[2]	R1	R1	MΩ min	R1 is the external integrating resistor
V_{REF1} (pin 3) Input Resistance[2]	R1	R1	MΩmin	connected between IROUT and IRJCT
V_{REF2} (pin 7) Leakage Current	1	10	nA typ	
DIGITAL INPUTS				
CIN (pin 17), HBEN (pin 18), LBEN (pin 19), STEN (pin 37)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+2.4	+2.4	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}, I_{IH}	1	1	μA max	V_{CC} = +5V to +12V
START (pin 14)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V to V_{DD}
V_{IH}	+3.0	+3.0	V min	
I_{IL}	−5/−50	−5/−50	μA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OL}
I_{IH}	+0.5/+2.0	+0.5/+2.0	mA typ/max	V_{CC} = +5V to V_{DD}, BUSY (pin 36) = V_{OH}
CLOCK (pin 15)				
V_{IL}	+0.8	+0.8	V max	V_{CC} = +5V
V_{IH}	+3.0	+3.0	V min	
V_{IL}	+1.2	+1.2	V max	V_{CC} = +12V (V_{IL} = 10% of V_{CC})
V_{IH}	+10.8	+10.8	V min	(V_{IH} = 90% of V_{CC})
I_{IL}	−0.1/−1.0	−0.1/−1.0	mA typ/max	V_{IN} = V_{IL}; V_{CC} = +5V to +12V
I_{IH}	+0.1/+1.0	+0.1/+1.0	mA typ/max	V_{IN} = V_{IH}; V_{CC} = +5V to +12V
DIGITAL OUTPUTS				
C_{OUT} (pin 16), OVRG (pin 34) $\overline{BUSY}$ (pin 35), BUSY (pin 36) and DB0–DB12 (pins 21–33)				
V_{OL}	+0.8	+0.8	V max	V_{CC} = +5V, I_{SINK} = 1.6mA
V_{OH}	+4.0	+4.0	V min	V_{CC} = +5V, I_{SOURCE} = 40μA
V_{OL}	+1.2	+1.2	V max	V_{CC} = +12V, I_{SINK} = 1.6mA
V_{OH}	+10.8	+10.8	V min	V_{CC} = +12V, I_{SOURCE} = 0.6mA
Capacitance per Pin[3]	5	5	pF typ	Outputs in high impedance state
Leakage per Pin	1	1	μA max	Outputs in high impedance state
DYNAMIC PERFORMANCE				
Conversion Time	160	160	ms typ	R1 = 1.8MΩ, C1 = 0.01μF, f_{CLK} = 250kHz
Propagation Delays[3]				
STEN to BUSY, $\overline{BUSY}$, or OVRG	400	700	ns max	Typically 250ns at +25°C (see next page) Flag load = 20pF
LBEN to DB0–DB7	300	500	ns max	Typically 160ns at +25°C (see next page) DB0–DB7 load = 20pF
HBEN to DB8–DB12	300	500	ns max	Typically 160ns at +25°C (see next page) DB8–DB12 load = 20pF
STRT Pulse Width	300	500	ns min	Typically 220ns at +25°C V_{IN} (STRT) = 0 to +3V
POWER SUPPLIES				
V_{DD}	+10/+12	+10/+12	V min/max	
V_{SS}	−5/−12	−5/−12	V min/max	
V_{CC}	+5/V_{DD}	+5/V_{DD}	V min/max	
I_{DD}	0.8/2	0.8/2	mA typ/max	STRT (pin 14) held HIGH,
I_{SS}	0.3/2	0.3/2	mA typ/max	digital outputs floating.
I_{CC}	0.1/1	0.1/1	mA typ/max	V_{CC} = +5V
	0.5/2	0.5/2	mA typ/max	V_{CC} = +12V

NOTES
[1]Full scale voltage = ± V_{REF1} ÷ 2.125. For V_{REF1} = +4.25V FS voltage is ±2.00V.
[2]The equivalent input circuit is the integrator resistor R1 in series with a voltage source V_{REF2} = V_{REF}/1 ÷ 2, see Figure 1.
[3]Guaranteed but not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +14V
V_{DD} to DGND	0V, +14V
V_{SS} to AGND	0V, −14V
V_{SS} to DGND	0V, −14V
AGND to DGND	0V, +14V
V_{CC} to DGND	0V, V_{DD}
V_{REF1}	V_{SS}, V_{DD}
V_{REF2}	AGND, V_{DD}
AIN	V_{SS}, V_{DD}
IRIN	V_{SS}, V_{DD}
IRJCT	AGND, V_{DD}
IROUT	V_{SS}, V_{DD}
Digital Input Voltage	
HBEN, LBEN, STEN, C_{IN}	DGND, (DGND +27V)
CLK, START	DGND, V_{DD}
Digital Output Voltage	
DB0–DB12, OVRG, BUSY, $\overline{BUSY}$, C_{OUT}	DGND, V_{CC}
Operating Temperature Range	0 to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation (Package)	
Up to +50°C	1000mW
Derates above +50°C by	10mW/°C
Lead Temperature (Soldering, 10secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

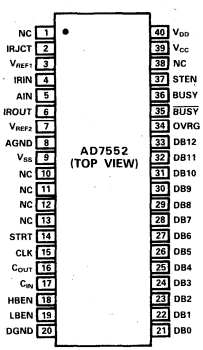
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

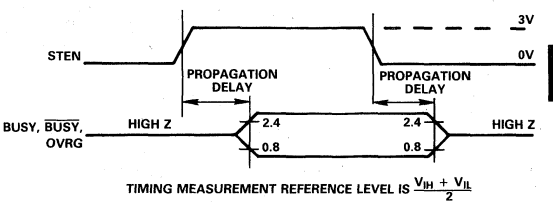
ORDERING INFORMATION

Price Model	Temperature Range	Package[1]
AD7552KN	0 to +70°C	Plastic–N40A

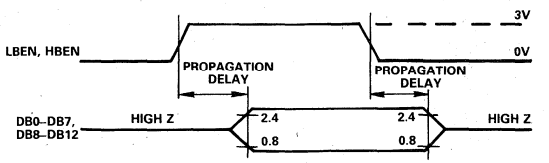
[1]See Section 19 for package outline information.

PIN CONFIGURATION





STEN to BUSY, $\overline{BUSY}$, or OVRG Propagation Delays



LBEN to DB0–DB7, HBEN to DB8–DB12 Propagation Delays

PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	NC	No Connection
2	IRJCT	IntegratoR JunCTion. Summing junction (negative input) of integrating amplifier.
3	V_{REF1}	Voltage REFerence Input (normally +4.25 volts).
4	IRIN	IntegratoR INput. External integrating resistor R1 is connected between IRJCT and IRIN.
5	AIN	Analog INput. Unknown analog input voltage to be measured. Full scale AIN equals $V_{REF}/2.125$.
6	IROUT	IntegratoR OUTput. External integrating capacitor C1 is connected between IROUT and IRJCT.
7	V_{REF2}	Voltage REFerence ÷ 2 Input. V_{REF2} is normally obtained by a potential divider circuit as shown in Figure 3.
8	AGND	Analog GrouND
9	V_{SS}	Negative Supply (−5V to −12V)
10	NC	No Connection
11	NC	No Connection
12	NC	No Connection
13	NC	No Connection
14	STRT	STaRT Conversion. When STRT goes to a Logic "1", the AD7552's digital logic is set up and BUSY is latched "high". When STRT returns "low", conversion begins in synchronization with CLK. Reinitiating STRT during conversion causes a conversion restart. STRT can be driven from an external logic source or can be programmed for continuous conversion by connecting an external capacitor between STRT and DGND. An externally applied STRT command must be a positive pulse of at least 300 nanoseconds to ensure proper set-up of the AD7552 internal logic.
15	CLK	CLocK Input. The CLK can be driven from external logic, or can be programmed for internal oscillation by connecting an external capacitor between CLK and DGND.
16	C_{OUT}	Count OUT provides a number (N) of gated clock pulses given by: $$N = \left[\frac{AIN}{V_{REF1}} 2.125 + 1\right] 4096$$
17	C_{IN}	Count IN is the input to the output counter. 2's complement binary data appears on the DB0 through DB12 output lines (if the HBEN and LBEN enable lines are "high") if C_{OUT} is connected to C_{IN}.
18	HBEN	High Byte ENable is the three-state logic enable input for the DB8–DB12 data outputs. When HBEN is "low", the DB8–DB12 outputs are floating. When HBEN is "high," digital data appears on the data lines.
19	LBEN	Low Byte ENable is the three-state logic enable for DB0–DB7. When LBEN is "low," DB0–DB7 are floating. When "high," digital data appears on the data lines.
20	DGND	Digital GrouND is the ground return for all digital logic and the comparator.
21	DB0	Data Bit 0 (least significant bit)
22	DB1	
23	DB2	
24	DB3	
25	DB4	
26	DB5	
27	DB6	CODE: 2's Complement
28	DB7	
29	DB8	
30	DB9	
31	DB10	
32	DB11	
33	DB12	Data Bit 12 (most significant bit)
34	OVRG	OVerRanGe indicates a Logic "1" if AIN exceeds plus or minus full scale by at least 1/2LSB. OVRG is a three-state output and floats until STEN is addressed with a Logic "1".
35	$\overline{BUSY}$	Not BUSY. $\overline{BUSY}$ indicates whether conversion is complete or in progress. $\overline{BUSY}$ is a three-state output which floats until STEN is addressed with a Logic "1." When addressed, $\overline{BUSY}$ will indicate either a "1" (conversion complete) or a "0" (conversion in progress).
36	BUSY	BUSY indicates conversion status. BUSY is three-state output which floats until STEN is addressed with a Logic "1." When addressed, BUSY indicates a "0" (conversion complete) or a "1" (conversion in progress).
37	STEN	STatus ENable is the three-state control input for BUSY, $\overline{BUSY}$, and OVRG. When STEN is "high", the three outputs are enabled.
38	NC	No Connection
39	V_{CC}	Logic Supply. Digital inputs and outputs are TTL compatible if V_{CC} = +5V, CMOS compatible for V_{CC} = +10V to V_{DD}.
40	V_{DD}	Positive Supply +10V to +12V.

Component limitations such as switch leakage, as well as operational amplifier offset voltage and bias current (and the temperature dependency of these errors), are major obstacles when designing high resolution integrating A/D converters. The AD7552 utilizes a patented *quad slope* conversion technique (Analog Devices Patent No. 3872466) to reduce the effects of such errors to second order effects.

Figure 1 shows a simplified quad slope integrator circuit. The various inputs AGND (Analog Ground), V_{REF1}, and AIN (Analog Input) are applied in sequence to the integrator via switches 1-3 (see Table I), creating four slopes at the integrator output (phase 1-4 of Figure 2). If the equivalent summing junction voltage V_S is precisely $0.5V_{REF1}$, the phase 1 and phase 2 integration times are equal, indicating there are no input errors. If $V_S \neq 0.5V_{REF1}$ (due to amplifier offset voltage, bias current, etc.), an error count "n" is obtained. The analog input integration cycle (phase 3) is subsequently lengthened or shortened by "n" counts, depending on whether the error was positive or negative.

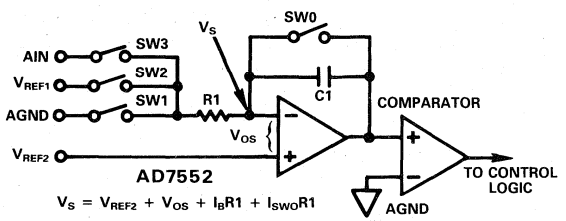


Figure 1. Simplified Quad Slope Integrator Circuit

Phase	Input Voltage	Integration Time
1	AGND–V_S	$t_1 = K_1t$
2	V_{REF1}–V_S	$t_2 = (K_1 + n)t$
3	AIN–V_S	$t_3 = (2K_1 - n)t$
4	V_{REF1}–V_S	$t_4 = (K_3 - 2K_1 + n - 2N)t$

Table I. Integrator Equivalent Input Voltages and Integration Times

where:
t = The CLK period
n = System error count
K_1 = A fixed count equal to 4352 counts
K_2 = A fixed count equal to 17408 counts ($K_2 = 4K_1$)
K_3 = A fixed count equal to 25600 counts
N = Digital output count corresponding to the analog input voltage, AIN

The time t_5 between the phase 4 zero crossing and the termination of counter K_3 is considered equal to 2N counts. N, the number of counts at the C_{OUT} terminal, is obtained by a divide-by-two counter stage. This reduces "jitter" effect. Barring third (and higher) order effects, it can be proven that:

(EQN 1)

$$N = \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right)\cdot 2K_1 + \frac{K_3}{2}}_{\text{ideal term}} + \underbrace{\left(\frac{AIN}{V_{REF1}} - 1\right)\cdot\left[\frac{AGND}{V_{REF1}}(1 + 2\alpha) - \alpha^2\right]\cdot 2K_1}_{\text{error term}}$$

where:

AGND = Voltage at AD7552 pin 8 (AGND) measured with respect to V_{REF1} and AIN signal common ground. (Ideally, AGND = 0V)

α is an error term equal to $\dfrac{2V_S - V_{REF1}}{V_{REF1}}$

Ideally $\alpha = 0$ when $V_S = 0.5V_{REF1}$.

NOTE:
$V_S = V_{REF2} + V_{OS} + I_B R_1 + I_{SWO} R_1$

WHERE:
$V_{REF2} = 0.5V_{REF1}$ if no error is present
V_{OS} = Offset voltage of integrator amplifier
$I_B R1$ = Equivalent integrator amplifier offset voltage due to bias current of integrator amplifier
$I_{SWO} R1$ = Equivalent integrator amplifier offset voltage due to SW0 leakage current.

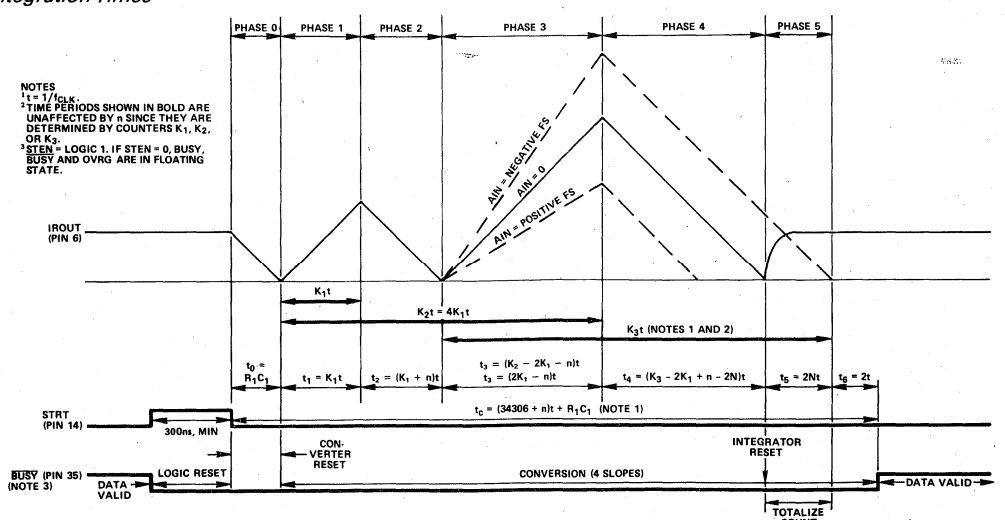


Figure 2. Quad Slope Timing Diagram

The ideal case assumes:

AGND = 0V

$V_S = \frac{V_{REF1}}{2}$, therefore $\alpha = 0$

Then (EQN 1) simplifies to:

$$N = \frac{AIN}{V_{REF1}} \cdot 8704 + 4096 \qquad \text{(EQN 2)}$$

or

$$N = \frac{AIN}{FS} \cdot 4096 + 4096 \qquad \text{(EQN 3)}$$

where:

FS = full scale input voltage = $\frac{V_{REF1}}{2.125}$

Equation 1 shows that only α and AGND generate error terms. Errors due to $\alpha \neq 0$ are strongly reduced because of the α^2 term in equation 1. Errors due to AGND $\neq 0$ will, however, have a first order effect on the system performance. Great care should be taken in any circuit layout to minimize or eliminate ground loops between AGND and signal ground. A recommended grounding system is shown in Figure 5.

OUTPUT CODING

The parallel output (DB0–DB12) of the AD7552 represents the number N in binary 2's complement coding when the C_{OUT} pin is connected to the C_{IN} pin (see Table II).

Analog Input (Note 1)	N (Note 2)	Parallel Digital Output (Note 3)			
		OVRG	DB12	DB11	DB0
+Overrange	8191	1	0	1111 1111 1111	
+(FS – 1LSB)	8191	0	0	1111 1111 1111	
+1LSB	4097	0	0	0000 0000 0001	
0	4096	0	0	0000 0000 0000	
–1LSB	4095	0	1	1111 1111 1111	
–(FS – 1LSB)	1	0	1	0000 0000 0001	
–FS	0	0	1	0000 0000 0000	
–Overrange	0	1	1	0000 0000 0000	

NOTES:
[1]FS = $\frac{V_{REF1}}{2.125}$; 1 Least Significant Bit (LSB) = FS(2^{-12})
[2]N = number of counts at C_{OUT} pin
[3]C_{OUT} strapped to C_{IN}; LBEN and HBEN = Logic 1

Table II. Output Coding (Bipolar 2's Complement)

ANALOG CIRCUIT SET-UP AND OPERATION

The following steps, in conjunction with the analog circuitry of Figure 3 explain the selection of the various component values required for proper operation.

1. **Determination of V_{REF1}**
   The reference voltage V_{REF1} and the full scale input voltage FS are related by

   $$V_{REF1} = 2.125\ (FS)$$

   V_{REF1} must be positive for proper operation. A typical value of V_{REF1} is +4.25V. An AD584 may be used to provide the reference.

2. **Selection of Integrator Components R1 and C1**
   The integrator time constant should be approximately equal to

   $$R1\,C1 \approx \frac{V_{REF1}(9 \times 10^3)}{f_{CLK}(V_{DD} - 4V)}$$

   The integrating capacitor C1 should be a low leakage, low dielectric absorption type such as Teflon, polystyrene or polypropylene. To minimize noise, the outside foil of C1 should be connected to the output of the integrating amplifier and not to its summing junction.

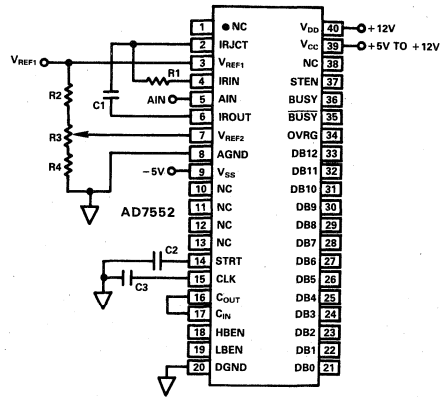


Figure 3. AD7552 Operational Diagram

Improper selection of the integrator time constant (time constant = R1 C1) may cause excessive noise due to the integrator output swing being too low, or may cause nonlinear operation if the integrator output attempts to exceed the rated output voltage of the amplifier.

3. **Determining Conversion Time**
   As shown in Figure 2, the conversion time is independent of the analog input voltage AIN, and is given by:

   $$t_{CONVERT} = t_{STRT} + \frac{34306}{f_{CLK}} + R1\,C1$$

   where:
   t_{STRT} = STRT pulse duration.
   R_1C_1 = Integrator Time Constant.
   f_{CLK} = CLK Frequency at pin 15.

4. **External or Auto STRT Operation**
   The STRT pin can be driven externally, or with the addition of C2, made to self-start.

   The value of C2 determines the length of time from end of conversion until a new conversion is initiated. This is the "data valid" time and is given by:

   $t_{DAV} \approx (1.17 \times 10^6\Omega)\ C2 + 20\mu s$

   When first applying power to the AD7552, a 0V to V_{DD} positive pulse (power up restart) is required at the STRT terminal to initiate auto STRT operation. See APPLICATIONS HINTS No. 5.

5. **Internal Clock Operation**
   The CLK input, pin 15, should normally be driven from an external crystal frequency source, particularly if operation above 250kHz is required. However, for noncritical applications an internal clock oscillator can be activated when a capacitor is connected from pin 15 to DGND. Figure 4 shows a typical curve of clock frequency versus capacitance, C3. Due to process variations the actual operating frequency for a given value of C3 can vary from device to device by up to 100%. Consequently it may be necessary to "tune" C3 to provide the correct clock frequency for a given V_{REF1} and R1C1. For proper operation the clock frequency should be limited to 250kHz. Conversion speeds of up to 80ms can be obtained by increasing the clock frequency to 500kHz. However the flicker due to noise will also increase. See APPLICATIONS HINTS No. 8.

6. **Initial Calibration**
   Trim R3 (Figure 3) so that the voltage on pin 2 (IRJCT) equals $1/2V_{REF1} \pm 0.6\%$. During this trim and measurement cycle apply a logic HIGH to pin 14 (STRT). This will prevent the AD7552 from executing a conversion.

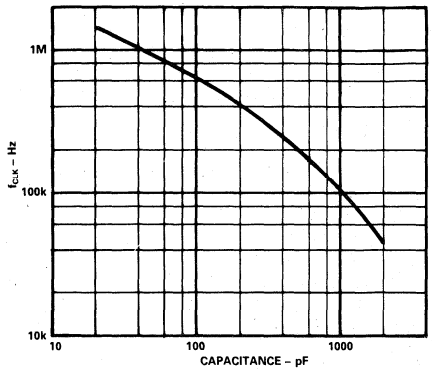


Figure 4. Internal Clock Frequency vs. C3

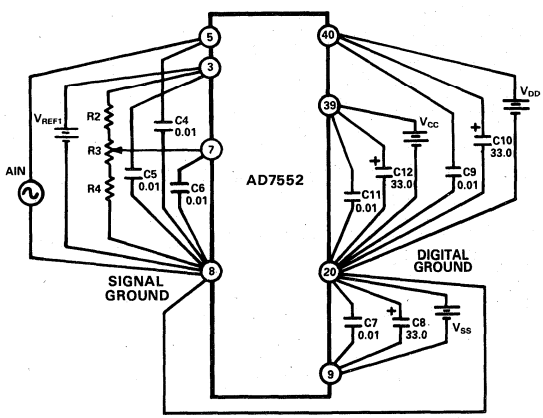
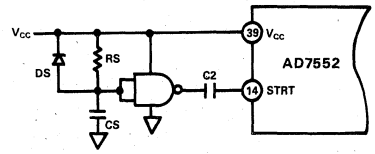


Figure 5. Recommended Grounding System

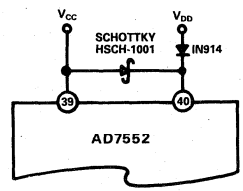
APPLICATIONS HINTS

1. Decouple AIN (pin 5), V_{REF1} (pin 3) and V_{REF2} (pin 7) through 0.01μF to signal ground.
2. Signal ground must be located as close to pin 8 (AGND) as possible.
3. Keep the lead lengths of R1 and C1 toward pin 2 (IRJCT) as short as possible. In addition, both components should lie over the analog ground plane. If C1 has an outside foil, connect it to pin 6 (IROUT), not pin 2.
4. Hold the data bit enables (HBEN, LBEN) in the 0 state during conversion. This is easily accomplished by tying $\overline{\text{STEN}}$ to the 1 state and driving HBEN and LBEN with $\overline{\text{BUSY}}$. This prevents the DB0 through DB12 outputs from coupling noise into the integrator during the phase 1–4 active integration periods.
5. To avoid the requirement of providing a positive STRT pulse on power-up to initiate the auto start operation, the following circuit may be used.

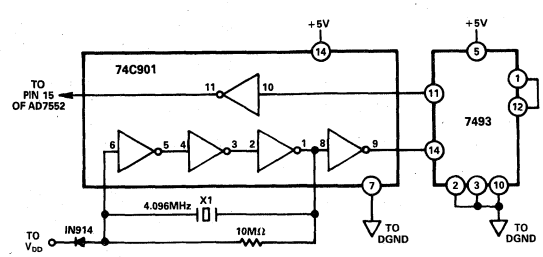


The output of the open collector NAND gate is initially high on power-up. When the charging voltage on CS reaches the input threshold level of the NAND gate, the output goes low and remains low to allow the AD7552 to self start.

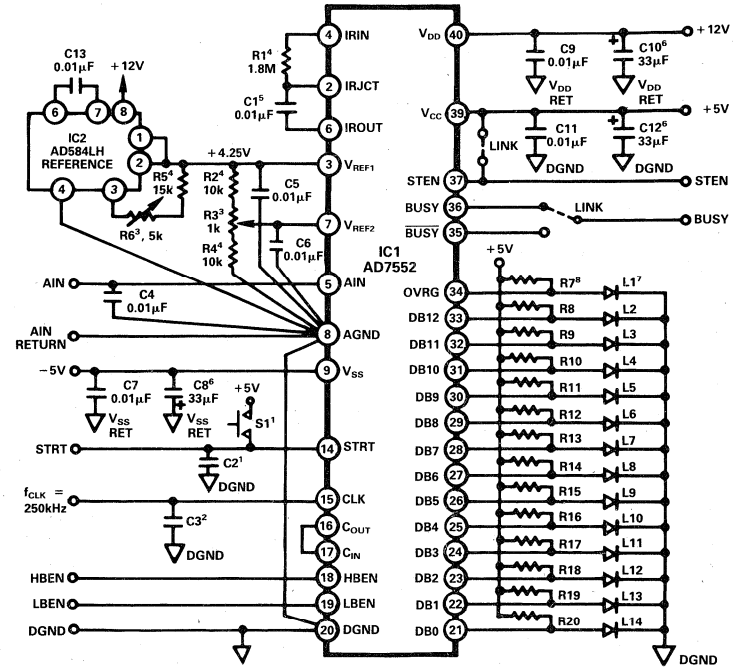
6. Under no circumstances should V_{CC} exceed V_{DD} especially during power-up and power-down. In cases where this situation could occur the following diode protection scheme is recommended.



7. Some solder fluxes and cleaning materials can form slightly conductive films which cause leakage effects across the integrating capacitor. The user is cautioned to ensure that the manufacturing process for circuits using the AD7552 does not allow such films to remain after assembly. Otherwise the accuracy and noise performance of the device will be affected.
8. A suggested crystal oscillator circuit is shown below for use with a V_{CC} of +5V. It uses a standard 4.096MHz crystal which is divided down by 16 to produce a clock frequency of 256kHz.



9. A printed circuit layout for an evaluation board is shown in Figure 8a and 8b. Figure 6 shows the circuit diagram for this evaluation board with component values for $f_{CLK} \doteq 250$kHz, $V_{REF1} = +4.25$V operation. Figure 7 shows the component overlay for Figure 8a. Note that either $\overline{\text{BUSY}}$ (pin 35) or BUSY (pin 36) is available at the edge connector via a wire link. Note also that STEN (pin 37) may be tied high via a wire link.



NOTES:
[1]S1 IS A PUSHBUTTON SWITCH TO INITIATE AUTO-START OPERATION. S1 AND C2 ARE NOT REQUIRED FOR EXTERNAL START OPERATION.
[2]C3 IS NOT REQUIRED FOR EXTERNAL CLOCK OPERATION.
[3]FOR CALIBRATION HOLD PIN 14 (STRT) HIGH. ADJUST R6 UNTIL THE VOLTAGE ON PIN 3 (V_{REF1}) IS 4.250V. ADJUST R3 UNTIL THE VOLTAGE ON PIN 2 (IRJCT) IS 2.125 ±0.025V.
[4]R1, R2, R4, R5 1% TOLERANCE, METAL FILM.
[5]C1 MUST BE A LOW LEAKAGE, LOW DIELECTRIC ABSORPTION TYPE SUCH AS TEFLON, POLYSTYRENE OR POLYPROPYLENE.
[6]C8, C10 AND C12 ARE SOLID ELECTROLYTE TANTULUM CAPACITORS.
[7]L1 – L14 ARE LEDS, MONSANTO MV55 OR EQUIVALENT.
[8]R7 – R13 AND R14 – R20 ARE PROVIDED BY TWO THICK-FILM. RESISTOR NETWORKS, EACH IN AN 8-PIN SINGLE-IN-LINE PACKAGE. SUITABLE NETWORKS AVAILABLE FROM BECKMAN INSTRUMENTS INC., 2500 HARBOR BOULEVARD, FULLTERTON, CA 92634, MODEL NO. 764–1–4K7.

Figure 6. Evaluation Board Circuit with Component Values for f_{CLK} = 250kHz, V_{REF1} = +4.25V

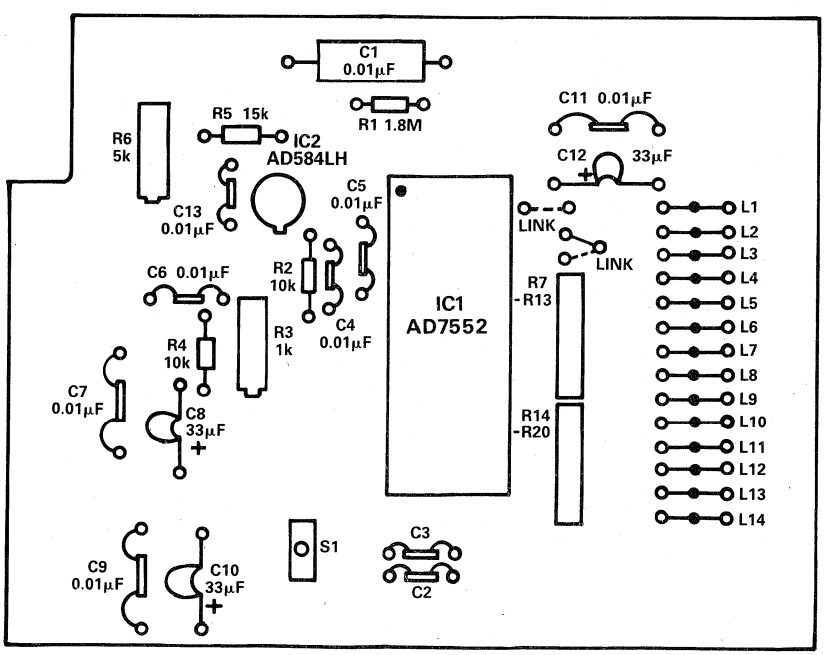


Figure 7. Component Overlay for Figure 8a

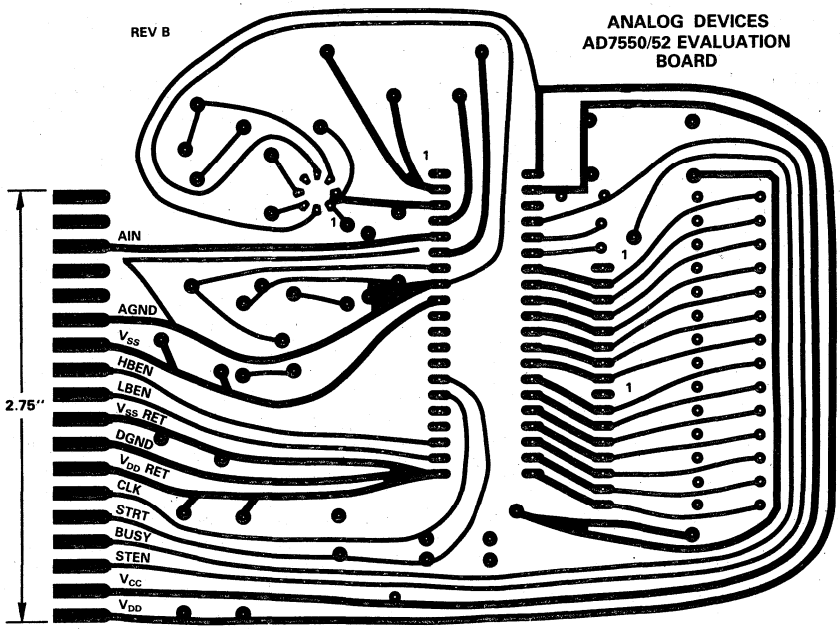


Figure 8a. Component Side

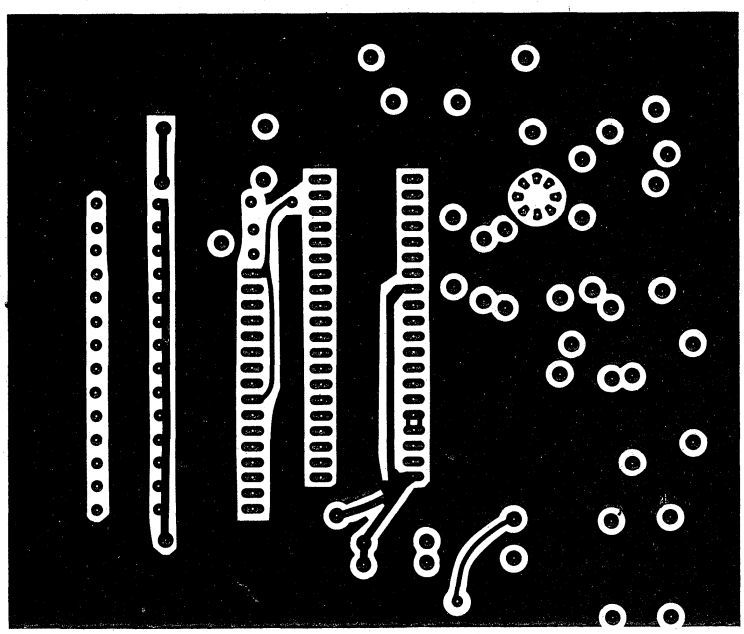


Figure 8b. Foil Side

OBTAINING SIGN-MAGNITUDE 4 DIGIT BCD CODING FROM THE AD7552

Referring to Figure 9 when a convert start pulse is received the four decade presettable up/down counter is loaded with the value 4096. The low level on the up/down count input (Q of X1 = 0) places the CD4029 counters into the count down mode. The contents of the four decade BCD counter are decremented each time a pulse is detected on C_{OUT}. The number of pulses appearing on C_{OUT} is related to both the magnitude and the polarity of the input voltage. If the counter reaches the all 0's state, the flip-flop (X1) is set, placing a high level signal on the up/down count input. The counter will now count up on succeeding C_{OUT} pulses.

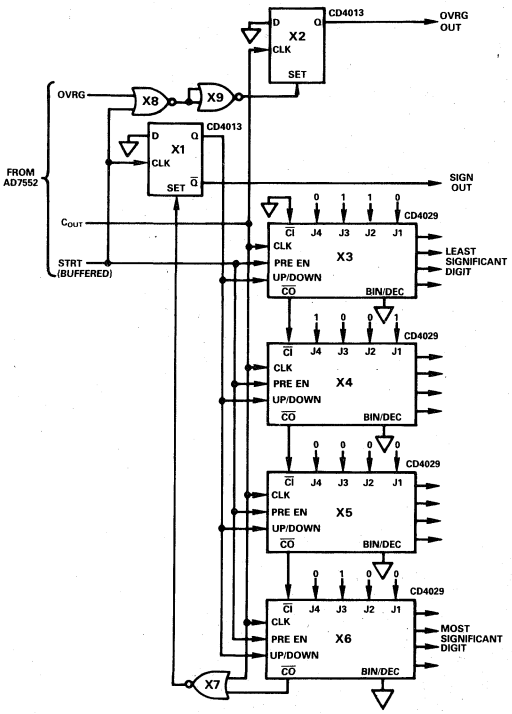


Figure 9. Sign-Magnitude BCD Conversion Circuitry

Analog Input[2]	N[3]	SIGN-MAGNITUDE BCD CODING[1] OVRG	Sign	Digit 4	Digit 3	Digit 2	Digit 1
+Overrange	8191	1	0	4	0	9	5
+FS − 1LSB	8191	0	0	4	0	9	5
+1LSB	4097	0	0	0	0	0	1
0+	4096	0	0	0	0	0	0
0−	4096	0	1	0	0	0	0
−1LSB	4095	0	1	0	0	0	1
−(FS − 1LSB)	1	0	1	4	0	9	5
−FS	0	1	1	4	0	9	6
−Overrange	0	1	1	4	0	9	6

NOTES
[1]Using circuit of Figure 9.
[2] FS = $V_{REF1} \div 2.125$; 1 Least Significant Bit (LSB) = FS(2^{-12}).
[3]N = number of counts at C_{OUT} pin.

Table III. Sign-Magnitude BCD Coding

Referring to Table III no counts occur on C_{OUT} when the input voltage is either overrange or equal to −FS. Since the most negative value which can be represented in sign-magnitude coding is −(FS − 1LSB) whereas in two's complement coding it is −FS, the X2 flip-flop of Figure 9 ensures that the OVRG output is high if either AIN is overrange or AIN = −FS. Note that there are two codes for zero analog input. This is the result of gating the carry out signal from X6 with the input clock signal C_{OUT}. As mentioned previously, the number of counts at the C_{OUT} terminal is obtained by an internal divide-by-two counter stage. Depending on whether the number of counts to this divide-by-two was odd or even C_{OUT} can remain in either a high or a low state at the end of phase 4. If AIN is negative and less than 1/2LSB (AIN = 0−), C_{OUT} is high after outputting 4096 counts thus preventing the sign flag from changing. If AIN is positive and less than 1/2LSB, C_{OUT} is low after outputting 4096 counts allowing the sign flag to change. If the carry out signal from X6 is directly connected back to X1, then the code for AIN = 0− vanishes leaving one code (the 0 + one) for 0V.

This circuit may be used to provide direct readout of analog input voltage with proper scaling of the reference voltage and serial output C_{OUT}. For instance, dividing C_{OUT} by two and adjusting V_{REF1} = +4.352V gives a FS voltage of 2.048V which will be displayed directly.

Analog Input[2]	N[3]	SIGN-MAGNITUDE CODING[1] OVRG	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
+Overrange	8191	1	0	1	1	1	1	1	1	1	1	1	1	1	1
+FS − 1LSB	8191	0	0	1	1	1	1	1	1	1	1	1	1	1	1
+1LSB	4097	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	4096	0	0	0	0	0	0	0	0	0	0	0	0	0	0
−1LSB	4095	0	1	0	0	0	0	0	0	0	0	0	0	0	1
−(FS − 1LSB)	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
−FS	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
−Overrange		1	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTES
[1]Using circuit of Figure 10.
[2] FS = $V_{REF1} \div 2.125$; 1 Least Significant Bit (LSB) = FS(2^{-12}).
[3]N = number of counts at C_{OUT} pin.

Table IV. Sign-Magnitude Binary Coding

OBTAINING SIGN-MAGNITUDE BINARY CODING FROM THE AD7552

The circuit of Figure 10 converts the two's complement coding from the AD7552 into sign-magnitude coding. It does this by complementing the AD7552 data and adding 1LSB whenever DB12 is high. In sign-magnitude coding the most negative value that can be represented is −(FS− 1LSB); in two's complement coding it is −FS. The OR gate in Figure 10 ensures only valid output codes are produced (see Table IV). Note that there is only one code for zero scale.

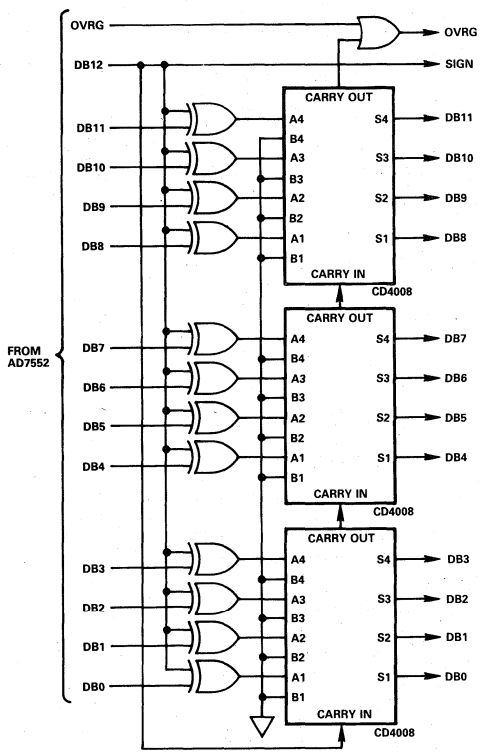


Figure 10. Sign-Magnitude Binary Conversion Circuitry

MICROPROCESSOR INTERFACING

The three-state output capability of the AD7552 allows the multiplexing of the data and status lines onto a single 8-bit wide bus. Figure 11 shows the AD7552 directly interfaced to the 6800 with convert start, data read, etc., all under program control. Note that the two status lines OVRG and BUSY are connected to the data bus in the MSB and LSB positions so that they can easily be interrogated by reading the status word to the microprocessor accumulator, rotating right or left through carry and then checking the carry flag.

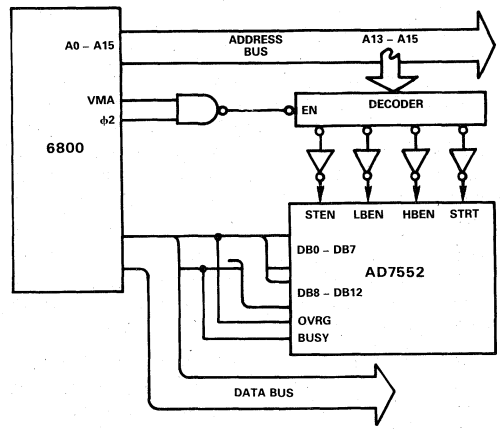


Figure 11. AD7552-6800 Direct Interface

Care should be taken when using fast-access memory or operating at high temperatures to ensure that the AD7552 output drivers relinquish the data bus in time to avoid any possible bus conflict with the following instruction. In any situation where bus conflict is likely, the interfacing technique of Figure 12 is recommended.

10

AD7552–8085A INTERFACE

Figure 12 shows the AD7552 interfaced to the 8085A. In this application the two status lines share the data bus with the data high byte (DB8–DB12) since the STEN and HBEN inputs are driven simultaneously from a single decoded address. The 8282 data latch which buffers the AD7552 three state drivers from the microprocessor bus ensures that the bus is relinquished promptly at the end of a data read instruction.

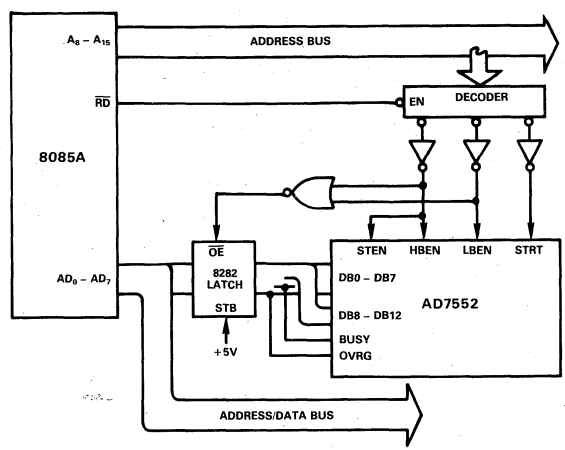


Figure 12. AD7552-8085A Direct Interface

CONTINUOUS CONVERSION MODE

Figure 13 shows the AD7552 connected for continuous conversion. The conversion STRT signal is synchronized with the ALE signal of the 8085A. The $\overline{BUSY}$ signal is used to update the 8-bit data latches at a time when the microprocessor is not attempting a read operation. Thus the AD7552 appears to the microprocessor as memory which can be read at any time although scrambled data can result if a data update occurs between reading the high byte and low byte data. One method of avoiding this is to read data only after an update has occurred. The microprocessor can be interrupted to perform a data read by tying the AD7552 STRT input to one of the RST inputs on the 8085A.

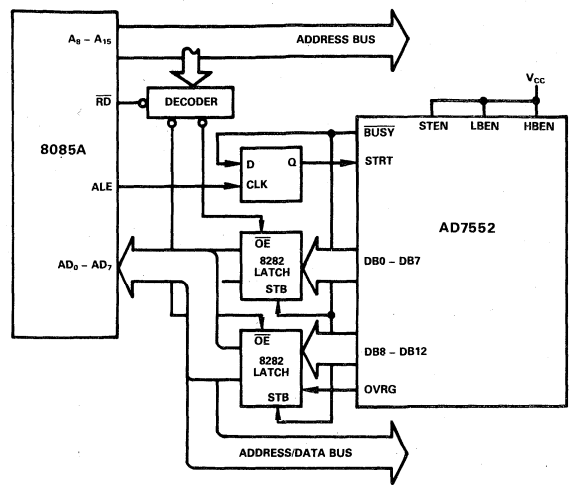


Figure 13. AD7552 in Continous Conversion Mode

OPTO-ISOLATED SERIAL INTERFACE

Figure 14 shows a serial interface to the MCS-85 system. This system can accommodate a remote interface where a common-mode voltage is expected to exist between system grounds.

Port C of the 8155 is configured as a control port. Port B is an input port. This port configuration is necessary if sign and/or overrange information is required. Magnitude information is obtained by interrogating the 8155 counter value. The rising edge of $\overline{BUSY}$ is used to cause an interrupt on the RST 7.5 line. The value ($2^{14} - C_{OUT}$) in the 8155 timer should now be read. When $\overline{BUSY}$ returns low, the 8155 counter is reset to FF_H. The falling edge of $\overline{BUSY}$ also latches the sign and overrange data into port B. This is indicated by a rising edge on BF (buffer full) which can be used to call the 8085 CPU to read port B data.

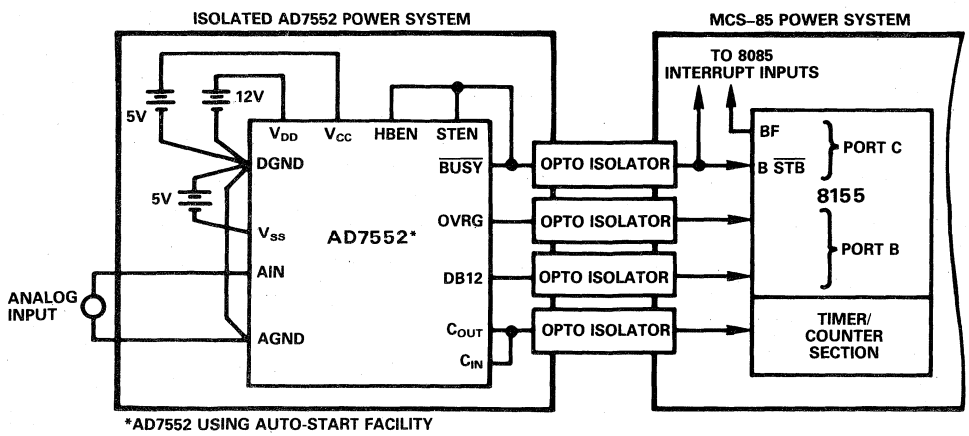
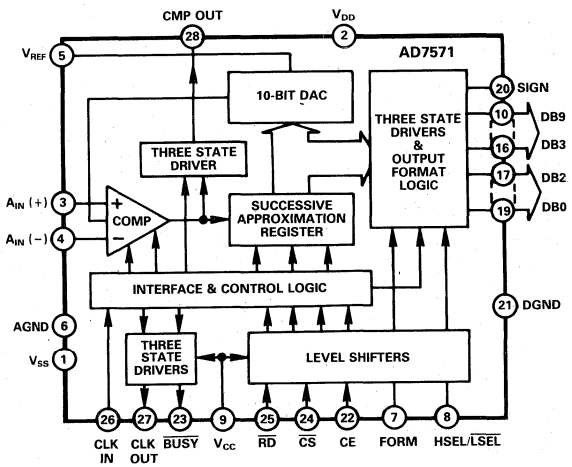


Figure 14. Optically Isolated Serial AD7552/MCS-85 Interface

CMOS
µP-Compatible 10-Bit Plus Sign ADC
AD7571

FEATURES
10-Bit Plus Sign Resolution
No Missed Codes Over Full Temperature Range
Conversion Time 80µs
Differential Analog Voltage Inputs, ±10V Range
Serial and Parallel Data Outputs
Easy Interface to Most Microprocessors
Internal Clock Oscillator
Single Supply Operation for Positive-Only Signals
Monolithic Construction

AD7571 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7571 is a high speed, low cost 10-bit plus sign CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 80µs. The device is designed for easy microprocessor interface allowing full parallel or double byte reading over three-state outputs. Conversion results are also available in serial form allowing opto-isolated operation using as few as two wires for the interconnect.

A new differential analog input configuration is used in the AD7571, increasing the common-mode rejection performance and allowing the analog zero input voltage to be offset from true analog ground. Analog input voltage range is ±10V using a single positive reference. With positive-only input signals the AD7571 can be operated from a single positive power supply.

PRODUCT HIGHLIGHTS

1. Pin Programmable Data Output Formats
   The output format for the 10-bits plus sign data is pin programmable allowing full parallel, two byte (left justified) and serial output formats.
2. Proven Control Logic
   The AD7571 control logic is similar to that used in the highly successful AD7574. This allows the AD7571 to be operated as a memory mapped input device interfacing to the µP via the control lines $\overline{CS}$ (chip select) and $\overline{RD}$ ($\overline{READ}$/WRITE).
3. All Active Components on Chip
   The addition of a few passive support components makes the AD7571 a complete 10-bit plus sign converter requiring only a reference voltage and power supply(ies). An on chip clock is also provided but the device can run from an external clock if required.
4. Differential Analog Inputs
   The analog input voltage can be unipolar or bipolar with an input range of ±10V. The differential input allows asymmetric input voltage ranges to be easily accommodated.
5. Single Supply Operation
   The AD7571 may be operated with a single positive supply if the input signal range is always positive with respect to AGND.

PACKAGE IDENTIFICATION

Suffix "N" – Plastic DIP (N28A)
Suffix "Q" – Cerdip (Q28A)
Suffix "D" – Ceramic DIP (D28B)

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_{CC} = +5V, V_{REF} = +5.12V, f_{CLK} = 550kHz External, Bipolar Configuration. All specifications T_{min} to T_{max} unless otherwise noted)

Parameter	AD7571JN[1]	AD7571KN	AD7571AQ	AD7571BQ	AD7571SD	AD7571TD	Units	Conditions/Comments
ACCURACY[2]								
Resolution	10 bits plus sign	*	*	*	*	*		
Relative Accuracy	±1	±3/4	*	**	*	**	LSB max	
Zero Input Reading	±000H	*	*	*	*	*	Hex	Full Scale Reading is ±3FFH
Roll-Over Error	±2	±1	*	**	*	**	LSB max	Difference in reading for equal positive and negative inputs near full scale
Minimum Resolution for which no Missing Codes are Guaranteed,	10 bits plus sign	*	*	*	*	*		
Full Scale Error (Gain Error)								
+25°C	±4	±3	*	**	*	**	LSB max	
T_{min} to T_{max}	±5	±4	*	**	*	**	LSB max	
Offset Errors								
Positive Differential Input	−3/4; +2	−3/4; +1	*	**	*	**	LSB max	
Negative Differential Input	−3/4; +2	−3/4; +1	*	**	*	**	LSB max	
Sign Bit Offset Error								
+25°C	±1	±1/2	*	**	*	**	LSB max	
T_{min} to T_{max}	±1	±1	*	**	*	**	LSB max	
Offset Error TC	±5	*	*	*	*	*	ppm/°C typ	
Sign Bit Offset TC	±5	*	*	*	*	*	ppm/°C typ	
Full Scale Error TC (Gain Error TC)	±5	*	*	*	*	*	ppm/°C typ	
POWER SUPPLY REJECTION								
V_{DD} Only	1	*	*	*	*	*	LSB max	14.25≤V_{DD}≤15.75V
V_{SS} Only	0.1	*	*	*	*	*	LSB max	−15.75≤V_{SS}≤−14.25V
V_{DD} and V_{SS} Together	1	*	*	*	*	*	LSB max	Same Limits as Above. Worst Case Combination.
ANALOG INPUTS								
Analog Input Range	±10.24	*	*	*	*	*	V	Full Scale with V_{REF} = +5.12V
Analog dc Input Impedance, A_{IN}(+), A_{IN}(−)	10	*	*	*	*	*	MΩ min	
Input Common Mode Voltage	±10	*	*	*	*	*	V	
Common Mode Rejection	0.1	*	*	*	*	*	LSB/V typ	
REFERENCE INPUT								
V_{REF} (for specified performance)	+5.12	*	*	*	*	*	V	±5%
V_{REF} Range[3]	+1 to +6	*	*	*	*	*	V	Degraded transfer accuracy
I_{REF}, Input Reference Current	1.5	*	*	*	*	*	mA max	V_{REF} = +5.12V
LOGIC INPUTS								
FORM (pin 7), HSEL/$\overline{LSEL}$ (pin 8), CE (pin 22), $\overline{CS}$ (pin 24), $\overline{RD}$ (pin 25)								
V_{IL} Input Low Voltage	+0.8	*	*	*	*	*	V max	V_{CC} = +5V
	+1.5	*	*	*	*	*	V max	V_{CC} = +15V
V_{IH} Input High Voltage	+2.4	*	*	*	*	*	V min	V_{CC} = +5V
	+13.5	*	*	*	*	*	V min	V_{CC} = +15V
I_{IN} Input Current +25°C	1	*	*	*	*	*	μA max	V_{IN} = 0V or V_{CC}
T_{min} to T_{max}	10	*	*	*	*	*	μA max	V_{IN} = 0V or V_{CC}
C_{In} Input Capacitance[4]	8	*	*	*	*	*	pF max	
CLK IN (Pin 26)								
V_{IL} Input Low Voltage	+1.5	*	*	*	*	*	V max	
V_{IH} Input High Voltage	+13.5	*	*	*	*	*	V min	
I_{IL} Input Low Current	10	*	*	*	*	*	μA max	
I_{IH} Input High Current	3	*	*	*	*	*	mA max	
LOGIC OUTPUTS								
DB9 to DB0 (pins 10-19), SIGN (pin 20), BUSY (pin 23), CLK OUT (pin 27), CMP OUT (pin 28)								
V_{OH} Output High Voltage	+4.0	*	*	*	*	*	V min	V_{CC} = +5V, I_{SOURCE} = 40μA
	+13.5	*	*	*	*	*	V min	V_{CC} = +15V, I_{SOURCE} = 100μA
V_{OL} Output Low Voltage	+0.4	*	*	*	*	*	V max	V_{CC} = +5V, I_{SINK} = 1.6mA
	+1.5	*	*	*	*	*	V max	V_{CC} = +15V, I_{SINK} = 2mA
Floating State Leakage Current (DB9–DB0, BUSY, CLK OUT, CMP OUT)	±10	*	*	*	*	*	μA max	
Floating State Output Capacitance[4]	7	*	*	*	*	*	pF max	
POWER REQUIREMENTS								
V_{DD}	+11.4 to +16.5	*	*	*	*	*	V	
V_{SS}	−11.4 to −16.5	*	*	*	*	*	V[4]	
V_{CC}	+4.5 to V_{DD}	*	*	*	*	*	V	
I_{DD} +25°C	7.5	*	*	*	*	*	mA max	
T_{min} to T_{max}	9.75	*	*	*	*	*	mA max	
T_{min} to T_{max}	5.0	*	*	*	*	*	mA typ	
I_{SS}	10	*	*	*	*	*	μA typ	
I_{CC}	50	*	*	*	*	*	μA typ	V_{IN} = 0V or V_{CC}
	200	*	*	*	*	*	μA max	
	0.5	*	*	*	*	*	mA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	*	*	*	*	*	mA max	

NOTES

[1]Temperature Range as follows: AD7571JN, KN; 0 to +70°C
AD7571AQ, BQ; −25°C to +85°C
AD7571SD, TD; −55°C to +125°C

[2]The analog input voltage at either AIN+ or AIN− must not exceed the V_{DD} or V_{SS} supply voltages. However, with only positive analog input signals, the AD7571 may be operated with V_{SS} = 0V. All relevant specifications in the above table will apply in this unipolar configuration.

[3]Typical value, not guaranteed or subject to test.

[4]Guaranteed but not tested.

*Specifications same as AD7571JN.

**Specifications same as AD7571KN.

Specifications subject to change without notice.

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = −15V, V_{CC} = +5V, f_{CLK} = 550kHz. External unless otherwise noted)

Parameter		Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (J, K, A & B Grades)	Limit at T_{min}, T_{max} (S & T Grades)	Units	Conditions/ Comments
STATIC RAM INTERFACE MODE		(See Figure 5)				
t_{CS}	$\overline{CS}$ Pulse Width Requirement	100	130	150	ns min	Start Conversion Only
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ Setup Time	0	0	0	ns min	
t_{BSCS}	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0	0	0	ns min	
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	0	0	0	ns min	
t_{RD}	$\overline{RD}$ Pulse Width	t_{RAD}	t_{RAD}	t_{RAD}	ns min	$t_{RD} \geq t_{RAD}$
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	150	190	220	ns typ	$\overline{BUSY}$ Load = 20pF
		210	250	300	ns max	
		175	220	250	ns typ	$\overline{BUSY}$ Load = 100pF
		240	300	340	ns max	
t_{RAD}	Data Access Time	300	360	390	ns typ	Bus Load = 20pF
		430	510	550	ns max	
		460	540	600	ns typ	Bus Load = 100pF
		680	800	900	ns max	
t_{RHD}	Data Hold Time	300	330	360	ns typ	
		200	220	260	ns min	
		400	450	480	ns max	
t_{RHCS}	$\overline{CS}$ to $\overline{RD}$ Hold Time	200	350	500	ns max	
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	0	0	0	ns min	
t_{RESET}	Reset Time Requirement	0.5	0.6	0.8	µs min	
$t_{CONVERT}$	Conversion Time Using Internal Clock Oscillator	See Typical Data of Figure 14.				f_{CLK} = 550kHz
$t_{CONVERT}$	Conversion Time Using External Clock	80	80	80	µs max	See Figure 15.
ROM INTERFACE MODE		(See Figure 8.)				
t_{RD}	$\overline{RD}$ Pulse Width Requirement	Same as t_{RD} in RAM mode.				
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	Same as RAM mode.				
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	Same as RAM mode.				
t_{RAD}	Data Access Time	Same as RAM mode.				
t_{RHD}	Data Hold Time	Same as RAM mode.				
t_{WBPD}	$\overline{RD}$ High to $\overline{BUSY}$ Propagation Delay	0.5	0.7	0.8	µs typ	$\overline{BUSY}$ Load = 20pF
		0.9	1.0	1.4	µs max	
$t_{CONVERT}$	Conversion Time Using Internal Clock Oscillator	Add t_{WBPD} to Typical Data Shown in Figure 14.				
SLOW-MEMORY INTERFACE MODE		(See Figure 11).				
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM mode.				
t_{RAD}	Data Access Time	40	60	70	ns typ	Bus Load = 20pF
		70	100	120	ns max	
		180	230	280	ns typ	Bus Load = 100pF
		300	370	420	ns max	
t_{RHD}	Data Hold Time	Same as RAM mode.				
t_{SELS}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Setup Time	Same as RAM mode.				
t_{SELH}	HSEL/$\overline{LSEL}$ to $\overline{RD}$ Hold Time	Same as RAM mode.				
t_{RESET}	Reset Time Requirement	Same as RAM mode.				
$t_{CONVERT}$	Conversion Time	Same as RAM mode.				
SERIAL DATA OUTPUT		(Applies to all Three Modes, see Figures 5, 8 and 11).				
t_{CEL}	CE to Low Impedance Outputs ($\overline{BUSY}$, CLK OUT, CMP OUT)	60	100	120	ns max	Low Impedance to DGND or V_{CC}
t_{CEH}	CE to High Impedance Outputs ($\overline{BUSY}$, CLK OUT, CMP OUT)	60	100	120	ns max	High Impedance to DGND or V_{CC}
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM mode.				
t_{WBPD}	$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay	Same as ROM mode.				
t_{SDS}	Serial Data to CLK OUT Setup Time	20	20	20	ns min	
t_{SDH}	Serial Data to CLK OUT Hold Time	500	500	500	ns min	

NOTE
All specified control signals are measured with $t_r = t_f$ = 20ns (10% to 90%) for +5V logic and timed from a voltage level of +1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}. Sample tested at +25°C to ensure conformance.

Specifications subject to change without notice.

10

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
V_{CC} to DGND	0V, V_{DD} +0.4
V_{SS} to AGND	0V, −17V
V_{SS} to DGND	0V, −17V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND (pins 7, 8, 22, 24, 25)	−0.3V, V_{CC}
CLK IN Input Voltage (pin 26) to DGND	−0.3V, V_{DD}
Digital Output Voltage to DGND (pins 10-20, 23, 27, 28)	−0.3V, V_{CC}
V_{REF} to AGND	−0.3V, V_{DD}
AIN (+), AIN (−) to AGND	V_{SS}, V_{DD}
Operating Temperature Range	
JN, KN	0 to +70°C
AQ, BQ	−25°C to +85°C
SD, TD	−55°C to +125°C
Storage Temperature	+65°C to +150°C
Lead Temperature (Soldering, 10secs)	+300°C
Power Dissipation (Any Package)	
To +75°C	1,000mW
Derates above +75°C	10mW/°C

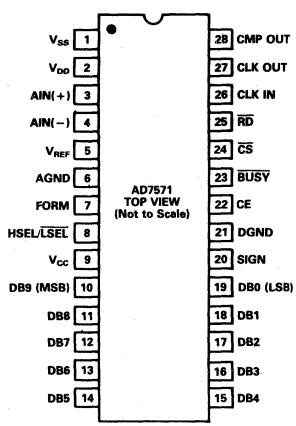
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: V_{CC} should never exceed V_{DD} by more than 0.4V, especially during power ON or OFF sequencing. See diode protection in Figure 16.

CAUTION

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



TERMINOLOGY AND DEFINITIONS

LEAST SIGNIFICANT BIT (LSB)

An ADC with 10-bits plus sign resolution can resolve 1 part in 2^{10} of either positive or negative full scale. For the AD7571 with ±10.24V full scale one LSB is 10.0mV.

RELATIVE ACCURACY

Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the device's measured first LSB transition point and the measured full scale transition point. For the purpose of specifying the relative accuracy of a 10-bit plus sign ADC, the AD7571 is treated as two separate unipolar ADCs with the transfer characteristics for both positive and negative differential inputs measured independently.

DIFFERENTIAL NONLINEARITY (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a non-zero width. Since all grades of the AD7571 guarantee no missing codes to 10-bits plus sign resolution, all 1024 codes plus sign bit (i.e., total of 2048 codes) must be present over the entire operating temperature ranges.

OFFSET ERRORS

Positive Differential Inputs: A measure of the difference between the ideal (+1LSB) and the actual differential analog input level required to produce the first positive LSB code transition (000 . . . 00 to 000 . . . 01), see Figure 1.

Negative Differential Inputs: A measure of the difference between the ideal (−1LSB) and the actual differential input level required to produce the first negative LSB code transition (100 . . . 00 to 100 . . . 01).

ORDERING INFORMATION

Relative Accuracy (T_{min} to T_{max})	Temperature Range and Package: Plastic (N28A) 0 to +70°C	Cerdip[1] (Q28A) −25°C to +85°C	Side-Brazed Ceramic (D28B) −55°C to +125°C
±1LSB	AD7571JN	AD7571AQ	AD7571SD
±1/2LSB	AD7571KN	AD7571BQ	AD7571TD

NOTES

[1]Analog Devices reserves the right to ship ceramic packages in lieu of cerdip packages.

See Section 19 for package outline information.

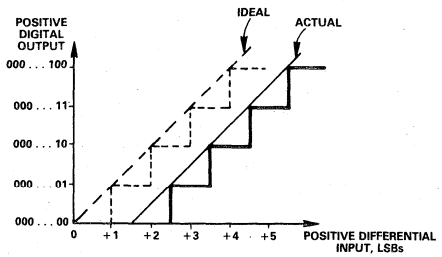


Figure 1. ADC Transfer Characteristics for Positive Differential Input with Offset Error of +1 1/2 LSBs

SIGN BIT OFFSET ERROR

Ideally occurring at 0V input, the sign bit transition may shift by up to ±1/2LSB for the AD7571 K/B/T grades and by ±1LSB for J/A/S grades. However, since all grades of the AD7571 are guaranteed to have no missed codes over their entire temperature ranges, the sign bit transition will always occur before the first LSB transitions occur.

The magnitude and polarity of offset errors depends on the clock frequency and V_{DD} power supply used to operate the AD7571. See Figure 2 and Figure 3.

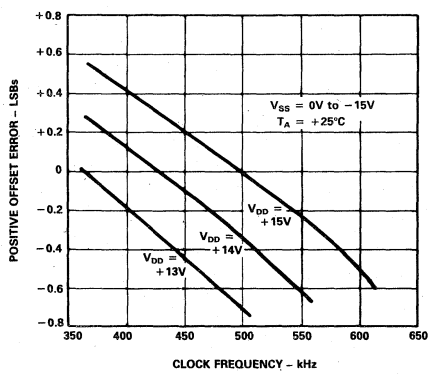


Figure 2. Typical Positive Offset Error vs. Clock Frequency for Different Supply Voltages

FULL SCALE ERROR (GAIN ERROR)

The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last

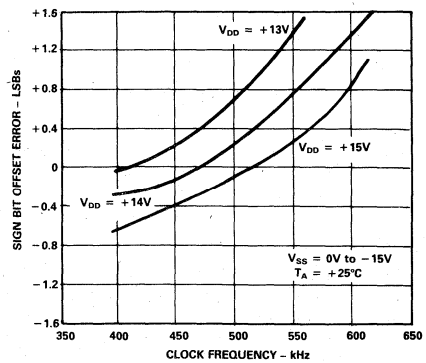


Figure 3. Typical Sign Bit Offset Error vs. Clock Frequency for Different Supply Voltages

digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS–2LSBs. In the AD7571 both positive and negative differential input ADC transfer characteristics exhibit the same magnitude and direction of gain error. This correspondence also extends to the gain error drift performance over temperature.

ZERO INPUT READING

Digital output which results when AIN (+) = AIN (−).

ROLL-OVER ERROR

This is the difference in digital output, i.e., reading, for equal positive and negative inputs near full scale.

POWER SUPPLY REJECTION

A measure of the maximum change in the full scale range of the AD7571 resulting from a change in supply voltage.

INPUT COMMON MODE VOLTAGE

For the AD7571, the voltage at both inputs can be raised above (or lowered below) analog ground potential. The common mode voltage represents the voltage range over which this is allowed. However, the maximum possible differential input signal range will be directly affected by this common mode voltage signal. Table I shows the analog input signal range with a common mode voltage of +6V.

Note that the supply voltage V_{SS} must be at least as negative as the most negative analog input applied to the AD7571.

AIN (+), Volts	AIN (−), Volts	Differential Input, Volts	Output Code										
			Sign	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
+6	+6	0	0	0	0	0	0	0	0	0	0	0	0
+6.01	+6	+0.01	0	0	0	0	0	0	0	0	0	0	1
+10.24	+6	+4.24	0	0	1	1	0	1	0	1	0	0	0
+5.99	+6	−0.01	1	0	0	0	0	0	0	0	0	0	1
−4.24	+6	−10.24	1	1	1	1	1	1	1	1	1	1	1
+6	+6.01	−0.01	1	0	0	0	0	0	0	0	0	0	1
+6	+10.24	−4.24	1	0	1	1	0	1	0	1	0	0	0
+6	+5.99	+0.01	0	0	0	0	0	0	0	0	0	0	1
+6	−4.24	+10.24	0	1	1	1	1	1	1	1	1	1	1

Table I. Realizable Output Codes vs. Analog Inputs with a Common Mode Voltage of +6V. Note that All Error Sources are Assumed to be Zero and V_{REF} = +5.12V.

ANALOG INPUT RANGE

With V_{REF} = +5.12V the maximum analog input voltage range is ±10.24V. The digital output data is related to the reference and differential input voltages by the following expression:

$$DATA = \frac{AIN(+) - AIN(-)}{2V_{REF}} \times 1024$$

The sign of this data is determined by the sign of AIN (+) – AIN (–).

The negative supply (V_{SS}) must be equal to or more negative than the most negative analog input signal applied to AIN+ or AIN– (pins 3 and 4).

BIPOLAR TRANSFER CHARACTERSTIC

The ideal composite transfer characteristic for the AD7571 is shown in Figure 4. The sign bit transition which ideally occurs at 0V analog input is not shown for ease of illustration.

The first LSB transition points are mirror images of each other. The effect of non-zero offset errors is to either broaden or narrow the zero code widths. The effect of non-zero Gain Error is to pivot the composite transfer characteristic around the 0V origin.

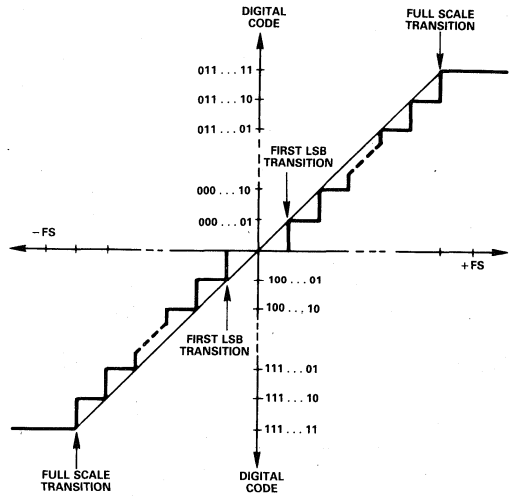


Figure 4. Composite AD7571 Transfer Characteristic

PIN	MNEMONIC	DESCRIPTION
1	V_{SS}	Negative supply 0V to –15V. V_{SS} must be equal to or more negative than the most negative analog input voltage. With positive only input signals AD7571 may be operated with V_{SS} = 0V.
2	V_{DD}	Positive supply, +15V.
3	AIN+	Positive differential input.
4	AIN–	Negative differential input.
5	V_{REF}	Voltage reference input. The AD7571 is specified with V_{REF} = +5.12V.
6	AGND	Analog ground.
7	FORM	Data format select. See pin 8 description.
8	HSEL/$\overline{LSEL}$	HIGH BYTE/$\overline{LOW\ BYTE}$ select. Used in conjunction with FORM (pin 7) to select the data output format.

FORM	HSEL/$\overline{LSEL}$	DATA OUTPUT FORMAT	ACTIVE OUTPUT PINS
0	X	SIGN + 10-BIT PARALLEL	PIN 20 (SIGN) & PINS 10–19 (DB9–DB0)
1	0	LOW BYTE (3LSBs)	PINS 17, 18 & 19 DB2, DB1 & DB0)
1	1	HIGH BYTE (SIGN + 7MSBs)	PIN 20 (SIGN) & PINS 10–16 (DB9–DB3)

X = "Don't care" state.

9	V_{CC}	Logic Supply. For V_{CC} = +5V digital inputs and outputs are TTL compatible. For V_{CC} = V_{DD} digital inputs and outputs are CMOS compatible.
10–19	DB9–DB0	DATA OUTPUT. Three state output. DB9 = MSB.
20	SIGN	SIGN BIT OUTPUT. Three state output. Sign = AIN(+) – AIN(–) and is a logic zero for positive differential inputs and logic one for negative differential inputs.
21	DGND	Digital Ground.
22	CE	CHIP ENABLE. This is an enabling signal for the AD7571. CE = 1: Normal device operation. CE = 0: All outputs are placed in high impedance state, $\overline{CS}$ and $\overline{RD}$ input activity is ignored. Conversion results, if they have not previously been read, are stored internally and can be read when device returns to normal operation.
23	$\overline{BUSY}$	$\overline{BUSY}$ indicates conversion status. Three-state output. $\overline{BUSY}$ is low during conversion. $\overline{BUSY}$ is placed into a high impedance state when CE = 0.
24	$\overline{CS}$	$\overline{CHIP\ SELECT}$. Decoded device address, used with $\overline{RD}$ (pin 25) to control conversion sequences (see operating modes).
25	$\overline{RD}$	$\overline{READ}$/WRITE control. Used with $\overline{CS}$ (pin 24) to control conversion sequences (see operating modes).
26	CLK IN	CLOCK INPUT for internal/external clock operation. Internal: Connect R_{CLK} and C_{CLK} timing components. See Figure 21 and Figure 22. External: Connect external clock via three-state buffer (see Figure 23). See section entitled "Internal/External clock".
27	CLK OUT	CLOCK OUTPUT. Three-state output. Used in conjunction with CMP OUT (pin 28) for serial data transfer. During a conversion CLK OUT frequency is CLK IN frequency divided by 4 otherwise CLK OUT is held at a logic HIGH. CLK OUT is placed into a high impedance state when CE = 0.
28	CMP OUT	COMPARATOR OUTPUT. Three-state output is used in conjunction with CLK OUT (pin 27) for serial data transfer. Output occurs during conversion and data is valid on rising edges of CLK OUT. Format is SIGN, MSB . . . . . LSB. CMP OUT is placed into a high impedance state when CE = 0.

Table II. Pin Function Description

FUNCTIONAL DESCRIPTION

The AD7571 uses the successive approximation technique to generate 10-bit plus sign conversion data. A block diagram of the device is shown previously. The comparator is a sampled data type comparator providing true differential analog inputs to allow conversion of both positive and negative input signals with a single positive reference. The comparator output drives the successive approximation register, which in turn, controls the output of the 10-bit thin-film R-2R D/A converter.

The control logic has been designed to allow easy interface to most microprocessors. Conversion start and data read are under the control of two input signals, $\overline{CS}$ ($\overline{CHIP\ SELECT}$) and $\overline{RD}$ ($\overline{READ}$/WRITE). Their timing determines the AD7571 operating mode (see Operating Modes Section). Upon receipt of a start command, $\overline{BUSY}$ goes low indicating conversion is in progress. The first decision made by the comparator concerns the sign of the differential input voltage AIN (+) – AIN (–). Based on the result of the sign decision, the comparator and its control logic then proceeds to successively approximate the differential input voltage by making differential voltage comparisons between AIN (+) – AIN (–) and the DAC output voltage V_{DAC} – AGND. Note that all comparator decisions are available at CMP OUT (pin 28) allowing serial data interfacing. To avoid misinterpretation of the serial data stream, a synchronizing signal (providing 11 rising edges) is available on CLK OUT (pin 27). Comparator output data is guaranteed valid on the rising edge of this synchronizing signal (see Operating Modes Section).

When the conversion is complete $\overline{BUSY}$ returns HIGH indicating the successive approximation register contains a valid representation of the differential analog input. This data can now be read out via the three-state data outputs. To allow easy interfacing to both 8-bit and 16-bit microprocessors, the data output format is controlled by FORM (pin 7) and HSEL/$\overline{LSEL}$ (pin 8) to provide sign plus 10-bits in parallel (one READ operation) or 3 lower bits followed by sign plus 7 upper bits (two READ operations). The internal successive approximation register is always reset after a sign plus 10-bit or sign plus 7-bit read operation (see Data Output Formats Section).

The CE input (CHIP ENABLE, pin 22) is an enabling signal for the AD7571. When CE is HIGH, normal device operation as outlined above occurs. When CE is LOW, all outputs are placed in the high impedance state and $\overline{CS}$ and $\overline{RD}$ activity is ignored. This device enabling signal allows a number of AD7571 to share common data and control lines in either serial or parallel data transfer configurations.

DATA OUTPUT FORMATS

The AD7571 has three possible data output formats, one serial and two parallel. Serial data is only available while a conversion is in progress. Parallel data, being the contents of the Successive Approximation Register, can be read before a conversion starts (ROM Mode) or after a conversion finishes (RAM and SLOW MEMORY Modes). Parallel data cannot be read during a conversion since control inputs $\overline{CS}$ and $\overline{RD}$ are ignored while $\overline{BUSY}$ is LOW.

SERIAL DATA OUTPUT FORMAT

The output of the comparator is available at CMP OUT (COMPARATOR OUTPUT, pin 28). To avoid misinterpretation of this serial output data stream, a synchronizing signal is made available at CLK OUT (CLOCK OUT, pin 27). Serial output data is valid on the rising edge of this synchronizing signal, 11 rising edges in total. The format of this output data is SIGN, DB9, DB8 . . . . . DB0. When a conversion is not taking place the CMP OUT output will continue to register activity but the CLK OUT output will be held at a logic HIGH. The CLK OUT frequency is synchronized to the converter's input clock frequency present on CLK IN (CLOCK INPUT, pin 26), but is divided by 4. Both CLK OUT and CMP OUT are placed in the high impedance state when the CE input (CHIP ENABLE, pin 22) is taken LOW. This feature allows numerous AD7571s to send digital data to a microprocessor using as few as three wires for the interconnect. Both CLK OUT and CMP OUT can drive one low power TTL load.

10-BITS PLUS SIGN FORMAT

This parallel format allows the AD7571 to interface directly to 12- and 16-bit microprocessors. It is also the more useful format in non-microprocessor based applications. This data can only be read once since an automatic internal reset occurs whenever the $\overline{RD}$ input returns HIGH regardless of the operating mode (STATIC RAM, ROM or SLOW MEMORY). This format is selected by holding the FORM input (DATA FORMAT SELECT, pin 7) at a logic LOW. When the FORM input is LOW, the Low Byte/High Byte select input (HSEL/$\overline{LSEL}$, pin 8) is ignored.

2 BYTE LEFT-JUSTIFIED FORMAT

This format has been included to allow direct interfacing to 8-bit microprocessors. The data is broken into two bytes, sign plus upper 7 bits as one byte, and lower 3 bits as the second byte. To configure a left-justified 8-bit output data bus, DB2 should be connected to SIGN, DB1 to DB9 and DB0 to DB8. This is shown in the typical circuits such as Figure 12. Two READ operations are thus required to obtain the full 10-bits plus sign data. The byte select input (HSEL/$\overline{LSEL}$) is used to select which byte of data is placed on the data bus during the next data READ operation. This input can be connected to the microprocessor's lowest address line A0, thus giving the AD7571 two effective memory addresses, one for high byte conversion data, and one for low byte conversion data. If the full 10-bits plus sign data is required, then the two bytes must be read in an ordered sequence of low byte first then high byte. This sequence is required because an automatic internal reset occurs when $\overline{RD}$ returns HIGH after reading the sign plus 7 bits of data. Reading the low byte does not cause the internal reset to occur. In applications where only sign plus 7-bit resolution is required this can be obtained by one READ operation. The conversion time is not altered as the AD7571 always completes a full 10-bits plus sign conversion regardless of the output data format requirements.

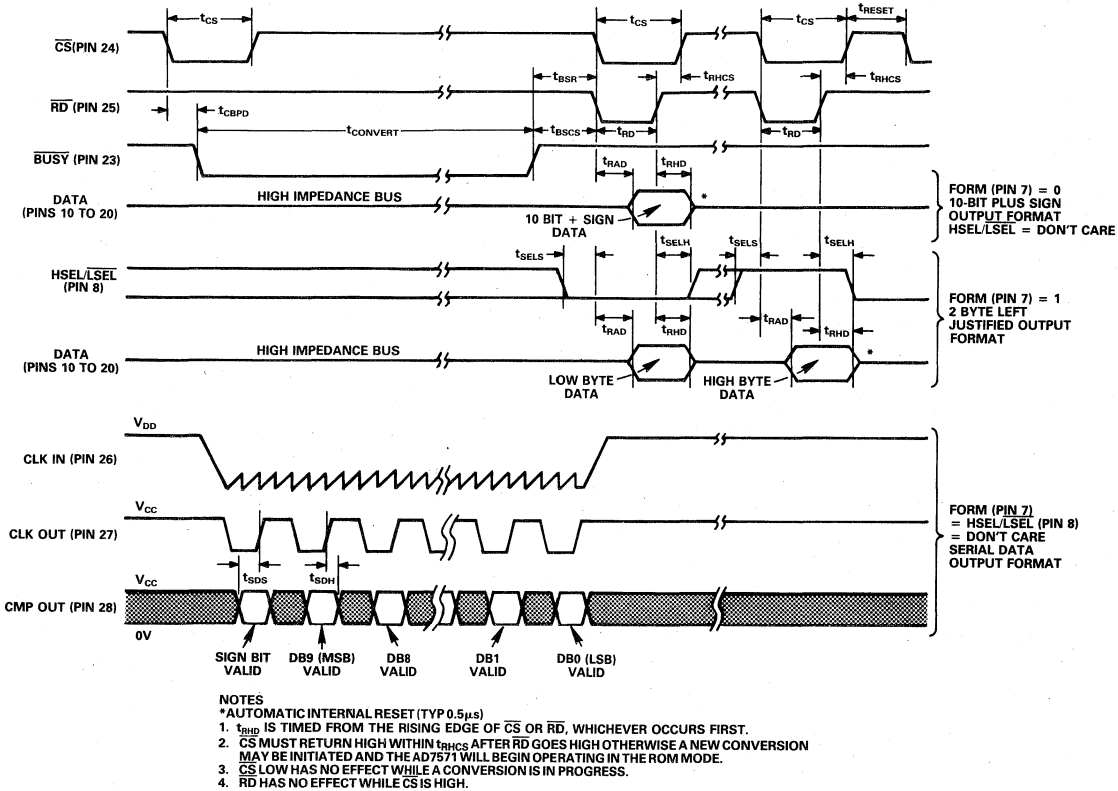


Figure 5. AD7571 Static RAM Mode Timing Diagram

OPERATING MODES

The AD7571 has been designed to interface with microprocessors as a memory mapped peripheral device. As such, its control logic allows it to mimic such standard memory systems as static RAM, ROM or SLOW MEMORY.

STATIC RAM MODE

In this mode, the AD7571 is controlled by microprocessor READ and WRITE instructions and offers complete control over the converter operation. A single WRITE instruction to the AD7571 assigned memory address commands the A/D to start a conversion and 80μs later, depending on the data format decision, either one or two READ instructions retrieves the conversion result. To operate in this mode, the AD7571 must be connected so that executing a WRITE instruction to the AD7571 address pulls the $\overline{CS}$ input LOW while $\overline{RD}$ remains HIGH. Executing a READ instruction to the AD7571 address(es) must cause both $\overline{CS}$ and $\overline{RD}$ inputs to be pulled LOW for the duration of the READ instruction. $\overline{BUSY}$ must have returned HIGH before a data READ is attempted, i.e., delay from conversion start to data READ must be at least as great as the AD7571 conversion time. Figure 5 shows the timing diagram for all output data formats. Figures 6 and 7 show typical hookup examples to 8-bit and 16-bit microprocessors respectively.

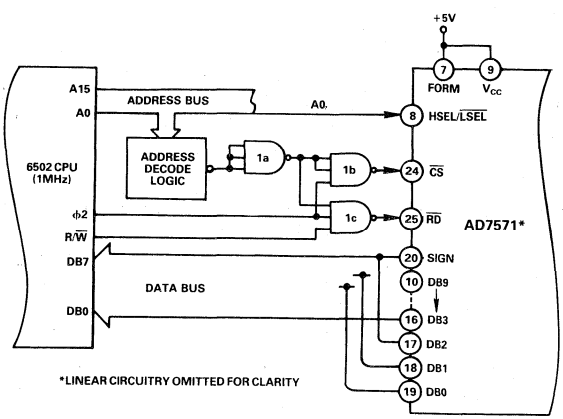


Figure 6. AD7571 to 6502 Interface, Static RAM Mode

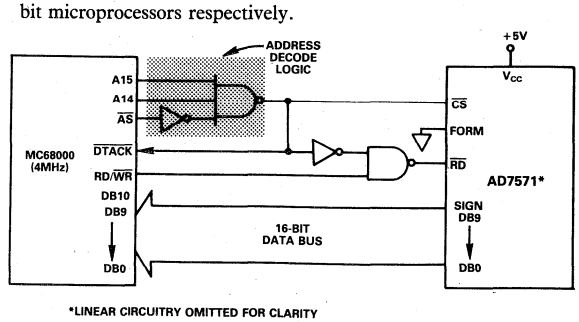


Figure 7. AD7571 to MC68000, Static RAM Mode

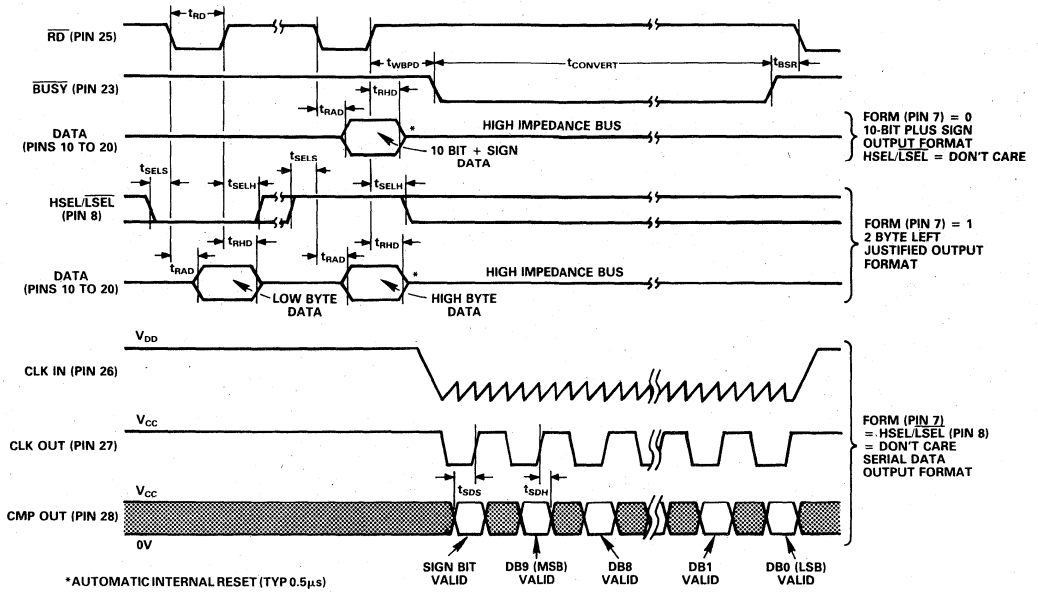


Figure 8. AD7571 ROM Mode Timing Diagram

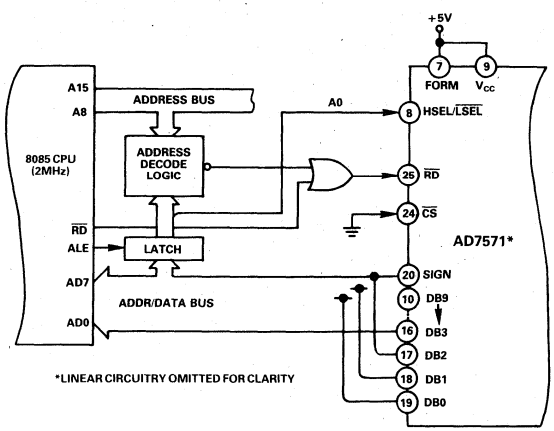


Figure 9. AD7571 to 8085 Interface, ROM Mode

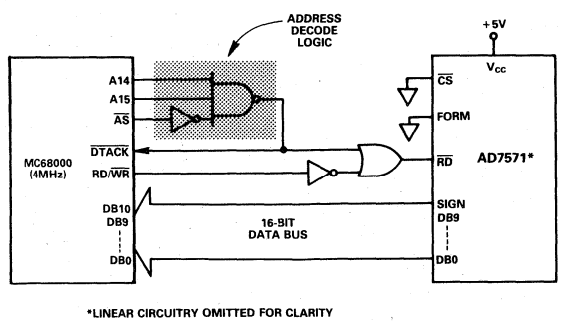


Figure 10. AD7571 to MC68000, ROM Mode

ROM MODE

This is the simplest method of interfacing the AD7571 to any microprocessor. Only READ instructions with a minimal amount of interface logic control the device's operation. This mode has the disadvantage that the time reference for the A/D conversion data is not well defined since the data read is the result of the previous conversion. This means that the time reference for the data sample will depend on when the previous READ operation finished. In applications where this uncertainty creates problems it can be eliminated by executing two complete READ operations separated by a software delay. To operate in this mode the $\overline{CS}$ input must be held LOW continuously and the $\overline{RD}$ input only pulled LOW when a READ instruction to the AD7571 memory address (es) is executed. A timing diagram is shown in Figure 8 and typical hookup examples to 8-bit and 16-bit microprocessors are shown respectively in Figures 9 and 10.

SLOW MEMORY MODE

In this mode, the normal A/D conversion time is treated as if it were the long access time of a slow memory device. It simplifies the software and can be used with any microprocessor which can be forced into a WAIT state for at least the duration of a conversion (e.g., Z80, 8085A). To operate in this mode, the AD7571 should be connected so that executing a memory READ instruction to its address causes both $\overline{CS}$ and $\overline{RD}$ inputs to be pulled low. $\overline{BUSY}$ subsequently goes LOW indicating a conversion start. Since $\overline{BUSY}$ is connected to the microprocessor READY input, the microprocessor is forced into a wait state thus suspending execution of the READ instruction. When $\overline{BUSY}$ returns HIGH (conversion finished), the microprocessor is released from the wait state to read the conversion data placed on the data bus by the AD7571. Many microprocessors test the condition of the READY/WAIT input shortly after the start of an instruction cycle. For this reason, the timing of the AD7571 and its associated address decode logic must be such that $\overline{BUSY}$ goes LOW early enough in the processor instruction cycle for the READY/WAIT input to be effective in forcing the processor into a WAIT state. In applications where the processor's memory READ/WRITE signal is not available early enough in the machine cycle for it to be used to enable or disable the address decode logic, the system software must be such that a WRITE operation to the AD7571 address(es) is never attempted, otherwise a bus conflict may occur between processor and AD7571.

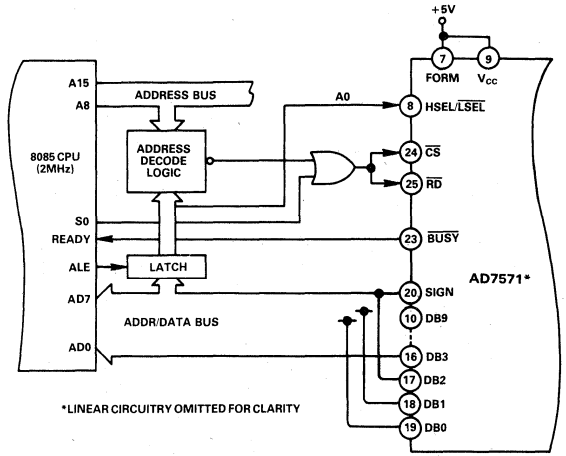


Figure 12. AD7571 to 8085 Interface Slow Memory Mode

A timing diagram for this mode is shown in Figure 11. A typical hookup example to the 8085A is shown in Figure 12.

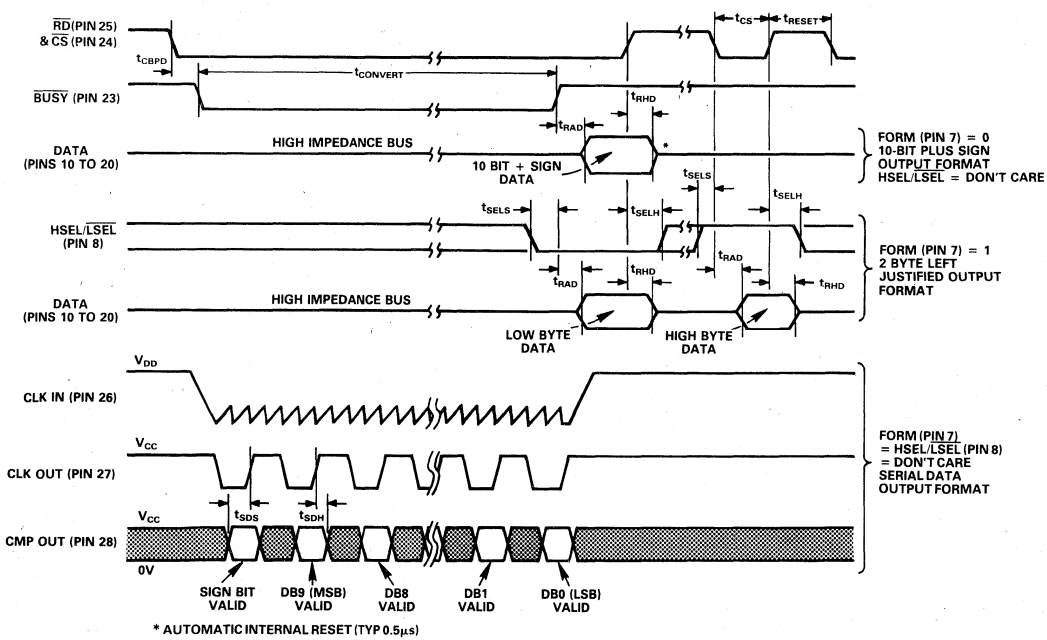


Figure 11. AD7571 Slow Memory Mode Timing Diagram

INTERNAL/EXTERNAL CLOCK

The AD7571 can be used with either its own internal asynchronous clock or with an externally applied clock. Whichever clock source is used, a single conversion ($\overline{BUSY}$ = LOW) lasts for 44 input clock cycles. Internal logic propagation delays add less than 0.5μs to this time.

INTERNAL CLOCK

A simplified equivalent circuit for the AD7571 internal clock circuitry is shown in Figure 13.

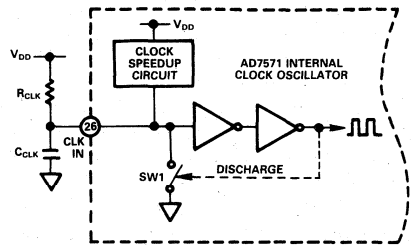


Figure 13. Simplified AD7571 Internal Clock Circuit

Clock pulses are generated by the action of an external capacitor C_{CLK} charging through an external resistor R_{CLK} and discharging through switch SW1. The clock speedup circuit acts to shorten the last clock period of a conversion. When a conversion is complete, the internal clock stops operation. However, in addition to conversion the internal clock also controls the automatic internal reset. For this reset operation, the internal clock runs for one cycle. Reset occurrences are indicated by asterisks in Figures 5, 8 and 11.

Nominal conversion times versus temperature for different R_{CLK} and C_{CLK} combinations are shown in Figure 14. The internal clock is useful in that it provides a convenient clock source for the AD7571. Due to process variations the actual operating frequency for a given R_{CLK} and C_{CLK} combination can vary from device to device by up to 10%. For this reason Analog Devices recommends using an external clock in the following situations.

1. Applications requiring a conversion time which is within 10% of 80μs, the minimum conversion time for specified accuracy. (A 550kHz clock frequency gives an 80μs conversion time.)
2. Applications where software constraints on time cannot accommodate time differences which may occur due to unit to unit clock frequency variations or temperature variations.

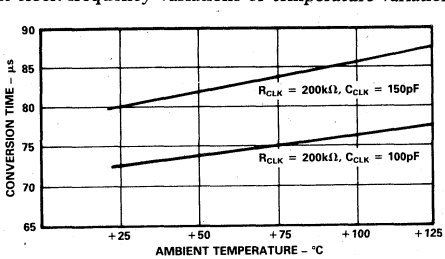


Figure 14. Typical Conversion Times vs. Temperature for Different R_{CLK} and C_{CLK}

EXTERNAL CLOCK

Due to the automatic internal reset cycle of the AD7571 the external clock source used to drive the CLK IN input must be capable of three-state operation. Figure 15 shows how the external clock (TTL compatible) should be connected. The $\overline{BUSY}$ output of the AD7571 controls the three-state enable input of a CD40109B three-state buffer. R1 is used as a pullup resistor and can be any value between 6kΩ and 100kΩ. The reset timing is still performed by the converter's internal logic and does not require an external clock pulse. The CD40109B also functions as a low-to-high voltage level shifter since the CLK IN input is not TTL compatible.

If a high level clock is already available, then an MC14503B three-state buffer can be used. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

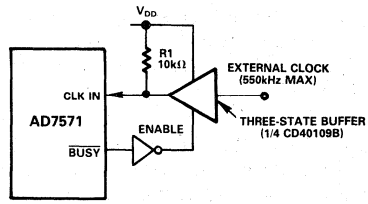


Figure 15. External Clock Connection

The AD7571 can be used with an external clock when configured in either the STATIC RAM or SLOW MEMORY modes, but is not recommended in the ROM mode. This is because the internal reset timing in this mode occurs after a conversion start command but before $\overline{BUSY}$ goes LOW (t_{WBPD} of Figure 8). With an external clock, it is possible for the comparator to have insufficient settling time before making the SIGN decision.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE: When initiating a conversion, $\overline{CS}$ should go LOW on a negative clock edge to provide optimum settling time for the MSB.

SLOW MEMORY MODE: When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a negative clock edge to provide optimum settling time for the MSB.

10

APPLICATION HINTS

1. INPUT CURRENT: Due to the internal comparator switching action, displacement currents will flow at the analog inputs. The magnitude and polarity of these displacement currents will depend upon the differential analog input voltage levels.

   The effect of placing bypass capacitors at the analog inputs is to integrate the transient currents over the switching cycle. This causes a dc current to flow through any output resistance of the analog signal sources, thereby causing an input error. This dc current has a maximum value under conditions of continuous conversions with an input clock frequency of 550kHz and a differential input voltage of 10.24V. Under these conditions the dc current is a maximum of approximately 25μA. Therefore, to ensure that the input error will remain less than 1/4LSB, bypass capacitors should not be used at either the analog inputs or the V_{REF} input for source resistances greater than 100Ω. Where bypass capacitors are not used, large values of source resistance will not cause errors as the transient input currents have reduced to zero by the time data is accepted from the comparator. If it is necessary to filter the incoming analog signals through a low pass filter, use a passive RC low pass filter with series R < 100Ω or else an active RC low pass filter. If input bypass capacitors are necessary for noise filtering and high source resistance is unavoidable, the input error can be compensated for by a full scale adjustment while the given source resistance and bypass capacitor are in place.

2. NOISE: The leads to the analog inputs (pins 3 and 4) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a twisted pair transmission line between source and ADC is recommended. The twisted pair keeps induced noise (due to capacitive and inductive coupling) to a minimum. Also any potential difference in grounds between signal source and ADC appears as a common mode voltage to the ADC's differential inputs. In general, the source resistance should be kept below 2kΩ. Large values of bypass capacitors will eliminate this system noise pickup, but will also introduce input scaling errors as outlined in the previous section.
3. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog signal lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both analog inputs and the reference input should be screened by AGND. A single point analog ground which is separate from the logic ground system should be established at or near the AD7571. This single point analog ground subsystem should be connected to the digital ground system by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

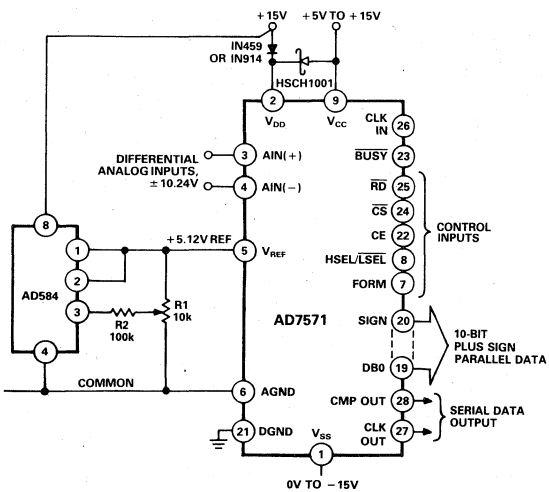


Figure 16. AD7571 Operational Diagram (see Table I for Pin Function Description)

4. OFFSET ERROR: For either positive or negative differential inputs, the procedure for adjusting the input offset error to zero is similar. The circuit for zero offset adjust is shown connected to the AIN(−) input which is assumed to be at some common mode voltage V_{CM}. For positive differential inputs the AIN(+) input is forced to V_{CM} + 10mV (V_{CM} + 1LSB) while the potentiometer is adjusted until the ADC output code flickers between 000 . . . . 00 and 000 . . . . 01. For negative differential inputs the AIN(+) input is forced to V_{CM} − 10mV (V_{CM} − 1LSB) while the potentiometer is adjusted until the ADC output code flickers between 100 . . . . 00 and 100 . . . . 01.

   In applications where the differential input voltage can swing both positive and negative no offset adjust is required since the offset errors for both positive and negative differential inputs are already mirror images of each other due to the architecture of the AD7571.

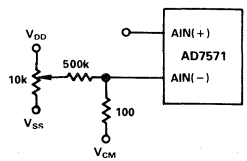


Figure 17. Zero Offset Adjust Circuit

5. FULL-SCALE ADJUST: The full-scale adjustment is made by applying a positive or negative differential input voltage to the analog inputs which is 1LSB down from the required positive or negative analog full scale range. The magnitude of the reference voltage V_{REF} is then adjusted until the ADC output code flickers between 011 . . . . 10 and 011 . . . . 11 for a positive differential input or between 111 . . . . 10 and 111 . . . . 11 for a negative differential input.
6. SUPPLY SEQUENCING: Do not allow V_{CC} to exceed V_{DD}. In cases where V_{CC} could exceed V_{DD}, the diode protection scheme shown in Figure 16 is recommended.

ANALOG DEVICES

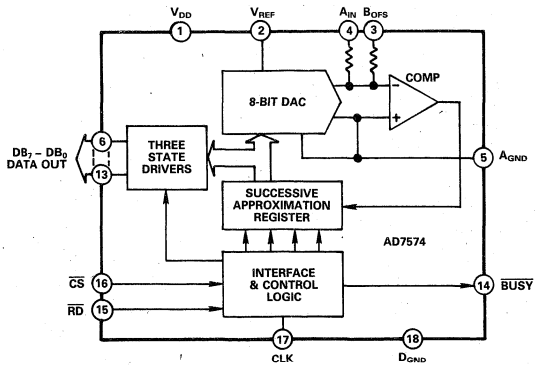
CMOS µP-Compatible 8-Bit ADC

AD7574

FEATURES

8-Bit Resolution
No Missed Codes over Full Temperature Range
Fast Conversion Time: 15µs
Interfaces to µP like RAM, ROM or Slow - Memory
Low Power Dissipation: 30mW
Ratiometric Capability
Single +5V Supply
Low Cost
Internal Comparator and Clock Oscillator

AD7574 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

AD7574 is a low-cost, 8-bit µP compatible ADC which uses the successive-approximations technique to provide a conversion time of 15µs.

Designed to be operated as a memory mapped input device, the AD7574 can be interfaced like static RAM, ROM, or slow memory. It's $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ}/\overline{WRITE}$ control) inputs are available in all µP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the µP data bus or system input port.

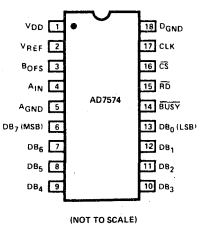
Internal clock, +5V operation, on-board comparator and interface logic, as well as low power dissipation (30mW) and fast conversion time make the AD7574 ideal for most ADC/µP interface applications. Small size (18-pin DIP) and monolithic reliability will find wide use in avionics, instrumentation, and process automation applications.

ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package[1]		
	Plastic (N18B) 0 to +70°C	Ceramic (D18B) -25°C to +85°C	Ceramic (D18B) -55°C to +125°C
±7/8LSB	AD7574JN	AD7574AD	AD7574SD
±3/4LSB	AD7574KN	AD7574BD	AD7574TD

[1] See Section 19 for package outline information.

PIN CONFIGURATION



(NOT TO SCALE)

18-PIN DIP
TOP VIEW

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N18B)
Suffix "D" – Ceramic DIP (D18B)

[1] See Section 19 for package outline information.

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CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Configuration, R_{CLK} = 180kΩ, C_{CLK} = 100pF, unless otherwise noted)

PARAMETER	LIMITS T_A = +25°C	LIMITS T_{min}, T_{max}[1]	UNITS	CONDITIONS/COMMENTS
ACCURACY				
Resolution	8	8	Bits	
Relative Accuracy Error				
AD7574JN, AD, SD	±¾	±¾	LSB max	
AD7574KN, BD, TD	±½	±½	LSB max	Relative Accuracy and Differential Nonlinearity are measured dynamically using the external clock circuit of Fig. 7b.
Differential Nonlinearity				
AD7574JN, AD, SD	±⅞	±⅞	LSB max	Clock frequency is 500kHz (conversion time 15μs)
AD7574KN, BD, TD	±¾	±¾	LSB max	
Full Scale Error (Gain Error)				Full Scale Error is measured after calibrating out offset error. See
AD7574JN, AD, SD	±5	±6.5	LSB max	Fig. 8a and associated calibration procedure for offset. Max Full
AD7574KN, BD, TD	±3	±4.5	LSB max	Scale change from +25°C to T_{min} or T_{max} is ±2 LSB.
Offset Error[2]				
AD7574JN, AD, SD	±60	±80	mV max	Maximum Offset change from +25°C to
AD7574KN, BD, TD	±30	±50	mV max	T_{min} or T_{max} is ±20mV.
Mismatch Between B_{OFS} (pin 3) and A_{IN} (pin 4) Resistances[3]	±1.5	±1.5	%	
ANALOG INPUTS				
Input Resistance				
At V_{REF} (pin 2)	5/10/15	5/10/15	kΩ min/typ/max	
At B_{OFS} (pin 3)	10/20/30	10/20/30	kΩ min/typ/max	
At A_{IN} (pin 4)	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (for specified performance)	-10	-10	V	±5% for specified transfer accuracy.
V_{REF} Range[4]	-5 to -15	-5 to -15	V	Degraded transfer accuracy.
Nominal Analog Input Range				
Unipolar Mode	0 to +$\|V_{REF}\|$		V	
Bipolar Mode	-$\|V_{REF}\|$ to +$\|V_{REF}\|$		V	
LOGIC INPUTS				
$\overline{RD}$ (pin 15), $\overline{CS}$ (pin 16)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.8	+0.8	V max	
I_{IN} Input Current	1	10	μA max	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	5	5	pF max	
CLK (pin 17)				
V_{INH} Logic HIGH Input Voltage	+3.0	+3.0	V min	
V_{INL} Logic LOW Input Voltage	+0.4	+0.4	V max	
I_{INH} Logic HIGH Input Current	+2	+2	mA max	During Conversion: $V_{IN(CLK)} \geq V_{INH(CLK)}$
I_{INL} Logic LOW Input Current	1	10	μA max	During Conversion: $V_{IN(CLK)} \leq V_{INL(CLK)}$ (see circuit of Fig. 7b if external clock operation is required).
LOGIC OUTPUTS				
BUSY (pin 14), DB_7 to DB_0 (pins 6-13)				
V_{OH} Output HIGH Voltage	+4.0	+4.0	V min	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	+0.4	+0.8	V max	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating Stage Leakage	1	10	μA max	V_{OUT} = 0V or V_{DD}
Floating State Output Capacitance (DB_7 to DB_0)[5]	7	7	pF max	
Output Code	Unipolar Binary, Offset Binary			See Figs. 8a, 9a, 10a and 8b, 9b, 10b.
POWER REQUIREMENTS				
V_{DD}	+5	+5	V	±5% for specified performance.
I_{DD} (STANDBY)	5	5	mA max	A_{IN} = 0V, ADC in RESET condition.
I_{REF}	V_{REF} divided by 5kΩ		max	Conversion complete, prior to RESET.

NOTES
[1] Temperature ranges as follows: JN, KN (0 to +70°C)
AD, BD (-25°C to +85°C)
SD, TD (-55°C to +125°C)
[2] Typical offset temperature coefficient is ±150μV/°C.
[3] R_{BOFS}/R_{AIN} mismatch causes transfer function rotation about positive Full Scale. The effect is an offset and a gain term when using the circuit of Figure 9a.
[4] Typical value, not guaranteed or subject to test.
[5] Guaranteed but not tested.

Specifications subject to change without notice.

(V_{DD} = +5V, C_{CLK} = 100pF, R_{CLK} = 180kΩ unless otherwise noted)

SYMBOL	SPECIFICATION	LIMIT at $T_A = +25°C$	LIMIT at $T_A = T_{min}$	LIMIT at $T_A = T_{max}$	CONDITIONS
STATIC RAM INTERFACE MODE (See Figure 1 and Table I)					
t_{CS}	$\overline{CS}$ Pulse Width Requirement	100ns min	150ns min	150ns min	
t_{WSCS}	$\overline{RD}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	90ns typ 120ns max	70ns typ 120ns max	150ns typ 180ns max	$\overline{BUSY}$ Load = 20pF
		120ns typ 150ns max	100ns typ 150ns max	180ns typ 200ns max	$\overline{BUSY}$ Load = 100pF
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ Setup Time	0 min	0 min	0 min	
t_{BSCS}	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0 min	0 min	0 min	
t_{RAD}	Data Access Time	120ns typ 150ns max	100ns typ 150ns max	180ns typ 220ns max	DB_0 - DB_7 Load = 20pF
		240ns typ 300ns max	220ns typ 300ns max	300ns typ 400ns max	DB_0 - DB_7 Load = 100pF
t_{RHD}	Data Hold Time	80ns typ 50ns min 120ns max	40ns typ 30ns min 80ns max	120ns typ 80ns min 180ns max	
t_{RHCS}	$\overline{CS}$ to $\overline{RD}$ Hold Time	250ns max	200ns max	500ns max	
t_{RESET}	Reset Time Requirement	3μs min	3μs min	3μs min	
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a			
$t_{CONVERT}$	Conversion Time using external clock	15μs	15μs	15μs	f_{CLK} = 500kHz circuit of Figure 7b
ROM INTERFACE MODE (See Figure 2 and Table II)					
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
t_{WBPD}	$\overline{RD}$ HIGH to $\overline{BUSY}$ Propagation Delay	400ns typ 1.5μs max	350ns typ 1.0μs max	1μs typ 2.0μs max	$\overline{BUSY}$ Load = 20pF
t_{BSR}	$\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time	$\overline{RD}$ can go LOW prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. See Table II.			
$t_{CONVERT}$	Conversion Time using internal clock oscillator	See typical data of Figure 7a. Add 2μs to data shown in Figure 7a for ROM Mode			
SLOW – MEMORY INTERFACE MODE (See Figure 3 and Table III)					
t_{CBPD}	$\overline{CS}$ to $\overline{BUSY}$ Propagation Delay	Same as RAM Mode			
t_{RESET}	Reset Time Requirement	Same as RAM Mode			
t_{RAD}	Data Access Time	Same as RAM Mode			
t_{RHD}	Data Hold Time	Same as RAM Mode			
$t_{CONVERT}$	Conversion Time	Same as RAM Mode			

ABSOLUTE MAXIMUM RATINGS

V_{DD} to A_{GND} . . . . . 0V, +7.0V
V_{DD} to D_{GND} . . . . . 0V, +7.0V
A_{GND} to D_{GND} . . . . . -0.3V, V_{DD}
Digital Input Voltage to D_{GND}
(pins 15 and 16) . . . . . -0.3V, +15.0V
Digital Output Voltage to D_{GND}
(pins 6 - 14) . . . . . -0.3V, V_{DD}
CLK Input Voltage (pin 17) to D_{GND} . . . . . -0.3V, V_{DD}
V_{REF} (pin 2) . . . . . ±20V
V_{BOFS} (pin 3) . . . . . ±20V
V_{AIN} (pin 4) . . . . . ±20V

Operating Temperature Range
JN, KN . . . . . .0°C to +70°C
AD, BD . . . . . -25°C to +85°C
SD, TD . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 secs.) . . . . . +300°C
Power Dissipation (Package)
Plastic (suffix N)
to +70°C 670mW
Derate above +70°C by . . . . . 8.3mw/°C
Ceramic (suffix D)
to +75°C 450mW
Derate above +75°C by . . . . . 6mW/°C

TERMINOLOGY

RESOLUTION: Resolution is a measure of the *nominal* analog change required for a 1-bit change in the A/D converter's digital output. While normally expressed in a number of bits, the analog resolution of an n-bit unipolar A/D converter is $(2^{-n})(V_{REF})$. Thus the AD7574, an 8-bit A/D converter, can resolve analog voltages as small as $(1/256)(V_{REF})$ when operated in a unipolar mode. When operated in a bipolar mode, the resolution is $(1/128)(V_{REF})$. Resolution does not imply accuracy. *Usable* resolution is limited by the differential nonlinearity of the A/D converter.

RELATIVE ACCURACY: Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the device's measured zero and measured full scale transition points. Relative accuracy, therefore, is a measure of code *position*.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity in an ADC is a measure of the size of an analog voltage range associated with any digital output code. As such differential nonlinearity specifies code width (usable resolution). An ADC with a specified differential nonlinearity of ±n bits will exhibit codes ranging in width from 1LSB - nLSB to 1LSB + nLSB. A specified differential nonlinearity of less than ±1LSB guarantees no-missing-codes operation.

STATIC RAM INTERFACE MODE

Table I and Figure 1 show the truth table and timing requirements for AD7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the AD7574 (once conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the AD7574 address location.

$\overline{BUSY}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the AD7574 conversion time. The delay can be generated by inserting NOP instructions (or other program instructions) between the WRITE (start convert) and READ (read data) operations. Once $\overline{BUSY}$ is HIGH (conversion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the AD7574. The data readout is destructive, i.e. when RD returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ *and* a conversion restart.

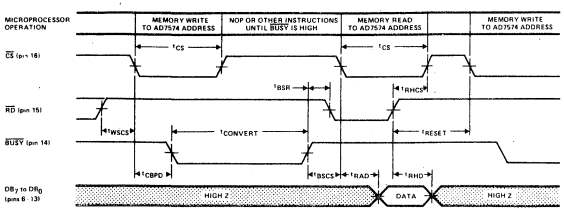


Figure 1. Static RAM Mode Timing Diagram

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB_7 - DB_0	
L	H	H	HIGH Z	WRITE CYCLE (START CONVERT)
L	⌐¬	H	HIGH Z → DATA	READ CYCLE (DATA READ)
L	¬⌐	H	DATA → HIGH Z	RESET CONVERTER
H	X[1]	X	HIGH Z	NOT SELECTED
L	H	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	⌐¬	L	HIGH Z	NO EFFECT, CONVERTER BUSY
L	¬⌐	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Note 1: If $\overline{RD}$ goes LOW to HIGH when $\overline{CS}$ is LOW, the ADC is internally reset. $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH. See application hint No. 1.

Table I. Truth Table, Static RAM Mode

ROM INTERFACE MODE

Table II and Figure 2 show the truth table and timing requirements for interfacing the AD7574 like Read Only Memory.

$\overline{CS}$ is held LOW and converter operation is controlled by the $\overline{RD}$ input. The AD7574 $\overline{RD}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the AD7574 address location. The converter is automatically restarted when $\overline{RD}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{BUSY}$ is HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is relatively poorly defined in time inasmuch as executing a data READ automatically starts a new conversion. This problem can be overcome by executing two READs separated by NO-OPS (or other program instructions) and using only the data obtained from the second READ.

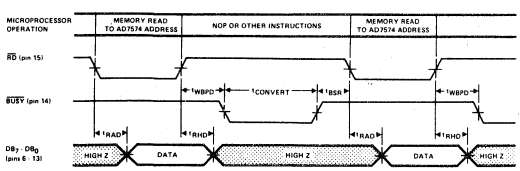


Figure 2. ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)

AD7574 INPUTS		AD7574 OUTPUTS		AD7574 OPERATION
$\overline{CS}$	$\overline{RD}$	$\overline{BUSY}$	DB_7 - DB_0	
L	⌐¬	H	HIGH Z → DATA	DATA READ
L	¬⌐	⌐¬	DATA → HIGH Z	RESET AND START NEW CONVERSION
L	⌐¬	L	HIGH Z	NO EFFECT; CONVERTER BUSY
L	¬⌐	L	HIGH Z	NOT ALLOWED, CAUSES INCORRECT CONVERSION

Table II. Truth Table, ROM Mode

SLOW-MEMORY INTERFACE MODE

Table III and Figure 3 show the truth table and timing requirements for interfacing the AD7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{CS}$ and $\overline{RD}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the AD7574 $\overline{CS}$ and $\overline{RD}$ inputs. $\overline{BUSY}$ is connected to the microprocessor READY input.

When the AD7574 is NOT addressed, the $\overline{CS}$ and $\overline{RD}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the AD7574 address. $\overline{BUSY}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{BUSY}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

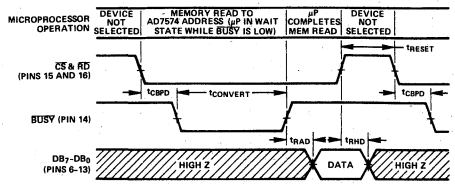


Figure 3. Slow Memory Mode Timing Diagram (CS and RD Tied Together)

AD7574 INPUTS	AD7574 OUTPUTS		AD7574 OPERATION
CS & RD	BUSY	DB_7 - DB_0	
H	H	HIGH Z	NOT SELECTED
⎍	H → L	HIGH Z	START CONVERSION
L	L	HIGH Z	CONVERSION IN PROGRESS, μP IN WAIT STATE
L	⎍	HIGH Z → DATA	CONVERSION COMPLETE, μP READS DATA
⎍	H	DATA → HIGH Z	CONVERTER RESET AND DESELECTED
H	H	HIGH Z	NOT SELECTED

Table III. Truth Table, Slow Memory Mode

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7574 uses the successive approximations technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a -10V reference, and +5V power.

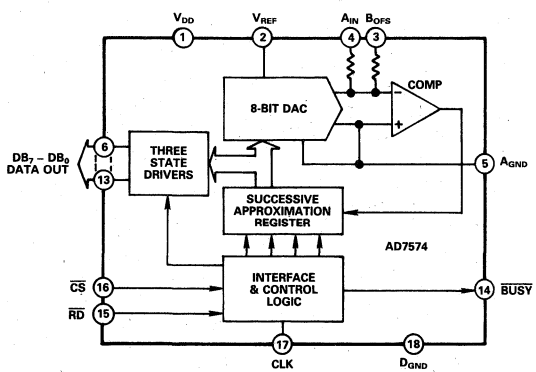


Figure 4. AD7574 Functional Diagram

Figure 4 shows the AD7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins for Control Logic and Timing Details), $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, A_{IN}. If the sum of the DAC bits is less than A_{IN}, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than A_{IN}, the trial bit is turned OFF and the next smaller bit is tried.

Each successively smaller bit is tried and compared to A_{IN} in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the DB_0 - DB_7 data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

10

DAC CIRCUIT DETAILS

The current weighting D/A converter is a precision multiplying DAC. Figure 5 shows the functional diagram of the DAC as used in the AD7574. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

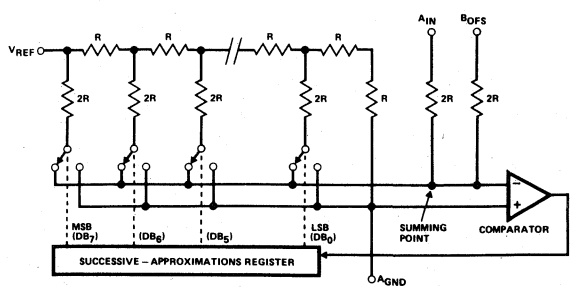


Figure 5. D/A Converter As Used In AD7574

OPERATING THE AD7574

APPLICATION HINTS

1. TIMING & CONTROL
   In the AD7574 when a conversion is finished the fresh data must be read before a new conversion can be started.
   Failure to observe the timing restrictions of Figures 1, 2 or 3 may cause the AD7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).
2. LOGIC DEGLITCHING IN uP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert starts, reads, or resets. The best way to avoid glitches is to gate the address decoding logic with RD or WR (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow-memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.
3. INPUT LOADING AT V_{REF}, A_{IN} AND B_{OFS}
   To prevent loading errors due to the finite input resistance at the V_{REF}, A_{IN} or B_{OFS} pins, low impedance driving sources must be used (i.e. op amp buffers or low output-Z reference).
4. RATIOMETRIC OPERATION
   Ratiometric performance is inherent to A/D converters such as the AD7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than -10V in magnitude.
5. OFFSET CORRECTION
   Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the AD7574 A_{IN} pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between V_{DD} and V_{REF} and applying the tap voltage to the amplifier's positive input (an example of a resistive tap offset adjust is shown in Figure 10a where R_8, R_9 and R_{10} can be used to offset the ADC).
6. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7574. In systems where the A_{GND}-D_{GND} intertie is not local, connect back-to-back diodes (IN914 or equivalent) between the AD7574 A_{GND} and D_{GND} pins.
7. INITIALIZATION AFTER POWER – UP
   Execute a memory READ to the AD7574 address location, and subsequently ignore the data. The AD7574 is internally reset when reading out data, i.e. the data readout is destructive.

CLOCK OSCILLATOR

The AD7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and ceases oscillating when conversion is complete.

The clock oscillator requires an external R and C as shown in Figure 6. Nominal conversion times versus R_{CLK} and C_{CLK} is shown in Figure 7a. The curves shown in Figure 7a are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2μs to the typical conversion time values shown.

The AD7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 15μs, as indicated by the unshaded region of Figure 7a. Conversion times faster than 15μs can cause transfer accuracy degradation.

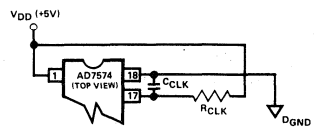


Figure 6. Connecting R_{CLK} and C_{CLK} To CLK Oscillator

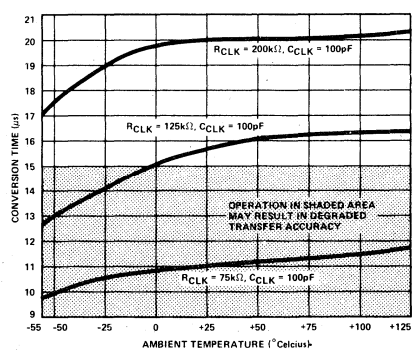


Figure 7a. Typical Conversion Time vs. Temperature For Different R_{CLK} and C_{CLK} (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2μs to values shown)

OPERATION WITH EXTERNAL CLOCK

For applications requiring a conversion time close to or equal to 15μs, an external clock is recommended. Using an external clock precludes the possibility of converting faster than 15μs (which can cause transfer accuracy degradation) due to temperature drift – as may be the case when using the internal clock oscillator.

Figure 7b shows how the external clock must be connected. The $\overline{BUSY}$ output of the AD7574 is connected to the three-state enable input of a 74125 three-state buffer. R_1 is used as a pullup, and can be between 6kΩ and 100kΩ. A 500kHz clock will provide a conversion time of 15μs.

The external clock should be used only in the static-RAM or slow-memory interface mode, and *not* in the ROM mode.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after $\overline{BUSY}$ = 1.

SLOW-MEMORY MODE

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

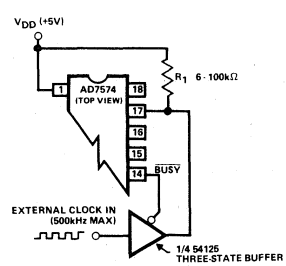


Figure 7b. External Clock Operation (Static RAM and Slow-Memory Mode)

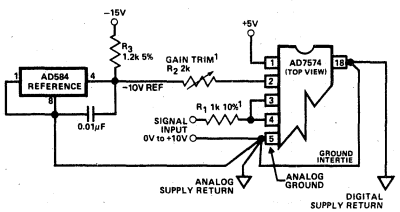
UNIPOLAR BINARY OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar operation. An AD584 is used as the -10V reference.

Calibration is as follows:

OFFSET

Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminals shown in Figure 8a. An example of an offset trim is shown in Figure 10a, where R_8, R_9 and R_{10} comprise a simple voltage tap which is applied to the amplifier's positive input.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

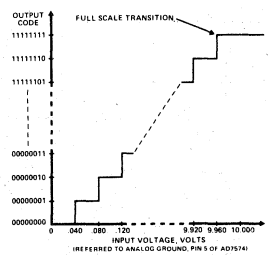
Figure 8a. AD7574 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive R_1 (i.e. +39.1mV at R_1).
2. While performing continuous conversions, adjust the offset potentiometer (described above) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

Offset adjustment must be performed before gain adjustment.

1. Apply -9.961V to the input of the buffer amplifier used to drive R_1 (i.e. +9.961V at R_1).
2. While performing continuous conversions, adjust trim pot R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for a -10V reference is ≈ 39.1mV

Figure 8b. Nominal Transfer Characteristic For Unipolar Circuit of Figure 8a

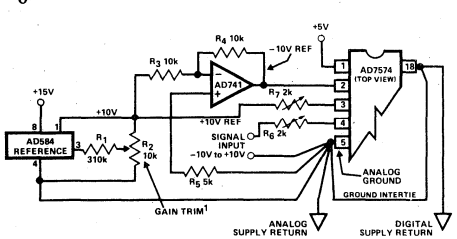
10

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of Figure 9a (Resistors R_8, R_9 and R_{10} in Figure 10a show how offset trim can be done at the buffer amplifier).

Calibration is as follows:

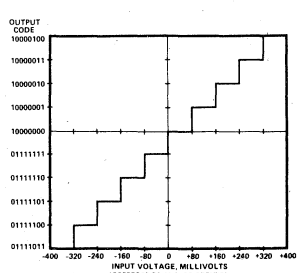
1. Adjust R_6 and R_7 for minimum resistance across the potentiometers.
2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at R_6).
3. While performing continuous conversions, trim R_6 or R_7 (whichever required) until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.



Note 1: R_1 and R_2 can be omitted if gain trim is not required

Figure 9a. AD7574 Bipolar (-10V to +10V) Operation (Output Code is Offset Binary)

4. Apply 0V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to R_6).
7. Doing continuous conversions, trim R_2 until DB_7 - DB_1 are LOW and the LSB (DB_0) flickers.
8. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of R_6).
9. If the ADC output code is not 11111110 ±1 bit, repeat the calibration procedure.



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ± 10V full scale is ≈ 78.1mV

Figure 9b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

OPERATING THE AD7574

BIPOLAR (COMPLEMENTARY OFFSET BINARY) OPERATION

Figure 10a shows the analog connections for complementary offset binary operation. The typical transfer characteristic is shown in Figure 10b. In this bipolar mode, the ADC is fooled into believing it is operated in a unipolar mode - i.e. the +10V to −10V analog input is conditioned into a 0 to +10V signal range. R_2 is the gain adjust, while R_9 is the offset adjust.

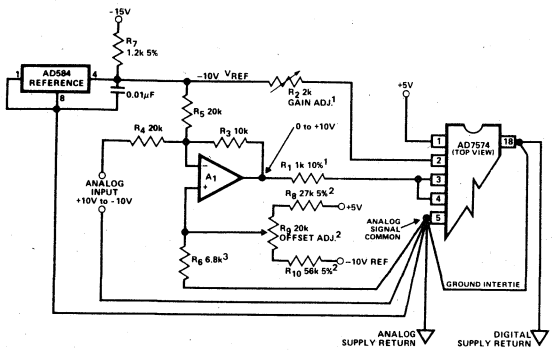
Calibration is as follows (adjust offset before gain):

OFFSET

1. Apply OV to the analog input shown in Figure 10a.
2. While performing continuous conversions, adjust R_9 until the converter output flickers between codes 01111111 and 10000000.

GAIN (FULL SCALE)

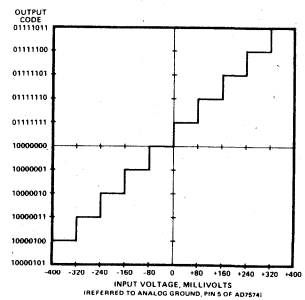
1. Apply −9.922V across the analog input terminals shown in Figure 10a.
2. While performing continuous conversions, adjust R_2 until DB_7 - DB_1 are HIGH and the LSB (DB_0) flickers between HIGH and LOW.



Notes:

1. R_1 and R_2 can be omitted if gain trim is not required
2. R_8, R_9 and R_{10} can be omitted if offset trim is not required
3. $R_6 \| R_8 \| R_{10} = 5k\Omega$. If R_8, R_9 and R_{10} not used, make $R_6 = 5k\Omega$

Figure 10a. AD7574 Bipolar Operation (-10V to +10V) (Output Code is Complementary Offset Binary)



Note: Approximate bit weights are shown for illustration. Nominal bit weight for ±10V full scale is ≈ 78.1mV

Figure 10b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10a

ANALOG DEVICES

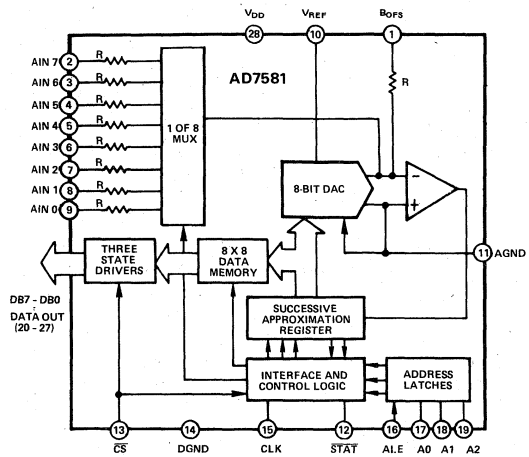
CMOS μP-Compatible 8-Bit 8-Channel DAS

AD7581

FEATURES

- 8-Bit Resolution
- On-Chip 8 X 8 Dual-Port Memory
- No Missed Codes Over Full Temperature Range
- Interfaces Directly to Z80/8085/6800
- CMOS, TTL Compatible Digital Inputs
- Three-State Data Drivers
- Ratiometric Capability
- Interleaved DMA Operation
- Fast Conversion
- A/D Process Totally Transparent to μP
- Low Cost

AD7581 FUNCTIONAL BLOCK DIAGRAM

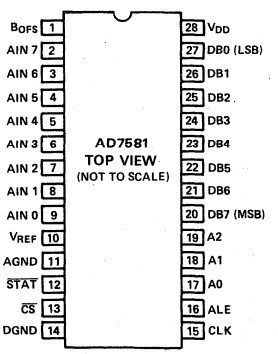


GENERAL DESCRIPTION

The AD7581 is a microprocessor compatible 8 bit, 8 channel, memory buffered, data-acquisition system on a monolithic CMOS chip. It consists of an 8 bit successive approximation A/D converter, an 8 channel multiplexer, 8 X 8 dual-port RAM, three-state DATA drivers (for interface), address latches and microprocessor compatible control logic. The device interfaces directly to 8080, 8085, Z80, 6800 and other microprocessor systems.

The successive approximation conversion takes place on a continuous, channel sequencing, basis using microprocessor control signals for the clock. Data is automatically transferred to its proper location in the 8 X 8 dual-port RAM at the end of each conversion. When under microprocessor control, a READ DATA operation is allowed at any time for any channel since on-chip logic provides interleaved DMA. The facility to latch the address inputs (A_0 - A_2) with ALE enables the AD7581 to interface with μP systems which feature either shared or separate address and data buses.

PIN CONFIGURATION



ORDERING INFORMATION

Differential Nonlinearity	Temperature Range and Package: Plastic 0 to +70°C	Temperature Range and Package: Ceramic -25°C to +85°C
±1 7/8LSB	AD7581JN	AD7581AD
±7/8LSB	AD7581KN	AD7581BD
±3/4LSB	AD7581LN	AD7581CD

PACKAGE IDENTIFICATION[1]

Suffix "N" – Plastic DIP (N28A)
Suffix "D" – Ceramic DIP (D28B)

[1] See Section 19 for package outline information.

10

DC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Operation, unless otherwise stated)

Parameter	Version[1]	Typical at +25°C	Limit Over Temperature	Units	Conditions/Comments
ACCURACY					
Resolution	All	8	8	Bits	
Relative Accuracy	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±3/4	±3/4 max	LSB	
	LN, CD	±1/2	±1/2 max	LSB	
Differential Nonlinearity	JN, AD	±1 7/8	±1 7/8 max	LSB	
	KN, BD	±7/8	±7/8 max	LSB	
	LN, CD	±3/4	±3/4 max	LSB	
Offset Error[2]	JN, AD	200	200 max	mV	Adjustable to zero, see Figure 7a.
	KN, BD	80	80 max	mV	
	LN, CD	50	50 max	mV	
Gain Error					
Worst Channel	JN, AD	±3	±6 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	±2	±4 max	LSB	Gain Error is Measured After Offset
	LN, CD	±1	±2 max	LSB	Calibration. Max Full Scale Change for Any Channel from +25°C to T_{min} or T_{max} is ±2LSB.
Gain Match Between Channels	JN, AD	2	3 max	LSB	Adjustable to zero, see Figure 7a.
	KN, BD	1 1/2	2 max	LSB	
	LN, CD	1	1 max	LSB	
B_{OFS} Gain Error	All	-2 1/2	–	LSB	
ANALOG INPUTS					
Input Resistance					
At V_{REF} (pin 10)	All	10/20/30	10/20/30	kΩ min/typ/max	
At B_{OFS} (pin 1)[3]	All	10/20/30	10/20/30	kΩ min/typ/max	
At Any Analog Input (pins 2-9)	All	10/20/30	10/20/30	kΩ min/typ/max	
V_{REF} (For Specified Performance)	All	-10	-10	V	±5%
V_{REF} Range[4]	All	-5 to -15	-5 to -15	V	
Nominal Analog Input Range					
Unipolar Mode	All	0 to +V_{REF}, 0 to -V_{REF}	0 to +V_{REF} 0 to -V_{REF}	V V	See Figure 7 and 8.
Bipolar Mode	All	$-VB_{OFS} \leqslant VA_{IN} \leqslant \lvert V_{REF}\rvert - VB_{OFS}$			See Figure 9
DIGITAL INPUTS					
$\overline{CS}$ (pin 13), ALE (pin 16), A_0 - A_2 (pins 17-19), CLK (pin 15)					
V_{INH} Logic HIGH Input Voltage	All	+2.2	+2.4 min	V	
V_{INL} Logic LOW Input Voltage	All	+1.2	+0.8 max	V	
I_{IN} Input Current	All	0.01	1 max	μA	V_{IN} = 0V, V_{DD}
C_{IN} Input Capacitance[5]	All	4	5 max	pF	
DIGITAL OUTPUTS					
$\overline{STAT}$ (pin 12), DB_7 to DB_0 (pins 20-27)					
V_{OH} Output HIGH Voltage	All	+4.8	+4.5 min	V	I_{SOURCE} = 40μA
V_{OL} Output LOW Voltage	All	+0.4	+0.6 max	V	I_{SINK} = 1.6mA
I_{LKG} DB_7 to DB_0 Floating State Leakage	All	0.3	10 max	μA	
Floating State Output Capacitance (DB_7 - DB_0)	All	5	10 max	pF	V_{OUT} = 0V to V_{DD}
Output Code	All	Unipolar Binary Figure 7 Complementary Binary Figure 8 Offset Binary Figure 9			
POWER REQUIREMENTS					
V_{DD}	All	+5	+5	V	
I_{DD} - Static	All	3 typ	5 max	mA	
I_{DD} - Dynamic	All	3 typ	8 max	mA	f_{CLK} = 1MHz

NOTES
[1] Temperature range as follows: JN, KN, LN (0 to +70°C), AD, BD, CD (-25°C to +85°C).
[2] Typical offset temperature coefficient is ±150μV/°C.
[3] R_{BOFS}/R_{AIN} (0-7) mismatch causes transfer function rotation about positive full scale. The effect is an offset and a gain term when using the circuits of Figure 8a, and Figure 9a.
[4] Typical value, not guaranteed or subject to test.
[5] Guaranteed but not tested.
[6] Typical change in B_{OFS} gain from +25°C to T_{min} or T_{max} is ±2LSBs.
Specifications subject to change without notice.

AC SPECIFICATIONS (V_{DD} = +5V, V_{REF} = -10V, Unipolar Operation, unless otherwise noted)

Symbol	Specification	Typical at +25°C	Limit Over Temperature	Units	Conditions
t_H	ALE pulse width	50	80 min	ns	See "Switching Terminology"
t_{ALS}	Address valid to latch set-up time	45	70 min	ns	
t_{ALH}	Address valid to latch hold time	10	20 min	ns	
t_{LCS}	Address latch to $\overline{CS}$ set-up time	10	20 min	ns	
t_{ACC}	$\overline{CS}$ to output propagation delay	200	250 max	ns	C_L = 100pF
t_{CW}	$\overline{CS}$ pulse width	250	280 min	ns	
t_{CF}	$\overline{CS}$ to output float propagation delay	50	80 max	ns	
t_{CLZ}	$\overline{CS}$ to low impedance bus	100	150 max	ns	
f_{CLK}	Clock frequency for stated accuracy	1600	1200 max[1]	kHz	

[1] Guaranteed conversion time of 66.6μs/channel with 1200kHz clock.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND . . . . . +7V
V_{DD} to DGND . . . . . +7V
AGND to DGND . . . . . -0.3V, V_{DD}
Digital Input Voltage to DGND
(pins 13, 16-19) . . . . . -0.3V, +15V
Digital Output Voltage to DGND
(pins 12, 20-27) . . . . . -0.3V, V_{DD}
CLK (pin 15) input voltage to DGND . . . . . -0.3V, +15V
V_{REF} (pin 10) to AGND . . . . . ±25V
V_{BOFS} (pin 1) to AGND . . . . . ±17V
AIN (0-7) (pin 9-2) . . . . . ±17V
Operating Temperature Range
JN, KN, LN . . . . . 0 to +70°C
AD, BD, CD . . . . . -25°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C

Power Dissipation (Package)
Plastic (Suffix N)
to +50°C 1200mW
Derate above +50°C by . . . . . 12mW/°C
Ceramic (Suffix D)
to +50°C 1000mW
Derate above +50°C by . . . . . 10mW/°C

10

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

GENERAL CIRCUIT INFORMATION

BASIC CIRCUIT DESCRIPTION

The AD7581 accepts eight analog inputs and sequentially converts each input into an eight-bit binary word using the successive approximation technique. The conversion results are stored in an 8 X 8 bit dual-port RAM. The device runs either directly from the microprocessor clock (in 6800 type systems) or from some suitable signal (e.g. ALE in 8085 type systems). Most applications require only a −10V reference and a +5V supply. Start-up logic is included on the device to establish the correct sequences on power-up. A maximum of 800 clock pulses are required for this period. Figure 1 shows the AD7581 functional diagram.

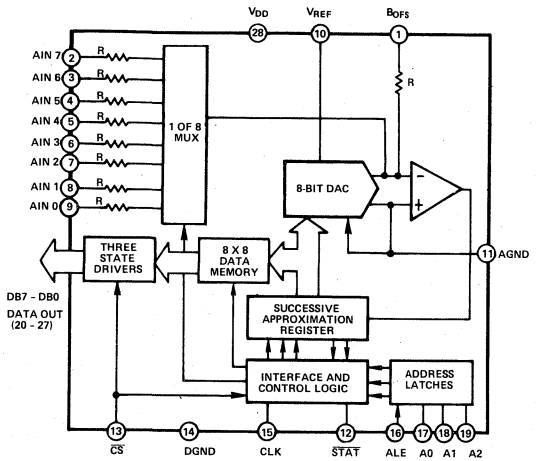


Figure 1. AD7581 Functional Diagram

Conversion of a single channel requires 80 input clock periods and a complete scan through all channels requires 640 input clock periods. When a channel conversion is complete, the successive approximation register contents are loaded into the proper channel location of the 8 X 8 RAM. At this time a status signal output, $\overline{STAT}$ (pin 12), gives a short negative going pulse (8 clock periods). This negative going $\overline{STAT}$ pulse is extended to 72 clock periods when channel 1 conversion is complete. An external pulse-width detector connected to the status pin can be used to derive conversion-related timing signals for microprocessor interrupts (see Channel Identification opposite page). Simultaneous with $\overline{STAT}$ going low, the MUX address is decremented. Eight clock periods later the next conversion is started.

Automatic interleaved DMA is provided by on-chip logic to ensure that memory updates take place at instants when the microprocessor is not addressing memory. Memory locations are addressed by A_0, A_1 and A_2. This address may be latched by ALE for systems which feature a multiplexed address/data bus or alternatively, for systems which have separate address and data buses, the address latches can be made transparent by tying ALE (pin 16) HIGH. $\overline{CS}$ (pin 13) activates three-state buffers to place addressed data on the $DB_0 - DB_7$ data output pins.

A/D CIRCUIT DETAILS

In the successive approximation technique, successive bits, starting with the most significant bit (DB_7), are applied to the input of the D/A converter. The DAC output is then compared to the unknown analog input voltage, A_{IN} (n), using a comparator. If the DAC output is greater than $A_{IN}(n)$, the data latch for the trial bit is reset to zero, and the next smaller data bit is tried. If the DAC output is less than $A_{IN}(n)$, the trial data bit stays in the "1" state, and the next smaller data bit is tried. Each successive bit is tried, compared to $A_{IN}(n)$, and set or reset in this manner until the least significant bit (DB_0) decision is made. The successive approximation register now contains a valid digital representation of $A_{IN}(n)$. $A_{IN}(n)$ is assumed to be stable during conversion.

The current weighting D/A converter is a precision multiplying DAC. Figure 2 shows the functional diagram of the DAC as used in the AD7581. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted i.e., the current in the MSB arm is V_{REF} divided by 2R, in the second arm is V_{REF} divided by 4R, etc. Depending on the D/A logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to A_{GND} or to the comparator summing point.

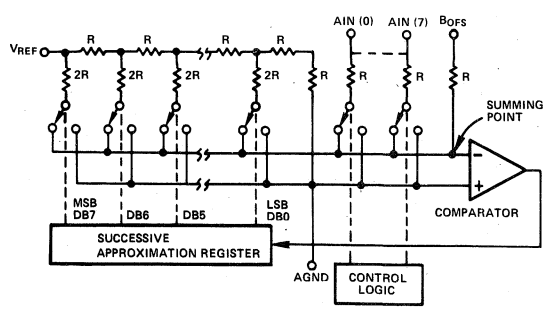


Figure 2. D/A Converter as Used in AD7581

TIMING AND CONTROL OF THE AD7581

CHANNEL SELECTION

Table I shows the truth table for the address inputs. The input address is latched when ALE goes LOW. When ALE is HIGH the address input latch is transparent.

A2	A1	A0	ALE	Channel Data To Be Read
0	0	0	1	Channel 0
0	0	1	1	Channel 1
0	1	0	1	Channel 2
0	1	1	1	Channel 3
1	0	0	1	Channel 4
1	0	1	1	Channel 5
1	1	0	1	Channel 6
1	1	1	1	Channel 7

Table I. Channel Selection Truth Table

TIMING AND CONTROL

A typical timing diagram is shown in Figure 3. When $\overline{CS}$ is HIGH, the three-state data drivers are in the high-impedance state. When $\overline{CS}$ goes LOW the data drivers switch to the low-impedance state (i.e., low impedance to DGND or to V_{DD}). Output data is valid after time t_{ACC}.

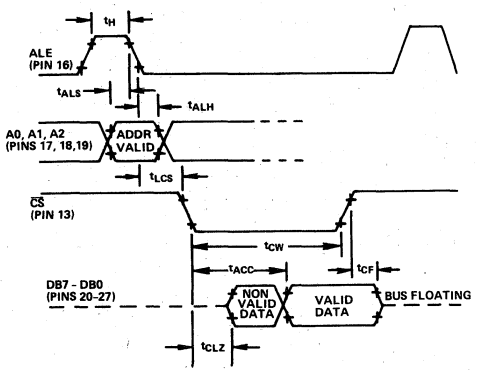


Figure 3. Timing Diagram for the AD7581

SWITCHING TERMINOLOGY

t_H: ALE pulse width requirement.
t_{ALH}: Address Valid to latch hold time.
t_{ALS}: Address Valid to latch set-up time.
t_{LCS}: Address latch to Chip Select set-up time.
t_{CW}: Chip Select pulse width requirement.
t_{ACC}: Chip Select to valid data propagation delay.
t_{CF}: Chip Select to output data float propagation delay.
t_{CLZ}: Chip Select to low impedance data bus.

CHANNEL IDENTIFICATION

In some real-time applications, it may be necessary to provide an interrupt signal when a particular channel receives updated data. To achieve this, it is necessary to identify which channel is currently under conversion. The $\overline{STAT}$ output provides an identifying signal by staying low for an additional 64 clock periods over normal (8 clock periods) when channel 0 is active. This is illustrated in Figure 4. Memory update takes place on a rising edge of a clock pulse and is completed in 200ns. This occurs 6 clock periods before $\overline{STAT}$ goes low.

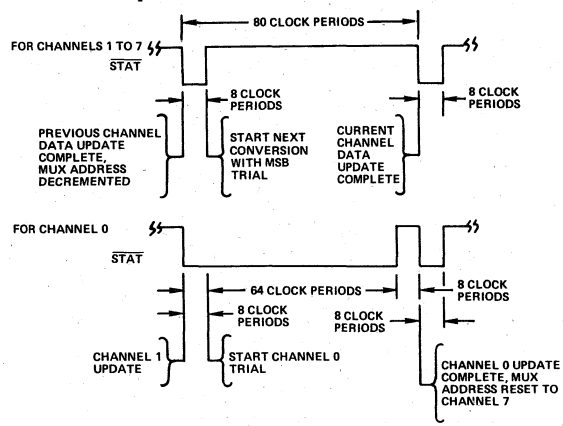


Figure 4. $\overline{STAT}$ Output for Channel Identification

10

One simple circuit using the $\overline{STAT}$ output is shown in Figure 5. The time constant RC is chosen such that X_2 ignores the normal $\overline{STAT}$ low pulse width (8 clock periods wide) but respond to the much wider $\overline{STAT}$ low pulse width (72 clock periods wide) occurring during channel 0 conversion. Typically for a 1μs clock period C = 0.022μF, R = 1.8kΩ.

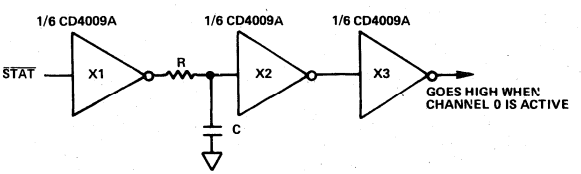


Figure 5. Hardware Channel Identification

Another possibility is to use the microprocessor to interrogate the $\overline{STAT}$ output and hence determine channel identity. A simple routine is shown in Figure 6.

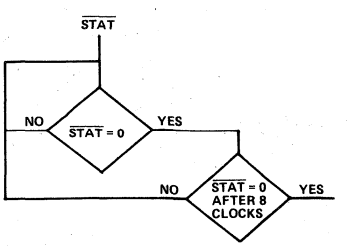


Figure 6. Software Channel Identification

OPERATING THE AD7581

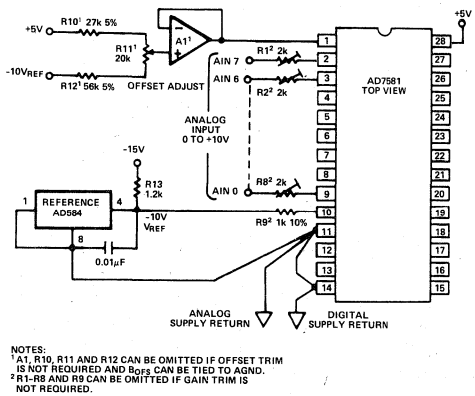
UNIPOLAR BINARY OPERATION

Figures 7a and 7b show the analog circuit connections and typical transfer characteristic for unipolar operation (0V to +10V). An AD584 is used for the -10V reference. Calibration is as follows (device clocked i.e., continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and and exercise ALE to latch the address.
2. With AIN 0 = 19.5mV (1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and DB_0 (LSB) flickers.



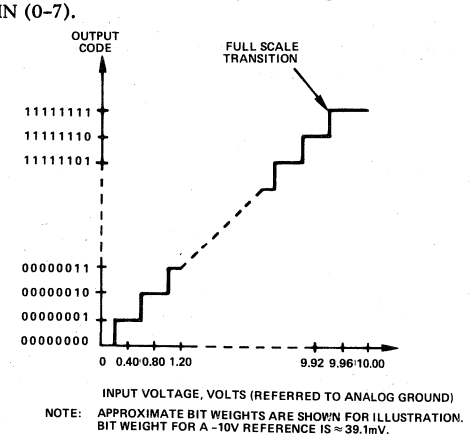
NOTES:
[1] A1, R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED AND B_{OFS} CAN BE TIED TO AGND.
[2] R1-R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.

Figure 7a. AD7581 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1. Apply +9.941V (FS - 3/2LSB) to all input channels AIN (0-7).



NOTE: APPROXIMATE BIT WEIGHTS ARE SHOWN FOR ILLUSTRATION. BIT WEIGHT FOR A -10V REFERENCE IS ≈39.1mV.

Figure 7b. Transfer Characteristic for Unipolar Circuit of Figure 7a

2. Select required channel n via A_0, A_1, A_2 and latch the Address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.

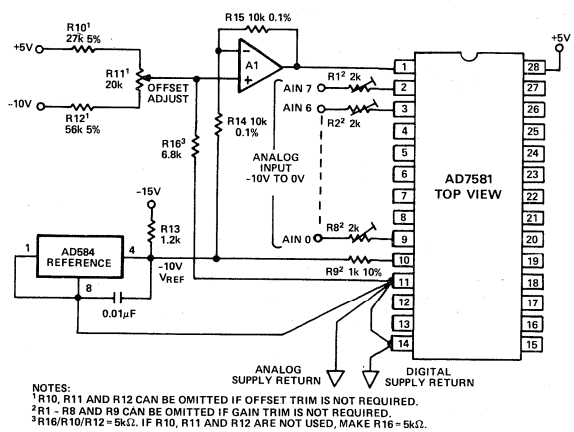
UNIPOLAR (COMPLEMENTARY BINARY) OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar (complementary binary) operation.
Calibration is as follows (continuous conversions);

OFFSET:

Comparator offset is trimmed out via the bipolar offset pin B_{OFS}. R10, R11 and R12 comprise a simple voltage tap buffered by A1 and feeding into B_{OFS}.

1. Since comparator offset will be the same regardless of which channel is active, take A_0, A_1 and A_2 LOW and exercise ALE to latch the address.
2. With AIN 0 = -9.98V (-FS + 1/2LSB) adjust R11, i.e., the offset voltage on B_{OFS}, until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.



NOTES:
[1] R10, R11 AND R12 CAN BE OMITTED IF OFFSET TRIM IS NOT REQUIRED.
[2] R1 - R8 AND R9 CAN BE OMITTED IF GAIN TRIM IS NOT REQUIRED.
[3] R16/R10/R12 = 5kΩ. IF R10, R11 AND R12 ARE NOT USED, MAKE R16 = 5kΩ.

Figure 8a. AD7581 (0V to -10V) Operation (Output Code is Complementary Binary)

GAIN (FULL SCALE)

In many applications gain adjustment is not required thus removing the need for trimmers in the analog channels. For channels requiring gain trim, the following procedure is recommended. Offset adjustment must be performed before gain adjustment.

1) Apply -58.6mV (3/2LSB) to all input channels AIN (0-7).
2) Select required channel n via A_0, A_1, A_2 and exercise ALE to latch the address.
3) Adjust trimmer RN of selected channel until DB_7 - DB1 are HIGH and the LSB (DB_0) flickers.
4) Select next channel requiring gain trim and repeat step 2 and 3.

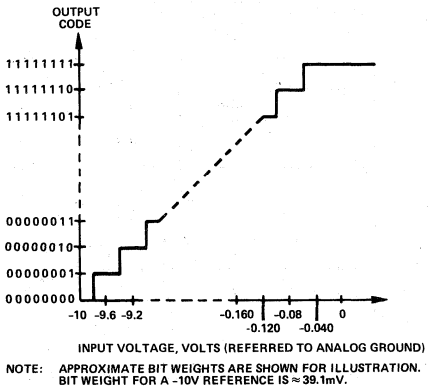


Figure 8b. Transfer characteristic for Unipolar Circuit of Figure 8a

BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for ±5V bipolar operation. Output coding is offset binary. Comparator offset correction is again applied to the B_{OFS} pin.

Calibration is as follows (continuous conversions);

OFFSET:

1. Apply -4.980V (-F.S. + 1/2LSB) to all input channels, AIN (0-7).
2. Trim R11 of the comparator offset circuit until $DB_7 - DB_1$ are LOW and the LSB (DB_0) flickers.

GAIN (FULL SCALE)

1. Apply +4.941V (+F.S. -3/2LSB) to all input channels, A_{IN} (0 - 7).
2. Select required channel n via A_0, A_1, A_2, and latch the address using ALE.
3. Adjust trimmer RN of selected channel until $DB_7 - DB_1$ are HIGH and the LSB (DB_0) flickers.
4. Select next channel requiring gain trim and repeat steps 2 and 3.
5. Apply -19.5mV to each gain-trimmed channel. If the ADC output code does not flicker between 01111111 and 10000000 repeat the calibration procedure.

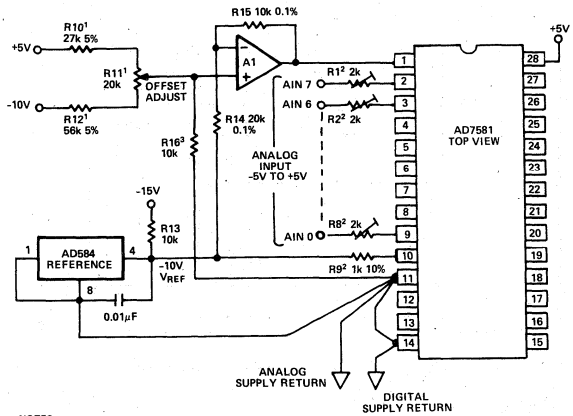


Figure 9a. AD7581 Bipolar (-5V to +5V) Operation (Output Code is Offset Binary)

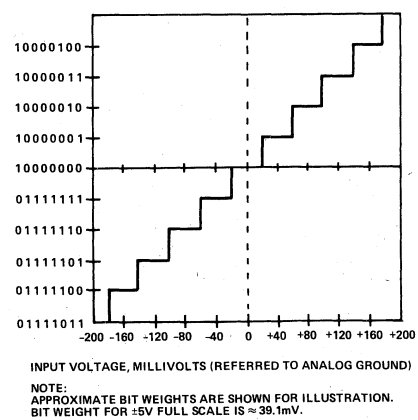


Figure 9b. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a

INTERFACING THE AD7581

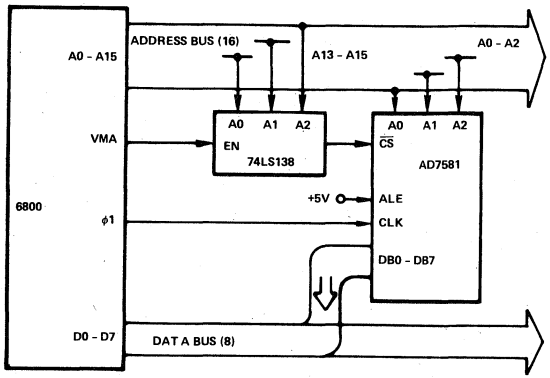


Figure 10. AD7581/6800 Interface

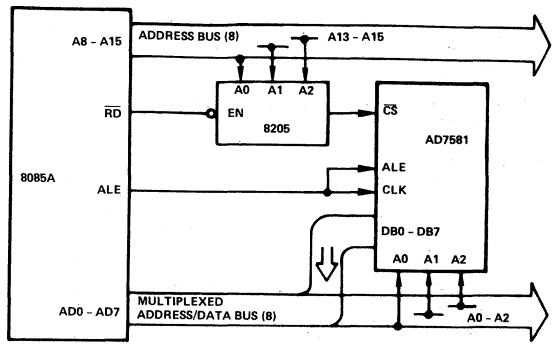


Figure 11. AD7581/8085 Interface

NOTES:

1. ANALOG AND DIGITAL GROUND
   It is recommended that A_{GND} and D_{GND} be connected locally to prevent the possibility of injecting noise into the AD7581. In systems where the A_{GND} - D_{GND} intertie is not local, connect back-to-back diodes (1N914 or equivalent) between the AD7581 A_{GND} and D_{GND} pins.
2. LOGIC DEGLITCHING IN μP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7581 $\overline{CS}$ terminal. These glitches can cause unwanted reads. The best way to avoid glitches is to gate the address decoding logic, e.g., with RD (8080), $\overline{RD}$ (8085) or VMA (6800).

ANALOG DEVICES

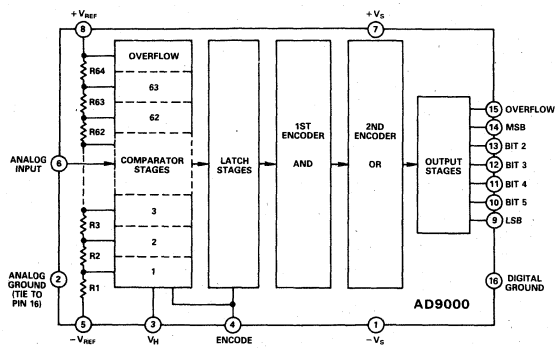
Ultra High-Speed 6-Bit Monolithic ADC

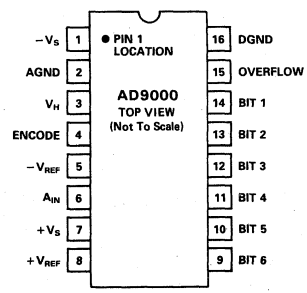
AD9000

FEATURES
6-Bit, 75MHz Minimum Word Rates
No T/H Required
−55°C to +125°C Temperature
Overflow Bit for Cascading Units

APPLICATIONS
Image Processing
Video Digitizing
Radar Digitizing
Military Systems

AD9000 FUNCTIONAL BLOCK DIAGRAM





Outline & Pin Designations

GENERAL DESCRIPTION

The AD9000 A/D Converter is another addition to the expanding line of monolithic high-speed data converters available from Analog Devices. As model number AD9000SD, this 6-bit, 75MHz A/D can be operated over a temperature range extending from −55°C to +125°C, making it useful for a variety of applications in a wide diversity of environments. For applications requiring operation from 0 to +70°C, the AD9000JD is the recommended choice.

The AD9000 is a "flash" converter which uses 64 parallel comparators to digitize fast-moving analog input signals without the need for external track-and-hold (T/H) circuits. An overflow bit can be used for connecting multiple units in a cascade arrangement to obtain up to eight bits of digital data at MHz word rates.

Two cascaded devices can be used to obtain seven bits, and four units will provide eight bits of ECL-compatible output data.

Careful design techniques assure temperature coefficients which allow the unit to be operated over extended temperature ranges. The flexibility and usefulness of the AD9000 are also enhanced by its ability to operate with maximum positive and negative reference voltages applied simultaneously, as contrasted with other flash converters which often limit the user to a small range of voltage within the extremes.

All models of the AD9000 are packaged in standard ceramic DIP 16-pin configurations.

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Model		AD9000SD			AD9000JD		
Parameter	Units	Min	Typ	Max	Min	Typ	Max
RESOLUTION (FS = Full Scale)	Bits		6			6	
LSB WEIGHT							
$+V_{REF} = -V_{REF} = 0.512V$	mV		16			16	
$+V_{REF} = -V_{REF} = 1.024V$	mV		32			32	
$+V_{REF} = -V_{REF} = 2.048V$	mV		64			64	
DC ACCURACY	%FS ± 1/4LSB		0.4			0.4	
Nonlinearity vs. Temperature	% of FS/°C		0.003			0.003	
Differential Linearity[1]							
$+V_{REF} = -V_{REF} = 0.512V$	LSB		0.75	1.0		0.75	
$+V_{REF} = -V_{REF} = 1.024V$	LSB		0.25	0.5		0.25	
$+V_{REF} = -V_{REF} = 2.048V$	LSB		0.2	0.4		0.2	
Integral Linearity[2]							
$+V_{REF} = -V_{REF} = 0.512V$	LSB		1.25	1.5		1.25	
$+V_{REF} = -V_{REF} = 1.024V$	LSB		0.7	1.0		0.7	
$+V_{REF} = -V_{REF} = 2.048V$	LSB		0.4	0.75		0.4	
Monotonicity		Guaranteed −55°C to +125°C			Guaranteed 0 to +70°C		
DYNAMIC CHARACTERISTICS							
In-Band Harmonics[2]							
(dc to 1MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		44			44	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		47			47	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		47			47	
(1MHz to 5MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		40			40	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		40			40	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		41			41	
(5MHz to 8MHz)							
$+V_{REF} = -V_{REF} = 0.512V$	dB below FS		30			30	
$+V_{REF} = -V_{REF} = 1.024V$	dB below FS		30			30	
$+V_{REF} = -V_{REF} = 2.048V$	dB below FS		31			31	
Conversion Time	ns		13			13	
Conversion Rate[3]	MHz	75	100		50		
Aperture Uncertainty (Jitter)	ps		25			25	
Aperture Time (Delay) (T_D)	ns		2			2	
Setup Time (t_s)[4]	ns	2			2		
Hold Time (t_h)[5]	ns	2			2		
Signal Transition Time[6]							
Input to Output Low ($t_{pd}-$)	ns	11	13	14	11	13	14
Input to Output High ($t_{pd}+$)	ns	8	10	12	8	10	12
Signal to Noise Ratio (SNR)[7]							
$+V_{REF} = -V_{REF} = 0.512V$	dB		36			36	
$+V_{REF} = -V_{REF} = 1.024V$	dB		37			37	
$+V_{REF} = -V_{REF} = 2.048V$	dB		36			36	
Signal to Noise Ratio (SNR)[8]							
$+V_{REF} = -V_{REF} = 0.512V$	dB		45			45	
$+V_{REF} = -V_{REF} = 1.024V$	dB		46			46	
$+V_{REF} = -V_{REF} = 2.048V$	dB		45			45	
Noise Power Ratio (NPR)[9]							
$+V_{REF} = -V_{REF} = 0.512V$	dB	27	29			29	
$+V_{REF} = -V_{REF} = 1.024V$	dB	27	29			29	
$+V_{REF} = -V_{REF} = 2.048V$	dB	27	29		27	29	
Transient Response[10]	ns			10			10
Overvoltage Recovery[11]	ns		5			5	
ANALOG INPUT (A_{IN})							
Voltage Range, Rated Performance	V	±0.5		±2			
Input Type		Unipolar (positive or negative) or Bipolar					
Input Current							
Hold (Latch) Mode	μA	−10		+10	−10		+10
Track (Sample) Mode[12]	μA		550	800		550	800
Input Capacitance[13]	pF		30			30	
Impedance[12]	kΩ		3.6			3.6	
Frequency Response[14]							
(75MHz Encode Rate)							
$+V_{REF} = -V_{REF} = 0.512V$	MHz		24			24	
$+V_{REF} = -V_{REF} = 1.024V$	MHz		20			20	
$+V_{REF} = -V_{REF} = 2.048V$	MHz		15			15	
REFERENCE INPUT							
Positive Reference ($+V_{REF}$)	V	−1.5		+2.0	−1.5		+2.0
Negative Reference ($-V_{REF}$)	V	−2.0		+1.5	−2.0		+1.5
Resistance	Ω	80	100	200	80	100	200
Bandwidth							
Small Signal, 3dB	MHz		25			25	
Large Signal, 3dB	MHz		20			20	

Model / Parameter	Units	AD9000SD Min	AD9000SD Typ	AD9000SD Max	AD9000JD Min	AD9000JD Typ	AD9000JD Max
ENCODE COMMAND INPUT							
Logic Compatibility			ECL			ECL	
Digital "1" (Hold/Latch)	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0" (Track/Sample)	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Digital "1" Current	μA	5	15	35	5	15	35
Digital "0" Current	μA	5	15	35	5	15	35
Required Termination (to −2V)	Ω			50			50
Pulse Width							
Hold/Latch [t_{pw}(H)]	ns	5	7		5	7	
Track/Sample [t_{pw}(T)]	ns	4	6		4	6	
Frequency[3]	MHz	75	100		50		
DIGITAL OUTPUT							
Format	Bits	6 Parallel (RZ) plus Overflow (NRZ)					
Logic Compatibility		ECL					
Digital "1"	V	−1.1	−0.9	−0.6	−1.1	−0.9	−0.6
Digital "0"	V	−2.0	−1.7	−1.5	−2.0	−1.7	−1.5
Required Termination (to −2V)	Ω	100			100		
Time Skew	ns			0.4			0.4
Coding		Binary (BIN) Offset Binary (OBN) No Data Ready Output Pulse					
POWER REQUIREMENTS							
+5V ±5% (+V_S)	mA		60	75		60	75
−5.2V ±5% (−V_S)	mA		67	85		67	85
Power Dissipation							
(+V_{REF} = −V_{REF} = 0V)	mW		650			650	
(+V_{REF} = −V_{REF} = 1V)	mW		690			690	
(+V_{REF} = −V_{REF} = 2V)	mW		810			810	
TEMPERATURE RANGE							
Operating (Case)	°C	−55		+125	0		+70
Storage	°C	−55		+150	−55		+150
THERMAL RESISTANCE[15]							
Junction to Air, θja (Free Air)	°C/W		95			95	
Junction to Case, θjc	°C/W		20			20	
PACKAGE TYPE[16]			D16A			D16A	

NOTES

[1]Encode Rate = 75MHz; Analog Input = 1kHz.

[2]Spurious in-band signals generated at 20MHz encode rate at analog inputs shown in ( ).

[3]Some spec degradation may occur at word rates (encode frequencies) above minimum shown. See Figure 4 for typical relationship between analog input frequencies and encode rates.

[4]This is internal time set by design and is the minimum time before positive leading edge of Encode Command that a latch output must be at "1" for digital output to be generated by the latch.

[5]This is internal time set by design and is the minimum time after positive leading edge of Encode Comand that a latch output must remain at "1" for digital output to be generated by the latch.

[6]Specifications with digital outputs terminated in 100Ω connected to −2V.

[7]RMS signal to rms noise ratio with 500kHz analog input.

[8]Peak-to-peak signal to rms noise ratio with 500kHz analog input.

[9]DC to 8.2MHz white noise bandwidth with slot frequency of 3.886MHz; and encode rate of 20MHz.

[10]For full-scale step input, 6-bit accuracy attained in specified time.

[11]Recovers to 6-bit accuracy in specified time after 150% FS input overvoltage.

[12]Measured in track (sample) mode with A_{IN} = +V_{REF}.

[13]Measured with A_{IN} = +V_{REF}.

[14]Specified frequencies are maximums with no missing codes.

[15]Recommended maximum junction temperature is +150°C. When using ±2V references, this temperature may be exceeded unless some form of heat sinking and/or cooling air is used. Note θja specification.

[16]See Section 19 for package outline information.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Parameter	Units	Lower Limit	Upper Limit
Supply Voltages			
$+V_S$	Volts	−0.3	+6.0
$-V_S$	Volts	−6.0	+0.3
Analog Input (A_{IN})	Volts	−3.0	+3.0
Encode Command Input	Volts	−6.0	0.0
Reference Inputs			
$+V_{REF}$	Volts	−3.0	+3.0
$-V_{REF}$	Volts	−3.0	+3.0
Hysteresis Control Input	Volts	0	+3.0
Temperature			
Operating			
AD9000SD	°C	−55	+125
AD9000JD	°C	0	+70
Storage	°C	−55	+150
Lead Soldering (10 seconds)	°C		+300

PIN	SYMBOL	FUNCTION
1	$-V_S$	−5.2V NEGATIVE SUPPLY VOLTAGE
2	A_{GND}	ANALOG GROUND
3	V_H	HYSTERESIS CONTROL
4	ENCODE	ENCODE COMMAND INPUT
5	$-V_{REF}$	NEGATIVE VOLTAGE REFERENCE
6	A_{IN}	ANALOG INPUT
7	$+V_S$	+5V POSITIVE SUPPLY VOLTAGE
8	$+V_{REF}$	POSITIVE VOLTAGE REFERENCE
9	BIT 6	LEAST SIGNIFICANT BIT (LSB) OUTPUT
10	BIT 5	BIT 5 OUTPUT
11	BIT 4	BIT 4 OUTPUT
12	BIT 3	BIT 3 OUTPUT
13	BIT 2	BIT 2 OUTPUT
14	BIT 1	MOST SIGNIFICANT BIT (MSB) OUTPUT
15	OVERFLOW	OVERFLOW BIT OUTPUT
16	D_{GND}	DIGITAL GROUND

NOTE: A_{GND} (PIN 2) and D_{GND} (PIN 16) SHOULD BE CONNECTED TOGETHER AS CLOSE TO CASE AS POSSIBLE.

THEORY OF OPERATION

Refer to the Block Diagram of the AD9000.

Reference voltages ($+V_{REF}$ and $-V_{REF}$) applied across an array of identical resistors establish the analog operating span of the unit ($+V_{REF}$) – ($-V_{REF}$). The 64 resistors in the array divide the range into quantization levels equal to intervals of one least significant bit (LSB) between each resistor.

Each tap of the resistor array is connected to its associated voltage comparator input; the other input of each comparator is connected to the analog input (A_{IN}) signal. In this way, the comparator stages simultaneously compare the analog input with each one of the 64 (including OVERFLOW) quantization levels within the analog span set by the reference voltages.

Any comparator whose reference level is less than the analog input voltage will change its output state to a digital "1". Comparators whose reference levels are greater than the analog input will remain at digital "0".

Depending on the value of A_{IN}, anywhere from none to 64 comparators might have digital "1" at their outputs; the remaining comparators will be at digital "0". Obviously, processing that many bits of digital information is impractical if the data remain in this type of unwieldy format.

Wired-or logic circuits within the AD9000 re-encode the comparator outputs into a manageable, binary format of six bits of parallel data; along with an overflow bit which allows cascading units to obtain higher resolution.

The outputs of the comparators are applied to latches controlled by the ENCODE input. When the encode command is low (digital "0"), the latches are transparent; this is the track (sample) mode of the AD9000.

When the ENCODE input changes to high (digital "1"), the latches go into a "hold" (latch) condition, "freezing" the most recent digital outputs of the comparators and applying them to the encoding circuits.

The signal held in the latches is converted to binary form by the encoders and applied to the output stages as a six-bit digital representation of the analog signal which was present at the comparator inputs at the instant the ENCODE command made the change to the "hold" mode.

After 5–7 nanoseconds in the "hold" mode, the ENCODE input again transitions to a "track" condition; and the six bits of parallel data (but not the OVERFLOW output) return to zero (RZ). The "track" portion of the ENCODE command is 4–6 nanoseconds and during this interval the latches respond to the new state of the comparator outputs. The ENCODE signal then transitions again to the hold/latch (digital "1") mode and the cycle repeats. Track mode and hold mode intervals are dependent on duty cycle; times cited here are approximations for an encode frequency of 75MHz.

Time relationships of the hold/latch mode and track/sample mode of the ENCODE command are often influenced by the word rate selected by the user. At higher rates, it may be desirable to shorten the "hold" portion and lengthen the "track" portion; this technique can often enhance overall performance of the unit.

There is no need for an external track-and-hold circuit because the latches are performing the track/hold function. The aperture uncertainty (jitter) and aperture time (delay) specifications shown on the Specifications Table are "worst case" specs for the individual comparator cells, but are valid for the AD9000 because they manifest themselves as converter characteristics.

The good linearity tempco of the AD9000 is the result of using matched diffused resistors in the input network. Linearity in this type of converter is dependent primarily on the tracking of resistors; expressed in another way, resistance **ratios** are more important than absolute resistance **values**. Comparator thresholds in the AD9000 remain constant within a small fraction of 1LSB over the complete operating temperature range because of the close tracking of the resistors within the network. The temperature coefficients of comparator input bias currents and initial offset voltages which contribute to nonlinearity are kept small in the design of the AD9000 to minimize their effects.

Low offset voltages in the comparators are critically important for establishing the lower limit of the analog span set by the voltage references. When the reference voltage across the resistor chain decreases (the difference between $+V_{REF}$ and $-V_{REF}$ becomes less), the smaller value of the LSB approaches the value of the "worst case" comparator offset voltage. As the two get closer to one another, increasing linearity errors can restrict the lower limit of the analog span if comparator offset is relatively large.

The upper limit of the analog span is established by the common-mode range of the comparators because this range sets the maximum differential between $+V_{REF}$ and $-V_{REF}$. In this characteristic, too, the design of the AD9000 suggests its use instead of some competing devices.

Unlike some units, the AD9000 allows maximums of positive and negative reference voltages to be applied simultaneously. In some "flash" A/D's, the analog span is limited to some small range within the range of references, as opposed to being equal to the extremes. The ability of the AD9000 to operate with full-scale references improves its usefulness to the designer by imposing fewer constraints on operating conditions.

Like all flash converters, the input resistance of the AD9000 varies as a function of analog input voltage. This is because the individual comparators draw no current until the input voltage exceeds the reference voltage of the comparator; after that, the comparator's input current remains essentially constant. Consequently, the converter's input current and input resistance increase in a series of small steps as successive comparators are operated by an increasing analog input.

The input capacitance of the unit is the sum of the junction capacitances of the individual comparators. For many flash converters, this total is sometime sufficiently high to require a low-impedance driving source for the analog input. In the AD9000, however, input capacitance is typically 30pF, which is considerably lower than many competing devices and imposes fewer restrictions on the driving source.

AD9000 TIMING DIAGRAM

Refer to Figure 1, AD9000 Timing Diagram.

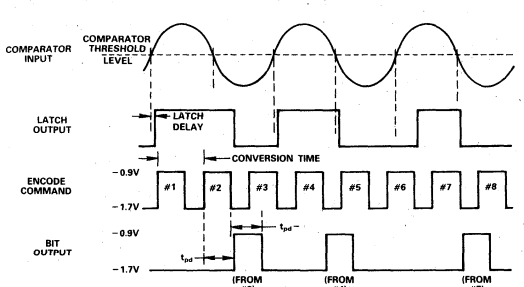


Figure 1. AD9000 Timing Diagram

The comparator input shown on the top of the diagram is the analog input applied to one of the 63 comparators used to establish the digital value of the output word. The latch output is the latch associated with that comparator.

Each time the analog input applied to the comparator exceeds the reference level of the comparator, the corresponding latch output transitions to a digital "1" level.

When the encode command is at $-0.9V$ (digital "1") and the latch outut is at digital "1", a bit output associated with the comparator/latch combination will appear at the output. This statement is true only if:

A. The latch output is at digital "1" for a minimum of two nanoseconds before the positive-going leading edge of the encode signal (t_s).

B. The latch output remains at digital "1" for a minimum of two nanoseconds after the positive-going leading edge of the encode signal (t_h).

In Figure 1, there is no bit output associated with encode command #1 because the latch output was at the digital "1" level for less than the required two nanoseconds before the encode command changed. Encode command #2 however, combines with the same latch output to cause a bit output to appear.

At first glance, it might appear encode command #5 should combine with the second latch output to cause a bit output. It does not, however, because the latch output did not remain at a digital "1" level for a minimum two nanoseconds after the positive-going leading edge of the encode command.

Like t_s and t_h, the latch delay interval shown in Figure 1 is based on internal timing and is approximately one nanosecond long, but has only academic interest for the user. The important time intervals for proper use of the AD9000 are conversion time (typically 13ns); and signal transition time from the input to a positive output ($t_{pd}+$), and a negative output ($t_{pd}-$). Both signal transition times are typically 10ns.

In Figure 1, the widths of the digital "1" latch signals vary because of interaction with the hold commands. The first one is longer than normal because of encode pulse #2 causing the latch to continue to hold the "1" level. The second latch output is the expected width; while the third is shorter than normal because of encode pulse #6, which delays its transition by keeping it latched at digital "0".

APPLYING THE AD9000

The wired-or logic used in the AD9000 causes the data bits to go low (logic "0") whenever the OVERFLOW bit goes high. This characteristic allows two or more AD9000's to be operated in a cascaded arrangement when more than six bits of resolution are required.

When operating as a single 6-bit A/D, however, that feature of the AD9000 might be undesirable. This is because analog inputs greater than the positive reference voltage will appear as digital outputs of all "0", the same digital output expected of maximum negative inputs. The OVERFLOW bit can serve as a "flag" by going to digital "1" when the positive reference is exceeded.

For some applications, it may be preferable to have the logic output bits "lock up" at digital "1" for positive overvoltages; and digital "0" for negative overvoltages.

This can be accomplished with external logic, as shown in Figure 2, a typical connection for 6-bit operation of the AD9000.

A hex AND gate is used to bring the digital outputs high any time the OVERFLOW bit indicates the positive reference has been exceeded; this gate is wire-ored with the outputs of the AD9000.

Figure 2 contains other details on the preferred method for connecting the AD9000 into circuit applications. The suggested buffer amplifier for the analog input is the Analog Devices'

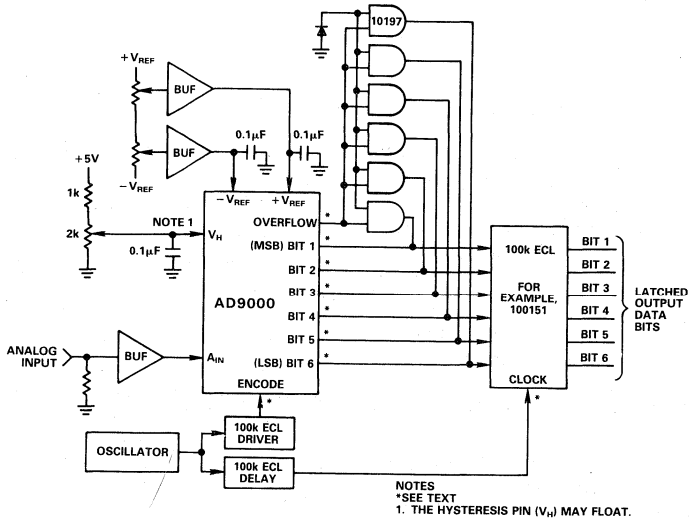


Figure 2. AD9000 6-Bit Operation

ADLH0033 or HOS-100; for the two reference voltages, AD741 devices are recommended. These high performance amplifiers are available in various models, making it easy for the user to select the unit best suited for his application.

The outputs of the reference buffer amplifiers are capacitively bypassed to help prevent noise from interfering with the performance of the AD9000. The ENCODE input is terminated in 50Ω connected to −2V; the CLOCK and digital outputs shown in Figure 2 are terminated in 100Ω, also to −2V.

If preferred, the hysteresis input (V_H) can be left floating, but experience indicates operation of the AD9000 may be improved with a variable voltage applied; this is particularly true at higher word rates.

Refer to Figure 3, which shows the effect of varying hysteresis control voltages.

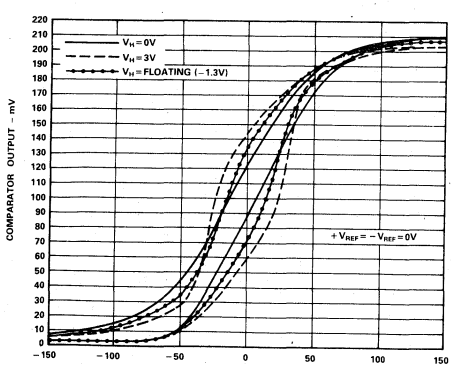


Figure 3. Comparator Output vs. Hysteresis Voltage

In this illustration of a typical comparator's output versus changes in hysteresis voltage, the combination of the two results in a "family" of classic hysteresis curves. The analog input (A_{IN}) voltage is measured in millivolts at the input of the comparator; the other comparator input, of course, is the voltage established by the tap on the resistor array discussed earlier. The comparator output shown on the vertical scale is internal to the AD9000 and appears at the output as an ECL-level signal.

For purposes of discussion of this particular comparator, $+V_{REF} = -V_{REF} = 0V$. Under these circumstances, the threshold of the illustrated comparator is close to 0mV. The thresholds of adjacent comparators would be at slightly different values, but the V_H hysteresis voltage would have the same general effect on the comparators' outputs.

Basically, the variations in hysteresis voltages change the gains of the comparators and slightly alter their outputs, as shown in Figure 3. In many applications, V_H could be left floating, which establishes a hysteresis voltage of approximately +1.3V. In other applications, however, the ability to introduce a small, predictable amount of hysteresis can enhance the AD9000's performance.

The hysteresis control input voltage can vary over a range of 0V to +3.0V, with voltages on the lower end of this span having only negligible effect. Variations between 0V and approximately +0.5V cannot generally be detected as having an impact on the comparator gain.

The interaction between analog input frequencies and the encoding word rate is shown in Figure 4.

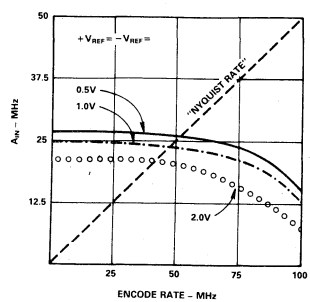


Figure 4. Analog Input vs. Encode Rate

The "Nyquist rate" is shown as a dotted line extending diagonally from dc to an analog input of 50MHz, and a word rate of 100MHz. As illustrated, the range of the analog input reference has a major effect on how closely the AD9000 approaches the Nyquist criteria.

In this figure, the analog input frequencies which are shown are the typical frequencies a user can expect to digitize without

missing codes. Note that as the "spread" of the reference voltages becomes larger, the expected analog input frequency becomes lower.

CASCADING AD9000's FOR MORE BITS

Earlier, there was an allusion to the capability for connecting multiple AD9000 units in a cascade arrangement to obtain more than six bits of digital information. Two cascaded devices would be used to obtain seven bits; and four cascaded devices used for eight bits of output. Although it is theoretically possible to generate multiple bits by employing this method, the practical limitations involved in doubling the number of AD9000's for each additional bit tend to restrict the technique to a maximum of eight bits of digital data.

A possible arrangement for achieving a 7-bit A/D converter is shown in Figure 5.

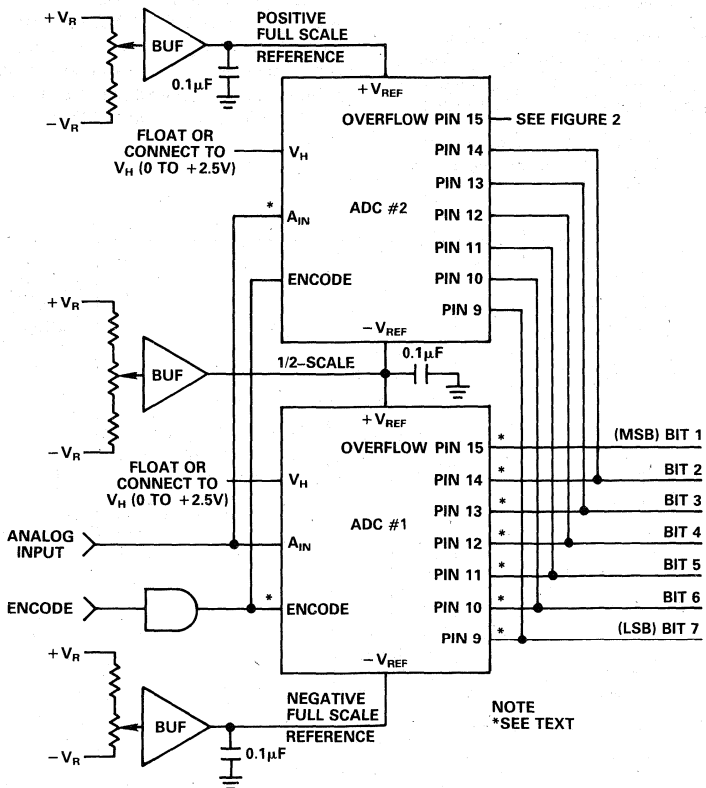


Figure 5. Cascaded AD9000's

When cascading units, the reference-resistor strings are connected in series and driven at the high, low, and mid-scale points. The 6-bit outputs of the two AD9000's are wired together and perform an *or* function; the Most Significant Bit (MSB) is provided by the OVERFLOW output of ADC #1.

If the analog input to the cascaded arrangement is below half-scale, the overflow bit of ADC #2 is low, and so are its output bits. This means the outputs of ADC #1 drive the output lines in response to the analog input.

When the analog input is above half-scale, the OVERFLOW bit of ADC #1 (the MSB) is high and acts as a carry; all the digital output bits of ADC #1 go low. ADC #2 converts the residual upper half-range, and its outputs drive the output lines. The conversions are occurring in parallel, so there is no loss of speed, regardless of whether or not one or both of the cascaded A/D's are operating. The OVERFLOW bit of ADC #2 is wire-ored with external logic in a fashion similar to the method used when operating the AD9000 as a six-bit converter.

If this same technique is expanded to eight bits with four cascaded AD9000 devices, the analog reference span is divided into four equal parts; and a small amount of external logic is used to establish Bit 2 and minimize time skew. The need to double the divisions of the reference span with each succeeding bit is a major deterrent in extending this method beyond eight bits of resolution.

The loads used in cascade are the same as those with a single AD9000, i.e., the ENCODE input is terminated in 50Ω and the CLOCK and digital outputs are terminated in 100Ω, with all loads connected to −2V.

AD9000 EVAULUATION/TEST BOARD

Evaluating and/or testing the AD9000 A/D converter is made easier with the use of a printed circuit board which contains an A/D and the necessary test and reconstruction circuits.

A block diagram of this circuit is shown in Figure 6.

The AD9000 being evaluated or tested is connected in a back-to-back arrangement with a high-speed, high-resolution D/A converter. This combination allows the user to select a reconstructed version of the digitized analog input; or to examine the error signal when checking linearity. All necessary circuit components are contained on the 8.5″ × 6.3″ printed circuit board; the user needs to provide only power supply voltages.

Two models of boards are available, but the only difference between them is the model number of the A/D which is installed at the time of shipment. The AD9000JD/PCB includes a model AD9000JD unit; the AD9000SD/PCB has a model AD9000SD.

In both boards, the A/D converter is installed in a socket; and all other circuits are soldered into place. This technique allows the evaluation board to be used as a test circuit for incoming AD9000 devices when production quantities are required. Complete operating instructions and a schematic are included with each board.

The test/evaluation board allows the user to check the performance of converters by providing a method for adjusting $+V_{REF}$, $-V_{REF}$, V_H, encode command pulse width, encode rate, and latch strobe delay. This kind of flexibility in assessing the unit's performance can supply valuable insight on how to obtain optimum performance from the AD9000 and get maximum benefit from its characteristics.

ORDERING INFORMATION

All versions of the AD9000 A/D converter are housed in 16-pin ceramic monolithic packages. Units operating over the standard temperature range of 0 to +70°C are designated AD9000JD; for operation over an extended temperature range of −55°C to +125°C, order model number AD9000SD.

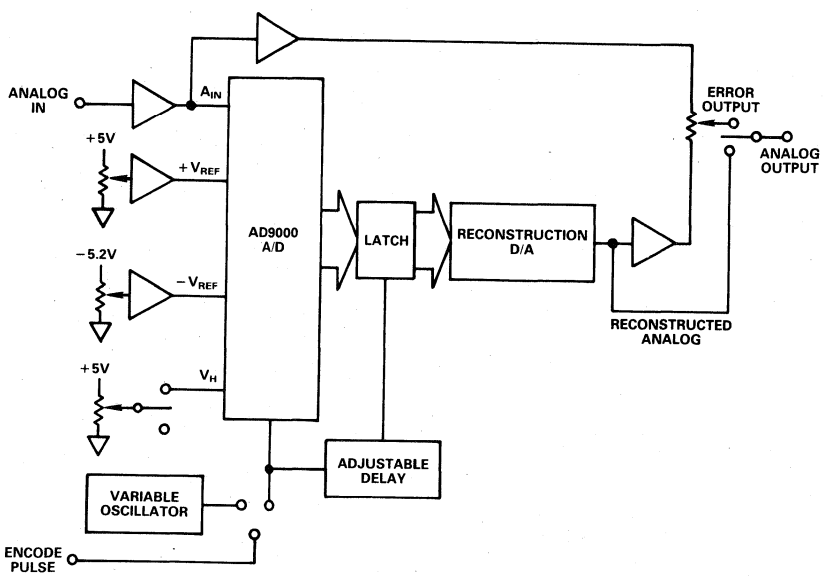


Figure 6. AD9000/PCB Block Diagram

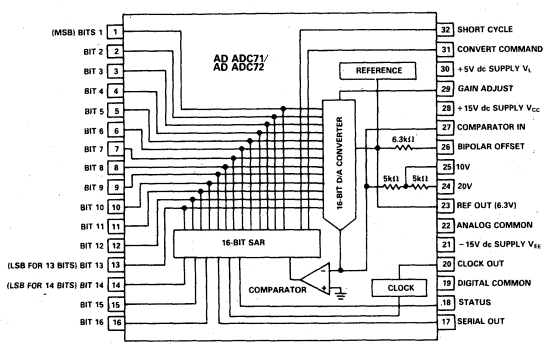
Complete, High Resolution 16-Bit A/D Converter

AD ADC71/ADC72

FEATURES

Complete 16-Bit Converter With Reference and Clock
±0.003% Maximum Nonlinearity
No Missing Codes to 14 Bits
Fast Conversion – 45μs (14 Bit)
Short Cycle Capability
Parallel or Serial Logic Outputs
Low Power: 850mW Typical
Industry Standard Pin Out

AD ADC71/ADC72 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC71 and AD ADC72 are high resolution 16-bit hybrid IC analog-to-digital converters including reference, clock, and laser-trimmed thin-film components. The package is a compact 32-pin metal (AD ADC71) or hermetic metal (AD ADC72) DIP. The thin-film scaling resistors allow analog input ranges of ±2.5V, ±5V, ±10V, 0 to +5V, 0 to +10V, and 0 to +20V.

Important performance characteristics of the devices are maximum linearity error of ±0.003% of FSR (AD ADC71K, AD ADC72K and B), and maximum conversion time of 50μs. This performance is due to innovative design and the use of proprietary monolithic D/A converter chips. Laser-trimmed thin-film resistors provide the linearity and wide temperature range for no missing codes.

The AD ADC71 and AD ADC72 provide data in both parallel and serial form with corresponding clock and status outputs. All digital inputs and outputs are TTL compatible.

APPLICATIONS

The AD ADC71 and AD ADC72 are excellent for use in applications requiring 14-bit accuracy over extended temperature ranges. Typical applications include medical and analytic instrumentation, precision measurement for industrial robots, automatic test equipment (ATE), multi-channel data acquisition systems, servo control systems and anywhere that excellent stability and wide dynamic range in the smallest space is required.

PRODUCT HIGHLIGHTS

1. The AD ADC71 and AD ADC72 provide 16-bit resolution with maximum linearity error less than ±0.003% (±0.006% for J and A grades) at 25°C.
2. Conversion time is 45μs typical to 14 bits with short cycle capability.
3. Two binary codes are available on the AD ADC71 and AD ADC72 output. They are complementary straight binary (CSB) for unipolar input voltage ranges and complementary offset binary (COB) for bipolar input ranges. Complementary two's complement (CTC) coding may be obtained by inverting pin 1 (MSB).
4. The proprietary chips used in this hybrid design provide excellent stability over temperature and lower chip count for improved reliability.

10

SPECIFICATIONS (typical at T_A = +25°C, V_S = ±15, +5 volts unless otherwise noted)

Model	AD ADC71JM, KM	AD ADC72JM, KM	AD ADC72AM, BM	Units
RESOLUTION	16 (max)	*	*	Bits
ANALOG INPUTS				
Voltage Ranges				
Bipolar	±2.5, ±5, ±10	*	*	Volts
Unipolar	0 to +5, 0 to +10, 0 to +20	*	*	Volts
Impedance (Direct Input)				
0 to +5V, ±2.5V	2.5	*	*	kΩ
0 to +10V, ±5.0V	5	*	*	kΩ
0 to +20V, ±10V	10	*	*	kΩ
DIGITAL INPUTS[1]				
Convert Command	Positive Pulse 150ns Wide (min) Trailing Edge Initiates Conversion			
Logic Loading	1 (max)	*	*	TTL Load
TRANSFER CHARACTERISTICS				
ACCURACY				
Gain Error	±0.1[2] (±0.2 max)	*	*	%
Offset Error				
Unipolar	±0.05[2] (±0.1 max)	*	*	% of FSR[3]
Bipolar	±0.1[2] (±0.2 max)	*	*	% of FSR
Linearity Error (max)	±0.006 (J)	±0.006 (J)	±0.006 (A)	% of FSR
	±0.003 (K)	±0.003 (K)	±0.003 (B)	% of FSR
Inherent Quantization Error	±1/2	*	*	LSB
Differential Linearity Error	±0.003	*	*	% of FSR
No Missing Codes @ 25°C[4]	To 14 Bits (K Grade)	*	To 14 Bits (B Grade)	Guaranteed
POWER SUPPLY SENSITIVITY				
±15V dc	0.003	*	*	% of FSR/% ΔV_S
+5V dc	0.001	*	*	% of FSR/% ΔV_S
CONVERSION TIME[5] (14 BITS)	45 (50 max)	*	*	µs
WARM-UP TIME	5 (min)	*	*	Minutes
DRIFT				
Gain	±15 (max)	±10 (±20 max)	+7 (±15 max)	ppm/°C
Offset				
Unipolar	±2 (±4 max)	±2 (±4 max)	±2 max	ppm of FSR/°C
Bipolar	±10 (max)	±8 (±10 max)	±5 (±10 max)	ppm of FSR/°C
Linearity	±2 (3 max)	±1.5 (2 max)	±1.0 (2 max)	ppm of FSR/°C
Guaranteed No Missing Code				
Temperature Range[4]				
71JW, 72JD, 72AD (13 Bits)	0 to 50	*	*	°C
71KW, 72KD, 72BD (14 Bits)	10 to 40	*	*	°C
DIGITAL OUTPUT[1]				
(All Codes Complementary)				
Parallel				
Output Codes[6]				
Unipolar	CSB	*	*	
Bipolar	COB, CTC[7]	*	*	
Output Drive	2	*	*	TTL Loads
Serial Data Code (NRZ)	CSB, COB	*	*	
Output Drive	2	*	*	TTL Loads
Status	Logic "1" During Conversion			
Status Output Drive	2 (max)	*	*	TTL Loads
Internal Clock				
Clock Output Drive	2 (max)	*	*	TTL Loads
Frequency	280	*	*	kHz
INTERNAL REFERENCE VOLTAGE	6.3	*	*	V dc
Error	±5 max	*	*	%
Max External Current Drain				
With no Degradation of Specs	±200 max	*	*	µA
Temperature Coefficent	±10 max	*	±5 max	ppm/°C
POWER SUPPLY REQUIREMENTS				
Power Consumption	0.85	*	*	W
Rated Voltage, Analog	±15 ±0.5 max	*	*	V dc
Rated Voltage, Digital	+5 ±0.25 max	*	*	V dc
Supply Drain +15V dc	+20	*	*	mA
Supply Drain −15V dc	−20	*	*	mA
Supply Drain +5V dc	+70	*	*	mA
TEMPERATURE RANGE				
Specification	0 to +70	*	−25 to +85	°C
Operating (Derated Specs)	−25 to +85	*	−25 to +125	°C
Storage	−55 to +125	*	*	°C

NOTES
[1] Logic "0" = 0.8V, max. Logic "1" = 2.0V, min for inputs. For digital outputs Logic "0" = +0.4V max. Logic "1" = 2.4V min.
[2] Adjustable to zero.
[3] Full Scale Range.
[4] For definition of "No Missing Codes", refer to Theory of Operation.
[5] Conversion time may be shortened with "Short Cycle" set for lower resolution.
[6] CSB – Complementary Straight Binary. COB – Complementary Offset Binary. CTC – Complementary Two's Complement.
[7] CTC coding obtained by inverting MSB (Pin 1).

*Specifications same as AD ADC71JM, KM.
Specifications subject to change without notice.

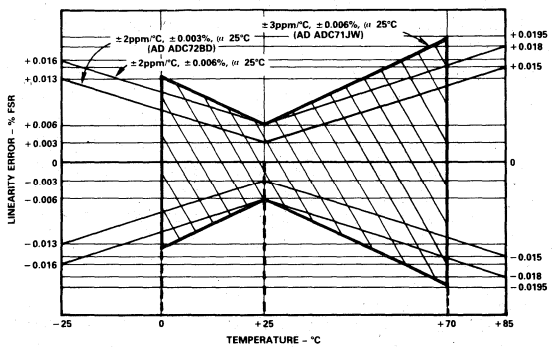


Figure 1. Linearity Error vs. Temperature

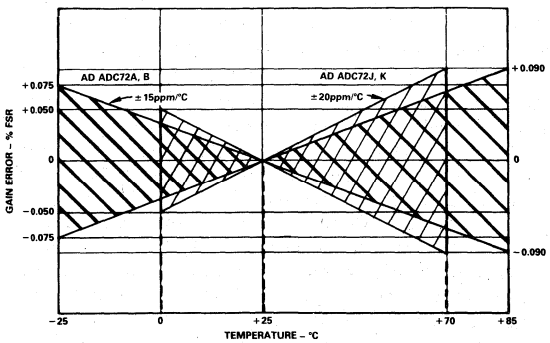


Figure 2. AD ADC72 Gain Drift Error vs. Temperature

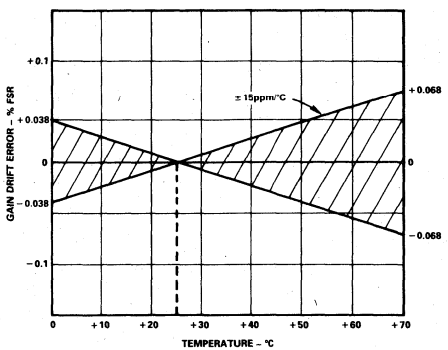


Figure 3. AD ADC71 Gain Drift Error vs. Temperature

ORDERING GUIDE

Model	Linearity Error (Max)	Specification Temp Range	Package Identification[1]
AD ADC71JM	±0.006% of FSR	0 to +70°C	HY32D
AD ADC71KM	±0.003% of FSR	0 to +70°C	HY32D
AD ADC72JM	±0.006% of FSR	0 to +70°C	HY32D
AD ADC72KM	±0.003% of FSR	0 to +70°C	HY32D
AD ADC72AM	±0.006% of FSR	−25°C to +85°C	HY32D
AD ADC72BM	±0.003% of FSR	−25°C to +85°C	HY32D

[1]See Section 19 for package outline information.

THEORY OF OPERATION

The analog continuum is partitioned into 2^{16} discrete ranges for 16-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of $\pm 1/2$LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of monolithic DACs that include the scaling network. The initial gain and offset errors are specified at $\pm 0.2\%$ FSR for gain and $\pm 0.1\%$ FSR for offset. These errors may be trimmed to zero by the use of external trim circuits as shown in Figures 5 and 7. Linearity error is defined for unipolar ranges as the deviation from a true straight line transfer characteristic from a zero voltage analog input, which calls for a zero digital output, to a point which is defined as a full scale. The linearity error is based on the DAC resistor ratios. It is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC71/AD ADC72 are specified as having no missing codes over temperature ranges as specified on the data page.

No Missing Code Definition for the AD ADC71 and AD ADC72:

A code is defined as being present and not missing if it is at least 0.2LSB wide and not overlapped by the adjacent codes including their noise when viewed on a dynamic cross plot. For testing details, please refer to the "ADC Testing" section in "Analog-Digital Conversion Notes", by Dan Sheingold, Analog Devices, Inc., 1977, Pages 211 through 215.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right on the diagram over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero for unipolar ranges or minus full scale point for bipolar ranges. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)

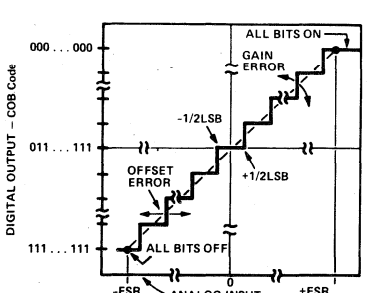


Figure 4. Transfer Characteristics for an Ideal Bipolar A/D

ϵ_O = Offset Drift Error (ppm of FSR/°C)

ϵ_L = Linearity Error (ppm of FSR/°C)

DESCRIPTION OF OPERATION

On receipt of a CONVERT START command, the AD ADC71/AD ADC72 converts the voltage at its analog input into an equivalent 16-bit binary number. This conversion is accomplished as follows: the 16-bit successive-approximation register (SAR) has its 16-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 6. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 16 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and $B_2 - B_{16}$ are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is reset unconditionally. This sequence continues until the Bit 16 (LSB) decision (keep) is made at t_{16}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the high Logic "0" state. Note that the clock remains high until the next conversion.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 6).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

GAIN ADJUSTMENT

The gain adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 510kΩ resistor to the gain adjust pin 29 as shown in Figure 5.

If no external trim adjustment is desired, pins 27 (offset adj) and pin 29 (gain adj) may be left open.

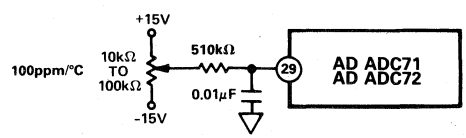


Figure 5. Gain Adjustment Circuit

OFFSET ADJUSTMENT

The zero adjust circuit consists of a 100ppm/°C potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 27 for all ranges. As shown in Figure 7, the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $32LSB_{14} \times 61ppm/LSB_{14} \times 1200ppm/°C = 2.3ppm/°C$ of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the

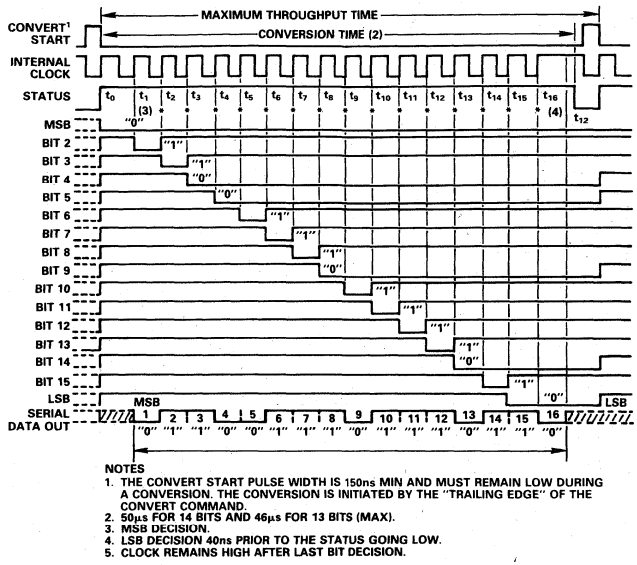


Figure 6. Timing Diagram (Binary Code 01100111011110110)

maximum offset adjustment required is typically no more than $\pm 16LSB_{14}$, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

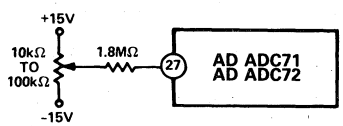


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100ppm/°C) are used, is shown in Figure 8.

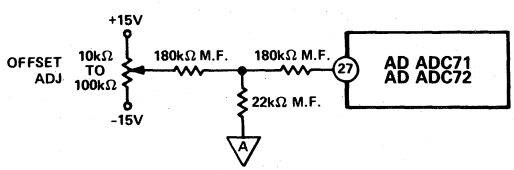


Figure 8. Low Tempco Zero Adjustment Circuit

In either adjust circuit, the fixed resistor connected to pin 27 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 27 is quite sensitive to external noise pick-up).

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form (Logic "1" = 0V and Logic "0" = 2.4V). Parallel data output coding is complementary binary for unipolar ranges and complementary offset binary for bipolar ranges. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 6. There are only 16 negative-going clock edges in the complete 16-bit conversion cycle. The first negative edge shifts an invalid bit into the register, which is shifted out on the last negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 32, permits the timing cycle shown in Figure 6 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 16-bit resolution. When 10-bit resolution is desired, pin 32 is connected to Bit 11 output pin 11. The conversion cycle then terminates and the STATUS flag resets after the Bit 10 decision (t_{10} + 40ns in timing diagram of Figure 6). Short cycle connections and associated maximum 8-, 10-, 12-, 13-, 14-, and 15-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 32 to Pin:	Resolution Bits	Resolution (%FSR)	Maximum Conversion Time (µs)	Status Flag Reset
16	15	0.003	53.5	t_{16} + 40ns
15	14	0.006	50.0	t_{15} + 40ns
14	13	0.012	46.5	t_{14} + 40ns
13	12	0.024	42.8	t_{12} + 40ns
11	10	0.100	35.6	t_{10} + 40ns
9	8	0.390	28.5	t_8 + 40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC71 and AD ADC72 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 9 for circuit details.

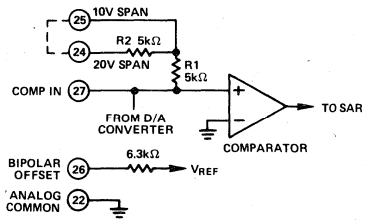


Figure 9. AD ADC71/AD ADC72 Input Scaling Circuit

Input Signal Line	Output Code	Connect Pin 26 to Pin	Connect Pin 24 to	For Direct Input, Connect Input Signal to
±10V	COB	27	Input Signal	24
±5V	COB	27	Open	25
±2.5V	COB	27	Pin 27	25
0V to +5V	CSB	22	Pin 27	25
0V to +10V	CSB	22	Pin 27	25
0V to +20V	CSB	22	Input Signal	24

Table II. AD ADC71/AD ADC72 Input Scaling Connections

Transition Values MSB LSB	Range	±10V	±5V	±2.5V	0 to +10V	0 to +5V
000 . . . 000*	+ Full Scale	+10V −3/2LSB	+5V −3/2LSB	+2.5V −3/2LSB	+10V −3/2LSB	+5V −3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	− Full Scale	−10V +1/2LSB	−5V +1/2LSB	−2.5V +1/2LSB	0V +1/2LSB	0V +1/2LSB

*Voltages given are the nominal value for transition to the code specified.
Note: For LSB value for range and resolution used, see Table IV.

Table III. Transition Values vs. Calibration Codes

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
	n = 13	2.44mV	1.22mV	0.61mV	1.22mV	0.61mV
	n = 14	1.22mV	0.61mV	0.31mV	0.61mV	0.31mV
	n = 15	0.61mV	0.31mV	0.15mV	0.31mV	0.15mV

NOTES
*COB = Complementary Offset Binary.
**CTC = Complementary Two's Complement – achieved by using an inverter to complement the most significant bit to produce ($\overline{MSB}$).
***CSB = Complementary Straight Binary.

Table IV. Input Voltage Range and LSB Values

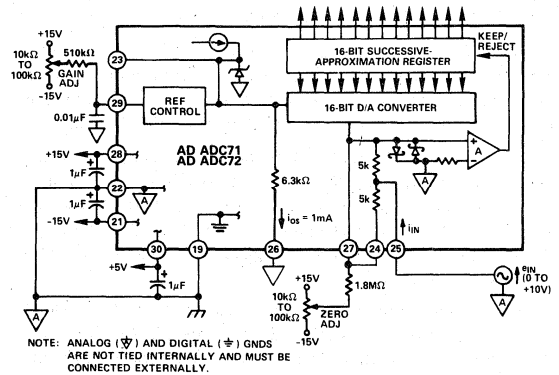


Figure 10. Analog and Power Connections for Unipolar 0 to +10V Input Range

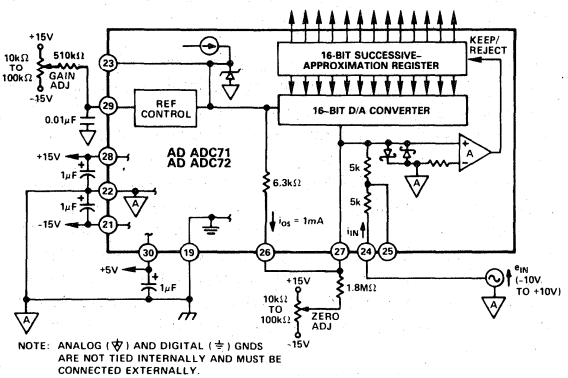


Figure 11. Analog and Power Connections for Bipolar +10V to +10V Input Range

CALIBRATION (14-Bit Resolution Examples)
External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figure 5 and 7, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and −FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to $+1LSB_{14}$ = 0.00061V. Adjust Zero for digital output = 11111111111110. Zero is now calibrated. Set analog input to +FSR − 2LSB = +9.9987V. Adjust Gain for 00000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.00000V; digital output code should be 01111111111111.

−10V to +10V Range: Set analog input to −9.99878V; adjust zero for 1111111111110 digital output (complementary offset binary) code. Set analog input to 9.99756V; adjust Gain for 00000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.00000V; digital output (complementary offset binary) code should be 01111111111111.

Other Ranges: Representative digital coding for 0 to +10V and −10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, −2.5V to +2.5V and −5V to +5V ranges can be found by halving proportionally the corresponding code equivalents listed for the 0 to +10V and −10V to +10V ranges, respectively, as indicated in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/2LSB using the static adjustment procedure described above. By summing a small sine or triangular wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

GROUNDING, DECOUPLING AND LAYOUT CONSIDERATIONS
Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return) and Analog Signal Ground. These grounds (pins 19 and 22) must be tied together at one point for the AD ADC71/AD ADC72 as close as possible to the converter. Ideally, a single solid analog ground plane under the converter would be desirable. Current flows through the wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system analog ground point and the ground pins of the AD ADC71/AD ADC72. Separate wide conductor stripe ground returns should be provided for high resolution converters to minimize noise and IR losses from the current flow in the path from the converter to the system ground point. In this way AD ADC71/AD ADC72 supply currents and other digital logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC71/AD ADC72's supply terminals should be capacitively decoupled as close to the AD ADC71/AD ADC72s as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are to be bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

The metal case is floating with respect to the power supplies, grounds and electrical signals. It must remain floating to perform to specifications. Do not ground the case. Glass beads standoff on the bottom will prevent shorting to board circuitry beneath the unit.

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The AD389 is a companion T/H designed for use with the AD ADC71/72 family. The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input which is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(\text{Full Scale Voltage})\ (2\pi)\ (\text{Aperture Jitter})}$$

For an application with a 14-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-14}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 24\text{kHz}$$

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 97\text{kHz}$$

Note that some additional aperture delay and jitter are added if the AD389 is not driven directly from the convert start line, but from the status line, which from some converters is delayed.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ±10V input range.

The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 50μs 14-bit A/D converter, the maximum droop rate will be 610μV/50μs or 12μV/μs dring the 50μs conversion period.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects.

The linearity error should be less than 1LSB over the transfer function,as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment. Thus, the ADC71 or ADC72 used with a companion AD389T/H offers high accuracy sampling in high precision applications.

Spec	14 Bit	16 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.6	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−96.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	10.2	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	3.0	0.1	μV/μs
Acquisition Time (to ±1LSB max) for 20kHz Signal w/15μs ADC	10	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−96.3	−86	dB
Gain Temperature Coefficient (max) for ±10°C Ambient Operation	6.1	1.5	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.3	0.1	mV
Linearity Error (max)	±0.0061	0.0015	0.003	%FSR

Table V. T/H Amplifier Requirements vs. AD389 Specs

AD389 in Combination With an	Throughput Rate	Input Frequency Range
AD ADC71 (13 bit)	22.2kHz	dc to 11.1kHz
AD ADC72 (14 bit)	16.7kHz	dc to 8.3kHz

Table VI. T/H & ADC Combinations and Maximum Throughput Rate

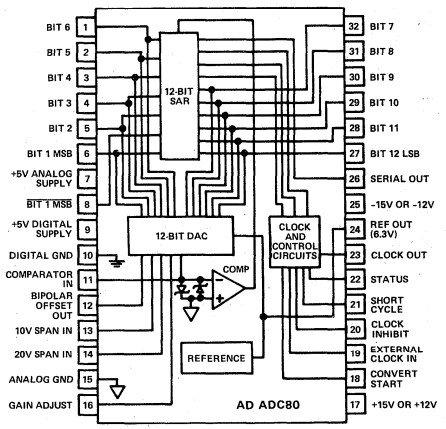
12-Bit Successive Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

True 12-Bit Operation: Max Nonlinearity ±0.012%
Low Gain T.C.: ±30ppm/°C max
Low Power: 800mW
Fast Conversion Time: 25μs
Precision 6.3V Reference for External Application
Short-Cycle Capability
Serial or Parallel Data Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count--High Reliability
Industry Standard Pinout
"Z" Models for ±12V Supplies

AD ADC80 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at +25°C of ±0.012%, max gain T.C. of 30ppm/°C, typical power dissipation of 800mW and max conversion time of 25μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of -25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5, ±5.0, ±10, 0 to +5 or 0 to +10 volts. The 6.3V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data may be read in both serial and parallel form.

The AD ADC80 is available in two performance grades, the AD ADC80-12 (0.012% of FSR max) and the AD ADC80-10 (0.048% of FSR max). Both grades are specified for use over the -25°C to +85°C temperature range and both are available in a 32-pin ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried zener reference is laser trimmed to 6.3 volts. The reference voltage is available externally and can supply up to 1.5mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC80-12	AD ADC80-10
RESOLUTION	12 Bits	10 Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5V, ±5V, ±10V	
Unipolar	0V to +5V, 0V to +10V	
Impedance (Direct Input)		
0V to +5V, ±2.5V	2.5kΩ	*
0V to +10V, ±5V	5kΩ	*
±10V	10kΩ	*
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100ns Wide (min) ("0" to "1" Initiates Conversion)	
Logic Loading	1TTL Load	
External Clock	1TTL Load	
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1% of FSR[3]	*
Offset Error[2]		
Unipolar	±0.05% of FSR	*
Bipolar	±0.1% of FSR	*
Linearity Error (max)[4]	±0.012% of FSR	±0.048% of FSR
Inherent Quantization Error	±1/2LSB	*
Differential Linearity Error	±1/2LSB	*
No Missing Codes Temperature Range	-25°C to +85°C	*
Power Supply Sensitivity		
±15V	±0.0030% of FSR/% V_S	*
+5V	±0.0015% of FSR/% V_S	*
DRIFT		
Specification Temperature Range	-25°C to +85°C	*
Gain (max)	±30ppm/°C	*
Offset		
Unipolar	±3ppm of FSR/°C	*
Bipolar (max)	±15ppm of FSR/°C	*
Linearity (max)	±3ppm of FSR/°C	*
Monotonicity	GUARANTEED	*
CONVERSION SPEED[5]	22μs typ, 25μs max	21μs max
DIGITAL OUTPUT		
(all codes complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2TTL Loads	
Serial Data Codes (NRZ)	CSB, COB	
Output Drive	2TTL Loads	
Status	Logic "1" During Conversion	
Status Output Drive	2TTL Loads	
Internal Clock		
Clock Output Drive	2TTL Loads	
Frequency[7]	575kHz	
INTERNAL REFERENCE VOLTAGE	6.3V ±10mV	
Max. External Current (with no degradation of specifications)	1.5mA	
Tempco of Drift	±10ppm/°C typ, ±20ppm/°C max	
POWER REQUIREMENTS		
Rated Voltages	±15V, +5V	
Range for Rated Accuracy	4.75V to 5.25V and ±14.0V to ±16.0V	
Z Models[8]	4.75V to 5.25V and ±11.4V to ±16.0V	
Supply Drain +15V	+10mA	
-15V	-20mA	
+5V	+70mA	
TEMPERATURE RANGE		
Specification	-25°C to +85°C	
Operating (Derated Specs)	-55°C to +100°C	
Storage	-55°C to +125°C	

NOTES
[1] DTL/TTL compatible i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital inputs, Logic "0" = +0.4V max and "1" = 2.4V min digital outputs.
[2] Adjustable to zero with external trimpots.
[3] FSR means Full Scale Range—for example, unit connected for ±10V range has 20V FSR.
[4] Error shown is the same as ±1/2LSB max for resolution of A/D converter.
[5] Conversion time with internal clock.
[6] See Table 1. CSB – Complementary Straight Binary
COB – Complementary Offset Binary
CTC – Complementary Two's Complement
[7] For conversion speeds specified.
[8] For Z models order AD ADC80Z-12 or AD ADC80Z-10.
*Specifications same as AD ADC80-12.

Specifications subject to change without notice.

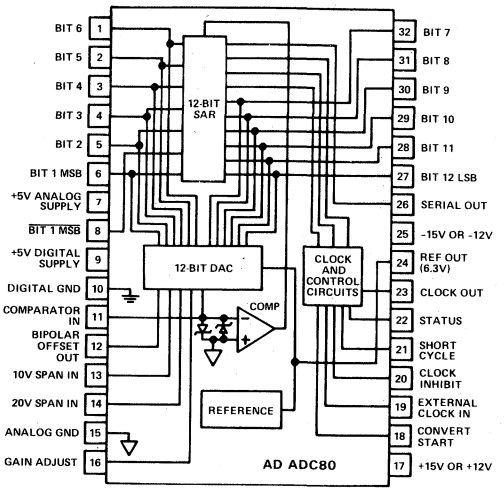


Figure 1. AD ADC80 Functional Diagram and Pinout

ORDERING GUIDE

Model	Supplies	Package Option[1]
AD ADC80-10	±15V +5	HY32E
AD ADC80-Z-10	±12V, +5	HY32E
AD ADC80-12	±15V, +5	HY32E
AD ADC80-Z-12	±12V, +5	HY32E

[1] See Section 19 for package outline information.

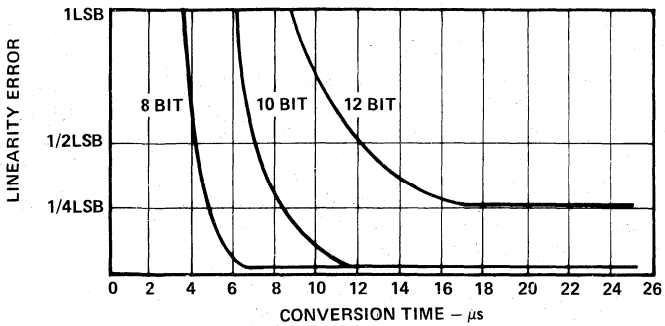


Figure 2. Linearity Error vs. Conversion Time (Normalized)

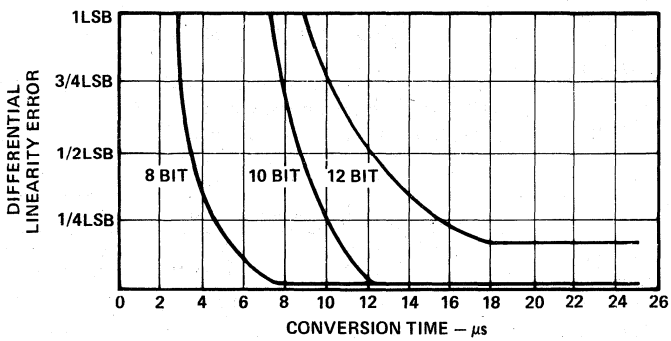


Figure 3. Differential Linearity Error vs. Conversion Time (Normalized)

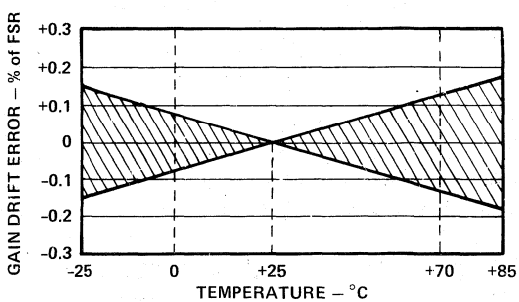


Figure 4. Maximum Gain Drift Error – % of FSR vs. Temperature

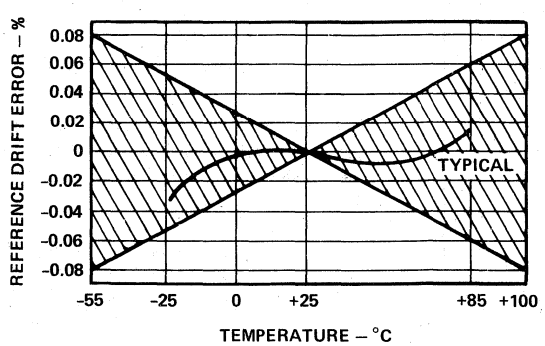


Figure 5. Reference Drift – % Error vs. Temperature

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the AD ADC80 have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 7 and 9. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in staircase step width between codes from the ideal least significant bit step size (Figure 6).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC80 is specified as having no missing codes over the entire temperature range from -25°C to +85°C.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G{}^2 + \epsilon_O{}^2 + \epsilon_L{}^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

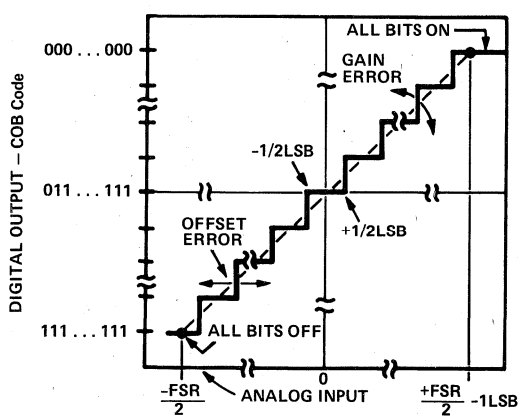


Figure 6. Transfer Characteristic for an Ideal Bipolar A/D

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8MΩ resistor to Comparator Input pin 11 for all ranges. As shown in Figure 7 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

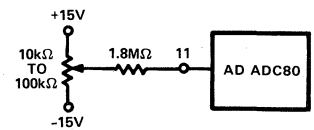


Figure 7. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 8.

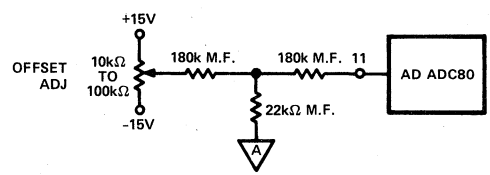


Figure 8. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 11 should be located close to this pin to keep the pin 11 connection runs short (Comparator Input pin 11 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10MΩ resistor to the gain adjust pin 16 as shown in Figure 9.

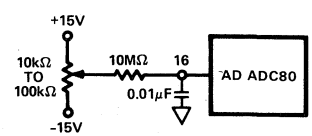


Figure 9. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 10.

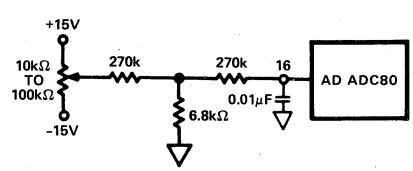


Figure 10. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

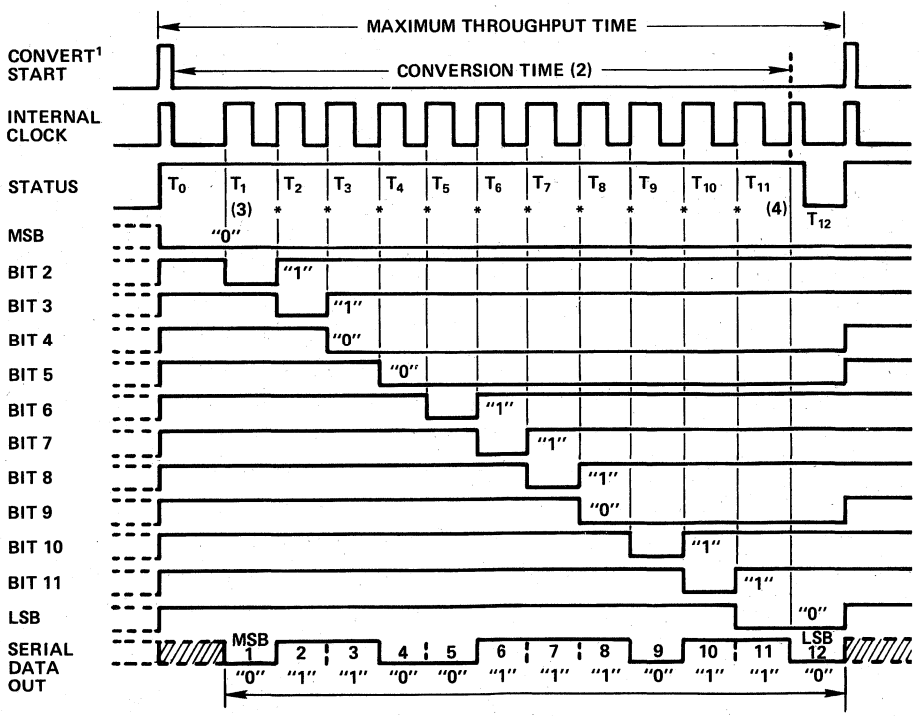
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 11. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 -B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 11).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND.
2. 25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW

*BIT DECISIONS

Figure 11. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 6) or its logical inverse BIT 1 (pin 8) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 11. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 11. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 21, permits the timing cycle shown in Figure 11 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, pin 21 is connected to Bit 11 output pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 11). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I. When 12-bit resolution is required, pin 21 is connected to +5V (pin 9).

Connect Short Cycle Pin 21 to Pin:	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} +40ns
28	10	0.100	21	t_{10} +40ns
30	8	0.390	17	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 12 for circuit details.

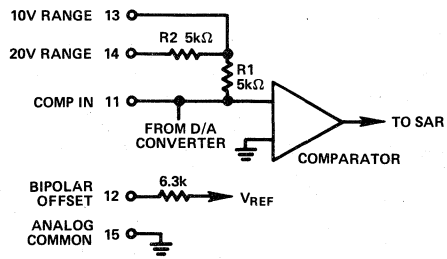


Figure 12. AD ADC80 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0V to +5V	CSB	15	Pin 11	13
0V to +10V	CSB	15	Open	13

Table II. AD ADC80 Input Scaling Connections

Binary (BIN) Output		INPUT VOLTAGE RANGE AND LSB VALUES				
Analog Input Voltage Range	Defined As:	±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definitions

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point and the two device grounds should be tied together. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

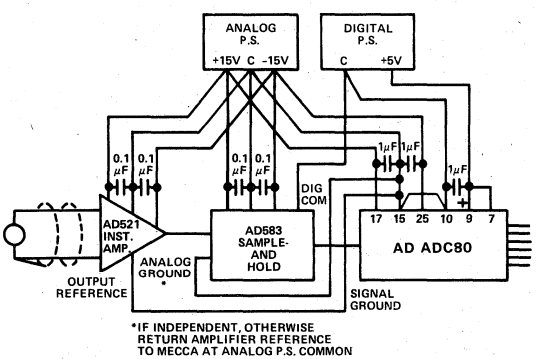


Figure 13. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 14–16.

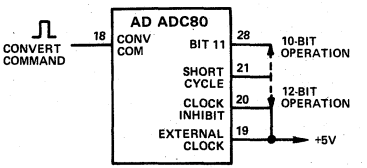


Figure 14. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

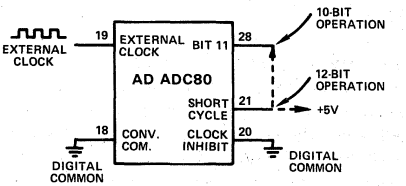


Figure 15. Continuous Conversion with External Clock. Conversion is Initiated by 14th Clock Pulse. Clock Runs Continuously.

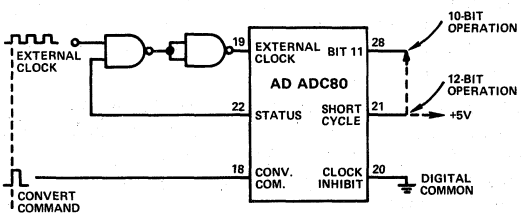


Figure 16. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command must be Synchronized with Clock.

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 17 and 18, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR –2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

–10V to +10V Range: Set analog input to –9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and –10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, –2.5V to +2.5V and –5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and –10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

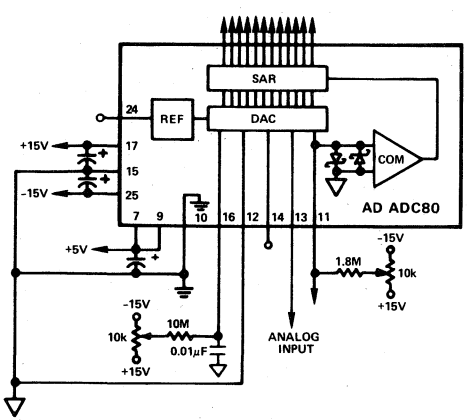


Figure 17. Analog and Power Connections for Unipolar 0–10V Input Range

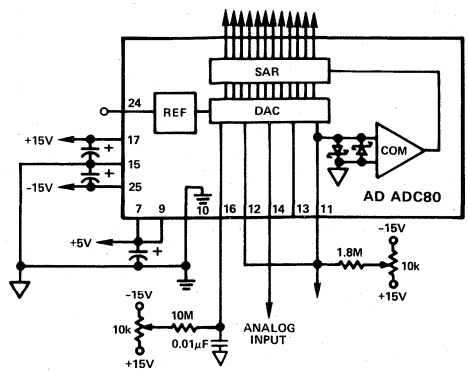


Figure 18. Analog and Power Connections for Bipolar ±10V Input Range

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 19 is a low cost solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

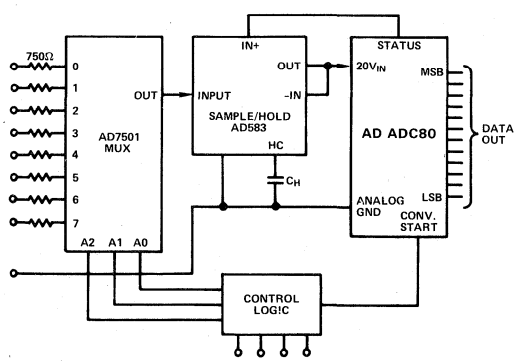


Figure 19. Data Acquisition System

ANALOG DEVICES

Fast, Complete 12-Bit A/D Converter

AD ADC84/AD ADC85

FEATURES

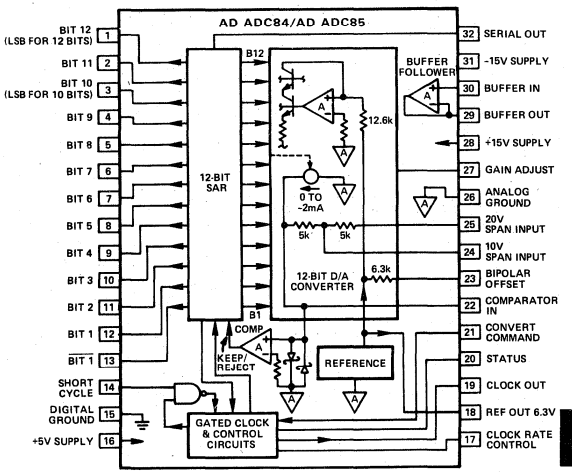
Performance

- Complete 12-Bit A/D Converter with Reference and Clock
- Fast Successive Approximation Conversion: 10μs
- Buried Zener Reference for Long Term Stability and Low Gain T.C.: 10ppm/°C
- Max Nonlinearity: <±0.012%
- Low Power: 880mW Typical
- Hermetic Package Available
- Low Chip Count – High Reliability
- Industry Standard Pin Out
- "Z" Models for ±12V Operation Available
- Extended Temperature Range -55°C to +125°C

Versatility

- Negative-True Parallel or Serial Logic Outputs
- Short Cycle Capability
- Precision +6.3V Reference for External Applications

AD ADC84/AD ADC85 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD ADC84/AD ADC85 series devices are high speed low cost 10- and 12-bit successive approximation analog-to-digital converters that include an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD ADC84/AD ADC85 series include a maximum linearity error at +25°C of ±0.012%, gain T.C. below 15ppm/°C, typical power dissipation of 880mW, and conversion time of less than 10μs for the 12-bit versions. Of considerable significance in severe and aerospace applications is the guaranteed performance from -55°C to +125°C of the AD ADC85S which is also available with environmental screening. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to +70°C, -25°C to +85°C, and -55°C to +125°C.

The design of the AD ADC84/AD ADC85 includes scaling resistors that provide analog input signal ranges of ±2.5, ±5, ±10, 0 to +5, or 0 to +10 volts. Adding flexibility and value are the +6.3V precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is negative-true and available in either serial or parallel form.

The AD ADC84/AD ADC85 series devices are available in two different performance grades. The devices are specified for either 10-bit accuracy (±0.048% FSR max) or 12-bit accuracy (±0.012% FSR max) with 6μs, 10μs max conversion times respectively.

The AD ADC84 and AD ADC85C specified for operation over the 0 to +70°C temperature range. The AD ADC85 and AD ADC85S are specified for the -25°C to +85°C, -55°C to +125°C ranges respectively.

PRODUCT HIGHLIGHTS

1. The AD ADC84/AD ADC85 series devices are complete 12-bit A/D converters. No external components are required to perform a conversion.
2. The AD ADC84/AD ADC85 directly replaces other devices of this type with significant increases in performance.
3. The fast conversion rate of the AD ADC84/AD ADC85 makes it an excellent choice for applications requiring high system throughput rates.
4. The internal buried zener reference is laser trimmed to 6.3V ±0.1% and ±10ppm/°C typical T.C. The reference is available externally and can provide up to 1mA.
5. The integrated package construction provides high quality and reliability with small size and weight.
6. The monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD ADC84	AD ADC85C	AD ADC85	AD ADC85S	UNITS
RESOLUTION	10/12	10/12	10/12	10/12	Bits
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±2.5, ±5, ±10	*	*	*	Volts
Unipolar	0 to +5, 0 to +10	*	*	*	Volts
Impedance (Direct Input)					
0V to +5V, ±2.5V	2.5(±20%)	*	*	*	kΩ
0V to +10V, ±5V	5(±20%)	*	*	*	kΩ
±10V	10(±20%)	*	*	*	kΩ
Buffer Amplifier[1]					
Impedance (min)	100	*	*	*	MΩ
Bias Current	50	*	*	*	nA
Settling Time					
To 0.01% for 20V Step	2	*	*	*	μs
DIGITAL INPUTS[2]					
Convert Command	Positive Pulse 50ns min Trailing Edge Initiates Conversion	*	*	*	
Logic Loading	1	*	*	*	TTL Load
TRANSFER CHARACTERISTICS ERROR					
Gain Error[3]	±0.1(±0.25% max)	*	*	*	%
Offset Error[3]	Adjustable to Zero	*	*	*	
Unipolar	±0.05(±0.2% max)	*	*	*	% of FSR[4]
Bipolar[5]	±0.1(±0.25% max)	*	*	*	% of FSR
Linearity Error (max)[6]	±0.048/±0.012	*	*	*	% of FSR
Inherent Quantization Error	±0.5	*	*	*	LSB
Differential Linearity Error	±0.5	*	*	*	LSB
No Missing Codes Temperature Range	0 to +70	0 to +70	−25 to +85	−55 to +125	°C
Power Supply Sensitivity					
±15V	±0.004	*	*	*	% of FSR/%V
+5V	±0.001	*	*	*	% of FSR/%V
DRIFT					
Specification Temperature Range	0 to +70	*	−25 to +85	−55 to +125	°C
Gain (max)	±30	±40/±25	±20/±15	±25	ppm/°C
Offset					
Unipolar	±3	*	*	±5 max	ppm/°C
Bipolar (max)[5]	±15	±20/±12	±10/±7	±10	ppm/°C
Linearity (max)	±3	*	±3/±2	*	ppm/°C
Monotonicity	GUARANTEED	*	*	*	
CONVERSION SPEED (MAX)	6/10	*	*	*	μs
DIGITAL OUTPUT					
(all codes complementary)					
Parallel					
Output Codes[7]					
Unipolar	CSB	*	*	*	
Bipolar	COB, CTC	*	*	*	
Output Drive	2	*	*	*	TTL Loads
Serial Data Codes (NRZ)	CSB, COB	*	*	*	
Output Drive	2	*	*	*	TTL Loads
Status	Logic "1" during Conversion	*	*	*	
Status Output Drive	2	*	*	*	TTL Loads
Internal Clock					
Clock Output Drive	2	*	*	*	TTL Loads
Frequency	1.9/1.22	*	*	*	MHz
INTERNAL REFERENCE VOLTAGE	6.3/±15mV max	*	*	*	Volts
Max. External Current (with no degradation of specifications)	1.0	*	*	*	mA
Tempco of Drift, (max)	±20/max	±10 typ	±5 typ	±5 typ	ppm/°C
POWER REQUIREMENTS					
Rated Voltages	+5, ±15	*	*	*	Volts
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	Volts
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.5	*	*	*	Volts
Supply Drain +15V	25 max	*	*	*	mA
−15V	30 max	*	*	*	mA
+5V	100 max	*	*	*	mA
Total Power Dissipation	1100 max	*	*	*	mW
TEMPERATURE RANGE					
Specification	0 to +70	*	−25 to +85	−55 to +125	°C
Operating (Derated Specs)	−25 to +85	*	−55 to +125	−55 to +125	°C
Storage	−55 to +125	*	*	*	°C
PACKAGE	Ceramic	Hermetic Ceramic	Hermetic Ceramic	Hermetic Ceramic	

NOTES

[1] Buffer Settling time adds to conversion speed when buffer is connected to input.

[2] DTL/TTL compatible Logic "0" = 0.8V max, Logic "1" = 2.0V min for digital output, Logic "0" = 0.4V max, Logic "1" = 2.4V min.

[3] Adjustable to zero.

[4] FSR means Full Scale Range.

[5] Guaranteed at V_{IN} = 0 volts.

[6] Error shown is the same as ±1/2LSB max error in % of FSR.

[7] See Table I.

[8] For ±12V operation add "Z" to model number. Input range limited to a maximum of ±5V.

*Specifications same as AD ADC84.

Specifications subject to change without notice.

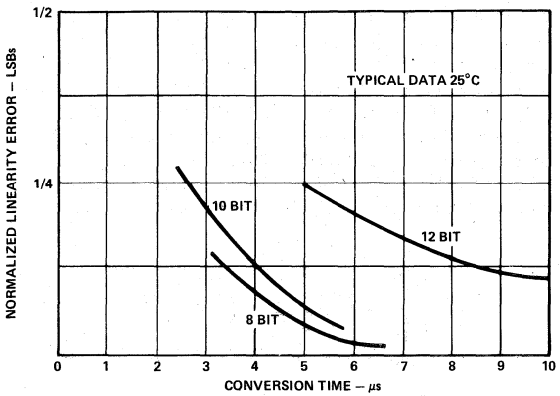


Figure 1. Linearity Error vs. Conversion Speed

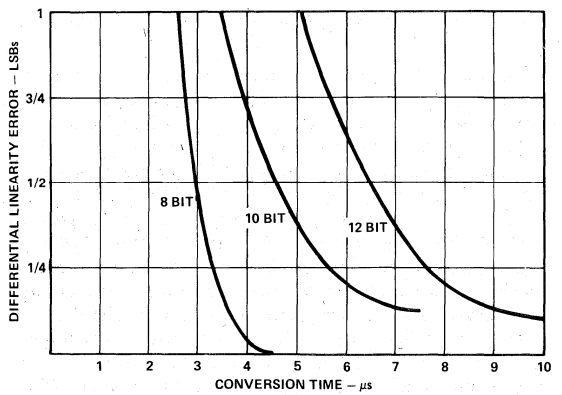


Figure 2. Change in Differential Linearity vs. Conversion Speed

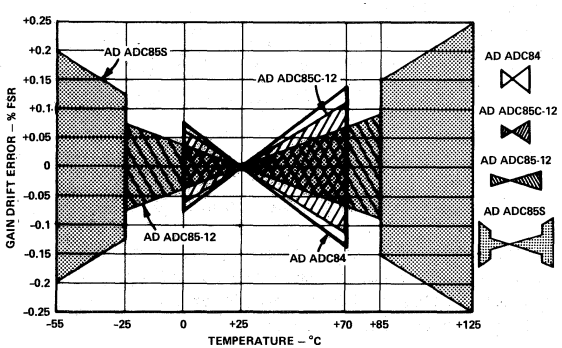


Figure 3. Gain Drift Error (% FSR) vs. Temperature

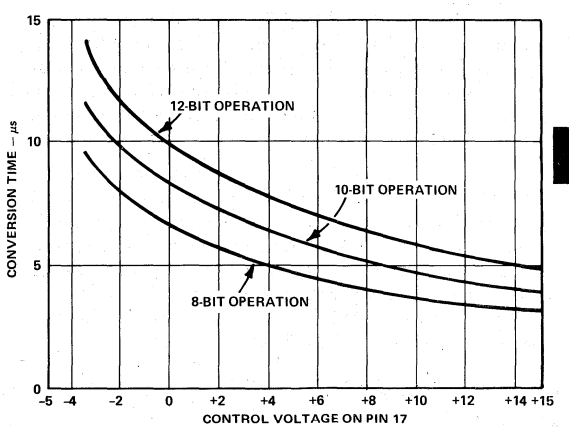


Figure 4. Conversion Speed vs. Control Voltage

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ORDERING GUIDE

Model[1]	Linearity	Temperature Range	Package	Gain T. C. – ppm/°C	Package Outline[2]
AD ADC84-10	±0.048%	0 to +70°C	Ceramic	±30	HY32F
AD ADC84-12	±0.012%	0 to +70°C	Ceramic	±30	HY32F
AD ADC85C-10	±0.048%	0 to +70°C	Hermetic Ceramic	±40	HY32F
AD ADC85C-12	±0.012%	0 to +70°C	Hermetic Ceramic	±25	HY32F
AD ADC85-10	±0.048%	-25°C to +85°C	Hermetic Ceramic	±20	HY32F
AD ADC85-12	±0.012%	-25°C to +85°C	Hermetic Ceramic	±15	HY32F
AD ADC85S-10	±0.048%	-55°C to +125°C	Hermetic Ceramic	±25	HY32F
AD ADC85S-12	±0.012%	-55°C to +125°C	Hermetic Ceramic	±25	HY32F

NOTES

[1] For complete model number suffixes must be added for "Z" option (±12V operation), linearity and military screening. The following guide shows the proper suffix order.
AD ADC(*)(**)-(***)

*Model Number
**"Z" Version Designator
***Linearity

Typical Part Numbers
AD ADC84-12
AD ADC85SZ-12

[2] See Section 19 for package outline information.

The analog continuum is partitioned into 2^{12} discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors are specified at ±0.1% FSR for gain and ±0.05% FSR for offset. These errors may be trimmed to zero by the use of the external trim circuits as shown in Figures 6 and 8. Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 5).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD ADC84/AD ADC85 are specified as having no missing codes over the entire temperature range as specified on the data page.

There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$RSS = \sqrt{\epsilon_G^2 + \epsilon_O^2 + \epsilon_L^2}$$

ϵ_G = Gain Drift Error (ppm/°C)
ϵ_O = Offset Drift Error (ppm of FSR/°C)
ϵ_L = Linearity Error (ppm of FSR/°C)

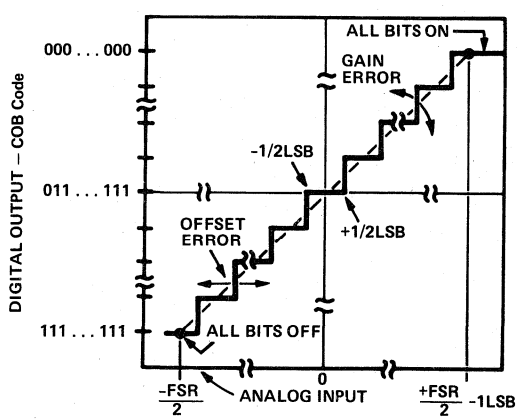


Figure 5. Transfer Characteristics for an Ideal Bipolar A/D

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across ±V_S with its slider connected through a 1.8MΩ resistor to Comparator Input pin 22 for all ranges. As shown in Figure 6 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a -1200ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ppm/°C = 2.3ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4LSB, use of a carbon composition offset summing resistor typically contributes no more than 1ppm/°C of FSR offset tempco.

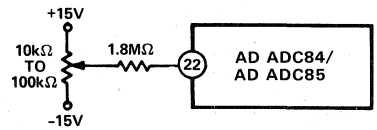


Figure 6. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 7.

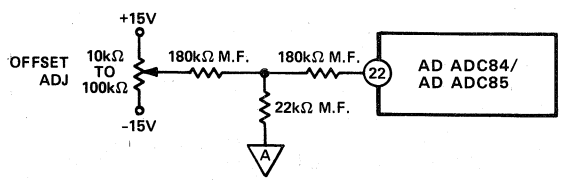


Figure 7. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin connection runs short (Comparator Input pin 22 is quite sensitive to external noise pick-up).

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across ±V_S with its slider connected through a 10MΩ resistor to the gain adjust pin 27 as shown in Figure 8.

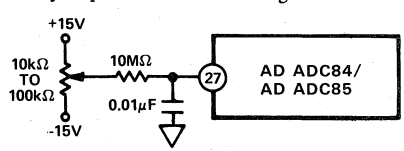


Figure 8. Gain Adjustment Circuit

An alternate gain adjust circuit which contributes negligible gain tempco if metal film resistors (Tempco <100ppm/°C) are used is shown in Figure 9.

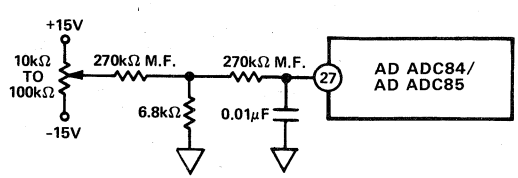


Figure 9. Low Tempco Gain Adjustment Circuit

THEORY OF OPERATION

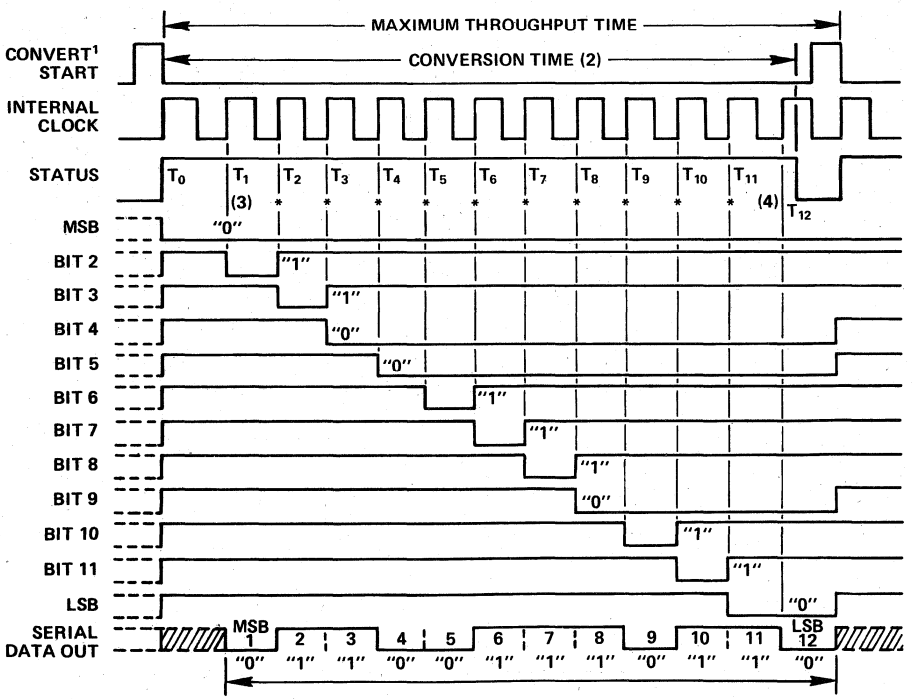
On receipt of a CONVERT START command, the AD ADC84/AD ADC85 converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 10. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All the SAR parallel bits, STATUS flip-flops, and the gated clock inhibit signal are initialized on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however; serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 10).

Incorporation of this 40ns delay guarantees that the parallel (and serial) data are valid at the Logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES:
1. THE CONVERT START PULSE WIDTH IS 50ns MIN AND MUST REMAIN LOW DURING A CONVERSION. THE CONVERSION IS INITIATED BY THE "TRAILING EDGE" OF THE CONVERT COMMAND.
2. 10μs FOR 12 BITS AND 6μs FOR 10 BITS (MAX).
3. MSB DECISION
4. LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW
*BIT DECISIONS

Figure 10. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Both parallel and serial data from TTL storage registers are in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary two's complement binary, depending on whether BIT 1 (pin 12) or its logical inverse $\overline{\text{BIT 1}}$ (pin 13) is used as the MSB. Parallel data becomes valid approximately 40ns before the STATUS flag returns to Logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is complementary binary for unipolar input ranges and complementary offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid 200ns after the rising clock edges, permitting serial data to be clocked directly into a receiving register on the negative-going clock edges as shown in Figure 10. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 10. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

Short Cycle Input: A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 10 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 14 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} +40ns in timing diagram of Figure 10). Short Cycle pin connections and associated maximum 12-, 10- and 8-bit conversion times are summarized in Table I.

Connect Short Cycle Pin 14 To Pin:	Connect Clock Rate Control Pin 17 To	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
16	15	12	0.024	10	t_{12} +40ns
2	16	10	0.100	6	t_{10} +40ns
4	28	8	0.390	3.2	t_8 +40ns

Table I. Short Cycle Connections

INPUT SCALING

The AD ADC84/AD ADC85 inputs should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 11 for circuit details.

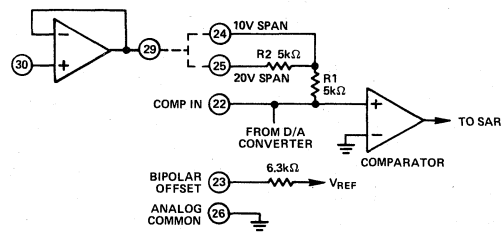


Figure 11. AD ADC84/AD ADC85 Input Scaling Circuit

Input Signal Range	Output Code	Connect Pin 23 To Pin	Connect Pin 25 To	For Direct Input Connect Input Signal To	For Buffered Input Pin 30 Connect Pin 29 To Pin
±10V	COB or CTC	22	Input Signal	25	25
±5V	COB or CTC	22	Open	24	24
±2.5V	COB or CTC	22	Pin 22	24	24
0V to +5V	CSB	26	Pin 22	24	24
0V to +10V	CSB	26	Open	24	24

Table II. AD ADC84/AD ADC85 Input Scaling Connections

INPUT VOLTAGE RANGE AND LSB VALUES

Analog Input Voltage Range		±10V	±5V	±2.5V	0V to +10V	0V to +5V
Code Designation		COB* or CTC**	COB* or CTC**	COB* or CTC**	CSB***	CSB***
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000 . . . 000****	+Full Scale	+10V -3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011 . . . 111	Mid Scale	0	0	0	+5V	+2.5V
111 . . . 110	-Full Scale	-10V +1/2LSB	-5V +1/2LSB	-2.5V +1/2LSB	0 + 1/2LSB	0 +1/2LSB

NOTES
*COB = Complementary Offset Binary
**CTC = Complementary Two's complement—obtained by using the complement of the most significant bit ($\overline{\text{MSB}}$). $\overline{\text{MSB}}$ is available to pin 13.
***CSB = Complementary Straight Binary.
****Voltages given are the nominal value for transition to the code specified.

Table III. Input Voltages and Code Definition

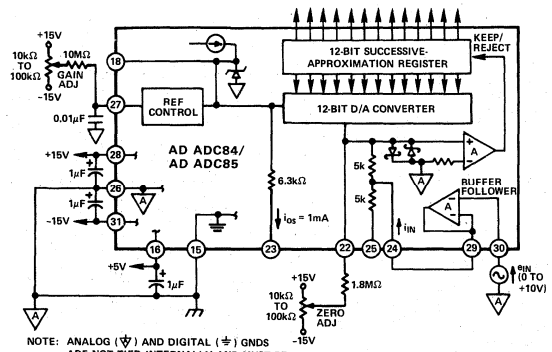


Figure 12. Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

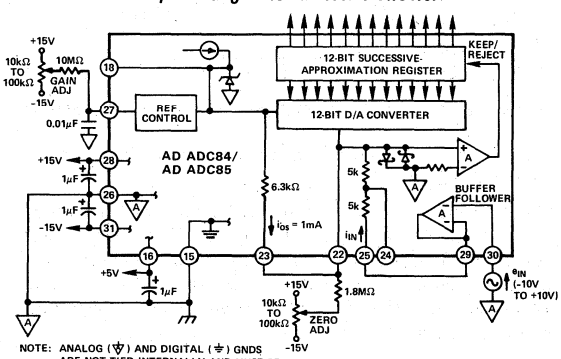


Figure 13. Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 12 and 13, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 000000000001 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 011111111111.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902V; adjust Gain for 000000000001 digital output (complementary offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (complementary offset binary) code should be 0111111111111.

Other Ranges: Representative digital coding for 0 to +10V and -10V to +10V ranges is given above. Coding relationships and calibration points for 0 to +5V, -2.5V to +2.5V and -5V to +5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -10V to +10V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 4.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC84/AD ADC85. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC84/AD ADC85's supply terminals should be capacitively decoupled as close to the AD ADC84/ AD ADC85 as possible. A large value capacitor such as 1μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

CLOCK RATE CONTROL ALTERNATE CONNECTIONS

If adjustment of the CLOCK RATE is desired for faster conversion speeds, the CLOCK RATE CONTROL may be connected to an external multi-turn trim potentiomer with a TCR of ±100ppm/°C or less as shown in Figures 14 and 15. If the potentiometer is connected to -15V, conversion time can be increased as shown in Figure 10. If these adjustments are used, delete the connections shown in Table I for pin 17. See Figure 1 for nonlinearity error vs. conversion speed and Figure 4 for the effect of the control voltage on clock speed.

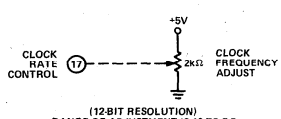


Figure 14. 12-Bit Clock Rate Control Optional Fine Adjust

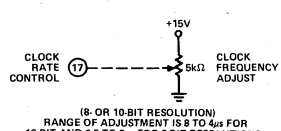


Figure 15. 8-Bit Clock Rate Control Optional Fine Adjust

10

MICROPROCESSOR INTERFACING

The 10μs conversion time of the ADC84/ADC85 suggests several different methods of interface to microprocessors. In systems where the AD ADC84/AD ADC85 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSB's reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSB's in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 7 shows a typical connection to an 8085-type bus, using a left-justified data format for unipolar inputs. Status polling is optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD ADC84/AD ADC85 should be reversed, as well

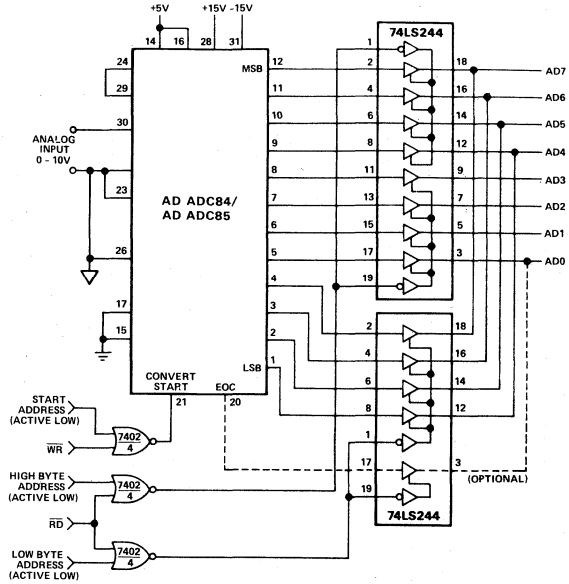


Figure 16. AD ADC84/ADC85-8085A Interface Connection

as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs (±5V, ±10V ranges), using the MSB directly yields a complementary offset binary-coded output. If complementary two's complement coding is desired, it can be produced by substituting $\overline{MSB}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

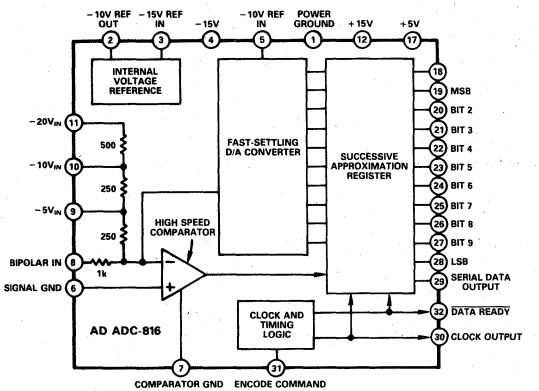
Ultra High Speed 10-Bit A/D Converters

AD ADC-816

FEATURES
10-Bit Resolution
800ns Conversion Time
Six Input Ranges
Unipolar and Bipolar Operation

APPLICATIONS
Data Acquisition Systems
Radar Systems
Analytical Instruments
Real-Time Waveform Analysis

AD ADC-816 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD ADC-816 A/D Converter is an ultra high speed successive approximation converter capable of 10 bits of resolution with a conversion time of only 800ns.

It is a thin-film hybrid, packaged in a 32-pin DIP. Three different models offer temperature ranges of 0 to +70°C, −25°C to +85°C, and −55°C to +125°C.

The design offers the user flexibility in both input and output configurations. Six different analog inputs are available with strap options: 0V to −5V; 0V to −10V; 0V to −20V; ±2.5V; ±5V; and ±10V. Output data are available in either serial or parallel format, also with external connections.

The AD ADC-816 can be incorporated into a wide variety of circuit and system applications with a minimum of external components and design effort. When used with the HTC-0300, HTC-0300A, HTC-0500, or other Analog Devices' high-performance track-and-hold units, the AD ADC-816 A/D can be a cost-effective solution for a broad range of digitizing problems.

Model number suffixes designate the various temperature ranges. The AD ADC-816KD operates over a range of 0 to +70°C; the AD ADC-816BD is for −25°C to +85°C; and the AD ADC-816SD is for use in operating environments between −55°C and +125°C.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	POWER GROUND	17	+5V POWER
2	−10V REFERENCE OUT	18	MSB (BIT 1)
3	−15V REFERENCE IN	19	MSB (BIT 1)
4	−15V POWER	20	BIT 2
5	−10V REFERENCE IN	21	BIT 3
6	SIGNAL GROUND	22	BIT 4
7	COMPARATOR GROUND	23	BIT 5
8	BIPOLAR INPUT	24	BIT 6
9	−5V ANALOG INPUT	25	BIT 7
10	−10V ANALOG INPUT	26	BIT 8
11	−20V ANALOG INPUT	27	BIT 9
12	+15V POWER	28	LSB (BIT 10)
13	NC	29	SERIAL DATA OUT
14	NC	30	CLOCK OUTPUT
15	NC	31	ENCODE COMMAND
16	NC	32	DATA READY OUTPUT

POWER GROUND (PIN 1), SIGNAL GROUND (PIN 6), AND COMPARATOR GROUND (PIN 7) MUST BE CONNECTED TOGETHER AND TO LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE.

10

SPECIFICATIONS

Parameter	Units	AD ADC-816KD	AD ADC-816BD
RESOLUTION	Bits	10	*
(FS = Full Scale)	%FS	0.1	*
LSB WEIGHT			
5V/10V/20V p-p FS	mV	4.88/9.76/19.53	*
ACCURACY			
Nonlinearity	LSB, max	±1/2	*
Differential Nonlinearity[1]	LSB, max	±1/2	*
Monotonicity		Guaranteed	*
DYNAMIC CHARACTERISTICS			
Conversion Time	ns, max[2]	800	*
Conversion Rate	MHz	1.25	*
ANALOG INPUT			
Voltage Ranges			
Unipolar[3]	V, p-p FS	5, 10, or 20	*
Bipolar	V, p-p FS	±2.5, 5, or 10	*
Reference			
Pin 5	V (max)	−10 (±0.5)	*
Impedance			
Unipolar 5V Input	Ω	250	*
Unipolar 10V Input	Ω	500	*
Unipolar 20V Input	Ω	1000	*
Bipolar Input	Ω	1000	*
Reference	Ω	2000	*
Zero Error Before Adjustment			
Unipolar	% of FS	0.2	*
Offset Error Before Adjustment			
Bipolar	% of FS	0.1	*
Gain Error Before Adjustment			
Unipolar/Bipolar	% of FS	0.3/0.2	*
Reference Output Tempco	ppm/°C max	±20	*
ENCODE COMMAND INPUT[4]			
Logic Levels,	V (max)	"0" = +0.4 (+0.8)	*
TTL-Compatible	V, min (max)	"1" = +2.0 (+5.5)	*
Loading	TTL Loads	1	*
Rise and Fall Times	ns	10	*
Width	ns, min	50	*
Frequency	MHz	1.25	*
DIGITAL OUTPUT			
Parallel			
@ Pins 19–28 + Pin 18	Bits	11 (10 + $\overline{\text{MSB}}$)	*
Time Skew	ns, max	5	*
Format	Non-Return-to-Zero (NRZ)		*
Series			
@ Pin 29	Bits	11 (10 + $\overline{\text{MSB}}$)	*
Timing	Successive decision pulses with MSB ($\overline{\text{MSB}}$) first; at internal clock frequency		*
Format	Non-Return-to-Zero (NRZ)		*
Coding[5]			
Unipolar Input	Binary (BIN)	*	
Bipolar Input	Offset Binary (OBN) or		
2's Complement (2SC)[6]			*
Logic Levels,	V, max	"0" = +0.4	*
TTL-Compatible	V, min	"1" = +2.4	*
Loading	TTL Loads	2	*
CLOCK OUTPUT			
Format		Series Train	*
Amplitude			
Minimum	V	0	*
Maximum	V	+5	*
Width	ns	30	*
Frequency	MHz	14.3	*
REFERENCE OUTPUT[7]			
Voltage	V (max)	10 (±0.02)	*
Current (sink only)	mA	0 to +20	*
Impedance	Ohms, max	10	*
DATA READY OUTPUT			
Signal Status	Logic "1" during reset and conversion		*
	Logic "0" when conversion is complete		*
Logic Levels,	V, max	"0" = +0.4	*
TTL-Compatible	V, min	"1" = +2.4	*
Loading	TTL Loads	4	*
Rise and Fall Times	ns, max	5	*
POWER REQUIREMENTS[8]			
+15V ±0.5% (Pin 12, Power)	mA, max	105	*
−15V ±3% (Pin 4, Power)	mA, max	25	*
−15V ±3% (Pin 3, Reference)	mA, max	35	*
+5V ±5% (Pin 17)	mA, max	180	*
Power Consumption	W, max	3.4	*
Power Supply Rejection Ratio			
(PSSR) for Rated Supplies	%/%	Infinite	*
TEMPERATURE RANGE[9]			
Operating	°C	0 to +70	−25 to +85[10]
Storage	°C	−65 to +125	*
PACKAGE OPTION[11]		HY32A	

NOTES
[1]Tested over full rated operating temperature range.
[2]Measured from leading edge Encode Command to trailing edge Data Ready; use trailing edge to strobe output data into external circuits.
[3]Bipolar input (Pin 8) must be tied to ground.
[4]Logic "1" resets converter; logic "0" initiates conversion.
[5]All coding is inverted analog.
[6]Two's Complement available for parallel output only.
[7]To use internal reference, connect −15V REFERENCE IN (Pin 3) to −15V POWER (Pin 4); and −10V REFERENCE OUT (Pin 2) to −10V REFERENCE IN (Pin 5). To use external reference, leave Pins 2 and 3 open or grounded; connect external reference to Pin 5. If Pin 3 is left disconnected or grounded, internal reference is disabled and power decreases approximately 200mW.
[8]Bypass power supplies with 1μF electrolytic capacitors as close to supply pins as possible.
[9]Maximum junction temperature is +150°C. At temperatures above +70°C, cooling air at rate of 70 Linear Feet Per Minute (LFPM) is required.
[10]AD ADC-816SD operating temperature −55°C to +125°C.
[11]See Section 19 for package outline information.
*Specifications same as AD ADC-816KD.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Positive Supply (Pin 12) . . . . . +16V dc
Negative Supply (Pins 3 & 4) . . . . . −16V dc
Logic Supply (Pin 17) . . . . . +7V dc
Logic Inputs . . . . . +7V dc
Analog Inputs . . . . . ±2 × Selected Analog Input Range

ANALOG DEVICES

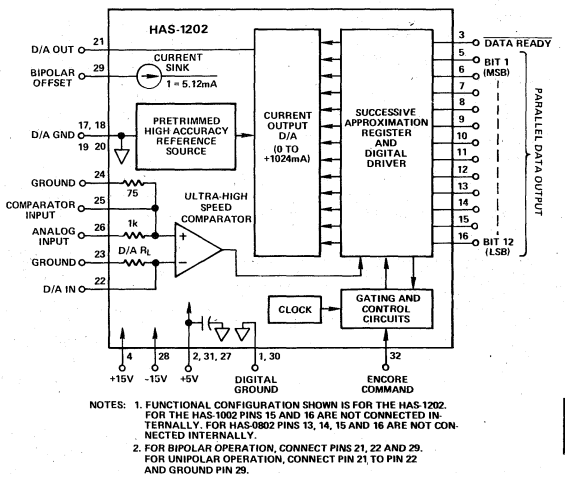
Ultra-Fast Hybrid Analog-to-Digital Converters

HAS-0802/1002/1202

FEATURES
Conversion Times as Low as 1.2μs
Resolution: 8, 10 and 12 Bits
Exceptional Accuracy, 0.012% of F.S.
Low Power
Contained in Glass or Metal 32-Pin DIP
Adjustment-Free Operation

APPLICATIONS
Waveform Analysis
Fast Fourier Transforms
Radar

HAS-0802/1002/1202 FUNCTIONAL BLOCK DIAGRAM



NOTES: 1. FUNCTIONAL CONFIGURATION SHOWN IS FOR THE HAS-1202. FOR THE HAS-1002 PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. FOR HAS-0802 PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.
2. FOR BIPOLAR OPERATION, CONNECT PINS 21, 22 AND 29. FOR UNIPOLAR OPERATION, CONNECT PIN 21 TO PIN 22 AND GROUND PIN 29.

10

GENERAL DESCRIPTION

With a typical conversion time of only 2.2μs for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are among the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.

SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

MODEL	UNITS	HAS-0802	HAS-1002	HAS-1202
RESOLUTION	BITS	8	10	12
LSB Weight	% Full Scale	0.4	0.1	0.025
	mV	40	10	2.5
RELATIVE ACCURACY (INCLUDING LINEARITY)	% Full Scale	0.05	0.025	0.012
Quantization Error	LSB	±1/2	*	*
LINEARITY VS. TEMPERATURE	ppm/°C	3	*	*
		(No Missing Codes over Temperature Range)		
INPUT OFFSET VOLTAGE				
Initial (Trimmable to Zero)	mV	10	*	*
Zero Offset vs. Temperature	μV/°C	15	*	*
Bipolar Offset vs. Temperature	μV/°C	100	*	*
GAIN ERROR				
Initial (Trimmable to Zero)	% Full Scale	0.1	*	*
Gain vs. Temperature	ppm/°C	30	*	*
INPUT				
Ranges (Full Scale)				
"Built-In" Standard Unipolar	V ±0.1%	+10.24	*	*
Bipolar	V ±0.05%	±5.12	*	*
Resistor Programmable (See Figure 3)	V, 0 to:	+5, +7.5, +15, +20, ±2.5, ±3.75, ±7.5, ±10		
Impedance	Ω min	1000	*	*
Overvoltage	V	Two Times Full Scale + or −		
CONVERSION TIME (COMPLETE CYCLE TIME)	μs max (typ)	1.5 (1.2)	1.7 (1.4)	2.8 (2.2)
CONVERSION RATE	kHz max	667	588	357
ENCODE COMMAND – TTL LOGIC INPUT				
Logic Levels (Positive Logic)	V	"0" = 0 to +0.4, "1" = +2 to +5		
Function[1]		Logic "1" Resets Converter Logic "0" Starts Conversion		
Loading		1 Standard TTL Load: "0" = −1.6mA, max "1" = 40μA, max		
Pulse Width	ns min	100	*	*
Repetition Rate		0 to Maximum Conversion Rate		
LOGIC OUTPUTS				
Data Ready (DR)				
Function		Signals conversion is complete when low. After DR goes low, data is valid. A new conversion may be initiated at this time. DR may be used to strobe data into external register if adequate register setup time is allowed.		
Timing		See Figure 1		
Loading		5 Standard TTL Loads, max		
Parallel Data				
Format		8-, 10-, or 12-bits parallel data. Valid from time DR output goes low until 20ns after receipt of next encode command.		
Logic Levels		TTL Compatible: "0" = 0V to +0.4V "1" = +2.4V to +5V		
Loading		Will drive up to 5 Standard TTL Loads or 2 TTL "S" or "H" Loads.		
Coding[2]		Offset Binary (BIN) for Unipolar Inputs: +10.24V = 1111....1 0V = 0000....0 Offset Binary (OBN) for Bipolar Inputs: +5.12V = 1111....1 0V = 0111....1 −5.12V = 0000....0		
POWER REQUIREMENTS				
+14.5V to +15.5V (+18V Absolute Max)	mA	40	*	*
−14.5V to −15.5V (−18V Absolute Max)	mA	15	*	*
+4.75V to +5.25V (+7V Absolute Max)	mA	200	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	0 to +70	*	*
Storage	°C	−55 to +125	*	*
PACKAGE OPTION[3]		HY32A (ceramic package)	HY32C (metal package)	

NOTES
[1] After converter is reset, all other logic signals, including clock, are internally generated.
[2] When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table I).
[3] See Section 19 for package outline information.

*Specifications same as model HAS-0802.
Specifications subject to change without notice.

*Table I. Output Coding**

SCALE	INPUT OF HTC-0300	INPUT OF HAS-1202	DIGITAL OUTPUT
UNIPOLAR OPERATION			
FS-1LSB	-10.2375V	+10.2375V	111111111111
3/4 FS	- 7.6800V	+ 7.6800V	110000000000
1/2 FS	- 5.1200V	+ 5.1200V	100000000000
1/4 FS	- 2.5600V	+ 2.5600V	010000000000
+1LSB	- 0.0025V	+ 0.0025V	000000000001
0	0.0000V	0.0000V	000000000000
BIPOLAR OPERATION			
+FS-1LSB	- 5.1175V	+ 5.1175V	111111111111
0	0.0000V	0.0000V	100000000000
-FS+1LSB	+ 5.1175V	- 5.1175V	000000000001
-FS	+ 5.1200V	- 5.1200V	000000000000

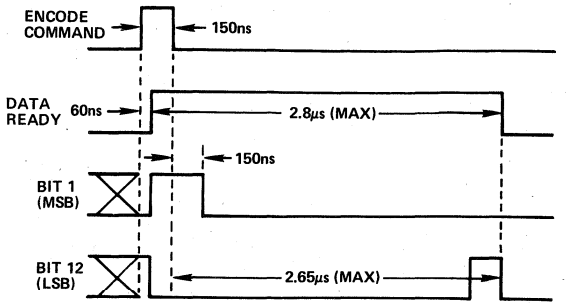
*Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

PIN DESIGNATIONS

HAS-1202*

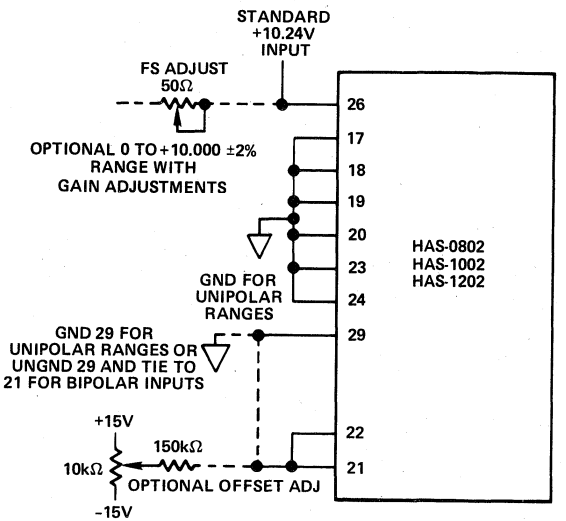
PIN	FUNCTION
1, 30	DIGITAL GROUND
2, 27, 31	+5V
3	DATA READY
4	+15V
5	BIT 1 OUTPUT (MSB)
6	BIT 2 OUTPUT
7	BIT 3 OUTPUT
8	BIT 4 OUTPUT
9	BIT 5 OUTPUT
10	BIT 6 OUTPUT
11	BIT 7 OUTPUT
12	BIT 8 OUTPUT
13	BIT 9 OUTPUT
14	BIT 10 OUTPUT
15	BIT 11 OUTPUT
16	BIT 12 OUTPUT (LSB)
17, 18, 19	ANALOG GROUND
20, 23, 24	ANALOG GROUND
21	D/A OUT
22	D/A IN
25	COMP INPUT
26	ANALOG INPUT
28	-15V
29	BIPOLAR OFFSET
32	ENCODE COMMAND

***HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.**



TIMING SHOWN FOR HAS-1202. TIMING IS SIMILAR FOR HAS-1002 AND HAS-0802 EXCEPT LSB IS BIT 10 AND 8, RESPECTIVELY, AND TOTAL TYPICAL CONVERSION TIME IS 1.4μs AND 1.2μs, RESPECTIVELY.

Figure 1. Timing Diagram (Typical)



NOTES:
1. THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO +10.24V) INPUT. 0V INPUT = 000000000000; +10.24 INPUT = 111111111111.
2. FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
3. FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 26 OF HAS-1202. THIS WILL RESULT IN 0 TO +10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
4. FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTENTIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100mV.

Figure 2. Input Connections For Standard Input Ranges

INPUT RANGE	R1	R2	Z_{IN}	ABSOLUTE MAXIMUM SIGNAL
0 to +5V, ±2.5V	SHORT	800	500	±10V
0 to +7.5V, ±3.75V	SHORT	2500	750	±15V
0 to +15V, ±7.5V	500	OPEN	1500	±30V
0 to +20V, ±10V	1000	OPEN	2000	±40V

Input Connections For Optional Input Ranges

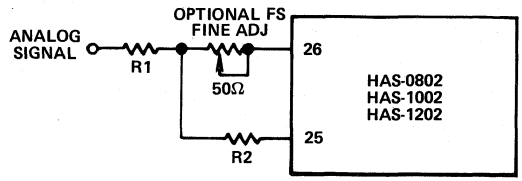


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

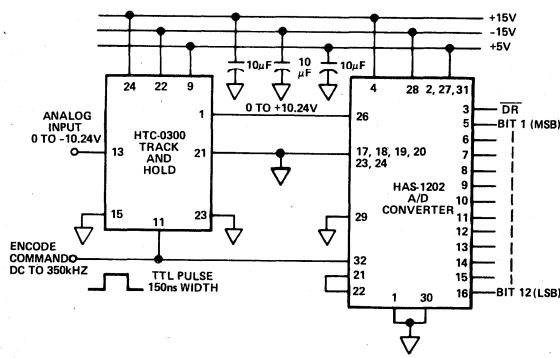


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range are also available. Consult the factory or nearest Analog Devices' sales office for further information.

ANALOG DEVICES

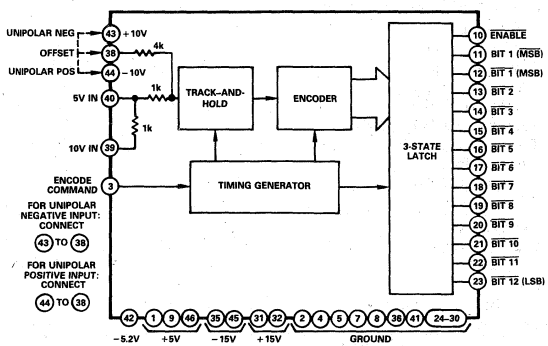
12-Bit, 1MHz Analog-to-Digital Converter

HAS-1201

FEATURES
12-Bit Resolution
1MHz Word Rate
T/H and Timing Circuits Included
Single Hybrid Package

APPLICATIONS
Radar Systems
Medical Instrumentation
Electro-Optics Systems
Test Systems

HAS-1201 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Resolution and speed are combined in a single hybrid package with the HAS-1201 A/D converter. This is a *complete* 12-bit, 1MHz unit which includes a track-and-hold and timing circuits. It's a total solution for the system designer who needs to perform the entire analog-to-digital conversion function in the smallest possible space.

This remarkable converter is the complete answer to the question of digitizing analog signals into high-resolution data outputs and doing it in the most cost-effective way. The HAS-1201 is the ideal choice for the designer who needs state-of-the-art performance in high-resolution, high speed A/D conversion.

All digital inputs and the three-state digital output are TTL compatible. Analog input impedance is 1,000 or 2,000 ohms and the unit can operate with 5V or 10V bipolar or unipolar ranges. The user needs to supply only an encode command and external power supplies for operation.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HAS-1201SM
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.025)
ACCURACY		
Gain	%FS	±1.5
Offset	%FS	±1.0
Linearity @ dc	%FS ± 1/2LSB	0.0125
Monotonicity	°C	Guaranteed −25 to +85
Gain vs. Temperature	% of FS/°C	0.005
Offset vs. Temperature	% of FS/°C	0.01
DYNAMIC CHARACTERISTICS		
In-Band Harmonics[1]		
(dc to 100kHz)	dB below FS	80
Conversion Rate	MHz, max	1.05
Aperture Time (Delay)	ns	30
Signal to Noise Ratio (SNR)[2]	dB (min)	68 (65)
Signal to Noise Ratio (SNR)[3]	dB (min)	77 (74)
Transient Response[4]	ns (max)	500 (1000)
Input Bandwidth		
Small Signal, 3dB[5]	kHz	3000
Large Signal, 3dB[6]	kHz	500
ANALOG INPUT		
Voltage Ranges	V, p-p FS	5.0/10.0
Impedance	Ω	1000/2000
Offset[7]		
Initial	mV (max)	2.0 (10)
Input Type		Bipolar or Unipolar
ENCODE COMMAND INPUT[8]		
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4
	V	"1" = +2.4 to +5
Impedance	TTL Loads	2
Rise and Fall Times	ns, max	25
Width		
Min	ns	50
Max	ns	Time Period − 50ns
Frequency	MHz, max	1.05
DIGITAL OUTPUT		
Format	Bits	12 Parallel; 3-State; NRZ
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4
	V	"1" = +2.4 to +5
Drive	TTL Loads	1
Coding		Straight Binary (BIN) Offset Binary (OBN) 2's Complement (2SC)
POWER REQUIREMENTS		
+15V ±3%	mA (max)	60 (70)
−15V ±3%	mA (max)	65 (80)
+5V ±5%	mA (max)	180 (220)
−5.2V +5%	mA (max)	30 (35)
Power Consumption	W (max)	3.0 (3.5)
TEMPERATURE RANGE[9]		
Operating	°C	−25 to +85
Storage	°C	−55 to +150
PACKAGE OPTION[10]	HY46A	

NOTES
[1]In-Band Harmonics expressed in terms of spurious in-band signals generated at 1MHz encode rate at analog inputs shown in ( ).
[2]RMS signal to rms noise ratio with 100kHz analog input.
[3]Peak-to-peak signal to rms noise ratio with 100kHz analog input.
[4]For full-scale step input, 12-bit accuracy attained in specified time.
[5]With analog input 40dB below FS.
[6]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 100kHz).
[7] Externally adjustable to zero.
[8]Transition from digital "0" to digital "1" initiates encoding.
[9]Case Temperature.
[10]See Section 19 for package outline information.

Specifications subject to change without notice.

HAS-1201 PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	24	GROUND
2	GROUND	25	GROUND
3	ENCODE COMMAND	26	GROUND
4	GROUND	27	GROUND
5	GROUND	28	GROUND
6	DO NOT CONNECT*	29	GROUND
7	GROUND	30	GROUND
8	GROUND	31	+15V
9	+5V	32	+15V
10	$\overline{\text{ENABLE}}$	33	NO CONNECTION
11	BIT 1 (MSB)	34	NO CONNECTION
12	$\overline{\text{BIT 1}}$ (MSB)	35	−15V
13	$\overline{\text{BIT 2}}$	36	GROUND
14	$\overline{\text{BIT 3}}$	37	DO NOT CONNECT*
15	$\overline{\text{BIT 4}}$	38	OFFSET
16	$\overline{\text{BIT 5}}$	39	10V RANGE IN
17	$\overline{\text{BIT 6}}$	40	5V RANGE IN
18	$\overline{\text{BIT 7}}$	41	GROUND
19	$\overline{\text{BIT 8}}$	42	−5.2V
20	$\overline{\text{BIT 9}}$	43	UNIPOLAR NEGATIVE
21	$\overline{\text{BIT 10}}$	44	UNIPOLAR POSITIVE
22	$\overline{\text{BIT 11}}$	45	−15V
23	$\overline{\text{BIT 12}}$ (LSB)	46	+5V

NOTE:
PINS 2, 4, 5, 7, 8, 24-30, 36 and 41 NEED TO BE CONNECTED TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.
*FOR FACTORY USE ONLY.

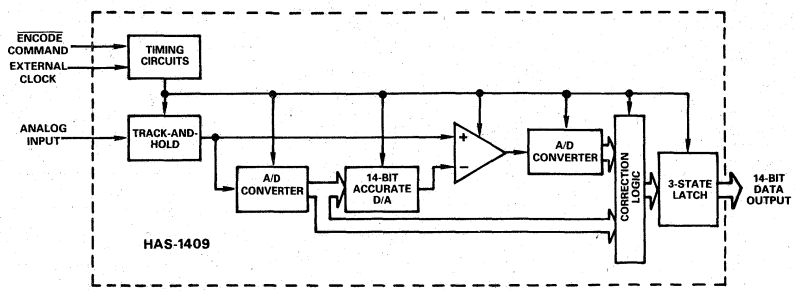
14-Bit, 125kHz Analog-to-Digital Converter

HAS-1409

FEATURES
14-Bit Resolution
125kHz Word Rates
Internal Track-and-Hold
40-Pin DIP

APPLICATIONS
FDM/TDM Transmultiplexers
CAT/NMR Scanners
PCM Systems
Digital Audio
General Instrumentation

HAS-1409 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

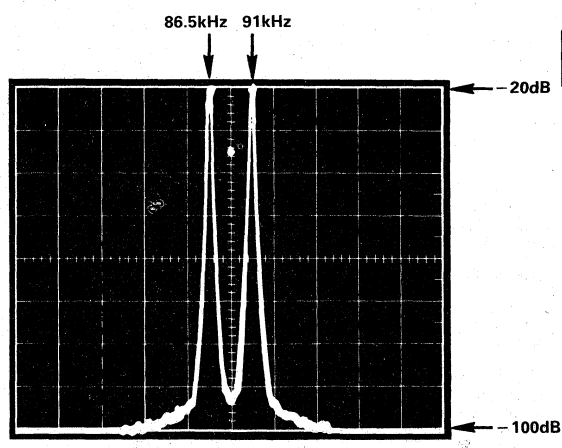
The HAS-1409KM, HAS-1409LM, and HAS-1409AKM hybrid A/D converters offer designers performance characteristics which have never before been available.

Now, for the first time, high resolution and high speed come together in a hybrid package which includes an internal track-and-hold. The HAS-1409 units have resolutions of 14 bits, are capable of word rates up to 125kHz, and are complete with track-and-hold; all of these features are housed in a single 40-pin DIP package which dissipates only two watts.

The HAS-1409KM and HAS-1409LM both include internal clocks, which allow the converters to be operated at any word rate from dc through 120kHz; the HAS-1409AKM is designed for applications which use an external system clock whose frequency establishes the user's optimum word rate, up to 125kHz.

The HAS-1409 A/D has been characterized with a companion D/A converter, the HDD-1409KM, to emphasize the superior ac performance needed for use in Frequency Division Multiplex/Time Division Multiplex (FDM/TDM) transmultiplexer systems. Although specifically designed for these kinds of applications, it can also be used for other digital signal processing such as Computer Aided Tomography (CAT) and Nuclear Magnetic Resonance (NMR) scanners, and Pulse Code Modulation (PCM).

Conventional data converters often display errors at midscale which make them inadequate for use in the types of systems cited above. The unique Digitally Corrected Subranging technique pioneered by Analog Devices, used with other proprietary techniques, virtually cancels midscale errors in the HAS-1409, thereby eliminating a major source of system errors.



10dB/div Vertical; 5kHz/div Horizontal
Spectrum analyzer shows extremely low intermodulation (IM) products of back-to-back HAS-1409 A/D and HDD-1409 D/A

The logic outputs are TTL-compatible and are presented as 14 bits of parallel data. Buffer output registers and a 3-state format provide dual advantages of good drive and bus compatibility.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Model	Units	HAS-1409KM	HAS-1409AKM	HAS-1409LM
RESOLUTION (FS = Full Scale)	Bits (%FS)	14 (0.006)	*	*
LSB WEIGHT	μV	610 or 1221, depending on input range	*	*
ACCURACY				
Linearity @ dc	%FS ± 1/2LSB	0.006	*	*
Monotonicity	°C	Guaranteed 0 to +85	*	*
Nonlinearity vs. Temperature	ppm/°C	5	*	*
Gain Error	%FS	1	*	*
Gain vs. Temperature	ppm/°C	20	*	*
DYNAMIC CHARACTERISTICS[1]				
Harmonics[2]	dB	−100	*	−80
Intermodulation Products[2]	dB	−100	*	−90
Conversion Rate	kHz	120 (112 guaranteed)	125[3]	*
Aperture Time (Delay)	ns	50	*	*
Signal to Noise Ratio (SNR)[4]	dB	80	*	*
Noise Power Ratio (NPR)[5]	dB	68	*	65
Transient Response[6]	μs	8	*	2
Overvoltage Recovery	μs	8	*	6
Input Bandwidth				
Small Signal, 3dB[8]	kHz	200	*	800
Large Signal, 3dB[9]	kHz	200	*	300
Idle Noise/kHz[10]	dB	−104	*	*
ANALOG INPUT				
Voltage Ranges	V, FS	±5; ±10	*	*
Overvoltage	V, max	±20	*	*
Input Type		Bipolar	*	*
Impedance	kΩ	5; 10	*	*
Offset				
Initial–Set at Factory	mV (max)	2 (10)	*	*
vs. Temperature	μV/°C	100	*	*
ENCODE COMMAND INPUT[11]				
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Impedance	TTL Loads	1	*	*
Width				
Min	ns	50	1 Clock	*
Max	ns	T−50[12]	Period	*
Frequency	kHz	dc to 125	Synchronous to External Clock	*
CLOCK INPUT				
Logic Levels, TTL-Compatible	V			
		N/A	"0" = 0 to +0.4	*
		N/A	"1" = +2.4 to +5	*
Impedance	TTL Loads	N/A	2	*
Frequency[13]	MHz, max	N/A	4.5	*
DIGITAL OUTPUT				
Format	Bits	14 Parallel; 3 State	*	*
Logic Levels, TTL-Compatible	V	"0" = 0 to +0.4	*	*
		"1" = +2.4 to +5	*	*
Drive	TTL Loads	5	*	*
Time Skew	ns, max	20	*	*
Coding		Offset Binary (MSB); 2's Complement ($\overline{MSB}$)	*	*
POWER REQUIREMENTS				
+15V ±5%	mA	20	*	*
−15V ±5%	mA	40	*	*
+5V ±5%	mA	220	180	*
Power Dissipation	W (max)	2.0 (2.4)	1.8 (2.2)	*
TEMPERATURE RANGE[14]				
Operating	°C	−25 to +85	*	*
Storage	°C	−55 to +150	*	*
THERMAL RESISTANCE[15]				
Junction to Air, θja (Free Air)	°C/W	25	*	*
Junction to Case, θjc	°C/W	16	*	*
MEAN TIME BETWEEN FAILURES[16] (MTBF)	Hours	4.15×10^4	*	*
PACKAGE OPTION[17]		HY40B	*	*

NOTES

[1]AC performance characteristics are based on back-to-back performance with HDD-1409 D/A Converter. All signals are referenced to rms value of full-scale sinewave.

[2]Harmonics and intermodulation products measured at 112kHz encode rate, with input frequencies of 86.5kHz and 91kHz at −21dB (see Figure 5).

[3]Requires external clock.

[4]Full-scale signal to rms noise with 10kHz analog input frequency and encode rate of 112kHz; input signal at −6dB.

[5]60kHz to 108kHz white noise bandwidth with slot frequency of 70kHz; and encode rate of 112kHz (see Figure 6).

[6]For full-scale 10-volt input, ±1LSB attained in specified time.

[7]Recovers to 14-bit accuracy in specified time after 2 × FS input overvoltage.

[8]With analog input 40dB below FS.

[9]With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 100kHz).

[10]Idle noise measured at 112kHz encode rate, with input frequency of 84kHz at −41dB (see Figure 7).

[11]HAS-1409KM has pin-selectable positive- or negative-edge triggering. HAS-1409AKM requires negative pulse synchronized to rising clock edge.

[12]T = Encode Command clock period.

[13]Clock frequency shown based on typically using 50% duty cycle and 36:1 division of external clock.

[14]Case Temperature.

[15]Maximum junction temperature = 150°C

[16]Calculated using MIL-HDBK 217; Ground; Benign; Case Temperature = 60°C.

[17]See Section 19 for package outline information.

*Specifications same as HAS-1409KM.

Specifications subject to change without notice.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

HAS-1409 PIN DESIGNATION

PIN	FUNCTION (ALL)	PIN	FUNCTION (AKM)	PIN	FUNCTION (KM & LM)
1	±10V INPUT	21	DIGITAL GROUND	21	DIGITAL GROUND
2	±5V INPUT	22	BIT 1 (MSB)	22	BIT 1 (MSB)
3	ANALOG GROUND	23	$\overline{\text{BIT 1}}$ (MSB)	23	$\overline{\text{BIT 1}}$ (MSB)
4	DIGITAL GROUND	24	$\overline{\text{BIT 2}}$	24	$\overline{\text{BIT 2}}$
5	+5V	25	$\overline{\text{BIT 3}}$	25	$\overline{\text{BIT 3}}$
6	+5V	26	$\overline{\text{BIT 4}}$	26	$\overline{\text{BIT 4}}$
7	N/C	27	$\overline{\text{BIT 5}}$	27	$\overline{\text{BIT 5}}$
8	N/C	28	$\overline{\text{BIT 6}}$	28	$\overline{\text{BIT 6}}$
9	+5V	29	$\overline{\text{ENABLE HIGH}}$ (MSBs)	29	$\overline{\text{ENABLE HIGH}}$ (MSBs)
10	DIGITAL GROUND	30	CLOCK/ENCODE	30	$\overline{\text{ENCODE}}$
11	$\overline{\text{ENABLE LOW}}$ (LSBs)	31	$\overline{\text{ENCODE}}$	31	ENCODE
12	$\overline{\text{BIT 14}}$ (LSB)	32	+5V	32	+5V
13	$\overline{\text{BIT 13}}$	33	DIGITAL GROUND	33	DIGITAL GROUND
14	$\overline{\text{BIT 12}}$	34	−15V	34	−15V
15	$\overline{\text{BIT 11}}$	35	+15V	35	+15V
16	$\overline{\text{BIT 10}}$	36	DIGITAL GROUND	36	DIGITAL GROUND
17	$\overline{\text{BIT 9}}$	37	ANALOG GROUND	37	ANALOG GROUND
18	$\overline{\text{BIT 8}}$	38	ANALOG GROUND	38	ANALOG GROUND
19	$\overline{\text{BIT 7}}$	39	+5V	39	+5V
20	DIGITAL GROUND	40	ANALOG GROUND	40	ANALOG GROUND

PIN 30 USED FOR CLOCK INPUT ON HAS-1409AKM; USED FOR ENCODE INPUT ON HAS-1409KM.
ALL +5V PINS ARE CONNECTED TOGETHER INTERNALLY (5, 6, 9, 32, 39). MUST ALSO BE CONNECTED TOGETHER EXTERNALLY CLOSE TO CASE.
ALL ANALOG GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (3, 37, 38,40).
ALL DIGITAL GROUND PINS ARE CONNECTED TOGETHER INTERNALLY (4, 10, 20, 21, 33, 36).
FOR BEST PERFORMANCE, ANALOG GROUND AND DIGITAL GROUND PINS MUST ALL BE CONNECTED TOGETHER AND TO GROUND EXTERNALLY AS CLOSE TO THE CASE AS POSSIBLE.

HAS-1409KM/HAS-1409AKM TIMING

Refer to the block diagram of the HAS-1409AKM A/D converter.

In the HAS-1409KM, and HAS-1409LM, signals applied to the timing circuits will be different from those shown. For them, these signals will be ENCODE or $\overline{\text{ENCODE}}$.

In all units, the analog input to be digitized is applied first to a track-and-hold (T/H) circuit, which is normally in "track", following all changes in analog as they occur since the T/H is operating as a buffer amplifier.

Refer to Figure 1, the timing diagram for the HAS-1409KM and HAS-1409LM A/D converters.

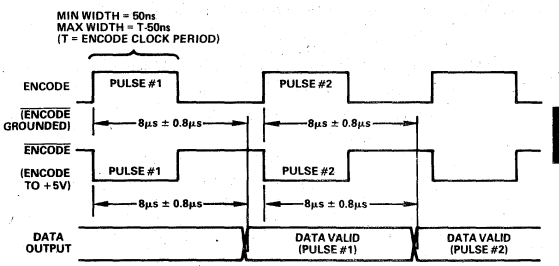


Figure 1. HAS-1409KM and HAS-1409LM A/D Timing Diagram

10

The user determines the point at which digitizing is to be done by applying an external TTL-compatible signal to the timing circuits; this causes the T/H to switch from the "track" mode to the "hold" mode. In the HAS-1409KM and HAS-1409LM, this "track" to "hold" transition can be accomplished with either positive triggering or negative triggering. As shown, positive-edge triggering is done with an ENCODE command and $\overline{\text{ENCODE}}$ connected to ground. Negative-edge triggering is accomplished with an $\overline{\text{ENCODE}}$ signal and ENCODE connected to +5V. The HAS-1409KM and HAS-1409LM return to "track" automatically approximately 5μs after the encode command.

Output data will be valid after a nominal delay of 8μs from the leading edge of the encode command. Strobing the output data into external circuits might best be accomplished by using a square-wave signal for the encode command and using its negative-going trailing edge as a time reference for the strobing action. Output data will not yet be valid when that trailing edge occurs, but the edge can be used as a known reference point for measuring the 8μs conversion time.

Internal timing circuits within the HAS-1409 generate the necessary control and timing pulses to operate the unit at a word rate of 112kHz. This rate is based on:

KM/LM: The internal clocks adjusted at the factory for this conversion rate.

AKM: The HAS-1409AKM divides the external clock frequency of 4.032MHz by a factor of 36:1 and provides 14 bits of parallel data at the 112kHz word rate established by this ratio. The 112kHz cited in this example is the minimum guaranteed word rate of the HAS-1409, and is a sample rate commonly used in transmultiplexer applications. (See FDM/TDM Transmultiplexers section of data sheet).

Figure 2 shows the timing relationship of the HAS-1409AKM A/D converter signals when the converter is being operated from an external clock.

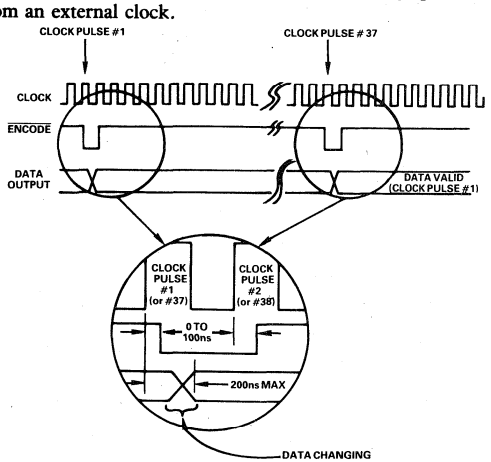


Figure 2. HAS-1409AKM A/D Timing Diagram (External Clock Operating at 4.032MHz)

As shown, the leading edge of the negative-going $\overline{\text{ENCODE}}$ pulse supplied by the user should occur from 0 to 100ns after the leading edge of the clock pulse which is shown (for purposes of illustrating timing relationships) as Clock Pulse #1. The trailing edge of this pulse should occur from 0 to 100ns after the leading edge of the *next* clock pulse (designated here as Clock Pulse #2).

The output data associated with the *preceding* clock pulse and $\overline{\text{ENCODE}}$ pulse will be valid within 200ns of the leading edge of Clock Pulse #1. Data associated with Clock Pulse #1 will be valid within 200ns of the leading edge of Clock Pulse #37. When the HAS-1409AKM is operated from a 4.032MHz clock, the trailing edge of the $\overline{\text{ENCODE}}$ pulse could be used to determine when the output data will be strobed into external circuits.

The $\overline{\text{ENCODE}}$ pulse is used to insure output data will remain in synchronization with the clock pulses. Using the leading edge of the first $\overline{\text{ENCODE}}$ as a reference, the HAS-1409AKM goes into "track" after 21 clock pulses (on Clock Pulse #22); and goes into "hold" after 34 clocks (Clock Pulse #35).

THEORY OF OPERATION

With the exception of the difference in input signals applied to the timing circuits, all converters operate in essentially the same way.

Referring again to the block diagram, the timing circuits "freeze" the analog signal at the output of the track-and-hold. This held value is applied to an A/D converter in the HAS-1409, and the same value is applied to one input of a difference amplifier.

The output of the internal A/D converter is digitized and applied to a D/A converter which is 14-bit accurate and optimized for ac applications; the A/D output is also applied to correction logic circuits.

The D/A output is applied to the second input of the difference amplifier, which generates an error signal indicative of the difference between the "held" analog input and a digital representation of that signal. This residue signal is then converted and is also applied to the digital correction circuits.

The correction circuits combine the two bytes to compensate for nonlinearities and other circuit errors. Basically, the information contained in the second byte is used as the Least Significant Bits (LSBs) and determines what corrective action is needed for the first byte (the MSBs) to insure its accuracy.

APPLICATIONS/TESTING

For FDM/TDM applications, the analog input frequency applied to the HAS-1409 will be in the frequency band of 60-108kHz; the combined HAS-1409/HDD-1409 performance parameters have been optimized for this use.

Refer to Figure 3 HAS-1409 Basic Interface.

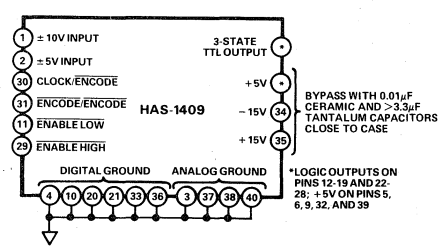


Figure 3. HAS-1409 Basic Interface

As shown, the anlog input is applied to Pin 1 or Pin 2, depending on the amplitude of the signal to be digitized. A TTL-compatible pulse is applied as $\overline{\text{ENCODE}}$; and another TTL-compatible signal is applied as the clock. As indicated earlier in the timing diagram, these signals must be synchronous.

The $\overline{\text{ENABLE HIGH}}$ and $\overline{\text{ENABLE LOW}}$ signals applied to Pins 29 and 11 control the state of the digital outputs. The TTL $\overline{\text{ENABLE HIGH}}$ signal affects $\overline{\text{BIT 1}}$ (MSB), Bit 1 ($\overline{\text{MSB}}$), and Bits 2-6; the $\overline{\text{ENABLE LOW}}$ affects Bits 7-14. When $\overline{\text{ENABLE HIGH}}$ and/or $\overline{\text{ENABLE LOW}}$ inputs are connected

to ground or logical "0", their corresponding bit outputs will be present. When they are connected to a logical "1" voltage, their associated bit outputs will be open.

The 3-state TTL digital output signals will be available at Pins 12-19 and Pins 22-28. Pins 34 and 35 are used for −15V and +15V supplies; +5V is applied to several places–Pins 5, 6, 9, 32, and 39 (all pins should be connected). All three supplies should be bypassed as close as possible to the hybrid case. For best performance, all ANALOG GROUND and DIGITAL GROUND pins *must* be connected together and to ground externally; this should also be done close to the case.

Refer to Figure 4 Basic Test Setup.

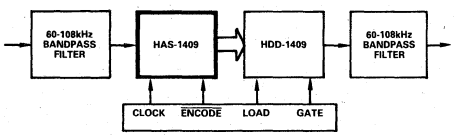


Figure 4. Basic Test Setup

The HAS-1409 A/D converter has been characterized for performance in a back-to-back hook-up with the HDD-1409 D/A converter. The analog signal to be digitized and reconstructed is applied to this test arrangement through a bandpass filter of 60kHz-108kHz; the resulting analog output is also passed through the same kind of filter.

CLOCK and $\overline{\text{ENCODE}}$ signals are generated in synchronization with one another and are timed for correct interaction with the STROBE and GATE signals applied to the D/A. Because of the back-to-back configuration of the two converters, the performance tests are indicative of the baseline characteristics of ***both*** units.

Refer to Figure 5 Intermodulation (Total Harmonic) Distortion Test Circuit.

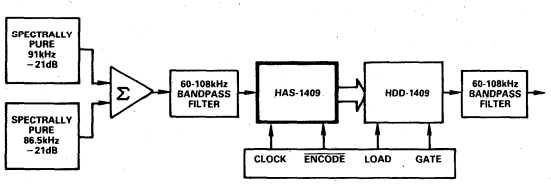


Figure 5. Intermodulation (Total Harmonic) Distortion Test Circuit

Harmonics levels and intermodulation (IM) products are measured in the same way to assure optimum performance in FDM/TDM system applications. The purpose of the testing is to insure that "beat" frequencies generated by the interaction of two signals are sufficiently suppressed to avoid interfering with the carrier frequencies and masking their information contents.

In these tests, the HAS-1409 is operated at a 112kHz word rate, established by the external 4.032MHz clock. Two pure sinewave signals at frequencies of 91kHz and 86.5kHz are applied to a summation amplifier at precise levels 21dB below the rms value of a full-scale sinewave.

These particular input frequencies are selected on the basis that their interaction with one another will generate second and third-order harmonics and IM products which are easily distinguished and measurable. As in any sampling scheme, these signals are "folded" back into the passband of interest and their amplitudes are a measure of A/D and D/A performance.

The output of the summation amplifier is applied through the 60-108kHz filter, digitized, reconstructed, and refiltered. Typically, the levels of harmonics and intermodulation products are −100dB.

Refer to Figure 6 Noise Power Ratio Test Circuit.

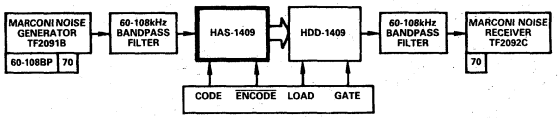


Figure 6. Noise Power Ratio Test Circuit

Noise Power Ratio (NPR) is a critical measure of A/D and D/A performance for FDM/TDM systems and the method of measuring this ratio must replicate the conditions which are present when the units are operating as a part of those systems. In this test, also, the HAS-1409 is operating at 112kHz word rates.

White noise in the frequency band of 60kHz to 108kHz is applied to the A/D, and the total power which is present in a narrow "slot" at a frequency of 70kHz is computed. A narrow bandstop filter whose center frequency is 70kHz is then switched in, and the total power remaining in the "slot" is computed. The ratio of these two readings is the NPR and the result for the HAS-1409 is typically 68dB. CAUTION: The high-performance characteristics of the HAS-1409 stress the measurement capabilities of most NPR test sets.

Refer to Figure 7 Idle Noise Test Circuit. In this test, a spectrally-pure sinewave of 84kHz is applied through a filter to the HAS-1409/HDD-1409 combination at a level of −41dB. An encode rate of 112kHz is used; the combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental input frequency and noise components.

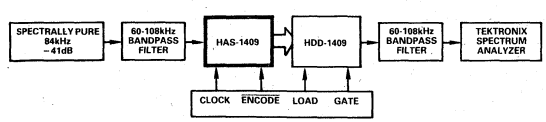


Figure 7. Idle Noise Test Circuit

The results of digitizing and reconstructing this signal are examined with a spectrum analyzer to determine the level of noise components contributed by the converters. Acceptable performance will show average idle noise components to be at −104dB when using a 1kHz-resolution filter.

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FDM/TDM TRANSMULTIPLEXERS

There are two standard formats used in telephony for multiplexing voice signals. The older of the two, frequency division multiplex (FDM), is used throughout the world for transmitting long distance telephone calls. In this scheme, voiceband signals are "stacked" into adjacent 4kHz channels in their assigned frequency domain by using single sideband (SSB) amplitude modulation.

Standard FDM hierarchy assembles twelve of these 4kHz channels into units called "groups", and then assembles five groups (60 channels) into "supergroups." The frequencies of group bands range from 60kHz to 108kHz, and the supergroup bands have center frequencies between 312kHz and 552kHz.

In the newer time division multiplex, or TDM, each voice signal is digitized using pulse code modulation (PCM), at an 8kHz sample rate. The resulting pulse streams are then interleaved in time and transmitted.

The assembly of time slots (channels) for TDM is not as universal as it is for FDM. In North America and Japan, the basic unit is 24 time slots, all of which are available to users. In Western Europe, the basic unit is 32 time slots; 30 are active, one is for signaling, and one is for framing.

TDM processing is growing at a rapid pace because the voice signals have good fidelity, and the hardware which is used benefits from the economics of lower and lower prices for digital integrated circuits.

Digital toll switching offices were first installed in the United States in the latter part of the 1970s. One of the major characteristics of these types of telephone offices is that they switch signals exclusively in the TDM format within the office. But their need to operate also with the older FDM format means all incoming and outgoing signals must be converted to and from digital form.

The interface between the two standard signal multiplexing formats used to make this conversion is the FDM/TDM transmultiplexer system. The translation from one format to the other can be accomplished with conventional analog and digital techniques by demultiplexing signals in one format down to baseband, and remultiplexing them again into the other format.

Digital signal processing (DSP) for the interface is attractive, however. The frequency ranges of the signals which are involved make efficient use of available technology; and the stringent interface specifications benefit from the inherent precision of a digital approach. Since the problem is well defined, digital techniques are distinctly viable solutions. An example of these techniques is shown in Figure 8.

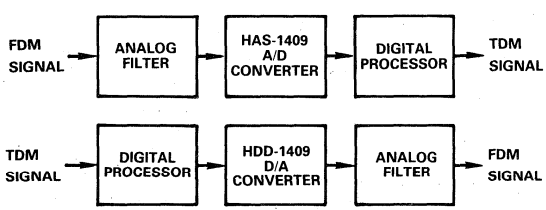


Figure 8. Digital FDM/TDM Translation

Undesirable out-of-band components are removed from the FDM signal by the analog filter. The output of the filter is then applied to the HAS-1409 A/D converter whose output is a digital word stream. The individual channels within this stream are separated via a real-time processing algorithm in the block labeled Digital Processor. The resulting signal is now in the TDM format for switching and/or transmitting.

The lower portion of Figure 8 depicts the process of going from TDM to FDM, using the HDD-1409 D/A converter, in a procedure which is basically an inverse operation. The exception is the analog filter, which performs essentially the same function in both directions.

Interfacing FDM and TDM occurs at two different levels. In North America and Japan, this translation takes place between two 12-channel group bands and a 24-channel TDM unit. In Europe, it is between a 60-channel supergroup and two 30-channel European TDM units.

Theoretically, the minimum word rate for the HAS-1409 A/D is equal to twice the bandwidth of the FDM group signal; that signal, in turn, is equal to the word rate of the TDM signal, i.e., 96kHz for the group band.

This minimum rate falls into the passband of interest because group frequencies occupy the band from 60kHz to 108kHz; as a consequence, the theoretical minimum rate would severely complicate the processing algorithm and introduce aliasing errors into the signal.

Operating at a conversion rate near this minimum is desirable, however, because the cost of the A/D and D/A converters increases as their word rates increase. In addition, a sampling rate which is an even multiple of the basic 8kHz PCM frequency simplifies the algorithm.

Since any sampling rate between the (108kHz) upper band and two times the 60kHz lower band (120kHz) will suffice, the HAS-1409 A/D converter is operated at 112kHz.

This rate provides the benefits enumerated above and prevents overlapping between channels caused by aliasing. A conversion rate of 112kHz also supplies a guard band of 8kHz between signal images; that guard band reduces the complexity of the analog reconstruction filter.

Computer Labs Division of Analog Devices uses this 112kHz word rate when testing the performance of the HAS-1409 A/D and HDD-1409 D/A converters back-to-back to help assure test conditions are a good replication of the operating conditions.

For some of the testing, the word rate interacts with the analog input frequencies to provide additional insight into performance. Harmonics tests and intermodulation products tests are examples.

Another is the test for idle noise, the sum of various noise spectra not influenced by modulation. Thermal noise, oscillator shot noise, baseband amplifier noise, and other sources are examples. Their sum is measured on a power basis because of their uncorrelated nature.

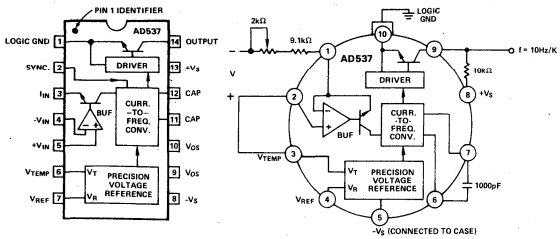
In the test, the input frequency is a spectrally-pure 84kHz. The combination of input frequency and encode rate cancels all harmonics, leaving only the fundamental frequency and the idle noise components.

Evaluating the amount of idle noise generated by the converters helps evaluate their nonlinear distortion, without rigorously testing for that characteristic. In transmultiplexer systems, the converters are the only important sources of this distortion, but converters which meet requirements for idle noise easily meet requirements for nonlinearity.

Voltage-to-Frequency & Frequency-to-Voltage Converters

Contents

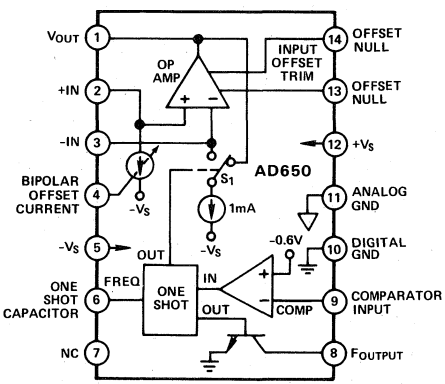
Selection Guide
Voltage-to-Frequency Converters



AD537

Page
Vol. I
11-7

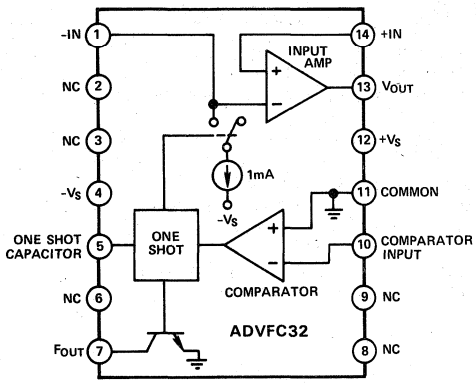
- Low Cost A/D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F/V Applications



AD650

Vol. I
11-15

- V/F Conversion to 1MHz
- Reliable Monolithic Construction
- Very High Linearity
  - 0.002% typ at 10kHz
  - 0.005% typ at 100kHz
  - 0.07% typ at 1MHz
- Input Offset Trimmable to Zero
- CMOS or TTL Compatible
- Unipolar, Bipolar, or Differential V/F
- V/F or F/V Conversion



ADVFC32

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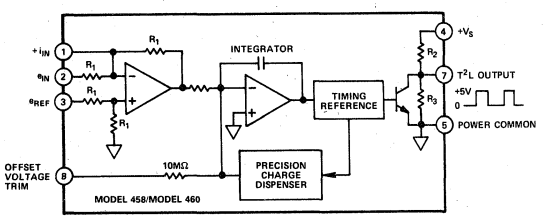
11-27

High Linearity
±0.01% max at 10kHz FS
±0.05% max at 100kHz FS
±0.2% max at 0.5MHz FS
Output DTL/TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction



MODEL 458/MODEL 460

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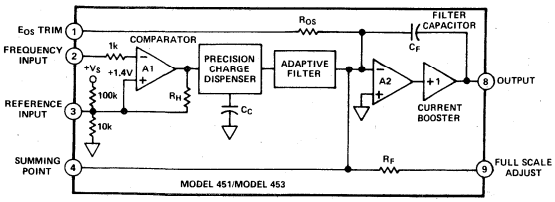
Model 458: Full Scale Output 100kHz
Model 460: Full Scale Output 1MHz
High Stability: 5ppm/°C max, Model 458L
15ppm/°C max, Model 460L
High Linearity: ±0.01% max at 100kHz, Model 458
±0.015% max at 1MHz, Model 460
Versatility: Differential Input Stage
Voltage and Current Inputs
Floating Inputs: ±10V CMV
Wide Dynamic Range: 6 Decades, Model 460
TTL/DTL Compatible Output
No External Components to Meet Rated Performance

Selection Guide
Frequency-to-Voltage Converters



MODEL 451/MODEL 453

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Model 451: Full Scale Input 10kHz
Model 453: Full Scale Input 1kHz
Versatility: Adjustable Threshold, Gain & Output Offset
Guaranteed Low Nonlinearity: 80ppm max, 451L and 453L
Accepts TTL, CMOS, HNIL, Sinewave, Pulse, Squarewave and Triangle Wave Input Signals
No External Components to Meet Rated Performance
+20mA Output to Operate Relays and Meters
Low Profile Package, 0.4" Case Height

Orientation
Voltage-to-Frequency & Frequency-to-Voltage Converters

VOLTAGE-TO-FREQUENCY CONVERTERS

Voltage-to-frequency converters (VFC's) convert analog voltage or current levels to pulse trains or square waves in a logic-compatible form (usually TTL) at frequencies that are accurately proportional to the analog quantity. The output continuously tracks the input signal, responding directly to changes in the input signal; external-clock synchronization is not required. V/F converters find applications in analog-to-digital converters with high resolution, long-term high-precision integrators, two-wire high-noise-immunity digital transmission, and digital voltmeters.

FREQUENCY-TO-VOLTAGE CONVERTERS

Frequency-to-voltage converters (FVC's) perform the inverse operation; they accept a wide variety of periodic waveforms and produce an analog output proportional to frequency. Combining adjustable threshold, gain, and output offset with low linearity-error, F/V converters offer economical solutions to a wide variety of applications where it is required to convert frequency to an analog voltage. Examples are motor-speed controllers, power-line frequency monitors, and VCO stabilization circuits. In analog-to-analog data transmission, they convert serially transmitted data in the form of pulse streams back to analog voltage.

Applications of both forms of conversion, as appropriate to specific device types, are illustrated with varying degrees of detail on the individual data sheets.

FACTORS IN CHOOSING VFC's AND FVC's

Voltage-to-frequency converters are available from Analog Devices in both pulse train and square wave outputs. The output of the change balance types, operate up to 1MHz F.S., is a train of pulses of constant height and width, with very low duty cycle for small analog inputs. The output of the AD537 is unique in that its output is square-wave, an advantage in some applications.

The most-popular VFC designs (Figure 1) contain an integrator, which charges at a rate proportional to the value of the input signal. Each time the integrator's charge has been increased by a precisely metered increment, the threshold crossing produces a pulse of accurately known area. The pulse serves both as the output (via a buffer) and as a subtractive charge

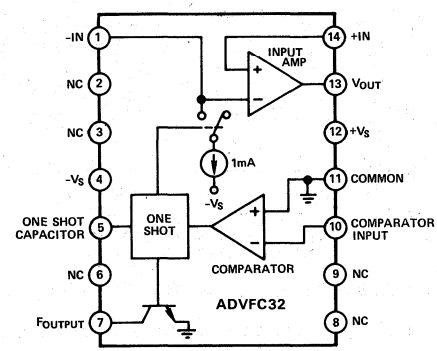


Figure 1. Block Diagram of the ADVFC32

increment to reduce the integrator's net charge. The next pulse is triggered when the net integral has again reached the threshold. The relationship between the pulse rate and the input level is linear. The AD537* operates on a somewhat different principle (Figure 2): an input current charges a capacitor between 2 threshold levels, first in one direction, then in the other, in an emitter-coupled astable multivibrator circuit. Since the time required to reach the switching threshold is inversely proportional to the analog input, the frequency is directly proportional. For constant analog input, the charging rate and the discharge rate are equal, so the output is a square wave.

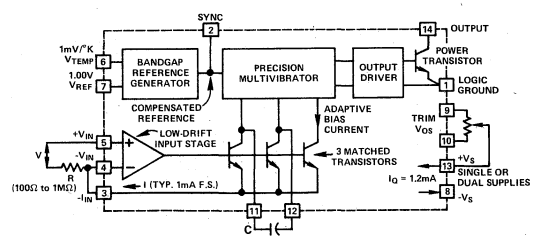
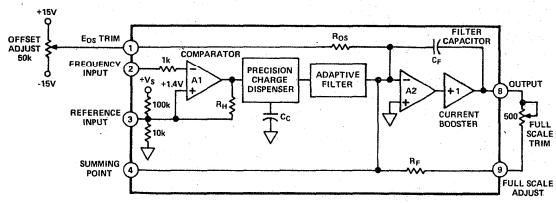


Figure 2. Block Diagram of the AD537

*A useful 20-page Application Note, "Applications of the AD537 IC Voltage-to-Frequency Converter", by Doug Grant, is available upon request.



MODEL	C_F	R_{OS}	R_H	R_F
451	0.015μF	3.3MΩ	2.2MΩ	18kΩ
453	0.001μF	3.9MΩ	1.0MΩ	22kΩ

Figure 3. Block Diagram – Models 451 & 453 FVC's

Frequency-to-voltage converters (Figure 3) average a train of equal-area pulses that are generated internally by a precision charge dispenser, in response to each crossing of an input threshold. The analog output voltage is proportional to the sum of the pulse areas over a given period. F/V conversion can also be obtained by using the ADVFC32.

SPECIFICATIONS

The salient specifications for VFC's are *(non)linearity*, as a percentage of full-scale frequency; *frequency range*, the greater the frequency range, the greater the resolution for a given counting period; *full-scale-calibration error; gain-temperature coefficient*, in ppm of signal per °C, where "gain" is the ratio of full-scale frequency to full-scale voltage, *input-offset temperature coefficient; overrange capability*, within rated specifications, and *step response*, the worst-case time interval required for the frequency to respond to a full-scale-step input change.

For FVC's, important specs, in addition to accuracy specs corresponding to the above, include *output ripple* (for specified input frequencies), *threshold* (for recognition that another cycle has been initiated, and for versatility in interfacing various types of sensors directly), *hysteresis*, to provide a degree of insensitivity to noise superimposed on a slowly-varying input waveform, and *dynamic response* (important in motor control).

Definitions of some critical specifications, and the conditions for adjusting or measuring them, are detailed on individual data sheets.

ANALOG DEVICES

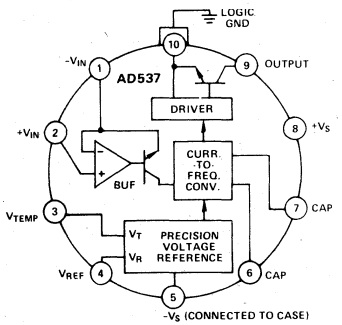
Integrated Circuit Voltage-to-Frequency Converter

AD537*

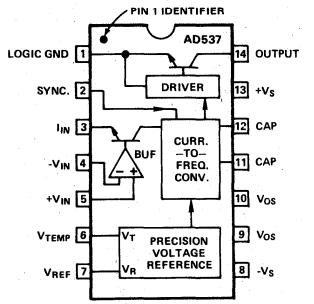
FEATURES

- Low Cost A-D Conversion
- Versatile Input Amplifier
  - Positive or Negative Voltage Modes
  - Negative Current Mode
  - High Input Impedance, Low Drift
- Single Supply, 5 to 36 Volts
- Linearity: ±0.05% FS
- Low Power: 1.2mA Quiescent Current
- Full Scale Frequency up to 100kHz
- 1.00 Volt Reference
- Thermometer Output (1mV/K)
- F-V Applications

AD537 FUNCTIONAL BLOCK DIAGRAMS



TO-100
TOP VIEW



TO-116 STYLE
TOP VIEW

PRODUCT DESCRIPTION

The AD537 is a monolithic V-F converter consisting of an input amplifier, a precision oscillator system, an accurate internal reference generator and a high current output stage. Only a single external RC network is required to set up any full scale (F.S.) frequency up to 100kHz and any F.S. input voltage up to ±30V. Linearity error is as low as ±0.05% for 10kHz F.S., and operation is guaranteed over an 80dB dynamic range. The overall temperature coefficient (excluding the effects of external components) is typically ±30ppm/°C. The AD537 operates from a single supply of 5 to 36V and consumes only 1.2mA quiescent current.

A temperature-proportional output, scaled to 1.00mV/K, enables the circuit to be used as a reliable temperature-to-frequency converter; in combination with the fixed reference output of 1.00V, offset scales such as 0°C or 0°F can be generated.

The low drift (1μV/°C typ) input amplifier allows operation directly from small signals (e.g., thermocouples or strain gages) while offering a high (250MΩ) input resistance. Unlike most V-F converters, the AD537 provides a square-wave output, and can drive up to 12 TTL loads, LEDs, very long cables, etc.

The excellent temperature characteristics and long-term stability of the AD537 are guaranteed by the primary band-gap reference generator and the low T.C. silicon chromium thin film resistors used throughout.

The device is available in either a TO-116 ceramic DIP or a TO-100 metal can; both are hermetically sealed packages.

The AD537 is available in three performance/temperature grades; the J and K grades are specified for operation over the 0 to +70°C range while the AD537S is specified for operation over the extended temperature range, -55°C to +125°C.

*COVERED BY PATENT NUMBERS 3,887,963 and RE 30,586.

PRODUCT HIGHLIGHTS

1. The AD537 is a complete V-F converter requiring only an external RC timing network to set the desired full scale frequency and a selectable pull-up resistor for the open-collector output stage. Any full-scale input voltage range from 100mV to 10 volts (or greater, depending on $+V_S$) can be accommodated by proper selection of timing resistor. The full scale frequency is then set by the timing capacitor from the simple relationship, f = V/10RC.
2. The power supply requirements are minimal, only 1.2mA quiescent current is drawn from a single positive supply from 4.5 to 36 volts. In this mode, positive inputs can vary from 0 volts (ground) to ($+V_S$ - 4) volts. Negative inputs can easily be connected for below ground operation.
3. F-V converters with excellent characteristics are also easy to build by connecting the AD537 in a phase-locked loop. Application particulars are shown in Figure 7.
4. The versatile open-collector NPN output stage can sink up to 20mA with a saturation voltage less than 0.4 volts. The Logic Common terminal can be connected to any level between ground (or $-V_S$) and 4 volts below $+V_S$. This allows easy direct interface to any logic family with either positive or negative logic levels.

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SPECIFICATIONS (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537JH	AD537JD	AD537K	AD537S[1]
CURRENT-TO-FREQUENCY CONVERTER				
Frequency Range	0 to 150kHz	*	*	*
Nonlinearity[1]				
f_{max} = 10kHz	0.15% max (0.1% typ)	*	0.07% max	**
f_{max} = 100kHz	0.25% max (0.15% typ)	*	0.1% max	**
Full Scale Calibration Error				
C = 0.01μF, I_{IN} = 1.000mA	±10% max	±7% max	±5% max	**
vs. Supply (f_{max} < 100kHz)	±0.1%/V max (0.01% typ)	*	*	*
vs. Temp. (T_{min} to T_{max})	±150ppm/°C max (50ppm typ)	*	50ppm/°C max (30ppm typ)[2]	150ppm/°C max
ANALOG INPUT AMPLIFIER				
(Voltage-to-Current Converter)				
Voltage Input Range				
Single Supply	0 to (+V_S - 4) Volts (min)	*	*	*
Dual Supply	-V_S to (+V_S - 4) Volts (min)	*	*	*
Input Bias Current				
(Either Input)	100nA	*	*	*
Input Resistance (Non-Inverting)	250MΩ	*	*	*
Input Offset Voltage				
(Trimmable in "D" Package Only)	5mV max	*	2mV max	**
vs. Supply	200μV/V max	100μV/V max	100μV/V max	**
vs. Temp. (T_{min} to T_{max})	5μV/°C	*	1μV/°C	10μV/°C max
Safe Input Voltage[3]	±V_S	*	*	*
REFERENCE OUTPUTS				
Voltage Reference				
Absolute Value	1.00 Volt ±5% max	*	*	*
vs. Temp. (T_{min} to T_{max})	50ppm/°C	*	100ppm/°C max[3]	**
vs. Supply	±0.03%/V max	*	*	*
Output Resistance[4]	380Ω	*	*	*
Absolute Temperature Reference[5]				
Nominal Output Level	1.00mV/K	*	*	*
Initial Calibration @ +25°C	298mV (±5mV)	*	298mV (±5mV max)	**
Slope Error from 1.00mV/K	±0.02mV/K	*	*	*
Slope Nonlinearity	±0.1K	*	*	*
Output Resistance[5]	900Ω	*	*	*
OUTPUT INTERFACE (Open Collector Output)				
(Symmetrical Square Wave)				
Output Sink Current in Logic "0"				
V_{OUT} = 0.4V max, T_{min} to T_{max})	10mA min	20mA min	20mA min	10mA min
Output Leakage Current in Logic "1"				
(T_{min} to T_{max})	200nA max	*	*	2μA max
Logic Common Level Range	-V_S to (+V_S - 4) Volts	*	*	*
Rise/Fall Times (C_T = 0.01μF)				
I_{IN} = 1mA	0.2μs	*	*	*
I_{IN} = 1μA	1μs	*	*	*
POWER SUPPLY				
Voltage, Rated Performance				
Single Supply	4.5V to 36V	*	*	*
Dual Supply	±5 to ±18V	*	*	*
Quiescent Current	1.2mA (2.5mA max)	*	*	*
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	-55°C to +125°C
Storage	-65°C to +150°C	*	*	*
PACKAGE OPTIONS[6]				
"D" Package: TO-116 Style (D14A)	–	AD537JD	AD537KD	AD537SD
"H" Package: TO-100	AD537JH	–	AD537KH	AD537SH

NOTES

*Specifications same as AD537JH.

**Specifications same as AD537K.

Specifications subject to change without notice.

[1] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[2] Guaranteed not tested.

[3] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be applied to the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor (see Figure 2).

[4] Loading the 1.0 volt or 1mV/K outputs can cause a significant change in overall circuit performance, as indicated in the applications section. To maintain normal operation, these outputs should be operated into the external buffer or an external amplifier.

[5] Temperature reference output performance is specified from 0 to +70°C for "J" and "K" devices, -55°C to +125°C for "S" model.

[6] See Section 19 for package outline information.

CIRCUIT OPERATION

A block diagram of the AD537 is shown on the first page. A versatile operational amplifier (BUF) serves as the input stage; its pupose is to convert and scale the input voltage signal to a drive current in the NPN follower. Optimum performance is achieved when, at the full scale input voltage, a 1mA drive current is delivered to the current-to-frequency converter. The drive current to the current-to-frequency converter (an astable multivibrator) provides both the bias levels and the charging current to the externally connected timing capacitor. This "adaptive" bias scheme allows the oscillator to provide low nonlinearity over the entire current input range of 0.1 to 2000μA. The square wave oscillator output goes to the output driver which provides a floating base drive to the NPN power transistor. This floating drive allows the logic interface to be referenced to a different level than $-V_S$. The "SYNC" input ("D" package only) allows the oscillator to be slaved to an external master oscillator; this input can also be used to shut off the oscillator.

The reference generator uses a band-gap circuit (this allows single-supply operation to 4.5 volts which is not possible with low T.C. zeners) to provide the reference and bias levels for the amplifier and oscillator stages. The reference generator also provides the precision, low T.C. 1.00 volt output and the V_{TEMP} output which tracks absolute temperature at 1mV/K.

V-F CONNECTION FOR POSITIVE INPUT VOLTAGES

The positive voltage input range is from $-V_S$ (ground in single supply operation) to 4 volts below the positive supply. The connection shown in Figure 1 provides a very high (250MΩ) input impedance. The input voltage is converted to the proper drive current at pin 3 by selecting a scaling resistor. The full scale current is 1mA, so, for example a 10 volt range would require a nominal 10kΩ resistor. The trim range required will depend on capacitor tolerance. Full scale currents other than 1mA can be chosen, but linearity will be reduced; 2mA is the maximum allowable drive.

As indicated by the scaling relationship in Figure 1, a 0.01μF timing capacitor will give a 10kHz full scale frequency, and 0.001μF will give 100kHz with a 1mA drive current. The maximum frequency is 150kHz. Polystyrene or NPO ceramic capacitors are preferred for T.C. and dielectric absorption; polycarbonate or mica are acceptable; other types will degrade linearity. The capacitor should be wired very close to the AD537.

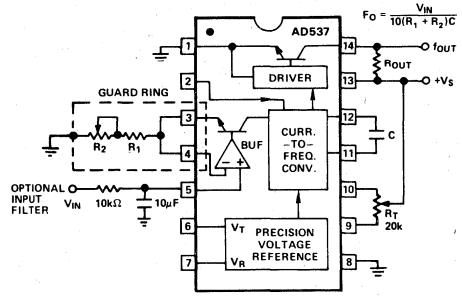

Figure 1. Standard V-F Connection for Positive Input Voltages

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V-F CONNECTIONS FOR NEGATIVE INPUT VOLTAGE OR CURRENT

A wide range of negative input voltages can be accommodated with proper selection of the scaling resistor, as indicated in Figure 2. This connection, unlike the buffered positive connection, is not high impedance since the 1mA F.S. drive current must be supplied by the signal source. However, very large negative voltages beyond the supply can be handled easily; just modify the scaling resistors appropriately. Diode CR1 (HP5082-2811) is necessary for overload and latchup protection for current or voltage inputs.

If the input signal is a true current source, R_1 and R_2 are not used. Full scale calibration can be accomplished by connecting a 200kΩ pot in series with a fixed 27kΩ from pin 7 to $-V_S$ (see calibration section, below).

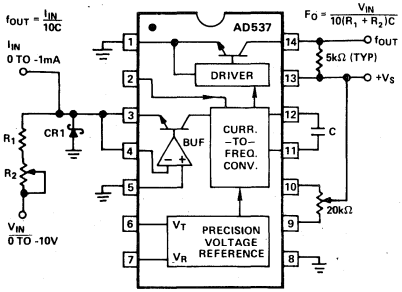


Figure 2. V-F Connections for Negative Input Voltage or Current

CALIBRATION

There are two independent adjustments: scale and offset. The first is trimmed by adjustment of the scaling resistor R and the second by the (optional) potentiometer connected to $+V_S$ and the V_{OS} pins ("D" package only). Precise calibration requires the use of an accurate voltage standard set to the desired FS value and a frequency meter; a scope is useful for monitoring output waveshape. Verification of linearity requires the availability of a switchable voltage source (or a DAC) having a linearity error below ±0.005%, and the use of long measurement intervals to minimize count uncertainties. *Every AD537 is automatically tested for linearity,* and it will not usually be necessary to perform this verification, which is both tedious and time-consuming.

Although drifts are small it is good practice to allow the operating environment to attain stable temperature and to ensure that the supply, source and load conditions are proper.

Begin by setting the input voltage to 1/10,000 of full scale. Adjust the offset pot until the output frequency is 1/10,000 of full scale (for example 1Hz for FS of 10kHz). This is most easily accomplished using a frequency meter connected to the output. Then apply the FS input voltage and adjust the gain pot until the desired FS frequency is indicated. In applications where the FS input is small, this adjustment will very slightly affect the offset voltage, due to the input bias current of the buffer amplifier. A change of 1kΩ in R will affect the input by approximately 100μV, which is as much as 0.1% of a 100mV FS range. Therefore, it may be necessary to repeat the offset and scale adjustments for the highest accuracy. The design of the input amplifier is such that the input voltage drift after offset nulling is typically below 1μV/°C.

In some cases the signal may be in the form of a negative current source. This can be handled in a similar way to a negative input voltage. However, the scaling resistor is no longer required, eliminating the capability of trimming full scale in this fashion. Since it will usually be impractical to vary the capacitance, an alternative calibration scheme is needed. This is shown in Figure 3. A resistor-potentiometer connected from the V_R output to $-V_S$ will alter the internal operating conditions in a predictable way, providing the necessary adjustment range. With the values shown, a range of ±4% is available; a larger range can be attained by reducing R1. This technique does not degrade the temperature-coefficient of the converter, and the linearity will be as for negative input voltages. The minimum supply voltage may be used.

Unless it is required to set the input node at exactly ground potential, no offset adjustment is needed. The capacitor C is selected to be 5% below the nominal value; with R2 in its mid-position the output frequency is given by

$$f = \frac{I}{10.5 \times C}$$

where f is in kHz, I is in mA and C is in μF. For example, for a FS frequency of 10kHz at a FS input of 1mA, C = 9500pF. Calibration is effected by applying the full-scale input and adjusting R2 for the correct reading.

This alternative adjustment scheme may also be used when it is desired to present an exact input resistance in the negative-voltage mode. The scaling relationship is then

$$f = \frac{V}{R_{exact}} \cdot \frac{1}{10.5\ C}$$

The calibration procedure is then similar to that used for positive input voltages, except that the scale adjustment is by means of R2.

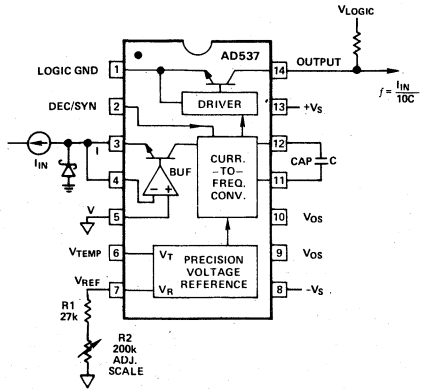


Figure 3. Scale Adjustment for Current Inputs

INPUT PROTECTION

The AD537 was designed to be used with a minimum of additional hardware. However, the successful application of a precision IC involves a good understanding of possible pitfalls and the use of suitable precautions.

The $-V_{IN}$, $+V_{IN}$ and I_{IN} pins should not be driven more than 300mV below $-V_S$. This would cause internal junctions to conduct, possibly damaging the IC. The AD537 can be protected from "below $-V_S$" inputs by a Schottky diode, CR1 (HP5082-2811) as shown in Figure 4. It is also desirable not to drive $+V_{IN}$, $-V_{IN}$ and I_{IN} above $+V_S$. In operation, the converter will become very nonlinear for inputs above ($+V_S$ -3.5V). Control currents above 2mA will also cause nonlinearity.

The 80dB dynamic range of the AD537 guarantees operation from a control current of 1mA (nominal FS) down to 100nA (equivalent to 1mV to 10V FS). Below 100nA improper operation of the oscillator may result, causing a false indication of input amplitude. In many cases this might be due to short-lived noise spikes which become added to the input. For example, when scaled to accept a FS input of 1V, the -80dB level is only 100μV, so when the mean input is only 60dB below FS (1mV), noise spikes of 0.9mV are sufficient to cause momentary malfunction.

This effect can be minimized by using a simple low-pass filter ahead of the converter and a guard ring around the I_{IN} or $-V_{IN}$ pins. For a FS of 10kHz a single-pole filter with a time-constant of 100ms (Figure 3) will be suitable, but the optimum configuration will depend on the application and type of signal processing. Noise spikes are only likely to be a cause of error when the input current remains near its minimum value for long periods of time; above 100nA (1mV) full integration of additive input noise occurs.

The AD537 is somewhat susceptible to interference from other signals. The most sensitive nodes (besides the inputs) are the capacitor terminals and the SYNC pin. The timing capacitor should be located as close as possible to the AD537 to minimize signal pickup in the leads. In some cases, guard rings or shielding may be required. The SYNC pin should be decoupled through a 0.005μF (or larger) capacitor to pin 13 ($+V_S$). This minimizes the possibility that the AD537 will attempt to synchronize to a spurious signal. This precaution is unnecessary on the metal can package since the SYNC function is not brought out to a package pin and is thus not susceptible to pickup.

DECOUPLING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD537.

A decoupling capacitor may also be useful from $+V_S$ to SYNC in those applications where very low cycle-to-cycle period variation (jitter) is demanded. By placing a capacitor across $+V_S$ and SYNC this noise is reduced. On the 10kHz FS range, a 6.8μF capacitor reduces the jitter to one in 20,000 which is adequate for most applications. A tantalum capacitor should be used to avoid errors due to dc leakage.

NONLINEARITY SPECIFICATION

The preferred method for specifying linearity error is in terms of the maximum deviation from the ideal relationship after calibrating the converter at full scale and "zero". This error will vary with the full scale frequency and the mode of operation. The AD537 operates best at a 10kHz full scale frequency with a negative voltage input; the linearity is typically within ±0.05%. Operating at higher frequencies or with positive inputs will degrade the linearity as indicates in the Specifications table. The shape of a typical linearity plot is given in Figure 4.

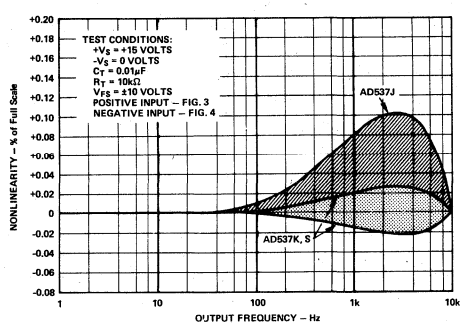


Figure 4a. Typical Nonlinearity Error Envelopes with 10kHz F.S. Output

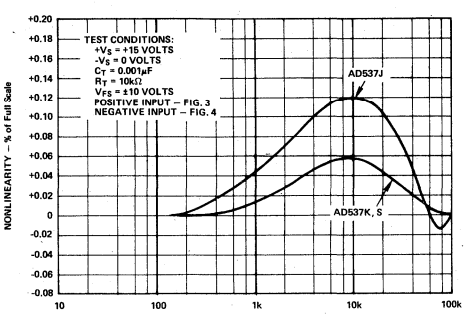
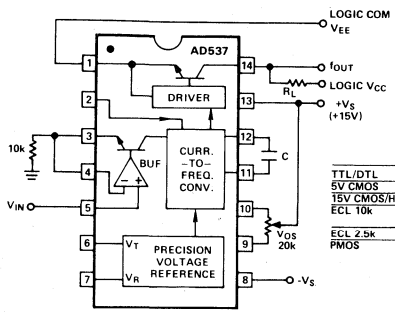


Figure 4b. Typical Nonlinearity Error with 100kHz F.S. Output

OUTPUT INTERFACING CONSIDERATIONS

The design of the output stage allows easy interfacing to all digital logic families. The collector and emitter of the output NPN transistor are both uncommitted; the emitter can be tied to any voltage between $-V_S$ and 4 volts below $+V_S$. The open collector can be pulled up to a voltage 36 volts above the emitter regardless of $+V_S$. The high power output stage can supply up to 20mA (10mA for "H" package) at a maximum saturation voltage of 0.4 volts. The stage limits the output current at 25mA; it can handle this limit indefinitely without damaging the device.

Figure 5 shows the AD537 with a standard 0 to +10 volt input connection and the output stage connections. The values for the logic common voltage, pull-up resistor, positive logic level, and $-V_S$ supply are given in the accompanying chart for several logic forms.



	VCC	VEE	RL	-VS
TTL/DTL	+5	GND	5k	GND
5V CMOS	+5	GND	20k	GND
15V CMOS/HNIL	+15	GND	10k	GND
ECL 10k	0	-8	5k	-8 to -15
ECL 2.5k	+1.3	-2	5k	-5
PMOS	0	-15	10k	-15

Figure 5. Interfacing Standard Logic Families

APPLICATIONS

The diagrams and descriptions of the following applications are provided to stimulate the discerning engineer with alternative circuit design ideas. "Applications of the AD537 IC Voltage-to-Frequency Converter", available from Analog Devices on request, covers a wider range of topics and concepts in data conversion and data transmission using voltage-to-frequency converters.

TRUE TWO-WIRE DATA TRANSMISSION

Figure 6 shows the AD537 in a true two-wire data transmission scheme. The twisted-pair transmission line serves the dual purpose of supplying power to the device and also carrying frequency data in the form of current modulation. The PNP circuit at the receiving end represents a fairly simple way for converting the current modulation back into a voltage square wave which will drive digital logic directly. The 0.6 volt square wave which will appear on the supply line at the device terminals does not affect the performance of the AD537 because of its excellent supply rejection. Also, note that the circuit operates at nearly constant average power regardless of frequency.

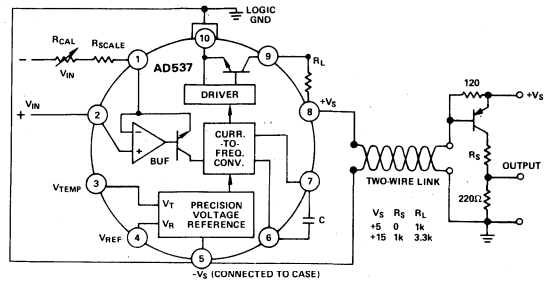


Figure 6. True Two-Wire Operation

F-V CONVERTERS

The AD537 can be used as a high linearity VCO in a phase-locked loop to accomplish frequency-to-voltage conversion. By operating the loop without a low-pass filter in the feedback path (first-order system), it can lock to any frequency from zero to an upper limit determined by the design, responding in three or four cycles to a step change of input frequency. In practice, the overall response time is determined by the characteristics of the averaging filter which follows the PLL.

Figure 7 shows a connection using a low-power TTL quad open-collector nand gate which serves as the phase comparator. The input signal should be a pulse train or square wave with characteristics similar to TTL or 5-volt CMOS outputs. Any duty cycle is acceptable, but the minimum pulse width is 40μs. The output voltage is one volt for a 10kHz input frequency. The output as shown here is at a fairly high impedance level; for many situations an additional buffer may be required.

Trimming is similar to V-F application trimming. First set the V_{OS} trimmer to mid-scale. Apply a 10kHz input frequency and trim the 2kΩ potentiometer for 1.00 volts out. Then apply a 10Hz waveform and trim the V_{OS} for 1mV out. Finally, retrim the full scale output at 10kHz. Other frequency scales can be obtained by appropriate scaling of timing components.

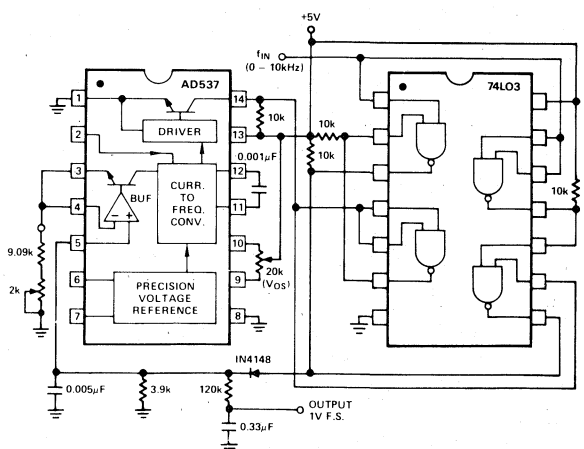


Figure 7. 10kHz F-V Converter

TEMPERATURE-TO-FREQUENCY CONVERSION

The linear temperature-proportional output of the AD537 can be used as shown in these applications to perform various direct temperature-to-frequency conversion functions; it can also be used with other external connections in a temperature sensing or compensation scheme. If the sensor output is used externally, it should be buffered through an op amp since loading that point will cause significant error in the sensor output as well as in the main V-F converter circuitry.

An absolute temperature (Kelvin) -to-frequency converter is very easily accomplished, as shown in Figure 8. The 1mV per K output serves as the input to the buffer amplifier, which then scales the oscillator drive current to a nominal 298μA at +25°C (298K). Use of a 1000pF capacitor results in a corresponding frequency of 2.98kHz. Setting the single 2kΩ trimmer for the correct frequency at a well-defined temperature near +25°C will normally result in an accuracy of ±2°C from -55°C to +125°C (using an AD537S). An NPO ceramic capacitor is recommended to minimize nonlinearity due to capacitance drift.

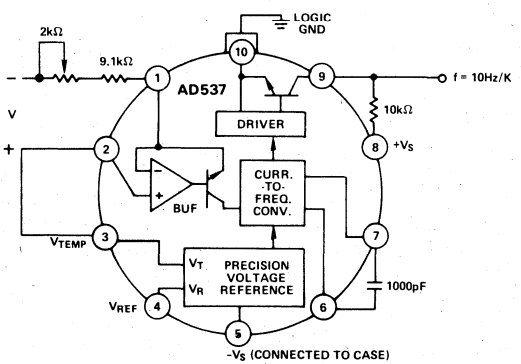


Figure 8. Absolute Temperature to Frequency Converter

OFFSET TEMPERATURE SCALES

Many other temperature scales can be set up by offsetting the temperature output with the voltage reference output. Such a scheme is shown by the Celsius-to-frequency converter in Figure 9. Corresponding component values for a Fahrenheit-to-frequency converter which give 10Hz/°F are given in parentheses.

A simple calibration procedure which will provide ±2°C accuracy requires substitution of a 7.27k resistor for the series combination of the 6.04k with the 2k trimmer; then simply set the 500Ω trimmer to give 250Hz at +25°C.

High accuracy calibration procedure:

1. Measure room temperature in K.
2. Measure temperature output at pin 6 at that temperature.
3. Calculate offset adjustment as follows:

$$\text{Offset Voltage (mV)} = \frac{V_{TEMP}\ (\text{pin 6})\ (\text{mV})}{\text{Room temp (K)}} \times 273.2$$

4. Temporarily disconnect 49Ω resistor (or 500Ω pot) and trim 2kΩ pot to give the offset voltage at the indicated node. Reconnect 49Ω resistor.
5. Adjust slope trimmer to give proper frequency at room temperature (+25°C = 250Hz).
   Adjustment for °F or any other scale is analogous.

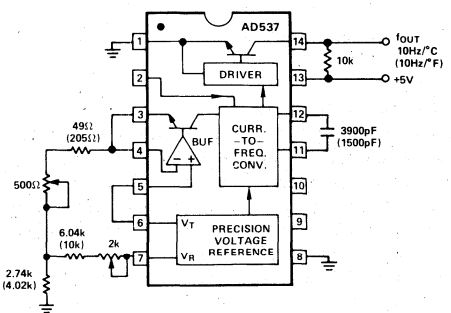


Figure 9. Offset Temperature Scale Converters-Centigrade and (Fahrenheit) to Frequency

SYNCHRONOUS OPERATION

The SYNC terminal at pin 2 of the DIP package can be used to synchronize a free running AD537 to a master oscillator, either at a multiple or a sub-multiple of the primary frequency. The preferred connection is shown in Figure 10. The diodes are used to produce the proper drive magnitude from high level signals. The SYNC terminal can also be used to shut off the oscillator. Shorting the terminal to $+V_S$ will stop the oscillator, and the output will go high (output NPN off).

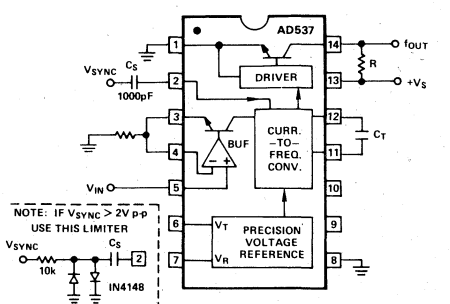


Figure 10. Connection for Synchronous Operation

Figure 12 shows the maximum pull-in range available at a given signal level; the optimum signal is a 0.8 to 1.0 volt square wave; signals below 0.1 volt will have no effect; signals above 2 volts p-p will disable the oscillator. The AD537 can normally be synchronized to a signal which forces it to a higher frequency up to 30% above the nominal free-running frequency, it can only be brought down about 1-2%.

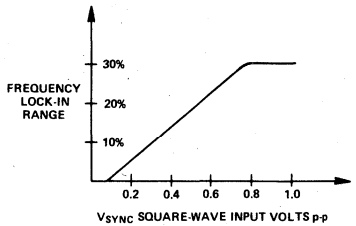


Figure 11. Maximum Frequency Lock-In Range Versus Sync. Signal

LINEAR PHASE LOCKED LOOP

The phase-locked-loop F/V circuit described earlier operates from an essentially noise-free binary input. PLL's are also used to extract frequency information from a noisy analog signal. To do this, the digital phase-comparator must be replaced by a linear multiplier. In the implementation shown in Figure 12, the triangular waveform appearing across the timing capacitor is used as one of the multiplier inputs; the signal provides the other input. It can be shown that the mean value of the multiplier output is zero when the two signals are in quadrature. In this condition, the ripple in the error signal is also quite small. Thus, the voltage at pin 5 is essentially zero, and the frequency is determined primarily by the current in the timing resistor, controlled either manually or by a control voltage.

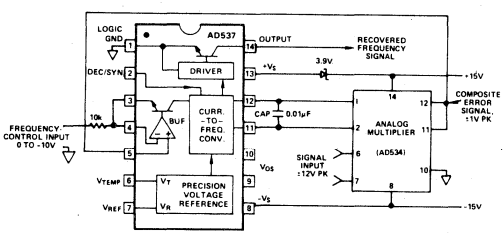


Figure 12. Linear Phase-Locked Loop

Noise on the input signal affects the loop operation only slightly; it appears as noise in the timing current, but this is averaged out by the timing capacitor. On the other hand, if the input frequency changes there is a net error voltage at pin 5 which acts to bring the oscillator back into quadrature. Thus, the output at pin 14 is a noise-free square-wave having exactly the same frequency as the input signal. The effectiveness of this circuit can be judged from Figure 13 which shows the response to an input of 1V rms 1kHz sinusoid plus 1V rms Gaussian noise. The positive supply to the AD537 is reduced by about 4V in order to keep the voltages at pins 11 and 12 within the common-mode range of the AD534.

Since this is also a first-order loop the circuit possesses a very wide capture range. However, even better noise-integrating properties can be achieved by adding a filter between the multiplier output and the VCO input. Details of suitable filter characteristics can be found in the standard texts on the subject.

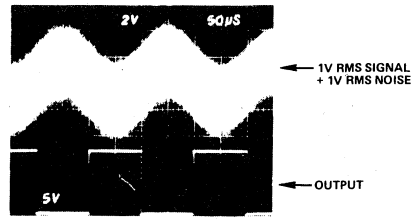


Figure 13. Performance of AD537 Linear Phase-Locked Loop

By connecting the multiplier output to the lower end of the timing resistor and moving the control input to pin 5, a high-resistance frequency-control input is made available. However, due to the reduced supply voltage, this input cannot exceed +6V.

TRANSDUCER INTERFACE

The AD537 was specifically designed to accept a broad range of input signals, particularly small voltage signals, which may be converted directly (unlike many V-F converters which require signal pre-conditioning). The 1.00V stable reference output is also useful in interfacing situations, and the high input resistance allows non-loading interfacing from a source of varying resistance, such as the slider of a potentiometer.

THERMOCOUPLE INPUT

The output of a Chromel-Constantan (Type E) thermocouple, using a reference junction at 0°C, varies from 0 to 53.14mV over the temperature range 0 to +700°C with a slope of 80.678μV/degree over most of its range and some nonlinearity over the range 0 to +200°C. For this example, we assume that it is desired to indicate temperature in Degrees Celsius using a counter/display with a 100ms gate width. Thus, the V-F converter must deliver an output of 7kHz for an input of 53.14mV. If very precise operation down to 0°C is imperative, some sort of linearizing is necessary (see, for example, Analog Devices' Nonlinear Circuits Handbook, pp92-97) but in many cases operation is only needed over part of the range.

The circuit shown in Figure 14 provides good accuracy from +300°C to +700°C. The extrapolation of the temperature-voltage curve back to 0°C shows that an offset of -3.34mV is required to fit the curve most exactly. This small amount of voltage can be introduced without an additional calibration step using the +1.00V output of the AD537. To adjust the scale, the thermocouple should be raised to a known reference temperature near 500°C and the frequency adjusted to value using R1. The error should be within ±0.2% over the range 400°C to 700°C.

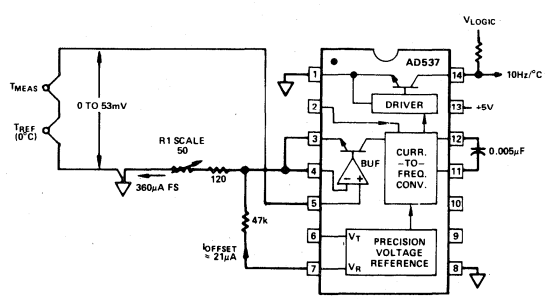


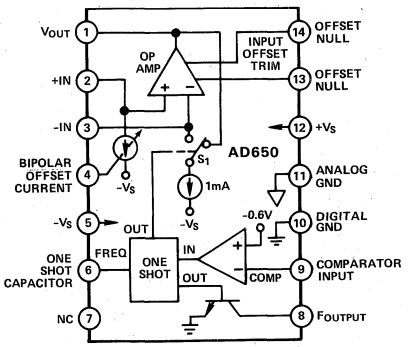
Figure 14. Thermocouple Interface with First-Order Linearization

Voltage-to-Frequency and Frequency-to-Voltage Converter

AD650

FEATURES
V/F Conversion to 1MHz
Reliable Monolithic Construction
Very Low Nonlinearity
0.002% typ at 10kHz
0.005% typ at 100kHz
0.07% typ at 1MHz
Input Offset Trimmable to Zero
CMOS or TTL Compatible
Unipolar, Bipolar, or Differential V/F
V/F or F/V Conversion

AD650 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20ppm (0.002% of full scale) and 50ppm (0.005%) maximum at 10kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades, allowing extremely high resolution measurements. Even at 1MHz full scale, linearity is guaranteed less than 1000ppm (0.1%) on the AD650KN, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased-locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package and are specified for the commerical (0 to +70°C) temperature range. For industrial temperature range (−25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full −55°C to +125°C extended temperature range.

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PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full scale output frequency up to 1MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pullup resistor can be connected to voltages up to +30V, or +15V or +5V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.

SPECIFICATIONS (@ +25°C with V_S = ±15V, unless otherwise noted)

Model	AD650J/AD650A Min	Typ	Max	AD650K/AD650B Min	Typ	Max	AD650S Min	Typ	Max	Units
DYNAMIC PERFORMANCE										
Full Scale Frequency Range	0		1	0		1	0		1	MHz
Nonlinearity[1] f_{max} = 10kHz		0.002	**0.005**		0.002	**0.005**		0.002	**0.005**	%
100kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
500kHz		0.02	**0.05**		0.02	**005**		002	**0.05**	%
1MHz		0.1			0.07	**0.1**		0.07	**0.1**	%
Full Scale Calibration Error[2], 100kHz		±5			5			5		%
1MHz		±10			±10			±5		%
vs. Supply[3]			**±0.002**			**±0.002**			**±0.002**	of FSR/%
vs. Temperature										
A, B, and S Grades										
at 10kHz			±75			±75			±75	ppm/°C
at 100kHz			±150			±150			±150	ppm/°C
J and K Grades										
at 10kHz		±75			±75					ppm/°C
at 100kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24kΩ between pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
Overload Recovery Time										
Step Input	1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			1 Pulse of New Frequency Plus 1µs			
ANALOG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	−10		0	−10		0	−10		0	V
Differential Impedance		2MΩ‖10pF			2MΩ‖10pF			2MΩ‖10pF		
Common Mode Impedance		1000MΩ‖10pF			1000MΩ‖10pF			1000MΩ‖10pF		
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	**±20**		±8	**±20**		±8	**±20**	nA
Input Offset Voltage										
(Trimmable to Zero)			**±4**			**±4**			**±4**	mV
vs. Temperature (T_{min} to T_{max})		±30			±30			±30		µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		C
COMPARATOR (F/V Conversion)										
Logic "0" Level	$-V_S$		−1	$-V_S$		−1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0"										
$I_{SINK} \leq 8mA$, T_{min} to T_{max}			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			100			100			100	nA
Voltage Range[5]	0		+36	0		+36	0		+36	V
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (1500Ω min load resistance)	0		+10	0		+10	0		+10	V
Source Current (750Ω max load resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9V		**±18**	±9V		**±18**	±9V		**±18**	V
Quiescent Current			**8**			**8**			**8**	mA
TEMPERATURE RANGE										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	−25°C		+85	−25		+85	−55°C		+125°C	
Storage – N Package	−25°C		+85	−25		+85				°C
D Package	−65°C		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[6]										
Plastic DIP – N14A		AD650JN			AD650KN					
Ceramic DIP – D14A		AD650AD			AD650BD			AD650SD		

NOTES

[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.
[2]Full scale calibration error adjustable to zero.
[3]Measured at full scale output frequency of 10kHz.
[4]Refer to F/V conversion section of the text.
[5]Referred to digital ground.
[6]See Section 19 for package outline information.

*Specifications same as AD650J/A.
**Specifications same as AD650K/B.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ORDERING GUIDE

Part Number	Gain Tempco ppm/°C 100kHz	1MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650AD	150 max	0.1% typ	−25 to +85	Ceramic
AD650BD	150 max	0.1% max	−25 to +85	Ceramic
AD650SD	150 max	0.1% max	−55 to +125	Ceramic

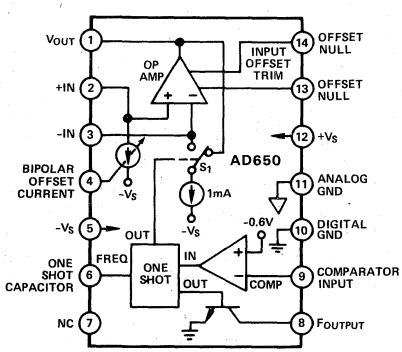
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage $+V_S$ to $-V_S$ 36V
Storage Temperature Ceramic . . . . . −55°C to +165°C
Plastic . . . . . −25°C to +125°C
Differential Input Voltage (Pins 2 & 3) . . . . . ±10V
Maximum Input Voltage . . . . . $\pm V_S$
Open Collector Output Voltage Above Digital GND . . 36V
Current 50mA
Amplifier Short Ckt to Ground . . . . . Indefinite
Comparator Input Voltage (Pin 9) . . . . . $\pm V_S$

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts from the switched 1mA internal current source. These bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.



AD650 Pin Configuration

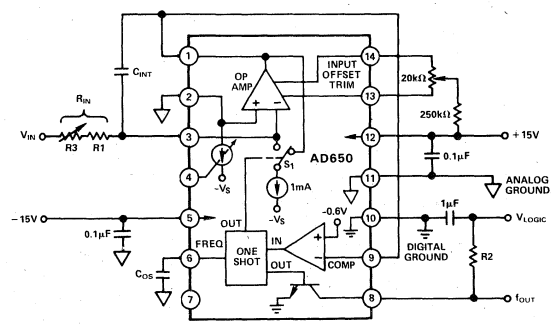


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V to F converter is shown in Figure 2a. The unit is comprised of an input integrator, a current source and steering switch, a comparator and a one-shot. When the output of the one-shot is low, the current steering switch S_1 diverts all the current to the output of the op amp; this is called the Integration Period. When the one-shot has been triggered, and its output is high, the switch S_1 diverts all the current to the summing junction of the op amp; this is called the Reset Period. The two different states are shown in Figure 2 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

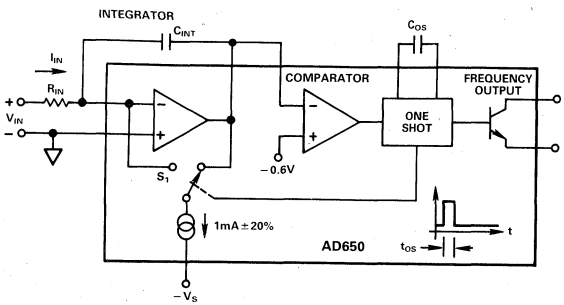


Figure 2a. Block Diagram

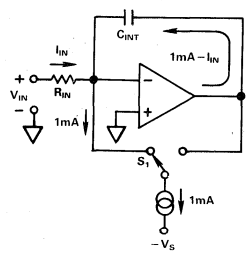


Figure 2b. Reset Mode

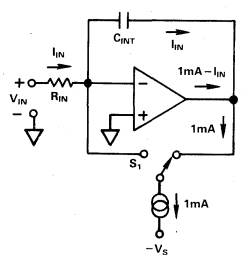


Figure 2c. Integrate Mode

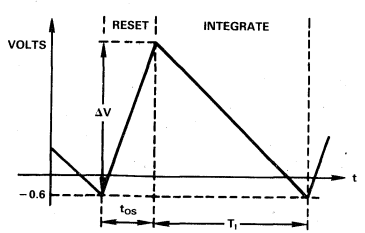


Figure 2d. Voltage Across C_{INT}

The positive input voltage develops a current ($I_{IN} = V_{IN}/R_{IN}$) which charges the integrator capacitor C_{INT}. As charge builds up on C_{INT}, the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (pin 1) crosses the comparator threshold (−0.6 volt) the comparator triggers the one shot, whose time period, t_{OS} is determined by the one shot capacitor C_{OS}.

Specifically, the one shot time period is:

$$t_{OS} = C_{OS} \times 6.8 \times 10^3\ sec/F + 3.0 \times 10^{-7} sec \quad (1)$$

The Reset Period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount:

$$\Delta V = t_{OS} \cdot \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}} \left(1mA - I_{IN}\right) \quad (2)$$

After the Reset Period has ended, the device starts another Integration Period, as shown in Figure 2, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as:

$$T_I = \frac{\Delta V}{\frac{dV}{dt}} = \frac{t_{OS}/C_{INT}(1mA - I_{IN})}{I_{IN}/C_{INT}} = t_{OS}\left(\frac{1mA}{I_{IN}} - 1\right) \quad (3)$$

The output frequency is now given as:

$$f_{OUT} = \frac{1}{t_{OS} + T_I} = \frac{I_{IN}}{t_{OS} \times 1mA} = 0.15\ \frac{F \cdot Hz}{A}\ \frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} F} \quad (4)$$

Note that C_{INT}, the integration capacitor has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

One Shot Timing

A key part of the preceding analysis is the one shot time period that was given in equation (1). This time period can be broken down into approximately 300ns of propagation delay, and a second time segment dependent linearly on timing capacitor C_{OS}. When the one shot is triggered, a voltage switch that holds pin 6 at analog ground is opened allowing that voltage to change. An internal 0.5mA current source connected to pin 6 then draws its current out of C_{OS}, causing the voltage at pin 6 to decrease linearly. At approximately −3.4V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one shot time period can be written mathematically as:

$$t_{OS} = \frac{\Delta V\ C_{OS}}{I_{DISCHARGE}} + T_{GATE\ DELAY} \quad (5)$$

substituting actual values quoted above,

$$t_{OS} = \frac{-3.4V \times C_{OS}}{-0.5 \times 10^{-3} A} + 300 \times 10^{-9} sec \quad (6)$$

This simplifies into the timed period equation given above.

COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance R_{IN}, timing capacitor C_{OS}, logic resistor R_2, and integration capacitor C_{INT}. The first two determine the input voltage and full scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R_2 is the easiest to define. As a pull up resistor, it should be chosen to limit the current through the output transistor to 8mA if a TTL maximum V_{OL} of 0.4V is desired. For example, a 5V logic supply is used, R_2 should be no smaller than 5V/8mA or 625Ω. A larger value can be used if desired.

R_{IN} and C_{OS} are the only two parameters available to set the full scale frequency to accommodate the given signal range. The

"swing" variable that is affected by the choice of R_{IN} and C_{OS} is nonlinearity. The selection guide of Figure 3 shows this quite graphically. In general, larger values of C_{OS} and lower full scale input currents (higher values of R_{IN}) provide better linearity. In Figure 3, the implications of four different choices of R_{IN} are shown. Although the selection guide is set up for a unipolar configuration with a zero to 10V input signal range, the results can be extended to other configurations and input signal ranges. For a full scale frequency of 100kHz (corresponding to 10V input), you can see that among the available choices, $R_{IN} = 20k$ and $C_{OS} = 620pF$ gives the lowest nonlinearity, 0.0038%. Also, if you wish to use the highest frequency that will give the 20ppm minimum nonlinearity, it is approximately 33kHz (40.2kΩ and 1000pF).

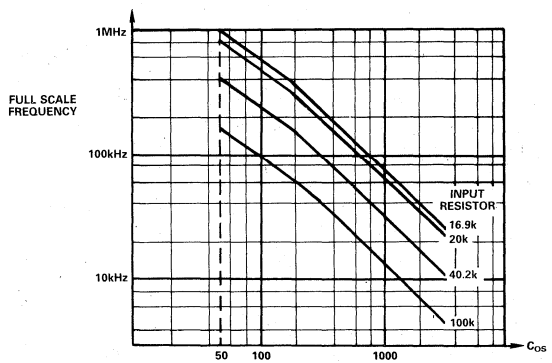


Figure 3a. Full Scale Frequency vs. C_{OS}

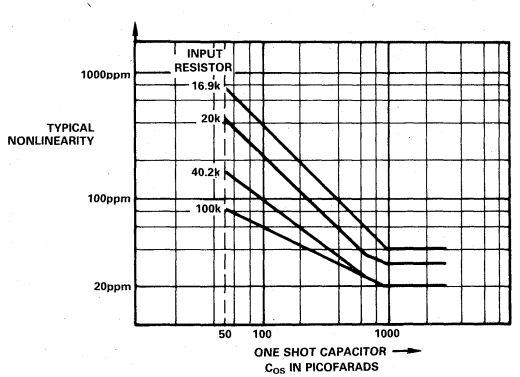


Figure 3b. Typical Nonlinearity vs. C_{OS}

For input signal spans other than 10V, the input resistance must be scaled proportionately. For example, if 100kΩ is called out for a 0–10V span, 10k would be used with a 0–1V span, or 200kΩ with a ±10V bipolar connection.

The last component to be selected is the integration capacitor C_{INT}. In almost all cases, the best value for C_{INT} can be calculated using the equation:

$$C_{INT} = \frac{10^{-4} F/sec}{f_{MAX}} \quad (1000pF \text{ minimum}) \qquad (7)$$

When the proper value for C_{INT} is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, hence large amounts of noise and interference can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, the continuous integration of the signal will be interrupted, allowing the noise to appear at the output. If the approximate amount of noise that will appear on C_{INT} is known (V_{NOISE}), the value of C_{INT} can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS} \times 1 \times 10^{-3} A}{+V_S - 3V - V_{NOISE}} \qquad (8)$$

For example, consider an application calling for a maximum frequency of 75kHz, a 0–1 volt signal range, and supply voltages of only ±9 volts. The component selection guide of Figure 3 is used to select 2.0kΩ for R_{IN} and 1000pF for C_{OS}. This results in a one shot time period of approximately 7μs. Substituting 75kHz into equation 7 yields a value of 1300pF for C_{INT}. When the input signal is near zero, 1mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across C_{INT} to increase by approximately 5.5 volts. Since the integrator output stage requires approximately 3 volts head room for proper operation, only 0.5 volt margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time might saturate the integrator, causing an error in signal integration. Increasing C_{INT} to 1500 or 2000pF will provide much more noise margin, thereby eliminating this potential trouble spot.

BIPOLAR V/F

Figure 4 shows how the internal bipolar current sink is used to provide a half-scale offset for a ±5V signal range, while providing a 100kHz maximum output frequency. The nominally 0.5mA (±10%) offset current sink is enabled when a 1.24kΩ resistor is connected between pins 4 and 5. Thus, with the grounded 10kΩ nominal resistance shown, a −5V offset is developed at pin 2. Since pin 3 must also be at −5V, the current through R_{IN} is 10V/40kΩ = +0.25mA at V_{IN} = +5V, and 0mA at V_{IN} = −5V.

Components are selected using the same guidelines outlined for the unipolar configuration with one alteration. The voltage

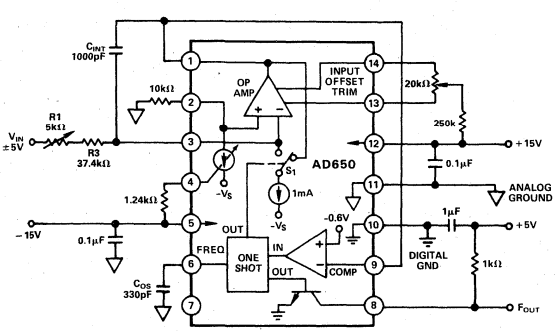


Figure 4. Connections for ±5V Bipolar V/F with 0 to 100kHz TTL Output

across the total signal range must be equated to the maximum input voltage in the unipolar configuration. In other words, the value of the input resistor R_{IN} is determined by the input voltage span, not the maximum input voltage.

As in the unipolar circuit, R_{IN} and C_{OS} must have low temperature coefficients to minimize the overall gain drift. The 1.24kΩ resistor used to activate the 0.5mA offset current should also have a low temperature coefficient. The bipolar offset current has a temperature coefficient of approximately −200ppm/°C.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 5 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source may be used since it only drives the noninverting integrator input. Typical input impedance at this terminal is 1GΩ or higher. For V/F conversion of positive input signals using the connection diagram of Figure 1, the signal generator must be able to source the integration current to drive the AD650. For the negative V/F conversion circuit of Figure 5, the integration current is drawn from ground through R1 and R3, and the active input is high impedance.

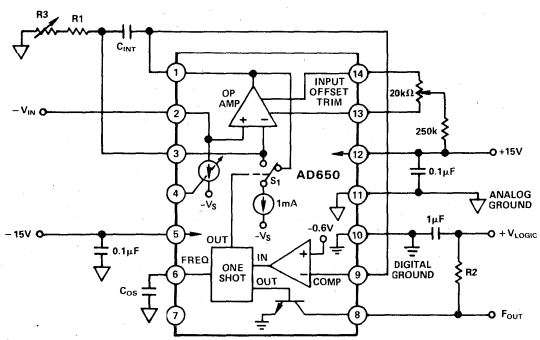


Figure 5. Connection Diagram for V/F Conversion, Negative Input Voltage

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in a previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

The AD650 also makes a very linear frequency-to-voltage converter. Figure 6 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshhold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C_{OS}). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

The circuit of Figure 6 can be biased to accommodate almost any input signal waveform. With a TTL input, the 1000pF coupling capacitor and 2.2kΩ resistor creates a clean negative spike that triggers the one shot on negative going edges. For

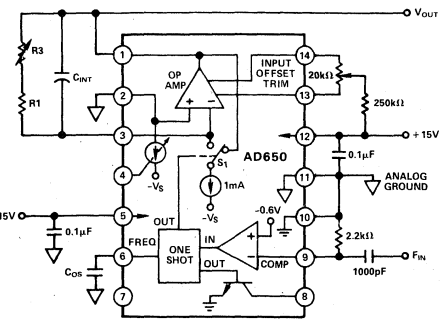


Figure 6. Connection Diagram for F/V Conversion

input signals with slower edges, a larger capacitor and/or resistor may be used as long as the comparator is never exposed to a voltage lower than −0.6V for longer than the one shot time period. If this happens, the one shot will trigger itself more than once per cycle, creating discontinuities in the F/V transfer function. An input pulse greater than 100ns but less than $0.3 \times t_{OS}$ is recommended (t_{OS} is defined by equation 1 in the circuit operation section, unipolar configuration).

HIGH FREQUENCY OPERATION

Proper RF techniques must be observed when operating the AD650 at or near its maximum frequency of 1MHz. Lead lengths must be kept as short as possible, especially on the one shot and integration capacitors, and at the integrator summing junction. In addition, at maximum output frequencies above 500kHz, a 3.6kΩ pulldown resistor from pin 1 to $-V_S$ is required (see Figure 7). The additional current drawn through the pulldown resistor reduces the op amp's output impedance and improves its transient response.

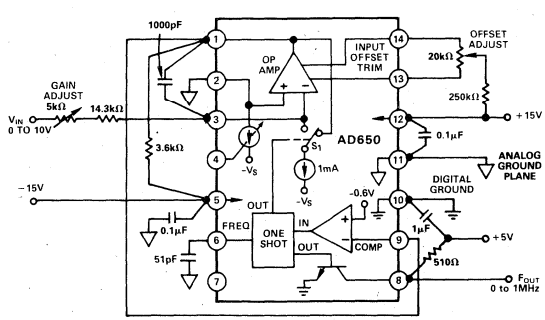


Figure 7. 1MHz V/F Connection Diagram

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 to 100Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1μF to 1.0μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to

exploit the full linearity and dynamic range of the AD650. Although some types of circuits may operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1MHz full scale it is necessary to use a pull-up resistor of about 500Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10mA. This much current being switched will surely cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20nH per inch; a current of 10mA being switched in 50ns at the end of 12 inches of 20 gauge wire will produce a voltage spike of 50mV. The separate digital ground of the AD650 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A 1μF to 10μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground – pin 10. The pull-up resistor should be connected directly to the frequency output – pin 8. The lead lengths on the bypass capacitor and the pull up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There may also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause any problem. In fact, the AD650 will tolerate as much as 0.25 volt dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (pin 11) at the package. All of the signal grounds should be tied directly to pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in reference 1.

TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_{OS} directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a 100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

150ppm/°C (AD650A) + 100ppm/°C (C_{OS}) + 10ppm/°C (R_{IN}) = 260ppm/°C

In bipolar configuration, the drift of the 1.24kΩ resistor used to activate the internal bipolar offset current source will directly affect the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input (pin 2), see Figure 4. That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp noninverting input will be determined solely by the AD650. Under these conditions the TC of the bipolar offset voltage is typically −200ppm/°C and is a maximum of −300ppm/°C. The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not so different from the nominal value as to preclude operation. This includes the integration capacitor, C_{INT}. A change in the capacitance value of C_{INT} simply results in a different rate of voltage change across the capacitor. During the Integration Phase (refer to Figure 2), the rate of voltage change across C_{INT} has the opposite effect that it does during the Reset Phase. The result is that the conversion accuracy is unchanged by either drift or tolerance of C_{INT}. The net effect of a change in the integrator capacitor is simply to change the peak to peak amplitude of the sawtooth waveform at the output of the integrator.

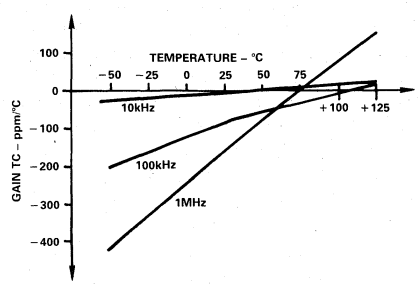


Figure 8. Gain TC vs. Temperature

The gain temperature coefficient of the AD650 is not a constant value. Rather the gain TC is a function of both the full scale frequency and the ambient temperature. At a low full scale frequency, the gain TC is determined primarily by the stability of the internal reference–a buried zener reference. This low speed gain TC can be quite good; at 10kHz full scale, the gain TC near 25°C is typically 0 ±50ppm/°C. Although the gain TC changes with ambient temperature (tending to be more positive

[1]"Noise Reduction Techniques in Electronic Systems", by H. W. OTT, (John Wiley, 1976).

at higher temperatures), the drift remains within a ±75ppm/°C window over the entire military temperature range. At full scale frequencies higher than 10kHz dynamic errors become much more important than the static drift of the dc reference. At a full scale frequency of 100kHz and above, these timing errors dominate the gain TC. For example, at 100kHz full scale frequency (R_{IN} = 40k and C_{OS} = 330pF) the gain TC near room temperature is typically −80 ±50ppm/°C, but at an ambient temperature near +125°C, the gain TC tends to be more positive and is typically +15 ±50ppm/°C. This information is presented in a graphical form in Figure 8. The gain TC always tends to become more positive at higher temperatures. Therefore it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100kHz full scale frequency. An average drift of −100ppm/°C means that as temperature is increased, the circuit will produce a lower frequency in reponse to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of −100ppm/°C. Now consider the 1MHz full scale frequency. It is not possible to achieve very much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately −20°C), a C_{OS} with a drift of −310ppm/°C is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of +75°C, the C_{OS} cap would change the gain TC from approximately 0ppm to +310ppm/°C.

The temperature effects of the components described above are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the end point method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and "zero". The nonlinearity will vary with the choice of one-shot capacitor and input resistor (see Figure 3). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated "bench-top" tester would prove useful. Such a system based on the Analog Devices' LTS-2010 is described in Reference 2.

The voltage-to-frequency transfer relation is shown in Figure 9 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the end points of the operating range (typically at 10mV and 10V) with a straight line. This straight line is then the ideal relationship which is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the end points – typically ten intermediate points will suffice. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full scale frequency and expressed either as parts per million of full-scale (ppm) or parts

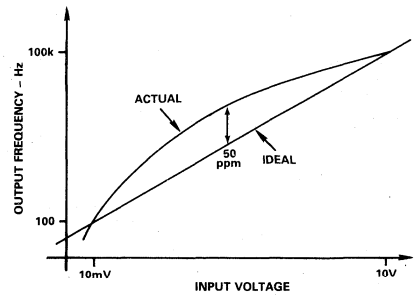


Figure 9a. Exaggerated Nonlinearity at 100kHz Full Scale

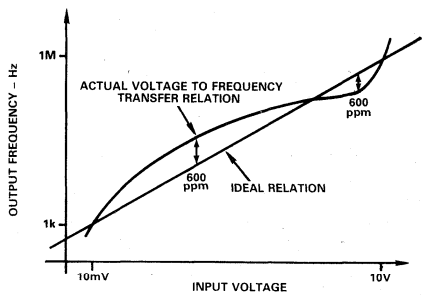


Figure 9b. Exaggerated Nonlinearity at 1MHz Full Scale

per hundred of full scale (%). For example, on a 100kHz full scale, if the maximum frequency error is 5Hz, the nonlinearity would be specified as 50ppm or 0.005%. Typically on the 100kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 9a). At higher full scale frequencies, (500kHz to 1MHz), the nonlinearity becomes "S" shaped and the maximum value may be either positive or negative. Typically, on the 1MHz scale (R_{IN} = 16.9k, C_{OS} = 51pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 9b.

PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply – ppm/%. For example, consider a VFC with a 10 volt input applied and an output frequency of exactly 100kHz when the power supply potential is ±15 volts. Changing the power supply to ±12.5 volts is a 5 volt change out of 30 volts, or 16.7%. If the output

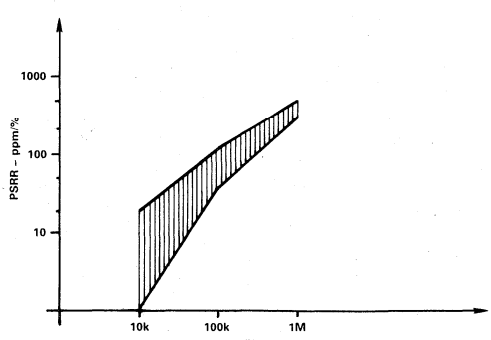


Figure 10. PSRR vs. Full Scale Frequency

[2]"V-F Converters Demand Accurate Linearity Testing", by L. DeVito, (Electronic Design, March 4, 1982)

frequency changes to 99.9kHz, the gain has changed 0.1% or 1000ppm. The PSRR is 1000ppm divided by 16.7% which equals 60ppm/%.

The PSRR of the AD650 is a function of the full scale operating frequency. At low full scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very good. At higher frequencies there are dynamic errors which become more important than the static reference signals, and consequently the PSRR is not quite as good. The values of PSRR are typically 0 ±20ppm/% at 10kHz full scale frequency (R_{IN} = 40k, C_{OS} = 3300pF). At 100kHz (R_{IN} = 40k, C_{OS} = 330pF) the PSRR is typically +80 ±40ppm/%, and at 1MHz (R_{IN} = 16.9kΩ, C_{OS} = 51pF) the PSRR is +350 ±50ppm/%. This information is summarized graphically in Figure 10.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 2 and 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently the voltage on the output (pin 1) must always be more positive than 2 volts below the inputs (pins 2 and 3). For example, in the F to V conversion mode, see Figure 6, the noninverting input of the op amp (pin 2) is grounded, which means that the output (pin 1) will not be able to go below −2 volts. Normal operation of the circuit as shown in the figure will never call for a negative voltage at the output; but one may imagine an arrangement calling for a bipolar output voltage (say ±10 volts) by connecting an extra resistor from pin 3 to a positive voltage. This will not work. A second major difference is that the output will only sink 1mA to the negative supply. There is no pulldown stage at the output other than the 1mA current source used for the V to F conversion. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 3 volts of the positive supply when it is not sourcing external current. When sourcing 10mA the output voltage may be driven to within 6 volts of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, pin 3, is bias current compensated and the noninverting input is not bias current compensated. The bias current at the inverting input is nominally zero, but may be as much as 20nA in either direction. The noninverting input typically has a bias current of 40nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20kΩ is connected to pins 13 and 14 and the wiper is connected to the positive supply through a 250kΩ resistor. A potential of about 0.6 volt is established across the 250kΩ resistor, and the 3μA current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and use a bipolar current either into or out of the null pin. The amount of current required will be very small – typically less than 3μA. This technique is shown in the applications section of this data sheet: the auto-zero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24kΩ resistor between pin 4 and the negative supply. The resultant current delivered to the op amp noninverting input is nominally 0.5mA and has a tolerance of ±10%. This current is then used to provide an offset voltage when pin 2 is tied to ground through a resistor. The 0.5mA which appears at pin 2 is also flowing through the 1.24kΩ resistor and this current may be measured by observing the voltage across the 1.24kΩ resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resultant offset voltage. It is possible to use other values of resistance between pin 4 and $-V_S$ to obtain a bipolar offset current different than 0.5mA. Figure 11 is a graph of the relationship between the bipolar offset current and the value of the resistor used to activate the source.

APPLICATIONS

DIFFERENTIAL VOLTAGE-TO-FREQUENCY CONVERSION

The circuit of Figure 12 accepts a true floating differential input signal. The common mode input, V_{CM}, may be in the range +15 to −5 volts with respect to analog ground. The signal input, V_{IN}, may be ±5 volts with respect to the common mode input. Both inputs are low impedance: the source which drives the common mode input must supply the 0.5mA drawn by the bipolar offset current source; and the source which drives the signal input must supply the integration current.

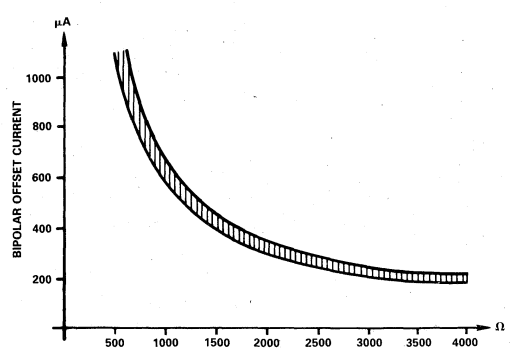


Figure 11. Bipolar Offset Current vs. External Resistor

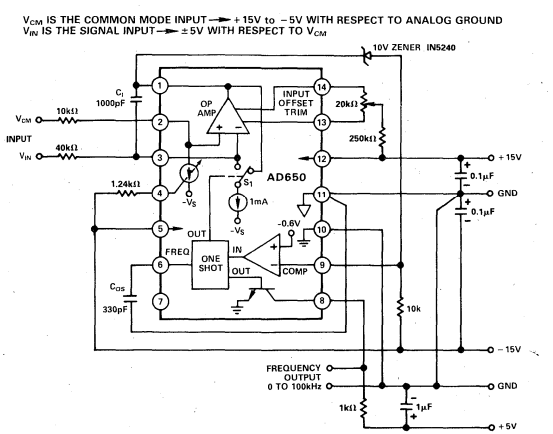


Figure 12. AD650 Differential Input

If less common mode voltage range is required, a lower voltage zener may be used. For example, if a 5 volt zener is used, the V_{CM} input may be in the range +10 to −5 volt. If the zener is not used at all, the common mode range will be ±5 volts with repect to analog ground. If no zener is used, the 10k pulldown resistor is not needed, and the integrator output (pin 1) is connected directly to the comparator input (pin 9).

AUTO ZERO CIRCUIT

In order to exploit the full dynamic range of the AD650 VFC, very small input voltages will need to be converted. For example, a six decade dynamic range based on a full scale of 10 volts will require accurate measurement of signals down to 10μV. In these situations a well-controlled input offset voltage is imperative. A constant offset voltage will not affect dynamic range, but simply shift all of the frequency readings by a few hertz. However, if the offset should change, then it will not be possible to distinguish between a small change in a small input voltage and a drift of the offset voltage. Hence, the useable dynamic range is less. The circuit shown in Figure 13 provides automatic adjustment of the op amp offset voltage. The circuit uses an AD582 sample and hold amplifier to control the offset, and the input voltage to the VFC is switched between ground and the signal to be measured via an AD7512DI analog switch. The offset of the AD650 is adjusted by injecting a current into or drawing a current out of pin 13. Note that only one of the offset null pins is used. During the "VFC Norm" mode, the SHA is in hold mode and the hold capacitor is very large, 0.1μF, to hold the AD650 offset constant for a long period of time.

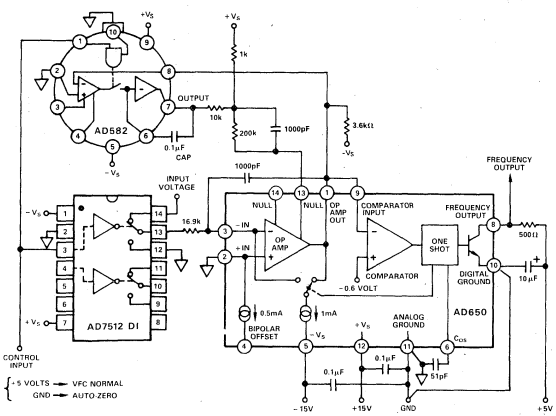


Figure 13. Auto-Zero Circuit for AD650 Voltage-to-Frequency Converter

When the circuit is in the "Auto Zero" mode the SHA is in sample mode and behaves like an op amp. The circuit is a variation of the classical two amplifier servo loop, where the output of the Device Under Test (DUT) – here the DUT is the AD650 op amp – is forced to ground by the feedback action of the control amplifier – the SHA. Since the input of the VFC circuit is connected to ground during the auto zero mode, the input current which can flow is determined by the offset voltage of the AD650 op amp. Since the output of the integrator stage is forced to ground it is known that the voltage is not changing (it is equal to ground potential). Hence if the output of the integrator is constant, its input current must be zero, so the offset voltage has been forced to be zero. Note that the output of the DUT could have been forced to any convenient voltage other than ground. All that is required is that the output voltage be known to be constant. Note also that the effect of the bias current at the inverting input of the AD650 op amp is also nulled in this circuit. The 1000pF capacitor shunting the 200kΩ resistor is compensation for the two amplifier servo loop. Two integrators in a loop requires a single zero for compensation. Note that the 3.6kΩ resistor from pin 1 of the AD650 to the negative supply is *not* part of the auto-zero circuit, but rather it is required for VFC operation at 1MHz.

PHASE LOCKED LOOP F/V CONVERSION

Although the F/V conversion technique shown in Figure 6 is quite accurate and uses only a few extra components, it is very limited in terms of signal frequency response and carrier feedthrough. If the carrier (or input) frequency changes instantaneously, the output cannot change very rapidly due to the integrator time constant formed by C_{INT} and R_{IN}. While it is possible to decrease the integrator time constant to provide faster settling of the F to V output voltage, the carrier feedthrough will then be larger. For signal frequency response in excess of 2kHz, a phase locked F/V conversion technique such as the one shown in Figure 14 is recommended.

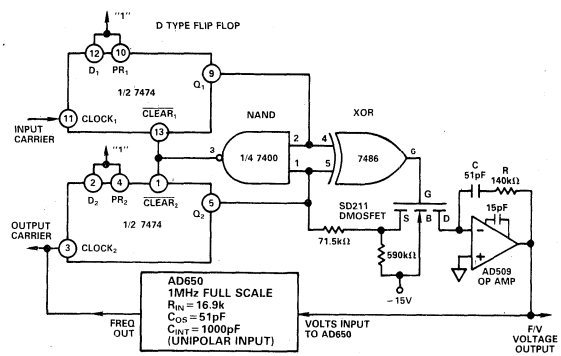


Figure 14. Phase Locked Loop F/V Conversion

In a phase locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable "divide by N" before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to "N times" the reference frequency, and it is this frequency output which is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 14 uses a digital phase detector which also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFD's) are available in integrated form. For a full discussion of phase lock loop circuits see Reference 3.

An analysis of this circuit must begin at the 7474 dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops will rise at exactly the same time. With two zero's, then two one's on the

[3]Phase Lock Techniques", by F.M. Gardner, 2nd Edition, 1979, John Wiley and Sons.

inputs of the exclusive or (XOR) gate, the output will remain low keeping the DMOS FET switched off. Also, the NAND gate will go low resetting the flip-flops to zero. Throughout the entire cycle just described, the DMOS integrator gate remained off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate will be turned on for the small time span that the two signals are mismatched. Since Q_2 will be low during the mismatch time, a negative current will be fed into the integrator, causing its output voltage to rise. This in turn will increase the frequency of the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator will be forced down slightly to synchronize the two signals.

Using a mathematical approach, the $\pm 25\mu A$ pulses from the phase detector are incorporated into the phase detector gain, K_d.

$$K_d = \frac{25\mu A}{2\pi} = 4 \times 10^{-6} \quad amperes/radian \tag{9}$$

Also, the V/F converter is configured to produce 1MHz in response to a 10 volt input, so its gain K_o is:

$$K_o = \frac{2\pi \times 1 \times 10^6 Hz}{10V} = 6.3 \times 10^5 \quad \frac{radians}{volt \cdot sec} \tag{10}$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency ω_n:

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \tag{11}$$

and damping factor

$$\zeta = \frac{R\sqrt{C\,K_o K_d}}{2} \tag{12}$$

For the values shown in Figure 14, these relations simplify to a natural frequency of 35kHz with a damping factor of 0.8.

For those desiring a simple approach to determining component values for other PLL frequencies and VFC full scale voltage, the following cookbook steps can be used:

1. Determine K_o (in units of radians per volt second) from the maximum input carrier frequency F_{max} (in hertz) and the maximum output voltage V_{max}.

$$K_o = \frac{2\pi \times F_{max}}{V_{max}} \tag{13}$$

2. Calculate a value for C based upon the desired loop bandwidth, f_n. Note that this is the desired frequency range of the output signal. The loop bandwidth (f_n) is *not* the maximum carrier frequency (f_{max}): the signal may be very narrow even though it is transmitted over a 1MHz carrier.

$$C = \frac{K_o}{f_n^2} \cdot 1 \times 10^{-7} \frac{V \cdot F}{Rad \cdot sec} \qquad \begin{matrix} C \text{ units FARADS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{14}$$

3. Calculate R to yield a damping factor of approximately 0.8 using this equation:

$$R = \frac{f_n}{K_o} \cdot 2.5 \times 10^6 \frac{Rad \cdot \Omega}{V} \qquad \begin{matrix} R \text{ units OHMS} \\ f_n \text{ units HERTZ} \\ K_o \text{ units RAD/VOLT•SEC} \end{matrix} \tag{15}$$

If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor may be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

PLL PERFORMANCE

The performance of the PLL circuit is demonstrated by the system shown in Figure 15; an analog signal is converted into a frequency, and then this frequency is converted back into an analog voltage by the PLL.

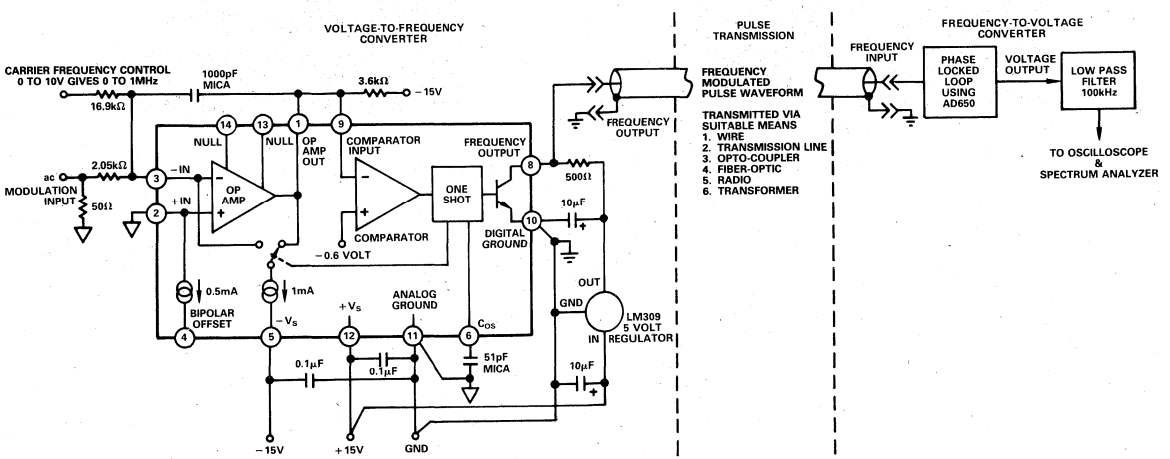


Figure 15.

The source of the frequency input signal used to drive the PLL is an AD650 with two separate inputs: one for dc to set the carrier frequency, and one for ac to establish a modulation. Note how the summing junction input to the AD650 allows such flexibility. The output frequency is then relayed to the PLL via a jumper cable. The signal at this point is a 5 volt digital pulse train and as such may be transmitted in any fashion suitable to the application at hand. For example, galvanic isolation is achieved with a simple transformer or opto-isolator; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The actual method of conveying the pulses is not crucial to the system performance. The PLL is the circuit shown in Figure 14, and the filter shown on the output signal is simply to attenuate carrier feedthrough to allow easy interpretation of the signal with an oscilloscope and spectrum analyzer.

The step response of the system is shown in Figure 16a. The signal output is swinging between 5 volts and 10 volts, for an input step of 500kHz to 1MHz. Note that the AD650 is actually overshooting to 1.1MHz and the response remains well controlled. Note the slight irregularity during the transition: this is caused by cycleslipping during the slew where feedback is lost temporarily and the PLL actually loses phase lock. The frequency response of the system when driven with sinewave excitation is shown in Figure 16b. Here the output level is set to 2 volts peak to peak, and the carrier is 800kHz. Note that the -3dB bandwidth is about 70kHz, which is consistent with a damping factor of 0.8 and a natural frequency of 35kHz[4]. When an unmodulated carrier is applied to the PLL, the noise that appears at the output determines the dynamic range of the system. The spectrum of the noise at the output of the PLL is shown in Figure 16c. By comparing this with Figure 16b, the dynamic range of the system is seen to be 80dB. The harmonic distortion of the system is shown in Figure 16d. The output is a 2V p-p sinewave at 5kHz, and the amplitude of the first harmonic is seen to be 48dB below the fundamental. The harmonic distortion can be improved to the level of 60dB by reducing the amplitude of the modulation, but this is at the expense of dynamic range since the intensity of the noise floor remains constant.

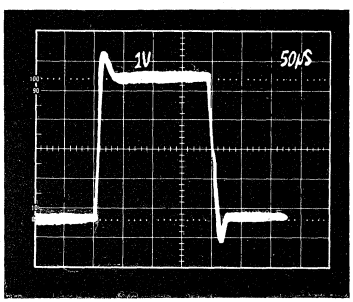


Figure 16a. Step Response

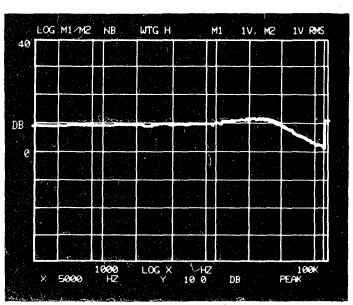


Figure 16b. Frequency Response

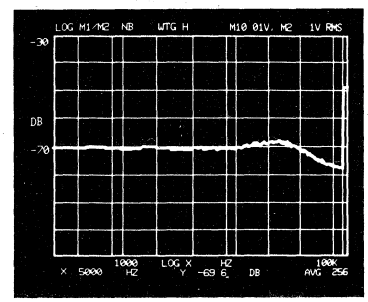


Figure 16c. Noise Output from PLL

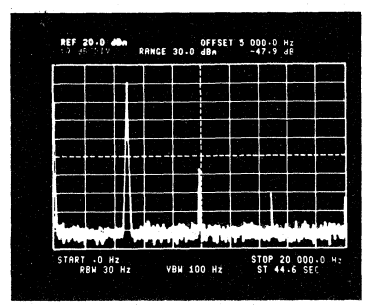


Figure 16d. Harmonic Distortion of PLL System

[4]See page 13 of reference 3.

Voltage-to-Frequency and Frequency-to-Voltage Converter

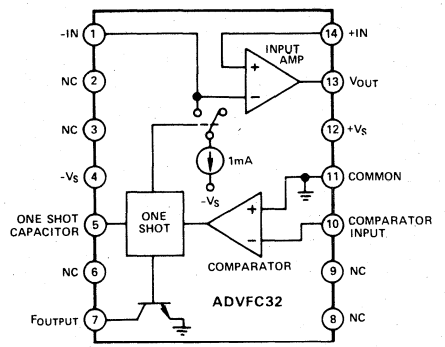
ADVFC32

FEATURES

High Linearity
- **±0.01% max at 10kHz FS**
- **±0.05% max at 100kHz FS**
- **±0.2% max at 500kHz FS**

Output TTL/CMOS Compatible
V/F or F/V Conversion
6 Decade Dynamic Range
Voltage or Current Input
Reliable Monolithic Construction

ADVFC32 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The industry standard ADVFC32 is a low cost monolithic voltage-to-frequency (V/F) converter or frequency-to-voltage (F/V) converter with good linearity (0.01% max error at 10kHz) and operating frequency up to 0.5MHz. In the V/F configuration, positive or negative input voltages or currents can be converted to a proportional frequency using only a few external components. For F/V conversion, the same components are used with a simple biasing network to accommodate a wide range of input logic levels.

TTL or CMOS compatibility is achieved in the V/F operating mode using an open collector frequency output. The pullup resistor can be connected to voltages up to 30 volts, or to +15V or +5V for conventional CMOS or TTL logic levels. This resistor should be chosen to limit current through the open collector output to 8mA. A larger resistance can be used if driving a high impedance load.

Input offset drift is only 3ppm of full scale per °C, and full scale calibration drift is held to a maximum of 100ppm/°C (ADVFC32BH) due to a low T.C. zener diode.

The ADVFC32 is available in commercial, industrial, and extended temperature grades. The commercial grade is packaged in a 14-pin plastic DIP while the two wider temperature range parts are packaged in hermetically sealed TO-100 cans.

PRODUCT HIGHLIGHTS

1. The ADVFC32 uses a charge balancing circuit technique (see Functional Block Diagram) which is well suited to high accuracy voltage-to-frequency conversion. The full-scale operating frequency is determined by only one precision resistor and capacitor. The tolerance of other support components (including the integration capacitor) is not critical. Inexpensive ±20% resistors and capacitors can be used without affecting linearity or temperature drift.
2. The ADVFC32 is easily configured to satisfy a wide range of system requirements. Input voltage scaling is set by selecting the input resistor which sets the input current to 0.25mA at the maximum input voltage.
3. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the ADVFC32.
4. The ADVFC32 is intended as a pin-for-pin replacement for VFC32 devices from other manufacturers.

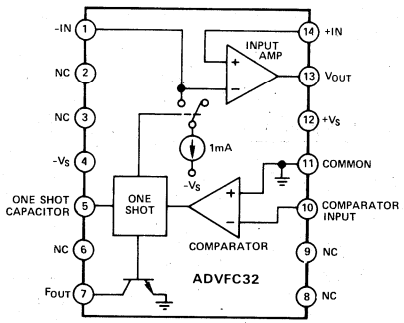
SPECIFICATIONS (typical @ +25°C with V_S = ±15V, unless otherwise noted)

Model	ADVFC32KN	ADVFC32BH	ADVFC32SH
DYNAMIC PERFORMANCE			
Full Scale Frequency Range	0 to 500kHz	*	*
Nonlinearity[1]			
f_{max} = 10kHz	±0.01% max	*	*
f_{max} = 100kHz	±0.05% max	*	*
f_{max} = 0.5MHz	±0.2% max, ±0.05% typ	*	*
Full Scale Calibration Error (adjustable to zero)	±5%	*	*
vs. Supply (Full Scale Frequency = 100kHz)	±0.015% of FSR/%max	*	*
vs. Temperature (Full Scale Frequency = 10kHz)	±75ppm/°C	±100ppm/°C max	±150ppm/°C
DYNAMIC RESPONSE			
Max Settling Time for Full Scale Step Input	1 Pulse of New Frequency Plus 1µs	*	*
Overload Recovery Time	1 Pulse of New Frequency Plus 1µs	*	*
ANALOG INPUT AMPLIFIER (V/F Conversion)			
Current Input Range	0 to +0.25mA	*	*
Voltage Input Range	0 to -10V[2], 0 to 0.25mA × R_{IN}[3]	*	*
Differential Impedance	2MΩ‖10pF (300kΩ‖10pF min)		
Common Mode Impedance	750MΩ‖3pF (300MΩ‖3pF min)		
Input Bias Current			
Noninverting Input	40nA (250nA max)	*	*
Inverting Input	±8nA (±100nA max)	*	*
Input Offset Voltage (trimmable to zero)[2,3]	4mV max	*	*
vs. Temperature (T_{min} to T_{max})	30µV/°C	*	*
Safe Input Voltage	±V_S	*	*
COMPARATOR (F/V Conversion)			
Logic "0" Level	-V_S to -0.6V	*	*
Logic "1" Level	+1V to +V_S	*	*
Pulse Width Range	0.1µs to (0.15/f_{max})	*	*
Input Impedance	250kΩ (50kΩ‖10pF min)	*	*
OPEN COLLECTOR OUTPUT (V/F Conversion)			
Output Voltage, Logic "0" I_{SINK} = 8mA	0.4V max	*	*
Output Leakage Current in Logic "1"	1µA max	*	*
Voltage Range	0 to +30V	*	*
Fall Times (Load = 500pF and I_{SINK} = 5mA)	400ns max	*	*
AMPLIFIER OUTPUT (F/V Conversion)			
Voltage Range (0mA≤I_O≤7mA)	0 to +10V	*	*
Source Current (0≤V_O≤7V)	+10mA min	*	*
Capacitive Load (without oscillation)	100pF max	*	*
Closed Loop Output Impedance	1Ω max	*	*
POWER SUPPLY			
Rated Voltage	±15V	*	*
Voltage Range	±9V to ±18V	*	*
Quiescent Current	6mA typ, 8mA max	*	*
TEMPERATURE RANGE			
Specified Range	0 to +70°C	-25°C to +85°C	-55°C to +125°C
Operating Range	-25°C to +85°C	-55°C to +125°C	-55°C to +125°C
Storage	-25°C to +85°C	-65°C to +150°C	-65°C to +150°C
PACKAGE OPTIONS[4]			
Plastic DIP – N14A	ADVFC32KN	N/A	N/A
TO-100	N/A	ADVFC32BH	ADVFC32SH

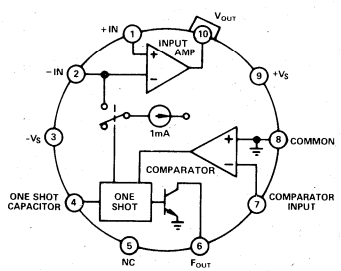
NOTES
[1] Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.
[2] See Figure 3.
[3] See Figure 1.
[4] See Section 19 for package outline information.
*Specifications same as ADVFC32KN.
Specifications subject to change without notice.

PIN CONFIGURATION
(TOP VIEWS)

"N" PACKAGE



"H" PACKAGE – TO-100



UNIPOLAR V/F, POSITIVE INPUT VOLTAGE

When operated as a V/F converter, the transformation from voltage to frequency is based on a comparison of input signal magnitude to the 1mA internal current source.

A more complete understanding of the ADVFC32 requires a close examination of the internal circuitry of this part. Consider the operation of the ADVFC32 when connected as shown in Figure 1. At the start of a cycle, a current proportional to the input voltage flows through R3 and R1 to charge integration capacitor C2. As charge builds up on C2, the output voltage of the input amplifier decreases. When the amplifier output voltage (pin 13) crosses ground (see Figure 2 at time t_1), the comparator triggers a one shot whose time period is determined by capacitor C1. Specifically, the one shot time period (in nanoseconds) is:

$$t_{OS} \cong (C_1 + 44pF) \times 6.7k\Omega$$

During this period, a current of $(1mA - I_{IN})$ flows out of the integration capacitor. The total amount of charge depleted during one cycle is, therefore $(1mA - I_{IN}) \times t_{OS}$. This charge is replaced during the remainder of the cycle to return the integrator to its original voltage. Since the charge taken out of C2 is equal to the charge that is put on C2 every cycle,

$$(1mA - I_{IN}) \times t_{OS} = I_{IN} \times \left(\frac{1}{F_{OUT}} - t_{OS} \right)$$

or, rearranging terms,

$$F_{OUT} = \frac{I_{IN}}{1mA \times t_{OS}}$$

The complete transfer equation can now be derived by substituting $I_{IN} = V_{IN}/R_{IN}$ and the equation relating C1 and t_{OS}. The final equation describing ADVFC32 operation is:

$$F_{OUT} = \frac{V_{IN}/R_{IN}}{1mA \times (C_1 + 44pF) \times 6.7k\Omega}$$

Components should be selected to optimize performance over the desired input voltage and output frequency range using the equations listed below:

$$C_1 = \frac{3.7 \times 10^7 pF/sec}{F_{OUT\ FS}} - 44pF$$

$$C_2 = \frac{10^{-4}\ Farads/sec}{F_{OUT\ FS}} \text{ (1000pF minimum)}$$

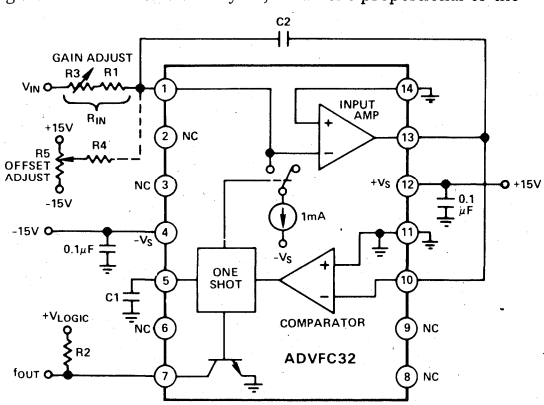


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

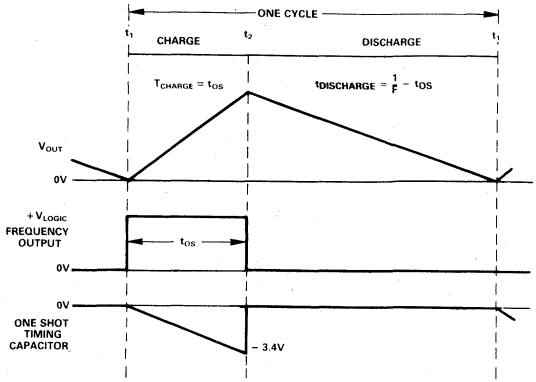


Figure 2. Voltage-to-Frequency Conversion Waveforms

$$R_{IN} = \frac{V_{IN\ FS}}{0.25mA}$$

$$R_2 \geq \frac{+V_{LOGIC}}{8mA}$$

Both R_{IN} and C_1 should have very low temperature coefficients as changes in their values will result in a proportionate change in the V/F transfer function. Other component values and temperature coefficients are not critical.

$V_{IN\ FS}$	$F_{OUT\ FS}$	C_1	R_{IN}	C_2
1V	10kHz	3650pF	4.0kΩ	0.01μF
10V	10kHz	3650pF	40kΩ	0.01μF
1V	100kHz	330pF	4.0kΩ	1000pF
10V	100kHz	330pF	40kΩ	1000pF

Table I. Suggested Values for C_1, R_{IN} and C_2

Input resistance R_{IN} is composed of a fixed resistor (R1) and a variable resistor (R3) to allow for initial gain error compensation. To cover all possible situations, R3 should be 20% of R_{IN}, and R1 should be 90% of R_{IN}. This allows a ±10% gain adjustment to compensate for the ADVFC32 full-scale error and the tolerance of C1.

If more accurate initial offset is required, the circuit of R4 and R5 can be added. R5 can have a value between 10kΩ and 100kΩ, and R4 should be approximately 10MΩ. The amount of current required to trim zero offset will be relatively small, so the temperature coefficients of these resistors are not critical. If large offsets are added using this circuit, temperature drift of both of these resistors is much more important.

BIPOLAR V/F

By adding another resistor from pin 1 (pin 2 of TO-100 can) to a stable positive voltage, the ADVFC32 can be operated with a bipolar input voltage. For example, an 80kΩ resistor to +10V causes an additional current of 0.125mA to flow into the integrator so that the net current flow to the integrator is positive even for negative input voltages. At negative full scale input voltage, 0.125mA will flow into the integrator from V_{IN} cancelling out the 0.125mA from the offset resistor, resulting in an output frequency of zero. At positive full scale, the sum of the two currents will be 0.25mA and the output will be at its maximum frequency.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 3 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full scale output frequency occurs at negative full scale input, and zero output frequency corresponds to zero input voltage.

A very high impedance signal source may be used since it only drive the noninverting integrator input. Typical input impedance at this terminal is 250MΩ or higher. For V/F conversion of positive input signals the signal generator must be able to source 0.25mA to properly drive the ADVFC32, but for negative V/F conversion the 0.25mA integration current is drawn from ground through R1 and R3.

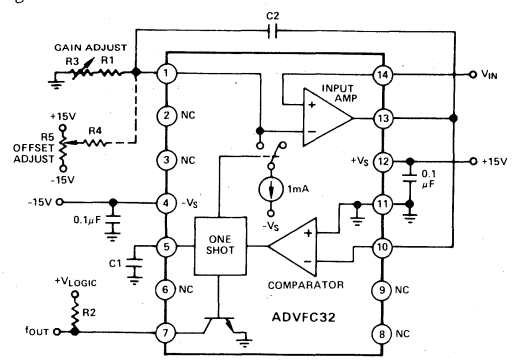


Figure 3. Connection Diagram for V/F Conversion, Negative Input Voltage

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in the previous section. For best operating results use component equations listed in that section.

F/V CONVERSION

Although the mathematics of F/V conversion can be very complex, the basic principle is easy to understand. Figure 4 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1mA into the integrator input for a measured time period (determined by C1). As the frequency increases, the amount of charge injected into the integration capacitor increases proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F conversion section.

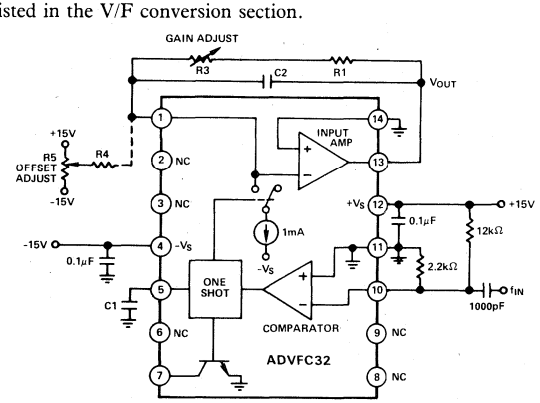


Figure 4. Connection Diagram for F/V Conversion, TTL Input

DECOUPLING

Decoupling power supplies at the device is good practice in any system, but absolutely imperative in high resolution applications. For the ADVFC32, it is important to remember where the voltage transients and ground currents flow. For example, the current drawn through the output pulldown transistor originates from the logic supply, and is directed to ground through pin 11 (pin 8 of TO-100). Therefore, the logic supply should be decoupled near the ADVFC32 to provide a low impedance return path for switching transients. Also, if there is a separate digital ground it should be connected to the analog ground at the ADVFC32. This will prevent ground offsets that could be created by directing the full 8mA output current into the analog ground, and subsequently back to the logic supply.

Although some circuits may operate satisfactorily with the power supplies decoupled at only one location on each board, this practice is not recommended for the ADVFC32. For best results, each supply should be decoupled with 0.1μF capacitor at the ADVFC32. In addition, a larger board level decoupling capacitor of 1μF to 10μF should be located relatively close to the ADVFC32 on each power supply.

COMPONENT TEMPERATURE COEFFICIENTS

The drift specifications of the ADVFC32 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_1 directly affect the overall temperature stability. In the application of Figure 2, a 10ppm/°C input resistor used with a 100ppm/°C capacitor may result in a maximum overall circuit gain drift of:

100ppm/°C (ADVFC32BH) + 100ppm/°C (C1)
+ 10ppm/°C (R_{IN}) = 210ppm/°C

Although R_{IN} and C_1 have the most pronounced effect on temperature stability, the offset circuit of resistors R4 and R5 may also have a slight effect on the offset temperature drift of the circuit. The offset will change with variations in the resistance of R4 and supply voltage changes. In most applications the offset adjustment is very small, and the offset drift attributable to this circuit will be negligible. In the bipolar mode, however, both the positive reference and the resistor used to offset the signal range will have a pronounced effect on offset drift. A high quality reference and resistor should be used to minimize offset drift errors.

Other circuit components do not directly influence temperature performance as long as their actual values are not so different from nominal value as to preclude operation. This includes integration capacitor C2. A change in the capacitance value of C2 results in a different rate of voltage change across C2, but this is compensated by an equal effect when C2 is discharged by the switched 1mA current source so that no net effect occurs.

The temperature effects of the components described above are the same when the ADVFC32 is configured for negative or bipolar input ranges, or F/V conversion.

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to pins 1, 13, and 14 is not a standard operational amplifier. Although it operates like an op amp in most applications, two key differences should be noted. First, the bias current of the positive input is typically 40nA while the bias current of the inverting input is ±8nA. Therefore, any attempt to cancel input offset voltage due to bias currents by matching input resistors will create worse offsets. Second, the output of this amplifier will sink only 1mA, even though it will source as much as 10mA. When used in the F/V mode, the amplifier must be buffered if large sink currents are required.

MICROPROCESSOR OPERATED A/D CONVERTER

With the addition of a few external components the ADVFC32 can be used as a ±10V A/D microprocessor front end. Although the nonlinearity of the ADVFC32 is only 0.05% maximum (0.01% typ), the resolution is much higher, allowing it to be used in 16-bit measurement and control systems where a monotonic transfer function is essential. The resolution of the circuit shown in Figure 5 is dependent on the amount of time allowed to count the ADVFC32 frequency output. Using a full scale frequency of 100kHz, an 8-bit conversion can be made in about 10ms, and a 2 second time period allows a 16-bit measurement, including offset and gain calibration cycles.

As shown in Figure 5, the input signal is selected via the AD7590 input multiplexer. Positive and negative references as well as a

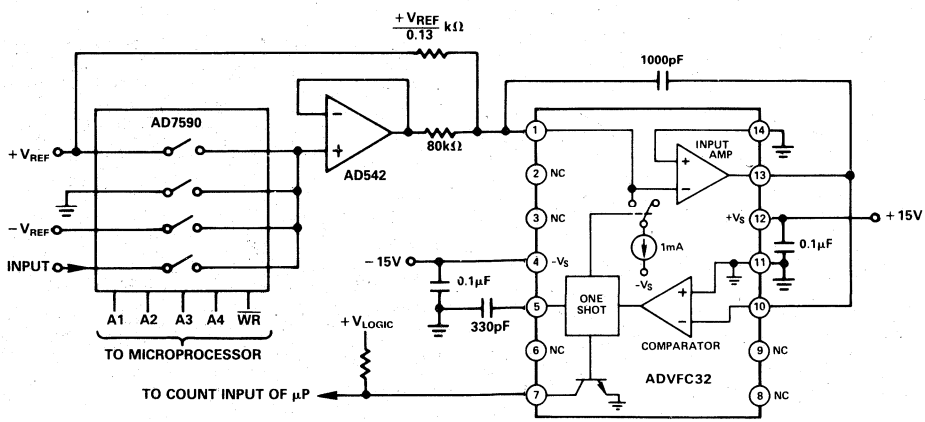


Figure 5. High Resolution, Self-Calibrating, Microprocessor Operated A/D Converter

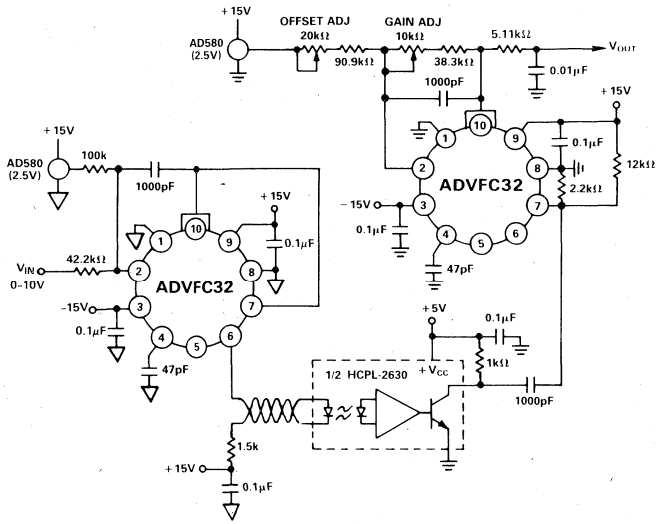


Figure 6. High Noise Immunity Data Link

ground input are provided to calibrate the A/D. This is very important in systems subject to moderate or extreme temperature changes since the gain temperature coefficient of the ADVFC32 is as high as ±150ppm/°C. By using the calibration cycles, the A/D conversion will be as accurate as the references provided. The AD542 following the input multiplexer provides a high impedance input (10^{12} ohms) and buffers the switch resistance from the relatively low impedance ADVFC32 input.

If higher linearity is required, the ADVFC32 can be operated at 10kHz, but this will require a proportionately longer conversion time. Conversely, the conversion time can be decreased at the expense of nonlinearity by increasing the maximum frequency to as high as 500kHz.

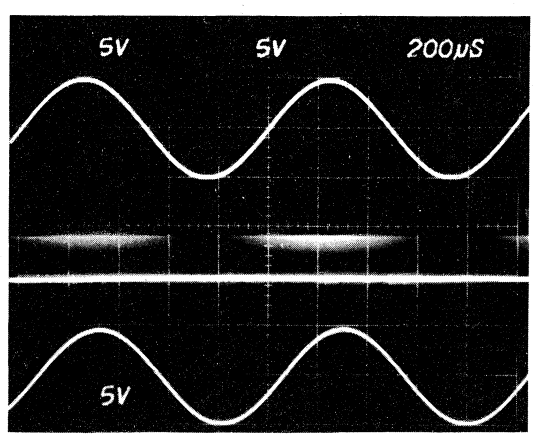
HIGH NOISE IMMUNITY, HIGH CMRR ANALOG DATA LINK

In many applications, a signal must be sensed at a remote site and sent through a very noisy environment to a central location for further processing. In these cases, even a shielded cable may not protect the signal from noise pickup. The circuit of Figure 6 provides a solution in these cases. Due to the optocoupler and voltage-to-frequency conversion, this data link is extremely insensitive to noise and common mode voltage interference. For even more protection, an optical fiber link substituted for the HCPL2630 will provide common mode rejection of more than several hundred kilovolts and virtually total immunity to electrical noise. For most applications, however, the frequency modulated signal has sufficient noise immunity without using an optical fiber link, and the optocoupler provides common mode isolation up to 3000V dc.

The data link input voltage is changed in a frequency modulated signal by the first ADVFC32. A 42.2kΩ input resistor and a 100kΩ offset resistor set the scaling so that a 0V input signal corresponds to 50kHz, and a 10V input results in the maximum output frequency of 500kHz. A high frequency optocoupler is then used to transmit the signal across any common mode voltage potentials to the receiving ADVFC32. The optocoupler is not necessary in systems where common mode noise is either very small or a constant low level dc voltage. In systems where common mode voltage may present a problem, the connection between the two locations should be through the optocoupler; no power or ground connections need to be made.

The output of the optocoupler drives an ADVFC32 hooked up in the F/V configuration. Since the reconstructed signal at pin 10 has a considerable amount of carrier feedthrough, it is desirable to filter out any frequencies in the carrier range of 50kHz to 500kHz. The frequency response of the F/V converter is only 3kHz due to the pole made by the integrator, so a second 3kHz filter will not significantly limit the bandwidth. With the simple one pole filter shown in Figure 6, the input to output 3dB point is approximately 2kHz, and the output noise is less than 15mV. If a lower output impedance drive is needed, a two pole active filter is recommended as an output stage.

Although the F/V conversion technique used in this circuit is quite simple, it is also very limited in terms of its frequency response and output ripple. The frequency response is limited by the integrator time constant and while it is possible to decrease that time constant, either signal range or output ripple must be sacrificed. The performance of the circuit of Figure 6 is shown in the photograph below. The top trace is the input signal, the middle trace is the frequency-modulated signal at the optocoupler's output, and the bottom trace is the recovered signal at the output of the F/V converter.



Digital Signal Processing Components

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•New product since publication of *1982-1983 Databook Update*

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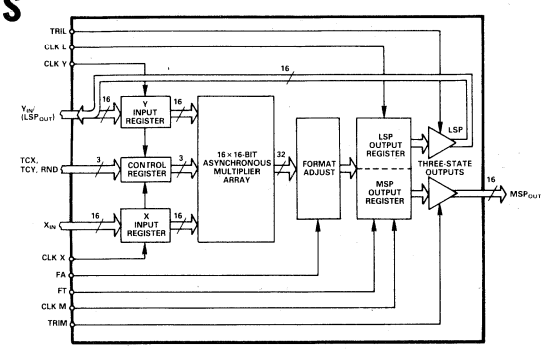
CMOS Multipliers



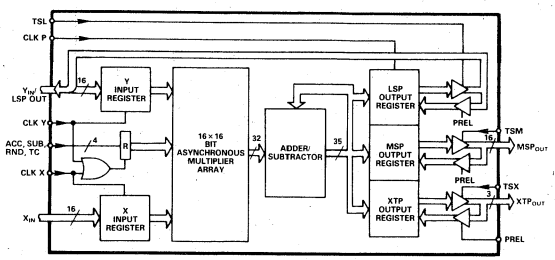
ADSP-1016 Functional Block Diagram

SPECIFICATIONS (max over power supply and temperature range unless otherwise noted).

Model	Bit Size	Multiply, Time (ns) +25°C/Over T_{amb}	Power Dissipation	Package	Temp. Range[1]	Notes	Page
ADSP-1080JD	8×8	100/115	75mW	40-Pin DIP	C	Two's Complement	12–51
ADSP-1080KD	8×8	85/100	75mW	40-Pin DIP	C	Two's Complement	12–51
ADSP-1080SD	8×8	100/130	100mW	40-Pin DIP	E	Two's Complement	12–51
ADSP-1080TD	8×8	85/115	100mW	40-Pin DIP	E	Two's Complement	12–51
ADSP-1081JD	8×8	90/105	75mW	40-Pin DIP	C	Unsigned Magnitude	12–57
ADSP-1081KD	8×8	75/90	75mW	40-Pin DIP	C	Unsigned Magnitude	12–57
ADSP-1081SD	8×8	90/120	100mW	40-Pin DIP	E	Unsigned Magnitude	12–57
ADSP-1081TD	8×8	75/105	100mW	40-Pin DIP	E	Unsigned Magnitude	12–57
ADSP-1012JD[2]	12×12	140/165	125mW	64-Pin DIP	C	Two's Complement	12–27
ADSP-1012KD	12×12	110/130	125mW	64-Pin DIP	C	Two's Complement	12–27
ADSP-1012SD	12×12	140/195	150mW	64-Pin DIP	E	Two's Complement	12–27
ADSP-1012TD	12×12	110/150	150mW	64-Pin DIP	E	Two's Complement	12–27
ADSP-1016JD[2]	16×16	180/220	125mW	64-Pin DIP	C	Two's Complement	12–35
ADSP-1016KD	16×16	145/170	125mW	64-Pin DIP	C	Two's Complement	12–35
ADSP-1016SD	16×16	180/250	150mW	64-Pin DIP	E	Two's Complement	12–35
ADSP-1016TD	16×16	145/200	150mW	64-Pin DIP	E	Two's Complement	12–35
ADSP-1024JG	24×24	235/275	125mW	84-Pin Grid	C	Two's Complement	12–43
ADSP-1024KG	24×24	200/235	125mW	84-Pin Grid	C	Two's Complement	12–43
ADSP-1024SG	24×24	235/325	150mW	84-Pin Grid	E	Two's Complement	12–43
ADSP-1024TG	24×24	200/275	150mW	84-Pin Grid	E	Two's Complement	12–43

NOTES
[1]C = Commercial 0 to +70°C; E = Extended −55°C to +125°C.
[2]ADSP-1012 and ADSP-1016 are also available in 68-Terminal Ceramic Leadless Chip Carrier and 68-Terminal Pin Grid Package.
Shading indicates new product since publication of *1982–1983 Databook Update*.

CMOS Multiplier/Accumulators



ADSP1010 Functional Block Diagram

SPECIFICATIONS (max over power supply and temperature range unless otherwise noted).

Model	Bit Size	Multiply Accumulate Time (ns) +25°C/Over T_{amb}	Power Dissipation	Package	Temp. Range[1]	Page
ADSP-1008JD	8×8	135/160	75mW	48-Pin DIP	C	12–7
ADSP-1008KD	8×8	105/125	75mW	48-Pin DIP	C	12–7
ADSP-1008SD	8×8	135/185	100mW	48-Pin DIP	E	12–7
ADSP-1008TD	8×8	105/145	100mW	48-Pin DIP	E	12–7
ADSP-1009JD[2]	12×12	165/195	125mW	64-Pin DIP	C	12–13
ADSP-1009KD	12×12	130/155	125mW	64-Pin DIP	C	12–13
ADSP-1009SD	12×12	165/225	150mW	64-Pin DIP	E	12–13
ADSP-1009TD	12×12	130/180	150mW	64-Pin DIP	E	12–13
ADSP-1010JD[2]	16×16	200/240	125mW	64-Pin DIP	C	12–19
ADSP-1010KD	16×16	165/190	125mW	64-Pin DIP	C	12–19
ADSP-1010SD	16×16	180/250	150mW	64-Pin DIP	E	12–19
ADSP-1010TD	16×16	165/220	150mW	64-Pin DIP	E	12–19
ADSP1110JD	16×16	200/240	125mW	28-Pin DIP	C	12–65
ADSP1110KD	16×16	165/190	125mW	28-Pin DIP	C	12–65
ADSP1110SD	16×16	180/250	150mW	28-Pin DIP	E	12–65
ADSP1110TD	16×16	165/220	150mW	28-Pin DIP	E	12–65

NOTES
[1]C = Commercial 0 to +70°C; E = Extended −55°C to +125°C
[2]ADSP-1009 and ADSP-1010 are also available in 68-Terminal Ceramic Leadless Chip Carrier and 68-Terminal Pin Grid Package.
Shading indicates new product since publication of *1982–1983 Databook Update*.

Orientation
Digital Signal Processing Components

WHAT IS DSP?

Digital signal processing is not new. In its most general form, the term describes all of the operations that are done by and with digital logic circuitry and computers to condition or extract meaning from signals acquired in the real world. However, most computers process information sequentially, and they have difficulty performing timely and error-free number-crunching of large arrays of fast-changing data.

DSP, an analogy to analog signal processing, consists of specialized techniques using high-performance circuits and programs that enable signals to be processed numerically at high speeds, often approaching real time i.e., "analog speeds and digital accuracy."

Three of these techniques—filtering, correlation, and fast Fourier transformations (FFT)—comprise sixty or seventy percent of all current DSP practice. Another twenty percent involve matrix operations (multiplication or addition of two matrices) typically required for graphics and control.

FILTERING, CORRELATION AND FFT

Digital filters are used for exactly the same purposes as analog filters; to pass signals in certain frequency bands and to attenuate signals in other frequency bands. Modern digital filtering is carried out by performing the successive multiplications and additions required to perform convolution in the time domain—corresponding to multiplication in the frequency domain.

To understand how a digital filter works, remember that, in the frequency domain, the spectrum of the input signal is multiplied by the frequency response function of the filter circuit to produce an output signal having a predetermined set of frequency components. You may recall that this multiplication in the frequency domain is equivalent to the convolution of two signals in the time domain, i.e., integration of the product of the folded input time function, $f(\tau\text{-}t)$, and an indicial response function, $g(t)$, with respect to time, to give a response which is a function of τ. An analog filter circuit automatically performs the convolution implied by its physical circuit architecture and coefficients to provide the (real) time-domain response, but manually computed response predictions are easier to perform in the frequency domain, using the classical continuous calculus.

Digital signal processing, however, makes it possible to perform large numbers of accurate incremental calculations in a short time. In digital signal processing, difference calculus replaces differential calculus, and time-response of the filter can be calculated directly by convolution. The input signal is already available in the form of a sampled time function in suitable increments (for all values of τ), the indicial response function for each time increment can be computed initially and stored in memory, and integration is replaced by summation.

A typical digital filtering process is illustrated by (1):

$$Y(n) = \sum_{m=0}^{n-1} H(m)\, X(n-m) \qquad (1)$$

Each output sample, Y(n), is obtained by multiplying m input samples, X(n – m), by m coefficients, H(m), and summing the results.

The filter coefficients, H(m), are weighted in the time domain so that, when transformed to the frequency domain, they describe the desired filter response. An ideal brick-wall low-pass filter, for example, is a square-wave in the frequency domain; thus the time-domain representation of its amplitude would be a (sin x)/x function of infinite duration. The H(m) would then be weighted according to a realizable approximation to that function. The convolving of the X(n-m) with the H(m) through equation 1 has the effect of multiplying the spectrum of the X(n-m) with that of the H(m). Since the frequency spectrum of the H(m) approximates the desired filter response, the Y(n) represent the correct values of time response appropriate to the filter characteristic and input waveshape.

Correlation is used to compare two signals, one of which is translated in time by a range of time delays. Auto-correlation compares a signal with delayed versions of the same signal; cross-correlation compares two different signals over a range of delay times. An algorithm for the digital implementation is

$$R(N) = \sum_{m=0}^{n-1} X(m)\, Y(m+N) \quad 0 < N \leq n-1 \qquad (2)$$

The degree to which X(m), the values of X at different times, m, are the same as the values of Y, Y(m+N), for a given delay time, N, determines the magnitude of R(N)—and thus the correlation between the two signals at time N– and provides a *correlation function* over all N, in the range 0 to n–1.

As in the case of filtering, the algorithm employs a large number of successive multiplications and additions and is thus well suited for computation by DSP.

The *Discrete Fourier Transform*, very similar to the function performed by the more-efficient fast Fourier transform (FFT), is simply a sampled version of the Fourier transform where:

$$F(k) = \sum_{m=0}^{N-1} f(m)\, \epsilon^{-j2\pi mk/N} \qquad (3)$$

The transform variable, k, corresponds to frequency, m to time, and N is a normalizing factor. The Fourier components, F(k), of the Discrete Fourier Transform are equivalent to the H(w) of the continuous Fourier Transform shown below.

$$H(w) = \int_{-\infty}^{+\infty} h(t)\, \epsilon^{-jwt}\, dt \qquad (4)$$

The fast Fourier transform performs the same function as the discrete Fourier transform but is much more computationally efficient.

MATRICES

Modern graphics and control systems make extensive use of matrix multiplications. For example, to reduce the scale of an object on a graphics screen one must multiply the address of every point on the object by a number less than 1. To scale the point P(X,Y,Z)

$$P'(X,Y,Z) = P(X,Y,Z)\cdot S(S_x,S_y,S_z)$$

$$= [X,Y,Z,1]\cdot \begin{vmatrix} S_x & 0 & 0 & 0 \\ 0 & S_y & 0 & 0 \\ 0 & 0 & S_z & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix}$$

$$P'(X,Y,Z) = [X\cdot S_x, Y\cdot S_y, Z\cdot S_z, 1] \qquad (5)$$

Similar operations abound in the control and graphics industries.

Note that each DSP technique requires multipliers to multiply two variables, and/or multiplier-accumulators to perform the multiplication and accumulate the sum of the products. Since the fastest microprocessors require about 5μs to perform a multiplication, their throughput rate—while performing the many repetitive operations called for by DSP—is quite slow. To enhance the speed of computation, dedicated peripheral devices operating at around 150ns per multiplication are required to obtain the throughput necessary for most of today's real-world signals. For this reason, multipliers are today the fundamental building block of DSP. Future unit device-functions for DSP will contain, in addition to multiplication, the on-chip memory, sequencing, and programming hooks necessary to perform the *complete* DSP algorithms shown above at considerably lower cost for comparable operations.

WHY USE DSP?

DSP is used to perform many of the same basic functions as analog signal processing. For example, analog filters and digital filters both pass signals in certain bands and attenuate signals outside that band. Digital signal processing, due to its higher cost, is used only when very high performance is required. For example, the 90th order FIR (finite impulse-response) filter transfer function shown in Figure 1 has a rolloff of 80dB/octave and can operate on 50kHz input signals. The phase response in the passband is linear.

The equivalent 13-pole analog filter would require at least seven op amps, many capacitors and resistors, and a long time to design. Moreover, the resulting filter would not be stable over time, temperature and power supply fluctuations; and to make it adjustable would be a near-impossible task.

Since the response of a digitally implemented filter is both stable and calculable—hence predictable—DSP is ideal for use in processors where stable implementation of very sharp rolloffs is required (e.g., spectrum analyzers and transmultiplexers) and/or where it is necessary to dynamically alter the transfer function of the system (e.g., adaptive filtering in the equalizer of a modem).

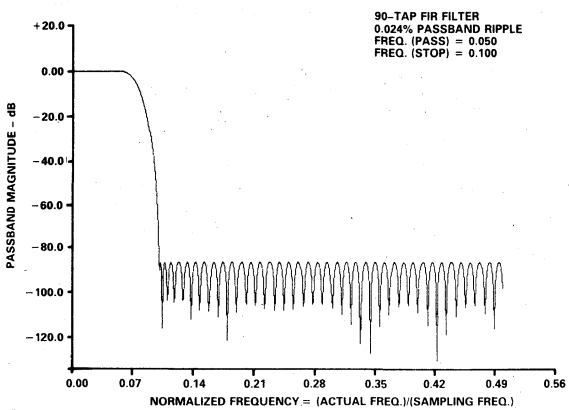


Figure 1. Normalized transfer function of 90-tap FIR filter having 0.024% passband ripple and 80dB/octave attenuation.

The advantages of digital signal processing in product development are substantial: prototype changes are commonly just software changes (high flexibility), and software simulation of the system will reflect the exact system performance. Simulation of analog systems cannot duplicate this precise correspondence. These advantages make DSP desirable in many applications where predictable performance is an inescapable requirement.

ANALOG DEVICES

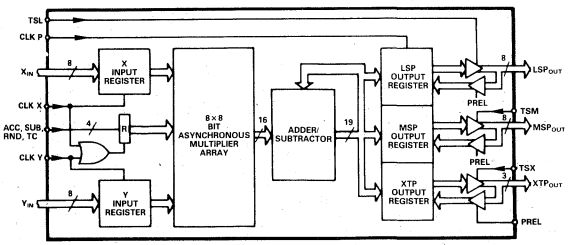
8×8-Bit CMOS Multiplier/Accumulator

ADSP-1008

FEATURES
- 8 × 8-Bit Parallel Multiplication/Accumulation
- 90mW Power Dissipation with CMOS Technology
- 105ns Multiply/Accumulate Time
- Improved TDC1008J Second Source
- Double Precision Adder With Three Guard Bits
- Available in 48-Pin DIP
- Single +5V Power Supply
- Specified from −55°C to +125°C Ambient

APPLICATIONS
- Matrix Manipulations
- Fourier Transformations
- Digital Filtering
- Image Processing

ADSP-1008 FUNCTIONAL BLOCK DIAGRAM



GENERAL INFORMATION

The ADSP-1008 is a TTL compatible high speed low power 8 × 8-bit multiplier accumulator that is pin for pin compatible with TRW's TDC1008J4. The ADSP-1008 has essentially the same speed as the TDC1008J but consumes only about 1/20 the power. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus, unlike existing bipolar and ECL devices, it is safe to both specify and operate the ADSP-1008 over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time saving techniques. A modified Booth algorithm reduces time consuming operations. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage of the multiplier.

The ADSP-1008 has two 8-bit input buses, two 8-bit product buses and a 3 bit extra product bus. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1008 to operate on an 8-bit bus.

The ADSP-1008 has a RND control which rounds the product to the 11 most significant bits by adding a 1 to the MSB of the LSP. The preload control is used in conjunction with the three state control to initialize the contents of the output registers.

The ACC and SUB controls are used to determine whether a multiply/add or a multiply/subtract, or a straight multiply is performed. The TC control is used to distinguish between two's complement or unsigned magnitude inputs.

The ADSP-1008 is available in a 48-pin ceramic DIP in high reliability or commercial grades.

PRODUCT HIGHLIGHTS

1. CMOS technology results in low 90mW max power dissipation.
2. Fast, 105ns, multiply time is ideal for digital signal processing applications.
3. The ADSP-1008 is an improved second source for the TDC1008J1.
4. The ADSP-1008 is specified and will operate over the extended temp range ambient.

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SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1008JD ADSP-1008KD Min	Max	ADSP-1008SD ADSP-1008TD Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

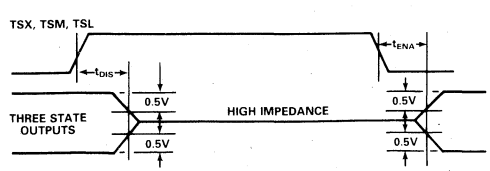
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1008JD ADSP-1008KD Min	Max	ADSP-1008SD ADSP-1008TD Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −0.4mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.8		0.8	V
I_{OH}	High-Level Output Current	@ V_{DD} = min & V_{OH} = 2.4V	−0.4		−0.4		mA
I_{OL}	Low-Level Output Current	@ V_{DD} = min & V_{OL} = 0.8V	4		4		mA
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0		10		10	µA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0		10		10	µA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max & High Z; V_{IN} = max		50		50	µA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max & High Z; V_{IN} = 0		10		10	µA
I_{CC}	Supply Current[2]			15		18	mA
I_{CC}	Quiescent	All V_{IN} = 0V; Trim & Tril = 5.0V		400		1500	µA
I_{CC}	Quiescent	All V_{IN} = 2.4V		10		15	mA

SWITCHING CHARACTERISTICS[3,4]

Parameter		ADSP-1008JD Min	Max@ 25°C	Max	ADSP-1008SD Min	Max@ 25°C	Max	ADSP-1008KD Min	Max@ 25°C	Max	ADSP-1008TD Min	Max@ 25°C	Max	Unit
t_D	Output Delay Three State Enable/Disable		35	40		*	45		*	45		*	45	ns
t_{ENA}	Z to High or Low		25	35		*	40		*	*		*	40	ns
t_{DIS}	High or Low to Z Figure 4													
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Set-Up Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MAC}	Multiply/Accumulate Time[4]		135	160		*	185		105	125		105	145	ns

NOTES
[1]All min & max specifications are over the power suply and temperature ranges indicated (unless otherwise noted).
[2]Maximum current is measured with the clock cycle = 10MHz and TTL input voltages.
[3]All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[4]Measured with power supply = +5.0V and TTL levels of 0.4V and 2.4V.
*Specifications same as ADSP-1008JD.
Specifications subject to change without notice.



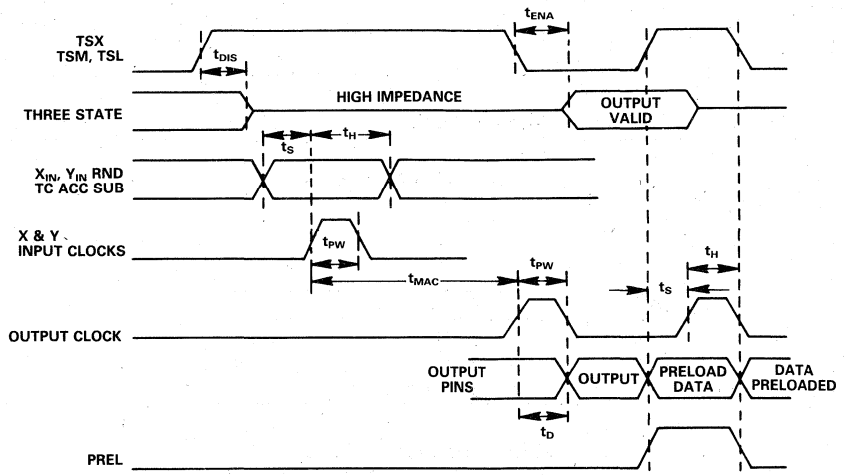


Figure 1. ADSP-1008 Timing Diagram

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip-flops. The RND, ACC, SUB and TC controls have a separate register which is loaded by the positive edge of either the X or Y input clocks. A logic 1 on the RND line rounds the product of the X & Y inputs to the 8 most significant bits by adding a 1 to the MSB of the 8 LSBs of the product.

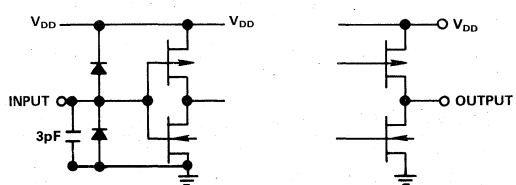
Once the inputs are loaded, they are multiplied and the product is then either added to the previous value of the output registers, or the value of the output registers is subtracted from the product, or the product is routed directly to the output registers. The ACC and SUB controls are used to determine which operation is performed (see Table II).

The output consists of three words: an 8-bit LSP, an 8-bit MSP and a 3-bit extended product, XTP. The rising edge of CLKP latches the LSP, MSP and the XTP into the output flip-flops.

TSL, TSH and TSX are the three state controls for the LSP, MSP, and XTP respectively. A logic 1 on TSL, TSH or TSX causes the appropriate output to be disabled. Similarly a logic 0 on TSL, TSH or XTP enables the appropriate output. These controls can be used in conjunction with the separate input clocks to interface the ADSP-1008 to an 8-bit bus.

The preload control, PREL, is used to initialize the output registers. If PREL is high and either the TSH, TSL or TSX control is also high the data located on the output pins controlled by the high three state is loaded into the output register on the rising edge of CLKP. PREL along with TSL, TSH and TSX can be used to preload either one, two, or all of the output registers simultaneously (see Table III) on the rising edge of CLKP.

The registered two's complement control, TC, allows multiplication of either two's complement or unsigned magnitude inputs (see Table I). When TC is a logic 1 the inputs are two's complement numbers. When TC is low, the inputs are in an unsigned magnitude format. (Negative full scale) × (negative full scale) will yield a valid +1 product in the ADSP-1008. The three additional most significant bits, XTP, accommodate valid summation of several large products. The sign bit is extended into these bits when the summation only occupies the lesser significant bits of the accumulator. For example, if the accumulated product only occupies the least eight significant bit positions the sign would extend from bit 8 through bit 18.



a. Equivalent Input Circuit *b. Equivalent Output Circuit*

Figure 2.

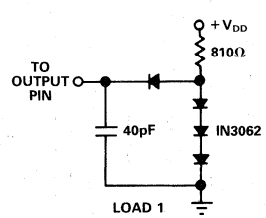


Figure 3. Normal Delay Measurement Loads

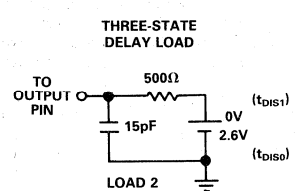


Figure 4. Three State Delay Measurement Load

X & Y INPUT DATA								OUTPUT DATA FORMATS															
BIT							LSB	XTP			MSP									LSP			
7	6	5	4	3	2	1	0	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACTIONAL TWO'S COMPLEMENT																										
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-2^4	2^3	2^2	2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
INTEGER TWO'S COMPLEMENT																										
-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	-2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
UNSIGNED MAGNITUDE																										
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table I. Data Formats

ACC	SUB	Function
1	1	$Output_t = X_t \cdot Y_t - Output_{t-1}$
1	0	$Output_t = X_t \cdot Y_t + Output_{t-1}$
0	X	$Output_t = X_t \cdot Y_t$

Table II. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance. Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table III. Preload Truth Table

PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	P12	25	X3
2	P11	26	X4
3	P10	27	X5
4	P9	28	X6
5	P8	29	X7
6	TSM	30	CLK X
7	CLK P	31	CLK Y
8	PREL	32	Y0
9	P7	33	Y1
10	P6	34	Y2
11	P5	35	Y3
12	GND	36	Y4
13	P4	37	V_{DD}
14	P3	38	Y5
15	P2	39	Y6
16	P1	40	Y7
17	P0	41	TC
18	TSL	42	TSX
19	SUB	43	P18
20	ACC	44	P17
21	RND	45	P16
22	X0	46	P15
23	X1	47	P14
24	X2	48	P13

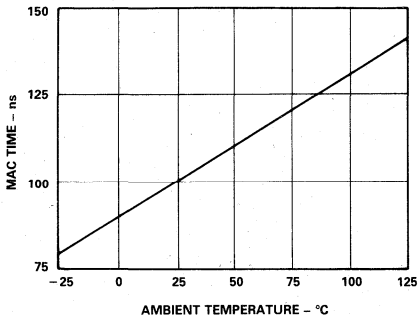


Figure 5. Approx. MAC Time vs. Temperature

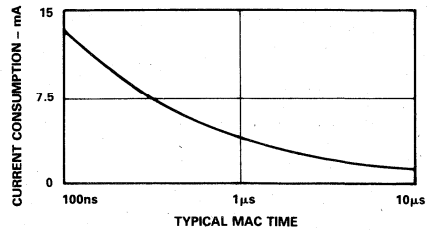


Figure 6. Typical I_{DD} vs. Frequency of Operation

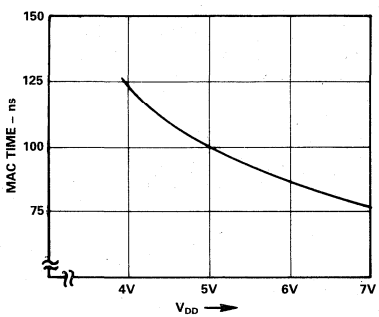


Figure 7. Typical MAC Time vs. Power Supply

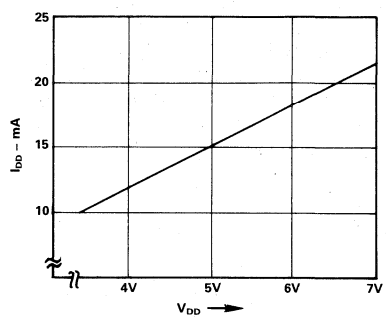


Figure 8. Typical I_{DD} vs. V_{DD} at f=8MHz; t_a=25°C; CMOS Inputs

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OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction the speed of the ADSP-1008 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies four parameters will change which in turn will effect the circuit design. These parameters are: input thresholds, output voltage swings, MAC speed and power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the MAC will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 7 shows the MAC speed will increase as the supply voltage increases and decrease as the supply voltages decreases. The change in speed is due to the dependence of the transconductance of CMOS devices on supply voltages.

Figure 8 shows that increasing power supply voltage also increases the power consumption of the device. Notice, however, that the worst case current consumption is only 22mA when using a 7.0V power supply.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3 to V_{DD}
Output Voltage	−0.3 to V_{DD}
Operating Temperature Range ($T_{AMBIENT}$)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C
Junction Temperature	175°C

ORDERING INFORMATION

Part Number	Temperature Range	Package
ADSP-1008KD	0 to +70°C	48-Pin Ceramic DIP (D48A)
ADSP-1008JD	0 to +70°C	48-Pin Ceramic DIP (D48A)
ADSP-1008TD	−55°C to +125°C	48-Pin Ceramic DIP (D48A)
ADSP-1008SD	−55°C to +125°C	48-Pin Ceramic DIP (D48A)

See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

APPLICATIONS

Temporal Averaging

Temporal Averaging is a well known method of reducing the noise in a picture or waveform. It is accomplished by averaging successive frames of an image or samples of a waveform. One particularly useful technique of temporal averaging is exponential smoothing.

The general form of the exponential smoothing model can be expressed as:

$$\hat{X}_t = \alpha X_t + (1-\alpha)\hat{X}_{t-1}$$

where:

X_t is a waveform or image frame with noise in it;

$\hat{X}_t$ is the averaged or smoothed waveform or signal; and

$\hat{X}_{t-1}$ is the smoothed sample one time period prior to X_t.

To see how exponential smoothing works like an average let $\alpha = 1/2$. Then

$$\hat{X}_t = 1/2\, X_t + 1/2\, \hat{X}_{t-1}$$

Which says that the "averaged" sample is equal to 1/2 the new sample (image or waveform plus noise) plus 1/2 the previous smoothed sample. This result is similar to the straight average of 2 frames. Notice, however, that for the t+1 frame or waveform:

$$\begin{aligned}\hat{X}_{t+1} &= 1/2\, X_{t+1} + 1/2\, \hat{X}_t \\ &= 1/2\, X_{t+1} + 1/2\,(1/2\, X_t + 1/2\, \hat{X}_{t-1}) \\ &= 1/2\, X_{t+1} + 1/4\, X_t + 1/4\, \hat{X}_{t-1}\end{aligned}$$

As is shown, the weight of the sample X_t and its effect on the smoothed image will be exponentially decreasing over time.

It can be shown that the noise reduction achieved with exponential smoothing is

$$\sqrt{\frac{\alpha}{2-\alpha}}$$

From a heuristic viewpoint, the random noise in a frame will add to the average only once whereas any stationary object will add to the average many times. Thus the power of the object in the averaged image is increased relative to the power of the random noise.

If $\alpha = 1/2$ as in the above example the noise reduction would be $1/\sqrt{3}$. Figure 9 shows the improvement in the signal to noise ratio of an image or waveform for different values of α.

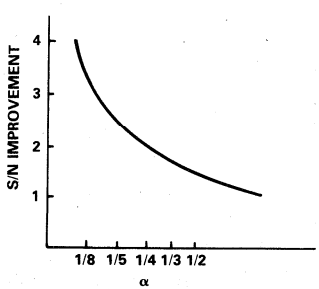


Figure 9. Noise Improvement with Exponential Smoothing

Noise Reduction vs. Motion Artifacts

If the objects in the image are not stationary, averaging will introduce motion artifacts. These artifacts are directly analogous to the effect obtained by taking a picture of a fast moving object with film that is too slow. The greater the number of frames or waveforms averaged and the faster the objects in the image or transients in the waveform are moving, the worse will be the motion artifacts induced by an average.

Notice from the general form of the exponential smoothing model that for different values of α the weight of the most recent sample X_t on the smoothed image or waveform can be varied. If $\alpha = 1$ the smoothed or averaged waveform is identically equal to the most recent sample. Thus no averaging takes place. If, on the other hand, α is very small, say 1/32, the effect of the most recent sample X_t will be very small. For images with fast moving objects, α must be made larger to avoid motion artifacts. For stationary images and waveforms, small α's guarantee significant noise reduction. From an empirical knowledge of the artifact inducing effects of motion and from Figure 9 an optimal value of α can be chosen. Since α can be larger than 1/2 in an exponential smoothing scheme, it can be used to obtain some S/N reduction in images with fast moving objects or waveforms with some variation. The improvement of the signal to noise ratio under these circumstances is unobtainable using other averaging techniques.

ADSP-1008 is an easy low power method of implementing exponential smoothing as is shown in Figure 10. Notice that no additional image or waveform memory, beyond that for the display, is required.

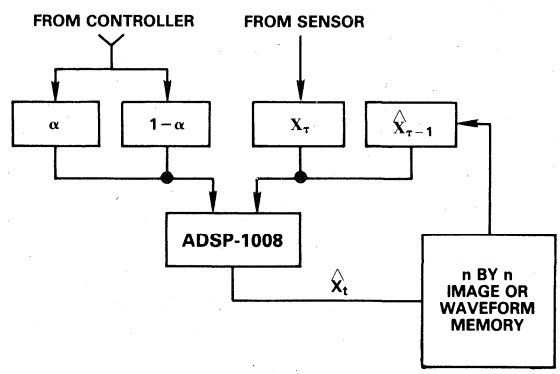


Figure 10. Exponential Smoothing with the ADSP-1008

The i^{th} pixel of the smoothed $\hat{X}_{t-1}$ frame is fetched from the n by n image memory when reading the i^{th} pixel of the new X_t. The i^{th} pixel of the $\hat{X}_{t-1}$ frame is multiplied by $1-\alpha$ and stored in the accumulator. The i^{th} pixel of X_t is then multiplied by α and added to $(1-\alpha)\, X_{t-1}$. This result is then stored in the i^{th} pixel as $\hat{X}_t$. Waveform smoothing is similar except the memory is n by 1. With minimal control logic the ADSP-1008 is capable of smoothing a 512 × 512 × 8 image memory in real time (30 frames/sec). If higher resolutions are required, say 1024 × 1024 × 8, then 2 ADSP-1008s should operate in a parallel architecture to handle real time imaging.

In many imaging situations, objects within the scene are sometimes in motion and sometimes at rest. If the motion can be detected or predicted the coefficients, α and $1-\alpha$ can be changed in real time to always provide the optimal trade off between smoothing and motion artifacts.

ANALOG DEVICES

12×12-Bit CMOS Multiplier/Accumulator

ADSP-1009

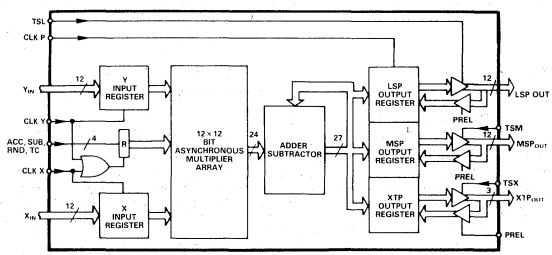
FEATURES

12 × 12-Bit Parallel Multiplication/Accumulation
150mW Power Dissipation with CMOS Technology
130ns Multiply/Accumulate Time
Improved TDC1009J Second Source
Available in 64-Pin Ceramic DIPs, or 68-Terminal Leadless Chip Carrier or 68-Pin Grid Arrays
Specified from −55°C to +125°C Ambient

APPLICATIONS

Digital Signal Processing
Digital Filtering
Fourier Transformations
Correlations
Matrix Manipulations
Image Processing

ADSP-1009 FUNCTIONAL BLOCK DIAGRAM



GENERAL INFORMATION

The ADSP-1009 is a TTL compatible high speed low power 12 by 12-bit multiplier/accumulator that, in DIP form, is pin for pin compatible with TRW's TDC1009J. The ADSP-1009 has essentially the same speed as the TDC1009J but consumes only about 1/20 the power. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus unlike most bipolar and ECL devices it is safe to both specify and operate the ADSP-1009 over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time saving techniques. A modified Booth algorithm is used. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage of the multiplier.

The ADSP-1009 has two 12-bit input buses, a 12-bit MSP product bus, a 12-bit LSP product bus, and a 3-bit extended product bus. All inputs are diode protected. The independently controlled input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1009 to operate from a single bus.

The ADSP-1009 has a RND control that rounds the product to the 12 most significant bits by adding a 1 to the MSB of the 12 LSBs of the multiplier array. The preload control is used in conjunction with the three state controls to initialize the contents of the output registers. The ADSP-1009 will perform either a multiplication and addition or multiplication and subtraction or a straight multiplication depending upon the status of the ACC and SUB controls. The TC control provides the capability for either two's complement or unsigned magnitude data formats.

The ADSP-1009 is available in either hermetically sealed 64-pin ceramic DIPs or 68-terminal leadless chip carriers or 68-pin grid arrays. Each package is available in high reliability or commercial grades.

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PRODUCT HIGHLIGHTS

1. The ADSP-1009, by virtue of its fast CMOS technology, provides both low power (150mW) and high speed (130ns). Full TTL compatibility is supplied without the need for external buffering.
2. The ADSP-1009 provides full pin-for-pin compatibility with the TDC1009J1. High performance is available to the user with greater than an order of magnitude reduction in power consumption.
3. The ADSP-1009 is also available in a 68-pin grid array or 68-terminal leadless chip carrier. Now designers can reduce their systems physical size without worrying about power dissipation.

ADSP-1009 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS Parameter		ADSP-1009JX[2] ADSP-1009KX Min	Max	ADSP-1009SX ADSP-1009TX Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

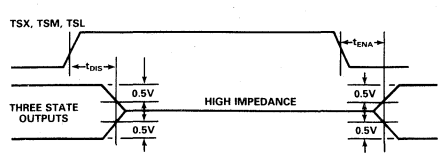
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1009JX ADSP-1009KX Min	Max	ADSP-1009SX ADSP-1009TX Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −0.4mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	μA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	μA
I_{DD}	Supply Current[3]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V; Trim & Tril = 5.0V		400		500	μA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[4,5]

		ADSP-1009JX			ADSP-1009SX			ADSP-1009KX			ADSP-1009TX			Unit
		Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	
t_D	Output Delay		35	40		*	45		*	*		*	45	ns
t_{ENA}	Z to High or Low		25	35		*	40		*	*		*	40	ns
t_{DIS}	High or Low to Z (Figure 5)													
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MAC}	Multiply/Accumulate Time		165	195		*	225		130	155		130	180	ns

NOTES
[1]All min & max specifications have + 5.0V power supply and are over specified temperature ranges unless otherwise stated.
[2]When ordering, substitute for X: D for 64-pin DIP, E for 68-terminal leadless chip carrier G for 68-pin grid array.
[3]Maximum current is measured with the clock cycle = 8MHz and TTL input voltages.
[4]All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[5]Measured with power supply at + 5.0V and TTL input voltages of 0.4V and 2.4V.
*Specifications same as ADSP-1009JX.
Specifications subject to change without notice.



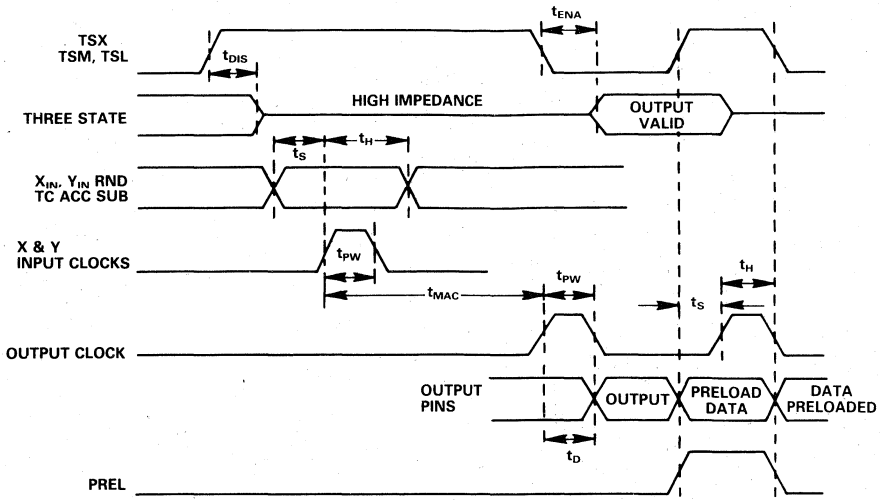


Figure 1. ADSP-1009 Timing Diagram

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip-flops. The RND, ACC, SUB and TC controls have a separate register which is loaded by the positive edge of either the X or Y input clocks. The output consists of three words: a 12-bit LSP, a 12-bit MSP and a 3-bit extended product. The rising edge of CLKP latches the LSP, MSP and the XTP into the output flip-flops.

Additionally each output register has its own three state control. A logic 1 on the TSL, TSH or TSX line disables the corresponding LSP, MSP or XTP product register. Similarly a logic 0 on TSL, TSH or TSX enables the appropriate output.

A logic 1 on the RND line rounds the product of the X & Y inputs to the 15 most significant bits by adding a 1 to the MSB of the LSP. Once the inputs are loaded, they are multiplied and the product is then either added to the previous value of the output registers, or the value of the output registers is subtracted from the product, or the product is stored directly in the output registers. The status of the ACC and SUB controls determines which operation is performed (see Table II).

The preload control PREL is used to initialize the output registers. If PREL is high and either TSH, TSL or TSX is also high the data located on the output pins controlled by the high three state is loaded into the output register on the rising edge of CLKP. PREL along with TSL, TSH and TSX can be used to preload either one, two or all of the output registers simultaneously (see Table III).

The registered two's complement control, TC, allows multiplication of either two's complement or unsigned magnitude inputs. When TC is a logic 1 the inputs are two's complement numbers. When TC is low the inputs are in an unsigned magnitude format. (Negative full scale) X (negative full scale) will yield a valid positive full scale product in the ADSP-1009.

The three additional most significant bits, XTP, accommodate valid summation of several large products. The sign bit is extended into these bits when the summation only occupies lesser significant bits of the accumulator. For example if the accumulated product only occupies the least 18 significant bit positions the sign would extend from Bit 19 through Bit 26.

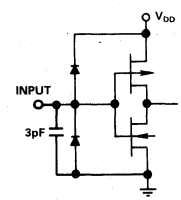


Figure 2. Equivalent Input Circuits

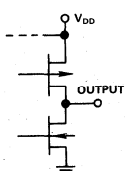


Figure 3. Equivalent Output Circuits

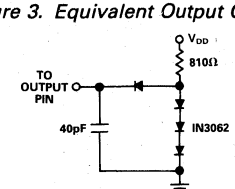


Figure 4. Normal Load Circuit for Delay Measurements

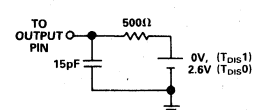


Figure 5. Three-State Delay Load Circuit

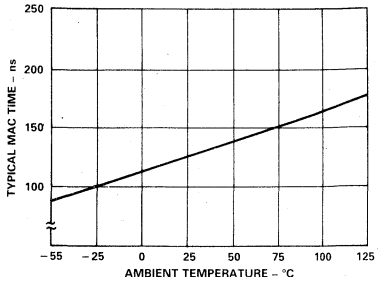


Figure 6. Approx. Multiply Time vs. Temperature

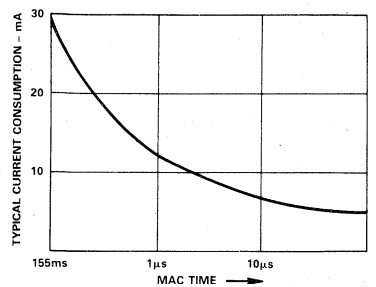


Figure 7. Typical I_{DD} vs. Frequency of Operation

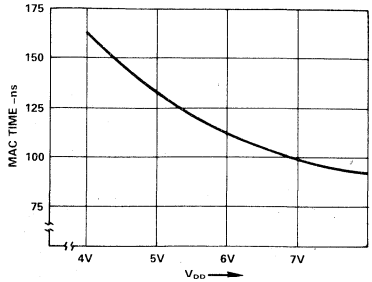


Figure 8. Typical MAC Time vs. Power Supply

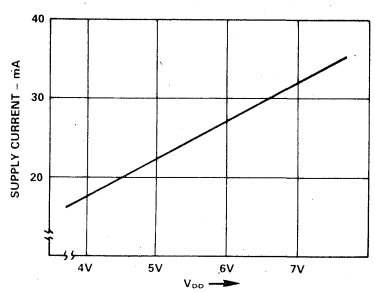


Figure 9. Typical I_{DD} vs. V_{DD} at f = 8MHz; t_a = 25°C; CMOS Inputs

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction the speed of the ADSP-1009 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies four parameters will change which in turn will effect the circuit design. These parameters are: input thresholds, output voltage swings, multiplication speed and power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 8 shows the multiplication speed will increase as the supply voltage increases and decrease as the supply voltages decreases. The change in speed is due to the dependence of transconductance of CMOS devices on supply voltages.

Figure 9 shows that increasing power supply voltage also increases the power consumption of the device. Notice, however, that the worst case power consumption is only 32mA when using a 7.0V power supply.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.3V to 7V
Input Voltage	–0.3V to V_{DD}
Output Voltage Range	–0.3V to V_{DD}
Operating Temperature Range ($T_{AMBIENT}$)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION*

Part Number	Temperature Range	Package*
ADSP-1009KD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1009JD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1009TD	–55°C to +125°C	64-Pin Ceramic DIP (D64A)
ADSP-1009SD	–55°C to +125°C	64-Pin Ceramic DIP (D64A)

*To obtain a 68-pin Grid Array, replace the suffix D by G (G68A).
To obtain a 68-terminal Leadless Chip Carrier, replace the suffix D by E (E68C).
See Section 19 for package outline information.

X & Y INPUT DATA FORMATS							OUTPUT DATA FORMATS																		
							XTP			MSP						LSP									
11	10	9	------	2	1	0	26	25	24	23	22	21	------	14	13	12	11	10	9	------	2	1	0
INTEGER TWO'S COMPLEMENT TC = 1																									
SGN																									
(-2^{11})	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}	-2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	------	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}
FRACTIONAL TWO'S COMPLEMENT TC = 1																									
SGN																									
(-2^{0})	2^{-1}	2^{-2}	------	2^{-9}	2^{-10}	2^{-11}	-2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	------	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	------	2^{-20}	2^{-21}	2^{-22}
UNSIGNED MAGNITUDE (INTEGER) TC = 0																									
2^{15}	2^{14}	2^{13}	------	2^{2}	2^{1}	2^{0}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	------	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}

Table I. Data Formats

ACC	SUB	Function
1	1	$Output_t = X_t \cdot Y_t - Output_{t-1}$
1	0	$Output_t = X_t \cdot Y_t + Output_{t-1}$
0	X	$Output_t = X_t \cdot Y_t$

Table II. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance, or output disabled. Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table III. Preload Truth Table

PIN CONFIGURATION FOR DIP

PIN	FUNCTION	PIN	FUNCTION
1	X4	33	P19
2	X3	34	P20
3	X2	35	P21
4	X1	36	P22
5	X0	37	P23
6	ACC	38	P24
7	SUB	39	P25
8	RND	40	P26
9	TSL	41	TSX
10	P0	42	TC
11	P1	43	Y11
12	P2	44	Y10
13	P3	45	Y9
14	P4	46	Y8
15	P5	47	Y7
16	GND	48	Y6
17	P6	49	V_{DD}
18	P7	50	Y5
19	P8	51	Y4
20	P9	52	Y3
21	P10	53	Y2
22	P11	54	Y1
23	CLKP	55	Y0
24	PREL	56	CLKY
25	TSM	57	CLKX
26	P12	58	X11
27	P13	59	X10
28	P14	60	X9
29	P15	61	X8
30	P16	62	X7
31	P17	63	X6
32	P18	64	X5

PACKAGE D64A

PIN CONFIGURATION FOR LCC

PIN	FUNCTION	PIN	FUNCTION
1	X4	35	P19
2	X3	36	P20
3	X2	37	P21
4	X1	38	P22
5	X0	39	P23
6	ACC	40	P24
7	SUB	41	P25
8	RND	42	P26
9	N/C	43	N/C
10	TSL	44	TSX
11	P0	45	TC
12	P1	46	Y11
13	P2	47	Y10
14	P3	48	Y9
15	P4	49	Y8
16	P5	50	Y7
17	GND	51	Y6
18	P6	52	V_{DD}
19	P7	53	Y5
20	P8	54	Y4
21	P9	55	Y3
22	P10	56	Y2
23	P11	57	Y1
24	CLKP	58	Y0
25	PREL	59	CLKY
26	N/C	60	N/C
27	TSM	61	CLKX
28	P12	62	X11
29	P13	63	X10
30	P14	64	X9
31	P15	65	X8
32	P16	66	X7
33	P17	67	X6
34	P18	68	X5

PACKAGE E68C

PIN CONFIGURATION FOR PIN GRID ARRAY

PIN	FUNCTION	PIN	FUNCTION
1	TSL	35	TSX
2	P0	36	TC
3	P1	37	Y11
4	P2	38	Y10
5	P3	39	Y9
6	P4	40	Y8
7	P5	41	Y7
8	GND	42	Y6
9	P6	43	V_{DD}
10	P7	44	Y5
11	P8	45	Y4
12	P9	46	Y3
13	P10	47	Y2
14	P11	48	Y1
15	CLK P	49	Y0
16	PREL	50	CLK Y
17	N/C	51	N/C
18	TSM	52	CLK X
19	P12	53	X11
20	P13	54	X10
21	P14	55	X9
22	P15	56	X8
23	P16	57	X7
24	P17	58	X6
25	P18	59	X5
26	P19	60	X4
27	P20	61	X3
28	P21	62	X2
29	P22	63	X1
30	P23	64	X0
31	P24	65	ACC
32	P25	66	SUB
33	P26	67	RND
34	N/C	68	N/C

PACKAGE G68A

ANALOG DEVICES

16×16-Bit CMOS Multiplier/Accumulator

ADSP-1010

FEATURES

- **16 × 16-Bit Parallel Multiplication/Accumulation**
- **150mW Power Dissipation With CMOS Technology**
- **165ns Multiply/Accumulate Time**
- **Improved TDC1010J Second Source**
- **Two's Complement or Unsigned Magnitude Data Formats**
- **Single +5V Power Supply**
- **Available in Hermetically Sealed 64-Pin Ceramic DIPs, 0.7 Square Inch Ceramic Flat Packs, 68-Pin Grid Array or 68-Terminal Leadless Chip Carrier**
- **Specified Over the Extended Temperature Range**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filtering**
  - **Fourier Transformations**
  - **Correlations**
  - **Power Series Expansions**
- **Matrix Manipulations**
- **Microprocessor Acceleration**

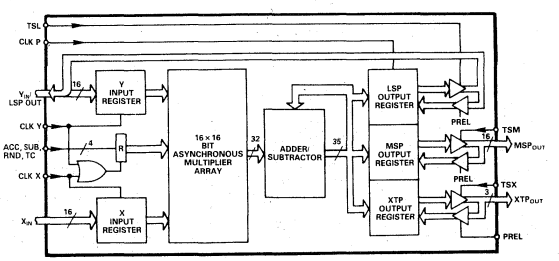
GENERAL INFORMATION

The ADSP-1010 is a TTL compatible high speed low power 16 by 16-bit monolithic multiplier/accumulator that, in DIP form, is pin for pin compatible with TRW's TDC1010J. The ADSP-1010 has essentially the same speed as the TDC1010J but consumes only about 1/20 the power. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus unlike most bipolar and ECL devices it is safe to both specify and operate the ADSP-1010 over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using CMOS technology. The high speed is obtained by the use of three time saving techniques. A modified Booth algorithm is used. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage of the multiplier.

The ADSP-1010 has two 16-bit input buses, a 16-bit MSP product bus, a 16-bit LSP product bus, the output port of which is shared with the Y input port, and a 3-bit extended product bus. All inputs are diode protected. The independently controlled input registers are D-type positive edge triggered flip-flops as are the product registers. Each product register has its own three state output control which, when combined with the independent input clocks, allows the ADSP-1010 to operate on a 16-bit microprocessor bus.

ADSP-1010 FUNCTIONAL BLOCK DIAGRAM



The ADSP-1010 has a RND control that rounds the product to the 16 most significant bits by adding a 1 to the MSB of the 16 LSBs of the multiplier array. The preload control is used in conjunction with the three state controls to initialize the contents of the output registers. The ADSP-1010 will perform either a multiplication and addition or multiplication and subtraction or a straight multiplication depending upon the status of the ACC and SUB controls. The TC control provides the capability for either two's complement or unsigned magnitude data formats.

The ADSP-1010 is available in either hermetically sealed 64-pin ceramic DIPs, 64-pin 0.7 square inch flat packs, a 68-pin Grid Array or a 68-terminal Leadless Chip Carrier. Each package is available in high reliability or commercial grades.

PRODUCT HIGHLIGHTS

1. The ADSP-1010, by virtue of its fast CMOS technology, provides both low power (150mW) and high speed (165ns). Full TTL compatibility is supplied without the need for external buffering.
2. The ADSP-1010 in DIP form, provides full pin-for-pin compatibility with the TDC1010J1. High performance is available to the user with greater than an order of magnitude reduction in power consumption.
3. The ADSP-1010 is also available in a 64-pin hermetically sealed flat pack, 68-pin Grid Array or 68-terminal LCC. Now designers can reduce their systems physical size without worrying about power dissipation and board space problems.

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ADSP-1010 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1010JX[2] ADSP-1010KX Min	ADSP-1010JX[2] ADSP-1010KX Max	ADSP-1010SX ADSP-1010TX Min	ADSP-1010SX ADSP-1010TX Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

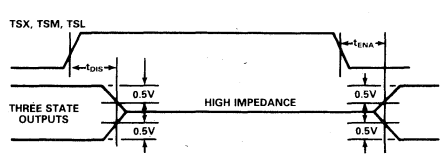
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1010JX ADSP-1010KX Min	ADSP-1010JX ADSP-1010KX Max	ADSP-1010SX ADSP-1010TX Min	ADSP-1010SX ADSP-1010TX Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5V		10		10	μA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	μA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	μA
I_{DD}	Supply Current[3]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V; TSM & TSL = 5.0V		500		2000	μA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[4,5]

		ADSP-1010JX Min	ADSP-1010JX Max@ 25°C	ADSP-1010JX Max	ADSP-1010SX Min	ADSP-1010SX Max@ 25°C	ADSP-1010SX Max	ADSP-1010KX Min	ADSP-1010KX Max@ 25°C	ADSP-1010KX Max	ADSP-1010TX Min	ADSP-1010TX Max@ 25°C	ADSP-1010TX Max	Unit
t_D	Output Delay		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MAC}	Multiply/Accumulate Time		200	240		180	250		165	190		165	220	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]When ordering substitute for X: D for 64-pin DIP, E for 68-terminal leadless chip carrier, G for 68-pin grid array or F for 64-pin flat pack.
[3]Maximum current is measured with the clock cycle = 6MHz and TTL input voltages.
[4]All transitions are measured at a +1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[5]Measured with power supply at +5V and TTL levels of 0.4V and 2.4V.
*Specifications same as ADSP-1010JD.
Specifications subject to change without notice.



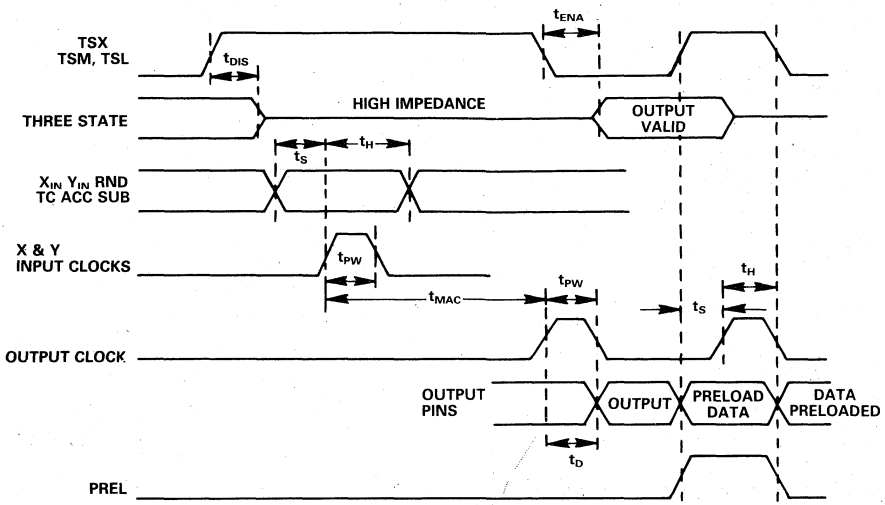


Figure 1. ADSP-1010 Timing Diagram

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip-flops. The RND, ACC, SUB and TC controls have a separate register which is loaded by the positive edge of either the X or Y input clocks. The output consists of three words: a 16-bit LSP, a 16-bit MSP and a 3-bit extended product. The rising edge of CLKP latches the LSP, MSP and the XTP into the output flip-flops.

Additionally each output register has its own three state control. A logic 1 on the TSL, TSH or TSX line disables the corresponding LSP, MSP or XTP product register. Similarly a logic 0 on TSL, TSH or TSX enables the appropriate output. These controls can be used in conjunction with the separate input clocks to interface the ADSP-1010 to a 16-bit bus.

A logic 1 on the RND line rounds the product of the X & Y inputs to the 19 most significant bits by adding a 1 to the MSB of the LSP. Once the inputs are loaded, they are multiplied and the product is then either added to the previous value of the output registers, or the value of the output registers is subtracted from the product, or the product is stored directly in the output registers. The status of the ACC and SUB controls determines which operation is performed (see Table I).

The preload control PREL is used to initialize the output registers. If PREL is high and either TSH, TSL or TSX is also high the data located on the output pins controlled by the high three state is loaded into the output register on the rising edge of CLKP. PREL along with TSL, TSH and TSX can be used to preload either one, two or all of the output registers simultaneously (see Table II).

The registered two's complement control, TC, allows multiplication of either two's complement or unsigned magnitude inputs. When TC is a logic 1 the inputs are two's complement numbers. When TC is low the inputs are in an unsigned magnitude format. (Negative full scale) X (negative full scale) will yield a valid positive full scale product in the ADSP-1010.

The three additional most significant bits, XTP, accommodate valid summation of several large products. The sign bit is extended into these bits when the summation only occupies lesser significant bits of the accumulator. For example if the accumulated product only occupies the least 16 significant bit positions the sign would extend from Bit 17 through Bit 35.

ACC	SUB	Function
1	1	$Output_t = X_t \cdot Y_t - Output_{t-1}$
1	0	$Output_t = X_t \cdot Y_t + Output_{t-1}$
0	X	$Output_t = X_t \cdot Y_t$

Table I. Function Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	Z
0	0	1	0	Q	Z	Q
0	0	1	1	Q	Z	Z
0	1	0	0	Z	Q	Q
0	1	0	1	Z	Q	Z
0	1	1	0	Z	Z	Q
0	1	1	1	Z	Z	Z
1	0	0	0	Z	Z	Z
1	0	0	1	Z	Z	Preload
1	0	1	0	Z	Preload	Z
1	0	1	1	Z	Preload	Preload
1	1	0	0	Preload	Z	Z
1	1	0	1	Preload	Z	Preload
1	1	1	0	Preload	Preload	Z
1	1	1	1	Preload	Preload	Preload

NOTE:
Z = Output buffers at high impedance (output disabled)
Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.
Preload = Output buffers at high impedance, or output disabled. Preload data (PD) supplied externally at output pins will be loaded into the output register at the rising edge of CLK P.

Table II. Preload Truth Table

X & Y INPUT DATA FORMATS							OUTPUT DATA FORMATS																	
							XTP			MSP							LSP								
15	14	13	------	2	1	0	34	33	32	31	30	29	------	18	17	16	15	14	13	------	2	1	0
INTEGER TWO'S COMPLEMENT TC = 1																								
SGN																								
(-2^{15})	2^{14}	2^{13}	------	2^{2}	2^{1}	2^{0}	-2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	------	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	------	2^{2}	2^{1}	2^{0}
FRACTIONAL TWO'S COMPLEMENT TC = 1																								
SGN																								
(-2^{0})	2^{-1}	2^{-2}	------	2^{-13}	2^{-14}	2^{-15}	-2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	2^{-1}	------	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	------	2^{-28}	2^{-29}	2^{-30}
UNSIGNED MAGNITUDE (INTEGER) TC = 0																								
2^{15}	2^{14}	2^{13}	------	2^{2}	2^{1}	2^{0}	2^{34}	2^{33}	2^{32}	2^{31}	2^{30}	2^{29}	------	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	------	2^{2}	2^{1}	2^{0}

Table III. Data Formats

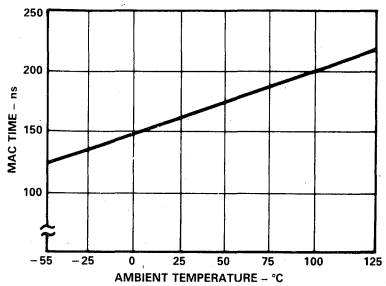


Figure 2. Approx. Worst Case Mutiply Time vs. Temperature

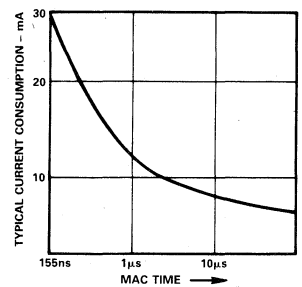


Figure 3. Typical I_{DD} vs. Frequency of Operation

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage Swing	−0.3V to V_{DD}
Output Voltage Range	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION*

Part Number	Temperature Range	Package
ADSP-1010KD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1010JD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1010TD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)
ADSP-1010SD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)

*To order 64-pin ceramic flat packs, replace the suffix D by F (F64A).
To order a 68-pin grid array, replace the suffix D by G (G68A).
To order a 68-terminal leadless chip carrier, replace the suffix D by E (E68C).
See Section 19 for package outline information.

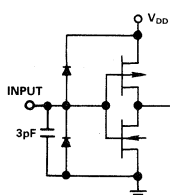


Figure 4. Equivalent Input Circuits

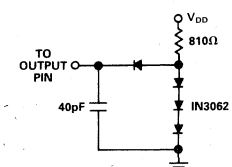


Figure 6. Normal Load Circuit for Delay Measurements

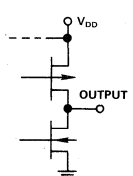


Figure 5. Equivalent Output Circuits

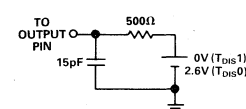


Figure 7. Three-State Delay Load Circuit

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

FIR FILTER DESIGN

Recent improvements in VLSI technology have led to the ability to economically implement digital filters. Compared to analog filtering the digital approach offers the advantages of no short-term drift with temperature or power supply fluctuations, no long term drift with age, architectures that eliminate phase distortion, identical performance in final products without individual tuning, and the capability for extremely high performance.

There are three classes of digital filters; finite impulse response (FIR), infinite impulse response (IIR), and lattice filters. Lattice filters have no general design theory, precluding their wide acceptance. Tradeoffs between FIR and IIR usually dictate which is appropriate for a given application.

The advantages of FIR filters are that the phase response can be made linear, that the filter has no poles and is, therefore, always stable, and that they are relatively easily designed and implemented. IIR filters, on the other hand, require fewer multiplications to yield a specified rolloff, which makes them faster and less expensive.

Since FIR filters have such unique and advantageous properties, their design will be discussed below:

Design of FIR Filters

The equation for a FIR filter is

$$(1) \qquad Y_n = \sum_{k=0}^{n-1} h_{(k)} X_{(n-k)}$$

where $Y_{(n)}$ = the filter output at time n
$X_{(n-k)}$ = the filter inputs
$h_{(k)}$ = coefficients corresponding to the impulse response of the filter

To see how (1) describes a filter, remember that the convolution of two signals in the time domain is equivalent to multiplication in the frequency domain. Assume that the coefficients $h_{(k)}$ can be weighted in the time domain so that when transformed to the frequency domain they describe the desired filter response. Then convolving the $X_{(n-k)}$ with the $h_{(k)}$ through equation 1 has the effect of multiplying the spectrum of the $X_{(n-k)}$ with that of the $h_{(k)}$. Since the spectrum of the $h_{(k)}$ is the desired filter response, the $X_{(n-k)}$ are filtered.

To design a FIR filter, then, requires one to determine the number of and value of the coefficients $h_{(k)}$. Several techniques exist to determine the coefficients. A very powerful and easy-to-use technique is the Remez Exchange, which will yield the best possible set of coefficients in the large majority of all filter designs. Optimal in this case means that, for a given filter's specifications, the Remez Exchange will design a filter with the minimum number of coefficients. Futhermore, the ripples in the passband will all have the same amplitude.

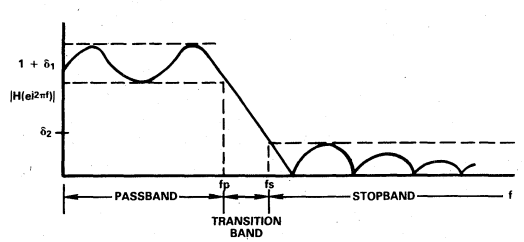


Figure 8. Filter Parameter Definition

The Remez Exchange is a linear programming algorithm that has been coded in FORTRAN. While it is relatively new (1973), it is well tested and reliable. The algorithm, the program flow chart and the FORTRAN listing are available from ADI by calling your local sales office.

To use the Remez Exchange, four steps are required:

(1) Specify the desired filter characteristics, δ_1, and δ_2, fp, fs and the sample rate of the data (see Figure 8).

For the program listing supplied by ADI, these definitions are the traditional FIR representations.

Passband Ripple = $20\ LOG_{10}\ (1 + \delta_1)$
Stopband Ripple = $20\ LOG_{10}\ (\delta_2)$
fp and fs are normalized to the sample rate.

(2) The order of the filter (for a FIR filter the number of coefficients) N is determined from the empirical formula

$$N = \frac{10\ LOG_{10}\ (\delta_1 \cdot \delta_2) - 15}{14\Delta F} + 1$$

This formula will yield a value of N which is around ±3 to the optimal number of coefficients for the filter parameters specified. The program could also be used to derive an estimate of N, as explained in the listing.

(3) Four cards are punched containing the relevant information. The format of these cards is explained in the program listing.

(4) The program is run and the coefficients are obtained.

To demonstrate the ease with which a filter can be designed suppose that you were designing a spectrum analyzer that required a low pass filter with the following charcteristics. The input sample frequency = 50kHz. The passband is from 0-1.2kHz. At 5kHz the stopband must be at −80dB. The maximum allowable passband ripple is .024%.

For the above filter the inputs would be:

Card #1 90, 1, 2, 0, 32
Card #2 0, 0.05, .1, 0.5
Card #3 1, 0
Card #4 1, 2.5

The coefficients as determined from the Remez Exchange are:

```
**********************************************************
                FINITE IMPULSE RESPONSE (FIR)
                LINEAR PHASE DIGITAL FILTER DESIGN
                REMEZ EXCHANGE ALGORITHM

                BANDPASS FILTER

 FILTER LENGTH =  90

 ***** IMPULSE RESPONSE *****
       H(  1) =  0.93799514E-04 = H(  90)
       H(  2) =  0.10488340E-03 = H(  89)
       H(  3) =  0.11847904E-03 = H(  88)
       H(  4) =  0.85088803E-04 = H(  87)
       H(  5) = -0.12898787E-04 = H(  86)
       H(  6) = -0.17661217E-03 = H(  85)
       H(  7) = -0.38194761E-03 = H(  84)
       H(  8) = -0.57682040E-03 = H(  83)
       H(  9) = -0.68772736E-03 = H(  82)
       H( 10) = -0.63653802E-03 = H(  81)
       H( 11) = -0.36574117E-03 = H(  80)
       H( 12) =  0.13416487E-03 = H(  79)
       H( 13) =  0.80301304E-03 = H(  78)
       H( 14) =  0.15048269E-02 = H(  77)
       H( 15) =  0.20436598E-02 = H(  76)
       H( 16) =  0.22036058E-02 = H(  75)
```

```
H( 17) =  0.18075542E-02 = H(  74)
H( 18) =  0.78227866E-03 = H(  73)
H( 19) = -0.78809389E-03 = H(  72)
H( 20) = -0.26394441E-02 = H(  71)
H( 21) = -0.43506525E-02 = H(  70)
H( 22) = -0.54176589E-02 = H(  69)
H( 23) = -0.53703832E-02 = H(  68)
H( 24) = -0.39105113E-02 = H(  67)
H( 25) = -0.10369754E-02 = H(  66)
H( 26) =  0.28777565E-02 = H(  65)
H( 27) =  0.70922608E-02 = H(  64)
H( 28) =  0.10598276E-01 = H(  63)
H( 29) =  0.12314963E-01 = H(  62)
H( 30) =  0.11345266E-01 = H(  61)
H( 31) =  0.72430554E-02 = H(  60)
H( 32) =  0.22823620E-03 = H(  59)
H( 33) = -0.87108370E-02 = H(  58)
H( 34) = -0.17870698E-01 = H(  57)
H( 35) = -0.25054727E-01 = H(  56)
H( 36) = -0.27939234E-01 = H(  55)
H( 37) = -0.24523273E-01 = H(  54)
H( 38) = -0.13575817E-01 = H(  53)
H( 39) =  0.50147623E-02 = H(  52)
H( 40) =  0.30071916E-01 = H(  51)
H( 41) =  0.59194371E-01 = H(  50)
H( 42) =  0.89057893E-01 = H(  49)
H( 43) =  0.11591199E+00 = H(  48)
H( 44) =  0.13618520E+00 = H(  47)
H( 45) =  0.14708640E+00 = H(  46)
```

A plot of such a filter's transfer function would appear as:

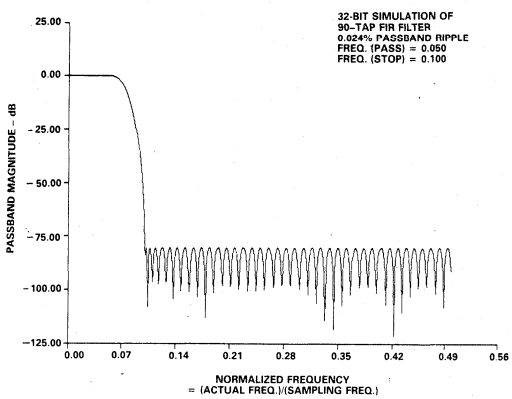


Figure 9. 32-Bit Simulation of 90-Tap FIR Filter

Once the filter coefficients have been determined, the hardware implementation is relatively straightforward. Equation (1) for a 5th order FIR filter can be expressed in hardware as:

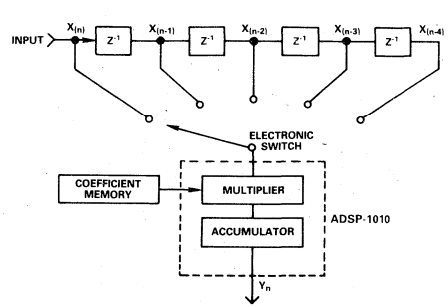


Figure 10. Hardware Implementation of FIR Filter

Note that the multiplier and accumulator can be combined on a single chip such as the ADSP-1010.

Notice that each output is the sum of the products of the five previous inputs and five coefficients. The sixth output Y_6 would then be:

$$Y_6 = X_6 h_0 + X_5 h_1 + X_4 h_2 + X_3 h_3 + X_2 h_4$$

One multiplier can be used sequentially to perform all the multiplications with intermediate products stored in the accumulator. Notice that the maximum frequency response of a 5th order FIR filter, as shown, assuming a multiply/accumulate time of 200ns, would be 0.5MHz (5 mult./accum. × 200ns = 1μs. Since 2 samples/cycle are needed to satisfy Nyquist's sampling theory, a 0.5MHz input is the upper limit for the frequency response). Two techniques can be employed to increase the frequency response. First, several multipliers can be used in a pipeline structure. Second, one can take advantage of the symmetry of the coefficients of a FIR filter. For the fifth order filter this allows one to write the output as

$$Y_n = h_0 [X_{(n)} + X_{(n-4)}] = h_1 [X_{(n-1)} + X_{(n-3)}] + h_2 [X_{(n-2)}]$$

The number of multiplies is halved and the number of accumulates stays the same. Thus with an extra accumulator and some control logic the bandwidth of a FIR filter can be doubled.

Higher order filters, like the 90th order filter discussed above, can also be implemented with a single multiplier/accumulator such as the ADSP-1010. Additional RAM for the input samples $X_{(n-k)}$ and additional ROM for the $h_{(k)}$ would be required. The maximum input frequency that a single MAC could filter in a 90th order structure would be about 25kHz.

Sources of Error

One significant advantage of digital filters is that their performance can be modeled exactly by software. Modeling is necessary to foresee and design around problems that may occur as a result of the finite register lengths in the hardware.

The coefficients $h_{(k)}$ were calculated on a VAX 11/750, which is a 32-bit machine. Since the ADSP-1010 is only a 16-bit device, the coefficients must be rounded or truncated before they are stored in RAM. This rounding or truncation can have undesirable effects on the filter transfer function.

To examine the effect of finite length coefficients on a 90th order filter we rounded the coefficients in Figure 11 to the 16 most significant bits. The filter response was then simulated in a software equivalent of a 16-bit MAC. The results are shown below.

As shown, the ripple in the stopband is increased significantly. This "extra" ripple is undesirable when the attenuation in the stopband using the 16-bit MAC is less than that specified. In this example, the minimum stopband attenuation is −71.25dB whereas the specified attenuation was −80dB. To live with this finite word length problem the designer must overspecify the filter. Some extra performance (1-2dB in this example) can be gained by "tweaking" the coefficients. Several commercially available programs for optimizing the coefficients to get the most attenuation possible for a given filter order considering finite register lengths are available. By rounding, however, the coefficients and resulting filter performance are very close to the theoretical optimum. Truncation, on the other hand, will lead to significantly worse filter performance. Since rounding is not much more difficult that truncation, one should never truncate the filter coefficients.

Roundoff error results from rounding the product of two 16-bit inputs to 16 bits. Fortunately the ADSP-1010 has a 32-bit product bus which minimizes this source of error to the roundoff errors in the LSPs of the products.

Finally, overflow or saturation of the accumulator can occur as a result of sequentially accumulating many products. The ADSP-1010 has three extended product bits in the accumulator to accommodate overflow. For the 90th order filter shown here, the three extra bits were sufficient. However, it is possible to saturate the accumulator. To determine whether overflow will be a problem, it is first necessary to calculate an upper bound for the filter response. A good estimate is the sum of the squares of the filter coefficients. If it appears that the filter will overflow, it must be "tinkered" with to avoid saturation. For low pass filtering, "tinkering" means that multiplications by positive coefficients should be alternated with multiplication by negative coefficients.

It is hoped that the design procedure described above will assist anyone in the design of high-performance FIR filters. As the cost of VLSI decreases even further, designs using FIR filters will become more popular than ever.

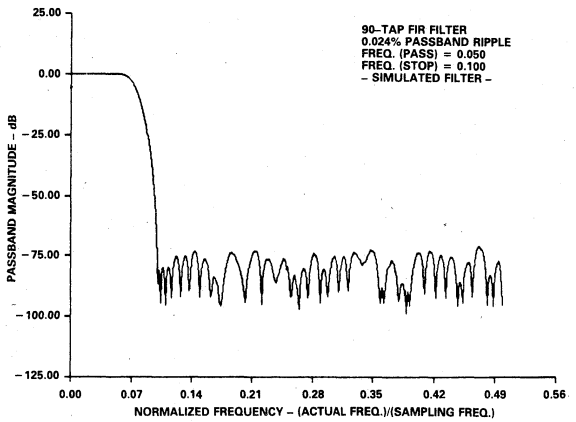


Figure 11. Performance of a 90-Tap Filter with 16-Bit Precision

12

PIN CONFIGURATION FOR PIN GRID ARRAY

PIN	FUNCTION	PIN	FUNCTION
1	Y1, P1	35	P32
2	Y2, P2	36	P33
3	Y3, P3	37	P34
4	Y4, P4	38	CLK P
5	Y5, P5	39	TSM
6	Y6, P6	40	PREL
7	Y7, P7	41	TSX
8	GND	42	TC
9	Y8, P8	43	V_{DD}
10	Y9, P9	44	CLK Y
11	Y10, P10	45	CLK X
12	Y11, P11	46	ACC
13	Y12, P12	47	SUB
14	Y13, P13	48	RND
15	Y14, P14	49	TSL
16	Y15, P15	50	X15
17	N/C	51	N/C
18	P16	52	X14
19	P17	53	X13
20	P18	54	X12
21	P19	55	X11
22	P20	56	X10
23	P21	57	X9
24	P22	58	X8
25	P23	59	X7
26	P24	60	X6
27	P25	61	X5
28	P26	62	X4
29	P27	63	X3
30	P28	64	X2
31	P29	65	X1
32	P30	66	X0
33	P31	67	Y0, P0
34	N/C	68	N/C

PACKAGE G68A

PIN CONFIGURATION FOR DIP AND FLAT PACK

PIN	FUNCTION	PIN	FUNCTION
1	X6	33	P24
2	X5	34	P25
3	X4	35	P26
4	X3	36	P27
5	X2	37	P28
6	X1	38	P29
7	X0	39	P30
8	Y0, P0	40	P31
9	Y1, P1	41	P32
10	Y2, P2	42	P33
11	Y3, P3	43	P34
12	Y4, P4	44	CLK P
13	Y5, P5	45	TSM
14	Y6, P6	46	PREL
15	Y7, P7	47	TSX
16	GND	48	TC
17	Y8, P8	49	V_{DD}
18	Y9, P9	50	CLK Y
19	Y10, P10	51	CLK X
20	Y11, P11	52	ACC
21	Y12, P12	53	SUB
22	Y13, P13	54	RND
23	Y14, P14	55	TSL
24	Y15, P15	56	X15
25	P16	57	X14
26	P17	58	X13
27	P18	59	X12
28	P19	60	X11
29	P20	61	X10
30	P21	62	X9
31	P22	63	X8
32	P23	64	X7

PACKAGE D64A/F64A

PIN CONFIGURATION FOR LCC

PIN	FUNCTION	PIN	FUNCTION
1	X6	35	P24
2	X5	36	P25
3	X4	37	P26
4	X3	38	P27
5	X2	39	P28
6	X1	40	P29
7	X0	41	P30
8	Y0, P0	42	P31
9	N/C	43	N/C
10	Y1, P1	44	P32
11	Y2, P2	45	P33
12	Y3, P3	46	P34
13	Y4, P4	47	CLK P
14	Y5, P5	48	TSM
15	Y6, P6	49	PREL
16	Y7, P7	50	TSX
17	GND	51	TC
18	Y8, P8	52	V_{DD}
19	Y9, P9	53	CLK Y
20	Y10, P10	54	CLK X
21	Y11, P11	55	ACC
22	Y12, P12	56	SUB
23	Y13, P13	57	RND
24	Y14, P14	58	TSL
25	Y15, P15	59	X15
26	N/C	60	N/C
27	P16	61	X14
28	P17	62	X13
29	P18	63	X12
30	P19	64	X11
31	P20	65	X10
32	P21	66	X9
33	P22	67	X8
34	P23	68	X7

PACKAGE E68C

ANALOG DEVICES

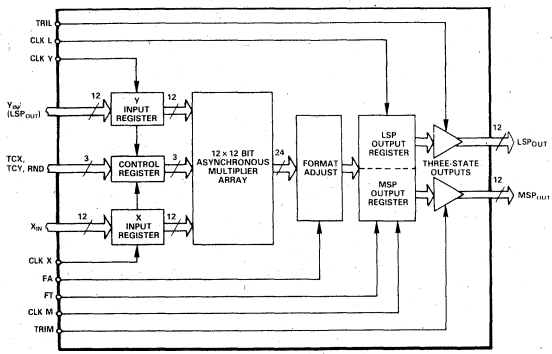
12×12-Bit CMOS Multiplier

ADSP-1012

FEATURES
- 12 × 12 Parallel Array Multiplier
- 150mW max Power Dissipation with CMOS Technology
- 110ns Multiply Time
- Improved MPY-12HJ Second Source
- Two's Complement, Unsigned Magnitude or Mixed Mode Multiplication
- Single +5 Volt Power Supply Operation
- Available in Hermetically Sealed 64-Pin DIP, 68 Terminal LCC, or 68-Pin Grid Array

APPLICATIONS
- Fourier Transformations
- FIR & IIR Digital Filters
- Matrix Multiplications

ADSP-1012 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1012 is a TTL compatible high speed low power 12 × 12-bit multiplier that, in DIP form, is pin for pin compatible with TRW's MPY-12HJ1. The ADSP-1012 has essentially the same speed as the MPY-12HJ but consumes only about 1/20th the power. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus unlike most bipolar and ECL devices it is safe to both specify and operate the ADSP-1012 over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using complementary MOS technology. The high speed is achieved by use of three speed saving techniques. A modified Booth algorithm reduces time consuming operations. Feed-forward carry organization is used. Finally a conditional sum adder speeds the final adder stage.

The ADSP-1012 has two 12-bit input buses and two 12-bit product buses. The inputs can be in either 2's complement, unsigned magnitude or mixed mode formats. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the LSP and MSP product registers. The product registers have three-state outputs which, when combined with the independent control of the input registers, allow the ADSP-1012 to operate on a 12-bit microprocessor bus.

The ADSP-1012 has a RND control which rounds the product to the 12 most significant bits by adding a 1 to the MSB of the LSP. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. It should only be used for 2's complement arithmetic. The FT control makes the output latches transparent.

The ADSP-1012 is available in both commercial and extended temp ranges. Additionally, all versions are available in either a 64-pin hermetically sealed ceramic DIP, 68 terminal LCC, or 68-pin grid array.

PRODUCT HIGHLIGHTS

1. The ADSP-1012, by virtue of fast CMOS technology, provides both low power (150mW) and high speed (110ns) multiplication.
2. The ADSP-1012 provides full pin-for-pin compatibility with the MPY-12HJ1.
3. The ADSP-1012 is also available in a 68 terminal LCC or 68-pin grid array, allowing designers to reduce their system's physical size without worrying about power dissipation and board space problems.

ADSP-1012 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS Parameter		ADSP-1012JX[2] ADSP-1012KX Min	Max	ADSP-1012SX ADSP-1012TX Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

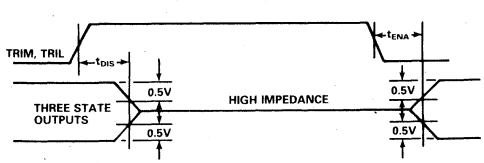
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1012JX ADSP-1012KX Min	Max	ADSP-1012SX ADSP-1012TX Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −0.4mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0		10		10	µA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0		10		10	µA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	µA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	µA
I_{DD}	Supply Current[3]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V; Trim & Tril = 5.0V		400		500	µA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[4,5]

		ADSP-1012JX			ADSP-1012SX			ADSP-1012KX			ADSP-1012TX			Unit
		Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	Min	Max@ 25°C	Max	
t_D	Output Delay		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MUC}	Unclocked Multiply Time		175	205		175	240		145	170		145	195	ns
t_{MC}	Clocked Multiply Time		140	165		140	195		110	130		110	150	ns

NOTES
[1]All min & max specifications have +5.0V power supply and are over specified temperature ranges unless otherwise stated.
[2]When ordering, substitute for X; D for 64-pin DIP, E for 68-terminal leadless chip carriers, or G for 68-pin grid array.
[3]Maximum current is measured with the clock cycle = 9MHz and TTL input voltages.
[4]All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[5]Measured with power supply = 5.0V and TTL voltages of 0.4 and 2.4 volts.
*Specifications same as ADSP-1012JX.
Specifications subject to change without notice.



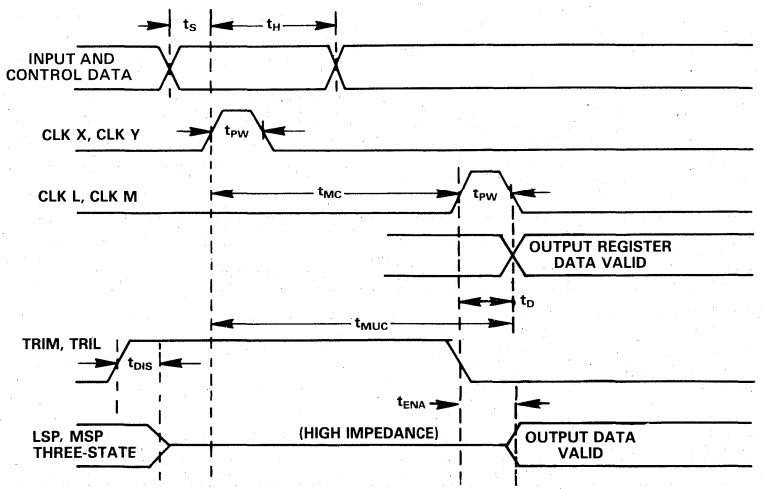
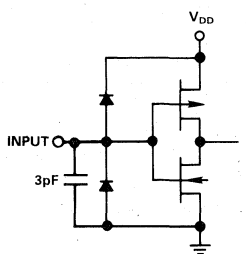
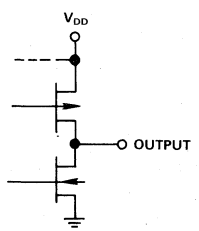


Figure 1. ADSP-1012 Timing Diagram



a. Equivalent Input Circuit



b. Equivalent Output Circuit

Figure 2.

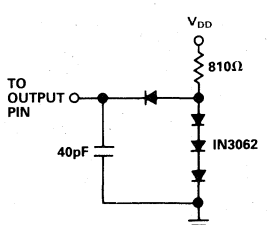


Figure 3. Normal Load Circuit for Delay Measurements

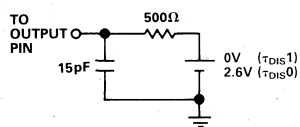


Figure 4. Three-State Delay Load Circuit

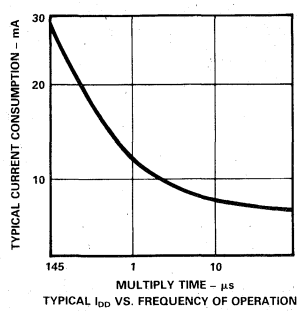


Figure 5. Typical Power Dissipation vs. Frequency

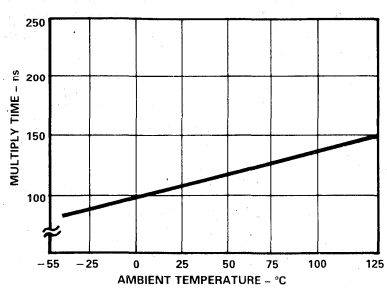


Figure 6. Approx. Multiply Time vs. Temperature

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip flops. The X and Y input data can be either two's complement or unsigned magnitude. A logic 1 on the appropriate TCX or TCY control line is required to signify a two's complement input while a logic 0 is required to signify an unsigned magnitude input.[1]

A logic 1 on the RND line rounds the product to the 12 most significant bits by adding a 1 to the MSB of LSP[3]. TCX, TCY and RND are registered inputs that are loaded by the rising edge of either CLKX or CLKY. 120ns later the product can be loaded into the separately controlled output registers by the rising edge of CLKL and CLKM. The FA control is used to adjust the output format.[2]

The output latches can be bypassed, however, by applying a logic 1 to the feedthrough, FT, line. This does not affect the data that was previously stored in the latches.

The output consists of two words, a 12-bit MSP and a 12-bit LSP. TRIL and TRIM are the three state controls for the LSP and MSP respectively. A logic 1 on TRIL or TRIM causes the appropriate output latch to be in the high impedance state.

X & Y INPUT DATA FORMATS[1]							OUTPUT DATA FORMATS (FA = 1)												
							MSP							LSP					
11	10	9	------	2	1	0	23	22	21	------	14	13	12	11	10	9	------	2	1	0
INTEGER TWO'S COMPLEMENT TCX, TCY = 1																				
SGN (-2^{11})	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}	SGN (-2^{23})	2^{22}	2^{21}	------	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}
FRACTIONAL TWO'S COMPLEMENT TCX, TCY = 1																				
SGN (-2^{0})	2^{-1}	2^{-2}	------	2^{-9}	2^{-10}	2^{-11}	SGN (-2^{-1})	2^{0}	2^{-1}	------	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	------	2^{-20}	2^{-21}	2^{-22}
UNSIGNED MAGNITUDE (INTEGER) TCX, TCY = 0																				
2^{11}	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}	2^{23}	2^{22}	2^{21}	------	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}
							FRACTIONAL TWO'S COMPLEMENT (SHIFTED, FA = 0)[2]													
							SGN (-2^{0})	2^{-1}	2^{-2}	------	2^{-9}	2^{-10}	2^{-11}	SGN (-2^{0})	2^{-12}	2^{-13}	------	2^{-20}	2^{-21}	2^{-22}
							INTEGER TWO'S COMPLEMENT (SHIFTED, FA = 0)[2]													
							SGN (-2^{22})	2^{21}	2^{20}	------	2^{13}	2^{12}	2^{11}	SGN (-2^{22})	2^{10}	2^{9}	------	2^{2}	2^{1}	2^{0}

Table I. Data Formats

NOTES

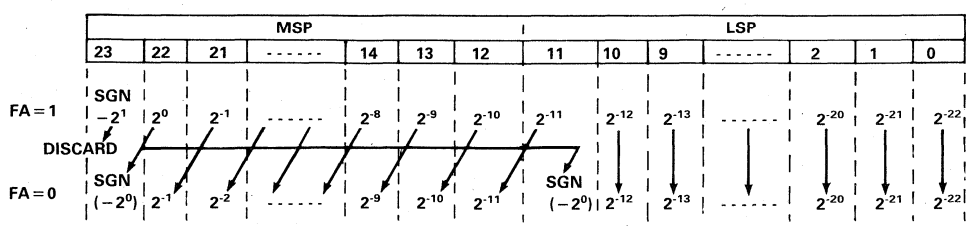
1. As Shown Above Both X and Y Input Data Have the Same Format. For Mixed-Mode Operation, (X and Y Inputs Having Different Formats) the Output Product Format is Determined as Follows:

Y INPUT DATA \ X INPUT DATA	UNSIGNED MAGNITUDE	TWO'S COMPLEMENT
UNSIGNED MAGNITUDE	UNSIGNED MAGNITUDE	TWO'S COMPLEMENT
TWO'S COMPLEMENT	TWO'S COMPLEMENT	TWO'S COMPLEMENT

FA Must Equal 1 to Get a Valid Product for Unsigned Magnitude or Mixed Mode Multiplications. When Performing Mixed-Mode Operations the Sign Bit is Contained in Product Bit 23.

2. The Format Adjust (FA = 0) is Used for the Two's Complement Data Format. The MSP is Left Shifted One Bit and the Sign Bit Duplicated in the MSB of the LSP as Shown Below:

When Using this Format (FA = 0), an Overflow Occurs By Attempting to Multiply 1.000 (−1 Base 10 in Fractional Two's Complement Notation or -2^{11} in Integer Two's Complement Notation) By Itself. The Result is Negative Full Scale Rather than Positive Full Scale. When FA = 0 this Input Condition Should Be Disallowed. If FA = 1, However, the Output Will Always Be Correct.



3. When Using the Round (RND) Control, a One is Added to the MSB of the LSP Regardless of Shift Position. When FA = 0 this is Product Bit Number 10 and when FA = 1 this is Product Bit Number 11.

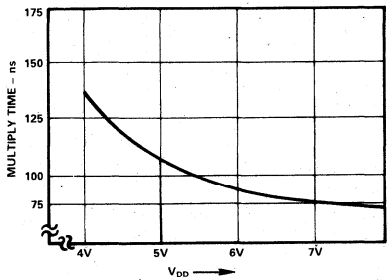


Figure 7. Typical Multiply Time vs. Power Supply

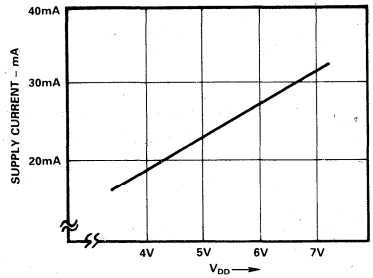


Figure 8. Typical I_{DD} vs. V_{DD} at f=9MHz; t=25°C; CMOS Inputs

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction the speed of the ADSP-1012 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies four parameters will change which in turn will affect the circuit design. These parameters are: input thresholds, output voltage swings, multiplication speed and power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 7 shows, the multiplication speed will increase as the supply voltage increases and decrease as the supply voltages decreases. The change in speed is due to the dependence of transconductance of CMOS devices on supply voltages.

Figure 8 shows that increasing power supply voltage also increases the power consumption of the device. Notice, however, that the worst case power consumption is only 32mA.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage Swing	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

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ORDERING INFORMATION*

Part Number	Temperature Range	Package
ADSP-1012KD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1012JD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1012TD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)
ADSP-1012SD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)

*To obtain a 68-pin grid array, replace the suffix D by G (G68A).
To obtain a 68-terminal leadless chip carrier, replace the suffix D by E (E68C).
See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

24×24 MULTIPLICATION

Often one needs more precision than can be provided by a 12×12-bit multiplication. Figure 9 illustrates four ADSP-1012s being used as a low power double precision multiplier. Here the ADSP-1012's (A, B, C, D) are used in conjunction with five external 12-bit adders (E, F, G, H, J). This configuration yields a full 24-bit product.

Any multiplication can be represented as $(MSB_X + LSB_X) \times (MSB_Y + LSB_Y)$. The product of two equal 24-bit inputs using 4 12-bit multipliers would then be $MSB^2 + 2\,(MSB \cdot LSB) + LSB^2$. Multiplier A and C perform the $LSB_X \cdot LSB_Y$ and the $MSB_Y \cdot LSB_X$ multiplications respectively. Multiplier B performs the $MSB_X \cdot LSB_Y$ multiplication. Finally, multiplier D does the $MSB_X \cdot MSB_Y$ product.

For two's complement multiplications, the rule for handling the mode controls, TCX and TCY, is; whenever the input contains a sign bit, set the mode control to logic "1". Thus the TCX and TCY inputs for multiplier A are both low since sign bits are not carried in the LSBs. Multipliers B and C require a 1, 0 and a 0, 1 respectively for TCX and TCY. Multiplier D has both mode controls set to 1 since both inputs are MSBs containing a sign bit.

The partial products and their carry bits are added as shown in accordance with the requirements for binary multiplication.

For unsigned magnitude multiplication TCX and TCY must equal 0 for all multipliers since no sign information is carried in the inputs. Finally the carry from adder G drives the LSB of adder J. All the remaining 11 bits of that input to adder J are tied low.

This configuration can handle a 24×24-bit multiply in the time it takes to perform 1 12×12-bit multiplication plus the required additions.

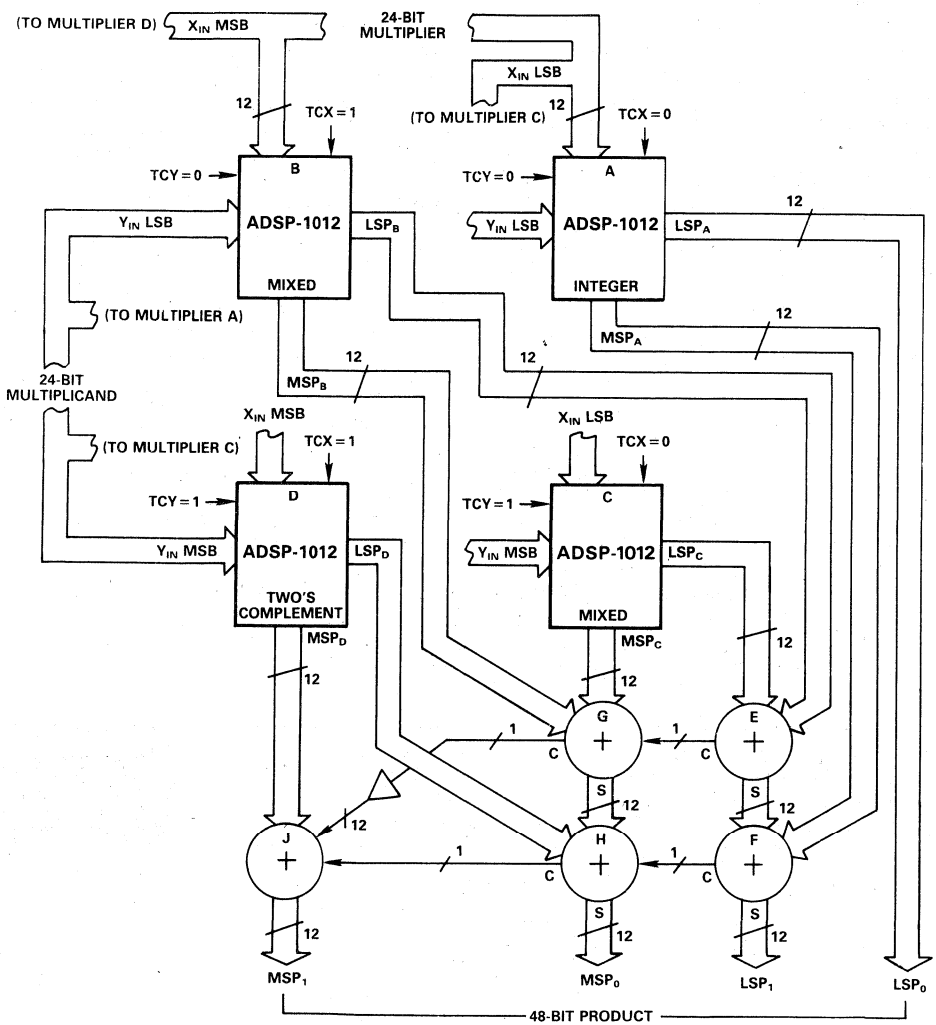


Figure 9. 24×24-Bit Expanded Multiplier Using the ADSP-1012

PIN CONFIGURATION FOR LCC

PIN	FUNCTION	PIN	FUNCTION
1	X7	35	P16
2	X6	36	P17
3	X5	37	P18
4	X4	38	P19
5	X3	39	P20
6	X2	40	P21
7	X1	41	P22
8	X0	42	P23
9	N/C	43	N/C
10	P0	44	TCY
11	P1	45	Y11
12	P2	46	Y10
13	P3	47	Y9
14	P4	48	Y8
15	P5	49	Y7
16	P6	50	Y6
17	P7	51	$+V_{DD}$
18	P8	52	$+V_{DD}$
19	P9	53	$+V_{DD}$
20	P10	54	Y5
21	P11	55	Y4
22	TRIL	56	Y3
23	TRIM	57	Y2
24	GND	58	Y1
25	GND	59	Y0
26	N/C	60	N/C
27	FT	61	TCX
28	FA	62	RND
29	CLK L	63	CLK Y
30	CLK M	64	CLK X
31	P12	65	X11
32	P13	66	X10
33	P14	67	X9
34	P15	68	X8

PACKAGE E68C

PIN CONFIGURATION FOR DIP

PIN	FUNCTION	PIN	FUNCTION
1	X7	33	P16
2	X6	34	P17
3	X5	35	P18
4	X4	36	P19
5	X3	37	P20
6	X2	38	P21
7	X1	39	P22
8	X0	40	P23
9	P0	41	TCY
10	P1	42	Y11
11	P2	43	Y10
12	P3	44	Y9
13	P4	45	Y8
14	P5	46	Y7
15	P6	47	Y6
16	P7	48	$+V_{DD}$
17	P8	49	$+V_{DD}$
18	P9	50	$+V_{DD}$
19	P10	51	Y5
20	P11	52	Y4
21	TRIL	53	Y3
22	TRIM	54	Y2
23	GND	55	Y1
24	GND	56	Y0
25	FT	57	TCX
26	FA	58	RND
27	CLK L	59	CLK Y
28	CLK M	60	CLK X
29	P12	61	X11
30	P13	62	X10
31	P14	63	X9
32	P15	64	X8

PACKAGE D64A

PIN CONFIGURATION FOR PIN GRID ARRAY

PIN	FUNCTION	PIN	FUNCTION
1	P0	35	TCY
2	P1	36	Y11
3	P2	37	Y10
4	P3	38	Y9
5	P4	39	Y8
6	P5	40	Y7
7	P6	41	Y6
8	P7	42	V_{DD}
9	P8	43	V_{DD}
10	P9	44	V_{DD}
11	P10	45	Y5
12	P11	46	Y4
13	TRIL	47	Y3
14	TRIM	48	Y2
15	GND	49	Y1
16	GND	50	Y0
17	N/C	51	N/C
18	FT	52	TCX
19	FA	53	RND
20	CLK L	54	CLK Y
21	CLK M	55	CLK X
22	P12	56	X11
23	P13	57	X10
24	P14	58	X9
25	P15	59	X8
26	P16	60	X7
27	P17	61	X6
28	P18	62	X5
29	P19	63	X4
30	P20	64	X3
31	P21	65	X2
32	P22	66	X1
33	P23	67	X0
34	N/C	68	N/C

PACKAGE G68A

ANALOG DEVICES

16×16-Bit CMOS Multiplier

ADSP-1016

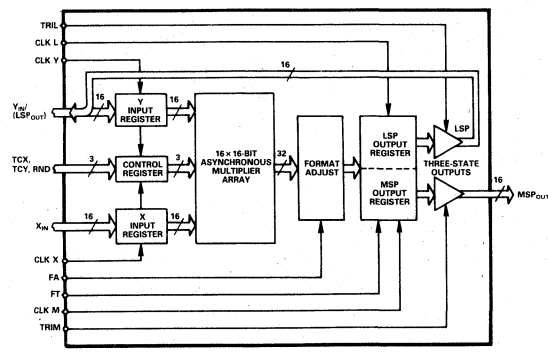
FEATURES

- 16 × 16 Parallel Array Multiplier
- 150mW max Power Dissipation with CMOS Technology
- 145ns Multiply Time
- Improved MPY-16HJ Second Source
- Two's Complement, Unsigned Magnitude or Mixed Mode Multiplication
- Single +5 Volt Power Supply Operation
- Available in Hermetically Sealed 64-Pin DIP, 0.7 Square Inch Flat Pack, 68-Pin Grid Array or 68-Terminal Leadless Chip Carrier
- Specified from −55°C to +125°C Ambient

APPLICATIONS

- Fourier Transformations
- Digital Filtering
- Microprocessor Acceleration
- Matrix Manipulations

ADSP-1016 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1016 is a TTL compatible high-speed low-power 16 × 16-bit multiplier that, in DIP form, is pin for pin compatible with TRW's MPY-16HJ1. The ADSP-1016 has essentially the same speed as the MPY-16HJ but consumes only about 1/20 the power. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus, unlike most equivalent bipolar and ECL devices, it is safe to both specify and operate the ADSP-1016 over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The low power is obtained by using complementary MOS technology. The high speed is achieved by use of three speed saving techniques. A modified Booth algorithm reduces time consuming operations. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage.

The ADSP-1016 has two 16-bit input buses and two 16-bit product buses. The LSP output port is shared with the Y input port. The inputs can be in either 2's complement, unsigned magnitude or mixed mode formats. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the LSP and MSP product registers. The product registers have three-state outputs which, when combined with the independent control of the input registers, allow the ADSP-1016 to operate on a 16-bit microprocessor bus.

The ADSP-1016 has a RND control which rounds the product to the 16 most significant bits by adding a 1 to the MSB of the LSP. The FA control formats the output for 2's complement by shifting the MSP up one bit and then repeating the sign bit in the MSB of the LSP. It should only be used for 2's complement arithmetic. The FT control makes the output latches transparent.

The ADSP-1016 is available in both commercial and extended temp ranges. Additionally, all versions are available in either a 64-pin hermetically sealed ceramic DIP, a 64-pin hermetically sealed flat pack, a 68-pin Grid Array or a 68-terminal Leadless Chip Carrier.

PRODUCT HIGHLIGHTS

1. The ADSP-1016, by virtue of CMOS technology, provides both low power (150mW) and high speed (145ns) multiplication. Full TTL compatibility is supplied without the need for external buffering.
2. The ADSP-1016 provides full pin-for-pin compatibility with the MPY-16HJ1.
3. The ADSP-1016 is also available in a 64-pin flat pack, 68-pin Grid Array or 68-terminal LCC, allowing designers to reduce their system's physical size without worrying about power dissipation and board space problems.

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ADSP-1016 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1016JX[2] ADSP-1016KX Min	Max	ADSP-1016SX ADSP-1016TX Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

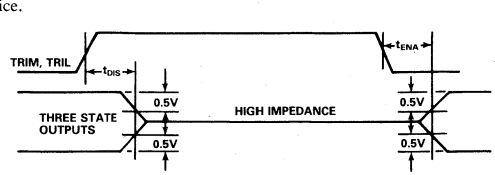
ELECTRICAL CHARACTERISTICS[1]

Parameter		Test Conditions	ADSP-1016JX ADSP-1016KX Min	Max	ADSP-1016SX ADSP-1016TX Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	µA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0V		50		50	µA
I_{DD}	Supply Current[3]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V; TRIM & TRIL = 5.0V		500		2000	µA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[4,5]

		ADSP-1016JX Max@			ADSP-1016SX Max@			ADSP-1016KX Max@			ADSP-1016TX Max@			
		Min	25°C	Max	Min	25°C	Max	Min	25°C	Max	Min	25°C	Max	Unit
t_D	Output Delay		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MUC}	Unclocked Multiply Time		215	260		*	295		180	210		180	245	ns
t_{MC}	Clocked Multiply Time		180	220		*	250		145	170		145	200	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]When ordering, substitute for X: D for 64-pin DIP, E for 68-terminal Leadless Chip Carrier, G for 68-pin Grid Array, or F for 64-pin Flat Pack.
[3]Maximum current is measured with the clock cycle = 6MHz and TTL input voltages.
[4]All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[5]Measured with power supply = +5.0V and TTL voltages of 0.4 and 2.4 volts.
*Specifications same as ADSP-1016JX.
Specifications subject to change without notice.



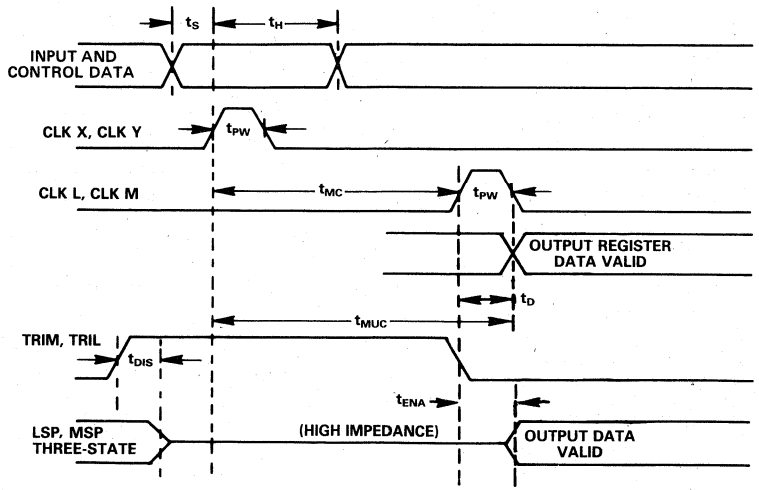
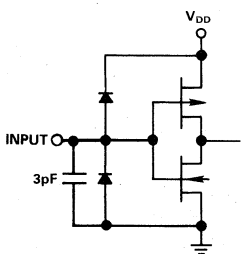
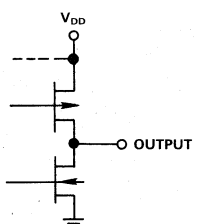


Figure 1. ADSP-1016 Timing Diagram



a. Equivalent Input Circuit



b. Equivalent Output Circuit

Figure 2.

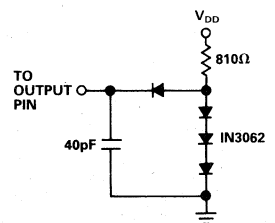


Figure 3. Normal Load Circuit for Delay Measurements

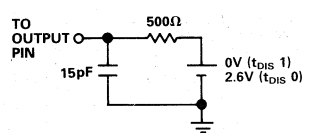


Figure 4. Three-State Delay Load Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage Swing	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION

Part Number*	Temperature Range	Package
ADSP-1016KD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1016JD	0 to +70°C	64-Pin Ceramic DIP (D64A)
ADSP-1016TD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)
ADSP-1016SD	−55°C to +125°C	64-Pin Ceramic DIP (D64A)

*To obtain 64-pin ceramic flat packs, replace the suffix D by F (F64A).
To obtain 68-pin leadless chip carriers, replace the suffix D by E (E68C).
To obtain 68-pin grid arrays, replace the suffix D by G (G68A).
See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

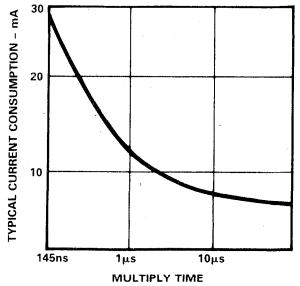


Figure 5. Typical Power Dissipation vs. Frequency

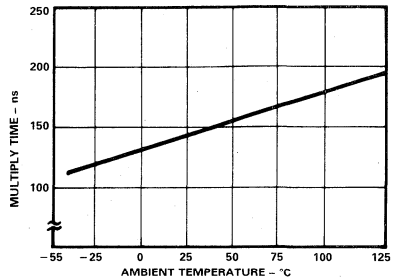


Figure 6. Approx. Multiply Time vs. Temperature

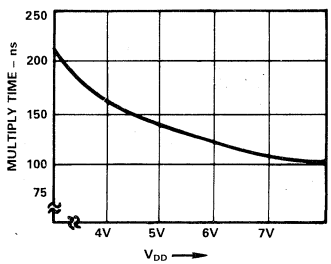


Figure 7. Typical Multiply Time vs. Power Supply

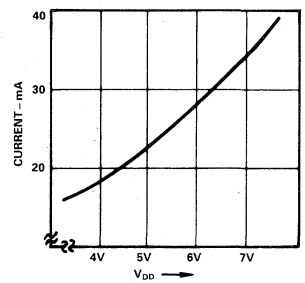


Figure 8. Typical I_{DD} vs. V_{DD} at f=6MHz; t=25°C

X & Y INPUT DATA FORMATS[1]							OUTPUT DATA FORMATS													
							MSP							LSP						
15	14	13	------	2	1	0	31	30	29	------	18	17	16	15	14	13	------	2	1	0
INTEGER TWO'S COMPLEMENT TCX, TCY = 1							(UNSHIFTED FA = 1)[2]													
SGN (-2^{15})	2^{14}	2^{13}	------	2^2	2^1	2^0	SGN (-2^{31})	2^{30}	2^{29}	------	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	------	2^2	2^1	2^0
							(SHIFTED FA = 0)[2]													
							SGN (-2^{30})	2^{29}	2^{28}	------	2^{17}	2^{16}	2^{15}	SGN (-2^{30})	2^{14}	2^{13}	------	2^2	2^1	2^0
FRACTIONAL TWO'S COMPLEMENT TCX, TCY = 1							(UNSHIFTED FA = 1)[2]													
SGN (-2^0)	2^{-1}	2^{-2}	------	2^{-13}	2^{-14}	2^{-15}	SGN (-2^1)	2^0	2^{-1}	------	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	------	2^{-28}	2^{-29}	2^{-30}
							(SHIFTED, FA = 0)[2]													
							SGN (-2^0)	2^{-1}	2^{-2}	------	2^{-13}	2^{-14}	2^{-15}	SGN (-2^0)	2^{-16}	2^{-17}	------	2^{-28}	2^{-29}	2^{-30}
UNSIGNED MAGNITUDE (INTEGER) TCX, TCY = 0							(UNSHIFTED FA = 1)[2]													
2^{15}	2^{14}	2^{13}	------	2^2	2^1	2^0	2^{31}	2^{30}	2^{29}	------	2^{18}	2^{17}	2^{16}	2^{15}	2^{14}	2^{13}	------	2^2	2^1	2^0

Table I. Data Formats

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip flops. The X and Y input data can be either two's complement or unsigned magnitude. A Logic 1 on the appropriate TCX or TCY control line is required to signify a two's complement input while a Logic 0 is required to signify an unsigned magnitude input (see note 1, below).

A Logic 1 on the RND line rounds the product to the 16 most significant bits by adding a 1 to the MSB of LSP (see note 3, below). TCX, TCY and RND are registered inputs that are loaded by the rising edge of the logical OR of CLKX and CLKY. 145ns later the product can be loaded into the separately controlled output registers by the rising edge of CLKL and CLKM. The FA control is used to adjust the output format (see note 2, below).

The output latches can be bypassed, however, by applying a Logic 1 to the feedthrough, FT, line. This does not affect the data that was previously stored in the latches.

The output consists of two words, a 16-bit MSP and a 16-bit LSP. The LSP port is shared with the Y input data port. TRIL and TRIM are the three state controls for the LSP and MSP respectively. A Logic 1 on TRIL or TRIM causes the appropriate output latch to be in the high impedance state. Care must be taken to make sure TRIL is high and the Y input data is settled before clocking the Y input into the Y input register.

NOTES

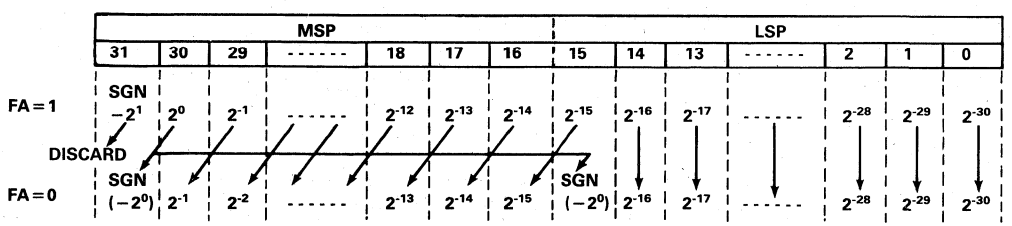
1. **If Both X and Y Inputs are in a Two's Complement Format, then the Output Will Be in a Two's Complement Format. Similarly if Both X and Y are Unsigned Magnitude the Output Will Be Unsigned Magnitude. If X is Unsigned Magnitude and Y Two's Complement or Vice Versa the Output Will Be in a Two's Complement Format. This is Summarized Below.**

Y INPUT DATA \ X INPUT DATA	UNSIGNED MAGNITUDE	TWO'S COMPLEMENT
UNSIGNED MAGNITUDE	UNSIGNED MAGNITUDE	TWO'S COMPLEMENT
TWO'S COMPLEMENT	TWO'S COMPLEMENT	TWO'S COMPLEMENT

FA Must Equal 1 to Get a Valid Product for Unsigned Magnitude or Mixed Mode Multiplications. When Performing Mixed-Mode Operations the Sign Bit is Contained in Product Bit 31.

2. **The Format Adjust (FA = 0) is Used for the Two's Complement Data Format. The MSP is Left Shifted One Bit and the Sign Bit Duplicated in the MSB of the LSP as Shown Below.**

   When Using this Format (FA = 0), an Overflow Occurs By Attempting to Multiply 10 . . . 0 (−1 Base 10 in Fractional Two's Complement Notation or -2^{15} in Integer Two's Complement Notation) By Itself. The Result is Negative Full Scale Rather than Positive Full Scale. When FA = 0 this Input Condition Should Be Disallowed. If FA = 1, However, the Output Will Always Be Correct.



3. **When Using the Round (RND) Control, a One is Added to the MSB of the LSP. When FA = 0 this is Product Bit Number 14 and when FA = 1 this is Product Bit Number 15.**

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction, the speed of the ADSP-1016 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies, four parameters will change which in turn will affect the circuit design. These parameters are: input thresholds; output voltage swings; multiplication speed; and, power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range, the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 7 shows, the multiplication speed will increase as the supply voltage increases and decrease as the supply voltage decreases. The change in speed is due to the dependence of the transconductance of CMOS devices on supply voltages.

Figure 8 shows that increasing power supply voltage also increases the power consumption of the device. Notice, however, that the worst case current consumption is only 33mA with a 7.0V supply.

32 × 32 MULTIPLICATION

Often one needs more precision than can be provided by a 16 × 16-bit multiplication. This situation could occur, for example, when trying to address points on a very high resolution graphics screen. Figure 9 illustrates four ADSP-1016s being used as a low power double precision multiplier. Here the ADSP-1016's (A, B, C, D) are used in conjunction with five external 16-bit adders (E, F, G, H, J). This configuration yields a full 64-bit product.

Any multiplication can be represented as $(MSB_X + LSB_X) \times (MSB_Y + LSB_Y)$. The product of two equal 32-bit inputs using 4 16-bit multipliers would then be $MSB^2 + 2(MSB \cdot LSB) + LSB^2$. Multiplier A and C perform the $LSB_X \cdot LSB_Y$ and the $MSB_Y \cdot LSB_X$ multiplications respectively. Multiplier B performs the $MSB_X \cdot LSB_Y$ multiplication. Finally, multiplier D does the MSB_X MSB_Y product.

For two's complement multiplications, the rule for handling the mode controls, TCX and TCY, is; whenever the input contains a sign bit, set the mode control to logic "1". Thus the TCX and TCY inputs for multiplier A are both low since sign bits are not carried in the LSBs. Multipliers B and C require a 1, 0 and a 0, 1 respectively for TCX and TCY. Multiplier D has both mode controls set to 1 since both inputs are MSBs containing a sign bit.

The partial products and their carry bits are added as shown in accordance with the requirements for binary multiplication.

For unsigned magnitude multiplication TCX and TCY must = 0 for all multipliers since no sign information is carried in the inputs. Finally the carry from adder G drives the LSB of adder J. All the remaining 11 bits of that input to adder J are tied low. This configuration can handle a 32 × 32-bit multiply in the time it takes to perform one 16 × 16-bit multiplication plus the required additions.

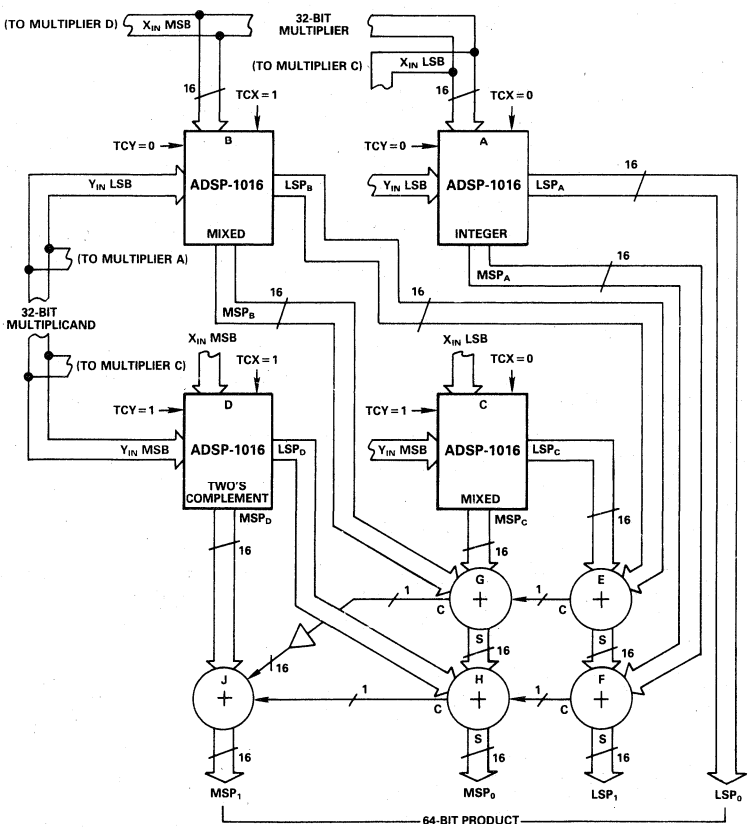


Figure 9. 32×32-Bit Expanded Multiplier Using the ADSP-1016

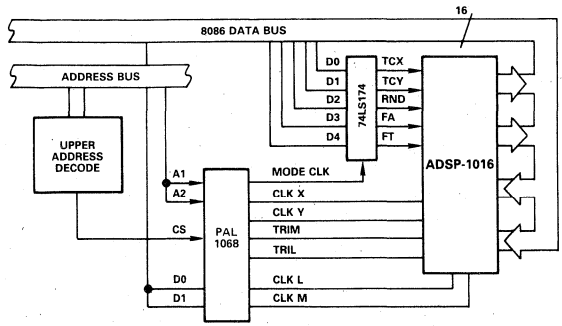
MICROPROCESSOR ACCELERATION

Microprocessors are optimized for manipulating data. In many cases, especially when working with signals or in graphics, a microprocessor may require a dedicated multiplier to augment its number crunching capability. The ADSP-1016 is an easy, low power way to extend the number crunching capabilities of 16-bit microprocessors such as the 8086 or 68000. Following is a note on interfacing the ADSP-1016 to the 8086.

CLK X = $\overline{A_2} \cdot \overline{A_1} \cdot \overline{WR} \cdot CS \cdot \overline{RD}$
CLK Y = $\overline{A_2} \cdot A_1 \cdot \overline{WR} \cdot CS \cdot \overline{RD}$
MODE CLK = $A_2 \cdot A_1 \cdot \overline{WR} \cdot CS \cdot \overline{RD}$
CLK L = $A_2 \cdot A_1 \cdot \overline{WR} \cdot CS \cdot \overline{RD} \cdot D0$
CLK M = $A_2 \cdot A_1 \cdot \overline{WR} \cdot CS \cdot \overline{RD} \cdot D1$
TRIL = $\overline{A_2} \cdot \overline{A_1} \cdot RD \cdot CS \cdot \overline{WR}$
TRIM = $\overline{A_2} \cdot A_1 \cdot RD \cdot CS \cdot \overline{WR}$
NOTE = When Latching Data
D1 or D0 = 1 Latches Product; D1 or D0 = 0 No Latch

PAL Product Terms

CS	A_2	A_1	$\overline{RD}$	$\overline{WR}$	OPERATION
0	X	X	X	X	NO OPERATION
1	0	0	1	0	WRITE X VALUE
1	0	1	1	0	WRITE Y VALUE
1	1	0	1	0	WRITE MODE
1	1	1	1	0	LATCH LSP
1	0	0	0	1	READ LSP
1	0	1	0	1	READ MSP
1	1	1	1	0	LATCH MSP




```
LOAD X          EQU 0          X VALUE DW 123H
LOAD Y          EQU 2          Y VALUE DW 4567H
LOAD MODE       EQU 4          MODE DW OH ; FT, FA, RND, TCY, TCX
LATCH PRODUCT   EQU 6
READ LSP        EQU 0
READ MSP        EQU 2

START   MOV     AX, MODE       ; GET MODE
        OUT     LOAD MODE, AX  ; OUTPUT IT
        MOV     AX, X VALUE
        OUT     LOAD X, AX     ; LOAD X
        MOV     AX, Y VALUE
        OUT     LOAD Y, AX       LOAD Y
        MOV     AX; 03
        OUT     LATCH RESULT, AX ; LATCH MSP AND LSP
        IN      AX, READ MSP   ; GET MS PRODUCT
        MOV     DX, AX
        IN      AX, READ LSP   ; GET LS PRODUCT INTO AX
```

8086 Assembly Language Program for Multiplier

ADSP-1016 PIN CONFIGURATIONS

PIN NO.	FUNCTION DIP	FLAT	LCC	PIN-GRID	PIN NO.	FUNCTION DIP	FLAT	LCC	PIN-GRID
1	X4	X4	X4	P0, Y0	35	P26	P26	P24	CLK M
2	X3	X3	X3	P1, Y1	36	P27	P27	P25	TRIM
3	X2	X2	X2	P2, Y2	37	P28	P28	P26	FA
4	X1	X1	X1	P3, Y3	38	P29	P29	P27	FT
5	X0	X0	X0	P4, Y4	39	P30	P30	P28	GND
6	TRIL	TRIL	TRIL	P5, Y5	40	P31	P31	P29	GND
7	CLK L	CLK L	CLK L	P6, Y6	41	CLK M	CLK M	P30	GND
8	CLK Y	CLK Y	CLK Y	P7, Y7	42	TRIM	TRIM	P31	V_{DD}
9	P0, Y0	P0, Y0	N/C	P8, Y8	43	FA	FA	N/C	V_{DD}
10	P1, Y1	P1, Y1	P0, Y0	P9, Y9	44	FT	FT	CLK M	TCY
11	P2, Y2	P2, Y2	P1, Y1	P10, Y10	45	GND	GND	TRIM	TCX
12	P3, Y3	P3, Y3	P2, Y2	P11, Y11	46	GND	GND	FA	RND
13	P4, Y4	P4, Y4	P3, Y3	P12, Y12	47	GND	GND	FT	CLK X
14	P5, Y5	P5, Y5	P4, Y4	P13, Y13	48	V_{DD}	V_{DD}	GND	X15
15	P6, Y6	P6, Y6	P5, Y5	P14, Y14	49	V_{DD}	V_{DD}	GND	X14
16	P7, Y7	P7, Y7	P6, Y6	P15, Y15	50	TCY	TCY	GND	X13
17	P8, Y8	P8, Y8	P7, Y7	N/C	51	TCX	TCX	V_{DD}	N/C
18	P9, Y9	P9, Y9	P8, Y8	P16	52	RND	RND	V_{DD}	X12
19	P10, Y10	P10, Y10	P9, Y9	P17	53	CLK X	CLK X	TCY	X11
20	P11, Y11	P11, Y11	P10, Y10	P18	54	X15	X15	TCX	X10
21	P12, Y12	P12, Y12	P11, Y11	P19	55	X14	X14	RND	X9
22	P13, Y13	P13, Y13	P12, Y12	P20	56	X13	X13	CLK X	X8
23	P14, Y14	P14, Y14	P13, Y13	P21	57	X12	X12	X15	X7
24	P15, Y15	P15, Y15	P14, Y14	P22	58	X11	X11	X14	X6
25	P16	P16	P15, Y15	P23	59	X10	X10	X13	X5
26	P17	P17	N/C	P24	60	X9	X9	N/C	X4
27	P18	P18	P16	P25	61	X8	X8	X12	X3
28	P19	P19	P17	P26	62	X7	X7	X11	X2
29	P20	P20	P18	P27	63	X6	X6	X10	X1
30	P21	P21	P19	P28	64	X5	X5	X9	X0
31	P22	P22	P20	P29	65	N/A	N/A	X8	TRIL
32	P23	P23	P21	P30	66	N/A	N/A	X7	CLK L
33	P24	P24	P22	P31	67	N/A	N/A	X6	CLK Y
34	P25	P25	P23	N/C	68	N/A	N/A	X5	N/C

PACKAGE D64A – F64A – E68C – G68A

ANALOG DEVICES

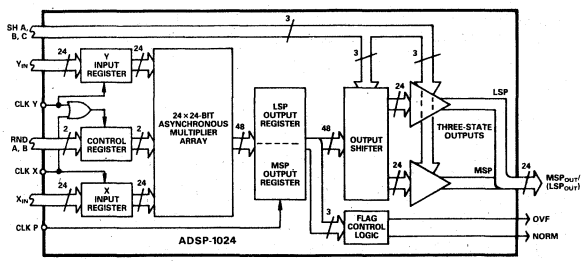
24×24-Bit CMOS Multiplier

ADSP-1024

FEATURES
- 24 × 24-Bit Parallel Array Multiplier
- 150mW max Power Dissipation with Monolithic CMOS Technology
- 200ns Multiply Time
- Two's Complement Format Multiplication
- Single +5 Volt Power Supply Operation
- Available in 84-Pin Grid Array

APPLICATIONS
- Fast Fourier Transforms
- High-Accuracy Digital Filtering
- Matrix Multiplications
- Mantissa Multiply for Floating Point Operations

ADSP-1024 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-1024 is a TTL compatible high-speed low-power 24 × 24-bit multiplier. The ADSP-1024 is a three-port device which has two 24-bit input buses and two 24-bit product buses. The MSP output port is shared with the LSP output port. The inputs are in 2's complement format. All inputs are diode protected. The independent input registers are D-type positive edge triggered flip-flops as are the LSP and MSP product registers. The product registers have three-state outputs which, when combined with the independent control of the input registers, allow the ADSP-1024 to operate on a microprocessor bus.

The ADSP-1024 attains a multiply time of 200ns while dissipating only 150mW, by using complementary MOS technology. Low power dissipation prevents the existence of a large temperature differential between the device's junction temperature and the ambient temperature. Thus the ADSP-1024 will operate over the extended temperature range (−55°C to +125°C ambient) without impairing its useful life.

The high speed multiply time is achieved by use of three speed saving techniques. A modified Booth algorithm reduces time consuming operations. Feed-forward carry organization is used. Finally, a conditional sum adder speeds the final adder stage.

The ADSP-1024 has two round control lines (RND A and RND B) which enable rounding on three different bits in the 48-bit product. The flag lines NORM and OVF tag the two's complement output as already normalized and overflowed, respectively. The product output may also be asynchronously shifted by using the lines SH A, SH B, and SH C, which shift left the 48-bit output by zero, one, or two bits.

The ADSP-1024 is available in both commercial and extended ranges. All versions are available in an 84-lead pin grid array.

12

PRODUCT HIGHLIGHTS

1. The ADSP-1024, by virtue of fast CMOS technology, provides both low power (150mW) and high speed (200ns) multiplication. Full TTL compatibility is supplied without the need for external buffering.
2. The ADSP-1024 is available in an 84-lead pin grid array, allowing designers to reduce their system's physical size without worrying about power dissipation and board space problems.

ADSP-1024 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1024JG ADSP-1024KG Min	ADSP-1024JG ADSP-1024KG Max	ADSP-1024SG ADSP-1024TG Min	ADSP-1024SG ADSP-1024TG Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

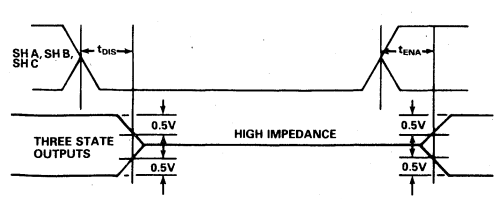
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1024JG ADSP-1024KG Min	ADSP-1024JG ADSP-1024KG Max	ADSP-1024SG ADSP-1024TG Min	ADSP-1024SG ADSP-1024TG Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	µA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0V		50		50	µA
I_{DD}	Supply Current[2]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V; SH A = 0V, SH B = 0V, SH C = 5.0V		500		2000	µA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[3,4]

		ADSP-1024JG Min	ADSP-1024JG Max@ 25°C	ADSP-1024JG Max	ADSP-1024SG Min	ADSP-1024SG Max@ 25°C	ADSP-1024SG Max	ADSP-1024KG Min	ADSP-1024KG Max@ 25°C	ADSP-1024KG Max	ADSP-1024TG Min	ADSP-1024TG Max@ 25°C	ADSP-1024TG Max	Unit
t_D	Output Delay		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	5			*			*			*			ns
t_{MC}	Clocked Multiply Time		235	275		*	325		200	235		200	275	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]Maximum current is measured with the clock cycle = 5MHz and TTL input voltages.
[3]All transitions are measured at a 1.5V level except for t_{ENA} and t_{DIS} which are shown below.
t_{DIS} 1 (see Figure 4) denotes the transition time from logical 1 to tri-state.
t_{DIS} 0 denotes the transition time from logical 0 to tri-state.
[4]Measured with power supply = +5.0V and TTL voltages of 0.4 and 2.4 volts.
*Specifications same as ADSP-1024JG.
Specifications subject to change without notice.



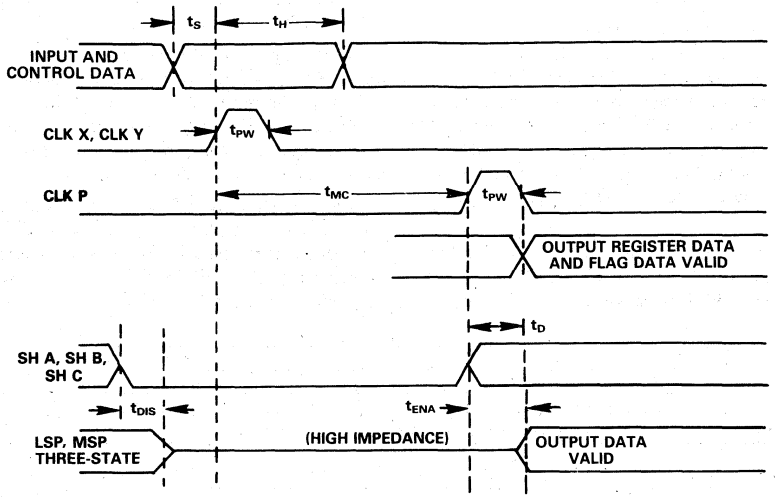
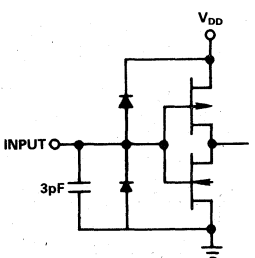
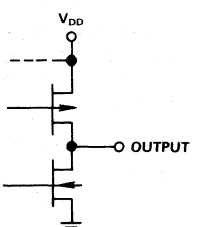


Figure 1. ADSP-1024 Timing Diagram



a. Equivalent Input Circuit



b. Equivalent Output Circuit

Figure 2.

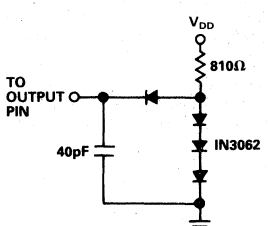


Figure 3. Normal Load Circuit for Delay Measurements

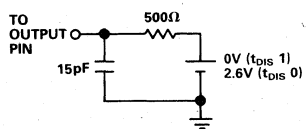


Figure 4. Three-State Delay Load Circuit

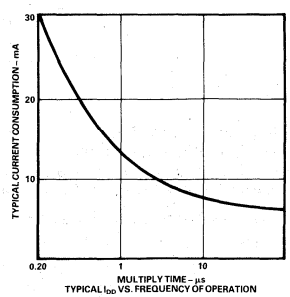


Figure 5. Typical Power Dissipation vs. Frequency

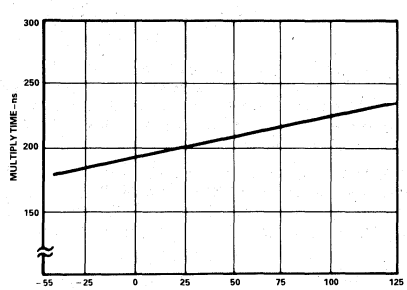


Figure 6. Approx. Worst Case Multiply Time vs. Temperature

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip flops. The X and Y input data must be in two's complement data format.

The output consists of two words, a 24-bit MSP and a 24-bit LSP. The MSP output port is shared with the LSP output port. 200ns after the inputs are clocked in by CLKX or CLKY, the product is loaded into the output registers by the rising edge of CLKP. The output words MSP and LSP may be read out at twice the input data clock rate, so as to keep the input data pipeline rate running at its full 200ns speed. MSP and LSP are read out by enabling the output words with the SH A, B, C control lines.

The lines SH A, SH B, and SH C are the three state and shifting controls for the output lines. A logic 0 on all three lines causes the output latch to be in the high impedance state. The output can also be shifted upward by zero, one, or two bits by using these lines (see notes 2 and 3). These shift lines are direct non-registered inputs (not clocked), and they have no effect on the flag outputs NORM and OVF. The shifting of MSP and LSP bytes may be controlled independently of each other.

Two flags appear at the same time as the output product. NORM flags the two's complement output as already normalized, and OVF flags the two's complement output as overflowed (see notes 4 and 5). The flags are generated from the latched product register, and are valid at the same time as the MSP & LSP output lines become valid.

A logic 1 on RND A or RND B rounds the product by adding a 1 to one of three places (see note 6). RND A and RND B are registered inputs that are loaded by the rising edge of the logical expression (CLKX OR CLKY). Thus positive true logic on the input clocks is recommended.

X & Y INPUT DATA FORMATS	OUTPUT DATA FORMATS	
	MSP	LSP
23 | 22 | 21 | ------ | 2 | 1 | 0	47 | 46 | 45 | ------ | 26 | 25 | 24	23 | 22 | 21 | ------ | 2 | 1 | 0
INTEGER TWO'S COMPLEMENT	NO SHIFT (SH C, B, A = 001 FOR MSP; = 100 FOR LSP)	
SGN (-2^{23}) | 2^{22} | 2^{21} | ------ | 2^{2} | 2^{1} | 2^{0}	SGN (-2^{47}) | 2^{46} | 2^{45} | ------ | 2^{26} | 2^{25} | 2^{24}	2^{23} | 2^{22} | 2^{21} | ------ | 2^{2} | 2^{1} | 2^{0}
	SHIFTED 1 BIT (SH C, B, A = 010 FOR MSP; = 101 FOR LSP)	
	SGN (-2^{46}) | 2^{45} | 2^{44} | ------ | 2^{25} | 2^{24} | 2^{23}	2^{22} | 2^{21} | 2^{20} | ------ | 2^{1} | 2^{0} | 0
	SHIFTED 2 BITS (SH C, B, A, = 011 FOR MSP; = 110 FOR LSP)[3]	
	2^{45} | 2^{44} | 2^{43} | ------ | 2^{24} | 2^{23} | 2^{22}	2^{21} | 2^{20} | 2^{19} | ------ | 2^{0} | 0 | 0
FRACTIONAL TWO'S COMPLEMENT	NO SHIFT (SH C, B, A = 001 FOR MSP; = 100 FOR LSP)	
(-2^{0}) | 2^{-1} | 2^{-2} | ------ | 2^{-21} | 2^{-22} | 2^{-23}	SGN (-2^{1}) | 2^{0} | 2^{-1} | ------ | 2^{-20} | 2^{-21} | 2^{-22}	2^{-23} | 2^{-24} | 2^{-25} | ------ | 2^{-44} | 2^{-45} | 2^{-46}
	SHIFTED 1 BIT (SH C, B, A = 010 FOR MSP; = 101 FOR LSP)	
	SGN (-2^{0}) | 2^{-1} | 2^{-2} | ------ | 2^{-21} | 2^{-22} | 2^{-23}	2^{-24} | 2^{-25} | 2^{-26} | ------ | 2^{-45} | 2^{-46} | 0
	SHIFTED 2 BITS (SH C, B, A = 011 FOR MSP; = 110 FOR LSP)[3]	
	2^{-1} | 2^{-2} | 2^{-3} | ------ | 2^{-22} | 2^{-23} | 2^{-24}	2^{-25} | 2^{-26} | 2^{-27} | ------ | 2^{-46} | 0 | 0

Table I. Data Formats

NOTES TO METHOD OF OPERATION

1. Double-Precision Multiplies are Available on the ADSP-1024, with the Constraint that the Least Significant 24 Bits of Each 48-Bit Double-Precision Operand Must Have a Logic 0 in the Most Significant Bit (Sign Bit). Thus in the Double-Precision Multiply, All Cross-Products will Yield a Product Whose Two MSB's are the Sign Bit (Same Result as for Two's Complement).
2. The Shift Control and Three-State Lines SH A, SH B, and SH C Control the Output Lines as Below:

SH C	SHB	SH A	FUNCTION
0	0	0	Tri-State All Output Lines.
0	0	1	Enable MSP, Shifted up Zero Bits.
0	1	0	Enable MSP, Shifted up One Bit.
0	1	1	Enable MSP, Shifted up Two Bits.
1	0	0	Enable LSP, Shifted up Zero Bit.
1	0	1	Enable LSP, Shifted up One Bit.
1	1	0	Enable LSP, Shifted up Two Bits.
1	1	1	Undefined.

   Note that the MSP and LSP May Be Shifted Independently. When Shifting up the MSP, the Most Significant Bits of the LSP Cross the Boundary and Are Read Out with the MSP; For Example, Shifting up the MSP by 2 Bits will Shift LSP Bit 23 into MSP Bit 25 and LSP Bit 22 into MSP Bit 24. Shifting up the LSP Has No Effect on Any MSP Bits. Note that Because the Shifter is Situated after the Output Register (Note 4), the MSP and LSP can be Read and Shifted Out in Either Order without Losing Any Bits in Either Word.
3. In All Multiply Cases Except Full-Scale Negative Times Full-Scale Negative (−1 Base 10 Times −1 Base 10 in Fractional Two's Complement Arithmetic), the Two MSP Product Bits are Identical Sign Bits. Thus, When Reading Out the MSP, the Output Can Be Shifted up One Bit to Eliminate a Redundant Sign Bit and Gain Another Magnitude Bit from the MSB of the LSP. This is Shown Below for the Different Shifting Options:

   No Shift — Bit 47 = Bit 46 = Sign.
   Shifted 1 Bit — Bit 47 = Sign.
   Shifted 2 Bits — No Sign Bits.

   Because Shifting Up Two Bits Results in the Loss of the Sign Information, Shifting up Two Bits Should Only Be Performed for A Positive Product. When Shifted up Two Bits, the Positive MSP Product Appears in Unsigned Magnitude Format, with 24 Bits of Significance and No Sign Bits.

4. The Flags NORM and OVF Signify Output Normalized and Output Overflowed, Respectively. OVF is Set to 1 Only if P_{47} and P_{46} are Opposite States. NORM is Set to 1 Only if P_{46} and P_{45} are Opposite States AND OVF is Low. The Flag and Shift Logic is Shown Below. Note that Since the Flags are Generated from the Latched Product Register, the Shift Position Will Have No Effect on the States of the Flags.

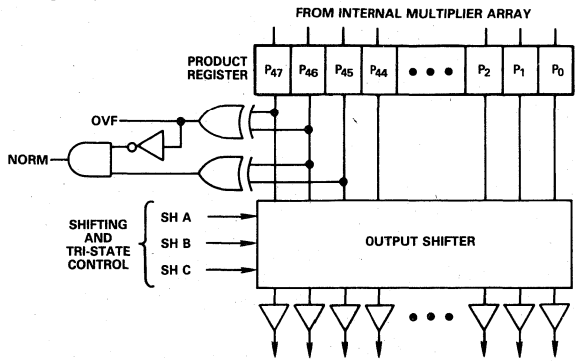


Figure 7. Flag and Shift Logic

Both Positive and Negative Numbers can Trigger Each Flag. Below is Shown the Ranges of Output Values, in Two's Complement Integer Format, Which Trigger OVF and NORM:

OVF	NORM	P_{47}	P_{46}	P_{45}	Range of Product Register (P) Fractional TC Format
0	0	0	0	0	$0 \leq P < +\frac{1}{2}$
		1	1	1	$-\frac{1}{2} \leq P < 0$
0	1	0	0	1	$+\frac{1}{2} \leq P < +1$
		1	1	0	$-1 \leq P < -\frac{1}{2}$
1	0	0	1	1	$+1\frac{1}{2} \leq P < +2$
		1	0	0	$-2 \leq P < -1\frac{1}{2}$
		0	1	0	$+1 \leq P < +1\frac{1}{2}$
		1	0	1	$-1\frac{1}{2} \leq P < -1$
OVF	NORM	P_{47}	P_{46}	P_{45}	Range of Product Register (P) TC Integer Format
0	0	0	0	0	$0 \leq P < +2^{45}$
		1	1	1	$-2^{45} \leq P \leq -1$
0	1	0	0	1	$+2^{45} \leq P < +2^{46}$
		1	1	0	$-2^{46} \leq P < (-2^{46} + 2^{45})$
1	0	0	1	1	$(+2^{46} + 2^{45}) \leq P < +2^{47}$
		1	0	0	$-2^{47} \leq P < (-2^{47} + 2^{45})$
		0	1	0	$+2^{46} \leq P < (+2^{46} + 2^{45})$
		1	0	1	$(-2^{47} + 2^{45}) \leq P < -2^{46}$

5. OVF Signals when the Product of the TC Inputs Overflows the Lower 47 Bits of the Product Register. OVF Will Only Be True in the Case when Both Inputs are Full Scale Negative. In that One Multiply Case, -2^1 Will Be a 0 and 2^0 Will Be a 1 (Denoting a Result of +1), all Other Bits Will Be Zero. The OVF Flag (-2^1 XOR 2^0) Will Be a 1, and the NORM Flag [(2^0 XOR 2^{-1}) AND OVF = 0] Will Be a 0.

   This Usage of OVF is Different from Overflow in an Accumulator. In an Accumulator, Overflow Denotes that the Sum has Exceeded the Number of Bits in the Register. Here, OVF Denotes that the Product has Overflowed the Two's Complement Product Format, Which Normally has Two Sign Bits in Bits 46 and 47 of the Product Register. The Full Scale Negative Times Full Scale Negative Case Yields a Correct Result (Bit 46 = 1), but Now Bit 46 is a Magnitude Bit, Not a Sign Bit.

6. RND A and RND B Round the Product as Below:

RND A	RND B	EFFECT ON TWO'S COMPLEMENT NUMBER
0	0	No Round.
0	1	Adds a 1 to LSP Bit 21.
1	0	Adds a 1 to LSP Bit 22.
1	1	Adds a 1 to LSP Bit 23.

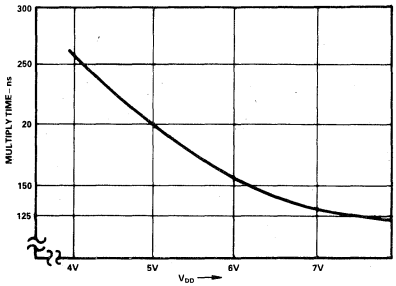


Figure 8. Typical Multiply Time vs. Power Supply

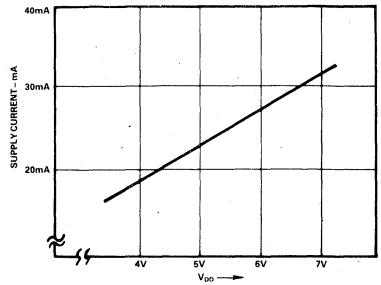


Figure 9. Typical I_{DD} vs. V_{DD} at f=5MHz; t=25°C; CMOS Inputs

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction the speed of the ADSP-1024 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies four parameters will change which in turn will affect the circuit design. These parameters are: input thresholds, output voltage swings, multiplication speed and power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 8 shows, the multiplication speed will increase as the supply voltage increases. The change in speed is due to the dependence of transconductance of CMOS devices on supply voltages.

Figure 9 shows that increasing power supply voltage also increases the power consumption of the device. Notice, however, that the worst case power consumption is only 32mA.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage Swing	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ADSP-1024KG	0 to +70°C	84-Pin Grid Array (G84A)
ADSP-1024JG	0 to +70°C	84-Pin Grid Array (G84A)
ADSP-1024TG	−55°C to +125°C	84-Pin Grid Array (G84A)
ADSP-1024SG	−55°C to +125°C	84-Pin Grid Array (G84A)

Note: For packaging options other than the pin grid array, contact Analog Devices, DSP Marketing Dept.

See Section 19 for package outline information.

32-BIT FLOATING POINT MULTIPLICATION – TWO'S COMPLEMENT

A 32-bit, 250ns floating point multiplier can be implemented using the ADSP-1024. This floating point multiplier achieves low power consumption by using the ADSP-1024 for the mantissa multiply. The floating point operands can be fed to the ADSP-1024 at a pipeline rate of 200ns (the multiply rate of the ADSP-1024); adding the peripheral control circuitry produces a typical input-to-output floating point multiply time of 250ns. The data format is a 24-bit mantissa and an 8-bit exponent.

In the floating point multiplier architecture, the ADSP-1024 performs the mantissa multiply, with the mantissa represented as a two's complement operand. The ADSP-1024, with its output shifter, performs the normalization of the mantissa product. The NORM and OVF flags supply the control lines to the external adders to denormalize the exponent as the mantissa is normalized.

The multiply cycle is divided into two phases by the clock (CLK X, Y, P). In phase I, the rising edge of CLK X, Y, P clocks in a new multiplier and multiplicand to the input latches of the ADSP-1024 and the ML_1 latches. Then, in parallel, the two operands are multiplied in the ADSP-1024 while the exponents are added in the 'LS283 adders.

The rising edge of the following clock cycle marks the beginning of phase II. The rising edge clocks the product into the output register of the ADSP-1024 and into the latches ML_2; simultaneously, new operands are clocked into the input registers of the multiplier and input latches ML_1. The flag outputs NORM and OVF are then used to normalize the mantissa and exponent of the product.

OVF and NORM are used to eliminate the redundant sign bits in the product, preserving maximum precision in the 24-bit mantissa output. IF OVF = 1 and NORM = 0, then we increment the exponent by 1 (because we have overflowed the two's complement format) and shift up the mantissa zero bits (because the product is already normalized in the two's complement input data format). If OVF = 0 and NORM = 1, then we shift up the mantissa one bit (to make it compatible with the two's complement input data format) and leave the exponent alone (we are just formatting the mantissa, but the exponent is already correct). If OVF = 0 and NORM = 0, then we shift up the mantissa two bits (because there are more than two redundant sign bits) and decrement the exponent by 1 (to account for the extra shift in the mantissa).

When the output data from the shifter and ALU have settled (typical propagation delay time 41ns), the normalized product may be read on the product output bus.

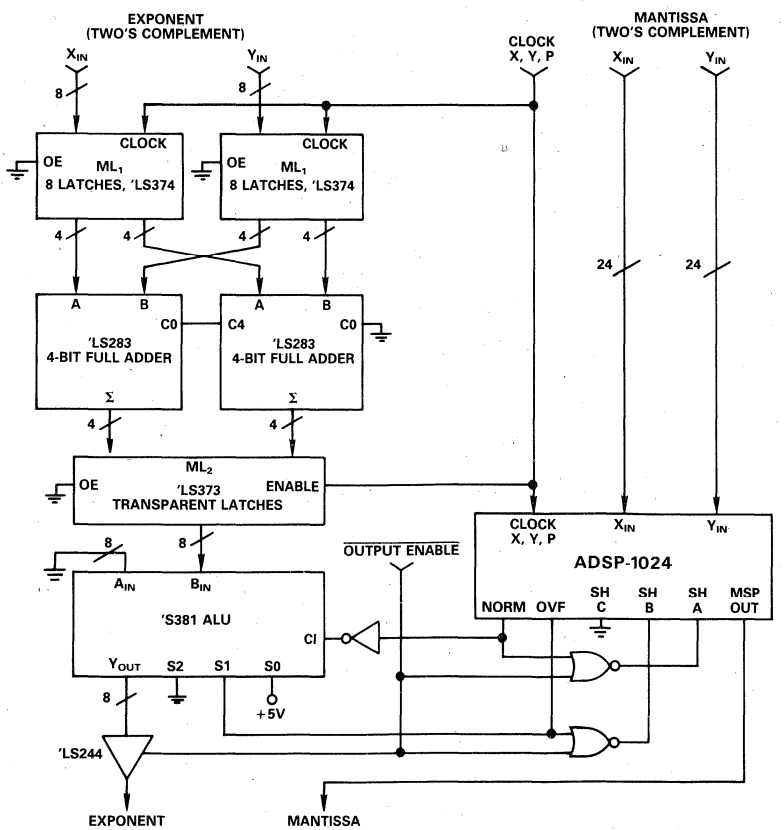


Figure 10. Floating Point Multiplier Circuit

PIN CONFIGURATION FOR
PIN GRID ARRAY

FUNCTION	PIN NO.	FUNCTION	PIN NO.
P16, P40	J6	X20	C6
P15, P39	L6	X21	C7
P14, P38	L5	X22	A7
P13, P37	K5	X23	B7
P12, P36	J5	CLKX	A6
P11, P35	L4	CLKY	A8
P10, P34	K4	RND2	B8
P9, P33	L3	RND1	A9
P8, P32	L2	Y0	A10
P7, P31	K3	Y1	B9
P6, P30	L1	Y2	A11
P5, P29	K2	Y3	B10
P4, P28	J2	Y4	C10
P3, P27	K1	Y5	B11
P2, P26	J1	Y6	C11
P1, P25	H2	Y7	D10
P0, P24	H1	Y8	D11
CTLA	G3	Y9	F10
CTLB	G2	Y10	E10
CTLC	G1	Y11	E11
CLKP	F2	V_{DD}	E9
GND	F3	Y12	F9
X0	E3	Y13	F11
X1	E1	Y14	G11
X2	E2	Y15	G10
X3	F1	Y16	G9
X4	D1	Y17	H11
X5	D2	Y18	H10
X6	C1	Y19	J11
X7	B1	Y20	K11
X8	C2	Y21	J10
X9	A1	Y22	L11
X10	B2	Y23	K10
X11	B3	OVR	K9
X12	A2	NOR	L10
X13	A3	P23, P47	L9
X14	B4	P22, P46	K8
X15	A4	P21, P45	L8
X16	C5	P20, P44	K6
X17	B5	P19, P43	K7
X18	A5	P18, P42	L7
X19	B6	P17, P41	J7

PACKAGE G84A

ANALOG DEVICES

8×8-Bit CMOS Multiplier

ADSP-1080

FEATURES

- **8 × 8-Bit Parallel Multiplication with Double Precision Product**
- **85ns Multiply Time**
- **100mW Power Dissipation with Monolithic CMOS Technology**
- **Two's Complement Data Format**
- **Improved MPY-8HJ Second Source**
- **Single +5 Volt Power Supply Operation**
- **Available in 40-Pin DIP**
- **Specified Over the Extended Temperature Range**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filters**
  - **Fourier Transforms**
- **Digital Image Processing**
- **Matrix Multiplication**
- **Microprocessor Acceleration**

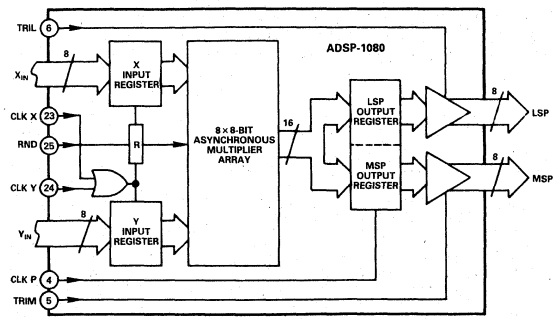
PRODUCT DESCRIPTION

The ADSP-1080 is a TTL compatible high-speed low-power 8 by 8-bit multiplier that is pin-for-pin compatible with TRW's MPY-8HJ. The ADSP-1080 offers 10MHz speed (100ns worst case multiply time over the commercial temperature range), while consuming an order of magnitude less power than the MPY-8HJ. The ADSP-1080 utilizes a two's complement data format for inputs and outputs.

The ADSP-1080's speed derives from several sources: a modified Booth algorithm implements the multiplier array; innovative feed-forward carry organization is used; and, a conditional sum adder accelerates the final adder stage.The ADSP-1080's low power results from its complementary MOS semiconductor technology.

The ADSP-1080 has two 8-bit input buses and two 8-bit product buses. All inputs and outputs are interpreted as two's complement numbers, allowing the ADSP-1080 to operate on positive and negative values. The product of the 8-bit inputs is a 16-bit output word, accessible through the 8-bit LSP (Least Significant Product) and MSP (Most Significant Product) signed product registers.

ADSP-1080 FUNCTIONAL BLOCK DIAGRAM



On the ADSP-1080, the independent input registers, as well as the product registers, are D-type positive edge triggered flip-flops. The product registers have three-state outputs which, when combined with the independent control of the input registers, allow the ADSP-1080 to operate on an 8-bit bus. A round control (RND) can be used to round the product to the eight most significant bits.

The ADSP-1080 is available in a 40-pin ceramic DIP in either military or commercial grades. Two different speed grades (J and K in commercial; S and T in extended) allow the user to make speed and price trade-offs.

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PRODUCT HIGHLIGHTS

1. Fast CMOS technology allows the ADSP-1080 to provide both high speed (85ns) and low power (100mW).
2. The ADSP-1080 is pin-for-pin compatible with the MPY-8HJ.
3. Full TTL compatibility is supplied without the need for external buffering.

ADSP-1080 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1080JD ADSP-1080KD Min	Max	ADSP-1080SD ADSP-1080TD Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

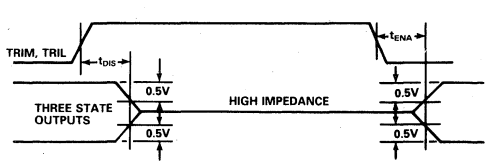
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1080JD ADSP-1080KD Min	Max	ADSP-1080SD ADSP-1080TD Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	μA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	μA
I_{DD}	Supply Current[2]			15		20	mA
I_{DD}	Quiescent	All V_{IN} = 0V; TRIM & TRIL = 5.0V		500		2000	μA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[3,4]

Parameter		ADSP-1080JD Min	Max@ 25°C	Max	ADSP-1080SD Min	Max@ 25°C	Max	ADSP-1080KD Min	Max@ 25°C	Max	ADSP-1080TD Min	Max@ 25°C	Max	Unit
t_D	Output Delay (Figure 5)		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MC}	Clocked Multiply Time		100	115		*	130		85	100		85	115	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]Maximum current is measured with the clock cycle = 10MHz and TTL input voltages.
[3]All transitions are measured at a +1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[4]Measured with power supply at +5.0V and TTL input voltages of 0.4V and 2.4V.
*Specifications same as ADSP-1080JD.
Specifications subject to change without notice.



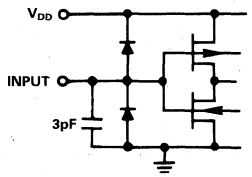


Figure 1. Equivalent Input Circuit

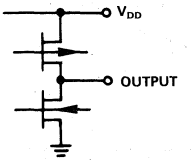


Figure 2. Equivalent Output Circuit

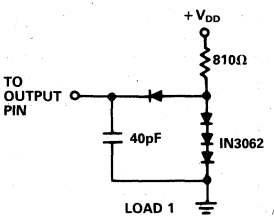


Figure 3. Three-State Disable Delay Load

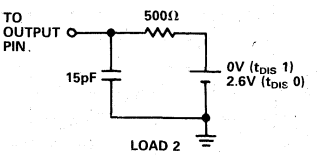


Figure 4. Test Load for Other Delay Measurements

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip-flops. The RND control has a separate register which is loaded by the rising edge of the ORing of the X and Y input clocks. A logic 1 on the RND line rounds the product to the 8 most significant bits by adding a 1 to the MSB of the 7 LSBs.

The output consists of two 8-bit words: a 7-bit plus sign two's complement MSP and a 7 bit LSP. The sign bit is repeated in bit 7 of the LSP. The rising edge of the CLK P latches both the LSP and the MSP into the output flip-flops. TRIL and TRIM are the three state controls for the LSP and MSP respectively. A logic 0 on TRIL or TRIM enables the appropriate output. A logic 1 on TRIL or TRIM causes the appropriate output latch to go to a high impedance state.

An overflow occurs if the fractional two's complement representation of -1 is multiplied by itself; the product is -1 instead of $+1$. To avoid this condition, disallow an input of -1 on the X and Y input simultaneously. Similarly, in integer two's complement multiplication, the product of negative full scale times negative full scale does not yield a valid result.

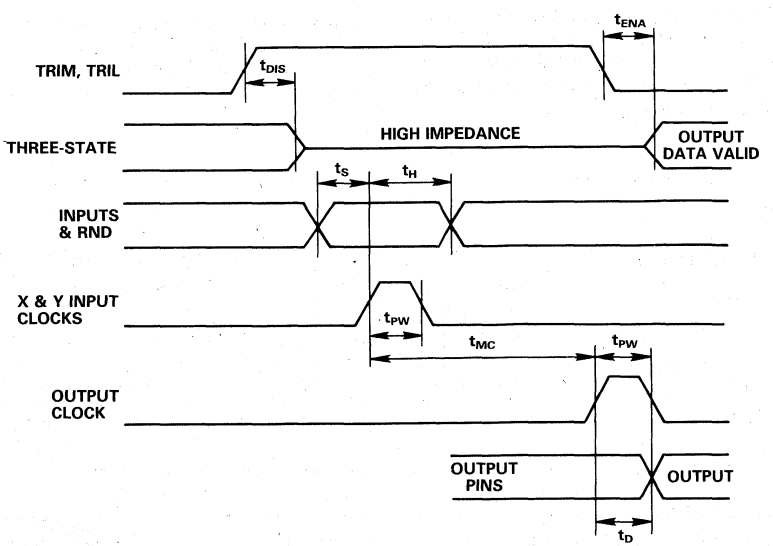


Figure 5. Timing Diagram

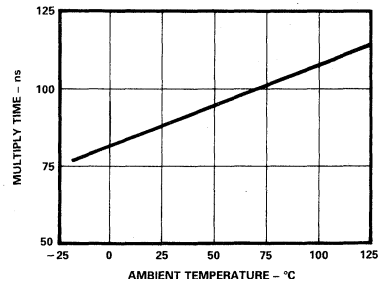


Figure 6. Approximate Worst Case Multiply Time vs. Temperature

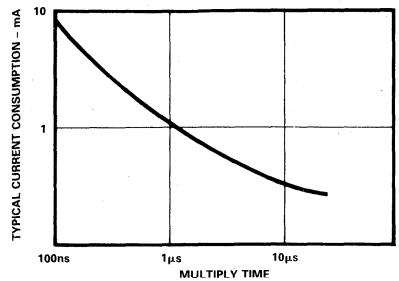


Figure 8. Tyical I_{DD} vs. Frequency of Operation

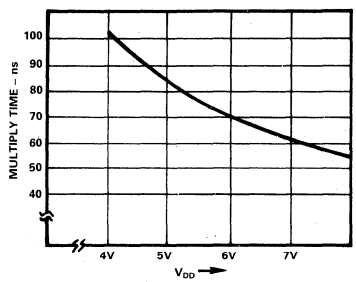


Figure 7. Typical Multiplication Time vs. Power Supply

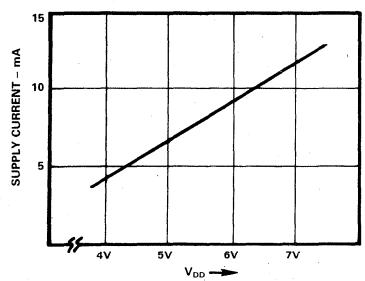


Figure 9. Typical I_{DD} vs. V_{DD} at f=8MHz; ta=25°C; CMOS Inputs

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction, the speed of the ADSP-1080 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies, four parameters will change, which in turn will effect the circuit design. These parameters are: input thresholds; output voltage swings; multiplication speed; and, power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range, the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases the output voltage swing will decrease.

As Figure 7 shows, the multiplication speed will increase as the supply voltage increases. The change in speed is due to the dependence of transconductance of CMOS devices on supply voltages.

Figure 9 shows that increasing power supply voltage also increases the power consumption of the device. However, the worst case power consumption is only 12mA when using a 7V power supply.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7.0V
Input Voltage Range	−0.3V to V_{DD}
Output Voltage	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION

Part Number	Temperature Range	Package
ADSP-1080KD	0 to +70°C	40-Pin Ceramic DIP (D40A)
ADSP-1080JD	0 to +70°C	40-Pin Ceramic DIP (D40A)
ADSP-1080TD	−55°C to +125°C	40-Pin Ceramic DIP (D40A)
ADSP-1080SD	−55°C to +125°C	40-Pin Ceramic DIP (D40A)

Note: For packaging options other than the DIP, contact Analog Devices, DSP Marketing Department.

See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

INPUT DATA FORMAT (X & Y)								OUTPUT DATA FORMATS (P)															
								MSP								LSP							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRACTIONAL TWO'S COMPLEMENT																							
SGN								SGN								SGN							
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	-2^0	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}
INTEGER TWO'S COMPLEMENT																							
SGN								SGN								SGN							
-2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	-2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	-2^{14}	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table I. Data Formats

PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	P10	40	P11
2	P9	39	P12
3	P8	38	P13
4	CLK P	37	P14
5	TRIM	36	P15 (MSB)
6	TRIL	35	Y7 (MSB)
7	P7	34	Y6
8	P6	33	Y5
9	P5	32	GND
10	P4	31	Y4
11	P3	30	V_{DD}
12	P2	29	Y3
13	P1	28	Y2
14	P0	27	Y1
15	X0	26	Y0
16	X1	25	RND
17	X2	24	CLK Y
18	X3	23	CLK X
19	X4	22	X7 (MSB)
20	X5	21	X6

PACKAGE D40A

ANALOG DEVICES

8×8-Bit CMOS Multiplier

ADSP-1081

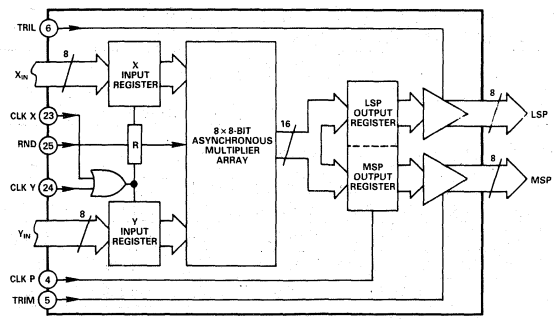
FEATURES

- **8×8-Bit Parallel Multiplication with Double Precision Product**
- **75ns Multiply Time**
- **100mW Power Dissipation with Monolithic CMOS Technology**
- **Unsigned Integer Data Format**
- **Improved MPY-8HUJ Second Source**
- **Single +5 Volt Power Supply Operation**
- **Available in 40-Pin DIP**
- **Specified over the Extended Temperature Range**

APPLICATIONS

- **Digital Signal Processing**
  - **Digital Filters**
  - **Fourier Transforms**
- **Digital Image Processing**
- **Matrix Multiplications**
- **Microprocessor Acceleration**

ADSP-1081 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The ADSP-1081 is a TTL-compatible high-speed low-power 8 by 8-bit multiplier which is pin-for-pin compatible with TRW's MPY-8HUJ. The ADSP-1081 offers sub-100 nanosecond speed (90ns worst case multiply time over the commercial temperature range), while consuming an order of magnitude less power than the MPY-8HUJ. Unlike the ADSP-1080 (an 8×8-bit multiplier with a two's complement data format), the ADSP-1081 uses an unsigned integer data format, providing additional precision.

The ADSP-1081's speed derives from several factors: a modified Booth algorithm, accelerated by a modified Wallace tree structure, is used to implement the multiplier array; innovative feed-forward carry organization is used; and, a conditional sum adder speeds the final adder stage. The ADSP-1081's low power results from its complementary MOS semiconductor technology.

The ADSP-1081 has two 8-bit input buses and two 8-bit product buses. All inputs and outputs are interpreted as unsigned integers, allowing operands and products to be represented with full magnitude precision. The product of the two 8-bit inputs is a full 16-bit word, accessible through the 8-bit LSP (Least Significant Product) and MSP (Most Significant Product) product registers.

On the ADSP-1081, the independent input registers, as well as the product registers, are D-type positive edge triggered flip-flops. The product registers have three-state controls which, when combined with the independent control of the input registers, allow the ADSP-1081 to operate on an 8-bit bus. A round control (RND) can be used to round the product to the eight most significant bits.

The ADSP-1081 is available in a 40-pin ceramic DIP, in either extended or commercial grades. Two different speed grades (J and K in commercial; S and T in extended) allow the user to make speed and price trade-offs.

PRODUCT HIGHLIGHTS

1. Fast CMOS technology allows the ADSP-1081 to provide both high speed (75ns) and low power (100mW).
2. The ADSP-1081 is pin-for-pin compatible with MPY-8HUJ.
3. Full TTL compatibility is supplied without the need for external buffering.

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ADSP-1081 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1081JD ADSP-1081KD Min	Max	ADSP-1081SD ADSP-1081TD Min	Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

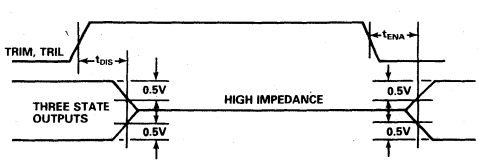
ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1081JD ADSP-1081KD Min	Max	ADSP-1081SD ADSP-1081TD Min	Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.2		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	μA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	μA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	μA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	μA
I_{DD}	Supply Current[2]			15		20	mA
I_{DD}	Quiescent	All V_{IN} = 0V; TRIM & TRIL = 5.0V		500		2000	μA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS[3,4]

Parameter		ADSP-1081JD Min	Max@ 25°C	Max	ADSP-1081SD Min	Max@ 25°C	Max	ADSP-1081KD Min	Max@ 25°C	Max	ADSP-1081TD Min	Max@ 25°C	Max	Unit
t_D	Output Delay (Figure 5)		35	40		*	45		*	*		*	45	ns
t_{ENA}	Three State Enable Delay		25	35		*	40		*	*		*	40	ns
t_{DIS}	Three State Disable Delay		25	35		*	40		*	*		*	40	ns
t_{PW}	Clock Pulse Width	25			*			*			*			ns
t_S	Input Register Setup Time	25			*			*			*			ns
t_H	Input Register Hold Time	0			*			*			*			ns
t_{MC}	Clocked Multiply Time		?	?		*	?		75	90		75	105	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]Maximum current is measured with the clock cycle = 10MHz and TTL input voltages.
[3]All transitions are measured at a +1.5V level except for t_{ENA} and t_{DIS} which are shown below.
[4]Measured with power supply at +5.0V and TTL input voltages of 0.4V and 2.4V.
*Specifications same as ADSP-1081JD.
Specifications subject to change without notice.



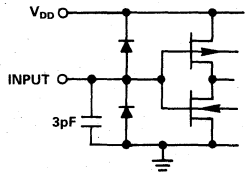


Figure 1. Equivalent Input Circuit

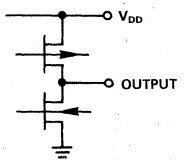


Figure 2. Equivalent Output Circuit

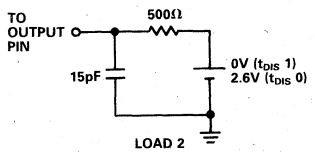


Figure 3. Three-State Disable Delay Load

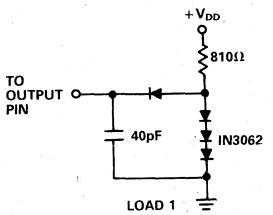


Figure 4. Test Load for Other Delay Measurements

METHOD OF OPERATION

The X and Y input registers are separately controlled positive edge triggered D-type flip-flops. The RND control has a separate register which is loaded by the rising edge of the ORing of the X or Y input clocks. A logic 1 on the RND line rounds the product to the 8 most significant bits by adding a 1 to the MSB of the 8 LSBs.

The output consists of two 8-bit words: the MSP (Most Significant Product) and the LSP (Least Significant Product). The rising edge of the CLK P latches both the LSP and the MSP into the output flip-flops. TRIL and TRIM are the three state controls for the LSP and MSP respectively. A logic 0 on TRIL or TRIM enables the appropriate output. A logic 1 on TRIL or TRIM causes the appropriate output latch to go to a high impedance state.

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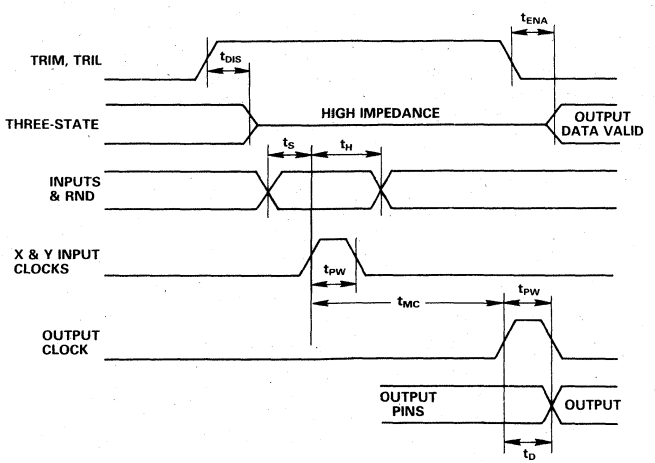


Figure 5. Timing Diagram

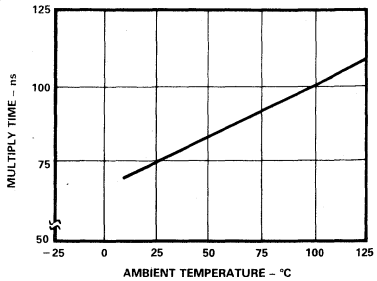


Figure 6. Approximate Worst Case Multiply Time vs. Temperature

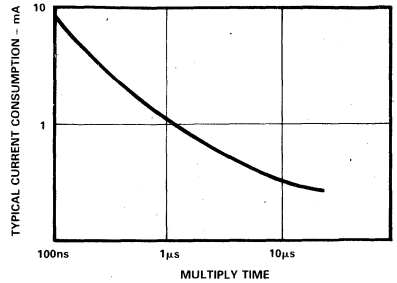


Figure 8. Typical I_{DD} vs. Frequency of Operation

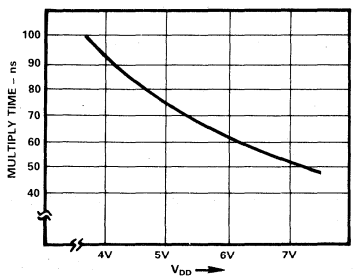


Figure 7. Typical Multiply Time vs. Power Supply

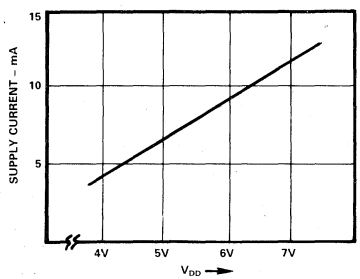


Figure 9. Typical I_{DD} vs. V_{DD} at f=8MHz; t_A=25°C; CMOS Inputs

OPERATIONS WITH NON-TTL SUPPLY VOLTAGES

By virtue of its CMOS construction, the speed of the ADSP-1081 can be increased by the use of a power supply voltage larger than 5.0V. When using non-TTL power supplies, four parameters will change, which in turn will affect the circuit design. These parameters are: input thresholds; output voltage swings; multiplication speed; and, power supply current.

The thresholds of the input inverter stages are selected to meet the TTL specs over the recommended power supply voltages. If the supply voltage is not within the recommended range, the inputs should be driven from 0 volts to the power supply voltage to ensure that the thresholds are crossed.

The output of the multiplier will swing from ground to the supply voltage if no load is applied. As the output loading increases, the output voltage swing will decrease.

As Figure 7 shows, the multiplication speed increases as the supply voltage increases. The change in speed is due to the dependence of transconductance of CMOS devices on supply voltages.

Figure 9 shows that increasing power supply voltage also increases the power consumption of the device. However, the worst case power consumption is only 12mA when using a 7V power supply.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7.0V
Input Voltage Range	−0.3V to V_{DD}
Output Voltage	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION

Part Number	Temperature Range	Package
ADSP-1081KD	0 to +70°C	40-Pin Ceramic DIP (D40A)
ADSP-1081JD	0 to +70°C	40-Pin Ceramic DIP (D40A)
ADSP-1081TD	−55°C to +125°C	40-Pin Ceramic DIP (D40A)
ADSP-1081SD	−55°C to +125°C	40-Pin Ceramic DIP (D40A)

Note: For packaging options other than the DIP, contact Analog Devices, DSP Marketing Department.

See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

APPLICATION NOTE

Unsigned vs.Two's Complement Arithmetic

ADSP multipliers support two different data formats: unsigned magnitude and two's complement. Generally, multipliers (e.g., the ADSP-1016 and ADSP-1012) support both modes, with control pins provided for mode selection. Pin limitations on 8 × 8-bit multipliers, however, dictate that separate devices be dedicated to each data format. The purpose of this note is to examine unsigned magnitude and two's complement formats and, relatedly, the trade-offs between the ADSP-1081 and the ADSP-1080.

Representing Numbers:

Numbers can be represented in a wide variety of formats. Base 10 numbers, for instance, have the following interpretation:

$$d_n d_{n-1} \ldots d_o \bullet f_i \ldots f_m = d_n \times 10^n + \ldots + d_o \times 10^0 + f_1 \times 10^{-1} + \ldots + f_m \times 10^{-m}$$

For digital processing machines, binary representations of numbers are generally used. Such representations allow efficient representation, powerful arithmetic design, and reliable operation. The two most commonly-used binary representations, unsigned and two's complement, are described below.

Unsigned Integer Data Format

An n-bit binary unsigned integer number has the following interpretation:

Bit Number	b_{n-1}	b_{n-2}	. . .	b_0
Unsigned Integer Weight	2^{n-1}	2^{n-2}	. . .	2^0

where b_i is the i^{th} bit of the number and has the value 0 or 1. In base 10, this number is equal to

$$\sum_{i=0}^{n-1} b_i 2^i$$

For example, the number 1011 is equal to $1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 = 8 + 2 + 1 = 11$.

Adding two unsigned integer numbers is straightforward. If we have c = a + b, where c = (c_n, c_{n-1}, . . . , c_0), a = (a_{n-1}, . . . , a_0) and b = (b_{n-1}, . . ., b_0), then $c_i = a_i + b_i + CAR_{i-1}$, where CAR_{i-1} is the carry from the addition performed on the i-1^{st} bit. As an example,

```
  1 0 1 0 1 0
  1 0 0 1 1 1
-------------
1 0 1 0 0 0 1
```

Note that two n-bit numbers, when added, could require n + 1 bits to represent the output. More generally, when m n-bit numbers are added together, (n + $\log_2$(m)) bits are needed to ensure that the result is adequately represented. So, for example, a 35-bit wide accumulator can accumulate just eight adds of 32-bit wide operands without risking overflow. If 256 32-bit words are to be added, the accumulator must be (32 + $\log_2$ 256), or 40, bits wide to ensure that the result won't overflow.

Multiplying binary numbers is structurally similar to the common method used for multiplying base 10 numbers. However, the fact that each binary digit is either a 0 or a 1 allows a multiplication to be reduced to a series of shifts and adds. To see why, consider 11001 × 10101:

```
      1 1 0 0 1
      1 0 1 0 1
      -------
      1 1 0 0 1
    0 0 0 0 0
  1 1 0 0 1
0 0 0 0 0
1 1 0 0 1
-----------
1 0 0 0 0 0 1 1 0 1
```

Another way to implement this operation is to begin with the multiplier 10101 and, wherever a 1 appears, shift the multiplicand the corresponding number of places and add it to the total. In this case, a 1 appears in the 0^{th}, 2^{nd}, and 4^{th} digit of the multiplier term, meaning we add together the multiplicand 11001 three times–once without a shift, once shifted two places to the left, and once shifted four places to the left:

```
      1 1 0 0 1
    1 1 0 0 1
  1 1 0 0 1
-----------
1 0 0 0 0 0 1 1 0 1,
```

yielding the same answer as was previously obtained.

The table below reflects the input and output data formats when multiplying two n-bit unsigned integer operands:

	Input				Output			
Bit Number	b_{n-1}	b_{n-2}	. . .	b_0	P_{2n-1}	P_{2n-2}	. . .	P_0
Unsigned Integer Weight	2^{n-1}	2^{n-2}	. . .	2^0	2^{2n-1}	2^{2n-2}	. . .	2^0

In general, multiplying two n-bit inputs yields a result that requires 2n bits to represent. The numbers spanned by the n-bit input values fall in the range 0 to $2^n - 1$; output values fall in the range 0 to $2^{2n} - 1$.

Finally, it is trivial to interpret unsigned integers as unsigned fractions or mixed numbers. Simple scaling by 2^{-m} shifts the implied binary point from after the Least Significant Bit (LSB) to after the m^{th} bit.

Bit Number	b_{n-1}	b_{n-2}	. . .	b_0
Unsigned Integer Weight	2^{n-1}	2^{n-2}	. . .	2^0
Shifted Unsigned Weight	2^{n-m-1}	2^{n-m-2}	. . .	2^{-m}

In the table above, either interpretation of the binary number b_{n-1} . . . b_0 is valid. Provided binary points are aligned, adds of mixed numbers follow the procedure described earlier. When multiplying unsigned mixed numbers, the location of the binary point can be readily determined from the product of the two scale factors; for example, the product of two n-bit numbers -- one with the binary point after the p^{th} digit and the other after the q^{th} digit -- is a 2n-bit number with the binary point after the $(p + q)^{th}$ digit. Dynamic range can be preserved for blocks of numbers by utilizing a common scaling factor, or exponent; this technique is commonly referred to as block floating point.

Two's Complement Data Format

A general binary two's complement number has the following interpretation:

Bit Number	b_{n-1}	b_{n-2}	. . .	b_0
Integer Two's Complement Weight	-2^{n-1}	2^{n-2}	. . .	2^0
Fractional Two's Complement Weight	-2^0	2^{-1}	. . .	$2^{-(n-1)}$

where b_i is the i^{th} bit of the numbers and has the value 0 or 1. In base 10, the value of an integer two's complement number is

$$-b_{n-1} \times 2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i$$

A fractional two's complement number, in base 10, has the value:

$$-b_{n-1} + \sum_{i=0}^{n-2} b_i 2^{i-(n-1)}$$

For example, in integer two's complement arithmetic, the number 1011 is equal to $-1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 = -5$.

For positive integers, the sign bit, or the Most Significant Bit (MSB), of a two's complement number will always be 0. Therefore, an n-bit two's complement number does no better than an $(n-1)$-bit unsigned integer number in terms of representing positive numbers.

The advantage of two's complement arithmetic is that negative numbers can also be represented. A full scale negative number is 1000 . . . 0, corresponding in integer format to -2^{n-1}; the smallest negative number is 1111 . . . 1, corresponding to -1 in integer two's complement format. An integer two's complement n-bit number, then, spans the range -2^{n-1}, . . . 0, . . ., $2^{n-1}-1$.

While the way negative two's complement numbers are represented may seem cumbersome, it has advantages for additions, logical complements, and subtractions. When adding two's complement numbers, we have $c = a + b$, where $c = (c_{n-1}, \ldots, c_0)$, $a = (a_{n-1}, \ldots, a_0)$, $b = (b_{n-1}, \ldots, b_0)$ and $c_i = a_i + b_i + CAR_{i-1}$. Here, two n-bit numbers are added and the result is limited to an n-bit field. In addition, the carry bit into the sign bit must be compared to the carry bit out of the sign bit; provided they have the same value (both 0 or 1), the carry out of the sign bit is ignored and the n-bit result is valid. If the carry bits into and out of the sign bit differ, the result is invalid because of addition overflow. Examples are provided below.

1011	1110	1001	0111
0010	0110	1010	0111
1101	10100	10011	1110
Valid Negative Result	Valid Positive Result with MSB Ignored	Invalid (overflow)	Invalid (overflow)

Complementing a two's complement number can be accomplished by reversing all bits and adding 1 to the LSB. If we let $\overline{b}_i$ denote the logical negative of b_i, then the complement of $b_{n-1}, \ldots, b_0$ is $\overline{b}_{n-1} \ldots \overline{b}_0 + 1$. For example, 0101 becomes 1010 + 1 = 1011, or in base 10, 5 becomes -5. To subtract b from a, we simply complement b and add it to a. For example, 11101 − 00001 = 11101 + 11111 = 11100, or, in base 10, $-3 - 1 = -4$.

Multiplying two's complement inputs can be understood by decomposing it into its partial products. We define inputs a and b as (a_s, a_w) and (b_s, b_w), where a_s and b_s are the sign bits (given weights -2^{n-1} in integer two's complement form) and a_w and b_w are $(n-1)$-bit least significant words. Then the product c of $a \times b$ is

$$c = a_s b_s \times 2^{2n-2} - (a_s b_w + b_s a_w) \times 2^{n-1} + a_w b_w.$$

In integer two's complement form, all possible products can be represented by a 2n-bit product word of the form:

Product Number	P_{2n-1}	P_{2n-2}	. . .	P_0
Integer Two's Complement Weight	-2^{2n-1}	2^{2n-2}	. . .	2^0
Fractional Two's Complement Weight	-2^1	2^0	. . .	$2^{-(2n-2)}$

This representation is provided by industry standard multiplier/accumulators (such as the ADSP-1010, the ADSP-1009, and the ADSP-1008). For industry standard 16×16-bit and 12×12-bit multipliers (such as the ADSP-1016 and ADSP-1012), this format is provided when the format adjust control is asserted.

With the above output representation, the two most significant bits are redundant for all but one special case (negative full scale $\times$ negative full scale). As can be easily demonstrated, all other combinations of positive and negative inputs will result in a product whose two MSB's are identical. Redundancy in the two MSB's is a serious limitation in many applications, since it effectively restricts the precision of the Most Significant Word (MSW) of the output to 14 bits of magnitude.

Another limitation of the above output format is that, with a fractional two's complement representation, the MSW of the output does not have the same format as the inputs ($-2^1\,2^0 \ldots 2^{n-2}$ *versus* $-2^0 2^{-1} \ldots 2^{n-1}$). This discrepancy means that outputs must be scaled down to preserve consistency in the data.

Since the two MSB's in a two's complement representation are generally redundant, and since eliminating one of these bits makes inputs and outputs consistent for fractional two's complement arithmetic, an alternative representational scheme may be preferable for many applications:

Product Bit	P_{2n-2}	P_{2n-3}	. . .	P_0
Integer Two's Complement Weight	-2^{2n-2}	2^{2n-3}	. . .	2^0
Fractional Two's Complement Weight	-2^0	2^{-1}	. . .	$2^{-(2n-2)}$

which requires just 2n–1 bits to represent the product of two n-bit two's complement inputs. Many DSP multipliers utilize this format (16×16-bit multipliers and 12×12-bit multipliers, such as the ADSP-1016 and ADSP-1012, with the format adjust low, and 8×8-bit multipliers, such as the ADSP-1080). The spare bit that is available is inserted in the MSB of the Least Significant Word (LSW), where the sign bit is repeated. The only restriction placed on this output format is that negative full scale x negative full scale does not provide a meaningful product.

Frequently in DSP, an n-bit number is to be moved to, or added to, the contents of a wider field. For instance, we may want to add a 32-bit product to a 35-bit accumulator. With an unsigned representation, effecting this operation is trivial. With a two's complement representation, implementing this operation can be accomplished with the aid of sign-extend logic.

The basic idea behind embedding an n-bit two's complement number into a larger field is to right justify the n-bit number and extend the sign bit into the MSB's of the wider field. For instance, if we want to represent the four bit number $b_3b_2b_1b_0$ in an eight-bit field, the proper representation is $b_3b_3b_3b_3b_3b_2b_1b_0$. For positive two's complement numbers, this sign extension results in filling in the MSB's with 0's, obviously preserving the value of the initial number. For negative two's complement numbers, we fill in the MSB's with 1's. To see why such a maneuver doesn't affect the value of the number, recall that $2^m + 2^{m-1} + \ldots + 2^0 = 2^{m+1} - 1$. In the case of a sign extend of two's complement negative numbers, we have changed $-2^{n-1} + b_w$ into $-2^{n+m-1} + 2^{n+m-2} + \ldots + 2^n + 2^{n-1} + b_w$. However, $2^{n+m-2} + 2^{n+m-3} + \ldots + 2^{n-1} = 2^{n+m-1} - 2^{n-1}$, so the representations are equivalent.

Finally, the implied binary point of two's complement numbers can be positioned anywhere in the word, provided the scaling factor is tracked. It may be necessary to shift numbers to maintain consistency with the location of the binary point. When downshifting negative two's complement numbers, the sign bit (which is shifted down) must be sign extended into the MSB's. When upshifting a two's complement number, the vacated LSB's are filled with zeroes. As an example, suppose the 4-bit two's complement integers 1100 and 0110 are to be downshifted (to prevent overflow on subsequent operations). The numbers would be downshifted to 1110 and 0011, and the implied binary point would be shifted up. Consequently, the shifted numbers are interpreted using the following weights: $(-2^4, 2^3, 2^2, 2^1)$. To verify equality, we check that 1100 unshifted is the base 10 number -4; in its new representation, it has the same value $(-16 + 8 + 4)$.

Conclusion

The preceding discussion allows the relative trade-offs in using unsigned magnitude versus two's complement arithmetic, or more specifically, the ADSP-1081 vs the ADSP-1080, to be summarized.

Clearly, if an application requires that a mixture of positive and negative numbers be multiplied together, two's complement multiplication is essential. However, if all products are obtained by multiplying pairs of numbers of the same sign, an unsigned magnitude multiplier offers distinct advantages. In this case, the magnitude of inputs has an extra bit of dynamic range using unsigned magnitude arithmetic. Also, with unsigned arithmetic, the magnitude of the product has an extra bit of dynamic range. To see why, consider unsigned inputs of n-1 bits. If we add an extra bit to the two multiplier inputs and use it to double the magnitude of these inputs, we quadruple the range of the output products. In contrast, if the additional bit is used to represent the sign of each input, the output range is only doubled -- since its magnitude range stays constant, with the sign of the output positive or negative. This difference in range is consistent with the fact that outputs in two's complement multiplication require one less bit to represent than outputs for unsigned magnitude multiplication.

Finally, in some applications, a multiplier may be used as a barrel shifter, since multiplying by 0 . . . 010 . . . 0, where the 1 is in the m^{th} bit, is equivalent to shifting the multiplicand up (to the left) by m bits. Then, by reading either the MSW or LSW of the product register, the barrel-shifted result can be obtained. In some cases, it may be desirable to shift an n-bit word into the upper n bits of a 2n-bit result register. Multiplying in two's complement mode cannot accomplish this shift, since the n-bit number 10 . . . 0 is a full scale negative. To perform the required shift, a full scale positive input must be used in unsigned integer format.

X & Y INPUT DATA FORMAT								OUTPUT DATA FORMATS																	
								MSP								LSP									
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
UNSIGNED FRACTIONAL																									
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}
UNSIGNED INTEGER																									
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Table I. Data Formats for the ADSP-1081

PIN CONFIGURATION

PIN	FUNCTION	PIN	FUNCTION
1	P10	40	P11
2	P9	39	P12
3	P8	38	P13
4	CLK P	37	P14
5	TRIM	36	P15 (MSB)
6	TRIL	35	Y7 (MSB)
7	P7	34	Y6
8	P6	33	Y5
9	P5	32	GND
10	P4	31	Y4
11	P3	30	V_{DD}
12	P2	29	Y3
13	P1	28	Y2
14	P0	27	Y1
15	X0	26	Y0
16	X1	25	RND
17	X2	24	CLK Y
18	X3	23	CLK X
19	X4	22	X7 (MSB)
20	X5	21	X6

PACKAGE D40A

ANALOG DEVICES

16×16-Bit CMOS Single Port Multiplier/Accumulator

ADSP-1110

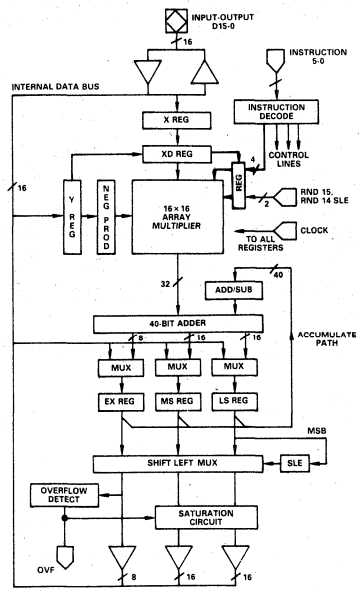
FEATURES

16 × 16-Bit Parallel Multiplication/Accumulation
28-Pin Ceramic DIP or Plastic Package
150mW Power Dissipation with CMOS Technology
200ns Multiply/Accumulate Time
40-Bit Wide Accumulator with Overflow Flag, Saturation Arithmetic, and Shift-Left Control
Two's Complement or Unsigned Magnitude Inputs
Specified Over the Full MIL Temperature Range

APPLICATIONS

Digital Filtering
Fast Fourier Transforms
Double-Precision Operations
Matrix Multiplication
Microprocessor Acceleration

ADSP-1110 FUNCTIONAL BLOCK DIAGRAM



GENERAL INFORMATION

The ADSP-1110 is a high-speed, low-power single-port 16 × 16-bit multiplier/accumulator (MAC), with processing throughput comparable to existing three-port MAC's. Its single-bus structure offers unique advantages: more compact packaging in a 28-pin DIP; simpler system interface to single-bus peripherals; and, significantly reduced cost. In addition, innovative on-chip features extend the ADSP-1110's capabilities and eliminate external hardware.

All inputs to and outputs from the ADSP-1110 pass through its single 16-bit I/O port. All I/O operations are single cycle. A multiply or MAC operation requires two cycles to complete—consistent with the two cycles required to load input pairs to the multiplier. An internal pipeline register enables a new input to be loaded as the previous multiply/accumulate is computed—allowing the device's full 5MHz computational bandwidth to be utilized.

A six-bit microcode instruction word governs the ADSP-1110's operation. The instruction set centers around I/O and multiply/accumulate operations. Additional instructions allow extra precision in single and double precision operations to be obtained efficiently.

Multiplier products are accumulated in a 40-bit wide Multiplier Result (MR) register. Multiplier inputs can be either two's complement or unsigned magnitude numbers. Overflow from the lower 32 bits of the MR into the upper eight guard bits is detected and can be monitored externally. Outputs can, conditional upon overflow status, be saturated to full scale. An MR register can be shifted left by one bit upon output; two independent round controls allow rounding consistent with output formatting.

The ADSP-1110 is optimal for applications where board space is limited but the performance of a DSP processor is required. In addition, a microprocessor-based system can realize greater throughput by utilizing the ADSP-1110 as an accelerator.

12

ADSP-1110 SPECIFICATIONS[1]

RECOMMENDED OPERATING CONDITIONS

Parameter		ADSP-1110JX[2] ADSP-1110KX Min	ADSP-1110JX[2] ADSP-1110KX Max	ADSP-1110SX ADSP-1110TX Min	ADSP-1110SX ADSP-1110TX Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	4.5	5.5	V
T_{AMB}	Operating Temperature ($T_{AMBIENT}$)	0	70	−55	125	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	ADSP-1110JX ADSP-1110KX Min	ADSP-1110JX ADSP-1110KX Max	ADSP-1110SX ADSP-1110TX Min	ADSP-1110SX ADSP-1110TX Max	Unit
V_{IH}	High-Level Input Voltage	@ V_{DD} = max	2.0		2.0		V
V_{IL}	Low-Level Input Voltage	@ V_{DD} = min		0.8		0.8	V
V_{OH}	High-Level Output Voltage	@ V_{DD} = min & I_{OH} = −1.0mA	2.4		2.4		V
V_{OL}	Low-Level Output Voltage	@ V_{DD} = min & I_{OL} = 4.0mA		0.4		0.6	V
I_{IH}	High-Level Input Current	@ V_{DD} = max & V_{IN} = 5.0V		10		10	µA
I_{IL}	Low-Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{IH}	Clocks, Control Inputs High Level Input Current	@ V_{DD} = max & V_{IN} = 5V		10		10	µA
I_{IL}	Clocks, Control Inputs Low Level Input Current	@ V_{DD} = max & V_{IN} = 0V		10		10	µA
I_{OZH}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = max		50		50	µA
I_{OZL}	Three State Leakage Current	@ V_{DD} = max; High Z; V_{IN} = 0		50		50	µA
I_{DD}	Supply Current[3]			25		30	mA
I_{DD}	Quiescent	All V_{IN} = 0V = 5.0V		500		2000	µA
I_{DD}	Quiescent	All V_{IN} = 2.4V		15		20	mA

SWITCHING CHARACTERISTICS

		ADSP-1110JX Min	ADSP-1110JX Max@ 25°C	ADSP-1110JX Max	ADSP-1110SX Min	ADSP-1110SX Max@ 25°C	ADSP-1110SX Max	ADSP-1110KX Min	ADSP-1110KX Max@ 25°C	ADSP-1110KX Max	ADSP-1110TX Min	ADSP-1110TX Max@ 25°C	ADSP-1110TX Max	Unit
t_{PW}	Clock Pulse Width	15			*			*			*			ns
t_{DS}	Data to Clock Setup Time	20			*			*			*			ns
t_{CS}	Control Inputs to Clock Setup	30			*			*			*			ns
t_{CH}	Input Control Hold Time	0			*			*			*			ns
t_{DH}	Input Data Hold Time	0			*			*			*			ns
t_{MAC}	Multiply/Accumulate Time		200	240		180	250		165	190		165	220	ns
t_D	Control to Bus Delay		55	60		*	65		*	*		*	65	ns
t_{DS}	Control to Bus Delay with Saturation		60	65		*	70		*	*		*	70	ns
t_{DLS}	Control to Bus Delay w/SL and Saturation		60	65		*	70		*	*		*	70	ns
t_O	Clock to Overflow		30			*			*			*		ns
t_{LO}	Output W/SL to Valid Overflow		60	65		*	70		*	*		*	70	ns

NOTES
[1]All min & max specifications are over power supply and temperature range indicated (unless otherwise stated).
[2]When ordering substitute for X: D for 28-pin ceramic DIP, N for 28-pin plastic
[3]Maximum current is measured with the clock cycle = 10MHz and TTL input voltages.
*Specifications same as ADSP-1110JX.
Specifications subject to change without notice.

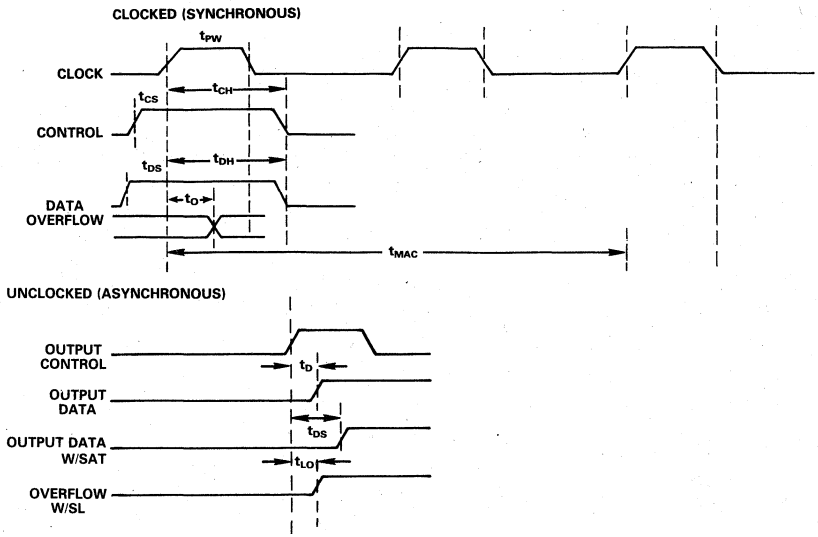


Figure 1. ADSP1110 Timing Diagram

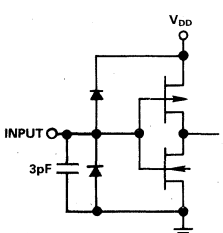


Figure 2a. Equivalent Input Circuits

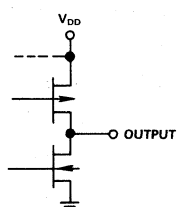


Figure 2b. Equivalent Output Circuits

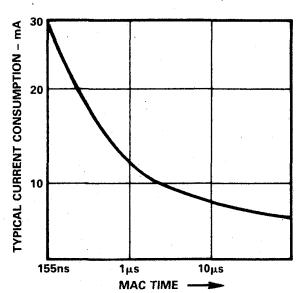


Figure 4. Typical Power Dissipation vs. Frequency

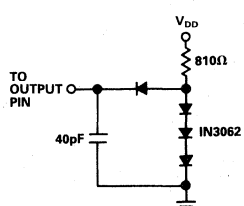


Figure 3. Normal Load Circuit for Delay Measurements

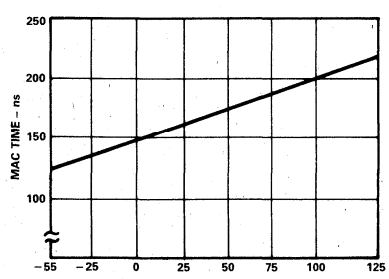


Figure 5. Typical Multiply Time vs. Temperature

METHOD OF OPERATION

The ADSP-1110's operation is controlled by a six-bit microcode instruction and two rounding control pins. Table I presents the 32 instructions that are executed by the ADSP-1110, along with the corresponding six-bit microcode instruction. Table II describes the mnemonics that are used in Table I's instruction set. The sections below further describe the instruction groups presented in Table I.

A dedicated *input instruction* loads the X input; this instruction executes in one cycle. An extensive set of *multi-operation instructions* load the Y input and otherwise control the ADSP-1110's multiplier/accumulator. Specifically, a multi-operation instruction i) loads Y; ii) specifies which multiply or MAC instruction is executed; and iii) clocks the result of the previous multiply or MAC into the MR register. Executing a multi-operation instruction requires two cycles.

During the first cycle of a multi-operation instruction, the X input is transferred to an internal pipeline register (XD), allowing a new X value to be loaded onto the chip during the second cycle. The register XD will not be overwritten until a new X value is loaded. Consequently, if a stream of data is to be scaled by a constant, the constant need only be loaded once into X.

Instruction	Microcode Instruction 5 4 3 2 1 0	Operation
NOP	0 0 0 0 x x	
CKMR	0 0 0 1 x x	Clock MR
X = BUS	0 0 1 0 x x	Input
BUS = EX	0 0 1 1 0 1	Output
BUS = EX (SL)	0 0 1 1 0 0	
BUS = MS	0 1 1 0 0 1	
BUS = MS (SL)	0 1 1 0 0 0	
BUS = MS (SAT)	0 0 1 1 1 1	
	0 1 1 0 1 1	
BUS = MS (SL,SAT)	0 1 1 0 1 0	
	0 0 1 1 1 0	
BUS = LS	0 1 1 1 0 1	
BUS = LS (SL)	0 1 1 1 0 0	
BUS = LS (SAT)	0 1 1 1 1 1	
BUS = LS (SL,SAT)	0 1 1 1 1 0	
LS = BUS	0 1 0 0 0 0	Preload
MS = BUS	0 1 0 1 x 0	
EX = BUS	0 1 0 0 1 0	
LS = MS	0 1 0 0 0 1	Shift
MS = EX	0 1 0 1 0 1	
EX = SIGN EXT MS	0 1 0 0 1 1	Sign Extend
MS = SIGN EXT LS	0 1 0 1 1 1	
Y = BUS; X_{US}*Y_{US}; CKMR	1 0 0 x 0 0	Multi-operation
Y = BUS; $-(X_{US}$*$Y_{US})$; CKMR	1 0 0 x 0 1	
Y = BUS; X_{US}*Y_{US} + MR; CKMR	1 0 0 0 1 0	
Y = BUS; $-(X_{US}$*$Y_{US})$ + MR; CKMR	1 0 0 0 1 1	
Y = BUS; $(X_{US}$*$Y_{US})$ − MR; CKMR	1 0 0 1 1 0	
Y = BUS; $-(X_{US}$*$Y_{US})$ − MR; CKMR	1 0 0 1 1 1	
Y = BUS; X_{TC}*Y_{US}; CKMR	1 0 1 x 0 0	
Y = BUS; $-(X_{TC}$*$Y_{US})$; CKMR	1 0 1 x 0 1	
Y = BUS; X_{TC}*Y_{US} + MR; CKMR	1 0 1 0 1 0	
Y = BUS; $-(X_{TC}$*$Y_{US})$ + MR; CKMR	1 0 1 0 1 1	
Y = BUS; X_{TC}*Y_{US} − MR; CKMR	1 0 1 1 1 0	
Y = BUS; = $-(X_{TC}$*$Y_{US})$ − MR; CKMR	1 0 1 1 1 1	
Y = BUS; X_{US}*Y_{TC}; CKMR	1 1 0 x 0 0	
Y = BUS; $-(X_{US}$*$Y_{TC})$; CKMR	1 1 0 x 0 1	
Y = BUS; X_{US}*Y_{TC} + MR; CKMR	1 1 0 0 1 0	
Y = BUS; $-(X_{US}$*$Y_{TC})$ + MR; CKMR	1 1 0 0 1 1	
Y = BUS; $(X_{US}$*$Y_{TC})$ − MR; CKMR	1 1 0 1 1 0	
Y = BUS; $-(X_{US}$*$Y_{TC})$ − MR; CKMR	1 1 0 1 1 1	
Y = BUS; X_{TC}*Y_{TC}; CKMR	1 1 1 x 0 0	
Y = BUS; $-(X_{TC}$*$Y_{TC})$; CKMR	1 1 1 x 0 1	
Y = BUS; X_{TC}*Y_{TC} + MR; CKMR	1 1 1 0 1 0	
Y = BUS; $-(X_{TC}$*$Y_{TC})$ + MR; CKMR	1 1 1 0 1 1	
Y = BUS; X_{TC}*Y_{TC} − MR; CKMR	1 1 1 1 1 0	
Y = BUS; $-(X_{TC}$*$Y_{TC})$ − MR; CKMR	1 1 1 1 1 1	

Table I. ADSP-1110 Instruction Set

Mnemonic	Description
=	Assign right side to left.
BUS	16-bit external data bus used for all I/O operations.
X	Input register for multiplier.
Y	Input register for multiplier.
EX	8-bit extension register for accumulator.
MS	16-bit most significant product register.
LS	16-bit least significant product register.
MR	40-bit accumulator comprising EX, MS and LS.
SL	Shift left.
SAT	Conditional on overflow, saturate the outputted value.
TC	Two's complement number.
US	Unsigned magnitude number.
SIGN	Sign bit (MSB) of specified register.
CKMR	Clock product into EX, MS, and LS.
x	Microcode instruction bit can be either a 0 or 1.

Table II. Summary of Mnemonics for ADSP-1110 Instruction Set

The ADSP-1110's multiply and multiply/accumulate operations consist of the following:

$$\pm X*Y$$

and,

$$\pm X*Y \pm MR$$

The ADSP-1110 allows inputs to be specified as two's complement or unsigned magnitude numbers. Table III describes, for all combinations of inputs, the proper interpretation of the MR register if it is output with or without the left shift option.

On the ADSP-1110, the result of a multiply or MAC operation is not latched into the MR register until the MR is explicitly clocked. A dedicated "CKMR" instruction performs this clocking. In addition, all multi-operation instructions clock the MR in parallel with other operations, eliminating overhead when computing MAC's (see *Instruction Sequences*). It is important to note that whenever "CKMR" is executed, it clocks the result of the *previous* multiply into the MR. For example, when the multi-operation instruction "Y = BUS; X*Y + MR; CKMR" is executed, the "CKMR" operation clocks the result of the preceding—not the current—MAC into the MR.

A number of the ADSP-1110's instructions affect the contents of the MR register—including *preload instructions*, *transfer instructions*, and *sign extend instructions*. In addition, this device's output instructions provide options for format adjusting the MR upon output.

The accumulator in the ADSP-1110 is 40 bits wide, segmented into three registers: a 16-bit most significant product register (MS); a 16-bit least significant product register (LS); and, an 8-bit extended product register (EX) (see Table III). The eight additional significant bits in EX allow up to 256 multiply/accumulates without risk of overflow.

Preloading the MR's three registers requires one cycle each. The proper sequence for preloading a value Z into MR and adding/subtracting it from the product $X_1 * Y_1$ is:

Instruction	Comment
1. X = BUS	Load X_1
2. Y = BUS; X*Y + MR; CKMR	Load Y_1, initiate MAC, clock garbage into MR
3. LS = BUS	Preload MR with Z
4. MS = BUS	Preload MR with Z
5. EX = BUS	Preload MR with Z
6. X = BUS	Load X_2
7. X*Y ± MR; Y = BUS; CKMR	MR = X_1*Y_1 + Z, initiate next multiply.

This sequence ensures that the value Z preloaded in cycles 3, 4, and 5 is added to the product of X_1 and Y_1 and, at the start of cycle 7, clocked into MR. If Z were preloaded prior to the first multiply, the "CKMR" operation would overwrite the Z value with whatever values were last placed in the multiplier array.

	MR			
INPUTS (X & Y)	**EX (8 BITS)**	**MS (16 BITS)**	**LS (16 BITS)**	
b_{15} | b_{14} | ------ | b_0	b_{39} | b_{38} | ------ | b_{32}	b_{31} | b_{30} | ------ | b_{16}	b_{15} | ------ | b_1	b_0
TWO'S COMPLEMENT INTEGER	(W/O SL)			
-2^{15} | 2^{14} | ------ | 2^0	-2^{39} | 2^{38} | ------ | 2^{32}	2^{31} | ------ | 2^{16}	2^{15} | ------ | 2^1	2^0
	(W/ SL) -2^{38} | 2^{37} | ------ | 2^{31}	2^{30} | ------ | 2^{15}	2^{14} | ------ | 2^0	0
TWO'S COMPLEMENT FRACTIONAL	(W/O SL)			
-2^0 | 2^{-1} | ------ | 2^{-15}	-2^9 | 2^8 | ------ | 2^2	2^1 | 2^0 | ------ | 2^{-14}	2^{-15} | ------ | 2^{-29}	2^{-30}
	(W/ SL) -2^8 | 2^7 | ------ | 2^1	2^0 | 2^{-1} | ------ | 2^{-15}	2^{-16} | ------ | 2^{-30}	0
UNSIGNED MAGNITUDE INTEGER				
2^{15} | ------ | 2^0	2^{39} | ------ | 2^{32}	2^{31} | ------ | 2^{16}	2^{15} | ------ | 2^1	2^0
UNSIGNED MAGNITUDE FRACTIONAL				
2^{-1} | ------ | 2^{-16}	2^7 | ------ | 2^0	2^{-1} | ------ | 2^{-16}	2^{-17} | ------ | 2^{-31}	2^{-32}
MIXED MODE INTEGER				
-2^{15} | 2^{14} | ------ | 2^0 & 2^{15} | 2^{14} | ------ | 2^0	-2^{39} | 2^{38} | ------ | 2^{32}	2^{31} | ------ | 2^{16}	2^{15} | ------ | 2^1	2^0
MIXED MODE FRACTIONAL				
-2^0 | 2^{-1} | ------ | 2^{-15} & 2^{-1} | 2^{-2} | ------ | 2^{-16}	-2^8 | 2^7 | ------ | 2^1	2^0 | ------ | 2^{-15}	2^{-16} | ------ | 2^{-30}	2^{-31}

Table III. ADSP-1110 Data Formats

At the beginning of a chain of multiply/accumulates, preloading MR can be avoided by first executing a multiply (overwriting previous contents of the accumulator) and then multiply/accumulate instructions on following cycles.

Transfer operations allow one MR register to be moved down to an adjacent one—useful in double-precision operations. The ADSP-1110 can, in one cycle, shift the EX to the MS or the MS to the LS register.

Anytime the result of a multiply or multiply/accumulate operation is clocked into the accumulator, the result is automatically sign extended into the upper MSB's of the accumulator. In addition, explicit instructions allow the MSB of the LS to be sign extended to the MS ("MS = SIGN EXT LS") or the MSB of the MS to be sign extended to the EX register ("EX = SIGN EXT MS"). This instruction is useful if the MS or LS of the MR is preloaded, or after an MR register transfer.

Output instructions allow any of the three registers comprising the MR register to be read in a single cycle. When written onto the ADSP-1110's 16-bit bus, the 8-bit EX register is automatically sign extended into the upper 8 MSB's. Standard output instructions of the ADSP-1110 are supplemented with two important options: a left shift capability and conditional saturation.

The ADSP-1110's output instructions include the ability to shift any MR register (EX, MS, or LS) left by one bit upon output. This shift does not affect the contents of MR, but does affect what appears on the ADSP-1110's 16-bit I/O port. Figure 6 shows which bits of the 40-bit wide MR register are output if the shift left option is invoked.

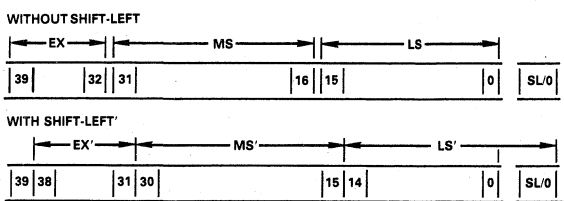


Figure 6. Accumulator register maps illustrating left-shift effects

The shift-left-on-output control, which scales up the MR register outputs by a factor of two, is useful under many circumstances. For example, two's complement multiplication results—for all but one case (negative full scale times negative full-scale)—in redundancy in the two MSB's of the 32-bit product. This redundancy means that the 16-bit MS register contains two identical sign bits (bits 31 and 30 of MR) and just 14 bits of magnitude. The ADSP-1110's shift-left control allows full precision in two's complement operations to be attained. Left shift control also provides a means for maximizing resolution when using block floating point, when downscaling two's complement results, and when upscaling mixed and unsigned magnitude results.

The shift left extend register, SL, is a one-bit latch that is loaded with the value of the MSB of the LS register whenever the MS is transferred to LS. The SL register retains its value until the next downshift of MS into LS overwrites its contents. Whenever the RND14/SLE pin is asserted during a "BUS = LS (SL)" or "BUS = LS (SL, SAT)" instruction, the SL bit will be appended to the upper 15 bits of the shifted LS. If the RND14/SLE is low, however, a zero will be inserted into the LSB of LS. Appending the SL bit to the shifted LS provides an extra bit of precision in applications such as double precision multiply/accumulates.

The RND14/SLE and RND15 pins are two independent controls that allow rounding consistent with whether the shifted or unshifted output option is used. The round control signals are latched at the beginning of only those cycles during which the device receives a multiply or MAC instruction. Asserting the RND15 (RND14/SLE) pin will cause a 1 to be added to Bit 15 (Bit 14) of the LS. The rounding will not occur until the subsequent cycle in which the result of the multiply or MAC operation is clocked into the MR. The RND14/SLE control can be used to ensure that a left-shifted MS (Bits 30 through 15) is rounded in the proper location.

The ADSP-1110's overflow flag monitors 9 bits (8 in the EX register and the 1 MSB of the MS register). If any bits in EX differ from the MSB of MS then an overflow has occurred from the MS into the EX, and the overflow flag is asserted (logic level one). Generally, the status of the overflow flag reflects the current contents of the MR and is updated each time a new result is clocked into the MR. However, if the MS register is output with a left-shift, the overflow logic determines whether the shifted MS overflows into the EX (when Bits 38 through 31 are identical) and is set accordingly. On the cycle following any left-shifted output, the overflow flag status reverts to reflect the contents of the MR.

Serious glitches can result from wraparound effects due to overflow in long multiply/accumulate chains. For example, if a positive number is added to positive full-scale, the 32 MSB's of the MR register will overflow into the 8-bit EX register. Simply reading the MS register may yield a negative two's complement number. To prevent this wraparound, the ADSP-1110 can—conditioned on overflow status—saturate an output to full scale.

The ADSP-1110's saturation logic operates only on output values; it has no effect on the contents of the MR register. This logic examines the sign of the MR (Bit 39, the MSB of the EX register) and the overflow status. As Table IV indicates, the low 32 bits of the MR are saturated to full scale positive (negative) if overflow has occurred in a positive (negative) MR.

Either the MS or LS registers can be left-shifted on output with conditional saturation. If the shifted value overflows the lower 32 bits, the outputted result will be saturated to full scale.

While the saturation control protects against overflow from the MS to the EX register, the user is not protected in the event the accumulated result overflows the entire 40-bit MR register.

OVF	MR BIT 39 (SIGN BIT)	Output Value with Saturation MS	LS
0	0	← No Change →	
0	1	← No Change →	
1	0	0111111111111111	1111111111111111
1	1	1000000000000000	0000000000000000

Table IV. Overflow and Saturation Circuitry Conditions

Clock and Timing

Figure 1 presents a timing diagram for the ADSP-1110. Control inputs consist of the six-bit wide microcode instruction and the two rounding control pins. The system clock for the ADSP-1110 operates at 10MHz, defining a basic cycle time of 100ns.

Microcode instructions are fetched from the microprogram store, decoded and used immediately for input and output control. On a CKMR and on a multiply instruction, the array controls are latched and used on the following two cycles to control the array (see ADSP-1110 Functional Block Diagram).

The ADSP-1110's instruction set contains two types of instructions: unclocked (all output instructions) and clocked (all other instructions).

For unclocked output instructions, the relevant timing specification is the delay between control inputs and valid outputs on the bus. The use of saturation and shift left with saturation controls slows down the availability of a valid output on the ADSP-1110's I/O bus; delay times are specified accordingly.

For clocked operations, the appropriate setup, hold, and clock-to-clock delays are specified. Specifications pertain to both control inputs (instructions and control pins) and data inputs.

The ADSP-1110's OVF flag is set according to the contents of the MR register. However, upon outputting the MR with the shift left control, the OVF flag may be modified if the left shift results in overflow. The relevant timing for this case is specified.

Instruction Sequences

All ADSP-1110 instructions are single cycle with the exception of a multiply/accumulate, which requires two cycles to complete. The sequencing of operations for three commonly-used instruction sequences is discussed below.

A single multiply operation involves three overhead statements in addition to the multiply command. The basic instruction sequence used is: "X = BUS" (load X value into X input register), "Y = BUS; MR = X*Y; CKMR" (load Y, multiply and clock MR), "NOP" (because a multiply requires two cycles), "CKMR" (clock MR), and "BUS = MS" (place MS register contents onto bus).

While a multiply/accumulate sequence operates in a manner similar to a single multiply, overhead as a percentage of multiply time is reduced substantially. In the instruction flow diagram shown in Table V, a NOP is needed only in the final multiply/accumulate operation. Also, new X values are loaded as multiply/accumulate instructions complete. In this sequence, the three cycles of overhead can be spread out over a large number of multiply/accumulates.

For a series of multiply/accumulate sequences, I/O operations can be further overlapped. At the end of each multiply/accumulate string, a new string is initiated. In this instance, the three overhead cycles become negligible in importance; the multiply/accumulate rate of the ADSP-1110 approaches 5MHz.

	CYCLE								
Data String	**1**	**2**	**3**	**4**	**...**	**N–3**	**N–2**	**N–1**	**N**
X = BUS	-----								
Y = BUS;X*Y;CKMR		-----	-----						
X = BUS			-----						
Y = BUS;X*Y + MR;CKMR				-----	-----				
.									
.									
.									
X = BUS					-----				
Y = BUS;X*Y + MR;CKMR						-----	-----		
NOP							-----		
CKMR								-----	
BUS = MS									-----

Table V. Multiply/Accumulate Instruction Sequence

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 7V
Input Voltage	−0.3V to V_{DD}
Output Voltage Swing	−0.3V to V_{DD}
Operating Temperature Range (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (10 Seconds)	300°C

ORDERING INFORMATION*

Part Number*	Temperature Range	Package
ADSP-1110KD	0 to +70°C	28-Pin Ceramic DIP (D28B)
ADSP-1110JD	0 to +70°C	28-Pin Ceramic DIP (D28B)
ADSP-1110TD	−55°C to +125°C	28-Pin Ceramic DIP (D28B)
ADSP-1110SD	−55°C to +125°C	28-Pin Ceramic DIP (D28B)

*The ADSP-1110 will be available in plastic in mid-1984 (N28A).

See Section 19 for package outline information.

CAUTION:

1. ESD sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

APPLICATIONS

The ADSP-1110 is a high-performance component for a host of digital signal processing applications including digital filters, FFT's, table look-up, and matrix operations. Other applications include acceleration for microprocessors requiring fast multiplication. This section examines some of these applications: the FFT, digital filters, and double precision multiplication.

FFT Applications

The fast Fourier transform (FFT) is the principal algorithm used to analyze the frequency components of a signal. The FFT significantly reduces the time required to compute a Fourier transform by taking advantage of patterns in the computations to economize on multiplications. The ADSP-1110 performs the "butterfly," the key arithmetic operation in an FFT, entirely on-chip.

Figure 7 illustrates a decimation-in-time butterfly. As outlined by equations (1)

$$A_0' = A_0 + A_1 e^{j\theta} \qquad (1)$$
$$A_1' = A_0 - A_1 e^{j\theta}$$

the complex number A_1 is multiplied by a rotation, $R = e^{j\theta}$, and subtracted from the complex number A_0, producing A_0'. A_1' is obtained by adding A_0 to the complex multiplication of A_1 and R. The rotation R can be written:

$$R = e^{j\theta} = \text{COS}\ \theta + j\ \text{SIN}\ \theta \qquad (2)$$
$$= C + jS$$

In an FFT A_0 and A_1 are complex numbers. Let

$$A_0 = X_0 + jY_0 \qquad (3)$$
$$A_1 = X_1 + jY_1$$

Then,

$$(A_1)e^{j\theta} = (X_1 + jY_1)(C + jS) \qquad (4)$$
$$= (X_1C - Y_1S) + j(X_1S + Y_1C)$$

allowing A_0' and A_1' to be represented as:

$$A_0' = X_0 + jY_0 + [(X_1C - Y_1S) + j(X_1S + Y_1C)] \qquad (5)$$
$$= X_0' + jY_0'$$
$$A_1' = X_0 + jY_0 - [(X_1C - Y_1S) + j(X_1S + Y_1C)]$$
$$= X_1' + jY_1'$$

Expanding and equating real and imaginary terms yields:

$$X_0' = X_0 + (X_1C - Y_1S) \qquad (6)$$
$$Y_0' = Y_0 + (X_1S + Y_1C)$$
$$X_1' = X_0 - (X_1C - Y_1S)$$
$$Y_1' = Y_0 - (X_1S + Y_1C)$$

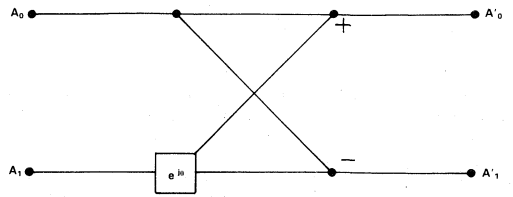


Figure 7. FFT "Butterfly" Diagram

Equations 6 can be used by the ADSP-1110 to efficiently implement the butterfly computation. First, X_0 is loaded into MR by multiplying it by positive full scale (0111...1≡k). X_0' is obtained as follows:

$$X_0' = kX_0 + X_1C - Y_1S \qquad (7)$$

Note that the factor k is not equal to unity. To ensure consistency in results, all stored cosine and sine factors (C and S) should similary be scaled by k.

$$X_1' = kX_0 - (X_1C - Y_1S) \qquad (8)$$
$$= 2kX_0 - X_0'$$

where X_0' is the accumulator's contents, and $2kX_0$ results from a mixed-mode multiplication of 2k and X_0 . This operation represents a multiply and subtraction which illustrates an additional feature of the ADSP-1110. Conventional MAC's cannot perform mixed mode multiplies or multiply/subtracts.

Table VI provides the details for computing an FFT Butterfly with the ADSP-1110. Each point requires ten cycles to compute the real component and ten cycles for the imaginary component. At 100 nanoseconds per cycle, this equals 2.0 microseconds. A 1024-point FFT requires about 5000 butterflies and therefore takes 10 milliseconds.

A butterfly calculation contains a series of multiply/accumulates and multiply/subtracts. This presents a challenge in rounding the result, becausc rounded outputs from earlier cycles become inputs in later cycles. The rounding on cycles 4, 6, 14, and 16 ensures that the outputs (on lines 7, 10, 17, and 20) are rounded correctly. Lines 4 and 14 round on bit 14 to prepare for a left shift during output. However, lines 6 and 16 round on bit 15. This is necessary because in performing the multiply and subtract on these lines, the original round on lines 4 and 14 becomes inverted—it becomes a subtraction of one, rather than an addition of one. To compensate, 2 must be added to the 14th bit, 1 to compensate for the previous round, and then 1 to round the current result. This can be easily accomplished in one step by adding a 1 to bit 15 rather than 2 to bit 14. Thus, the result in MS maintains the correct rounded result after the next accumulation.

Block floating point techniques extend dynamic range and prevent overflows when performing FFTs. Outputs are downscaled by a factor of 2 during an iteration where the possibility of overflow exists. The ADSP-1110 performs the division by 2 by not left-shifting the two's complement MR output.

Cycle	Instruction	Contents
18′.	X = BUS	Load K
19′.	Y = BUS;X_{TC}*Y_{TC};CKMR	Load X_0, MR = Previous
20′.	BUS = MS	
1.	X = BUS	Load C
2.	Y = BUS;X_{TC}*Y_{TC} + MR;CKMR	Load X_1, MR = KX_0
3.	X = BUS	Load S
4.	Y = BUS;MR − X_{TC}*Y_{TC};CKMR/RND14	Load Y_1, MR = $KX_0 + X_1C$
5.	X = BUS	Load 2K
6.	Y = BUS;X_{US}*Y_{TC} − MR;CKMR/RND15	Load X_0, MR = $KX_0 + (X_1C - Y_1S)$ + RND14
7.	BUS = MS	Output X_0′
8.	X = BUS	Load K
9.	Y = BUS;X_{TC}*Y_{TC};CKMR	Load Y_0, MR = $KX_0 - (X_1C - Y_1S)$ + RND14
10.	BUS = MS	Output X_1′
11.	X = BUS	Load S
12.	Y = BUS;X_{TC}*Y_{TC} + MR;CKMR	Load X_1, MR = KY_0
13.	X = BUS	Load C
14.	Y = BUS;X_{TC}*Y_{TC} + MR;CKMR/RND14	Load Y_1, MR = $KY_0 + X_1S$
15.	X = BUS	Load 2K
16.	Y = BUS;X_{US}*Y_{TC} − MR;CKMR/RND15	Load Y_0, MR = $KY_0 + (X_1S + Y_1C)$ + RND14
17.	BUS = MS	Output Y_0′
18.	X = BUS	Load K
19.	Y = BUS;X_{TC}*Y_{TC} + MR;CKMR	Load new X_0, MR = $KY_0 - (X_1S + Y_1C)$ + RND14
20.	BUS = MS	Output Y_1′

Table VI. Sample FFT "Butterfly" Sequence

FIR Filters

The ADSP-1110 is readily included in an FIR filter configuration. Figure 8 diagrams an N-tap finite impulse response (FIR) filter. FIR filters perform convolution in the time domain, corresponding to multiplication in the frequency domain. The coefficients C_n represent the filter's impulse response—the time domain equivalent of the filter's desired frequency response.

When implemented with the ADSP-1110, FIR filters employ a single RAM with a memory map as diagrammed in Figure 9. This contrasts with the multiple RAMs usually required in three-port MAC designs. Except in adaptive filters, where the filter response changes to meet changing system requirements, the filter coefficients C_n remain constant.

Input data, on the other hand, is continuously updated. Each new data sample overwrites the oldest data point in RAM, an action that is tracked by an address counter. The Z_{N-1} sample, for instance, is overwritten with the new Z_0 sample, and the previous Z_{N-2} sample becomes the new Z_{N-1} data point.

In the time interval between new data samples, the filter multiplies each of the N previously stored data samples, Z_n, by the respective filter coefficients, C_n. The resulting sum of the products represents the filtered signal output. An overflow flag and optional saturation logic allows long FIR filters to be implemented without risking overflow.

Note that the use of the ADSP-1110 does not require a complicated control circuit. Figure 10, for example, diagrams the controller circuit flow-chart for the FIR filter described above. When implemented in hardware, the controller's complexity remains comparable to that of the controller required for a three-port MAC-based filter design.

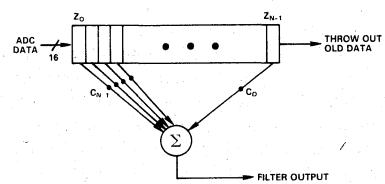


Figure 8. FIR Filter Design

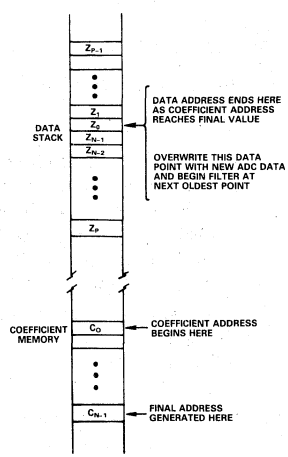


Figure 9. Memory Map

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IIR Filters

Infinite impulse reponse (IIR) filters use feedback to improve filter performance at the cost of a more complicated design. The principal advantage of an IIR filter is the relatively small number of multiplies needed to achieve a high-performance filter. The ADSP-1110, unlike conventional MAC's, has architectual features that eliminate some of the disadvantages associated with implementing IIR's.

The time required for the ADSP-1110 to calculate a biquad section of an IIR filter is (5 MAC operations) × (200 nanoseconds/operation) + 100ns (output cycle), or 1.1 microseconds. In the equation for a biquad,

$$Y_0 = a_0X_0 + a_1X_{-1} + a_2X_{-2} - b_1Y_{-2} - b_2Y_{-2} \qquad (9)$$

the coefficient b_1 often ranges from 1 to 2. The most conventional way to represent the coefficients and data is in fractional two's complement notation. Since this numbering system only ranges from -1 to 0.999 . . . , all coefficients and data for the IIR filter have to be divided by 2 to handle b_1 when using a conventional MAC. To compensate, external shifters are needed on output to shift the result up by one bit (multiply by 2).

A coefficient in the $+2$ to -2 range can be handled with the ADSP-1110 by using a mixed-mode multiply. Since the coefficient's sign is known in advance, the multiply-and-add, and multiply-and-subtract functions supply the sign to an unsigned magnitude number. The MS register is left-shifted as usual on output to obtain the correct result.

Stability is an important issue for IIR filters. The ADSP-1110's wide accumulator, together with the hard-limiting provided by its saturation circuit, prevent the overflow problems and large-scale oscillations that often plague IIR filters.

Register Transfers Aid DP Multiplies

In order to handle double precision multiplication (multiplying two 32-bit two's complement numbers), conventional MACs require additional external logic. The ADSP-1110, in contrast, performs these operations without external support. Moreover, the device performs a double precision multiplication in 15 100-nanosecond cycles, 7 of which represent overhead.

Equation 10 represents a double precision multiply:

$$\begin{aligned} P &= (X)(Y) \\ &= (MSW_x + LSW_x \cdot 2^{-16})(MSW_y + LSW_y \cdot 2^{-16}) \qquad (10) \\ &= MSW_x \cdot MSW_y + (MSW_x \cdot LSW_y + MSW_y \cdot LSW_x) \cdot 2^{-16} \\ &\quad + LSW_x \cdot LSW_y \cdot 2^{-32} \end{aligned}$$

where P is the 64-bit product of two 32-bit two's complement numbers, X and Y. MSW_x represents the 16 most significant bits of word X, and LSW_x represents the 16 least significant bits. The product P equals the sum of partial products; each partial product's sign and significance must be taken into account in order to obtain the proper result.

A double precision multiply requires no external logic. Furthermore, as illustrated in the following sequence, the ADSP-1110 performs the operation in 15 cycles.

Cycle #	Operation	Comments
1.	X = BUS	Load LSW_x.
2.	Y = BUS;X_{US}*Y_{US}; CKMR	Load LSW_y and multiply (unsigned).
3.	NOP	No op.
4.	Y = BUS;X_{US}*Y_{TC} + MR; CKMR	Load MSW_y and perform MAC (mixed-mode).
5.	LS = MS	MS shifts into LS. (The LS of the $(LSW_x)(LSW_y)$ product can be discarded since usually only 32 bits of precision are needed in the final product.)
6.	MS = EX	Shift EX into MS.
7.	X = BUS	Load MSW_x.
8.	Y = BUS;X_{US}*Y_{TC} + MR;CKMR/ RND15	Load LSW_y and perform MAC (mixed-mode) with round in bit 15.
9.	NOP	No op.
10.	Y = BUS;X_{TC}*Y_{TC} + MR;CKMR	Load MSW_y and perform MAC (two's complement).
11.	LS = MS	Shift MS into LS.
12.	MS = EX	Shift EX into MS.
13.	CKMR	Clock the output registers. This loads the MAC from step 10 into the accumulator.
14.	BUS = MS(SL)	Output MS with left shift.
15.	BUS = LS(SL)	Output LS with left shift. The SLE register provides an extra bit.

Table VII.

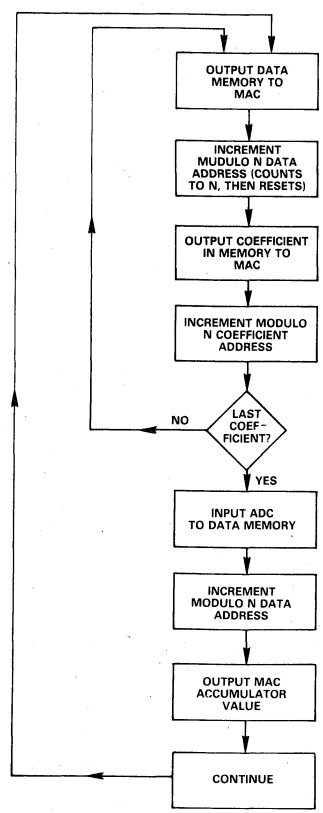

Figure 10. Controller Flow Chart for FIR Filter

In this double precision multiply sequence, shown in Table VII, the four basic multiplications require only eight cycles. Cycles 5, 6, 11, 12, 13, 14, and 15 represent overhead time.

8-Bit Extend Register Simplifies Double Precision MAC

The previous discussion concerned double precision multiplies. The ADSP-1110 also readily handles double precision multiply/accumulate operations. For example:

$$AP = \sum_{i=1}^{N} X_i Y_i \qquad (11)$$

$$= \sum_{i=1}^{N} (MSW_{xi} + LSW_{xi} \cdot 2^{-16})(MSW_{yi} + LSW_{yi} \cdot 2^{-16})$$

where each X and Y is a 32-bit number, and AP is a 72-bit accumulated product. Note that AP can be expressed as the sum of accumulated partial products as follows:

$$AP = \left[\left\{\sum_{i=1}^{N} (MSW_{xi})(MSW_{yi})\right\}\right] + \qquad (12)$$

$$+ \left[\left\{\sum_{i=1}^{N} ((MSW_{xi})(MSW_{yi}) + (LSW_{xi})(MSW_{yi}))\right\}\right] \cdot 2^{-16}$$

$$+ \left\{\sum_{i=1}^{N} (LSW_{xi})(LSW_{yi})\right\} \cdot 2^{-32}$$

Computing the accumulated double precision product AP requires the same basic sequence as in computing a single precision MAC. Simply compute a summation of partial products, rather than the summation of products themselves.

The summation of partial products often leads to sums greater than 32-bits. The 8-bit extension register stores any overflow, letting the summation proceed without error. The output and shift cycles occur once each at the end of the appropriate partial product calculation. A 32-point double precision FIR filter, requires (32-points)(4-multiplies)(2 cycles/multiply) +9 overhead cycles = 273 total cycles. At 100 nanoseconds per cycle, this represents a total of 273 microseconds or roughly 800ns/double precision multiply.

An optional procedure, which cuts the multiply/accumulate time by roughly 25%, entails omitting the $LSW_x \times LSW_y$ accumulation and instead adding ¼ of the number of accumulations to the final result. This removes the bias because the LSW's of both words have a mean value of ½ and when multiplied together have a mean product of ¼. Thus any bias in the answer is removed. A simple way to add 1's to the LSB is to assert the round control on the appropriate number of multiply operations.

PIN DESIGNATIONS

28-PIN DIP

PIN	FUNCTION	PIN	FUNCTION
1	RND15	15	CLK
2	RND14/SLE	16	CTL_D
3	I/O_{14}	17	CTL_E
4	I/O_{12}	18	CTL_F
5	I/O_{10}	19	OVF
6	I/O_8	20	I/O_1
7	I/O_6	21	I/O_3
8	I/O_4	22	I/O_5
9	I/O_2	23	I/O_7
10	I/O_0	24	I/O_9
11	CTL_A	25	I/O_{11}
12	CTL_B	26	I/O_{13}
13	CTL_C	27	I/O_{15}
14	GND	28	V_{DD}

PACKAGE D28B/N28A

Synchro & Resolver Converters

Contents

•New product since publication of *1982–1983 Databook Update.*

Inductosyn is a registered trademark of Farrand Industries, Inc.

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Selection Guide
Synchro & Resolver Converters

The products in this section are generally concerned with angular measurements. They include the following classes of device:

Digital Angle to Trigonometric (sine-cosine) Analog Voltage
Digital-to-Resolver Converters
Digital-to-Synchro Converters
Inductosyn™-to-Digital Converters
Resolver-to-Analog Voltage Converters
Resolver-to-Digital Converters
Resolver-to-Digital Display (Angular-Position Indicators)
Synchro-to-Analog Voltage Converters
Synchro-to-Digital Converters
Synchro-to-Digital Display (Angular-Position Indicators)

Complete descriptions, specifications, and applications information on the products in this section can be found in the data sheets. Brief general information can be found overleaf.

The Selection Guide is provided to ease the job of finding the right unit to do your job. Devices are listed in the Selection Guide vertically, by model number, in alphabetic, then numeric order, as well as by function and type of input. Salient characteristics are listed horizontally. A bullet is placed at each intersection that is appropriate for each device.

			ANALOG I/O				DIGITAL I/O								
							BCD				RESOLUTION (BITS)				
			SYNCHRO	RESOLVER	INDUCTOSYN™	LINEAR	BINARY	0 to ±180°	0 to 360°	PULSE TRAIN	16	14	12	10	
SYNCHRO RESOLVER INPUT	Angle Position Indicator	API1620	•	•			•		•		•				
		API1718	•	•			•		•		•				
DIGITAL INPUT	Digital to Synchro Resolver	DSC1705	•	•			•					•			
		DSC1706	•	•			•						•		
		DRC1745	•	•			•					•			
		DRC1746	•	•			•				•				
	Digital to Trig. (Analog)	DRC1765		•		•	•					•			
		DRC1766		•		•	•				•				
		DTM1716		•		•						•			
		DTM1717		•		•							•		
INDUCTOSYN INPUT	Inductosyn/ Resolver to Digital	IRDC1730		•	•		•						•		
		IRDC1731		•	•					•			•		
		IRDC1732		•	•		•						•		
		IRDC1733		•	•		•						•		
		1S20		•	•		•						•		
		1S40		•	•		•					•			
		1S60		•	•		•				•				
		1S61		•	•		•				•				
RESOLVER INPUT	Resolver to Digital Converters	RDC1740		•			•					•			
		RDC1741		•			•						•		
		RDC1742		•			•						•		
	Sync/Resolver Analog	SAC1763	•	•		•									
	Synchro or Resolver to BCD Converters	SBCD1752[1]	•	•				•				•[1]			
		SBCD1753[2]	•	•					•			•[2]			
		SBCD1756[1]	•	•				•				•[1]			
		SBCD1757[2]	•	•					•			•[2]			
	Synchro or Resolver to Binary	SDC1700	•	•			•						•		
		SDC1702	•	•			•							•	
		SDC1704	•	•			•					•			
		SDC1721	•	•			•				•				
		SDC1725	•	•			•						•		
		SDC1726	•	•			•							•	
SYNCHRO INPUT	Synchro to Digital	SDC1740	•				•					•			
		SDC1741	•				•						•		
		SDC1742	•				•						•		

NOTES
[1] 13-Bit BCD plus sign.
[2] 14-Bits BCD.
Industosyn is a registered trademark of Farrand Industries Inc.
Shading indicates new products since publication of *1982–1983 Databook Update.*

Here's an example of its use: if you were looking for a 14-bit digital-to-resolver converter with the highest accuracy in the smallest package, you might start at the 14-bit column; you would see that there are two resolver families that have 14-bit resolution and error less than 5 arc-minutes: DRC1745 and DRC1705; the DRC1745 is a hybrid, and the DRC1705 is in a >0.4" module. Thus, you would be quickly led to look at the DRC1745 data sheet and be guided to its location by the page number at the right.

In addition to the devices listed in the chart, data sheets for the following accessory products are also to be found in this section:

ACCURACY (arc-min)						ASSEMBLY/PACKAGE TECHNOLOGY				PAGE		
						MODULE						
<1	<5	<10	<20	>20	HYBRID	<0.4"H	0.4"H	>0.4"H	INSTRUMENT	VOLUME I	VOLUME II	
	•								•		13-5	API1620
	•								•		13-5	API1718
	•							•			13-9	DSC1705
	•	•						•			13-9	DSC1706
	•				•					13-5		DRC1745
	•				•					13-5		DRC1746
	•				•					13-13		DRC1765
	•				•					13-13		DRC1766
	•					•					13-13	DTM1716
	•					•					13-13	DTM1717
		•				•					13-21	IRDC1730
		•				•					13-27	IRDC1731
		•		•	•					13-17		IRDC1732
		•				•					13-21	IRDC1733
		•			•					13-29		1S20
	•	•			•					13-29		1S40
		•	•		•					13-29		1S60
		•			•					13-29		1S61
		•			•					13-23		RDC1740
		•	•		•					13-23		RDC1741
		•			•					13-23		RDC1742
			•					•			13-37	SAC1763
			•					•			13-41	SBCD1752[1]
			•					•			13-41	SBCD1753[2]
			•					•			13-41	SBCD1756[1]
			•					•			13-41	SBCD1757[2]
		•				•					13-49	SDC1700
				•		•					13-49	SDC1702
•	•					•					13-49	SDC1704
	•							•			13-55	SDC1721
					•						13-59	SDC1725
			•								13-59	SDC1726
		•			•					13-23		SDC1740
		•	•		•					13-23		SDC1741
		•			•					13-23		SDC1742

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Orientation
Synchro & Resolver Converters

These products constitute a complete line of devices for the digital measurement and control of angular and linear displacements by means of synchros, resolvers, and Inductosyns. In addition to modules and hybrid circuits that perform the appropriate conversions, the line also includes modules that perform purely algebraic or logical functions; in some cases, solid-state circuitry emulates the functions of electromechanical devices.

The range of synchro processing modules now available covers a wide area of application. They are widely used in military and radar applications, but there are additional fields in which they could be used to advantage because of the proven ruggedness and high precision of the electromechanical hardware, their standardized specifications, and their low cost. They have a number of advantages over potentiometers and optical systems.

In this introductory section, there will be provided a brief set of device definitions. Detailed data and applications information is given in the data sheets. For a complete introduction to synchro/digital conversion, Analog Devices has available a 208-page book, *Synchro and Resolver Conversion*, edited by G. Boyes (1980), $11.50.

In this section, and in much of the text, the word "Synchro" appears frequently. In many cases, the word "Resolver" could be used in its place. The modules make use of angular data in resolver form; if the input data is in three-wire synchro form, transformers in "Scott T" configuration convert it to resolver form; analog outputs are available in both forms. There are a number of voltage and frequency options.

REPRESENTATION OF ANGLES IN DIGITAL FORM

Binary

The most commonly used method of representing angles in digital form is simple natural binary weighting, where the most-significant bit (MSB) represents 180°, the next represents 90°, etc. The table shows the bit weights in degrees, degrees-and-minutes, and radians for this coding method.

Bit No.	Degrees	Degrees, minutes		Radians
1	180	180	0	3.141593
2	90	90	0	1.570796
3	45	45	0	0.785398
4	22.5	22	30	0.392699
5	11.25	11	15	0.196349
6	5.625	5	37.5	0.098175
7	2.8125	2	48.75	0.049087
8	1.40625	1	24.38	0.024544
9	0.70312	0	42.19	0.012272
10	0.35156	0	21.09	0.006136
11	0.17578	0	10.55	0.003068
12	0.08789	0	5.27	0.001534
13	0.04395	0	2.64	0.000767
14	0.02197	0	1.32	0.000383
15	0.01099	0	0.66	0.000192
16	0.00549	0	0.33	0.000096

BCD

When angular measures have to be displayed in visual form, BCD coding is used, through the use of binary-to-BCD converters, such as the BDM1615, which provides the necessary scaling and conversion, e.g., from 10100000000000 (180° + 45°) to 10 0010 0101.0000 000 (or 225.00°).

TYPICAL S/D/S DEVICES

Binary-to-Binary-Coded-Digital Converter (BDM1615/16/17)
A device that accepts angular data in binary form and converts it to BCD form, with fractional degrees in decimal fractions of 1° (1615, 1617) or minutes and seconds (1616). The BCD output is modulo 360°.

Digital-to-Synchro Converters (DSC1705/06)
Devices that accept parallel binary digital inputs (14 or 12 bits) and an ac reference signal, and provide outputs in 3-wire synchro form.

Inductosyn/Resolver-to-Digital Converter (IRDC1730)
A device that produces a digital output capable of resolving (to 12 bits) intermediate distances within a single track-pitch of a Farrand linear-Inductosyn stator in displacement- and angle-measuring Inductosyn systems. The moving element is used as though it were a resolver input; hence the device will also convert resolver information to digital.

Synchro-to-Digital Converter
A device that accepts either 3-wire synchro- or 4-wire resolver inputs, together with a 2-wire ac reference, and outputs angular binary data in a continuously tracking mode, employing a Type 2 servo loop. The inputs may be from either remote synchros or from electrically simulated synchros (e.g., DSC's).

Digital Converter and Processor for Two-Speed Synchros (TSL1612)
A two-speed processor takes as inputs two sets of digital information, representing the angles from coarse and fine synchros, and combines them to produce a single 19-bit word representing the actual angle of the "coarse" shaft. The TSL consists of the processing logic alone—it can be used with a pair of SDC's, which provide the two sets of digital information.

High Power Output, Hybrid, Digital-to-Resolver Converters

DRC1745, DRC1746

FEATURES

- 14- or 16-Bit Resolution
- 2 or 4 Arc-Minutes Accuracy
- 2VA max Mean Output Drive Capability
- Full Accuracy for dc to 2.6kHz Reference
- Full Accuracy with dc or Pulsating Power Supplies (PPS)
- Guaranteed Operation With 3V dc Pedestal on PPS
- Can Drive Pure Inductive, Resistive or Highly Capacitive Loads
- LS or CMOS Latched Inputs With Separate High/Low Byte Enable
- Low Radius Vector Variation (0.03%)
- Optional TransZorb™ Protection Against Inductive Spikes on Output
- Protected Against +200% Overvoltage on Analog Input
- Remote Output Sensing Facility
- No Trims or External Adjustments
- Full Output Short Circuit Protection
- Single 40-Pin Package

APPLICATIONS

- Driving Synchro and Resolver Control Transformers
- Avionic Equipment (e.g., Air Data Computers)
- Interfacing With Servo Systems
- Fire Control System Outputs
- Naval Retransmission Unit Outputs
- Outputs to Radars and Navigational Aids
- Aircraft and Naval Simulators

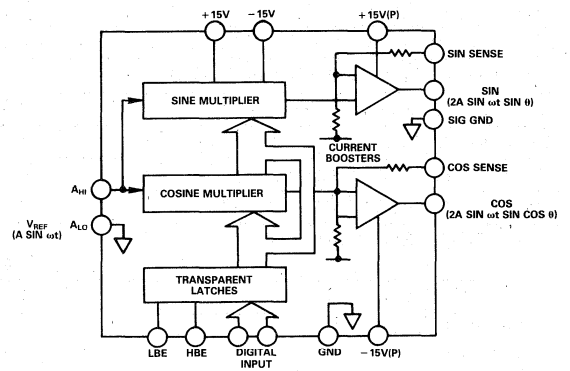
GENERAL DESCRIPTION

The DRC1745 and DRC1746 are hybrid packaged Digital to Resolver converters. They accept a 14-bit or 16-bit digital input word representing angle and output sine and cosine voltages multiplied by an analog input. The converters maintain full accuracy when the analog input frequency is in the range dc to 2.6kHz.

The units have internal power amplifiers capable of driving a 2VA load which can be pure inductive, resistive or highly capacitive. The output is fully short circuit protected against overcurrent. The output of the converter can be used to drive directly into resolver control transformers or in conjunction with an external transformer module to drive synchro control transformers. The power available is more than adequate to drive all standard synchro control transformers.

The separately powered output stage is compatible with conventional ±15V dc power supplies or pulsating power supplies with pedestal components as low as 3V dc (guaranteed) 2V (typical).

DRC1745, DRC1746 FUNCTIONAL BLOCK DIAGRAM



NOTE: "A_{LO}", "GND", AND "SIG GND" ARE INTERNALLY CONNECTED IN STAR POINT.

The use of pulsating power supplies greatly reduces the internal power dissipation in the hybrid package which in turn maximizes the converter's Mean Time Between Failures (MTBF).

A particular feature of the converters is that they have a remote sensing facility which means that output accuracy can be maintained even when long lines have to be driven.

The converters are latched and the latches can be CMOS or Low Power Schottky (LS). The former gives advantages in terms of power dissipation and the latter in terms of glitch performance when used in fast dynamic update modes. The latches are transparent and have a separate high and low byte enable.

As an option, the output stage can be fitted with internal TransZorb™ protection. This gives full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. This condition can occur at switch off or as a consequence of external power supply fault conditions.

The units are packaged in 40-pin dual in line hybrid packages and require no external trims or adjustments.

MODELS AVAILABLE

The DRC1745 (14-bit resolution) and DRC1746 (16-bit resolution) are available with accuracies of ±2 or ±4 arc-minutes. Both units have optional TransZorb protection and a choice of either LS or CMOS inputs (see Ordering Information).

TransZorb is a trade name of General Semiconductor Industries, Inc.

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SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models		DRC1745	DRC1746
DIGITAL INPUT RESOLUTION		14 Bits (1.32 arc-minutes)	16 Bits (0.33 arc-minutes)
DIGITAL INPUT FORMAT		Parallel natural binary. TTL compatible. Includes internal 27kΩ pull-up resistors.	*
RECOMMENDED ANALOG INPUT (V_{REF})		3.4 Volts rms (single ended input)	*
OUTPUT WITH RECOMMENDED ANALOG INPUT		6.8 Volts rms	*
GAIN (V_{REF} to V_O)		2 ±0.1%	*
GAIN OUTPUT TEMPERATURE COEFFICIENT		5ppm/°C of FSR (typ) 25ppm/°C (max)	*
ANALOG INPUT (V_{REF}) FREQUENCY RANGE		dc to 2.6kHz	*
ANALOG INPUT IMPEDANCE		10.2kΩ	*
ANALOG OUTPUT IMPEDANCE		0.02mΩ (typ) 0.2mΩ (max)	*
OUTPUT OFFSET VOLTAGE		10mV (typ) 25mV (max)	*
OUTPUT OFFSET VOLTAGE DRIFT		15μV/°C (typ) 50μV/°C (max)	*
OUTPUT DRIVE CAPABILITY		2VA (max mean) ±400mA peak @10 volt peak	*
PHASE SHIFT (V_{REF} to V_O)		0.08° @ 400Hz	*
OUTPUT PROTECTION			
Overvoltage		TransZorb (optional) ±12 volts standoff, ±15 volt clamp.	*
Overcurrent		Limit set @ 550mA peak. (Case header must be maintained @ 125°C max). All 4 quadrants individually trimmed.	*
RESPONSE TO A STEP INPUT		20μs (max) to within accuracy of converter. Any size digital step input.	*
VECTOR ACCURACY			
Radius Error		0.03%	*
Angular Error		±2 or ±4 arc-minutes	±2 or ±4 arc-minutes
POWER SUPPLY (NO LOAD)			
LS Latch Options	+15 Volts	15mA (typ) 22mA (max)	*
	−15 Volts	15mA (typ) 22mA (max)	*
	+15(P) Volts	20mA (typ) 34mA (max)	*
	−15(P) Volts	20mA (typ) 34mA (max)	*
	+5 Volts	44mA (typ) 72mA (max)	*
CMOS Latch Options	+15 Volts	24mA (typ) 30mA (max)	*
	−15 Volts	15mA (typ) 22mA (max)	*
	+15(P) Volts	20mA (typ) 34mA (max)	*
	−15(P) Volts	20mA (typ) 34mA (max)	*
Additional Current (Load Dependent)	+15(P) Volts	400mA Peak (max)	*
	−15(P) Volts	400mA Peak (max)	*
PULSATING POWER SUPPLY PEDESTAL		2V dc (typ) 3V dc (Guaranteed Operation)	*
POWER DISSIPATION		See Power Dissipation section of this data sheet.	*
CASE TEMPERATURE RANGE[1]		−55°C to +125°C Operating	*
		−65°C to +150°C Storage	*
PACKAGE[2]		40-Pin DIL – HY40A	*
WEIGHT		0.9 oz (25 grams)	*

NOTES
[1]Adequate heat sinking must be provided to keep the case temperature less than 125°C.
[2]See Section 19 for package outline information.

*Specifications same as DSC1745.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM INPUTS

+15V to GND	+17V
−15V to GND	−17V
+5V to GND	+5.5V
+15(P) to −15(P)	+40V
V_{REF}	±15V

CAUTION:

1. The +5 volt power supply must *never* go below GND potential.
2. Correct polarity voltages must be maintained on the ±15V and the ±15V(P) pins.

THEORY OF OPERATION

The operation of the DRC1745 and DRC1746 is illustrated in the block diagram shown in Figure 1.

The reference voltage, V_{REF}, (A sin ωt) is multiplied by both Sin θ and Cos θ where θ is the digital angle. The resultant outputs then pass through the current booster output stage to provide the resolver format output voltages viz:

2A Sin ωt Sin θ (Sine output)
and 2A Sin ωt Cos θ (Cos output)

(Note: Converter has a gain of 2 from input to output.)

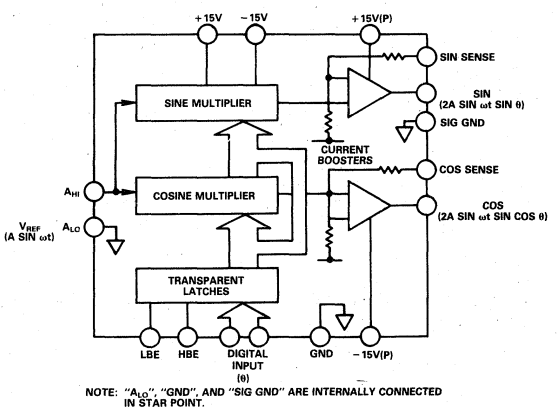


Figure 1. Theory of Operation

CONNECTING THE CONVERTER

The connections to the DRC1745 and DRC1746 are very straightforward.

The digital inputs should be connected to the converter using pins 1 (MSB) through 14 (LSB) in the case of the DRC1745 and through 16 (LSB) in the case of the DRC1746. The format of the digital angular input is shown under the "Bit Weight Table" section on this page.

The digital input control lines should be connected as described under the "Digital Data Input" section.

A_{Lo} and A_{Hi} are for the analog input reference voltage (V_{REF}). It should be noted that this is a single ended input where A_{LO} is grounded internally. If it is desired, the V_{REF} input can be externally isolated using the STM1681 transformer. See the section on "Output and Reference Transformers".

The converters have separate power supply inputs for the output amplifier stage (+15V(P) and −15V(P)) and for the remainder of the converter (+15V and −15V). When dc power supplies are used for the output stage, the supplies may be linked. However, when pulsating power supplies are used for the output stage, a separate dc supply must be provided for the +15V and −15V requirement. The converters have internal capacitive decoupling of 47nF on both power stage and converter supply but it is recommended that 6.8μF capacitors are taken from the +15V and −15V pin to "GND".

The "Case" pin is joined to the case which is isolated and should be connected to a convenient zero potential point in the system.

The sine and cosine outputs are taken from the "Sin" and "Cos" pins with "SIG GND" as the common connection.

The remote sense facility using "Cos Sense" and "Sin Sense" connections should be used as described under the "Remote Output Sensing" heading. If not used, the sense outputs should be connected to the corresponding Sin and Cos outputs.

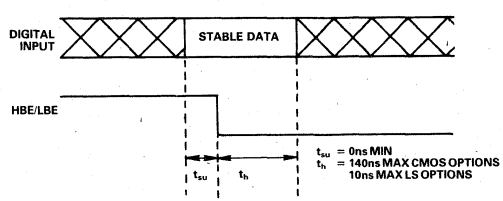
DIGITAL DATA INPUT

The digitial input to the converters is internally buffered by transparent latches. The latches will be CMOS (type 54C373) or low power Schottky (LS) (type 54LS373) depending on the option.

The "HBE" input controls the input of the most significant 8 bits and the "LBE" input controls the input of the least significant bits (6 in the case of the DRC1745 and 8 in the case of the DRC1746).

A logic "Hi" on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital input. When "HBE" and "LBE" are taken to a logic "Lo" state, the converter output will be latched at the level of the data present on the input at the low going edge and remains constant until "HBE" and "LBE" are taken to a "Hi" state again. If the latches are not required, "HBE" and "LBE" can be left open circuit. The timing diagram in Figure 2 illustrates the use of "HBE" and "LBE".

Internal resistive pull-ups (to +5V using 27k resistors) are employed on all digital inputs. This ensures full TTL compatibility for either latch option even when sourcing 50μA of leakage current into each external digital driver.



NOTE: INTERNAL LATCHES ARE: 54LS373 (LS) 54C373 (CMOS)

Figure 2. Data Transfer Diagram

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB DRC1745)	0.0220
15	0.0110
16 (LSB DRC1746)	0.0055

POWER DISSIPATION, PULSATING POWER SUPPLIES AND HEAT SINKING

The DRC1745 and the DRC1746 can be used with conventional dc power supplies or a pulsating power supply on the output stage. The latter gives significant reductions in power dissipation within the hybrid package without any attendant loss of accuracy.

When using a pulsating power supply full advantage can be taken of the special design which allows the power supply to have a very low dc pedestal voltage. This results in minimized power dissipation. The pedestal voltage can in fact be as low as 2 volts (typical) 3 volts (guaranteed operation). It need not exceed 5 volts even at 2VA loading.

Full accuracy is retained during operation on pulsating power supplies because the output stage employing these supplies is only used to provide current gain. Overall operational loop gain is independently powered. There are no special switch-on/switch-off power supply sequencing requirements, and full internal protection is provided (except when driving capacitive loads.)

The section below demonstrates the power dissipation differences for different load conditions when using dc supplies and pulsating power supplies.

Dc Power Supplies: When using dc power supplies, the expression for additional load dependent power dissipation is:

$$P = \frac{2\,V_{dc}I_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) - \frac{V_o I_1\,\mathrm{Cos}\alpha}{2} \qquad (1)$$

Where V_o is the peak output voltage.
I_1 is the peak value of the output load current.
θ is the digital angle.
α is the load phase angle.
V_{dc} is the dc power supply voltage (usually ± 15 volts).

Pulsating Power Supplies:
When using a pulsating power supply, the expression for additional load dependent power dissipation within the hybrid is:

$$P = \frac{2\,V_pI_1}{\pi}\,(|\mathrm{Sin}\theta| + |\mathrm{Cos}\theta|) + \frac{V_{ac}I_1}{\pi}\,(\mathrm{Sin}\alpha - \alpha\mathrm{Cos}\alpha) \qquad (2)$$

Where V_{ac} is the peak ac component of the pulsating power supply assumed equal to the peak output voltage, V_o.
I_1 is the peak value of the output load current.
θ is the digital angle
α is the load phase angle.
V_p is the dc pedestal voltage of the pulsating power supply.

Note that $I_1 = \frac{V_o}{|Z|}$ where V_o = Peak output voltage

$= 2 \times V_{REF}$

$|Z|$ = output load

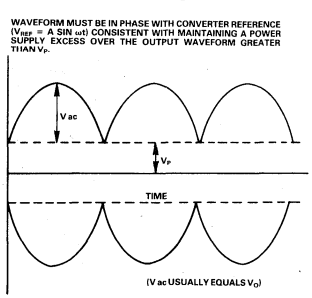


Figure 3. Pulsating Power Supply Format

Examples of Power Dissipation:
Many factors influence the power dissipation within the hybrid. The following four examples, using typical load values and *worst case* digital angle conditions (45 degrees), illustrate the saving in power dissipation which can be achieved by using a pulsating power supply employing a low pedestal voltage.

Note that in the following examples we have chosen:

$V_{dc} = \pm 15$ volts
$V_p = 3$ volts
$V_o = 9.6$ volts (6.8 volts rms)
$V_{ac} = 9.6$ volts (should be chosen to equal V_o)
$I_1 = 292$mA (equivalent to a 1.4VA mean load)

1) DC power supply, $\theta = 45°$ resistive load.

$$P = \frac{2\mathrm{X}15\mathrm{X}0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} - \frac{9.6\mathrm{X}0.292\mathrm{X}1}{2}$$

$= 3.943 - 1.402$

$= \underline{2.54\ \text{Watts}}$

2) As example (1) but with a 3 volt pedestal pulsating power supply.

From equation (2):

$$P = \frac{2\mathrm{X}3\mathrm{X}0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} + \frac{9.6\mathrm{X}0.292\mathrm{X}0}{\pi}$$

$= \underline{0.79\ \text{Watts}}$

Thus the pulsating power supply has cut down the internal dissipation by 1.75 watts, a ratio of 3.2:1.

3) DC power supply, $\theta = 45°$, pure inductive load ($\alpha = \frac{\pi}{2}$)

From equation (1):

$$P = \frac{2\mathrm{X}15\mathrm{X}0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} - \frac{9.6\mathrm{X}0.292\mathrm{X}0}{2}$$

$= \underline{3.94\ \text{Watts}}$

(4) As example (3) but with 3 volt pedestal pulsating power supply.

From equation (2):

$$P = \frac{2\mathrm{X}3\mathrm{X}0.292(\mathrm{Sin}45° + \mathrm{Cos}45°)}{\pi} + \frac{9.6\mathrm{X}0.292\mathrm{X}1}{\pi}$$

$= \underline{1.68\ \text{Watts}}$

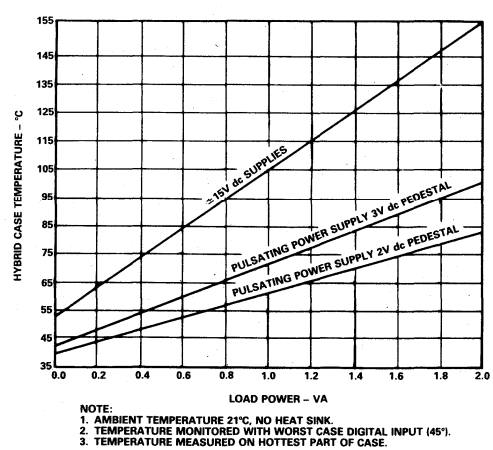


Figure 4. Case Temperature for Resistive Loads

Thus the pulsating power supply has cut down the internal dissipation by 2.26 watts, a ratio of 2.3.:1.

The graph shown in Figure 4 shows the temperature at the hottest part of the base of the hybrid (in the middle of the base between "+15V(P)" and the opposite "N/C" pin) for resistive loads up to 2VA using dc supplies and pulsating supplies with pedestals of 3 volts and 5 volts.

Figure 5 shows a similar graph for inductive loads up to 1VA.

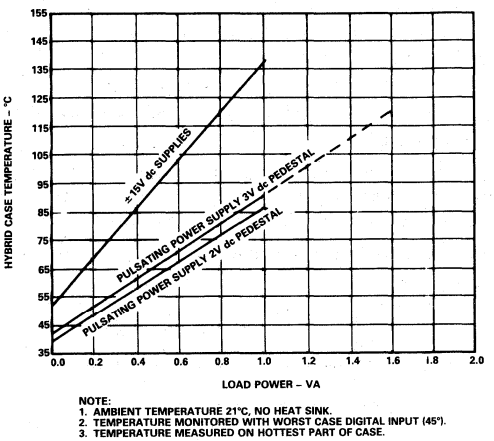


Figure 5. Case Temperature for Inductive Loads

As can be seen from Figures 4 and 5, it will be necessary to provide heat sinking when driving significant loads in order to keep the temperature of the case below its 125°C maximum.

The converters have been designed with a flat metal base to facilitate mounting on heat sinking materials. Special thermal management techniques have been employed within the hybrid output stage to give:

Angle

0°, 90° θJunction/case = less than 12°C/watt
45°, 135° θJunction/case = less than 6°C/watt

Consequently the internal junction temperatures do not exceed case header temperature by more than 20°C when using pulsating power (even under worst case pure inductive load conditions. The maximum permitted junction temperature is 155°C).

CALCULATING THE LOAD

The following describes how to calculate the load.

In the case of synchro control transformers first determine the value of Z_{so}. This impedance is normally quoted by the synchro manufacturer.

The load presented by the control transformer will be:

$$\frac{3}{4} \times \frac{V^2}{|Z_{so}|}$$

where V^2 is the rms signal input voltage.

When the STM1681 output transformers are used it is necessary to add 0.25VA to the calculated figures.

For example, assume that a 90V rms signal, 400Hz synchro control transformer is to be driven by the DRC1745 in conjunction with the STM1681/612 output and reference isolation transformer set. (The STM1681/612 boosts the 6.8V rms signal from the DRC1745 to the 90V rms required by the control transformer.)

Z_{so} for the control transformer is quoted as:

$$700 + j4900$$

Therefore

$$|Z_{so}| = \sqrt{700^2 + 4900^2} = 4950 \text{ Ohms}$$

Therefore, the load presented by the control transformer is:

$$\frac{90^2}{4950} \times \frac{3}{4} = 1.23\text{VA}$$

Adding to this value 0.25VA for the STM1681 gives a figure of 1.48VA total.

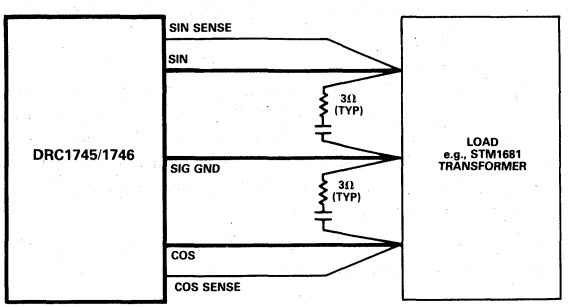
In the case of a resolver control transformer the same exercise must be performed but it is not necessary to multiply by 3/4. Some resolver manufacturers quote rms input current and in this case the load will be the product of the input current and the rms voltage used to drive it. The 0.25VA must be added if the STM1681 transformers are to be used.

DRIVING CAPACITIVE LOADS

In many cases, synchros or resolvers have capacitively tuned inputs in order to minimize power dissipation. The tuning of the synchro or resolver can either be on the load itself or on the primary of the transformer driving the load. If the capacitors are fitted on the load, (i.e., on the secondary of the driving transformers) then the capacitive value will appear to the DRC1745 or DRC1746 as n^2 times the value of the capacitor used where n is the transformer turns ratio.

The DRC1745 and DRC1746 can readily drive capacitive inputs up to 150nF at the primary of the output transformer without special precautions. However when the effective capacitance to be driven is greater than 150nF special precautions must be taken. Viz:

1. An additional resistor must be included with each tuning capacitor as shown in Figure 6. A minimum of 3 ohms is recommended referred to the converter output. This figure will vary with the square of the turns ratio when driving the output transformers.



NOTE: THE REMOTE SENSE FACILITY IS SHOWN IN THE ABOVE DIAGRAM.

Figure 6. Incorporating a Resistor in the Tuning Circuit

2. A delayed switch on power sequencing system must be employed that inhibits the application of power to the output stage (and hence the tuned load) for at least 100μs after the +15V and −15V supplies have been established to the computing core of the converter (+15V and −15V pins). This allows the negative feedback loop encompassing the output stage of the converter to be established prior to the application of additional phase shift associated with the tuning, thereby, avoiding a potential limit cycle.
3. Care must be taken in tolerancing the tuning capacitors in order to retain the accuracy under tuned load conditions.

The use of these precautions enables the converters to drive fully tuned 2VA loads.

SHORT CIRCUIT PROTECTION

The short circuit current limit is set at 550mA peak and is individually trimmed for each output and the sign of each output.

Under short circuit or excessive current conditions the overcurrent protection circuit will trip and linearly reduce the output current to zero. The output stage will then enter a wait period before attempting to redrive the load. This function, which will be performed at approximately 500kHz and a mark space of 3:1, affords additional protection to the converter.

When the overload conditions are removed, the output is automatically restored to its normal condition.

VECTOR ERRORS AND EFFECTS

The error law used in the converter has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the thin film resistor networks used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays, or metal cutting control where perfect circles have to be generated.

BANDWIDTH

The open loop gain bandwidth product of the DRC1745 and DRC1746 has been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6kHz. This results in a closed loop bandwidth of 300kHz.

REMOTE SENSE FACILITY AND ADDITIONAL OUTPUT ERRORS

A remote sense facility is included in the DRC1745 and DRC1746 in order to reduce errors caused by the output interconnection wiring when driving large loads. The magnitude of this error is illustrated by two examples below.

Assume that the sine and cosine load impedances are perfectly matched and the sine output wiring resistance matches the cosine output wiring resistance to within 5%. Then for a resistive load of 1.4VA (33 ohms) and the worst case angle of 45 degrees, there will be 1.3 arc-minutes of extra error introduced for every 250 milliohms of resistance for the loop wiring between the converter and the load.

In the case of an inductive load under similar conditions, 500 milliohms would produce the same error.

Example 1.

Take the case of a 1.4VA resistive load at an angle of 45 degrees driven via a printed circuit board track 0.010″ wide in 1 ounce copper (400 milliohms per foot) matched to ±5% as above.

Then 1.3 arc-minutes of extra error is introduced for a length of track equal to: $\frac{250}{400}$ ft. = 7.5 inches
or 3.75 inches to the load and back

Example 2.

Take the case of a 1.4VA inductive load at an angle of 45 degrees driven via 22 gauge wire of resistance 17 milliohms per foot, method to ±5% as above.

Then 1.3 arc-minutes of extra error is introduced when the loop wiring is: $\frac{500}{17}$ ft. = 29.4 feet
or 14.7 ft. to the load and back

Using the remote sense facility as shown in Figure 7 will half this error or allow twice the distance to be driven for the same additional error.

If the remote sense is not used then "COS SENSE" should be joined to "COS" and "SIN SENSE" should be joined to "SIN" at the converter.

Note also that when output transformers are used with the converters they should be regarded as the load and the remote sense wires taken to the transformer primary inputs.

Sense wiring may employ minimum wire gauge; it does not carry load current.

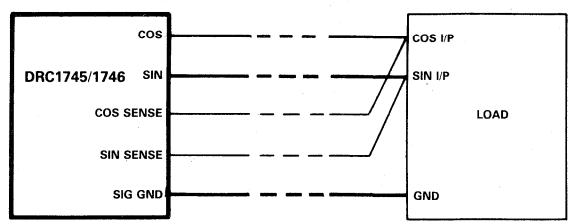


Figure 7. Using the Remote Sense Facility

TRANSZORB™ OUTPUT PROTECTION

As an option, the output stages of the converter can be internally fitted with TransZorb protection. This form of protection can be advantageous and significantly increase the Mean Time Between Failures when driving inductive loads. The TransZorbs, which are effectively back to back zener diodes, give full protection against transient voltages generated by an inductive load in response to an abrupt change in load current. Such a change can occur at switch off or as a consequence of external power supply fault conditions. The TransZorbs are rated to give protection against worst case transients corresponding to an instantaneous interruption of the converter when driving into a full 2VA pure inductive load with the converter operating at the maximum case temperature of 125°C.

Figure 8 shows a simplified diagram of the converter output stage indicating the action of the TransZorb when the 15 volt supply is interrupted.

It is important to appreciate that destructively high voltages can be generated (given by E = Ldi/dt) even for modest inductive loading, under many fault conditions, since di/dt is effectively uncontrolled. Internal TransZorb protection is a better and more direct solution to the problem than employing a pair of reverse biased diodes to the output stage power supplies. This is because the transient is contained within the specific load disturbed and does not escape into the power supply wiring and hence cause possible damage to other equipments and devices. A domino effect of catastrophic failure is therefore prevented.

TransZorb is a registered trade name of General Semiconductor Industries, Inc.

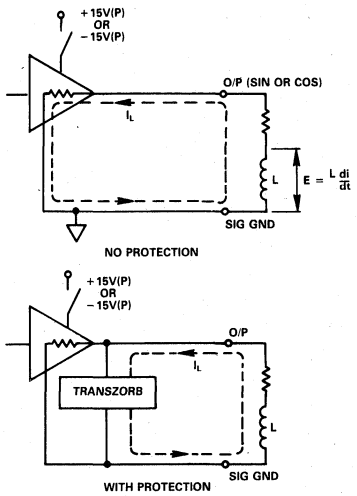


Figure 8. DRC1745/DRC1746 Output Stage Showing TransZorb Protection

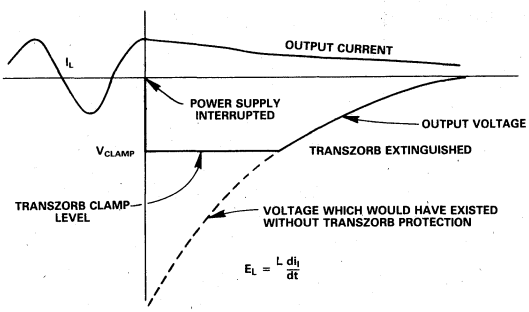


Figure 9. Transient Waveforms and TransZorb Clamping

Figure 9 shows the nature of the transient waveforms where by the very large transient voltage generated by the inductive load is limited to a safe clamp level when it is applied to the output stage.

OUTPUT AND REFERENCE TRANSFORMERS

The STM1681 module contains a reference input isolation transformer as well as a pair of output transformers which are capable of handling the full drive capability of the DRC1745 and DRC1746.

The reference transformer part of the STM1681 can accept voltages of 11.8 volts, 26 volts or 115 volts depending on the option and its output is 3.4 volts rms which is suitable for connecting to A_{Hi} and A_{Lo} on the converter.

The pair of output transformers accept the 7 volt rms output of the converter and provide a synchro or resolver format output depending on the option. (Note that for resolver output options, the part number is RTM1681).

The specification below defines the STM1681 module.

Note that smaller output transformers are available if full load capability is not required. Please consult the factory.

REFERENCE INPUT TRANSFORMER

Input Voltage (R_{Hi}, R_{Lo})	11.8, 26, 115 volts rms depending on option (+10% max voltage)
Output Voltages (A_{Hi}, A_{Lo})	3.4 volts rms ±0.1%
Frequency Range	360 to 2600Hz
Input Impedance	
11.8V input	5kΩ (min)
26V input	25kΩ (min)
115V input	475kΩ (min)

OUTPUT TRANSFORMERS

Input Voltage (SIN, COS)	6.8 volts rms ±0.1%
Output Voltages (S1, S2, S3, [S4])	11.8, 26, 90 volts rms depending on option
Output Format	Synchro or Resolver depending on option
Accuracy	
0.1VA load	±1 Arc Min
1.4VA load	±2.5 Arc Mins
2.0VA load	±3.5 Arc Mins
Output Impedance	
11.8V output	6Ω (max)
26V output	30Ω (max)
90V output	400Ω (max)
Module Size	3.125″ × 1.5″ × 1″ (79.4 × 38.1 × 25.4mm)
Operating Temperature	−55°C to +105°C

The pin out and dimensions of the STM1681 are shown on the next page, and the connection to the converter and load in Figure 10.

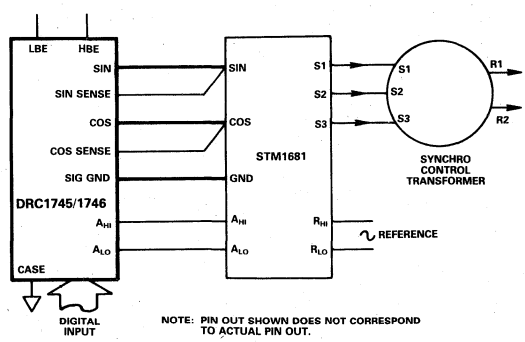


Figure 10. Connecting the DRC1745 to the STM1681 Transformers and a Synchro Control Transformer Load

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of voltage both when used with or without the reference and output transformer STM1681.

When the converters are used with the STM1681 transformer, a

resistance of value 3kΩ per extra volt required should be inserted in the A_{Hi} line. Care should be taken to ensure that the voltage on the analog input (A_{Hi}, A_{Lo}) is 3.4 volts rms in order to provide a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and therefore the resistor tolerance should be chosen so that the correct voltage appears across the A_{Hi}, A_{Lo} pins. Note that the input to the reference transformer should not exceed the rated max.

Note that the best dc output offset performance is achieved when the STM1681 transformers are used. However the use of resistive scaling can never cause an additional offset of greater than 6.5mV (max), 2.6mV (typ).

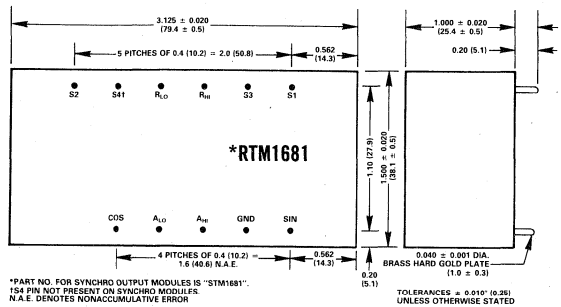
OTHER PRODUCTS

We manufacture a wide range of hybrid and modular circuits for processing synchro and resolver information. Please ask for our comprehensive literature.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

RTM1681



ORDERING INFORMATION

The converter part number should be suffixed with an option code as shown below in order to fully specify the device.

DRC1745/LT4

- 1745 = 14-bit resolution
- 1746 = 16-bit resolution
- 2 = ±2 Arc-Mins Accuracy
- 4 = ±4 Arc-Mins Accuracy
- L = Low power Schottky input latches
- C = CMOS input latches
- T = Internal TransZorb protection
- 0 = Without TransZorb protection

The STM1681 transformer should be ordered as follows:

STM1681/611

- STM for synchro output options
- RTM for resolver output options
- 1 = 26V rms Ref. input, 11.8V rms output, synchro format
- 2 = 115V rms Ref. input, 90V rms output, synchro format
- 3 = 11.8V rms Ref. input, 11.8V rms output, resolver format
- 4 = 26V rms Ref. input, 26V rms output, resolver format
- 8 = 26V rms Ref. input, 11.8V rms output, resolver format.
- 1 = 360 to 2600Hz operation
- 6 = −55°C to +105°C operating temperature range.

ANALOG DEVICES

14- & 16-Bit, Hybrid Digital-to-Resolver Converter

DRC1765, DRC1766

FEATURES

- Single Rank Transparent LS or CMOS Latched Inputs Registers With High and Low Byte ENABLE
- 14- or 16-Bit Resolution
- ±2 or ±4 Arc-Minutes Accuracy
- Very Low dc Offset Voltage
- 4.3mA Peak Output Will Drive Resistive, Inductive or Capacitive Load
- Low Radius Vector Variation (Transformation) Ratio). (0.03%)
- CMOS Version Requires Only ±15V Supplies
- Low Power Dissipation (CMOS Option)
- DC to 2.6kHz Operation
- Single 32 Pin Package
- Protection Against +200% Overload On Analog Input

APPLICATIONS

- Polar to Rectangular Coordinate Conversion
- Missile and Fire Control Systems
- Simulators
- Low Frequency Oscillators
- PPI Displays
- Radar and Navigational Systems
- Axis Rotation
- Avionics

GENERAL DESCRIPTION

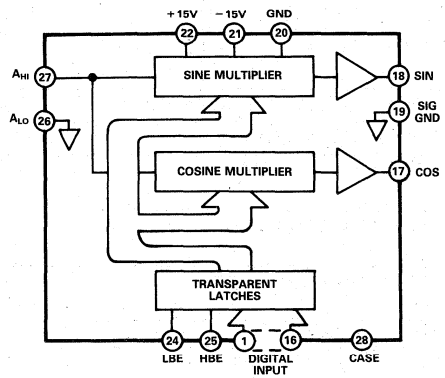
The DRC1765 and DRC1766 are hybrid digital to resolver converters which accept a 14-bit or 16-bit digital input work representing angle and output Sine and Cosine voltages which are multiplied by an analog input reference voltage. The analog input voltage can either be dc or ac voltage of frequency up to 2.6kHz.

The digital input to the converter is latched with a transparent high and low byte ENABLE system to facilitate easy interfacing to microprocessor systems. The input latches can be CMOS or Low Power Schottky.

The units are available in accuracy grades of ±2 and ±4 arc-minutes.

A particular feature of the converters is their low dc output offset voltage (±2mV typ). This compares very favorably

DRC1765, DRC1766 FUNCTIONAL BLOCK DIAGRAM



with similar products on the market where the offset voltage can be as high as ±50mV. This low offset voltage means that external trim adjustments are not required which is particularly important in display applications.

The converters have a closed loop bandwidth of 300kHz and are able to drive into a load which can be inductive, resistive or capacitive to the extent of 15nF.

A further feature of the converters is that the radius vector variation (transformation ratio) is very low at 0.03%. This means that the individual Sine and Cosine outputs are independently accurate which is important in coordinate conversion or display applications.

The power consumption of the DRC1765 and DRC1766 is particularly low in the case of the CMOS latch option which only requires ±15 volts power rails.

The converters are housed in a 32-pin triple DIP hybrid package and hermetically sealed.

MODELS AVAILABLE

The DRC1765 (14-bit resolution) is available with accuracies of ±2 or ±4 arc-minutes. The DRC1766 (16-bit resolution) is available with accuracies of ±2 or ±4 arc-minutes. Both models offer a choice of LS or CMOS logic inputs.

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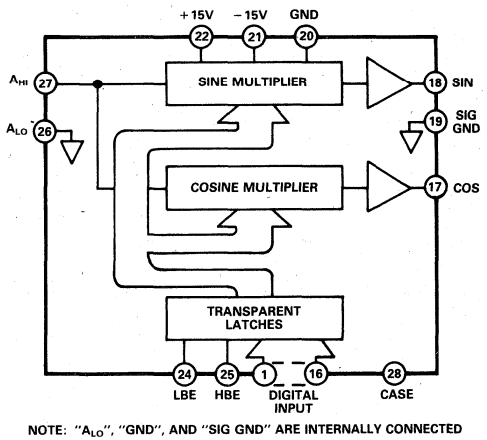
SPECIFICATIONS (typical @ 25°C, unless otherwise stated)

Models	DRC1765	DRC1766
DIGITAL INPUT RESOLUTION	14 Bits (1.3 arc-minutes)	16 Bits (0.33 arc-minutes)
DIGITAL INPUT FORMAT	Parallel natural binary. TTL compatible. Includes internal pull ups of 27kΩ.	*
RECOMMENDED ANALOG INPUT (V_{REF})	3.4 Volts rms	*
OUTPUT (SINE AND COSINE) WITH RECOMMENDED ANALOG INPUT	6.8 Volts rms ± 0.1%	*
OUTPUT TEMPERATURE COEFFICIENT	5ppm/°C of FSR (typ) 25ppm/°C of FSR (max)	* *
ANALOG INPUT FREQUENCY RANGE	dc to 2.6kHz	*
ANALOG INPUT IMPEDANCE	10.2kΩ	*
ANALOG OUTPUT IMPEDANCE	20mΩ (max) 2mΩ (typ)	* *
ANALOG OFFSET VOLTAGE	± 2mV (typ) ± 12mV (max)	* *
OUTPUT DRIVE CAPABILITY	4.3mA peak @ ± 10V peak	*
OUTPUT PROTECTION	Any one output may be grounded indefinitely	*
RESPONSE TO A STEP INPUT	20μs (max) to within accuracy of converter. Any size step input.	*
VECTOR ACCURACY		
Radius Error	0.03%	*
Angular Error	± 2, ± 4 minutes	*
POWER SUPPLIES		
CMOS Options		
+ 15 Volts	18mA (typ) 26mA (max)	*
− 15 Volts	15mA (typ) 23mA (max)	*
LS Options		
+ 15 Volts	18mA (typ) 25mA (max)	*
− 15 Volts	15mA (typ) 23mA (max)	*
+ 5 Volts	43mA (typ) 80mA (max)	*
TEMPERATURE RANGE		
Operating	− 55°C to + 125°C	*
Storage	− 65°C to + 150°C	*
DIMENSIONS	1.74" × 1.14" × 0.28"	*
PACKAGE TYPE[1]	32-pin triple DIP – HY32C	*
WEIGHT	20 grams (typ)	*

NOTES
[1]See Section 19 for package outline information.
*Specifications same as DRC1765.
Specifications subject to change without notice.

THEORY OF OPERATION

The block diagram below illustrates the operation of the DRC1765 and DRC1766.



NOTE: "A_{LO}", "GND", AND "SIG GND" ARE INTERNALLY CONNECTED

Figure 1. Theory of Operation

An input signal applied between A_{HI} (analog input HI) and A_{LO} (analog input LO) is multiplied by both sineθ and cosineθ where θ is represented by a digital input word.

The resulting outputs at pins Sin and Cos are;

V_O Sin = $2V_i$ Sinθ
V_O Cos = $2V_i$ Cosθ

All the signal inputs and outputs are referred to the SIG GND.

CONNECTING THE CONVERTER

The connections to the DRC1765 and DRC1766 are very straightforward.

The digital inputs should be connected to the converter using pins 1 (MSB) through 14 (LSB) in the case of the DRC1765 and through 16 (LSB) in the case of the DRC1766. The format of the digital angular input is shown under the "Bit Weight Table" section on this page.

The digital input control lines should be connected as described under the "Digital Data Input" section.

A_{LO} and A_{HI} are for the analog input reference voltage (V_{REF}). It should be noted that this is a single ended input where A_{LO} is grounded internally. If it is desired, the V_{REF} input can be externally isolated using the STM1680 transformer. See the section on Reference Transformer.

The "Case" pin is joined to the case which is isolated and should be connected to a convenient zero potential point in the system.

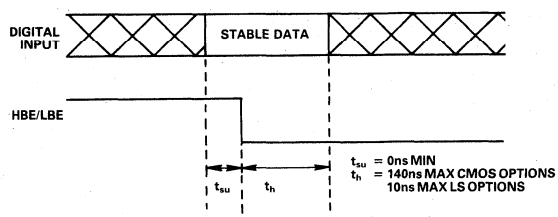
The sine and cosine outputs are taken from the "Sin" and "Cos" pins with "SIG GND" as the common connection.

DIGITAL DATA INPUT

The digital input to the converters is internally buffered by transparent latches. The latches can be CMOS (type 54C373) or low power Schottky (LS) (type 54LS373) depending on the option.

The "HBE" input controls the input of the most significant 8-bit and the "LBE" input controls the input of the least significant bit (6 in the case of the DRC1765 and 8 in the case of the DRC1766).

A logic "Hi" on the control lines causes the input to appear transparent and the converter output will follow the changes on the digital input. When "HBE" and "LBE" are taken to a logic "Lo" state the converter output will be latched at the level of the data present on the input at the low going edge and remains constant until "HBE" and "LBE" are taken to a "Hi" state again. If the latches are not required, "HBE" and "LBE" can be left open circuit. The timing diagram in Figure 2 illustrates the use of "HBE" and "LBE".



NOTE: INTERNAL LATCHES ARE: 54LS373 (LS) 54C373 (CMOS)

Figure 2. Data Transfer Diagram

Internal resistive pull-ups (to +5V using 27k resistors) are employed on all digital inputs. This ensures full TTL compatibility for either latch option even when sourcing 50μA of leakage current in each external digital driver.

BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0439
14 (LSB DRC1765)	0.0220
15	0.0110
16 (LSB DRC1766)	0.0055

VECTOR ERRORS AND EFFECTS

The conversion technique has no inherent vector errors. The figure of 0.03% given in the specification is accounted for by tolerances in some of the internal components used in the converter.

These very low vector errors make the converters ideally suited for applications such as displays, or metal cutting control where perfect circles have to be generated.

BANDWIDTH

The open loop gain bandwidth product of the DRC1765 and DRC1766 has been tailored to ensure that the full angular accuracy is maintained over the broadband range of dc to 2.6kHz. This results in a closed loop bandwidth of 300kHz.

DEGLITCHING THE CONVERTERS

The DRC1765 and DRC1766 are fundamentally digital to analog converters and can, therefore, produce glitches on the output at the major transition points of the digital input. For most applications these glitches can be removed by simple smoothing circuits on the outputs. However, in applications where the smoothing is not an acceptable solution, sample and hold amplifiers such as the Analog Devices type AD582 can be used to remove the glitches.

ABSOLUTE MAXIMUM INPUTS

A_{HI} to A_{LO}	$\pm V_{SUPPLY}$
+15V Pin	+17V
−15V Pin	−17V
+5V Pin (LS Option)	−0.4V to +7V
Case to GND	±20V
Any Logical Input	−0.4V to +5.5V

RESISTIVE INPUT SCALING

The analog reference input can be externally resistively scaled to cater for a wide range of voltage.

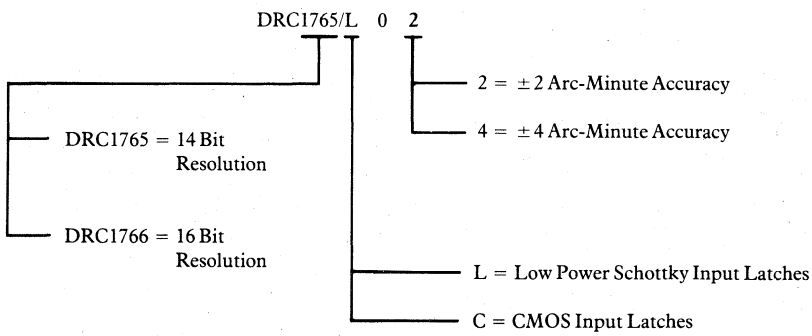
A resistance of value 3kΩ per extra volt required should be inserted in the A_{HI} line. Care should be taken to ensure that the voltage on the analog input (A_{HI}, A_{LO}) is 3.4 volts rms in order to provide a full scale analog output. The maximum output voltage of the converter is proportional to the input voltage (gain of 2) and, therefore, the resistor tolerance should be chosen so that the correct voltage appears across the A_{HI}, A_{LO} pins.

REFERENCE INPUT TRANSFORMER

Input Voltage (R_{HI}, R_{LO})	11.8, 26, 115 volts rms depending on option (+10% max voltage)
Output Voltages (A_{HI}, A_{LO})	3.4 volts rms ±0.1%
Frequency Range	360 to 2600 Hz
Input Impedance 11.8V input	5kΩ (min)

ORDERING INFORMATION

The converter part number should be suffixed with an option code as shown below in order to fully specify the device.



ANALOG DEVICES

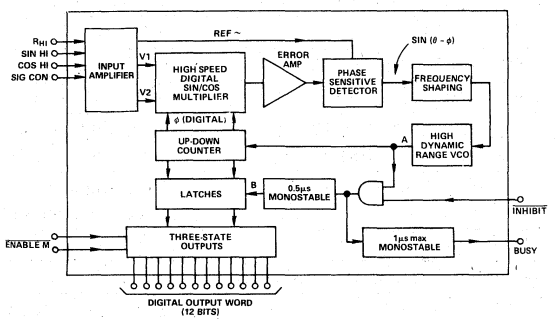
Hybrid, Tracking Inductosyn™/ Resolver-to-Digital Converter

IRDC1732

FEATURES
Low Cost
High Tracking Rate
Reference Frequency 400Hz to 10kHz
Hybrid Construction
Tri-State Digital Output
No External Adjustment

APPLICATION
Industrial Controls
Machine Tool and Robots

IRDC1732 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The IRDC1732 converts resolver format (sine and cosine) signals into a 12-bit parallel digital word. A resolver input is converted into a 12-bit natural binary digital word that represents the shaft angle. An Inductosyn input is similarly converted. The 12-bit word now represents the distance moved through an Inductosyn pitch.

The converter is of the continuous tracking loop type employing a type 2 servo loop and operates at input rates in excess of 100 revolutions or pitches per second.

Operation of the converter is possible over the reference frequency range of 400Hz to 10kHz; the signal and reference voltages are nominally 2.5V rms. The signal and reference inputs are nonisolated resistive.

As the IRDC1732 uses only the ratio of sine to cosine value for the conversion of the angle it is insensitive to reference voltage, frequency and waveform variations. The ratiometric amplitude measurement technique also ensures a high degree of input noise immunity. The inclusion of a phase sensitive demodulator within the tracking loop means that the converter is insensitive to signals which are not phase and frequency coherent with the reference input.

The IRDC1732 is of hybrid manufacturing technique using only three integrated circuit chips, including 1 LSI custom chip, for the realization of the converter function. Hybrid construction and the small number of chips ensures high realiability. The IRDC1732 is housed in a triple DIP 32-pin enclosure. The industrial temperature range (0 to +70°C) version IRDC1732/560 is housed in a ceramic case and the extended temperature range (−55°C to +125°C) version IRDC1732/460 and 410 are housed in a hermetically sealed metal case.

MODELS AVAILABLE

Three versions of the IRDC1732 are available: the industrial temperature range and the extended temperature range. Details of how to specify the exact part number are listed under "Ordering Information".

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Inductosyn is a registered trademark of Farrand Industries, Inc.

SPECIFICATIONS (typical @ +25°C, unless otherwise noted)

Models	IRDC1732/560	IRDC1732/460	IRDC1732/410
RESOLUTION	12 Bits (Natural Binary)	*	*
ACCURACY[1]	±21 arc mins	*	*
DIGITAL OUTPUT	Parallel 1LS TTL Load MSB = 180°or Halfpitch	*	*
SIGNAL & REFERENCE FREQUENCY	1kHz to 10kHz	*	400Hz
SIGNAL VOLTAGE	2.5V rms	*	
SIGNAL INPUT IMPEDANCE	50kΩ ± 2%	*	*
REFERENCE VOLTAGE	2.5V to 10V rms	*	*
ALLOWABLE PHASE SHIFT (SIGNAL TO REFERENCE)	±20° Will Give No Additional Static Error	*	*
TRACKING RATE	100 Revolution or Pitches Per Second Minimum	*	50 Revolution or Pitches Per Second Minimum
SETTLING TIME (179° Step)	20ms max	*	40ms max
ACCELERATION CONSTANT (K_a)	650,000/sec/sec	*	159,878
BUSY OUTPUT	Logic "Hi" When BUSY 1μs max 1LS TTL Load	*	*
INHIBIT INPUT	Logic "Lo" to INHIBIT 1LS TTL Load	*	*
POWER SUPPLIES	$+V_S$ +12V to +15V @ 10mA $-V_S$ −12V to −15V @ 10mA +5V @ 3mA	* * *	* * *
POWER DISSIPATION	0.320 Watts	*	*
TEMPERATURE RANGE	0 to +70°C Operating −60°C to +150°C Storage	−55°C to +125°C Operating *	* *
PACKAGE TYPE[2]	HY32J	HY32B	*
WEIGHT	1 oz (28 grams)	*	*

NOTES
[1]Accuracy applies over the operating range and for ±10% signal and reference voltage and frequency variation. ±5% power supply variation.
[2]See Section 19 for package outline information.
*Specifications same as IRDC1732/560.
Specfications subject to change without notice.

OPERATION OF THE CONVERTER

The IRDC1732 is a tracking converter. This means that the output automatically follows the input for speeds up to and including 100 rps. There is no requirement for a convert command as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter is indicated by a BUSY pulse.

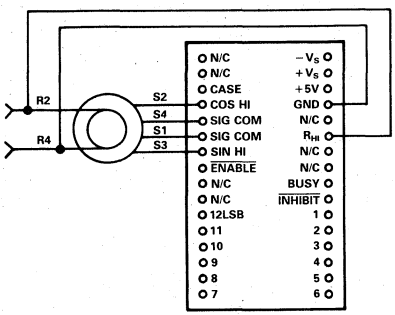


Figure 1.

CONNECTING THE CONVERTER

The electrical connection of the converter is straightforward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin potential.

The resolver connection S1 through S4 are made to the sine and cosine inputs as shown in the IRDC1732 electrical connection diagram, Figure 1.

It is suggested that decoupling capacitors of $0.1\mu F$ and $6.8\mu F$ are connected in parallel between the power supply lines ($+V_S$, $-V_S$ and $+5V$) and GND adjacent to the converter. When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter.

THEORY OF OPERATION

The sine and cosine signals are applied to the signal input.

$$V_1 = K\ E_O \sin \omega t \sin \theta$$
$$V_2 = K\ E_O \sin \omega t \cos \theta$$

Where θ is the angle of the resolver shaft or the distance through a particular pitch of the Inductosyn.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K\ E_O \sin \omega t \sin \theta \cos \phi$$
and $$K\ E_O \sin \omega t \cos \theta \sin \phi$$

These signals are subtracted by the error amplifier to give:

$$K\ E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$$
or $$K\ E_O \sin \omega t \sin (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals within the rated accuracy of the converter, the resolver shaft angle θ.

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB)	0.0879

Bit Weight Table

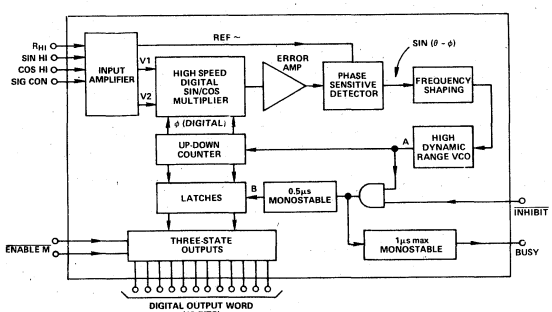


Figure 2. Functional Diagram

DATA TRANSFER

The readiness of the converter for data transfer is given by the state of the BUSY output. The signal appearing on the BUSY output pin is a series of pulses of TTL levels when the angular input of the converter is changing. A BUSY pulse is initiated each time the input moves by an LSB and the internal counter is incremented or decremented. With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

The $\overline{\text{ENABLE}}$ input pin state determines the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins.

From the above it can be seen that there are two methods available for transferring data.

The first is to detect the state of the BUSY which is "Hi" for 1μs max and transfer the data when BUSY is "Lo". Both $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ must be in their correct state of "Hi" and "Lo" respectively to present data to the output.

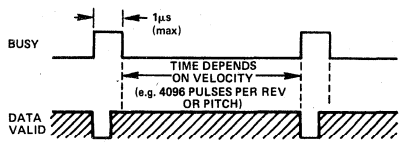


Figure 3.

The alternative method is to use the $\overline{\text{INHIBIT}}$ input. As can be seen from the functional diagram, application of the $\overline{\text{INHIBIT}}$ prevents the two internal monostable circuits being triggered and consequently the latches being updated. Data will always be valid 1μs after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is true regardless of the time when $\overline{\text{INHIBIT}}$ is applied.

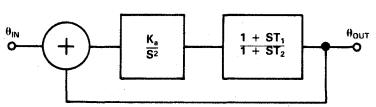
The three state $\overline{\text{ENABLE}}$ can be used at any time to present the data in the latches to the output pins.

The internal operation of the converter cannot be affected by the logic state present on either the $\overline{\text{ENABLE}}$ or $\overline{\text{INHIBIT}}$ input pins.

Use of the BUSY pulses output as an incremental counter input is not recommended as the BUSY output signals a change of output irrespective of direction.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

IRDC1732/560 and IRDC1732/460

$k_a = 650{,}000$
$T_1 = 2.3\text{ms}$
$T_2 = 0.4\text{ms}$

IRDC1732/410

$k_a = 159{,}878$
$T_1 = 3.7\text{ms}$
$T_2 = 0.7\text{ms}$

ACCELERATION ERROR

A tracking converter like the IRDC1732 employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$k_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure (deg/sec^2).

An example using the K_a of the IRDC1732/500.

Acceleration of 50 revolutions sec^{-2} with $K_a = 650{,}000$

$$\text{error in LSB's} = \frac{50 \times 4096}{650{,}000} = 0.3\text{LSB}.$$

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITION
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

PIN FUNCTION DESCRIPTION

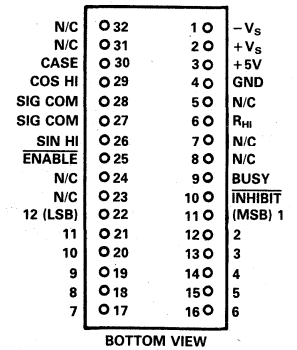
$-V_S$	Main negative power supply −12V dc to −15V dc.
$+V_S$	Main positive power supply +12V dc to +15V dc.
+5V	Logic voltage.
GND	Power supply ground. Digital ground. Reference voltage low.
Bit 1-12	Parallel output data bits 1MSB = 180°.
Sin Hi Cos Hi	Input analog signals.
R_{HI}	Reference voltage input HI. Reference low connects to GND.
$\overline{\text{INHIBIT}}$	Inhibit logic input. Taking this pin "lo" inhibits data transfer from counter to output latches. The conversion loop continues to track.
BUSY	Converter BUSY. A "Hi" output indicates that the the output latches are being updated. Data should not be transferred from the converter output while BUSY is "Hi".
$\overline{\text{ENABLE}}$	The output data bits are set to a low impedance state by application of a logic "lo".
CASE	This should normally be grounded. Case can be be taken to any voltage with a low impedance up ±20V.
N/C	Pins designated N/C not connected internally.
SIG COM	Internally connected to GND.

ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
$+5V$[2]	0V to +5.5V
R_{HI} to GND	±20V dc
Sin Hi/Cos Hi	±20V dc
Case to	±20V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:
1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

PIN CONFIGURATION



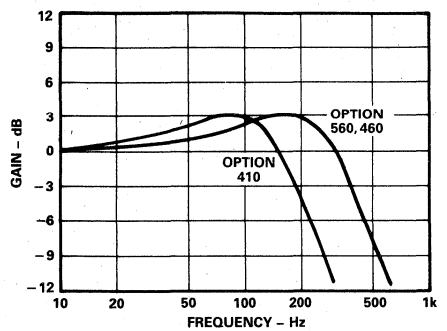


Figure 4. Magnitude of Gain vs. Frequency

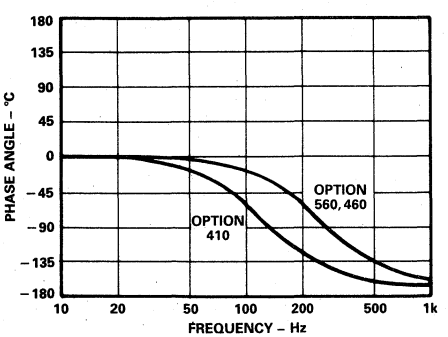


Figure 5. Output Angular Phase vs. Frequency

13

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

An example of the MTBF results: IRDC1732 at Naval Sheltered conditions 50°C = 974,000 hours or 111 years (410,460 options).

ORDERING INFORMATION

IRDC1732 X Y 0

Inductosyn/Resolver-to-Digital Converter

Y = 1 400Hz Reference Frequency

Y = 6 1kHz to 10kHz Reference Frequency

X = 4 −55°C to +125°C Operating Temperature Range

X = 5 0 to +70°C Operating Temperature Range

ANALOG DEVICES

12- and 14-Bit Hybrid Synchro/ Resolver-to-Digital Converters

SDC/RDC1740/1741/1742

FEATURES
Internal Isolating Transformers
14-Bit or 12-Bit Resolution
Three Accuracy Options
Three-State Latched Output
Continuous Tracking—Even During Data Transfer
Simple Data Transfer
Laser Trimmed—No External Adjustments
Hi Rel Options Available
Hermetically Sealed

APPLICATIONS
Avionic Systems
Servo Mechanisms
Coordinate Conversion
Axis Transformation
Antenna Monitoring
Artillery Fire Control Systems
Engine Controllers

GENERAL DESCRIPTION

The SDC1740, SDC1741 and SDC1742 are hybrid, continuous tracking synchro or resolver to digital converters which employ a type 2 servo loop and contain three-state latches on the digital outputs.

The input signals can either be 3-wire synchro plus reference or 4-wire resolver format plus reference depending on the option; and the outputs are presented in TTL compatible parallel natural binary buffered by three-state latches.

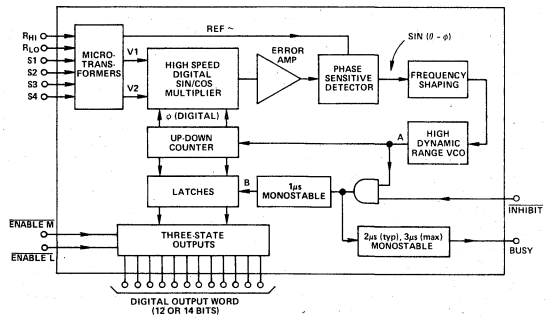
The three-state output facility, which has separate $\overline{\text{ENABLE}}$ inputs for the most significant 8 bits and the least significant 4 bits (or 6 bits in the case of the SDC1740), not only simplifies multiplexing of more than one device onto a single data bus, but also enables the $\overline{\text{INHIBIT}}$ to be used without opening the internal converter loop.

An outstanding feature of these converters is that although the profile height is only 0.28 inches (7.1mm) they contain internal transformers which provide for true isolation on the signal and reference inputs.

The converters are hermetically sealed in a metal 32-pin dual-in-line package.

To ensure a high level of reliability each converter receives a stringent pre-cap visual inspection, constant acceleration and final electrical test.

SDC/RDC1740/1741/1742 FUNCTIONAL BLOCK DIAGRAM



MODELS AVAILABLE

The three synchro/resolver-to-digital converters described in this data sheet differ primarily in the areas of resolution, accuracy and dynamic performance as follows:

Model SDC1740XYZ is a 14-bit converter with an overall accuracy of ±5.3 arc minutes and a resolution of 1.3 arc minutes.

Model SDC1741XYZ is a 12-bit converter with an overall accuracy of ±15.3 arc minutes and a resolution of 5.3 arc minutes.

Model SDC1742XYZ is a 12-bit converter with an overall accuracy of ±8.5 arc minutes and a resolution of 5.3 arc minutes.

Each model has two operating temperature range versions, those covering the industrial temperature range (0 to +70°C) and the extended temperature range (−55°C to +125°C).

The XYZ code defines the option as follows: (X) signifies the operating temperature range, (Y) signifies the reference frequency, (Z) signifies the signal and reference voltage and whether it will accept synchro or resolver format.

More information about the option codes is given under the heading of "Ordering Information".

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SPECIFICATIONS (typical @ +25°C unless otherwise specified)

Models	SDC/RDC1740	SDC/RDC1741	SDC/RDC1742
ACCURACY[1,2]	±5.3 arc min	±15.3 arc min	±8.5 arc min
RESOLUTION	14 Bits (1LSB = 1.3 arc min)	12 Bits (1LSB = 5.3 arc min)	** **
OUTPUT	14-Bits Parallel Natural Binary	12-Bit Parallel Natural Binary	**
SIGNAL & REFERENCE FREQUENCY	400Hz or 2.6kHz	*	*
SIGNAL VOLTAGE (Line-to-Line)	90V, 26V or 11.8V	*	*
SIGNAL INPUT IMPEDANCE			
90V Signal	200k (Resistive)	*	*
26V Signal	57.7k (Resistive)	*	*
11.8V Signal	26k (Resistive)	*	*
REFERENCE VOLTAGE	115V, 26V or 11.8V rms	*	*
REFERENCE IMPEDANCE			
115V Reference	120k (Resistive)	*	*
26V Reference	27k (Resistive)	*	*
11.8V Reference	12.3k (Resistive)	*	*
TRANSFORMER ISOLATION	350V dc	*	*
TRACKING RATE (min)	12 R.P.S.	18 R.P.S.	**
ACCELERATION CONSTANT (K_a)	39,000/sec^2	82,000/sec^2	**
STEP RESPONSE (179° Step for Settling to 1LSB of Error)	150ms	100ms	100ms
POWER LINES			
+15V	14mA (typ) 17mA (max)	19mA (typ) 23mA (max)	**
−15V	14mA (typ) 16mA (max)	19mA (typ) 23mA (max)	**
+5V	60mA (typ) 72mA (max)	45mA (typ) 110mA (max)	**
POWER DISSIPATION	0.72 Watts (typ) 0.86 Watts (max)	0.8 Watts (typ) 1.3 Watts (max)	** **
DATA LOGIC OUTPUT[3]	6 TTL Loads	*	*
BUSY OUTPUT LOGIC LOADING[3]	2 TTL Loads	*	*
BUSY LOGIC OUTPUT WIDTH	1.2μs (typ) 3μs (max)	*	*
INHIBIT INPUT (to INHIBIT)	Logic "0" 1 TTL Load	*	*
ENABLE INPUTS (to ENABLE)[4]	Logic "0" 1 TTL Load	*	*
TEMPERATURE RANGE	Option 5YZ Option 4YZ		
Operating Range	0 to +70°C −55°C to +125°C	*	*
Storage Range	−65°C to +150°C *	*	*
PACKAGE TYPE[5]	Hermetic DIP HY32B	* *	* *
WEIGHT	0.8 oz (23 grams)	*	*

NOTES
[1]Specified over the appropriate operating temperature range and for: (a) ± 10% signal and reference amplitude variation; (b) 10% signal and reference harmonic distortion; (c) ± 5% power supply variation; (d) ± 10% variation in reference frequency.
[2] 2.6kHz options accuracy decreases 1 × 1.3 arc min on SDC/RDC1740.
[3]Schottky logic loading rules apply.
[4]ENABLE M enable most significant 8 bits
ENABLE L enable least significant 4 bits (or 6 bits for SDC/RDC1740).
[5]See Section 19 for package outline information.
*Specifications same as SDC/RDC1740.
**Specifications same as SDC/RDC1741.
Specifications subject to change without notice.

THEORY OF OPERATION

If the unit is a synchro-to-digital converter the 3-4 wire synchro output will be connected to S1, S2 and S3 on the unit and the Scott T transformer pair will convert these signals into resolver format.

i.e., $V_1 = K E_O \sin \omega t \sin \theta$
$V_2 = K E_O \sin \omega t \cos \theta$

Where θ is the angle of the synchro shaft.

If the unit is a resolver-to-digital converter, the 4-wire resolver output will be connected to S1, S2, S3 and S4 on the unit and the transformers will act purely as isolators.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

The V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$K E_O \sin \omega t \sin \theta \cos \phi$
and $K E_O \sin \omega t \cos \theta \sin \phi$

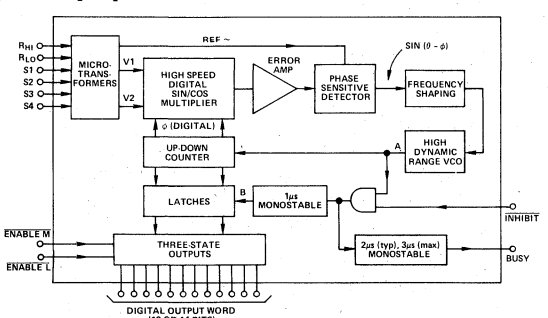
These signals are subtracted by the error amplifier to give:

$K E_O \sin \omega t (\sin \theta \cos \phi - \cos \theta \sin \phi)$
or $K E_O \sin \omega t \sin (\theta - \phi)$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals within the rated accuracy of the converter, the synchro shaft angle θ.

Assuming that the "$\overline{\text{INHIBIT}}$" is at a logic high state, then the digital word θ will be strobed into the latches 1μs after the updown counter has been updated. If the three state "$\overline{\text{ENABLE}}$" is at a logic low, then the digital output word will be presented to the output pins of the unit.



Functional Diagram of the SDC/RDC1740/1741/1742

DATA TRANSFER

Data transfer from the converters is straightforward.

Consider the timing sequence shown in the timing diagram which assumes that the input to the converter is changing.

From this diagram, it can be seen that there are two ways to transfer data.

One method is to detect the state of the BUSY signal, which is high for up to 1.2μs (typical) while the updown counters and latches are settling, and transfer data when it is in a low state.

An alternative method is to use the $\overline{\text{INHIBIT}}$ input. As can be seen from the functional diagram, application of the $\overline{\text{INHIBIT}}$ prevents the two monostables being triggered and consequently the latches being updated. Therefore, it follows that data will always be valid after 3μs has elapsed from the application of the $\overline{\text{INHIBIT}}$ (i.e., taken to logic low). It can also be seen that this method of data transfer is valid regardless of when $\overline{\text{INHIBIT}}$ is applied.

The three-state $\overline{\text{ENABLE}}$ can be used at any time in order to present the data in the latches to the output pins. $\overline{\text{ENABLE M}}$ enables the most significant 8 bits while $\overline{\text{ENABLE L}}$ enables the least significant 4 bits (6 bits in the SDC/RDC1740).

Note that the operation of the internal converter loop cannot be affected in any way by the logic state present on the $\overline{\text{INHIBIT}}$ and $\overline{\text{ENABLE}}$ pins.

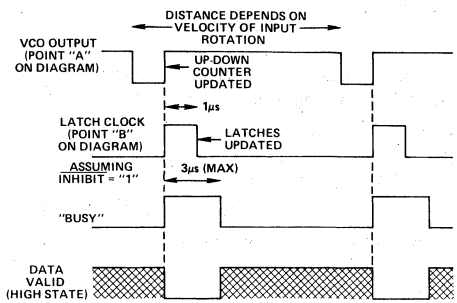


Figure 1. Timing Diagram

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12 (LSB) for 1741/42	0.0879
13	0.0439
14 (LSB) for 1740	0.0220

Table I. Bit Weight Table

CONNECTING THE CONVERTER

The electrical connections to the converter are straightforward. The power lines, which must not be reversed, should be connected to the "+15V", "−15V" and "+5V" pins with the common connection to the ground pin "GND". It is suggested that a parallel combination of a 0.1μF and a 6.8μF capacitor is placed in each of the three positions from "+15V" to "GND", from "−15V" to "GND" and from "+5V" to "GND".

The pin marked "case" is connected electrically to the case and should be taken to a convenient zero volt potential in the system.

The digital output is taken from pin "1" through to pin "12" for the SDC/RDC1741/1742 and pin "1" through to pin "14" for the SDC/RDC1740 where pin "1" is the MSB.

The reference connections are made to "R_{HI}" and "R_{LO}".

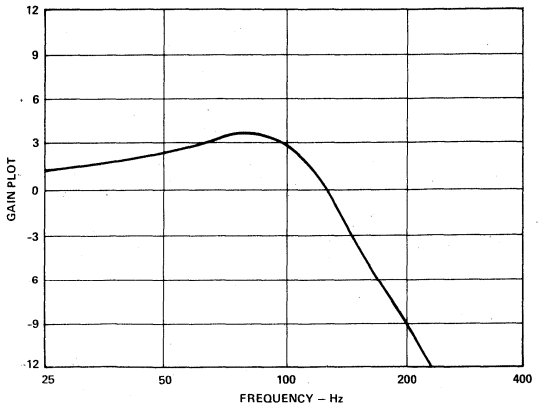


Figure 2.

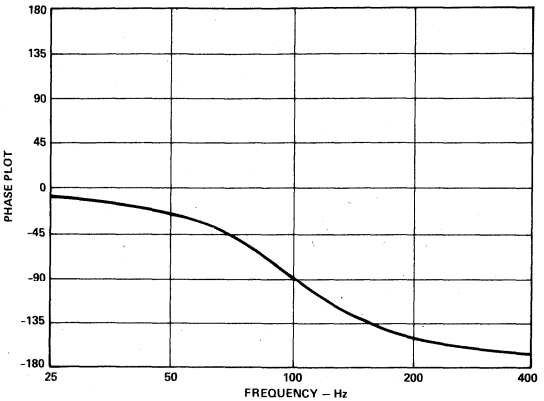


Figure 3.

In the case of a synchro, the signals are connected to "S1", "S2" and "S3" according to the folowing convention:

$E_{S1-S3} = E_{RL0-RHI}$ Sin ωt Sin θ
$E_{S3-S2} = E_{RL0-RHI}$ Sin ωt Sin (θ + 120°)
$E_{S2-S1} = E_{RL0-RHI}$ Sin ωt Sin (θ + 240°)

For a resolver, the signals are connected to "S1", "S2", "S3" and "S4" according to the following convention:

$E_{S1-S3} = E_{RL0-RHI}$ Sin ωt Sin θ

$E_{S2-S4} = E_{RHI-RLO}$ Sin ωt Cos θ

The "BUSY", "$\overline{\text{INHIBIT}}$" and "$\overline{\text{ENABLE}}$" pins should be connected as described under the heading "Data Transfer".

RESISTIVE SCALING OF INPUTS

A feature of these converters is that the signal and reference inputs can be resistively scaled to accommodate any range of input signal and reference voltages.

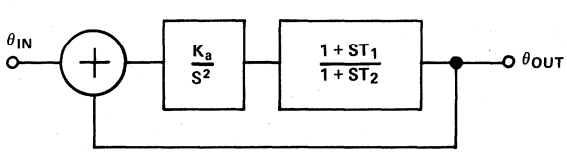
This means that a standard converter can be used with a personality card in systems where a wide range of input and reference voltages are encountered.

To calculate the values of the external scaling resistors in the case of a synchro converter, add 1.11kΩ per extra volt of signal in series with "S1" , "S2" and "S3", and 1kΩ per extra volt of reference in series with "R_{HI}".

In the case of a resolver-to-digital conveter, add 2.22kΩ in series with "S1" and "S2" per extra volt of signal and 1kΩ per extra volt of reference in series with "R_{HI}".

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

Model SDC/RDC1741/1742

where $k_a = 82{,}000$
$T_1 = 0.0086$
$T_2 = 0.0015$

Refer: – Figures 2 and 3

Model SDC/RDC1740

where $k_a = 39{,}000$
$T_1 = 0.013$
$T_2 = 0.002$

Refer: – Figures 4 and 5

ACCELERATION ERROR

A tracking converter employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$k_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 5 times the K_a figure.

An example using the K_a of the SDC1742.

Acceleration of 50 revolutions sec^{-2} with $K_a = 82{,}000$

$$\text{error in LSB's} = \frac{50 \times 4096}{82{,}000} = 2.5\text{LSB}.$$

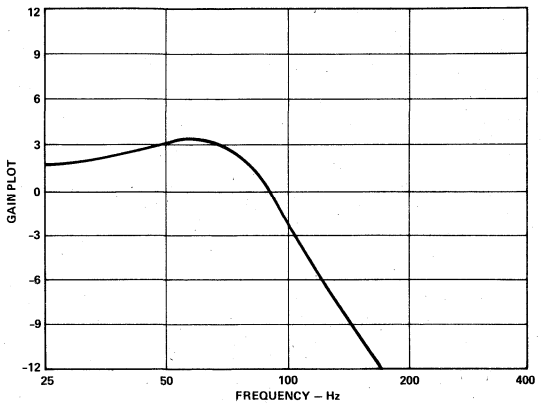


Figure 4.

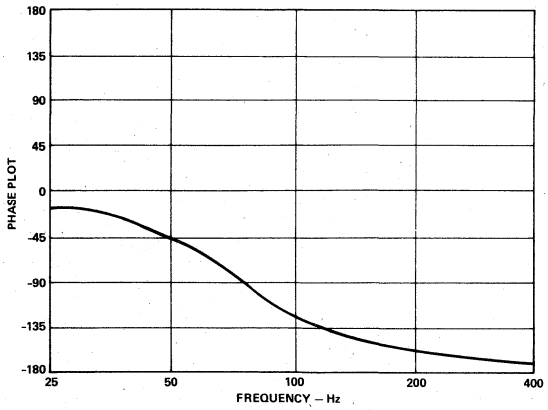


Figure 5.

ABSOLUTE MAXIMUM INPUTS

$+V_S$[1] to GND	0V to +17V dc
$-V_S$[1] to GND	0V to −17V dc
$+5V$[2]	0V to +5.5V dc
R_{HI} to GND	±350V dc
S_1, S_2, S_3, S_4 to GND	±350V dc
Case to GND	±20V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

OTHER PRODUCTS

Many other hybrid products concerned with the conversion of synchro data are manufactured by us, some of which are listed below. If you have any questions about our products or require advice about their use for a particular application, please contact our Applications Engineering Department.

The *IRDC1732* is a low cost hybrid Inductosyn™ or resolver-to-digital converter with a tri-state latched 12-bit natural binary output.

The *DRC1745* and *DRC1746* are 14- and 16-bit natural binary latched output hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins., and the outputs can supply 2VA at 7V rms.

The *DRC1765* and *DRC1766* are 14- and 16-bit natural binary latched input hybrid digital-to-resolver converters. The accuracies available are ±2 and ±4 arc mins., and the outputs of ±10V can supply 4.3mA peak.

The *SDC/RDC1767* and *1768* are hybrid synchro-to-digital converters with transformer isolation similar to the SDC1740/41 and 42 described on this data sheet with the additional features of analogue velocity output, dc error output and enhanced dynamic characteristics.

As well as this range of hybrid converters we manufacture an extensive range of modular products for synchro data conversion, with operating temperature ranges of 0 to +70°C and −55°C to +105°C.

Inductosyn is a registered trademark of Farrand Industries, Inc.

RELIABILITY

The reliability of these products is very high due to the extensive use custom chip circuits that decreases the active components.

Calculations of the MTBF figure under various environmental conditions are available on request.

As an example of the Mean Time Between Failures (MTBF) calculated according to MIL-HDBK-217D, the curve below shows the MTBF in years versus case temperature in Naval Sheltered conditions for SDC1742.

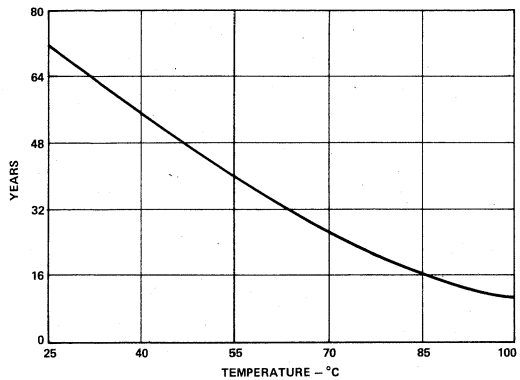


Figure 6.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

As part of the standard manufacturing procedure, all converters receive the following processing:

PROCESS	CONDITIONS
1. Pre-Cap Visual Inspection	In-House Criteria
2. Constant Acceleration	5000G
3. Final Electrical Test	Performed at 25°C

Extended temperature range versions receive additional processing as follows:

Burn-In	160 hrs at 125°C
Gross Leak Test	In-House Criteria

ORDERING INFORMATION

When ordering, the converter part numbers should be suffixed by an option code in order to fully define them. All the standard options and their option codes are shown below. For options not shown, please consult the factory.

SDC 1740 X Y Z

SDC = Synchro-to-Digital Converter
RDC = Resolver to Digital Converter

1740 = 14-Bit Resolution, ± 5.3 arc min Accuracy
1741 = 12-Bit Resolution, ± 15.3 arc min Accuracy
1742 = 12-Bit Resolution, ± 8.5 arc min Accuracy

Z = 1	Signal	11.8V	Reference	26V Synchro
Z = 2	Signal	90V	Reference	115V Synchro
Z = 3	Signal	11.8V	Reference	11.8V Resolver
Z = 4	Signal	26V	Reference	26V Resolver
Z = 8	Signal	11.8V	Reference	26V Resolver

Y = 1 400Hz Reference Frequency
Y = 4 2.6kHz Reference Frequency

X = 4 −55°C to +125°C Operating Temperature Range
X = 5 0 to +70°C Operating Temperature Range

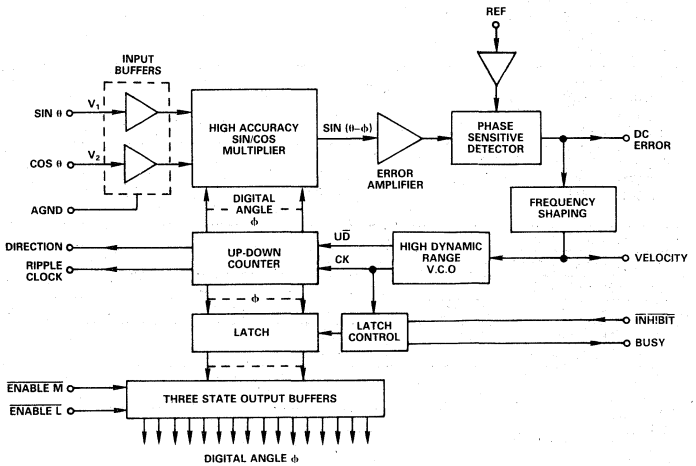
Hybrid, Tracking Resolver-to-Digital Converters

1S20/1S40/1S60/1S61

FEATURES
Low Cost
32-Pin Hybrid
High Tracking Rate 170rps at 12 Bits
Velocity Output
DC Error Output
Logic Outputs for Extension Pitch Counter

APPLICATIONS
Numerical Control of Machine Tools
Robotics

1S20/1S40/1S60/1S61 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The 1S20/40/60/61 are a series of low cost hybrid converters with a high tracking rate and all essential features for numerically controlled machine applications. These converters are housed in a 32-pin triple DIP ceramic package measuring 1.1″ × 1.7″ × 0.205″ (28 × 43.2 × 5.2mm).

The 1S20/40/60/61 convert resolver format input signals into a parallel natural binary digital word. Typically, these signals would be obtained from a brushless resolver and the resolver/converter combination gives a parallel absolute angular output word similar to that provided by an absolute encoder. The ratiometric conversion principle of the 1S20/40/60/61 series ensures high noise immunity and tolerance of lead length when the converter is at a distance from the resolver.

The output word is in three-state digital logic form with a high and low byte enable input so that the converter can communicate with an 8- or 16-bit digital highway. In this series there are 12-, 14- and two 16-bit resolution (±4 arc mins and ±10 arc mins accuracy) models available.

Repeatability is 1LSB for all models under constant temperature conditions.

The 1S20/40/60/61 are available with three frequency options covering the range 400Hz to 10kHz.

Models Available
Four models are available in this range and three frequency options for each model.

1S20 is a 12-bit up to 170 revolutions per second
1S40 is a 14-bit up to 42.5 revolutions per second
1S60 is a 16-bit up to 10.5 revolutions per second
1S61 is a 16-bit up to 10.5 revolutions per second

APPLICATIONS/USER BENEFITS

The 1S20/40/60/61 has been specifically designed for the numerically controlled machine and robot industry. Using the type 2 servo loop tracking principle ideally suits these converters to the electrically noisy environment found in these industrial applications.

By using hybrid construction techniques, small size, low power and high reliability are further benefits offered by these converters. This small size with the three-state digital outputs makes these converters ideal for multichannel operation.

The layout of the connections simplifies the parallel connection to a digital highway.

The provision of the digital outputs of DIRECTION and RIPPLE CLOCK allow simple extension counters for multi-pitch operation to be implemented.

Analog outputs of velocity and dc error for control loop stabilization and bite (built in test) provide two more features required in these applications.

SPECIFICATIONS (typical @ +25°C, unless otherwise specified)

Models	1S20	1S40	1S60	1S61	Units
RESOLUTION	12	14	16	16	Bits
ACCURACY[1]	±8.5	±5.3	±4.0	±10	arc-mins
REPEATABILITY[2]	1	*	*	*	LSB
SIGNAL AND REFERENCE FREQUENCY[3]	400-10k	*	*	*	Hz
DIGITAL OUTPUT	Parallel natural binary				
Max Load	20	*	*	*	LSTTL
TRACKING RATE (min)					
400Hz – 2.6kHz	50	12.5	3.0	3.0	rps
2.6kHz – 5kHz	90	22.5	5.5	5.5	rps
5kHz – 10kHz	170	42.5	10.5	10.5	rps
SETTLING TIME					
400Hz – 2.6kHz	150	180	350	350	ms
2.6kHz – 5kHz	40	50	130	130	ms
5kHz – 10kHz	20	25	60	60	ms
ACCELERATION CONSTANT (K_a)					
400Hz – 2.6kHz	9,500	*	*	*	sec^{-2}
2.6kHz – 5kHz	144,000	*	*	*	sec^{-2}
5kHz – 10kHz	713,000	*	*	*	sec^{-2}
SIGNAL VOLTAGE	2.0	*	*	*	V rms
SIGNAL INPUT IMPEDANCE	>10	*	*	*	MΩ
REFERENCE VOLTAGE	2.0	*	*	*	V rms
REFERENCE INPUT IMPEDANCE	125	*	*	*	kΩ
ALLOWABLE PHASE SHIFT[4]					
(Signal to Reference)	±10	*	*	*	Degrees
BUSY OUTPUT[5]	Logic "Hi" when Busy				
Max Load	20	*	*	*	LSTTL
BUSY WIDTH	430	*	*	*	ns
$\overline{\text{ENABLE}}$ INPUTS	Logic "Lo" to ENABLE				
Load	1	*	*	*	LSTTL
ENABLE AND DISABLE TIMES	120(typ)	*	*	*	ns
	220(max)	*	*	*	ns
$\overline{\text{INHIBIT}}$ INPUT	Logic "Lo" to INHIBIT	*	*	*	
Load	1	*	*	*	LSTTL
DIRECTION OUTPUT (DIR)[5]	Logic "Hi" when counting up Logic "Lo" when counting down				
Max Load	20	*	*	*	LSTTL
RIPPLE CLOCK[5]	Negative pulse indicating when internal counters change from all "1's" to all "0's" or vice versa.				
Max Load	20	*	*	*	LSTTL
VELOCITY OUTPUT[6] (at specified min tracking rate).					
Polarity	positive for increasing angle	*	*	*	–
Output Voltage[7]	±10	*	*	*	V dc
Accuracy	±10	*	*	*	% FSD
Zero Offset	±8	*	*	*	mV
DC ERROR OUTPUT VOLTAGE[6]	40	10	2.5	2.5	mV/LSB
POWER SUPPLIES					
$+V_S$	+11.5 to +16	*	*	*	V
$-V_S$	−11.5 to −16	*	*	*	V
+5V	+4.75 to +5.25	*	*	*	V
POWER SUPPLY CONSUMPTION[7]					
$+V_S$	20, 30 (max)	*	*	*	mA
$-V_S$	20, 30 (max)	*	*	*	mA
+5V	105, 125 (max)	*	*	*	mA
POWER DISSIPATION[7]	1.1, 1.5 (max)	*	*	*	W
TEMPERATURE RANGE					
Operating	0 to +70	*	*	*	°C
Storage	−55 to +125	*	*	*	°C
PACKAGE TYPE[8]	HY32J	*	*	*	
WEIGHT	1(28)	*	*	*	oz. (grms)

NOTES

[1]Specified over the operating temperature range and for:
a). ±10% signal and reference amplitude variation.
b). 10% signal and reference harmonic distortion.
c). ±10% on frequency range of option.

[2]Specified at constant temperature. Over the operating temperature range, worst case repeatability could be up to 1.5 Arc Mins for all models.

[3]See frequency range options.

[4]For no additional error with a static input, see "Dynamic Accuracy vs. Resolver Phase Shift".

[5]See timing diagram.

[6]These outputs should be connected via buffers or comparator inputs (max load 100pF).

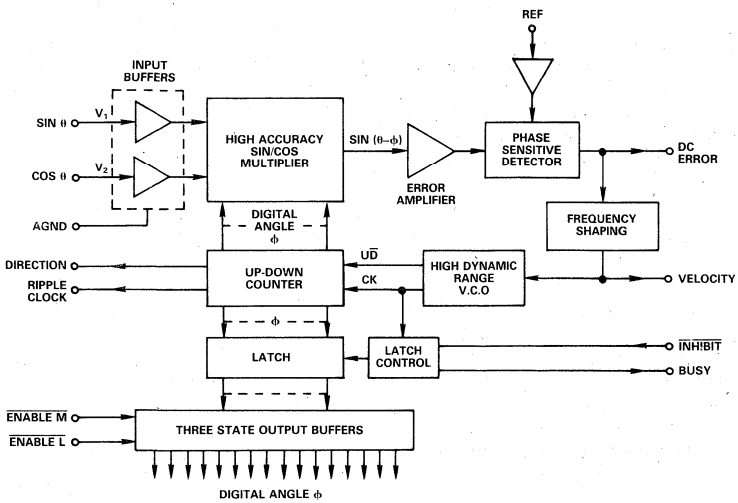
[7]$\pm V_S = \pm 15$ volts.

[8]See Section 19 for package outline information.

*Specifications same as 1S20.

Specifications subject to change without notice.

FUNCTIONAL DIAGRAM



BIT WEIGHT TABLE

Bit Number	Weight in Degrees
1 (MSB)	180.0000
2	90.0000
3	45.0000
4	22.5000
5	11.2500
6	5.6250
7	2.8125
8	1.4063
9	0.7031
10	0.3516
11	0.1758
12	0.0879
13	0.0440
14	0.0220
15	0.0110
16	0.0055

THEORY OF OPERATION

The sine and cosine signals are applied to the signal input.

$$V_1 = K E_O \text{ Sin } \omega t \text{ Sin } \theta$$
$$V_2 = K E_O \text{ Sin } \omega t \text{ Cos } \theta$$

Where θ is the angle of the resolver shaft or the distance through a particular pitch of the Inductosyn™.

To understand the conversion process, then assume that the current word state of the up-down counter is ϕ.

V_1 is multiplied by Cos ϕ and V_2 is multiplied by Sin ϕ to give:

$$K E_O \text{ Sin } \omega t \text{ Sin } \theta \text{ Cos } \phi$$
and $$K E_O \text{ Sin } \omega t \text{ Cos } \theta \text{ Sin } \phi$$

These signals are subtracted by the error amplifier to give:

$$K' E_O \text{ Sin } \omega t \text{ (Sin } \theta \text{ Cos } \phi - \text{Cos } \theta \text{ Sin } \phi)$$
or $$K' E_O \text{ Sin } \omega t \text{ Sin } (\theta - \phi)$$

A phase sensitive detector, integrator and Voltage Controlled Oscillator (VCO) form a closed loop system which seeks to null Sin $(\theta - \phi)$.

When this is accomplished, the word state of the up-down counter (ϕ), equals, within the rated accuracy of the converter, the resolver shaft angle θ.

OPERATION OF THE CONVERTER

The 1S20/40/60/61 are tracking converters, this means that the output automatically follows the input for speeds up to the maximum tracking rate for the frequency option specified. No convert command is necessary as the conversion is initiated by each LSB increment of the input. Each LSB increment of the converter initiates a BUSY pulse.

As the digital output of the converter passes through the major carry; i.e., all "1's" to all "0's" or the converse, a RIPPLE CLOCK (RC) logic output is initiated indicating that a revolution or a pitch of the input has been completed.

The direction of input rotation is indicated by the DIRECTION (DIR) logic output. This direction data is *always* valid in advance of a RIPPLE CLOCK pulse.

The $\overline{\text{INHIBIT}}$ logic input only inhibits the data transfer from the up-down counter to the output latches and therefore does not interrupt the operation of the tracking loop. Releasing the $\overline{\text{INHIBIT}}$ automatically generates a BUSY pulse to refresh the output data.

Two $\overline{\text{ENABLE}}$ inputs are provided, $\overline{\text{ENABLE M}}$ for the Most Significant 8 bits and $\overline{\text{ENABLE L}}$ for the Least Significant remainder. The operation of these enables has no effect on the conversion process.

The tracking conversion technique produces an internal signal at the input to the VCO that is proportional to the rate of the input angle. This is a bipolar dc analog signal that is made available at the VELOCITY (VEL) pin. As this is an internal control signal it is not closely characterized.

The signal at the output of the phase sensitive detector is the input to the internal nulling loop and hence is proportional to the error between the input angle and the output digital angle. As the converter is a type 2 servo loop, this DC ERROR signal will increase if the output angle fails to track the input for any reason, it is therefore an indication that the input has exceeded the maximum tracking rate of the converter or due to some internal malfunction, the converter is unable to reach a null. By the use of two external comparators this voltage can be used as a "built in test".

NOTE: The DC ERROR voltage has no internal filtering.

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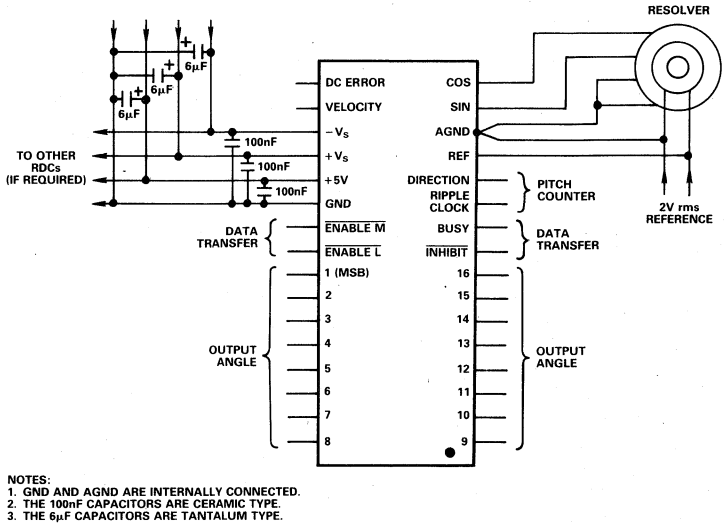


Figure 1. Electrical Connections

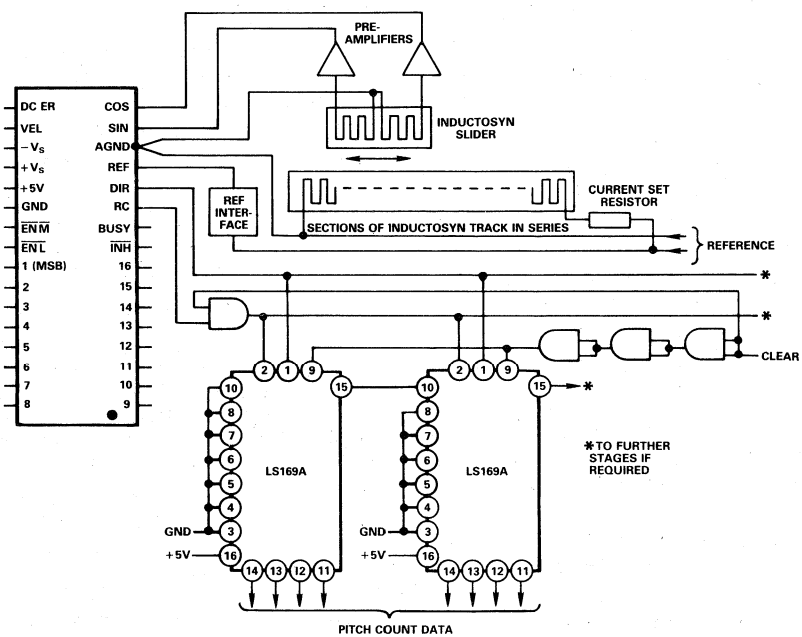


Figure 2. Connections for Use with Industosyn/"LS" External Counters

CONNECTING THE CONVERTER

The electrical connection of the converter is straight-forward. The power supply voltages connected to $+V_S$ and $-V_S$ pins can be $\pm 12V$ to $\pm 15V$ but must not be reversed. The $+5V$ supply connects to the $+5V$ pin and should not be allowed to become negative with respect to the GND pin.

It is suggested that decoupling capacitors of 100nF are connected in parallel between the power lines ($+V_S$, $-V_S$ and $+5V$) and GND adjacent to the converter.

When more than one converter is used on a card, then separate decoupling capacitors should be used for each converter (refer to Figure 1).

The converter has some H/F decoupling provided internally, as well as input protection on the signal and reference inputs.

The resolver connections are made to the sine and cosine inputs, reference and analog ground as shown in the electrical connection diagram (Figure 1).

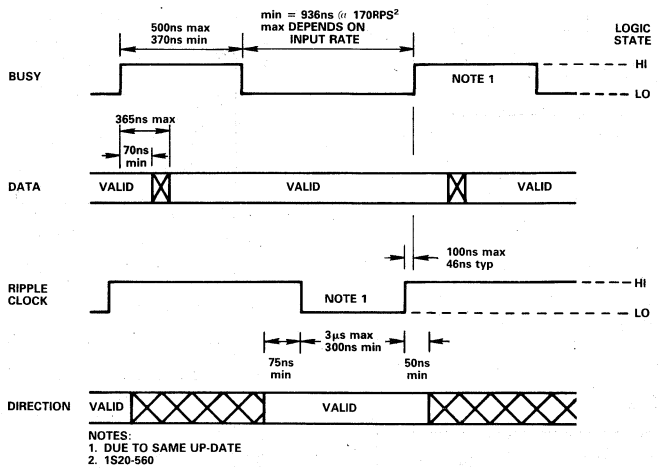


Figure 3. Timing Diagram

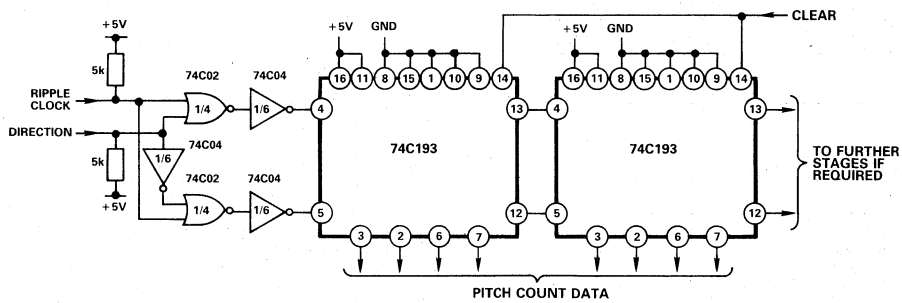


Figure 4. CMOS External Counter

DATA TRANSFER

The readiness of the converter for data transfer is given by the state of the BUSY output. The signal appearing on the BUSY output pin is a series of pulses of TTL levels when the angular input of the converter is changing. A BUSY pulse is initiated each time the input moves by an LSB and the internal counter is incremented or decremented. With the $\overline{\text{INHIBIT}}$ input pin in the "Hi" TTL state, data will be transferred automatically to the output latches.

The $\overline{\text{ENABLE}}$ input pin determines the state of the output data. A TTL logic "Hi" maintains the output data pins in a high impedance condition, the application of a logic "Lo" presents the data in the latches to the output pins.

From the above it can be seen that there are two methods available for transferring data.

One method is to transfer data when the BUSY is in a "Lo" state or clock the data out on the trailing edge of the BUSY pulse. Both the $\overline{\text{INHIBIT}}$ and the $\overline{\text{ENABLES}}$ must be in their correct state of "Hi" and "Lo's" respectively.

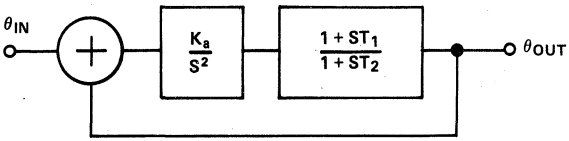
The alternative method is to use the $\overline{\text{INHIBIT}}$ input. Data will always be valid one microsecond after the application of a logic "Lo" to the $\overline{\text{INHIBIT}}$. This is regardless of the time when the $\overline{\text{INHIBIT}}$ is applied.

In order to count input revolutions or pitches, an external extension counter is required. A circuit performing this function is shown in Figure 2.

The DIRECTION (DIR) and RIPPLE CLOCK (RC) logic outputs should always be used in the manner shown in the application circuit. We recommend the circuit in Figure 2 to be used as the circuit in Figure 4 uses CMOS and great care must be taken to keep the stray capacitances low because of the high tracking rate of the converter.

DYNAMIC PERFORMANCE

The transfer function of the converter is given below.



Open loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{K_a}{S^2} \cdot \frac{1 + ST_1}{1 + ST_2}$$

Closed loop gain:

$$\frac{\theta_{OUT}}{\theta_{IN}} = \frac{1 + ST_1}{1 + ST_1 + \frac{S^2}{K_a} + \frac{S^3 T_2}{K_a}}$$

1S20/1S40/1S60/1S61 (typical values)

Constant \ Option	510	550	560
K_a	9,500	144,000	713,000
T_1	17.4ms	4.1ms	1.85ms
T_2	2.6ms	0.6ms	0.25ms
Gain Plot	Figure 5	Figure 7	Figure 9
Phase Plot	Figure 6	Figure 8	Figure 10

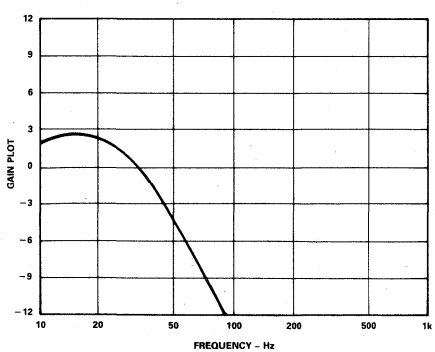


Figure 5

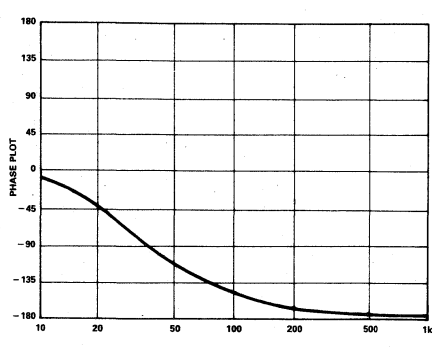


Figure 6

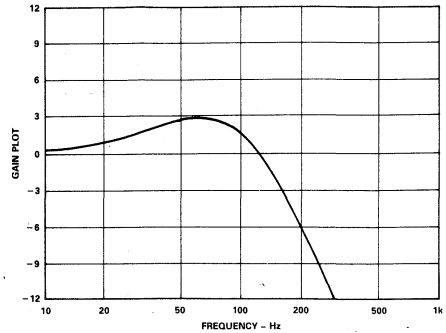


Figure 7

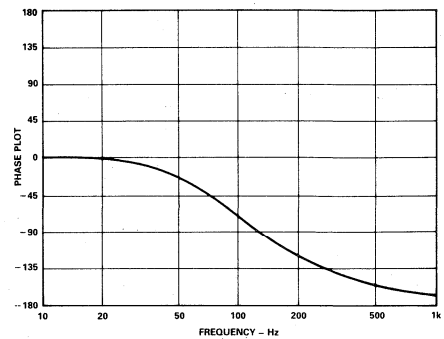


Figure 8

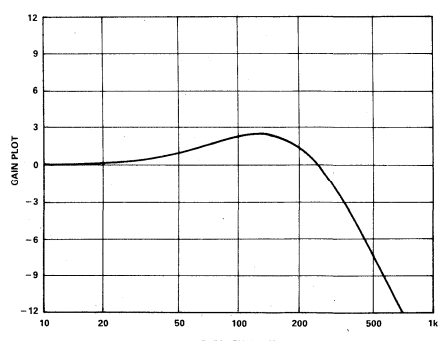


Figure 9

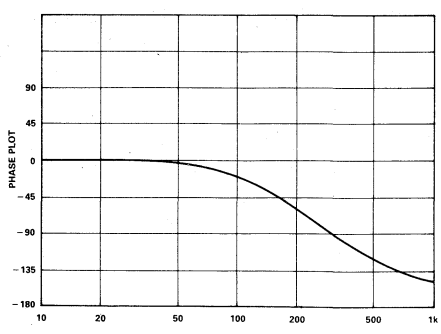


Figure 10

ACCELERATION ERROR

A tracking converter like the 1S20 employing a type 2 servo loop does not suffer any velocity lag, however, there is an additional error due to acceleration. This additional error can be defined using the acceleration constant K_a of the converter.

$$K_a = \frac{\text{Input acceleration}}{\text{Error in output angle}}$$

The numerator and denominator have the same units. K_a does not define maximum acceleration only the error due to acceleration, maximum acceleration is in the region of 10 times the K_a figure (deg/sec^2).

An example using the K_a of the 1S60/560

Acceleration of 33 revolutions sec^{-2} with K_a = 713,000

Additional error = 1 arc-min

DYNAMIC ACCURACY VS. RESOLVER PHASE SHIFT

Most resolvers, particularly those of the brushless type, exhibit a phase shift between the signal and the reference. This phase shift will give rise under dynamic conditions to an additional error defined by:

$$\frac{\text{Shaft Speed (RPS)} \times \text{Phase Shift (DEGS)}}{\text{Reference Frequency}}$$

For example, for a phase shift of 20°, a shaft rotation of 22rps and a reference frequency of 5kHz, the converter will exhibit an additional error of:

$$\frac{20 \times 22}{5000} = 0.088°$$

This effect can be eliminated by putting a phase shift in the reference to the converter equivalent to the phase shift in the resolver.

PROCESSING FOR HIGH RELIABILITY

STANDARD PROCESSING

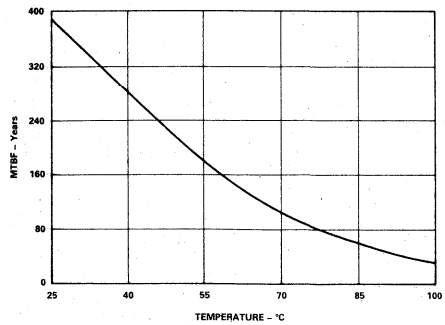
As part of the standard manufacturing procedure, all converters receive the following processing:

Process	Condition
1. Pre-Cap Visual Inspection	In-House Criteria
2. Burn-In	70°C
3. Constant Acceleration	5000G
4. Gross Leak Test	In-House Criteria
5. Final Electrical Test	Performed at 25°C

MEAN TIME BETWEEN FAILURES (MTBF)

The reliability of these products is very high due to the extensive use of custom chip circuitry. For details of MTBF figures under particular conditions please consult the factory.

The graph below shows the typical variation of MTBF with temperature for the 1S20, under ground benign environment.



ABSOLUTE MAXIMUM INPUTS (with respect to GND)

$+V_S$[1]	0V to +17V dc
$-V_S$[1]	0V to −17V dc
$+5V$[2]	0V to +7.0V dc
Reference	±17V dc
Sine	±17V dc
Cosine	±17V dc
Any Logical Input	−0.4V to +5.5V dc

CAUTION:

1. Correct polarity voltages must be maintained on the $+V_S$ and $-V_S$ pins.
2. The +5 volt power supply must *never* go below GND potential.

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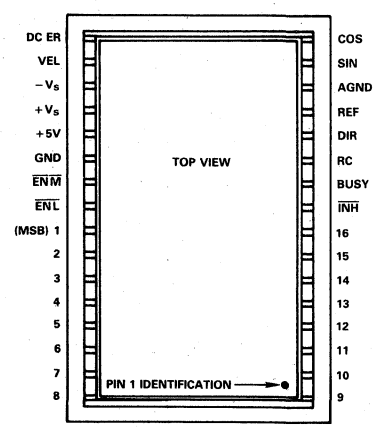
PIN CONFIGURATION



OTHER PRODUCTS

IRDC1732–	Inductosyn™/Resolver to Digital Converter (Hybrid)
IPA1751–	Inductosyn™ Pre-Amplifier
OSC1754–	Power Oscillator
OSC1758–	Power Oscillator (Hybrid)
IPA1764–	Inductosyn™ Pre-Amplifier (Hybrid)
MCI1794–	3 Channel Inductosyn™/Resolver to Digital Converter (Multibus Compatible Card)

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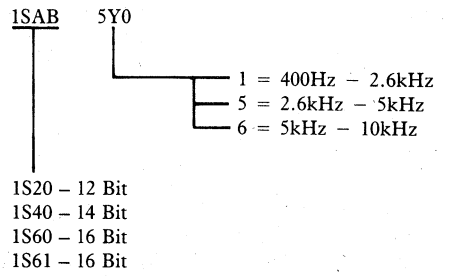
ORDERING INFORMATION



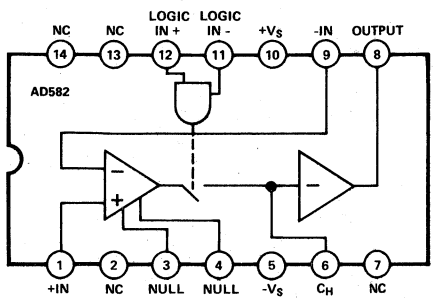
Sample/Track-Hold Amplifiers

Contents

•New product since publication of *1982–1983 Databook Update.*

Selection Guide
Sample/Track-Hold Amplifiers

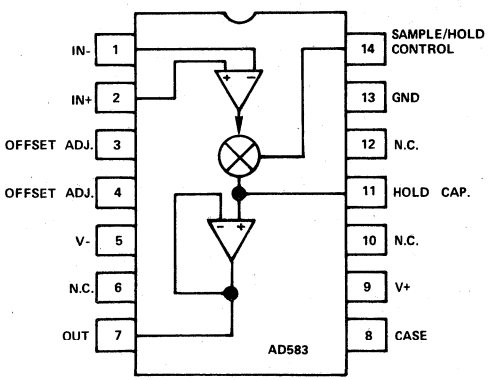
General Purpose



AD582

Page

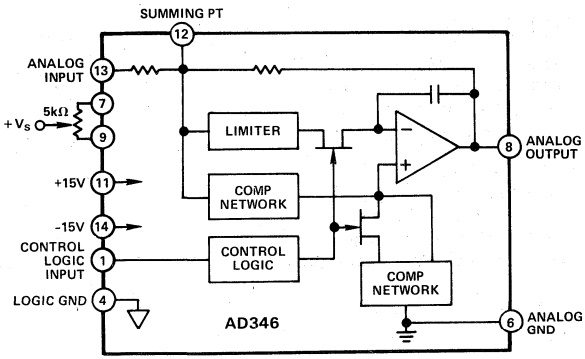
Suitable for 12-Bit Applications Vol. I
High Sample/Hold Current Ratio: 10^7 14–23
Low Acquisition Time: 6μs to 0.1%
Low Charge Transfer: <2pC
High Input Impedance in Sample and Hold Modes
Connect in Any Op Amp Configuration
Differential Logic Inputs



AD583

High Sample-to-Hold Current Ratio: 10^6 Vol. I
High Slew Rate: 5Vμs 14–27
High Bandwidth: 2MHz
Low Aperture Time: 50ns
Low Charge Transfer: 10pC
DTL/TTL Compatible
May Be Used as Gated Op Amp

High Speed



AD346

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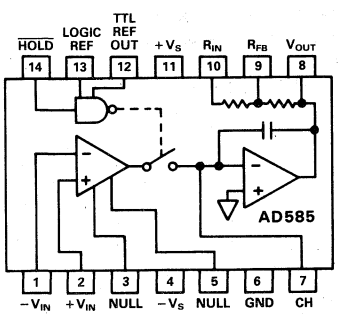
Vol. I
14-11

Fast 2.0μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor



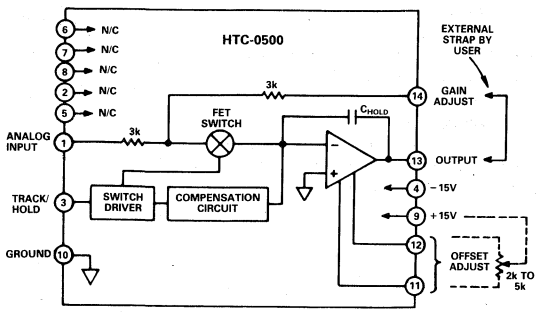
AD585

Vol. I
14-31

Fast 2.5μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset: 1mV
Sample/Hold Offset Step: 1mV
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements

Selection Guide
Sample/Track-Hold Amplifiers
High Speed



HTC-0500

700ns Acquisition Time
<750mW Power Dissipation
14-Pin DIP
0.01% Linearity

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

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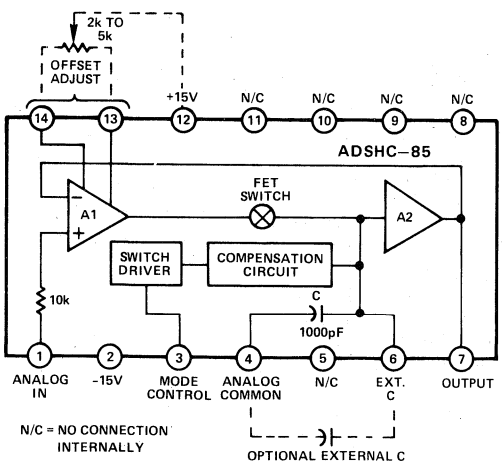
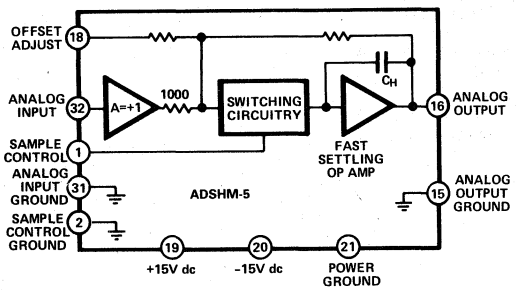


ADSHC-85

Improved SHC-85 Replacement
500ns Sample-to-Hold Transient
50μV rms Noise
Low Droop Rate of 0.2mV/ms

Vol. I
14–37

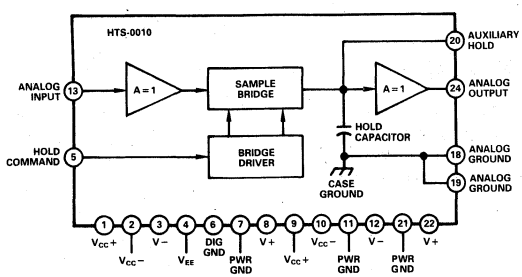
Very High Speed



ADSHM-5

Page

2nd Source–Replaces All SHM-5 Series Vol. II
Fast 350ns Acquisition Time to ±0.01% 14–11
Aperture Uncertainty 250ps
ADSHM-5K
Ultra Fast 250ns Acquisition Time to ±0.01%
100ns Acquisition Time to ±0.1%
Wide 12MHz Bandwidth
300V/μs Slew Rate
Super Low 2nA Input Bias Current

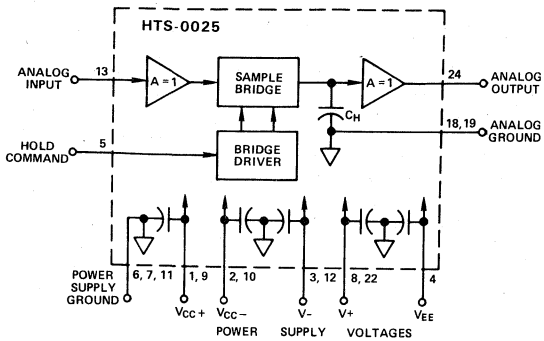


HTS-0010

Aperture Jitter of 5ps Vol. I
Acquisition Time 10ns 14–49
Output Current ±40mA
Slew Rate 300V/μs

Selection Guide
Sample/Track-Hold Amplifiers

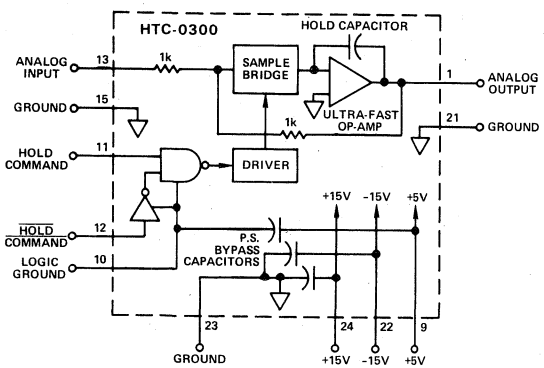
Very High Speed



HTS-0025

Aperture Time to 20ps
Acquisition Time to 20ns
Linearity 0.01%
$10^{10}\Omega$ Input Z (HTS-0025)
±50mA Output Current

Page
Vol. I
14–55

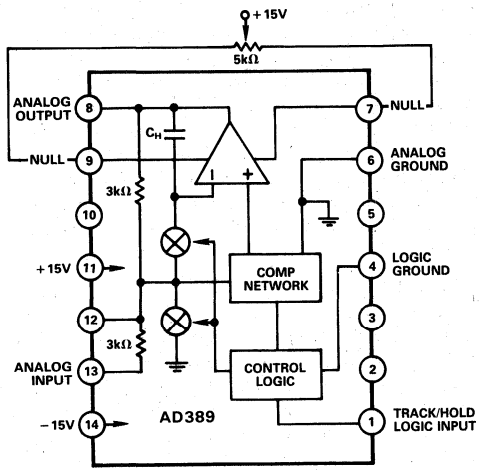


HTC-0300

Aperture Jitter of 100ps
Input Range ±10V
Output Current ±50mA
Max Droop Rate 5μV/μs

Vol. I
14–41

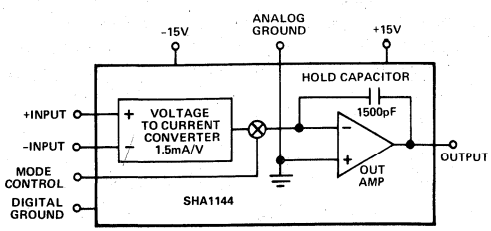
High Resolution



AD389

Page

- Companion to High Resolution A/D Converters — Vol. I 14–17
- Fast Acquisition Time: 2.5μs to ±0.003%
- Low Droop Rate: 0.1μV/μs
- Aperture Jitter: 400ps
- Internal Hold Capacitor
- Unity Gain Inverter
- Low Power Dissipation: 300mW



SHA1144

- High Resolution 14-Bit Sample-and-Hold Amplifier — Vol. II 14–15
- ±10V Range
- 50ns Aperture Delay
- 0.5ns Aperture Jitter
- Acquisition Time: 6μs to ±0.003%
- 6μs Settling Time
- 0.001% Max Gain Linearity Error
- Complete with Input Buffer: No External Components Required to Meet Rated Performance

Orientation
Sample/Track-Hold Amplifiers

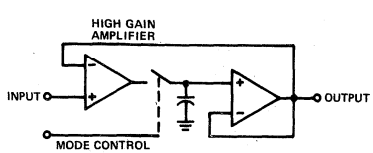
The principal application for sample/track-hold amplifiers is to maintain an analog-to-digital converter's input constant during conversion, at a value representing the analog input as of a certain precisely known time. The characteristics of the SHA are crucial to system accuracy and the reliability of the digital data, especially in 12-bit and/or high-throughput-rate applications.

A sample/track-hold amplifier (s/h or SHA), as its name indicates, has two modes of operation, programmed by a digital control-input. In the *track*– or *sample*–mode, the output follows the input, usually with a gain of +1. When the mode-input switches to *hold*, the output of the SHA ideally retains the last value it had when the command to hold was given, and it retains that value until the logic input dictates *track (sample)*, at which time the output ideally jumps to the input value and follows the input until the next *hold* command is given.

Analog Devices *track-holds* and *sample-holds* are functionally identical; they are designed to acquire input signals for either immediate hold or for a possibly extended period of tracking. They should not be confused with ac devices termed "sample-hold" that can *only* obtain quick samples and cannot track the input continuously.

SHA CIRCUITRY AND HARDWARE

A sample-hold amplifier usually consists of a storage capacitor, input- and output buffer-amplifiers, and a switch and its drive-circuitry. During *sample*, the circuit is connected to promote rapid charging of the capacitor. During *hold*, the capacitor is disconnected from its charging source and–ideally– retains its charge. The figure below shows a typical feedback configuration (AD583): the input buffer is a high-gain differential amplifier with a current output that charges the capacitor through the logic-controlled switch. The capacitor is unloaded by a unity-gain buffer-follower. The output is fed back to the negative input (as in an op-amp follower configuration), and thus, in *sample*, the charge on the capacitor is compelled to follow the input. In *hold*, the input amplifier no longer drives the capacitor; it retains its charge, unloaded by the output follower. In another popular configuration, the capacitor is used as the feedback element of an inside-the-loop integrator (AD582, AD585, SHA1144, HTC-0300). The highest-speed devices (HTS-0025) usually run open loop.

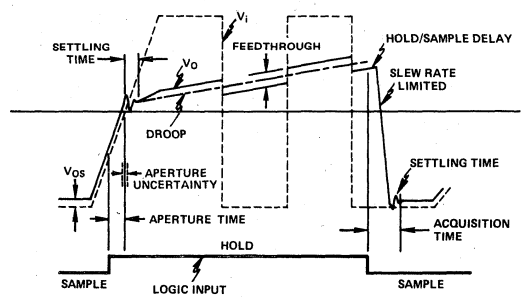


Since drive current is finite, and leakage current in *hold* is not zero, the capacitance–if large–limits the slewing rate in *sample* and–if small–converts leakage current to "droop" in *hold*. In s/h *hybrids*, the capacitance is usually fixed, and the properties of the complete device are optimized for one condition– and so specified. In s/h *monolithic ICs*, the capacitor is omitted, and furnished by the user (both for flexibility and because good capacitors for this purpose are hard to integrate). The optimum capacitance can be selected for the specific application. Design curves of performance vs. capacitance, given on the IC data sheets (AD582 and AD583) facilitate this process. In some types, the gain connections are external, like those of an op amp (AD582, AD583, SHA1144), permitting gains other than +1.

PERFORMANCE

In the *sample* mode, it is useful to consider that a SHA's performance can be characterized by specifications similar to those of a closed-loop operational amplifier (offset, drift, nonlinearity, gain error, bias current, etc.), but with somewhat slower response (gain-bandwidth, slewing rate, settling time) because of the need to charge the storage capacitor.

However, during the *sample-to-hold, hold,* and *hold-to-sample* states, the dynamic nature of the mode-switching introduces a number of specifications that are peculiar to SHAs. The most-important of these are defined below and illustrated in the adjoining figure. They include the *aperture time* and its *uncertainty*, the *sample-to-hold step, feedthrough* and *droop* (in hold), and *acquisition time.*



DEFINITIONS

Acquisition Time is the time required by the output of the device to reach its final value, within a specified error band, after the *sample* command has been given. Included are switch-delay time, the slewing interval, and settling time for a specified output-voltage change.

Aperture (Delay) Time is the time required after the *hold* command for the switch to open fully. The sample is, in effect, delayed by this interval, and the *hold* command would have to be advanced by this amount for precise timing.

Aperture Uncertainty—or *Aperture (Delay) Jitter*—is the range of variation in the *aperture time*. If the *aperture time* is "tuned out" by advancing the *hold* command a suitable amount, this spec establishes the ultimate timing error, hence, the maximum sampling frequency to a given resolution.

Charge Transfer (or *offset step*), the principal component of *sample-to-hold* offset (or *pedestal*), is the charge transferred to the storage capacitor via stray capacitance when switching to the *hold* mode. It can sometimes be reduced by lightly coupling an appropriate-polarity version of the *hold* signal to the capacitor for cancellation. The associated voltage error ($\Delta Q/C$) can be reduced by using greater capacitance for storage; but this increases response time.

Droop is the change of the output voltage during *hold* as a result of leakage or bias currents flowing through the storage capacitor. Its polarity depends on the sources of leakage current within a given device. In ICs, it is specified as a *(droop* or *drift)* current, in modules, a dV/dt. (Note: I = CdV/dt.)

Feedthrough is the fraction of the input signal variation or ac input waveform that appears at the output in *hold*. It is caused by stray capacitive coupling from the input to the storage capacitor, principally across the open switch.

Sample-to-Hold Offset, a shift in level between the last value in *sample* and the value settled-to in *hold*, is the residual step error after the *charge transfer* is accounted for and/or cancelled. Since it is unpredictable in magnitude and may be a function of the signal, it is also known as *offset nonlinearity.*

ANALOG DEVICES

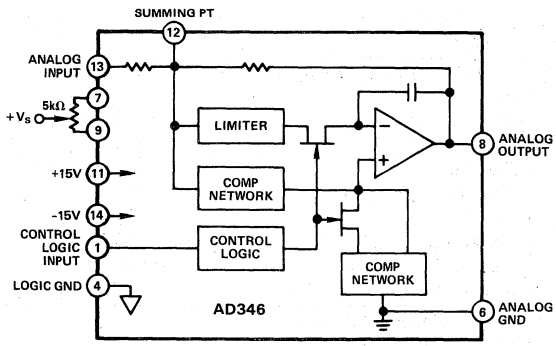
High Speed Sample-and-Hold Amplifier

AD346

FEATURES

Fast 2.0μs Acquisition Time to ±0.01%
Low Droop Rate: 0.5mV/ms
Low Offset
Low Glitch: <40mV
Aperture Jitter: 400ps
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor

AD346 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD346 is a high speed (2μs to 0.01%), adjustment free sample-and-hold amplifier designed for high throughput rate data acquisition applications. The fast acquisition time (2μs to 0.01%) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 97kHz.

The AD346 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset. The AD346 is also laser trimmed to eliminate the need for external trimming potentiometers.

Typical applications for the AD346 include sampled data systems, D/A deglitchers, peak hold functions, strobed measurement systems and simultaneous sampling converter systems.

The device is available in two versions: the "J" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, −55°C to +125°C.

ORDERING GUIDE

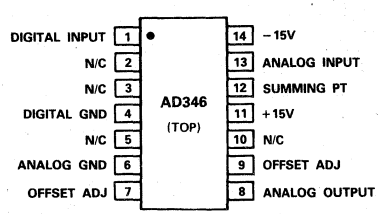
Model	Temperature Range	Package Outline[1]
AD346JD	0 to +70°C	HY14C
AD346SD	−55°C to +125°C	HY14C

NOTE
[1]See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The AD346 is an improved second source for other sample and holds of the same pin configuration.
2. The AD346 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.5mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.

PIN CONFIGURATION



PIN OUT

14

SPECIFICATIONS (typical @ +25°C, V_S = ±15V unless otherwise noted)

Model	AD346JD	AD346SD	Units
ANALOG INPUT			
Voltage Range	±10.0	*	Volts
Input Impedance	3.0	*	kΩ
DIGITAL INPUT			
"0" Input Threshold Voltage (Hold)	+0.8 max	*	Volts
"1" Input Threshold Voltage (Sample)	2.0 min	*	Volts
"0" Input Current	50.0	*	μA
"1" Input Current	1.0	*	μA
TRANSFER CHARACTERISTICS			
Gain	−1.0	*	V/V
Gain Error	±0.02 max (±0.01 typ)	*	% FSR
Gain Error, $T_{min}-T_{max}$	±0.05 max (±0.03 typ)	*	% FSR
Offset Voltage	±3 max (±1 typ)	*	mV
Offset Voltage, $T_{min}-T_{max}$	±20 max (±6 typ)	*	mV
Pedestal	±4 max (±2 typ)	*	mV
Pedestal, $T_{min}-T_{max}$	±20 max (±8 typ)	±20 max (±10 typ)	mV
Droop Rate	0.5 max (0.1 typ)	*	mV/ms
Droop Rate, $T_{min}-T_{max}$	60 max (20 typ)	700 max (200 typ)	mV/ms
DYNAMIC CHARACTERISTICS			
Full Power Bandwidth			
V_{OUT} = +10V, −3dB	1.4	*	MHz
Output Slew Rate	50	*	V/μs
Acquisition Time			
To ±0.01% 10V Step	2.0 max (1.0 typ)	*	μs
To ±0.01% 20V Step	2.5 max (1.6 typ)	*	μs
Aperture Delay	60 max (30 typ)	*	ns
Aperture Jitter	0.4	*	ns
Settling Time			
Sample Mode (10V Step)	2.0 max (1.0 typ)	*	μs
Sample to Hold	500	*	ns
Feedthrough (Hold Mode)			
at 1kHz	0.02 max (0.005 typ)	*	% FSR
Transient Peak Amplitude			
Sample/Hold/Sample	40	*	mV
ANALOG OUTPUT			
Output Voltage Swing[1]	±10.0 min	*	Volts
Output Current	3.0	*	mA
POWER REQUIREMENTS			
Operating Voltage Range	±12 to ±18	*	Volts
Supply Current			
+V	18 max (9 typ)	*	mA
−V	−10 max (−3 typ)	*	mA
Power Supply Rejection Ratio	100	*	μV/V
Power Consumption	500 max (200 typ)	*	mW

NOTES
[1]Maximum output swing is 4V less than $+V_S$.
*Specifications same as AD346JD.
Specifications subject to change without notice.

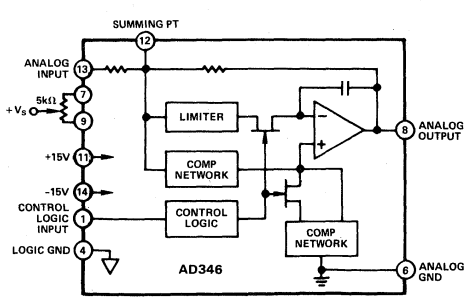


Figure 1. Functional Block Diagram

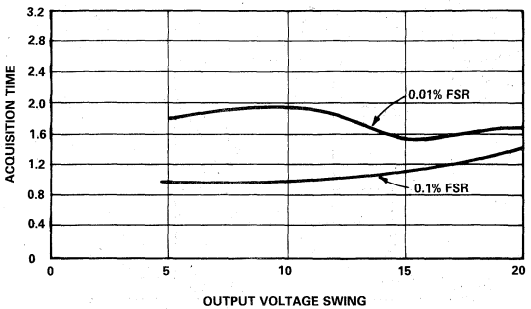


Figure 2. Acquisition Time vs. Output Voltage

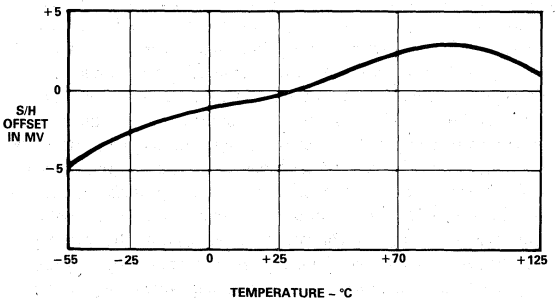


Figure 4. S/H Offset Drift (Typical)

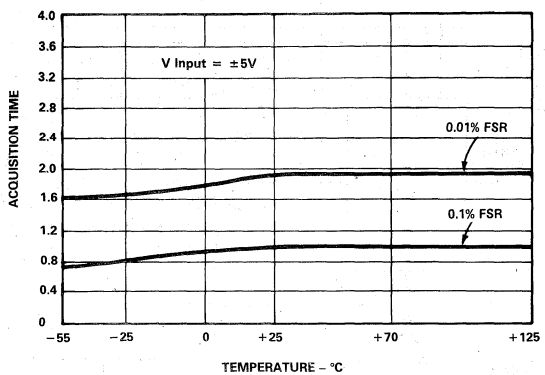


Figure 3. Acquisition Time vs. Temperature

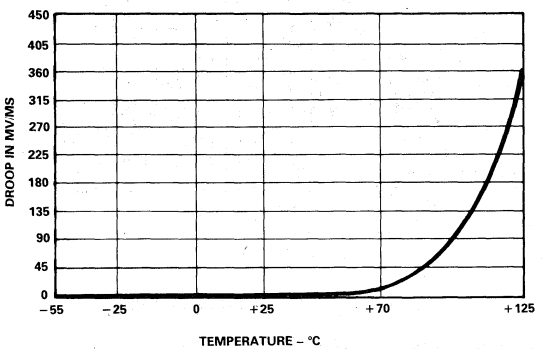


Figure 5. Droop vs. Temperature (±5 Volts)

TERMINOLOGY

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sampling timing.

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency.

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage.

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Pedestal during hold is a sample-to-hold offset. This is an offset that occurs from such phenomena as charge dumps when switches are opened, coupling of the logic signal transients.

Transients are the spikes or glitches that occur on the output at the start and end of hold time.

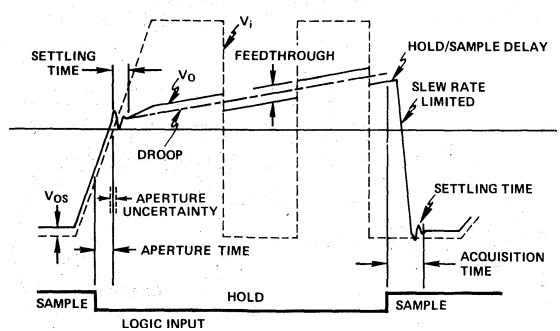


Figure 6. Pictorial Showing Various S/H Characteristics

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD346. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

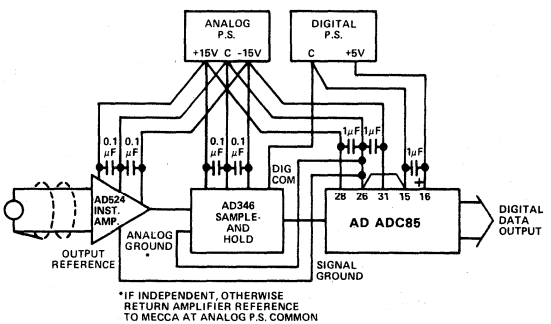


Figure 7. Basic Grounding Practice

SAMPLED DATA SYSTEMS

The fast acquisition time of the AD346 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acqusition systems. The AD346 can be used with a number of different A/D converters to achieve high throughput rates. Figures 8, 9 and 10 show the use of an AD346 with the AD578, AD5240 and AD ADC85.

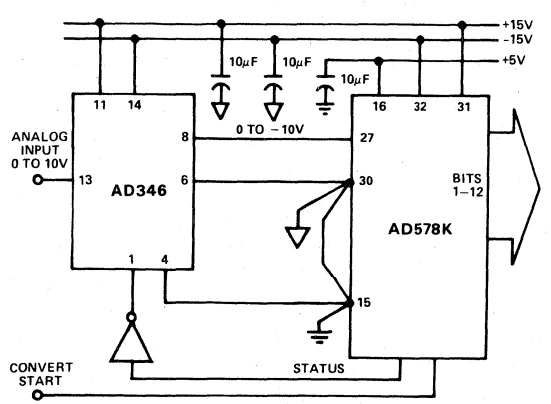


Figure 8. 153kHz–12-Bit, A/D Conversion System

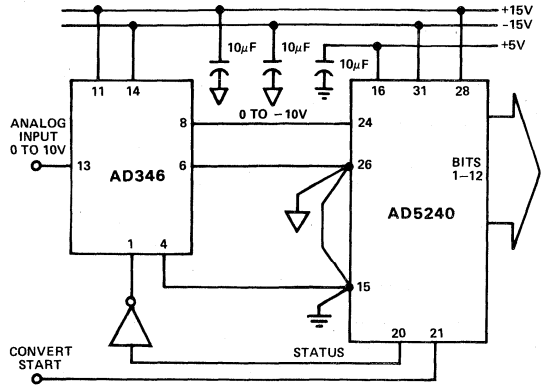


Figure 9. 142.8kHz–12-Bit, A/D Conversion System

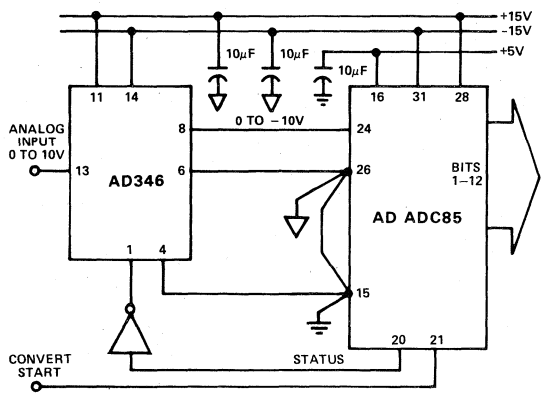


Figure 10. 83.3kHz–12-Bit, A/D Conversion System

In sampled data systems there are two limiting factors in digitizing high frequency signals. The first limitation is the bandwidth and aperture uncertainty of the sample-and-hold amplifier. The second limitation is the maximum update rate for the SHA and A/D converter combination. For high throughput rate data acquisition systems all factors must be understood.

The aperture time is the time required for the sample and hold amplifier to switch from sample to hold. Since this is a constant it can be tuned out by advancing the sample-to-hold command by 60ns with respect to the input signal and, therefore, can be eliminated as an error source. Once the aperture time has been eliminated the aperture jitter which is the variation aperture time from sample-to-sample, remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(2)\ (\text{Full Scale Voltage})\ \pi\ (\text{Aperture Jitter})}$$

For an application with a 10-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-10}}{(2)\ (10)\ \pi\ (4 \times 10^{-10}\ \text{sec})}$$

F_{max} = 388.6kHz.

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{2\ (10)\ \pi\ (4 \times 10^{-10}\ \text{sec})}$$

F_{max} = 97.1kHz.

The maximum throughput rate is the sum of the sample-and-hold acquisition time, settling time and the A/D conversion time as shown in Figure 11.

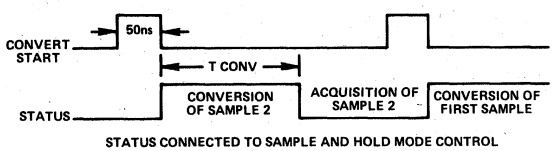


Figure 11. Start/Status Timing for Sampled Data System

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, what has been assumed is that an ideal brickwall filter has been placed in the signal path prior to the AD346 and A/D converter.

AD346 in Combination With an	Throughput Rate	Input Frequency Range
AD578K	153kHz	dc to 76.5kHz
AD5240	143kHz	dc to 71.5kHz
AD ADC85	83.3kHz	dc to 41.6kHz
AD579	263kHz	dc to 131kHz
HAS1002	250kHz	dc to 125kHz
MAH1001	333kHz	dc to 166kHz

Table I. SHA & ADC Combinations and Maximum Throughput Rate

MULTICHANNEL CONVERSION

In multichannel conversion systems, elements of the acquisition chain may be shared by two or more input sources. This sharing may occur in a number of ways, depending on the desired properties of the multiplexed system.

The data acquisition system shown in Figure 12 is one solution to digitizing data from many analog channels. For most efficient use of time, the multiplexer is acquiring the next channel to be converted while the sample-hold is holding the previous output level for conversion. When conversion is complete, the status line from the converter causes the S/H to return to the sample mode and acquire the new data. After the acquisition time is completed, the sample hold can be switched to hold. A conversion can then begin and the multiplexer can be switched to the next channel.

In applications where the AD346 is to be driven from high impedance sources or directly from an analog multiplexer, a fast slewing, fast settling wideband op amp like the ADLH0032 should be used as an input buffer.

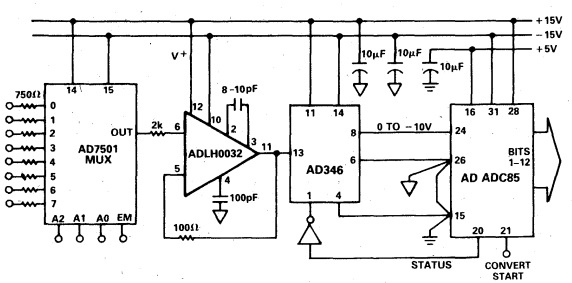


Figure 12. Data Acquisition System

ANALOG DEVICES

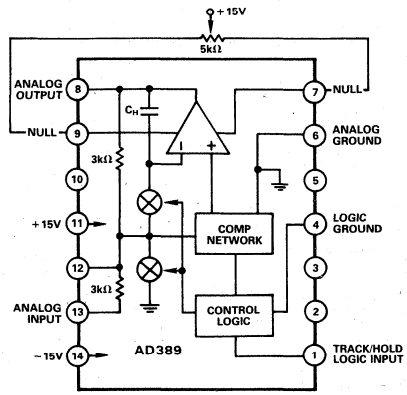
High Resolution Track-and-Hold Amplifier

AD389

FEATURES

Companion to High Resolution A/D Converters
Fast Acquisition Time: 2.5μs to ±0.003%
Low Droop Rate: 0.1μV/μs
Aperture Jitter: 400ps
Internal Hold Capacitor
Unity Gain Inverter
Low Power Dissipation: 300mW

AD389 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD389 is a high accuracy, adjustment free track-and-hold amplifier designed for high resolution data acquisition applications. The fast acquisition time (2.5μs to 300μV) and low aperture jitter (400ps) make it suitable for use with fast A/D converters to digitize signals up to 40kHz.

The AD389 is complete with an internal hold capacitor and it incorporates a compensation network which minimizes the sample to hold charge offset.

Typical applications for the AD389 include sampled data systems, peak hold functions, strobed measurement systems and simultaneous sampling converter systems. When used with autozero and autocalibration techniques, this T/H combined with a high linearity A/D will offer 14-bit performance over the converter's full no-missing-code temperature range.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "B" specified over the full industrial temperature range, −25°C to +85°C.

ORDERING GUIDE

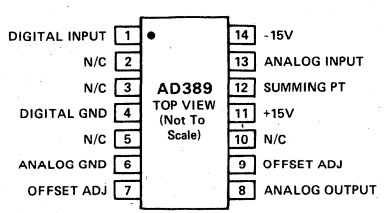
Model	Temperature Range	Package Outline[1]
AD389KD	0 to +70°C	HY14C
AD389BD	−25°C to +85°C	HY14C

NOTE
[1]See Section 19 for package outline information.

PRODUCT HIGHLIGHTS

1. The AD389 is the ideal companion track-and-hold amplifier to 14-bit accurate A/D converters.
2. The AD389 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.
3. The droop rate is only 0.1μV/μs so that it may be used in slower high resolution systems without the loss of accuracy.
4. The fast acquisition time and low aperture make it suitable for high speed data acquisition systems and digital audio recording.
5. The AD389T/H amplifier is ideal for applications requiring wide dynamic range.
6. Clever circuit design eliminates any measurable thermal tail (see Figures 11a and 11b).

PIN CONFIGURATION



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SPECIFICATIONS (typical @ +25°C and nominal power supply voltage of ±15V unless otherwise noted)

Model	AD389KD	AD389BD	UNITS
ANALOG INPUT			
Voltage Range	±10 min	*	V
Overvoltage, no damage	±15 max	*	V
Impedance	3000	*	Ω
DIGITAL INPUT (TTL Compatible)			
Track Mode, Logic "1"	2 to 5.5V	*	V
Hold Mode, Logic "0"	0 to 0.8V	*	V
Logic "1" Current	20	*	μA
Logic "0" Current	360	*	μA
ANALOG OUTPUT			
Voltage	±10 min	*	V
Current	3	*	mA
Short Circuit Current	20	*	mA
Impedance	1	*	Ω
DC ACCURACY/STABILITY			
Gain	−1.00	*	V/V
Gain Error	±0.01 (±0.02 max)	*	%
Gain Nonlinearity (±10V Output Track)	±0.001	*	%
Gain Temperature Coefficient	1 (5 max)	*	ppm/°C
Offset Voltage	±3 max, adjustable to zero	*	mV
Output Offset @ T_{min}, T_{max} (Track)	±6	*	mV
TRACK MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	1.5	*	MHz
Full Power Bandwidth	0.5	*	MHz
Slew Rate	30	*	V/μs
Noise in Track Mode, dc to 1.0MHz	200	*	μV rms
TRACK-TO-HOLD SWITCHING			
Aperture Time	30	*	ns
Aperture Uncertainty (Jitter)	0.4	*	ns
Offset Step (Pedestal)	±2 (4 max)	*	mV
Pedestal with Temperature	±4	±6	mV
Switching Transient			
Amplitude	200	*	mV
Settling to 1mV	0.5 (2 max)	*	μs
Settling to 0.3mV	1.0 (3 max)	*	μs
HOLD MODE DYNAMICS			
Droop Rate	0.1 (1 max)	*	μV/μs
Droop Rate at T_{max}	10 max	40 max	μV/μs
Feedthrough Rejection (10V p-p @ 20kHz)	86 (74 min)	*	dB
HOLD-TO-TRACK DYNAMICS			
Acquisition Time to ±0.01% of 20V	1.5 (3 max)	*	μs
Acquisition Time to ±0.003% of 20V	2.5 (5 max)	*	μs
POWER REQUIREMENTS			
Nominal Voltages for Rated Performance	±15 (±3%)	*	V
Operating Range[1]	±11 to ±18	*	V
Power Supply Rejection	100	*	μV/V
Supply Current			
$+V_S$	15 (20 max)	*	mA
$-V_S$	−4 (10 max)	*	mA
Power Dissipation	300 (500 max)	*	mW
TEMPERATURE RANGE			
Operating	0 to +70	−25 to +85	°C
Storage	−55 to +125	*	°C
THERMAL RESISTANCE			
Junction to Air, θja (free air)	60	*	°C/W
Junction to Case, θjc	20	*	°C/W

NOTES

[1]Operating to derated performance with $|V_{IN}| < |V_S - 5V|$.

*Specifications same as AD389KD.

Specifications subject to change without notice.

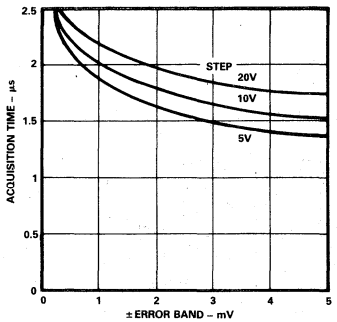


Figure 1. Acquisition Time vs. Final Error Band

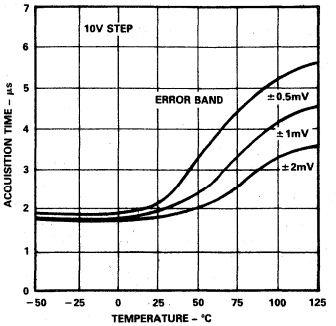


Figure 2. Acquisition Time vs. Temperature

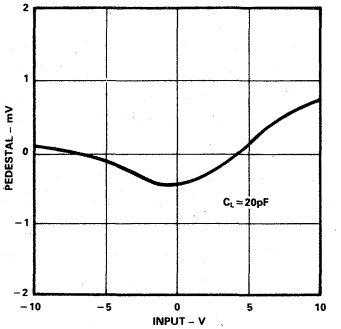


Figure 3. Pedestal vs. Input Voltage

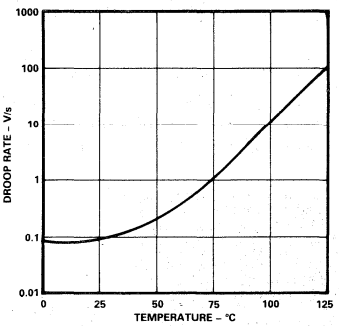


Figure 4. Droop Rate vs. Temperature

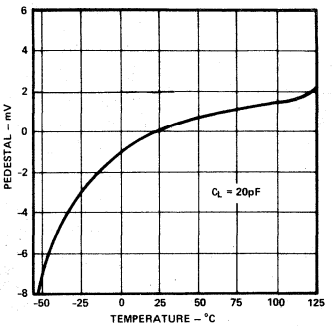


Figure 5. Pedestal vs. Temperature

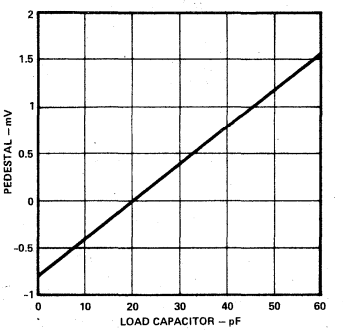


Figure 6. Pedestal vs. Load Capacitor

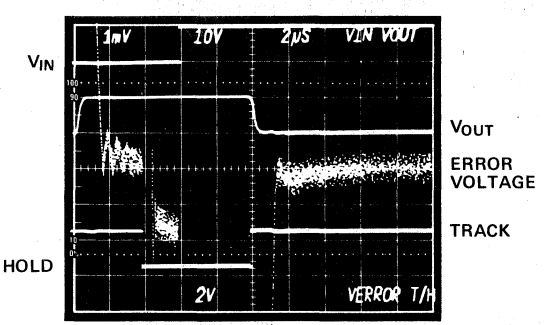


Figure 7. Hold to Track Acquisition Time

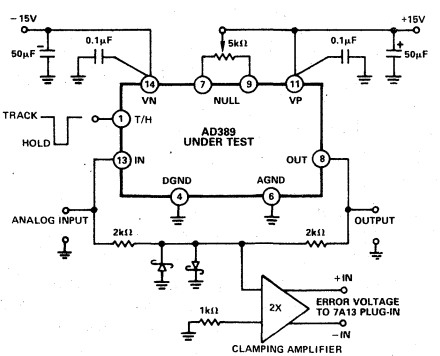


Figure 8. Pedestal and Acquisition Time Test Circuit

TERMINOLOGY

Aperture Time is the time required after the "hold" command until the switch is fully open and it produces a delay in the effective sampling timing.

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the track-to-hold command with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency.

Acquisition Time is the time required by the device to reach its final value within a given error band after the track command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage.

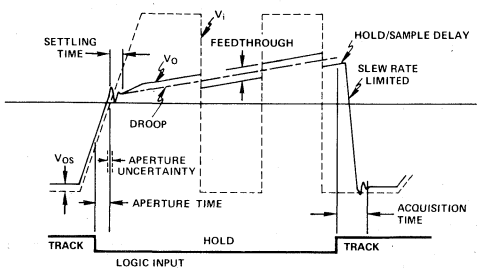


Figure 9. Pictorial Showing Various T/H Characteristics

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Pedestal during hold is a track-to-hold offset. This is an offset that occurs from such phenomena as charge dumps when switches are opened, and coupling of the logic signal transients.

Thermal Tail is the slow drift of the output stage as it settles to the final value with a thermally induced offset due to self-heating; see Figures 11a. and 11b.

Transients are the spikes or glitches that occur on the output at the start and end of hold time.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pins of the AD389. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

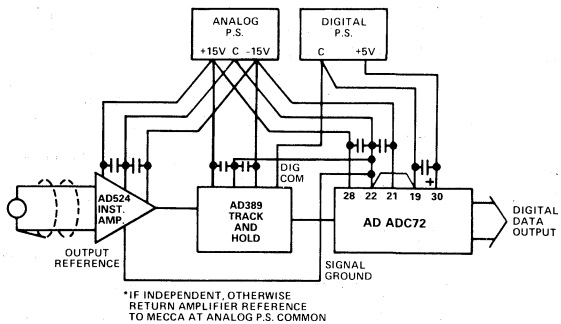


Figure 10. Basic Grounding and Decoupling Practice

DECOUPLING

The AD389 can only settle accurately and fast if the power supplies do not change during transients. Therefore, it is necessary to put 0.1 microfarad (0.1μF) decoupling capacitors right between the supply and analog ground pins and to have 50μF tantalum caps close by.

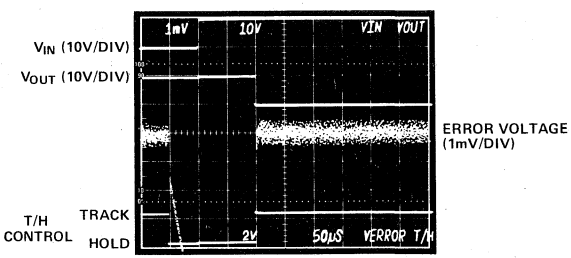


Figure 11a. Acquisition Time after 100μs in the Hold Mode. The AD389 Shows no "Thermal Tail".

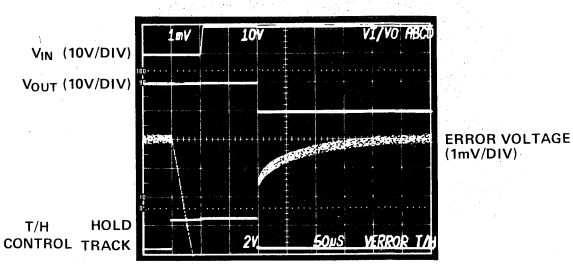


Figure 11b. Typical Thermal Tail and Acquisition Time of Other 12-Bit T/Hs Make them Unsuitable for High Resolution Applications

SAMPLED DATA SYSTEMS

The fast acquisition time of the AD389 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. Figures 12 and 13 show the use of an AD389 with the ADC72 and AD376.

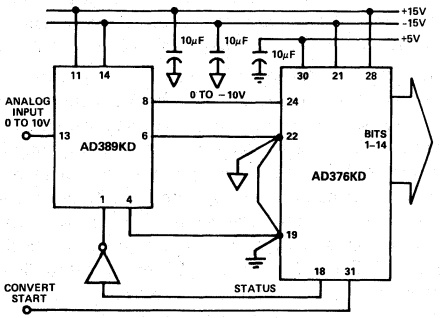


Figure 12. 20kHz–14-Bit, A/D Conversion System

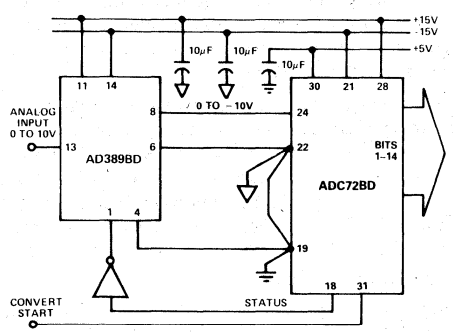


Figure 13. 8.3kHz–14-Bit, A/D Conversion System for −25°C to +85°C Operation

In sampled data systems there are two limiting factors in digitizing high frequency signals. The first limitation is the bandwidth and aperture uncertainty of the sample-and-hold amplifier. The second limitation is the maximum update rate for the T/H and A/D converter combination. For high throughput rate data acquisition systems all factors must be understood.

The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dt of the analog input which is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{(\text{Full Scale Voltage})\ (2^{-N})}{(\text{Full Scale Voltage})\ (2\pi)\ (\text{Aperture Jitter})}$$

For an application with a 14-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-14}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 24\text{kHz}$$

For an application with a 12-bit A/D converter with a 10V full scale:

$$F_{max} = \frac{(10)\ 2^{-12}}{(10)\ (2\pi)\ (4 \times 10^{-10}\ \text{sec})} = 97\text{kHz}$$

Note that some additional aperture delay and jitter are added if the AD389 is not driven directly from the convert start line, but from the status line, which from some converters is delayed.

The maximum throughput rate is the sum of the sample-and-hold acquisition time, settling time and the A/D conversion time.

The maximum input frequency is constrained by the Nyquist sampling theorem to be half of the maximum throughput rate. Input frequencies higher than half the maximum throughput rate result in "under sampling" or aliasing errors of the input signal. In the following table the maximum input frequency is reported as half of the throughput rate, with an ideal brickwall low pass filter has been placed in the signal path prior to the AD389 and A/D converter to eliminate aliasing.

AD389 in Combination With an	Throughput Rate	Input Frequency Range
ADC71 (13 bit)	22.2kHz	dc to 11.1kHz
ADC72 (14 bit)	16.7kHz	dc to 8.3kHz
AD376 (14 bit)	40.0kHz	dc to 20kHz

Table I. T/H & ADC Combinations and Maximum Throughput Rate

T/H REQUIREMENTS FOR HIGH RESOLUTION APPLICATIONS

The characteristics required for high resolution track-and-hold amplifiers are low feedthrough, low pedestal shifts with changes of input signal or temperature, high linearity, low temperature coefficients, and minimal droop rate.

For sampling a 20kHz signal to 14 bit and 16 bits for example, the following specs are required:

Spec	14 Bit	16 Bit	AD389KD	Units
Aperture Jitter (max)	2.4	0.6	0.4	ns
Slew Rate (max w/20V pk-pk signal)	1.26	1.26	30	V/μs
Feedthrough (1LSB max)	−84.3	−96.3	−86	dB
Droop Rate (1LSB max in 15μs)	40.7	10.2	0.1	μV/μs
Droop Rate (1LSB max in 50μs)	12.2	3.0	0.1	μV/μs
Acquisition Time (to ± 1LSB max) for 20kHz Signal w/15μs ADC	10	10	3-5	μs
Pedestal Shift (max) with Input Signal	−84.3	−96.3	−86	dB
Gain Temperature Coefficient (max) for ± 10°C Ambient Operation	6.1	1.5	2.0	ppm/°C
Thermal Tail (max) within 50μs after Hold	1.2	0.3	0.1	mV
Linearity Error (max)	±0.0061	0.0015	0.003	%FSR

Table II. T/H Amplifier Requirements vs. AD389 Specs

Aperture Jitter will affect exactly when the switch closes, even though the T/H control line is driven by a very precise clock. All high speed sampled data systems are very dependent on low aperture jitter for digitizing high frequency signals for spectrum analysis and accurate signal reconstruction.

The T/H amplifier slew rate determines the maximum frequency tracking rate and part of the settling time when sampling pulses and square waves. The feedthrough from input to output while in the hold mode should be less than 1LSB. The amplitude of 1LSB of the companion A/D converter for a given input range will vary from 610μV for a 14-bit A/D using a 0 to 10V input range to 4.88mV for a 12-bit A/D using a ± 10V input range. The hold mode droop rate should produce less than 1LSB of droop in the output during the conversion time of the A/D converter. For 610μV/LSB, as noted in the example above, for a 50μs 14-bit A/D converter, the maximum droop rate will be 610μV/50μs or 12μV/μs during the 50μs conversion period.

The linearity error should be less than 1LSB over the transfer function, as set by the resolution of the A/D converter. The T/H acquisition time, T/H settling time along, with the conversion time of the A/D converter determines the highest sampling rate. This in turn will determine the highest input signal frequency that can be sampled at twice a cycle per the Nyquist criteria. The pedestal shift due to input signal changes should either be linear, to be seen as a gain error, or negligible as with the feedthrough spec. The temperature coefficients for drift should be low enough such that full accuracy is maintained over some minimum temperature range. The droop rate and pedestal will shift more over temperature above +70°C (+158°F). For commercial and industrial users, these shifts will only appear above the highest temperatures their equipment will ever expect to experience. Most precision instrumentation is installed only in human inhabitable work spaces or in controlled enclosures if the area has a hostile environment.

Minimal thermal tail effects are another requirement of high resolution applications. The self-heating errors induced by the changing current levels in the output stages of T/H amps may cause more than 1LSB of error due to thermal tail effects. The performance of a typical AD389 in contrast to a typical 12-bit T/H circuit is shown in Figures 11a. and 11b. The test circuit is shown in Figure 8.

OFFSET ADJUST TRIM

In most data acquisition systems only one offset adjustment is made. In many cases it is the offset adjust of the ADC that is used to cancel all other accumulated system offsets. The offset or pedestal of the AD389 can be nulled by means of 5kΩ potentiometer between pins 7, 9, and 11. If the offset of the AD389 is not adjusted, then connect pins 7 and 9 to pin 14, the negative supply. Otherwise the high impedance of the null pin together with parasitic capacitances can cause tail effects.

ANALOG DEVICES

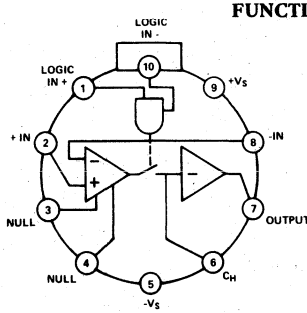
Low Cost Sample/Hold Amplifier

AD582

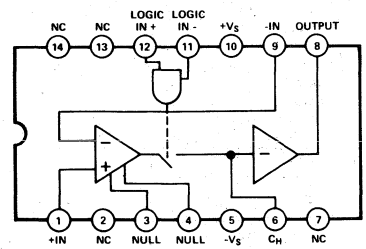
FEATURES

- **Suitable for 12-Bit Applications**
- **High Sample/Hold Current Ratio: 10^7**
- **Low Acquisition Time: 6μs to 0.1%**
- **Low Charge Transfer: <2pC**
- **High Input Impedance in Sample and Hold Modes**
- **Connect in Any Op Amp Configuration**
- **Differential Logic Inputs**

AD582 PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM



10-PIN TO-100
TOP VIEW



14-PIN TO-116
TOP VIEW

PRODUCT DESCRIPTION

The AD582 is a low cost integrated circuit sample and hold amplifier consisting of a high performance operational amplifier, a low leakage analog switch and a JFET integrating amplifier – all fabricated on a single monolithic chip. An external holding capacitor, connected to the device, completes the sample and hold function.

With the analog switch closed, the AD582 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its last level, regardless of input voltage.

Typical applications for the AD582 include sampled data systems, D/A deglitchers, analog de-multiplexers, auto null systems, strobed measurement systems and A/D speed enhancement.

The device is available in two versions: the "K" specified for operation over the 0 to +70°C commercial temperature range and the "S" specified over the extended temperature range, -55°C to +125°C. All versions may be obtained in either the hermetic sealed, TO-100 can or the TO-116 DIP.

PRODUCT HIGHLIGHTS

1. The specially designed input stage presents a high impedance to the signal source in both sample and hold modes (up to ±12V). Even with signal levels up to $\pm V_S$, no undesirable signal inversion, peaking or loss of hold voltage occurs.
2. The AD582 may be connected in any standard op amp configuration to control gain or frequency response and provide signal inversion, etc.
3. The AD582 offers a high, sample-to-hold current ratio: 10^7. The ratio of the available charging current to the holding leakage current is often used as a figure of merit for a sample and hold circuit.
4. The AD582 has a typical charge transfer less than 2pC. A low charge transfer produces less offset error and permits the use of smaller hold capacitors for faster signal acquisition.
5. The AD582 provides separate analog and digital grounds, thus improving the device's immunity to ground and switching transients.

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SPECIFICATIONS (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Time, 20V p-p Input, Hold 0V	200ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_{min} to T_{max}	1nA	150nA max
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	25k min (50k typ)	*
Common Mode Rejection V_{CM} = 20V p-p	60dB min (70dB typ)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 100pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 100pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 100pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	6mV max (2mV typ)	*
Offset Voltage, T_{min} to T_{max}	4mV	8mV max (5mV typ)
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_{min} to T_{max}	100nA	400nA max (100nA typ)
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	4.5mA max (3mA typ)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode (see next page)	60dB min (75dB typ)	*
TEMPERATURE RANGE		
Specified Performance	0 to +70°C	-55°C to +125°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*
Lead Temperature (Soldering, 15 sec)	+300°C	*
PACKAGE OPTION[1]		
"H" Package: TO-100	AD582KH	AD582SH
"D" Package: TO-116 Style (D14A)	AD582KD	AD582SD

NOTES
*Specifications same as AD582K.
[1] See Section 19 for package outline information.
Specifications subject to change without notice.

APPLYING THE AD582

Both the inverting and non-inverting inputs are brought out to allow op amp type versatility in connecting and using the AD582. Figure 1 shows the basic non-inverting unity gain connection requiring only an external hold capacitor and the usual power supply bypass capacitors. An offset null pot can be added for more critical applications.

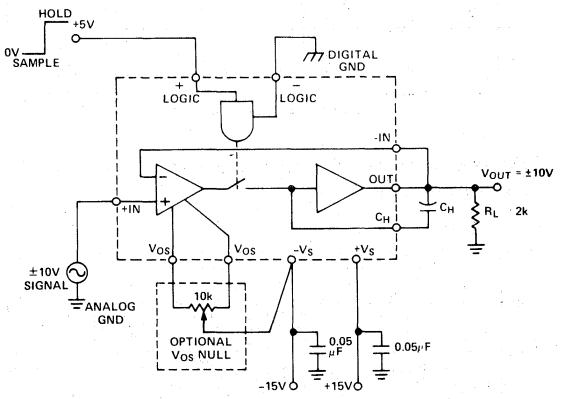


Figure 1. Sample and Hold with A = +1

Figure 2 shows a non-inverting configuration where voltage gain, A_V, is set by a pair of external resistors. Frequency shaping or non-linear networks can also be used for special applications.

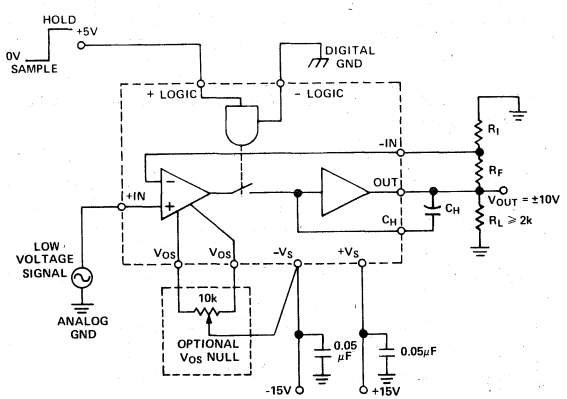


Figure 2. Sample and Hold with A = (1 + R_F/R_I)

The hold capacitor, C_H, should be a high quality polystyrene (for temperatures below +85°C) or Teflon type with low dielectric absorption. For high speed, limited accuracy applications, capacitors as small as 100pF may be used. Larger values are required for accuracies of 12 bits and above in order to minimize feedthrough, sample to hold offset and droop errors (see Figure 6). Care should be taken in the circuit layout to minimize coupling between the hold capacitor and the digital or signal inputs.

In the hold mode, the output voltage will follow any change in the $-V_S$ supply. Consequently, this supply should be well regulated and filtered.

Biasing the +Logic Input anywhere between -6V to +0.8V with respect to the -Logic will set the sample mode. The hold mode will result from any bias between +2.0V and ($+V_S$ - 3V). The sample and hold modes will be controlled differentially with the absolute voltage at either logic input ranging from $-V_S$ to within 3V of $+V_S$ (V_S - 3V). Figure 3 illustrates some examples of the flexibility of this feature.

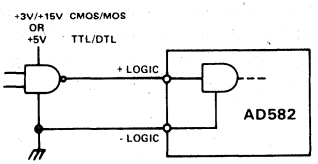


Figure 3A. Standard Logic Connection

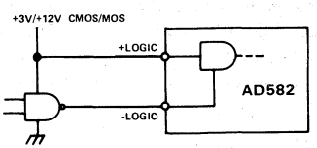


Figure 3B. Inverted Logic Sense Connection

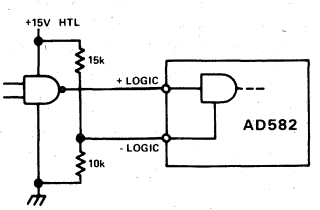


Figure 3C. High Threshold Logic Connection

DEFINITION OF TERMS

Figure 4 illustrates various dynamic characteristics of the AD582.

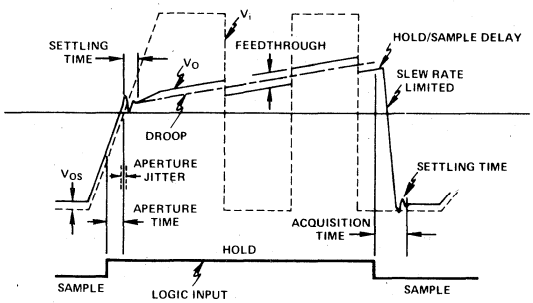


Figure 4. Pictorial Showing Various S/H Characteristics

Aperture Time is the time required after the "hold" command until the switch is fully open and produces a delay in the effective sample timing. Figure 5 is a plot giving the maximum frequency at which the AD582 can sample an input with a given accuracy (lower curve).

Aperture Jitter is the uncertainty in Aperture Time. If the Aperture Time is "tuned out" by advancing the sample-to-hold command 200ns with respect to the input signal, the Aperture Jitter now determines the maximum sampling frequency (upper curve of Figure 5).

Acquisition Time is the time required by the device to reach its final value within a given error band after the sample command has been given. This includes switch delay time, slewing time and settling time for a given output voltage change.

Droop is the change in the output voltage from the "held" value as a result of device leakage. In the AD582, droop can be in either the positive or negative direction. Droop rate may be calculated from droop current using the following formula:

$$\frac{\Delta V}{\Delta T}\ (\text{Volts/sec}) = \frac{I(pA)}{C_H(pF)}$$

(See also Figure 6.)

Feedthrough is that component of the output which follows the input signal *after* the switch is open. As a percentage of the input, feedthrough is determined as the ratio of the feedthrough capacitance to the hold capacitance (C_F/C_H).

Charge Transfer is the charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the hold mode. The charge transfer generates a sample-to-hold offset where:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H(pF)}$$

(See also Figure 6.)

Sample-to-Hold Offset is that component of D.C. offset independent of C_H (see Figure 6). This offset may be nulled using a null pot, however, the offset will then appear during the sampling mode.

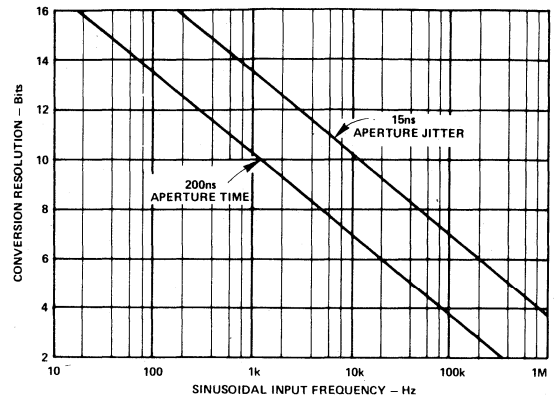


Figure 5. Maximum Frequency of Input Signal for ½LSB Sampling Accuracy

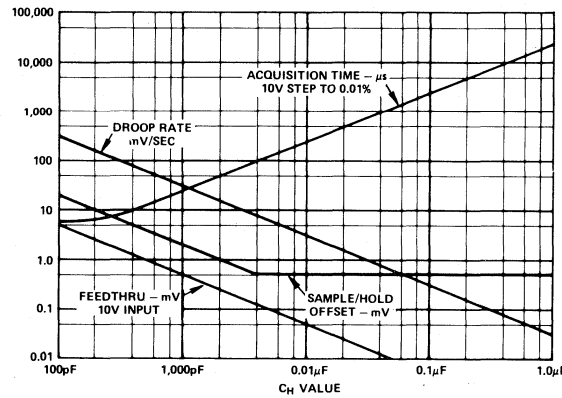


Figure 6. Sample-and-Hold Performance as a Function of Hold Capacitance

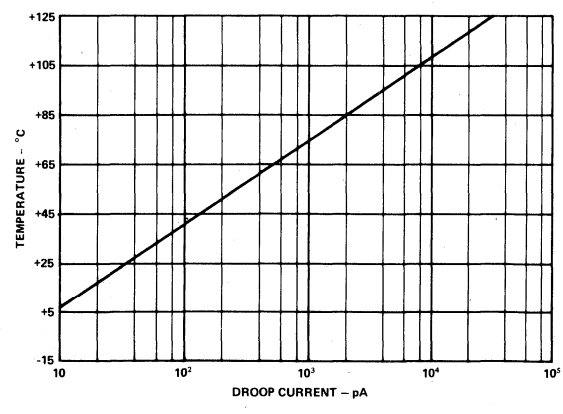


Figure 7. Droop Current vs. Temperature

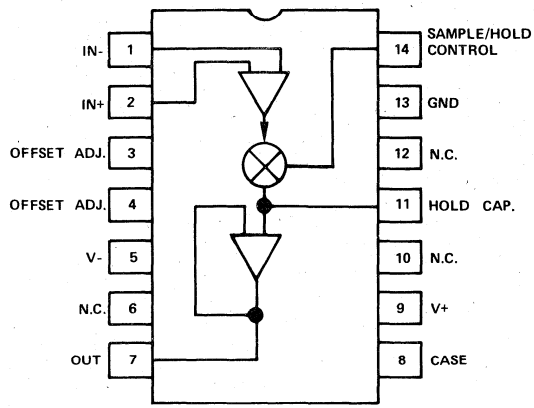
IC Sample-and-Hold Gated Op Amp

AD583

FEATURES

- High Sample-to-Hold Current Ratio: 10^6
- High Slew Rate: 5V/μs
- High Bandwidth: 2MHz
- Low Aperture Time: 50ns
- Low Charge Transfer: 10pC
- DTL/TTL Compatible
- May Be Used as Gated Op Amp

AD583 FUNCTIONAL BLOCK DIAGRAM



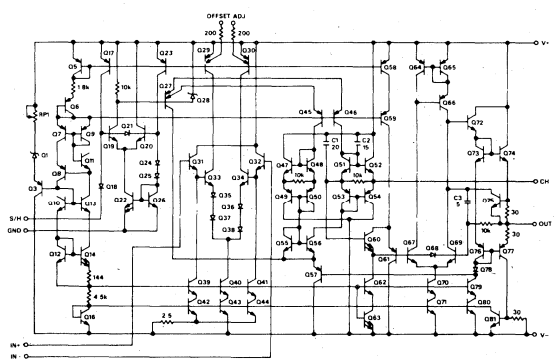
TO-116

PRODUCT DESCRIPTION

The AD583 is a monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and unity gain amplifier. An external holding capacitor, connected to the switch output, completes the sample-and-hold or track-and-hold function.

With the analog switch closed, the AD583 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open the capacitor holds the output at its previous level.

The AD583 may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.



Schematic Diagram

PRODUCT HIGHLIGHTS

1. Sample-and-hold operation is obtained with the addition of one external capacitor.
2. Low charge transfer (10pC) and high sample-to-hold current ratio insure accurate tracking.
3. Any gain or frequency response is available using standard op amp feedback networks.
4. High slew rate and low aperture time permit sampling of rapidly changing signals.
5. Output, gated through a low leakage analog switch, also makes the AD583 useful for applications such as analog switches, peak holding circuits, etc.

SPECIFICATIONS (typical @ +25°C, hold capacitor of 1000pF and ±15V dc unless otherwise specified)

MODEL	AD583KD
OPEN LOOP GAIN R_L = 2kΩ, T_{min} to T_{max}	25k min (50k typ)
OUTPUT VOLTAGE SWING R_L = 2kΩ, T_{min} to T_{max}	±10V min
OUTPUT CURRENT	±10mA min
OUTPUT RESISTANCE	5Ω
OFFSET VOLTAGE T_{min} to T_{max}	6mV max (3mV typ) 8mV max (4mV typ)
BIAS CURRENT T_{min} to T_{max}	200nA max (50nA typ) 400nA max
OFFSET CURRENT T_{min} to T_{max}	50nA max (10nA typ) 100nA max
INPUT RESISTANCE	5MΩ min (10MΩ typ)
COMMON MODE RANGE	±10V min
COMMON MODE REJECTION T_{min} to T_{max}	74dB min (90dB typ)
GAIN BANDWIDTH PRODUCT	2MHz
SLEW RATE Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = ±10V p-p	5V/μs
RISE TIME Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	100ns
OVERSHOOT Av = +1, R_L = 2kΩ, C_L = 50pF, V_{out} = 400mV p-p	20%
DIGITAL INPUT CURRENT V_{in} = 0, T_{min} to T_{max} V_{in} = +5.0V, T_{min} to T_{max}	 0.8mA max (Logic "Sample") 20μA max (Logic "Hold")
DIGITAL INPUT VOLTAGE Low T_{min} to T_{max} High T_{min} to T_{max}	 0.8V max 2.0V min
ACQUISITION TIME Av = +1, R_L = 2kΩ, C_L = 50pF to 0.1% of final value: to 0.01% of final value:	 4μs 5μs
APERTURE TIME	50ns
APERTURE JITTER	5ns
DRIFT CURRENT[1] T_{min} to T_{max}	50pA max (5pA typ) 1.0nA max (0.05nA typ)
CHARGE TRANSFER	20pC max (10pC typ)
SUPPLY CURRENT	5.0mA max (2.5mA typ)
POWER SUPPLY REJECTION[2]	74dB min (90dB typ)
OPERATING TEMP	0 to +70°C
STORAGE TEMP	–65°C to +150°C
PACKAGE STYLE[3]	TO-116 Style D14A

NOTES
[1] Voltage on hold is zero.
[2] Sample mode only.
[3] See Section 19 for package outline information.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	40V
Differential Input Voltage	±30V
Digital Voltage (Pin 14)	+8V, -15V
Output Current	Short Circuit Protected
Internal Power Dissipation	30mW (Derate power dissipation by 4.3mW/°C above +150°C ambient temperature)

APPLYING THE AD583

Figure 1 shows the AD583 connected in a simple sample and hold configuration with unity gain and offset nulling. Any other standard op amp gain and frequency response configuration may also be used. Note that the holding capacitor, C_H, should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), teflon or Mica types are recommended.

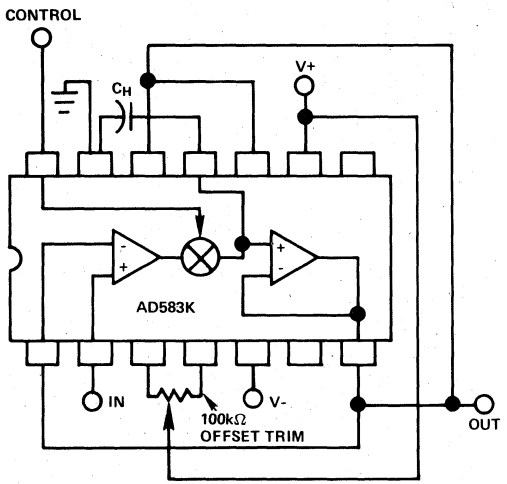


Figure 1. Basic Track-and-Hold/Sample-and-Hold

Figure 2 shows the guard ring used to reduce leakage paths between the pc board and the package. This minimizes drift during the hold command.

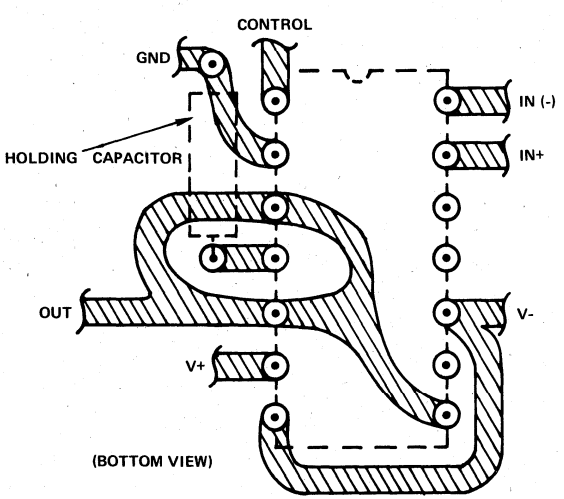


Figure 2. Guard Ring Layout

Also note that the input amplifier of the AD583 may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

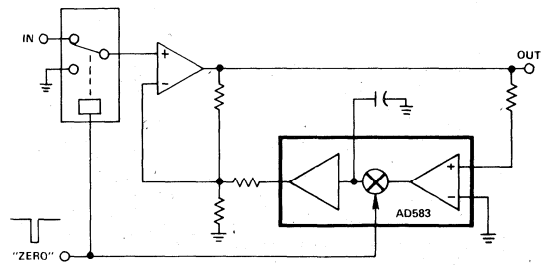


Figure 3. Automatic Offset Zeroing

The circuit of Figure 3 illustrates how the AD583 may be used to automatically zero a high gain amplifier. Basically, the input is periodically grounded and the output offset is then sampled and fed back to cancel the error. This technique is useful in A/D conversion, instrumentation, DVM's to eliminate offset drift errors by periodically rezeroing the system.

Care should be taken to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

DEFINITION OF TERMS

Acquisition Time:
Acquisition Time is the time required by the device to reach its final value within ±0.1% after the sample command has been given. This includes switch delay time, slewing time, and settling time and is the minimum sample time required to obtain a given accuracy.

Charge Transfer:
Charge Transfer is the small charge transferred to the holding capacitor from the interelectrode capacitance of the switch when the unit is switched to the sample mode. Sample-to-hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

Aperture Time:
The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

Drift Current:
Leakage currents from the holding capacitor during the hold mode cause the output voltage to drift. Drift rate (or droop rate) is calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T}\ \text{(Volts/sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

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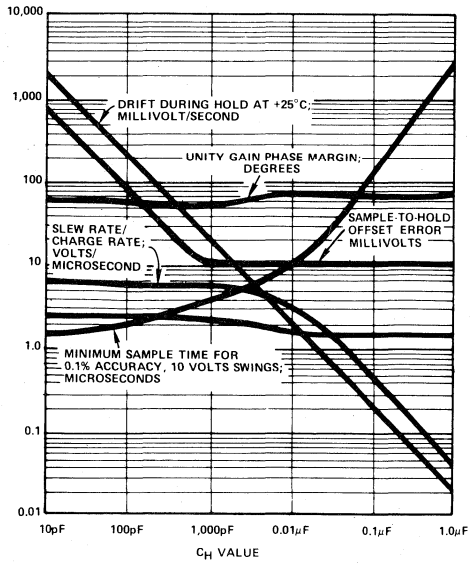
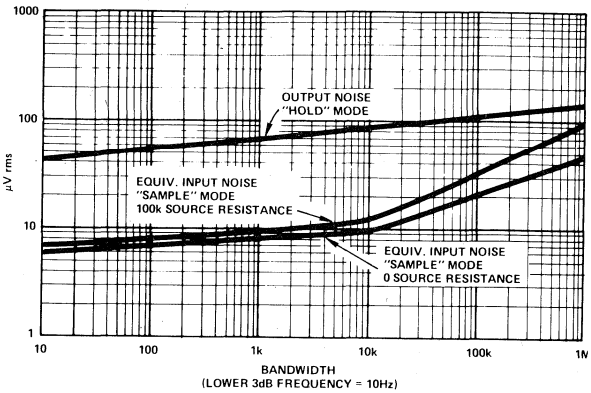
Performance Curves

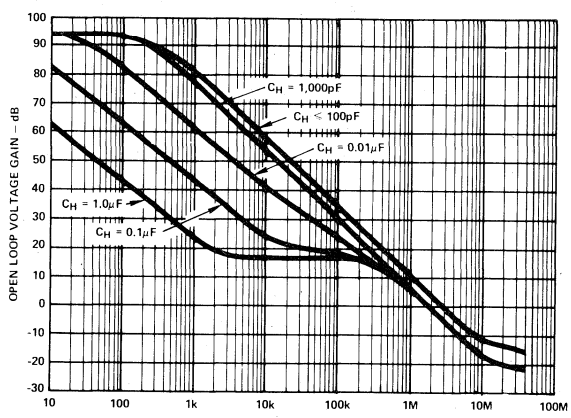
V_{SUPPLY} = ±15V dc, T_A = +25°C, C_H = 1,000pF unless otherwise specified



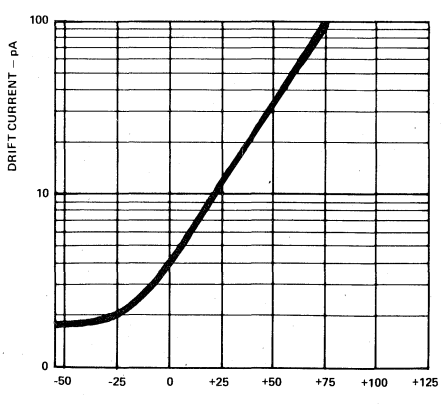
Typical Sample-and-Hold Performance as a Function of Holding Capacitance



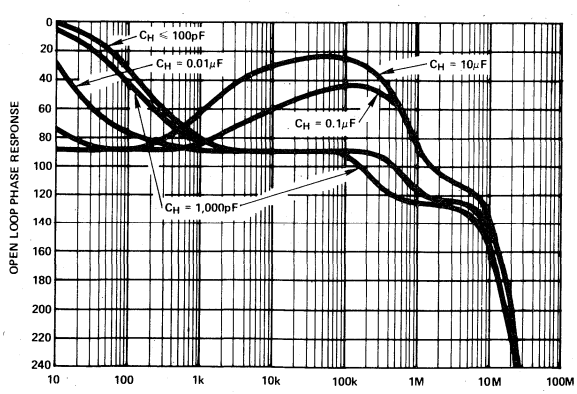
Broadband Noise Characteristics



Open Loop Frequency Response



Drift Current vs. Temperature



Open Loop Phase Response

ANALOG DEVICES

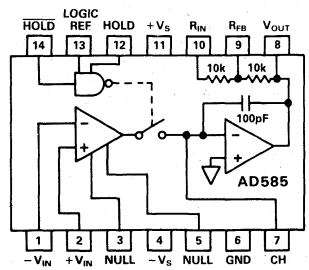
High Speed Sample-and-Hold Amplifier

AD585

FEATURES
Fast 3.0μs Acquisition Time to ±0.01%
Low Droop Rate: 1.0mV/ms
Sample/Hold Offset Step: 3mV
Aperture Jitter: 0.5ns
Extended Temperature Range: −55°C to +125°C
Internal Hold Capacitor

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay & Storage
Peak Amplitude Measurements

AD585 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD585 is a monolithic sample-and-hold circuit consisting of a high performance operational amplifier in series with an ultra-low leakage analog switch and a FET input integrating amplifier. An internal holding capacitor and connections to the internal feedback resistors, completes the sample and hold.

With the analog switch closed, the AD585 functions like a standard op amp; any feedback network may be connected around the device to control gain and frequency response. With the switch open, the capacitor holds the output at its previous level.

The AD585 offers performance previously unavailable in monolithic sample-and-hold amplifiers. The combination of a fast acquisition time (3.0μs to 0.01%) and low offset step (3mV) are suitable for high speed 12-bit data acquisition systems.

The device is available in three versions: the "J" specified for operation over the 0 to +70°C commercial temperature range is available in a 14-pin plastic DIP; the "A" specified for the −25°C to +85°C industrial temperature range, and the "S" specified over the extended temperature range −55°C to +125°C. The "A" and "S" versions are available in a 14-pin hermetic ceramic package.

PRODUCT HIGHLIGHTS

1. The droop rate is only 1.0mV/ms so that it may be used in slower high accuracy systems without the loss of accuracy.
2. The fast acquisition time and low aperture make it suitable for very high speed data acquisition systems.
3. The AD585 has internal pretrimmed application resistors for applications versatility.
4. The AD585 is complete with an internal hold capacitor for ease of use. Capacitance can be added externally to reduce the droop rate when long hold times and high accuracy are required.

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SPECIFICATIONS (typical @ +25°C and V_S = ± 15V and C_H = Internal A = +1 unless otherwise specified)

Model	AD585J	AD585A	AD585S
SAMPLE/HOLD CHARACTERISTICS			
Acquisition Time, 10V Step to 0.01%	3μs max	*	*
20V Step to 0.01%	5μs max	*	*
Aperture Time, 20V p-p Input, Hold 0V	35ns	*	*
Aperture Jitter, 20V p-p Input, Hold 0V	0.5ns	*	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*	*
Droop Rate	1mV/ms max	*	*
Droop Rate T_{min} to T_{max}	Doubles Every 10°C	*	*
CHARGE TRANSFER	0.3pC	*	*
Sample-to-Hold Offset	3mV max	*	*
Feedthrough 20V p-p, 10kHz Input	0.5mV p-p	*	*
TRANSFER CHARACTERISTICS			
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	200kV/V	*	*
Closed Loop Gain Accuracy	0.05%	*	*
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	80dB min	*	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p	2MHz	*	*
Full Power Bandwidth V_{OUT} = 20V p-p	160kHz	*	*
Slew Rate V_{OUT} = 20V p-p	10V/μs	*	*
Output Resistance Hold Mode I_{OUT} = ± 10mA	0.05Ω	*	*
Output Short Circuit Current	50mA max	*	*
ANALOG INPUT CHARACTERISTICS			
Offset Voltage	2mV max	*	*
Offset Voltage, T_{min} to T_{max}	3mV max	*	*
Bias Current	2nA	*	*
Input Capacitance, f = 1MHz	10pF	*	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	$10^{12}\Omega$	*	*
Absolute Max Diff Input Voltage	30V	*	*
Absolute Max Input Voltage, Either Input	± V_S	*	*
DIGITAL INPUT CHARACTERISTICS			
Input Voltage With Respect to Pin 13 (TTL Compatible)			
Logic Reference	1.4V ± 0.2V	*	*
Hold Mode, $\overline{Hold}$ – Logic Reference or Logic Reference – $\overline{Hold}$			
T_{min} to T_{max}	+0.4V min	*	*
Sample Mode, T_{min} to T_{max}	−0.4V max	*	*
Logic Input Current (Either Input)	50μA max	*	*
POWER SUPPLY CHARACTERISTICS			
Operating Voltage Range	+5V, −12V to ± 18V	*	*
Supply Current, R_L = ∞	10mA max	*	*
Power Supply Rejection, Sample Mode	70dB min	*	*
TEMPERATURE RANGE			
Specified Performance	0 to +70°C	−25°C to +85°C	−55°C to +125°C
Operating	−25°C to +85°C	−55°C to +125°C	−55°C to +125°C
Storage	−65°C to +150°C	*	*
Lead Temperature (Soldering, 15 sec)	+300°C	*	*
PACKAGE OPTION[1]			
(N14A)	AD585JN	–	–
(D14A	–	AD585AD	AD585SD
(E20A)	–	AD585AE	AD585SE

NOTES
*Specifications same as AD585J
Specifications subject to change without notice. [1]See Section 19 for package outline information.

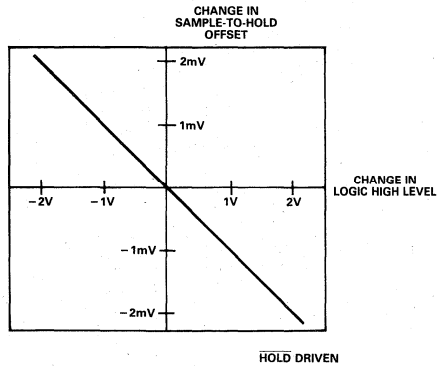


Figure 1. Sample-to-Hold Offset vs. Logic Level (HOLD Active)

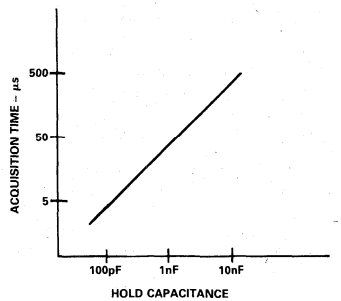


Figure 2. Acquisition Time vs. Hold Capacitance

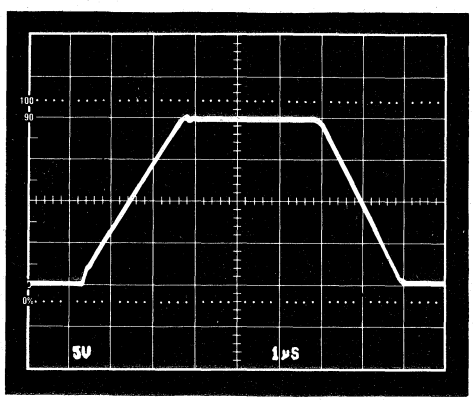


Figure 3. Follower, Sample Mode (Large Signal)

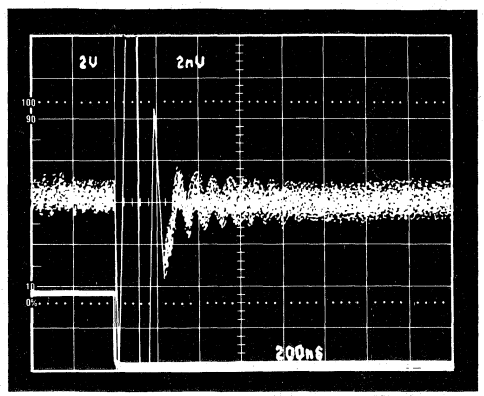


Figure 4. Sample-to-Hold Settling Time (HOLD Active)

14

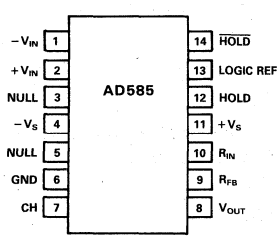


Figure 5. Pin Configuration

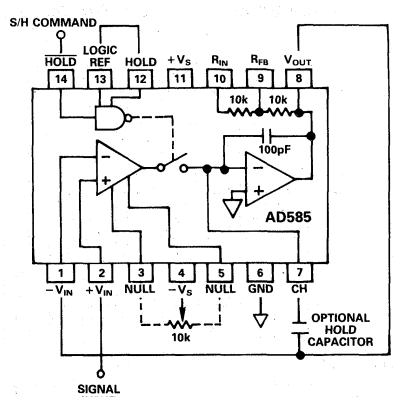


Figure 6. Connection Diagram, Gain = +1, HOLD Active

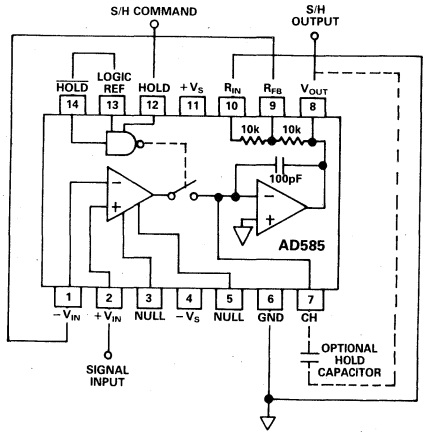


Figure 7. Connection Diagram, Gain = +2, HOLD Active

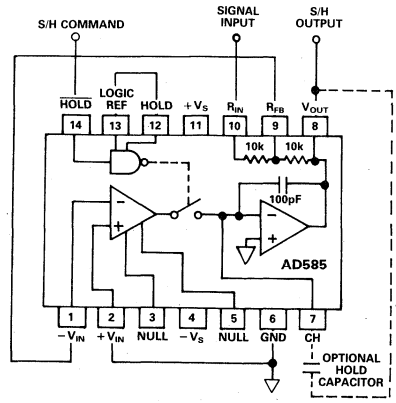


Figure 8. Connection Diagram Gain = −1, $\overline{HOLD}$ Active

SAMPLE DATA SYSTEMS

In sample data systems there are a number of limiting factors in digitizing high frequency signals accurately. Figure 9 shows pictorially the sample-and-hold errors that are the limiting factors. In the following discussions of error sources the errors will be divided into the following groups: 1. Sample-to-Hold Transition, 2. Hold Mode and 3. Hold-to-Sample Transition.

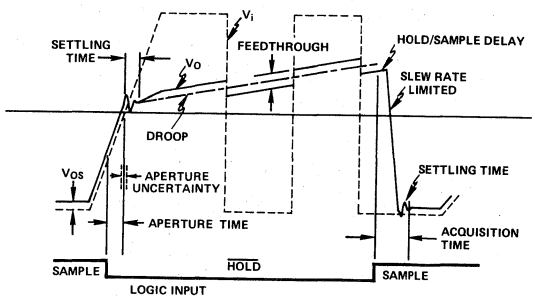


Figure 9. Pictorial Showing Various S/H Characterstics

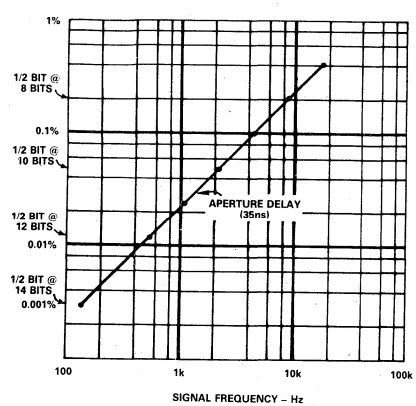


Figure 10. Aperture Delay Error vs. Frequency

SAMPLE-TO-HOLD TRANSITION

The aperture time is the time required for the sample-and-hold amplifier to switch from sample to hold. Since this is effectively a constant then it may be tuned out. If however, the aperture delay time is not accounted for then errors of the magnitude as shown in Figure 10 will result.

To eliminate the aperture delay as an error source the sample-to-hold command may be advanced with respect to the input signal.

Once the aperture time has been eliminated as an error source then the aperture jitter which is the variation in aperture time from sample-to-sample remains. The aperture jitter is a true error source and must be considered. The aperture jitter is a result of noise within the switching network which modulates the phase of the hold command and is manifested in the variations in the value of the analog input that has been held. The aperture error which results from this jitter is directly related to the dV/dT of the analog input.

The error due to aperture jitter is easily calculated as shown below. The error calculation takes into account the desired accuracy corresponding to the resolution of the A/D converter.

$$F_{max} = \frac{2^{-(N+1)}}{\pi\ (\text{Aperture Jitter})}$$

For an application with a 10-bit A/D converter with a 10V full scale to a 1/2LSB error maximum.

$$F_{max} = \frac{2^{-(10+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 310.8\text{kHz}.$$

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum.

$$F_{max} = \frac{2^{-(12+1)}}{\pi\ (0.5 \times 10^{-9})}$$

$$F_{max} = 77.7\text{kHz}.$$

Figure 11 shows the entire range of errors induced by aperture jitter with respect to the input signal frequency.

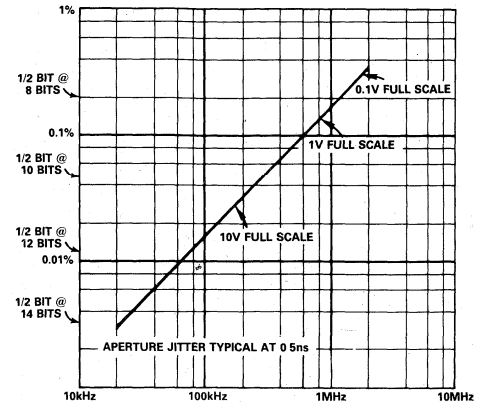


Figure 11. Aperture Jitter Error vs. Frequency

Sample-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching in to hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting sample-to-hold offset is a function of the logic level as shown in Figure 1.

The sample-to-hold offset can be reduced by adding capacitance to the internal 100pF capacitor. This may be easily accomplished by adding an external capacitor between Pins 7 and 8. The sample-to-hold offset is then governed by the relationship:

$$\text{S/H Offset (V)} = \frac{\text{Charge (pC)}}{C_H \text{ Total (pF)}}$$

For the AD585 in particular it becomes:

$$\text{S/H Offset (V)} = \frac{0.3 \text{ pC}}{100\text{pF} + (C_{EXT})}$$

The addition of an external hold capacitor also effects the acquisition time of the AD585. The change in acquisition time with respect to the C_{EXT} is shown graphically in Figure 2.

HOLD MODE

In the hold mode there are two important specifications that must be considered, feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode, hold-mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a sample and hold follows an analog multiplexer that switches between many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dT is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dT} \text{ (Volts/Sec)} = \frac{I_L(\text{pA})}{C_H(\text{pA})}$$

For the AD585 in particular,

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF} + (C_{EXT})}$$

Additionally the leakage current doubles for every 10°C increase in temperature; therefore, the hold-mode droop rate characteristic will also double in the same fashion. The hold-mode droop rate can be traded-off with acquisition time to provide the best combination of droop error and acquisition time. The tradeoff is easily accomplished by varying the value of C_{EXT}.

Since a sample and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (T_{CONV}) is required to calculate the maximum allowable dV/dT.

$$\frac{dV \text{ max}}{dt} = \frac{\Delta V \text{ max}}{T_{CONV}}$$

The maximum $\frac{dV \text{ max}}{dT}$ as shown by the previous equation is the limit not only at 25°C but at the maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dT} \times 2\,\frac{(\Delta T°C)}{10°C} \leq \frac{dV \text{ max}}{dT}$$

HOLD-TO-SAMPLE TRANSITION

The Nyquist theorem states that a band-limited signal which is sampled at a rate at least twice the maximum signal frequency can be reconstructed without loss of information. This means that a sampled data system must sample, convert and acquire the next point at a rate equal to twice the signal frequency. Thus the maximum input frequency is equal to

$$\frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

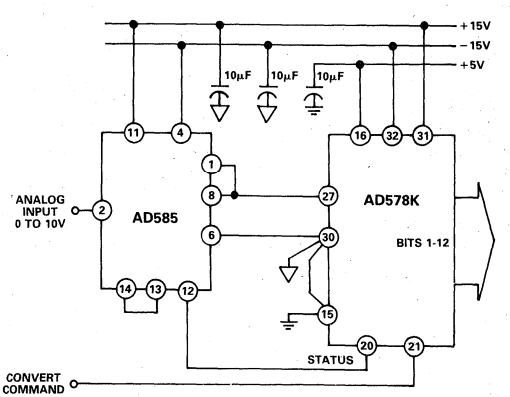


Figure 12. A/D Conversion System, 117.6kHz Throughput 58.8kHz max Signal Input

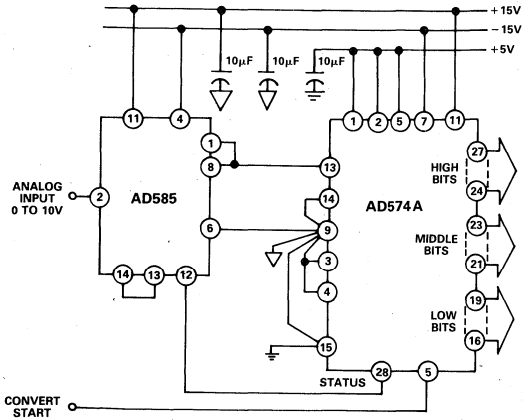


Figure 13. 12 Bit A/D Conversion System, 26.3kHz Throughput Rate, 13.1kHz max Signal Input

OPTIONAL CAPACITOR SELECTION

If an additional capacitor is going to be used in conjunction with the internal 100pF capacitor it must have a low dielectric absorption. Dielectric absorption is just that; it is the charge absorbed into the dielectric that is not immediately added to or removed from the capacitor when rapidly charged or discharged. The capacitor with dielectric absorption is modeled in Figure 14.

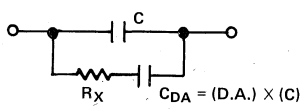


Figure 14. Capacitor Model with Dielectric Absorption

If the capacitor is charged slowly, C_{DA} will eventually charge to the same value as C. But unfortunately, good dielectrics have very high resistances, so while C_{DA} may be small, R_X is large and the time constant $R_X C_{DA}$ typically runs into the millisecond range. In fast-charge, fast-discharge situations the effect of dielectric absorption resembles "memory". In a data acquisition system where many channels with widely varying data are being sampled the effect is to have an ever changing offset which appears as a very nonlinear sample-to-hold offset since the difference between the voltage being measured and the voltage previously measured determines the fraction by which the dielectric absorption figure is multiplied. It is impossible to readily connect for this error source. The only solution is to use a capacitor with dielectric absorption less than the maximum tolerable error. Capacitor types such as polystyrene, polypropylene or Teflon are recommended.

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD585. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

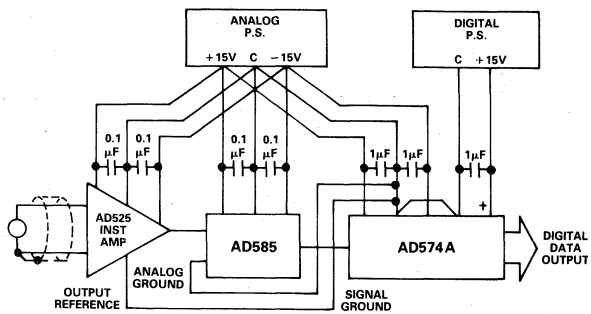


Figure 15. Basic Grounding Practice

ANALOG DEVICES

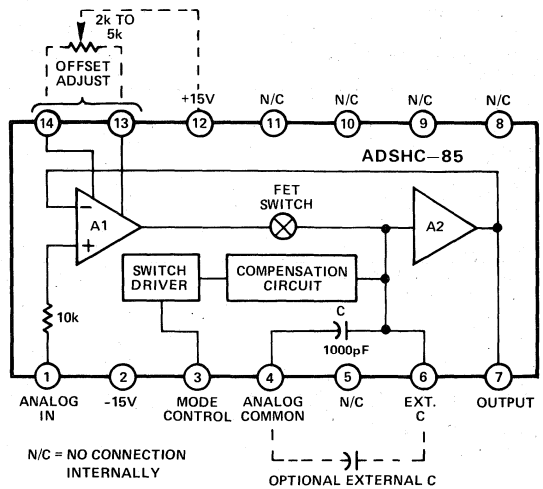
Fast 0.01% Track/Sample-and-Hold Amplifiers

ADSHC-85

FEATURES
Improved SHC-85 Replacement
500ns Sample-to-Hold Transient
50μV rms Noise
Low Droop Rate of 0.2mV/ms

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

ADSHC-85 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSHC-85 Sample/Hold amplifier combines fast acquisition time and linear performance with low cost to provide an economical solution for a variety of applications.

The unit is an improved second source for the SHC-85, featuring faster sample-to-hold settling, and lower noise. It is pin-for-pin compatible with other 14-pin DIP packages of this type; designed to acquire and hold analog signals as large as ±10V dc.

Accuracies of ±0.01% can be achieved in 4.5μs for 10-volt input steps, and in only 5μs for 20-volt steps.

Both commercial temperature ranges and extended temperature ranges are available, respectively, in the ADSHC-85 and the ADSHC-85ET.

TRACK-AND-HOLD (T/H) MODE

When operated in the T/H mode, the ADSHC-85 "tracks" all changes in analog input as they occur, functioning like a unity gain amplifier. The "hold" mode is initiated by the user and causes the output of the T/H unit to be "frozen".

A logic "1" at Pin 3 causes the unit to be in a "track" (or sample) mode; a logic "0" puts the output in "hold".

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SPECIFICATIONS (typical @ +25°C, 1,000pF internal capacitance, and nominal supply voltages unless otherwise noted)

MODEL	UNITS	ADSHC-85	ADSHC-85ET
ANALOG INPUT			
Voltage Range	V	±10	*
Overvoltage, no damage	V max	±15	*
Impedance	Ohms	10^{11}	*
Capacitance	pF	10	*
Bias Current	nA, max	0.5	*
Initial Offset Voltage	mV, max	±6, adjustable to zero	*
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample/Track" Logic "1"	+2.0V to +5.5V	50nA max	
"Hold" Logic "0"	0V to +0.8V	−50μA max	
ANALOG OUTPUT			
Voltage	V	±10	*
Current	mA	±10	*
Impedance	Ohms, max	1	*
Capacitive Load	pF	1,000	*
Noise			
@ 100kHz	μV rms	50	*
@ 1.0MHz	μV rms	150	*
DC ACCURACY/STABILITY			
Gain	V/V	+1	*
Gain Error	%	±0.01	*
Gain Nonlinearity	%	±0.01	*
Gain Temperature Coefficient	ppm/°C (max)	±2 (±10)	*
Input Offset vs. Temperature	μV/°C (max)	±25 (±100)	*
SAMPLE (TRACK) MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	MHz	3	*
Full Power (−3dB)	kHz	200	*
Slew Rate	V/μs	15	*
SAMPLE (TRACK)-TO-HOLD SWITCHING			
Aperture Time	ns	25	*
Aperture Uncertainty (Jitter)	ns	0.5	*
Offset Step (Pedestal)	mV	1.0	*
Switching Transient			
Amplitude	mV	325	*
Settling to 1mV	μs, max	0.5	*
HOLD MODE DYNAMICS			
Droop Rate			
Typical (Maximum)	mV/ms	0.2 (0.5)	*
Variation with Temperature		Doubles/10°C Change	*
Feedthrough Rejection			
(20V p-p @ 1kHz)	dB	80	*
HOLD-TO-SAMPLE (TRACK) DYNAMICS			
Acquisition Time (to ±0.01%)			
10V Step	μs, max	4.5	*
20V Step	μs, max	5.0	*
POWER REQUIREMENTS[1]			
Nominal Voltages	V (%)	±15 (±3)	*
Current	mA, typ (max)	±18 (±20)	*
Power Supply Rejection			
(dc − 50kHz)	μV/V (max)	100 (200)	*
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +125
Storage	°C	−55 to +125	*
MTBF[2]			
Mean Time Between Failures	hours	466,797	*
PACKAGE OPTION[3]		HY14D	*

NOTES
*Specifications same as Model ADSHC-85.
[1]Recommended power supply ADI Model 902-2 ±15V @ ±100mA
[2]Calculated using MIL-HNBK-217; Ground; Fixed; +70°C case
[3]See Section 19 for package outline information.
Specifications subject to change without notice.

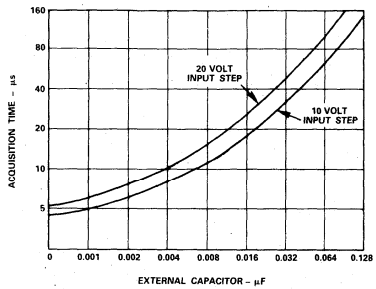


Figure 1.

As shown in Figure 2, two different intervals of time can affect the point on the analog input which is sampled when the T/H is switched from "track" to "hold". One of these, aperture time, is a constant and, therefore, should not be regarded as an error source. The other, aperture uncertainty (or "jitter"), may vary from one "hold" command to the next and qualifies as a valid error source.

This "jitter" is the result of noise signals of various kinds which modulate the phase of the hold command and are manifested as sample-to-sample variations in the value of the analog input which is being "frozen". The aperture error which results from this jitter is directly related to the dV/dt of the analog input.

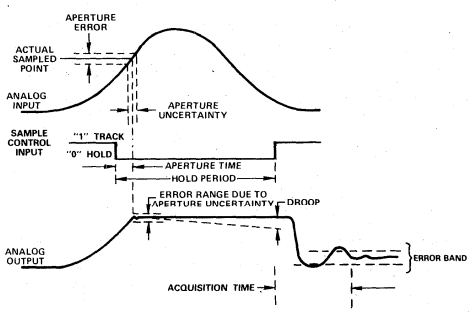


Figure 2. Track-and-Hold Operation

Another phenomenon associated with the hold period which can contribute to error is feedthrough. High feedthrough rejection is important in a track-and-hold to prevent leakage from input to output during the hold interval.

Acquisition time is the interval required for the T/H to reestablish accurate tracking of the analog input signal after the "hold" period has ended.

Longer intervals will be required for greater accuracy; but the interval is also affected by the rate of change of the input. Nyquist sampling is the most stringent tracking requirement.

SAMPLE-AND-HOLD (S/H)MODE

In the S/H mode, the output of the ADSHC-85 is left in the "hold" mode most of the time, but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse at the MODE CONTROL input is dictated by (1) the acquisition time of the ADSHC-85, in combination with (2) the desired accuracy of the sampled output.

A third factor which affects the accuracy is the amount of change which has occurred since the preceding sample; this is analogous to the situation which happens between successive "hold" commands when operating as a T/H.

OPTIONAL EXTERNAL CAPACITOR

The droop, charge offset, and acquisition time of the ADSHC-85 are determined by the holding capacitor.

(Charge offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switching FET when switching into "hold". The charge is essentially restored by a compensation circuit inside the ADSHC-85 when the unit goes into the "hold" mode.)

The droop rate can be reduced with the use of an external capacitor, but this technique is not an unmixed blessing, since additional capacitance which improves droop rate characteristics also adds to settling time.

Figure 1 approximates the relationship of acquisition time and added external capacitance. The droop rate is determined by:

$$\text{Droop} = \frac{dV}{dt} = \frac{0.5 \times 10^{-9}}{1{,}000\text{pF} + C_{ext}}$$

OFFSET ADJUSTMENT

Offset in the Functional Diagram should be adjusted with the analog input grounded, and with the sample/hold switching continuously between the "sample" and "hold" modes.

Output offset error is adjusted to zero when the unit is in the "hold" mode. This will compensate for both charge offset (see above) and amplifier offset.

APPLICATIONS

The most common application for a track-and-hold is to place it ahead of a converter to allow digitizing of signals with bandwidths higher than the converter alone can handle.

For these kinds of applications, the ADSHC-85 series can reduce system aperture to 500 picoseconds or less.

Their ability to be operated as either track-and-hold or sample-and-hold devices adds to their flexibility, and makes them appropriate for multiple uses.

OPERATION WITH A/D CONVERTER

Figure 3 shows in simplified form the use of an ADSHC-85 as a track-and-hold in combination with a converter.

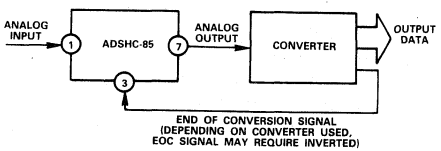


Figure 3.

The maximum value of input signal frequency that can be acquired and digitized using this combination is influenced by the bandwidth of the T/H, but is also dictated by:

A. The aperture uncertainty (jitter) of the ADSHC-85
and
B. The desired accuracy, and corresponding resolution of the converter (the larger the number of bits, the lower the maximum instantaneous input frequency).

If the desired accuracy of digitizing were 0.1% to a tolerance of ± 1/2LSB, the maximum value of input signal frequency which can be digitized is determined by:

$$F\,max = \frac{2^{-N}}{2\pi T_a} = \frac{1}{2\pi \cdot 1{,}024 \cdot 5 \times 10^{-10}} = 310.8\text{kHz}$$

where 0.1% is 10 bits; and aperture uncertainty of the ADSHC-85 is 0.5ns.

For this situation, the converter in Figure 3 could be either the Analog Devices Model HAS-1002, or the Analog Devices Model AD579.

Either of these units and the ADSHC-85 could acquire and digitize an analog input frequency of slightly less than 311kHz.

The maximum throughput rate of each of these combinations would be different, however.

When using an ADSHC-85 with HAS-1002, throughput would be 169k samples per second (a period of 4.5μs plus 1.4μs). Using the AD579 results in 154k (4.5μs plus 2.0μs). NOTE: These update rates are based on using the ADSHC-85 without external capacitance; none is required because droop is insignificant during the conversion time.

Without violating the Nyquist sampling theorem, the HAS-1002 could be used for input frequencies from dc through 84kHz; the AD579 for inputs from dc through 77kHz. Input frequencies higher than these (up to the maximum of 311kHz) would result in "undersampling" of the input signal. Signals up to 311kHz could be processed if their bandwidth is less than one-half the sample frequency (example: IF signals).

SIMULTANEOUS SAMPLE/HOLD

The ADSHC-85 can be used for time correlation of sampled data signals by using one sample/hold for each analog signal. The outputs of the units are then applied to the input of an analog multiplexer.

The worst-case droop error of the sample/hold in the last channel to be sampled is determined by the maximum "Hold" time of the system. This maximum hold time, in turn, is established by the A/D conversion rate, and the number of data channels.

Droop error is computed by:

MAX DROOP ERROR (for Channel N) = (T × n) (Droop Rate)

where $T = \frac{1}{\text{A/D Conversion Rate}}$

and n = number of multiplexer data channels

Figure 4 shows an 8-channel system using ADSHC-85 units for simultaneous sampling. Their outputs are applied to either a Model AD7501 or Model AD7503 CMOS analog multiplexer; the output of the MUX is then applied through an amplifier to a Model HAS-1202.

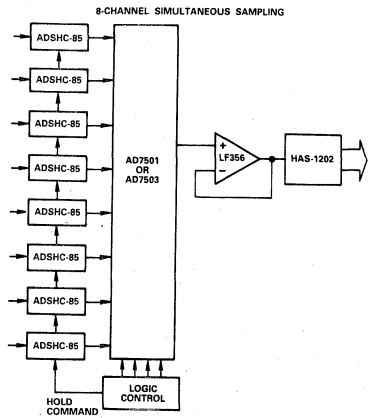


Figure 4.

When the input signal range is ± 10 volts, this 12-bit system will have a value for the Least Significant Bit (LSB) of slightly less than 5mV (4.88mV).

If the system is going to maintain 12-bit integrity, the droop rate must be appreciably less than 1/2LSB. In this example, if one assumes a system sample rate of 20kHz, the computed droop error of the last channel meets that requirement:

$$\text{Droop} = \left(\frac{1}{\text{System Sample Rate}}\right) (\text{max T/H droop})$$

$$\text{Droop} = \left(\frac{1}{20 \times 10^3}\right) (0.5\text{mV/ms}) = 25\mu\text{V}$$

The computed droop error is negligible; therefore, no external capacitance need be added to the ADSHC-85s. This should hold true for all except the very slowest A/Ds which might be substituted for the HAS-1202.

RECOMMENDED CONVERTERS

The application notes above offer suggestions on converters from the Analog Devices product line which are candidates for use with the ADSHC-85 Sample/Hold units.

Depending on the application and desired resolution, a number of units should be considered.

They include:

ADC84	AD579	HAS-1202	MAS-0801
ADC85	HAS-0802	MAH-0801	MAS-1001
AD578	HAS-1002	MAH-1001	MAS-1202

ANALOG DEVICES

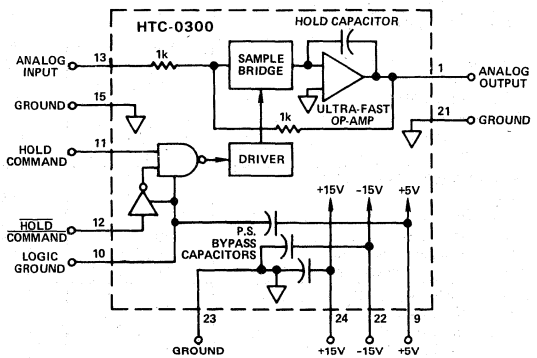
Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTC-0300

FEATURES
Aperture Jitter of 100ps
Input Range ±10V
Output Current ±50mA
Max Droop Rate 5μV/μs

APPLICATIONS
Data Acquisition Systems
Peak Measurement Systems
Simultaneous Sample & Hold
Analog Delay

HTC-0300 FUNCTIONAL BLOCK DIAGRAM



NOTE: PIN 12 SHOULD BE GROUNDED IF NOT USED.

GENERAL DESCRIPTION

The HTC-0300 is a hybrid microcircuit track-and-hold amplifier useable for a wide range of signal processing applications, including waveform measurements, analog signal delay, and signal sampling.

The HTC-0300 has an aperture jitter of only 100 picoseconds; wide dynamic input range of ±10 volts; and laser-trimmed gain and offset which preclude the need for external adjustments. Its speed and precision are the result of innovative design techniques using high-speed op amps and diode switches. These techniques also enhance the HTC-0300 performance in feedthrough rejection, linearity, harmonic distortion, droop rate, and output voltage swing.

Applications which require a minimum temperature coefficient on offset voltage and a slight increase in bandwidth are likely candidates for the "A" series of the HTC-0300 family.

Units are available in glass packages as the HTC-0300 and HTC-0300A; and in metal packages as the HTC-0300M and HTC-0300AM.

ORDERING INFORMATION

Models HTC-0300 and HTC-0300A are ceramic package versions; models HTC-0300M and HTC-0300AM are hermetically-sealed metal packages.

Mating individual pin sockets are available from AMP. Part number 6-330808-0 is the knockout end type; part number 6-330808-3 is the open end type.

APPLICATIONS

Track-and-hold amplifiers can be used in a number of different ways, but the most common application for these units is to place them ahead of an A/D converter to digitize signals with bandwidths higher than the digitizer can handle by itself.

The HTC-0300 is designed to be used with the Analog Devices HAS-Series of A/D converters; but it lends itself readily for use with the Analog Devices hybrid AD578, AD579, ADC84, ADC85 as well as the modular MAH and MAS units.

The use of the HTC-0300 T/H can reduce system aperture to 100 picoseconds, when used with the appropriate A/D converter. It can also be used for peak-holding functions, simultaneous sampling A/D's (when combined with analog multiplexers), and other high-speed analog signal processing applications.

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SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

	UNITS	HTC-0300	HTC-0300A	HTC-0300M[1]	HTC-0300AM[1]
ANALOG INPUT					
Voltage Range	V	±10	*	*	*
Overvoltage, no damage	V max	±15	*	*	*
Impedance	Ω (max)	1,000 (±50)	*	*	*
Initial Offset Voltage	mV (max)	±2 (±20)	*	*	*
DIGITAL INPUT (TTL Compatible)					
Mode Control					
Hold Input $\overline{\text{Hold}}$ Input		Voltage	Current		
"0" = Track "0" = Hold		0V to +0.4V	−2mA max	*	*	*
"1" = Hold "1" = Track		+2.5V to +5V	50μA max	*	*	*
ANALOG OUTPUT					
Voltage	V min	±10	*	*	*
Current (not short circuit protected)	mA max	±50	*	*	*
Impedance (dc)	Ω (max)	0.1 (1.0)	*	*	*
Noise in Track Mode[2]					
@ 100kHz	μV rms	15	*	*	*
@ 1.0MHz	μV rms	34	*	*	*
@ 5.0MHz	mV rms	0.1	*	*	*
DC ACCURACY/STABILITY					
Gain	V/V	−1.00	*	*	*
Gain Error	%	±0.2	*	*	*
Gain Nonlinearity	% max	±0.01	*	*	*
Gain Temperature Coefficient	ppm/°C (max)	10 (50)	*	*	*
Input Offset vs. Temperature	μV/°C (max)	400 (750)	100 (200)	*	**
SAMPLE (TRACK) MODE DYNAMICS					
Frequency Response					
Small Signal (−3dB)	MHz	8	10	*	**
Full Power (−3dB)	MHz	6	8	*	**
Slew Rate	V/μs (min)	250 (120)	260 (180)	250 (100)	**
Harmonic Distortion (4V p-p; R_L = 1k)	dB (max)	75 (62)	*	*	*
SAMPLE (TRACK)-TO-HOLD SWITCHING					
Aperture Time	ns (max)	6 (±2)	*	*	*
Aperture Uncertainity (Jitter)	ps (rms) max	100	*	*	*
Offset Step (Pedestal)	mV (max)	5 (50)	5 (20)	*	**
Sensitivity to Temperature	μV/°C (max)	200 (400)	100 (200)	*	**
Sensitivity to +5V	mV/V	60	25	*	**
Switching Transient					
Amplitude	mV	200	*	*	*
Settling to 0.1%	ns (max)	100 (200)	*	*	*
HOLD MODE DYNAMICS					
Droop Rate	μV/μs (max)	5 (7)	1.0 (5)	*	**
Variation with Temperature		Doubles/10°C change	*	*	*
Feedthrough Rejection					
(20V p-p dc to 2.5MHz)	dB	70	74	*	**
HOLD-TO-SAMPLE (TRACK) DYNAMICS					
Acquisition Time (to ±0.1%)					
10V Step	ns (max)	170 (200)	150 (170)	*	**
20V Step	ns (max)	220 (270)	200 (250)	*	**
POWER REQUIREMENTS					
Nominal Voltages					
Power Supplies	V (±)	±15 (3)	*	*	*
Logic Supply	V (±)	+5 (0.25)	*	*	*
Currents					
+15V	mA, max	38	28	*	**
−15V	mA, max	27	21	*	**
+5V	mA, max	25	*	*	*
Power Dissipation	mW, max	1100	860	*	**
Power Supply Rejection Ratio ±15V					
(dc to 50kHz)	mV/V	0.5	*	*	*
TEMPERATURE RANGE					
Operating (case)	°C	0 to +70	*	−55 to +100	−55 to +125
Storage	°C	−55 to +125	*	*	*
THERMAL RESISTANCE[3]					
Junction to Air, θja (free air)	°C/W	48	*	45	45
Junction to Case, θjc	°C/W	20	*	12	12
MTBF[4]					
Mean Time Between Failures	hours			6.44×10^5	9.4×10^5
PACKAGE OPTIONS[5]		HY24E	*	HY24G	**

NOTES
*Specifications same as HTC-0300.
**Specifications same as HTC-0300A.
[1]"MB" version specs same as "M" versions.
[2]Noise level increases when high duty cycle repetitive hold command is applied.
[3]Maximum junction temperature is 150°C.
[4]Calculated for "MB" versions using MIL-HNBK-217; Ground Fixed; +70°C case.
[5]See Section 19 for package outline information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

PIN DESIGNATIONS

PIN	FUNCTION
1	ANALOG OUTPUT
2	N/A
3	N/A
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	+5V
10	LOGIC GROUND
11	HOLD
12	$\overline{\text{HOLD}}$
13	ANALOG INPUT
15	GROUND
18	N/A
19	N/A
21	GROUND
22	-15V
23	GROUND
24	+15V

TRACK-AND-HOLD (T/H) MODE

When operated in the "track" mode, the HTC-0300 functions as an operational amplifier with a gain of −1, following all changes in the analog input signal as they occur.

When a TTL-compatible digital logic "1" is applied to the Hold Command input (Pin 11) of the T/H, the inverted analog output of the HTC-0300 is "held" at the value which was present at the time of the Hold Command, plus the aperture time.

For applications which require an inverted Hold Command, this "freezing" of the inverted analog output can be accomplished with a digital "0" applied to the $\overline{\text{Hold}}$ input port (Pin 12); in this case, a digital"1" establishes the "track" mode of operation.

Refer to Figure 1, the Track/Hold Waveforms for the HTC-0300.

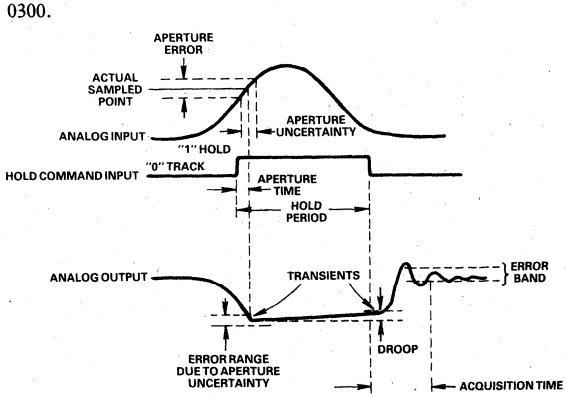


Figure 1. Track/Hold Waveforms–HTC-0300

As shown, two different intervals of time can affect the point on the analog input which is sampled when the T/H is switched from "track" to "hold" (there is no major difference in operation whether this change in state is accomplished via the Hold or $\overline{\text{Hold}}$ input; the functioning of the HTC-0300 is essentially the same, with only a slight difference in timing because of an additional logic package in the $\overline{\text{Hold}}$ signal path.)

The delay interval, aperture time, is a constant and, therefore, should not be regarded as an error source. The care used in the design of the HTC-0300 assures that aperture time is within its spec from unit to unit; and is also repeatable from one "hold" command to the next in any given unit. In this way, aperture time can be compensated with system timing to assure an optimum sampling point on the signal being digitized. Refer to Figure 2.

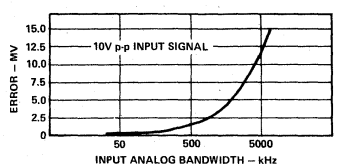


Figure 2. HTC-0300 Error Due to Aperture Uncertainty

The other interval affecting the held value is aperture uncertainty, or "jitter." It is the result of noise signals of various kinds which modulate the phase of the hold command and shows up as sample-to-sample variations in the value of the analog signal which is being "frozen."

The error resulting from this jitter, as one might expect, is directly related to the dV/dt of the analog input being applied to the HTC-0300 T/H. If very high-speed inputs are sampled, any given value of jitter will result in larger errors in the held value at the output as the dV/dt increases.

The high feedthrough rejection of the HTC-0300 is an important characteristic of the unit in the hold mode because it precludes errors being introduced during the conversion interval of the digitizer used at the output of the T/H. Basically, high feedthrough

rejection is important to prevent leakage from analog input to analog output during the hold interval.

As shown in Figure 1, droop is the amount the output changes during the hold period; this change is the result of loading on the internal hold capacitor. Low droop rates are important in using track-and-hold amplifiers with converters to assure they are appropriate for applications requiring high-resolution digitizing. Excessive droop rates can negate the effectiveness of having converters of 10 or 12 bits or more; the lower-order bits may be in error because of the change in the value being held during the conversion cycle. This comment is particularly germane to successive-approximation converters.

The return to the "track" mode at the end of the hold period is accomplished by changing the digital logic level of the Hold Command; Figure 1 depicts the hold command as it would appear at the (Pin 11) Hold input.

Acquisition Time is the interval required for the analog output to reestablish accurate tracking of the changing input and remain within a specified error band around its final value. Not unexpectedly, the greater the change in the input value, the longer this interval will be. Nyquist sampling is the most stringent application.

The transients shown in Figure 1 are "spikes" which occur on the output of the T/H at the beginning and end of the "hold" period because of switching transients within the unit. When a track-and-hold is used at the output of a D/A converter for "deglitching" discontinuities in the output of the converter, these transients occur at the update rate and can be filtered.

SAMPLE-AND-HOLD (S/H) MODE

Although it is generally used in the track-and-hold mode as described above, the HTC-0300 can also be used as a sample-and-hold device for applications requiring this capability.

In the S/H mode, the output of the unit is usually in the "hold" mode, but is switched to the "sample" (track) mode of operation for brief intervals.

The width of the sample pulse which is applied to the $\overline{\text{Hold}}$ input (or, if using inverted logic, the Hold input) is determined by (1) the acquisition time of the HTC-0300, and (2) the desired accuracy of the sampled output.

In addition to these considerations, the accuracy of the output will also be a function of the amount of change which has occurred since the preceding sample.

This latter phenomenon is illustrated in Figure 3. In that drawing, the analog input has changed drastically between the first and second hold commands. There is a considerably smaller change between the third and fourth pulses; as a consequence, movement in the held value of the output is correspondingly smaller.

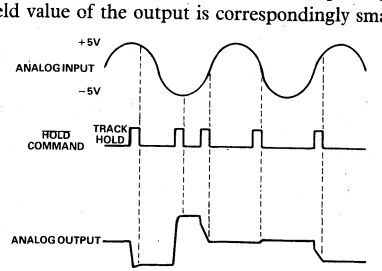


Figure 3. Sample/Hold Operation

Refer to Figure 4, which illustrates settling accuracy versus acquisition time. This graph shows dramatically that closer accuracies require increasing amounts of time to acquire the signal. As shown, the relationship approaches an asymptotic curve and is not a linear function.

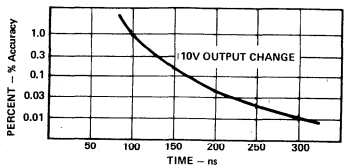


Figure 4. Settling Accuracy vs. Acquisition Time

As in any amplifier, amplitude and phase response are important in the HTC-0300. Typical phase and gain characteristics versus input frequency are shown in Figure 5. The two parameters are

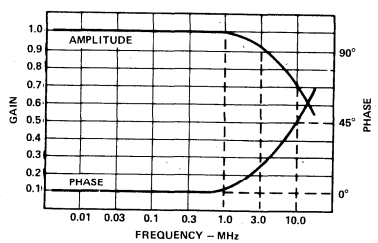


Figure 5. Amplitude and Phase Response

relatively flat from dc to 1-2MHz and then decay gracefully to help assure stable operation. As shown, the cutoff frequency is approximately 10MHz.

The HTC-0300 is suitable for most applications requiring a track-and-hold for update rates up to 5MHz. (Note: In this instance, 5MHz conversion rates are only a guide and are based on system acquisition time, not logic speed. Higher rates are possible with trade-offs in acquisition time.)

The HTC-0300 is a "closed loop" track-and-hold unit. As shown in the block diagram, the switches are located within the feedback loop, hence the "closed loop" nomenclature.

The internal power supply bypass capacitors which are shown may have to be supplemented with external bypassing, depending upon the application. For most applications, electrolytic capacitors of 10-22 microfarads on each supply will enhance performance of the unit.

Bypassing all power supplies with 0.01 – 0.1μF ceramics is another of the considerations in assuring optimum performance. A massive ground plane, careful component layout, and physically separating digital and analog signals as much as possible are also among the multitude of items which can affect the operation of circuits containing the HTC-0300 track-and-hold.

Cross-coupling of analog and digital signals is generally the major problem at high frequencies. Relatively low levels of ground plane noise can "mask" lower-order bits when the HTC-0300 is used in high-resolution digitizing. The user should exercise great care in both electrical and mechanical design to assure satisfactory performance.

High Speed Hybrid Track-and-Hold Amplifiers

HTC-0500

FEATURES
700ns Acquisition Time
<750mW Power Dissipation
14-Pin DIP
0.01% Linearity

APPLICATIONS
Data Acquisition Systems
Data Distribution Systems
Analog Delay and Storage
Peak Amplitude Measurements

GENERAL DESCRIPTION

The Analog Devices HTC-0500 Track/Sample Hold is a remarkable combination of speed and low power dissipation in a 14-pin DIP. Its low cost makes it extremely attractive for a wide range of applications which were often uneconomical until now.

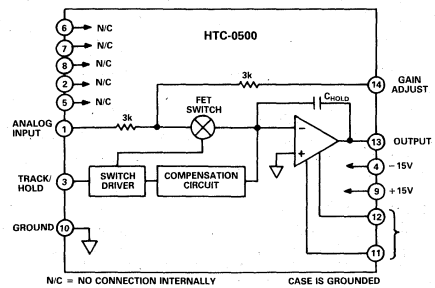
Exceptional speed and minimum power in a small, cost-effective package are not the only characteristics which make this unit worth serious consideration for a variety of uses. The innovative design ideas which have been included make it possible for the user to vary the gain of this inverting amplifier.

In many instances, Track/Sample-Hold devices may allow the user to decrease the gain, but increasing the gain is impossible. This is because the majority of these units close the feedback loop internally.

The HTC-0500, however, gives the designer flexibility when it is incorporated into its system application because it can be varied around its normal unity gain. In fact, as shown in the functional block diagram, the user must close the feedback loop externally with a strap to get proper operation.

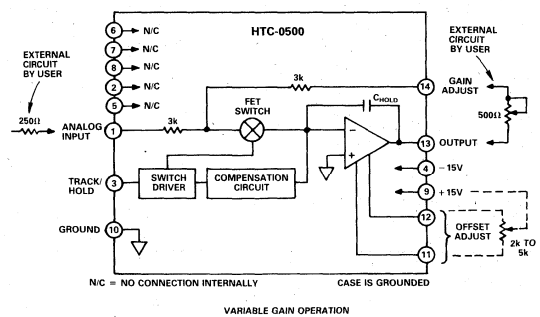
Figure 2 shows a suggested method for changing gain over a range which is approximately 8 percent below to approximately 17 percent above nominal. This kind of potential gain variation can be an important element when the HTC-0500 is combined with other components in a system design. The gain of the HTC-0500 can be changed as necessary to compensate for variations in other portions of the system. External adjustments also allow the offset to be nulled.

HTC-0500 FUNCTIONAL BLOCK DIAGRAM



The HTC-0500 is a perfect choice for use with Analog Devices' converters such as the HAS-1202, AD578, and AD579 in applications which do not require the speed of the model HTC-0300 Track-and-Hold, but require higher speed than the ADSHC-85.

The standard unit is housed in a metal dual in-line package; its model number is HTC-0500AM. A temperature range of −55°C to +125°C is available with model HTC-0500SM.



VARIABLE GAIN OPERATION

Figure 2.

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SPECIFICATIONS (typical @ +25°C, and nominal power supply voltage unless otherwise noted)

	UNITS	HTC-0500AM	HTC-0500SM
ANALOG INPUT			
Voltage Range	V (min)	±12 (±10)	*
Overvoltage, no damage	V, max	±15	*
Impedance	Ω (max)	3000 (±15)	*
Initial Offset Voltage	mV, max	±5, adjustable to zero	*
DIGITAL INPUT (TTL Compatible)			
Mode Control	Voltage	Current	
"Sample/Track" Logic "0"	0V to +0.8V	2 Standard TTL Loads	*
"Hold" Logic "1"	+2.0V to +5.5V	2 Standard TTL Loads	*
ANALOG OUTPUT			
Voltage	V (min)	±12 (±10)	*
Current	mA (min)	±15 (±10)	*
Impedance	Ω, max	1	*
Noise			
dc to 100kHz } Track Mode	μV rms	15	*
dc to 1.0 MHz } Track Mode	μV rms	60	*
DC ACCURACY/STABILITY			
Gain	V/V	−1.00	*
Gain Error	% (max)	±0.1 (±0.2)	*
Gain Nonlinearity (±10V Output)	% (max)	±0.01 (±0.02)	*
Gain Temperature Coefficient	ppm/°C (max)	10 (15)	*
Input Offset vs. Temperature (Track)	μV/°C (max)	100 (200)	*
SAMPLE (TRACK) MODE DYNAMICS			
Frequency Response			
Small Signal (−3dB)	MHz (min)	2 (1.5)	*
Large Signal (−3dB)	MHz (min)	1.5 (1)	*
Slew Rate	V/μs (min)	55 (40)	*
SAMPLE (TRACK)-TO-HOLD SWITCHING			
Aperture Time	ns (max)	30 (±5)	*
Aperture Uncertainty (Jitter)	ps (max)	60 (100)	*
Offset Step (Pedestal)	mV, max	±5	*
Variation with Temperature	μV/°C, max	25	*
Switching Transient			
Amplitude	mV, max	100	*
Settling to 1mV	ns (max)	400 (600)	*
HOLD MODE DYNAMICS			
Droop Rate	μV/μs (max)	0.5 (2)	*
Variation with Temperature		Doubles/10°C Change	*
Feedthrough Rejection			
(10V p-p @ 300kHz)	dB (min)	80 (75)	*
HOLD-TO-SAMPLE (TRACK) DYNAMICS			
Acquisition Time (to ±0.1%)			
10V Step	ns (max)	700 (800)	*
20V Step	ns (max)	900 (1100)	*
Acquisition Time (to ±0.01%)			
10V Step	ns (max)	850 (1000)	*
20V Step	ns (max)	1100 (1300)	*
POWER REQUIREMENTS[1]			
Nominal Voltages	V (%)	±15 (±3)	*
Current	mA (max)	±25 (±27)	*
Power Supply Rejection			
(dc − 50kHz)	mV/V (max)	1.5 (3)	*
Pedestal Sensitivity to			
Power Supply			
+15V	mV/V (max)	3 (5)	*
−15V	mV/V (max)	3 (5)	*
Power Dissipation	mW (max)	750 (810)	*
TEMPERATURE RANGE			
Operating (Case)	°C	−25 to +85	−55 to +125
Storage	°C	−55 to +125	*
THERMAL RESISTANCE[2]			
Junction to Air, θja (free air)	°C/W	53	*
Junction to Case, θjc	°C/W	12	*
MTBF			
Mean Time Between Failures	hours		5.48×10^5
PACKAGE OPTION[3]			
14-Pin Metal DIL		HY14D	*

NOTES
*Specifications same as HTC-500AM.
[1]Recommended power supply ADI Model 902-2 ±15V @ ±100mA.
[2]Maximum junction temperature is 150°C.
[3]See Section 19 for package outline information.
Specifications subject to change without notice.

APPLICATIONS

The HTC-0500 Track-and-Hold amplifier bridges the gap in price/performance trade-offs between monolithic Sample-Hold amplifiers such as the Analog Devices AD582 and AD583; and high-speed hybrid T/Hs such as the Analog Devices HTC-0300 and HTS-0025.

Designs which require faster acquisition speeds than those available with the AD582, AD583 or ADSHC-85, but do not need the high performance capabilities of either the HTC-0300 or HTS-0025, are ideal candidates for the HTC-0500.

The hallmarks of the HTC-0500 family are outstanding performance in a small 14-pin hybrid package at an economical price, which provides the designer with a cost-effective solution to digitizing applications.

TRACK-AND-HOLD (T/H) MODE

The HTC-0500, like other track-and-hold units, is a circuit which can continuously follow a changing analog signal; but can quickly switch into a hold mode to "capture" or "freeze" the signal at a point selected by the user. After the desired hold interval is completed, it is returned to the track mode of operation and reacquires the input signal.

Generally speaking, the HTC-0500 is used ahead of analog-to-digital converters to allow digitizing signals whose bandwidth is too high for the A/D alone to handle. It can also be used as a deglitcher on the output of D/A converters; analog holding functions, and for other processing of analog signals.

The T/H used with an A/D directly affects multiple parameters of performance within the system; resolution, accuracy, signal-handling capabilities, and multiple other characteristics are dependent on both the track-and-hold and the converter. The user needs to understand the interactions between the devices to assure optimum system use.

In the "track" mode, the HTC-0500 operates as an amplifier with a gain of -1, following all changes in the analog input.

The user determines the point at which the analog input will be "captured" by applying a TTL digital "1" logic signal to the Track/Hold (Pin 3) input of the HTC-0500. The inverted analog output of the HTC-0500 is "held" at the value which was present at the time of the Hold Command, plus the aperture time.

The time relationships and the characteristics which affect the performance are illustrated in Figure 3.

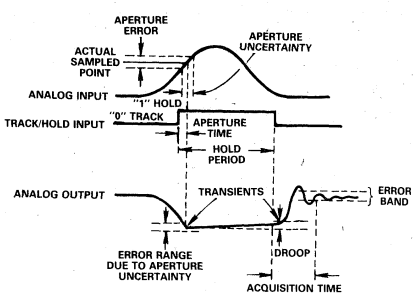


Figure 3. Track-and-Hold Operation

As shown, aperture time is a predictable, repeatable delay between the application of the Hold Command and the instant the analog input is sampled. Because of its characteristics, aperture delay should not be considered an error source, since it can be negated with correct system timing. Careful attention to the timing used within the system will assure the "freezing" of the signal being digitized will occur at the optimum point on the changing analog input.

Aperture uncertainty (or "jitter"), on the other hand, is a valid error source which has an effect on the sample point. This uncertainty is the result of noise signals of various kinds which modulate the phase of the hold command; its results show up as variations in the value of the signal being "captured," on a sample-to-sample basis. These variations manifest themselves as an effective aperture error on the input signal and a corresponding range of errors in the analog output which is "held".

The width of the aperture error (and, consequently, the output error range) is directly related to the dV/dt of the analog input. If one assigns a fixed aperture error for purposes of illustration, it is easy to visualize the effect of increasing the dV/dt of the analog signal; the error range at the output increases as the bandwidth of the input increases.

The amount of error vis-a-vis bandwidth is illustrated in Figure 4.

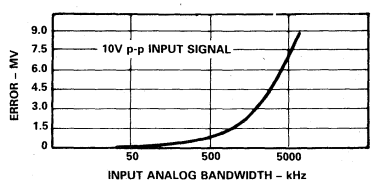


Figure 4. HTC-0500 Error Due to Aperture Uncertainty

The droop shown in Figure 3 is the amount the analog output changes during the hold period and is the result of loading on the internal hold capacitor. The exceptionally low droop rate of the HTC-0500 is a "plus" for the system designer interested in using the unit with high-resolution A/D converters. Excessive droop rates in a T/H can cause converters of 10 or 12 bits or more to perform at less than their rated accuracies; the lower-order bits might be in error if there is a change at the converter input during the conversion cycle. Using the HTC-0500 for these kinds of applications decreases that possibility.

The acquisition time shown in Figure 3 is the interval from the change of state of the Hold Command to the time when the analog output has been reacquired and remains within a specified error band around its final value. Nyquist sampling is the most stringent application, since this would cause the maximum change from one sample to the next.

As shown in the SPECIFICATIONS section, the acquisition time of the HTC-0500 is truly remarkable for a unit in its price category, even when settling to accuracies of 0.01%. This characteristic makes it extremely attractive for the user who cannot compromise technical performance, but must also consider the economic consequences of his design.

The transients which are called out in Figure 3 are "spikes" which occur on the output of the T/H at the beginning and end of the hold period; they are the result of switching transients within the unit.

Refer to Figure 5, which illustrates these switching transients, and pedestal voltage; and their time relationships to the Hold

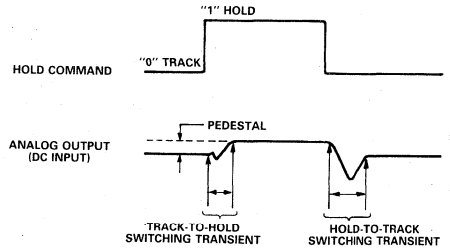


Figure 5.

Command. No inference should be drawn from the illustration regarding the relative amplitudes of the Hold Command, transients, and pedestal; refer elsewhere in this data sheet for actual values.

Pedestal during the hold period is a sample-to-hold offset caused by charge dumps when electronic switches are opened; coupling of the logic signal transients; and other phenomena. This pedestal can be eliminated with calibration when using the HTC-0500 with an A/D converter, since it shows up as an offset.

SAMPLE-AND-HOLD (S/H) MODE

Although it is classified as a track-and-hold unit and is usually operated in that mode as described above, the HTC-0500 can also be used as a sample-and-hold device.

When used in this manner, the output of the unit remains in the "hold" mode most of the time, but is switched to the "sample" (track) mode for brief intervals.

Refer to Figure 6.

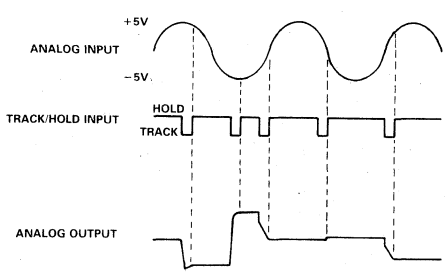


Figure 6. Sample/Hold Operation

When operating as a S/H, the signal applied to the Track/Hold (Pin 3) input will usually be a digital logic "1" which holds the HTC-0500 output at the input value present at the time of the leading edge of the Track/Hold pulse.

Figure 6 shows asynchronous pulses applied to cause the output to reslew to new values. The trailing edge establishes the sample (track) mode; the leading edge returns the output to "hold".

The exceptional acquisition time of the HTC-0500 makes it attractive for sample-hold applications because of its ability to acquire new output values quickly. This characteristic allows the width of the sample pulse to be considerably narrower than might be possible if using competing units.

The width of the sampling pulse applied at the Track/Hold input will be dependent on:

A. The acquisition time of the HTC-0500
B. The desired accuracy of the sample output
C. The amount of change which has occurred since the preceding sample.

Settling accuracy versus acquisition time is shown pictorially in Figure 7.

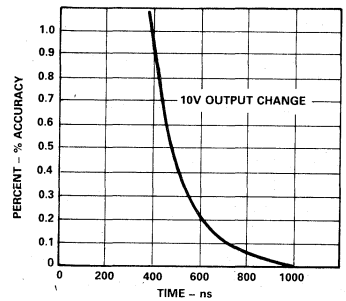


Figure 7. Settling Accuracy vs. Acquisition Time – HTC-0500

When operating in the track mode, the HTC-0500 is no different from any other amplifier; phase and gain are important to assure stable operation. In Figure 8, these charcteristics are plotted as a function of input frequency.

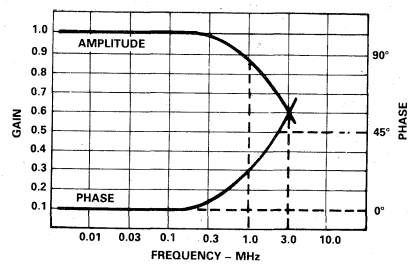


Figure 8. Amplitude and Phase Response – HTC-0500

ORDERING INFORMATION

All versions of the HTC-0500 are housed in 14-pin metal dual in-line packages. For commercial applications operating over a case temperature range of −25°C to +85°C, specify model HTC-0500AM. For a temperature range of −55°C to +125°C, specify model HTC-0500SM.

Mating individual pin sockets are available from AMP. Knock-out end type are part number 6-330808-0; open end type are 6-330808-3.

ANALOG DEVICES

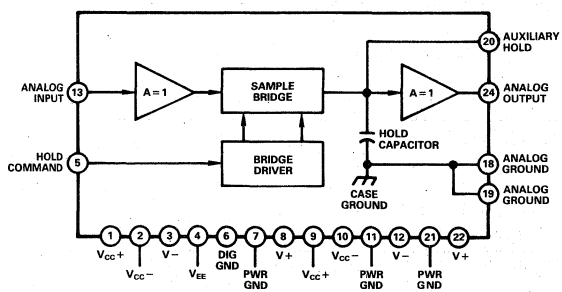
Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTS-0010

FEATURES
Aperture Jitter of 5ps
Acquisition Time 10ns
Output Current ±40mA
Slew Rate 300V/μs

APPLICATIONS
Data Acquisition Systems
Radar Systems
Instrumentation Systems
Medical Electronics

HTS-0010 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices HTS-0010 Track-and-Hold is another example of Analog's continuing efforts to advance the state of the art in high-speed circuits.

The HTS-0010 adds breadth to a line of devices which offers designers the industry's widest range of track-and-hold and sample-and-hold units.

Its pinouts are similar to its predecessor HTS-0025 Track-and-Hold, but it provides enchanced performance in many of the characteristics established by that device. Two pins which are unused on the HTS-0025 are used on the HTS-0010, but with those exceptions, the two devices have identical pin assignments. This plug-in compatibility gives designers remarkable flexibility in selecting those parameters which are optimum for their applications.

The HTS-0010 Track-and-Hold (T/H) uses many of the proven design concepts which have made the HTS-0025 T/H the standard of comparison for high-speed circuits of this type. A dc-coupled Schottky diode bridge is driven by a high impedance buffer amplifier and followed by a low impedance output amplifier to achieve the best possible combination of speed and drive capabilities.

All models of the HTS-0010 are housed in a standard 24-pin metal DIP. The unit operating over a temperature range of 0 to +70°C is HTS-0010KD; the unit for a range of −55°C to +100°C is HTS-0010SD.

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SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

	Units	HTS-0010KD	HTS-0010SD
ANALOG INPUT			
Voltage Range			
For Rated Performance	V p-p	2	*
Maximum Without Damage	V	±3	*
Impedance	Ω	10^5	*
Capacitance	pF max	7	*
Bias Current	μA max	20	*
DIGITAL INPUT (ECL Compatible)			
Mode Control			
Hold Command Input			
"0" = Track	V	−1.5 to −1.8	*
"1" = Hold	V	−0.8 to −1.1	*
ANALOG OUTPUT			
Current (Not Short Circuit Protected)	mA max	±40	*
Impedance	Ω (max)	9 (12)	*
Noise in Track Mode			
@ 5.0MHz Bandwidth	μV rms (max)	20 (40)	*
DC ACCURACY/STABILITY (FS = Full Scale)			
Gain (No Load)[1]	V/V (min)	0.96 (0.93)	*
Gain Nonlinearity; 2V FS Input	% max	0.1	*
Gain Nonlinearity; 1V FS Input	% max	0.01	*
Gain Temperature Coefficient	ppm/°C (max)	30 (40)	30 (50)
Initial Offset Voltage	mV (max)	±2 (±5)	*
Offset vs. Temperature	μV/°C (max)	125 (175)	*
TRACK (SAMPLE) MODE DYNAMICS			
Frequency Response			
Full Power Bandwidth	MHz min	40	*
Small Signal (−3dB) Bandwidth	MHz min	60	*
Slew Rate	V/μs (min)	300 (250)	*
Harmonic Distortion (Track Mode;			
4MHz, 2V p-p Input)			
R_L = 1kΩ	dB max	−68	*
R_L = 500Ω	dB max	−65	*
R_L = 200Ω	dB max	−64	*
R_L = 75Ω	dB max	−50	*
TRACK (SAMPLE)-TO-HOLD SWITCHING			
Effective Aperture Delay Time[2]	ns (max)	−2 (±1)	*
Aperture Uncertainty (Jitter)	ps (rms)max	5	*
Offset Step (Pedestal)	mV (max)	±2 (±10)	*
Sensitivity to Temperature	μV/°C max	50	250[3]
Sensitivity to −5.2V	mV/V max	10	*
Switch Delay Time	ns	1.5	*
Switching Transient			
Amplitude	mV (max)	15 (30)	*
Settling to 1mV	ns (max)	5 (14)	*
HOLD MODE DYNAMICS			
Droop Rate	mV/μs max	0.1	*
Variation with Temperature[4]		Doubles/10°C Change	
Feedthrough Rejection			
(2V p-p Input)			
@ 1MHz	dB min	62	*
@ 10MHz	dB min	52	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS[5]			
Acquisition Time (1V Step)			
to ±1%	ns (max)	10 (15)	*
to ±0.1%	ns (max)	14 (19)	*
Acquisition Time (2V Step)			
to ±1%	ns (max)	13 (16)	*
to ±0.1%	ns (max)	16 (22)	*
Switch Delay Time	ns	1.5	*

	Units	HTS-0010KD	HTS-0010SD
POWER REQUIREMENTS			
V+ (+15V ±0.5V)	mA max	38	*
V− (−15V ±0.5V)	mA max	48	*
V_{CC}+ (+5.0V ±0.25)	mA max	20	*
V_{CC}− (−5.0V ±0.25)[6]	mA max	20	*
V_{EE} (−5.2V ±0.25)[6]	mA max	50	*
Power Dissipation	W max	1.75	*
Power Supply Rejection Ratio[7] (dc to 10kHz)	mV/V max	10	*
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +100
Storage	°C	−55 to +125	*
THERMAL RESISTANCE[8]			
Junction to Air, θja (Free Air)	°C/W	42	*
Junction to Case, θjc	°C/W	12	*
MTBF[9]			
Mean Time Between Failures	Hours		6.83×10^5
PACKAGE OPTION[10]		HY24G	*

NOTES

[1] $\text{Gain} = \frac{R_L \times 0.96}{R_L + 9}$

[2] Effective Aperture Delay Time is delay between Hold strobe and held value of analog output, referenced to analog input (see text).

[3] Pedestal temperature variation on HTS-0010SD is same as HTS-0010KD below +70°C, but increases between +70°C and +100°C.

[4] Droop rate never exceeds 3mV/μs at +70°C, nor 10mV/μs at +100°C.

[5] For acquisition time measurements, $R_L = 200\Omega$; $C_L = 3pF$.

[6] V_{CC}− may be tied to V_{EE} with adequate bypass capacitors (see text).

[7] Variations in V− (−15V) have greater effect on unit performance than variations in other supplies; PSRR shown is for V−.

[8] Maximum junction temperature is +150°C.

[9] Calculated using MIL-HNBK 217; Ground; Fixed; +70°C case temperature.

[10] See Section 19 for package outline information.

*Specifications same as HTS-0010KD.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1	V_{CC}+ (+5V)
2	V_{CC}− (−5V)
3	V− (−15V)
4	V_{EE} (−5.2V)
5	HOLD COMMAND
6	DIGITAL GROUND
7	POWER GROUND
8	V+ (+15V)
9	V_{CC}+ (+5V)
10	V_{CC}− (−5V)
11	POWER GROUND
12	V− (−15V)
13	ANALOG INPUT
14	N/A
15	N/A
16	N/A
17	N/A
18	ANALOG GROUND
19	ANALOG GROUND
20	AUXILIARY HOLD
21	POWER GROUND
22	V+ (+15V)
23	N/A
24	ANALOG OUTPUT

POWER GROUND (PINS 7, 11 AND 21), ANALOG GROUND (PINS 18 AND 19), AND DIGITAL GROUND (PIN 6) MUST BE CONNECTED TOGETHER AND TO A LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE. HYBRID CASE IS CONNECTED TO ANALOG GROUND INTERNALLY.

Applications

One of the main uses for track-and-hold (T/H) units is ahead of analog-to-digital (A/D) converters to allow digitizing signals with bandwidths higher than the A/D can handle by itself. The use of an appropriate T/H allows the converter to become a true "Nyquist converter", i.e., capable of digitizing analog signals whose maximum bandwidth is one-half the encoding rate.

The characteristics of the HTS-0010 T/H make it useful in multiple other applications beside this "standard" use of devices of this kind. It can be used in sample and hold circuits, peak holding applications, simultaneous sampling A/Ds (with appropriate analog multiplexing), and for many other data processing needs.

Refer to Figure 1, HTS-0010 Interconnection Diagram.

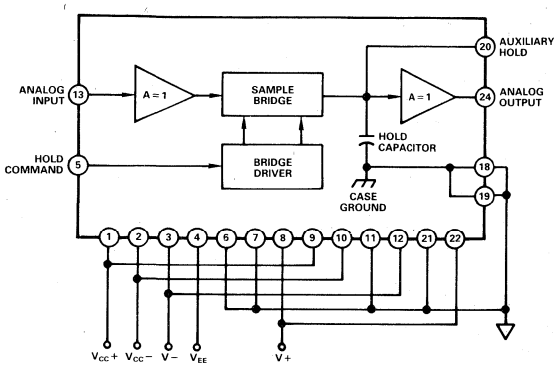


Figure 1. HTS-0010 Interconnection Diagram

Bypass capacitors are used internally on all power supply leads on the HTS-0010 track-and-hold. External bypassing of all power supplies with 0.01μF–0.1μF ceramics will help performance. In addition, electrolytic capacitors of 10-22 microfarads on each supply will also enhance the HTS-0010's operation

A massive ground plane, careful component layout, and physically separating analog and digital signals are among the other considerations which can have major effects in improving the high-speed characteristics of the HTS-0010 track-and-hold.

As shown in Figure 1, supply voltages must be applied to all pins for which they are designated. In addition, it is extremely important to connect all grounds together, and to a solid, low-impedance ground plane. These connections must be made as close to the hybrid as physically possible.

Five different voltages are shown for powering the HTS-0010. These are the voltages which are used in final test and calibration and are the recommended voltages for best performance, but minor variations from these recommendations are possible.

For best performance, the amplifier supplies, $V_{CC}-$ and $V_{CC}+$ should be equal and opposite, as shown. If desired, the ECL logic supply ($V_{EE} = -5.2V$) can be used also for $V_{CC}-$, to eliminate the need for a separate power supply voltage. If it is, bypass capacitors should be used at each supply pin to decrease the possibility of logic switching noise introducing extraneous signals.

TRACK-AND-HOLD MODE

When operated in the "track" mode, the HTS-0010 T/H functions as a buffer amplifier, following all changes in analog input as they occur. The user selects the point at which digitizing is to be done by applying an external ECL-compatible HOLD COMMAND to Pin 5.

Refer to Figure 2, Track/Hold Waveforms.

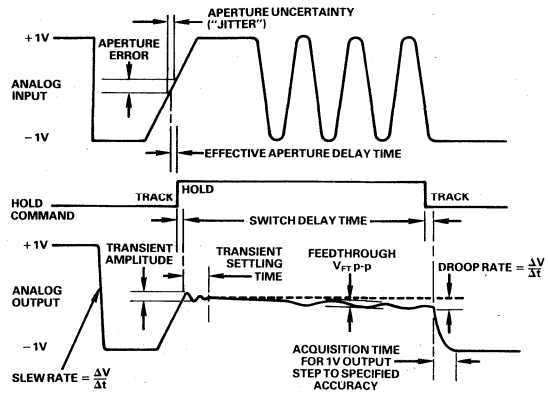


Figure 2. Track/Hold Waveforms

A varying, ideal analog input is shown at the top of Figure 2 for purposes of illustrating the response of the HTS-0010 to various types of inputs. This method of presentation helps show some of the critical, and often misleading, parameters of high-speed track-and-hold devices.

During the track mode, the unit operates as a high-speed buffer amplifier, with the output following input changes as they occur. In this mode, the response of the HTS-0010 is limited primarily by the slew rate characteristics of the device. As a result, the analog output is a faithful reproduction of the input as long as the highest frequency component of the input signal does not exceed the bandwidth of the unit.

The analog output shown on the bottom of Figure 2 tracks the input until a HOLD COMMAND is applied to Pin 5. When this pulse arrives, the sample bridge of the HTS-0010 disconnects the hold capacitor from the input. The short, but finite, interval required for this action is called aperture time.

Two other delay intervals combine with aperture time. One is delay in the hold command caused by propagation delay in the bridge driver; for purposes of discussion, this is a digital delay (t_d) because it is the time required for logic switching to occur. The other is propagation delay through the input buffer amplifier, which is an analog delay (t_a) because it affects the analog input signal being applied to the hold capacitor (see HTS-0010 Block Diagram).

Each of these three components is critical in the design of track-and-hold circuits, but the user needs to be concerned only with their combined overall effect. The combination is specified here as Effective Aperture Delay Time and is defined as the interval between the leading edge of the hold command and that instant when the input signal is equal to the held value.

Basically, effective aperture delay time is a measure of the difference between the analog and digital delay (t_d–t_a) and can assume a zero, positive, or negative value depending upon the comparative lengths of the two delays. In the HTS-0010, the analog delay (t_a) is greater than the switching delay (t_d), and causes the unit to hold an input voltage which occurred before the hold command because the hold capacitor sees a delayed version of the input signal.

The specification for Effective Aperture Delay Time is a more useful measurement for assessing T/H performance than is the measurement of only aperture time because it includes all three

of the components which have an effect on how quickly the device can make the change from the track mode to the hold mode.

The time intervals discussed above help explain what happens when the HTS-0010 makes the change from the track mode to the hold mode. In normal operation, however, they become academic discussions since most users of the T/H are more interested in when the held value has reached its steady state.

Aperture uncertainty or "jitter," is the result of noise signals of various kinds which modulate the phase of the hold command. This jitter shows up as a sample-to-sample variation in the value of the analog signal which is being "frozen."

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 2. The amplitude of the error is related to the dV/dt of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dV/dt increases.

The design characteristics of the HTS-0010 insure that effective aperture delay time is within its specification from unit to unit; and is also repeatable from one "hold" command to the next within any unit. Therefore, it should not be regarded as an error source the way aperture uncertainty is. Effective aperture delay time can be compensated with system timing which correctly establishes the beginning of the hold period.

Referring again to Figure 2, a switching transient appears in the analog output as a result of this transition from "track" to "hold." The Specifications table includes the maximum amplitude and duration of this transient; and also includes information on the switch delay time which precedes it. The held output is settled to within 1mV 6-15ns after the leading edge of the hold signal.

Feedthrough rejection is a measure of the amount of leakage from input to output during the hold interval after the HTS-0010 has settled to its specified accuracy. High feedthrough rejection is important because it assures no errors will be introduced during the conversion interval of the converter used at the output of the T/H.

In the illustration, V_{FT} is the small amount of "ripple" voltage on the held value of analog output. The ratio of output feedthrough to input signal is measured in dB and is equal to:

$$20 \log \left[\frac{V_{FT\ p\text{-}p}}{V_{IN\ p\text{-}p}} \right]$$

As shown, droop is that amount of change in the analog output which occurs during the hold interval. Improving (lessening) the droop rate can be accomplished by adding capacitance in parallel with the internal hold capacitor, but at the expense of slowing down the T/H and its ability to handle high-speed signals.

Applications which require longer hold times than the standard HTS-0010 provides may require external capacitance in parallel with the internal hold capacitor. For these, the user can parallel extra capacitance by connecting it between pin 20 and ground. The droop rate will be improved, but the overall speed and bandwidth of the T/H will be reduced. This extra connection should be made close to the hybrid case or it may introduce small amounts of electrical noise.

Switch delay time shown in Figure 2 is the interval between the end of the hold command and the start of movement in the analog output as it begins to retrack the analog input. This delay occurs at both the beginning and the end of the hold interval and is primarily the result of propagation delay through the output buffer amplifier.

Acquisition time is the time required for the output of the T/H to reacquire and begin tracking accurately the analog input after the T/H has returned to the "track" mode. The acquisition time "clock" starts when the output begins moving and stops when the output has settled to its specified accuracy. As might be expected, longer acquisition times are required for larger signals and/or greater accuracy.

High slew rates are also important during acquisition time, but the desire for speed must be tempered with practical considerations. If the design of the unit achieves only speed without regard for overshoot, the acquisition time will be lengthened. Excessive "ringing" around the signal being acquired precludes applying successive hold commands at MHz update rates.

SAMPLE-AND-HOLD (S/H) MODE

Although generally used in the track-and-hold mode, the HTS-0010 can also be used as a sample-and-hold device for applications where this capability is needed.

The operation of the unit is essentially a "mirror" of the T/H operation, in that the output is usually in the "hold" mode but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse which is used will be based on factors which are different for each application. Basically, the user establishes the width of this pulse by taking into account:

1. The acquisition time of the HTS-0010.
2. The desired accuracy of the sampled output.
3. The maximum amount of change which has occurred since the preceding sample.

This latter phenomenon is illustrated in Figure 3 Sample/Hold Operation.

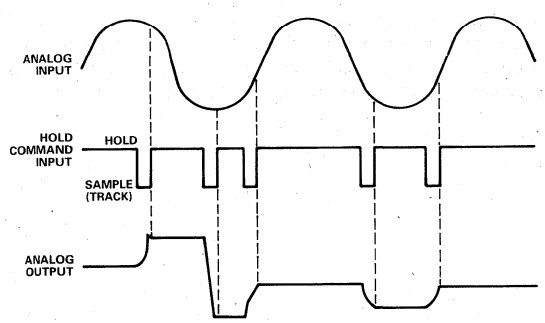


Figure 3. Sample/Hold Operation

When operating as a S/H, the signal applied to the HOLD COMMAND input (Pin 5) is usually a digital logic "1" which holds the HTS-0010 output at the input value present at the time of the sample/hold pulse.

Figure 3 shows asynchronous pulses applied to cause the output to reslew to new values. The trailing edge establishes the sample (track) mode; the leading edge returns the output to "hold".

In Figure 3, the analog input applied to the unit has changed drastically between the first and second sample (track) pulses. Smaller differences in the input values are present at the times of the second and third pulses. These differences in input show

up as differences in the amount of movement of the analog output.

The exceptional acquisition time of the HTS-0010 makes it extremely attractive for sample-hold applications because of its ability to acquire new output values quickly. This characteristic of the device allows the use of a narrow sample pulse and an inherently faster sample rate, limited only by the factors enumerated earlier.

Refer to Figure 4 Settling Accuracy vs. Acquisition Time.

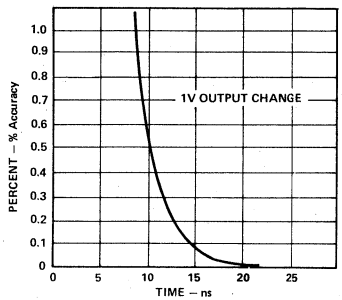


Figure 4. Settling Accuracy vs. Acquisition Time

This graph illustrates that closer accuracies require correspondingly longer amounts of time to acquire the signal. As shown, the accuracy/time relationship approaches an asymptotic curve, as opposed to being a linear function.

Another point to consider in Figure 4 is the output change which is illustrated is for a 1V change. If the output is required to change less than one volt (as it is between the second and third pulses in Figure 3, for example), the amount of time required to acquire the new value will be less than that which is shown.

When using the HTS-0010 or any other high-speed track-and-hold in the real world of data acquisition for fast-changing signals, the line between the device operating as a T/H or a S/H tends to "blur."

The designer using it as a T/H ahead of an A/D converter will generally vary the amount of "hold" time to obtain optimum operation for his particular application. When that performance is achieved, the HTS-0010 may, in the strictest sense of the word, be operating as a sample-and-hold. But it is useful to regard the two modes of operation separately when discussing the theory of operation of the unit.

DIFFERENCES: HTS-0010 VS. HTS-0025

As noted earlier, pin designations for the HTS-0010 T/H are similar to the predecessor HTS-0025 T/H. Two pins not used on the HTS-0025 are used for HTS-0010 functions, and attempts to use it as a "drop-in" replacement for the HTS-0025 need to take this into account.

Pins 20 and 21 on the HTS-0010 are used for auxiliary hold and power ground, respectively. These pins are not used on the HTS-0025 because that unit does not have a capability for accepting external capacitance in parallel with the hold capacitor; nor does it have as many ground connections. If circuits using the HTS-0025 are using those pin locations as tie points, it may preclude the possibility of substituting a model HTS-0010 unit in the circuit.

Current drive on the HTS-0010 is slightly less than it is on the HTS-0025 ($\pm$40mA vs. $\pm$50mA) but 3dB bandwidth is higher (60MHz vs. 30MHz).

The user of the HTS-0010 can reasonably expect higher speeds because of improvements in aperture uncertainty (5ps rms vs. 20ps rms); switching transient amplitude (15mV vs. 30mV); and acquisition time (10ns vs. 20ns for 1% settling). Noise levels in the track mode are also improved (40μV vs. 0.1mV maximum).

Voltage supplies for the internal amplifiers ($V_{CC}+$ and $V_{CC}-$) have a wider range on the HTS-0025 than they do on the HTS-0010 but $V_{CC}-$ can be connected to V_{EE} if desired, as explained elsewhere in the data sheet.

ORDERING INFORMATION

All versions of the HTS-0010 track/hold are housed in 24-pin metal dual in-line hybrid packages. For commercial applications operating over a temperature range of 0 to +70°C, specify model HTS-0010KD. For a temperature range of −55°C to +100°C, specify model HTS-0010SD.

Mating individual pin sockets are available from AMP. Knockout end type are part number 6-330808-0; open end type are 6-330808-3.

ANALOG DEVICES

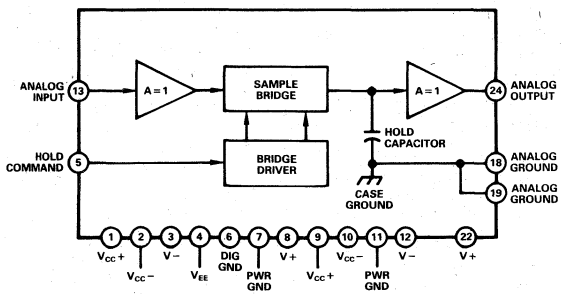
Ultra High Speed Hybrid Track-and-Hold Amplifiers

HTS-0025

FEATURES
Aperture Jitter of 20ps
Acquisition Time 25ns
Output Current ±50mA
Slew Rate 250V/μs

APPLICATIONS
Data Acquisition Systems
Radar Systems
Instrumentation Systems
Medical Electronics
High Resolution Displays

HTS-0025 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The Analog Devices HTS-0025 Track-and-Hold is another in Analog's range of track-and-hold (T/H) amplifiers useable in a variety of high-speed circuits. The HTS-0025 is part of a line of devices which offers designers the industry's widest range of track-and-hold and sample-and-hold units.

The design concepts used in the HTS-0025 T/H have made it the standard of comparison for high-speed circuits of this type. A dc-coupled Schottky diode bridge is driven by a high-impedance buffer amplifier and followed by a low impedance output amplifier. This achieves the best possible combination of speed and drive capabilities.

The pinouts of the HTS-0025 are similar to the HTS-0010 Track-and-Hold, so designers can select either the HTS-0025 or HTS-0010 for their particular applications. This kind of flexibility makes it possible to choose those parameters which are optimum for each application.

All models of the HTS-0025 are housed in a standard 24-pin metal DIP. The unit operating over a temperature range of 0 to +70°C is HTS-0025; the unit for a range of −55°C to +100°C is HTS-0025M.

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SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

	Units	HTS-0025	HTS-0025M
ANALOG INPUT			
Voltage Range			
For Rated Performance	V p-p	2	*
Maximum Without Damage	V	±4	*
Impedance	Ω	10^{10}	*
Capacitance	pF max	7	*
Bias Current	nA max	15	*
DIGITAL INPUT (ECL Compatible)			
Mode Control			
Hold Command Input			
"0" = Track	V	−1.5 to −1.8	*
"1" = Hold[1]	V	−0.8 to −1.1	*
ANALOG OUTPUT			
Current (Not Short Circuit Protected)	mA max	±50	*
Impedance	Ω(max)	3 (10)	*
Noise in Track Mode			
@ 5.0MHz Bandwidth	mV rms max	0.1	*
DC ACCURACY/STABILITY (FS = Full Scale)			
Gain (No Load)	V/V (min)	0.95 (0.92)	*
Gain Nonlinearity; 2V FS Input	% max	0.1	*
Gain Nonlinearity; 1V FS Input	% max	0.01	*
Gain Temperature Coefficient	ppm/°C (max)	30 (40)	*
Output Offset Voltage	mV (max)	±5 (±20)	*
(Track Mode)			
vs. Temperature	µV/°C (max)	100 (150)	200 (300)
TRACK (SAMPLE) MODE DYNAMICS			
Frequency Response			
Full Power Bandwidth	MHz min	20	15
Small Signal (−3dB) Bandwidth	MHz min	30	20
Slew Rate	V/µs (min)	250 (140)	250 (120)
Harmonic Distortion (Track Mode;			
4MHz, 2V p-p Input)			
R_L = 1kΩ	dB max	−68	*
R_L = 500Ω	dB max	−65	*
R_L = 200Ω	dB max	−64	*
R_L = 75Ω	dB max	−50	*
TRACK (SAMPLE)-TO-HOLD SWITCHING			
Effective Aperture Delay Time[2]	ns	5	*
Aperture Uncertainty (Jitter)	ps (rms) max	20	*
Offset Step (Pedestal)	mV (max)	±5 (±20)	*
Sensitivity to Temperature	µV/°C max	100	150[3]
Sensitivity to −5.2V	mV/V max	10	*
Switch Delay Time	ns	5	*
Switching Transient			
Amplitude	mV (max)	20 (25)	*
Settling to 5mV	ns (max)	20 (30)	*
HOLD MODE DYNAMICS			
Droop Rate	mV/µs (max)	0.2 (0.8)	*
Variation with Temperature		Doubles/10°C Change	
Feedthrough Rejection			
(2V p-p Input)			
@ 1MHz	dB min	70	*
@ 10MHz	dB min	65	*
HOLD-TO-TRACK (SAMPLE) DYNAMICS[4]			
Acquisition Time (1V Step)			
to ±1%	ns (max)	20 (30)	20 (40)
to ±0.1%	ns (max)	25 (35)	25 (40)
Acquisition Time (2V Step)			
to ±1%	ns (max)	25 (35)	25 (40)
to ±0.1%	ns (max)	30 (40)	30 (45)
Switch Delay Time	ns	1.5	*
POWER REQUIREMENTS			
V+ (+15V ±0.5V)	mA max	55	54
V− (−15V ±0.5V)	mA max	55	54
V_{CC}+ (+5.0V to +15.5V)[5]	mA max	15	*
V_{CC}− (−5.0V to −15.5V)[5]	mA max	15	*
V_{EE} (−5.2V ±0.25)[5]	mA max	40	34
Power Dissipation[6]	W max	2.3	2.4
Power Supply Rejection Ratio[7]	mV/V max	18	*
(dc to 10kHz)			
TEMPERATURE RANGE			
Operating (Case)	°C	0 to +70	−55 to +100
Storage	°C	−55 to +125	*
THERMAL RESISTANCE[8]			
Junction to Air, θja (Free Air)	°C/W	42	*
Junction to Case, θjc	°C/W	12	*
MTBF[9]			
Mean Time Between Failures	Hours		3.45×10^5
PACKAGE OPTION[10]		HY24G	*

NOTES

[1] One ECL 10k Gate, no resistor; requires 1kΩ to −5.2V
[2] Effective Aperture Delay Time is delay between Hold strobe and held value of analog output, referenced to analog input (see text).
[3] Pedestal temperature variation on HTS-0025M is same as HTS-0025 below +70°C, but increases between +70°C and +100°C.
[4] For acquisition time measurements, R_L = 200Ω; C_L = 13pF.
[5] V_{CC}+ may be tied to V+; V_{CC}− may be tied to V− or V_{EE} with adequate bypass capacitors (see text).
[6] Maximum power shown based on V_{CC}+ = V+; V_{CC}− = V−. Power is reduced to 2.0W maximum with V_{CC}+ = +5V and V_{CC}− = −5V.
[7] Variations in V− (−15V) have greater effect on unit performance than variations in other supplies; PSRR shown is for V−.
[8] Maximum junction temperature is +150°C.
[9] Calculated using MIL-HNBK 217.
[10] See Section 19 for package outline information.

*Specifications same as HTS-0025.

Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION
1	$V_{CC}+$ (+5V TO +15.5V)
2	$V_{CC}-$ (−5V TO −15.5V)
3	V− (−15V)
4	V_{EE} (−5.2V)
5	HOLD COMMAND
6	DIGITAL GROUND
7	POWER GROUND
8	V+ (+15V)
9	$V_{CC}+$ (+5V TO +15.5V)
10	$V_{CC}-$ (−5V TO −15.5V)
11	POWER GROUND
12	V− (−15V)
13	ANALOG INPUT
14	N/A
15	N/A
16	N/A
17	N/A
18	ANALOG GROUND
19	ANALOG GROUND
20	N/A
21	N/A
22	V+ (+15V)
23	N/A
24	ANALOG OUTPUT

POWER GROUND (PINS 7 AND 11), ANALOG GROUND (PINS 18 AND 19), AND DIGITAL GROUND (PIN 6) MUST BE CONNECTED TOGETHER AND TO A LOW-IMPEDANCE GROUND FOR PROPER OPERATION. MAKE CONNECTIONS AS CLOSE TO DEVICE AS POSSIBLE. HYBRID CASE IS CONNECTED TO ANALOG GROUND INTERNALLY.

Applications

One of the main uses for Track-and-Hold (T/H) units is ahead of analog-to-digital (A/D) converters to allow digitizing signals with bandwidths higher than the A/D can handle by itself. The use of an appropriate T/H allows the converter to become a true "Nyquist converter", i.e., capable of digitizing analog signals whose maximum bandwidth is one-half the encoding rate.

The characteristics of the HTS-0025 T/H make it useful in multiple other applications besides this "standard" use of devices of this kind. It can be used in sample and hold circuits, peak holding applications, simultaneous sampling A/Ds (with appropriate analog multiplexing), and for many other data processing needs.

Refer to Figure 1, HTS-0025 Interconnection Diagram.

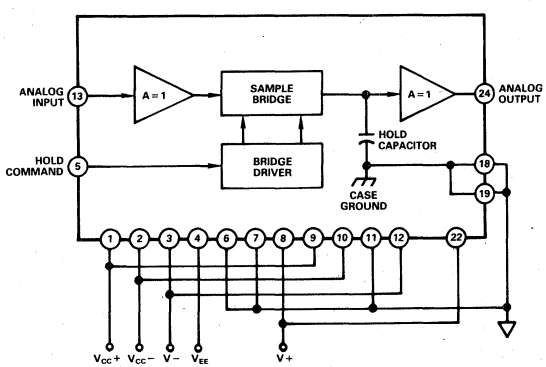


Figure 1. HTS-0025 Interconnection Diagram

Bypass capacitors are used internally on all power supply leads on the HTS-0025 Track-and-Hold. External bypassing of all power supplies with 0.01μF–0.1μF ceramics will help performance. In addition, electrolytic capacitors of 10-22 microfarads on each supply will also enhance the HTS-0025's operation.

A massive ground plane, careful component layout, and physically separating analog and digital signals are among the other considerations which can have major effects in improving the high-speed characteristics of the HTS-0025 Track-and-Hold.

As shown, supply voltages must be applied to all pins for which they are designated; it is extremely important to connect all grounds together, and to a solid, low-impedance ground plane as close to the hybrid as physically possible.

The five different voltages shown are the voltages used in final test and calibration, and are the recommended voltages for best performance; minor variations are possible.

For best performance, amplifier supplies, $V_{CC}-$ and $V_{CC}+$ should be equal and opposite. The ECL logic supply (V_{EE} = −5.2V) can be used also for $V_{CC}-$; if it is, bypass capacitors should be used at each supply pin to decrease the possibility of logic switching noise introducing extraneous signals.

TRACK-AND-HOLD MODE

When operated in the "track" mode, the HTS-0025 T/H functions as a buffer amplifier, following all changes in analog input as they occur. The user selects the point at which digitizing is to be done by applying an external ECL-compatible HOLD COMMAND to Pin 5.

Refer to Figure 2, Track/Hold Waveforms.

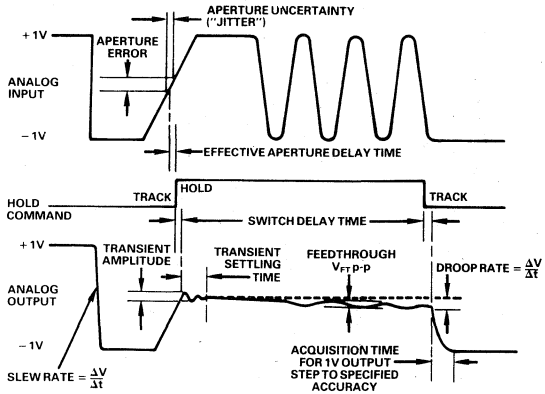


Figure 2. Track/Hold Waveforms

A varying, ideal analog input is shown at the top of Figure 2 for purposes of illustrating the response of the HTS-0025 to various types of inputs. This method of presentation shows many of the critical, and sometimes confusing, parameters of high-speed track-and-hold devices.

In the track mode, the response of the HTS-0025 is limited primarily by the slew rate characteristics of the device. As a result, the analog output is a faithful reproduction of the input as long as the highest frequency component of the input signal does not exceed the bandwidth of the unit.

The analog output shown on the bottom of Figure 2 tracks the input until a HOLD COMMAND is applied to Pin 5. When this pulse arrives, the sample bridge of the HTS-0025 disconnects the hold capacitor from the input. The short, but finite, interval required for this action is called aperture time (t_{sa}).

Other delay intervals combine with aperture time. One is delay in the hold command caused by propagation delay in the bridge driver; for purposes of discussion, this is a digital delay because it is the time required for logic switching to occur. Another is propagation delay through the input buffer amplifier, which is an analog delay because it affects the analog input signal being applied to the hold capacitor (see HTS-0025 Block Diagram).

Each of these three components is critical in the design of track-and-hold circuits, but user concern is limited only to their combined effect. The combination is specified here as Effective Aperture Delay Time and is defined as the interval between the leading edge of the hold command and that instant when the input signal is equal to the held value.

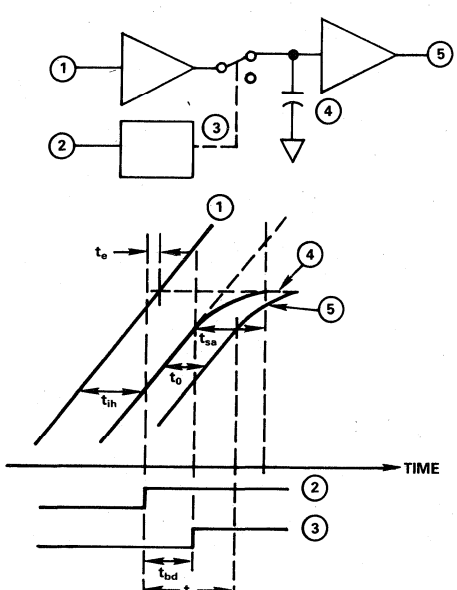
Additional details on the timing intervals in T/H circuits are shown in Figure 3.

The model T/H shown at the top of Figure 3 contains the basic elements of the HTS-0025, shown in their simplest form. The lower portion of the figure calls out multiple intervals of incremental time involved in switching from "track" to "hold" but no attempt is made to assign numerical values to them. Their definitions are intended solely to help understand the theory of T/H operation.

Effective aperture delay time (t_e) is digital delay plus averaging of the switch delay, minus analog delay. Depending on the comparative lengths of these combined delays, the value of t_e can be zero, positive, or negative.

The specification for Effective Aperture Delay Time is a more useful measurement for assessing T/H performance than aperture time because it includes all three of the components which have an effect on how quickly the device can make the change from the track mode to the hold mode.

In normal operation, these time intervals become academic discussions since users of the T/H are more interested in when the held value has reached its steady state.



(1) ANALOG INPUT
(2) ENCODE COMMAND INPUT
(3) SWITCH CONTROL
(4) HOLD CAPACITOR
(5) ANALOG OUTPUT

t_{ih} = ANALOG DELAY INPUT TO HOLD CAPACITOR = (DELAY FROM (1) TO (4))

t_{bd} = DIGITAL DELAY THROUGH BRIDGE DRIVER (DELAY (2) TO (3)).

t_{sa} = APERTURE TIME OF SWITCH

t_e = EFFECTIVE APERTURE DELAY TIME = $t_{bd} + \frac{t_{sa}}{2} - t_{ih}$ (DELAY (2) TO (1)).

t_s = SWITCH DELAY TIME = $t_{bd} + t_o$ (DELAY (2) TO (5)).

t_o = OUTPUT BUFFER DELAY (DELAY (4) TO (5))

Figure 3. T/H Timing Intervals

The waveforms in Figure 3 are idealized and based on an analog input which has a constant dV/dt. Other phenomena which are involved, such as transients, "jitter," etc. are illustrated in Figure 2.

Aperture uncertainty, or "jitter," is the result of noise signals of various kinds which modulate the phase of the hold command. This jitter shows up as a sample-to-sample variation in the value of the analog signal which is being "frozen".

Aperture uncertainty manifests itself as an aperture error, as shown in Figure 2. The amplitude of the error is related to the dV/dt of the analog input. For any given value of aperture uncertainty, aperture error will increase as the input dV/dt increases.

The design of the HTS-0025 insures that effective aperture delay time is within its specification from unit to unit; and is also repeatable from one "hold" command to the next within any unit. Therefore, it should not be regarded as an error source the way aperture uncertainty is. Effective aperture delay time can be compensated with system timing which correctly establishes the beginning of the hold period.

A switching transient appears in the analog output as a result of the transition from "track" to "hold." The Specifications table includes the maximum amplitude and duration of this transient; and also includes information on the switch delay time which precedes it. The held output is settled to within 5mV 20-25ns after the leading edge of the hold signal.

Feedthrough rejection is a measure of the amount of leakage from input to output during the hold interval after the HTS-0025 has settled to its specified accuracy. High feedthrough rejection is important because it assures no errors will be introduced during the conversion interval of the converter used at the output of the T/H.

In the illustration, V_{FT} is the small amount of "ripple" voltage on the held value of analog output. The ratio of output feedthrough to input signal is measured in dB and is equal to:

$$20 \log \left[\frac{V_{FT\ p\text{-}p}}{V_{IN\ p\text{-}p}} \right]$$

As shown, droop is that amount of change in the analog output which occurs during the hold interval.

Switch delay time shown in Figure 2 is the interval between the edges of the hold command and the start of movements in the analog output. This delay occurs at both the beginning and the end of the hold interval and is primarily the result of propagation delay through the output buffer amplifier.

Acquisition time is the time required for the output of the T/H to reacquire and begin accurate tracking of the analog input after the T/H has returned to the "track" mode. The acquisition time "clock" starts when the output begins moving and stops when the output has settled to its specified accuracy. As might be expected, longer acquisition times are required for larger signals and/or greater accuracy.

High slew rates are also important during acquisition time, but the desire for speed must be tempered with practical considerations. If the design of the unit achieves only speed without regard for overshoot, the acquisition time will be lengthened. Excessive "ringing" around the signal being acquired precludes applying successive hold commands at MHz update rates.

SAMPLE-AND-HOLD (S/H) MODE

Although generally used in the track-and-hold mode, the HTS-0025 can also be used as a sample-and-hold device for applications where this capability is needed.

The operation of the unit is essentially a "mirror" of the T/H operation, in that the output is usually in the "hold" mode but is switched to the "sample" (track) mode for brief intervals.

The width of the sample pulse which is used will be based on factors which are different for each application. Basically, the user establishes the width of this pulse by taking into account:

1. The acquisition time of the HTS-0025.
2. The desired accuracy of the sampled output.
3. The maximum amount of change which has occurred since the preceding sample.

This latter phenomenon is illustrated in Figure 4 Sample/Hold Operation.

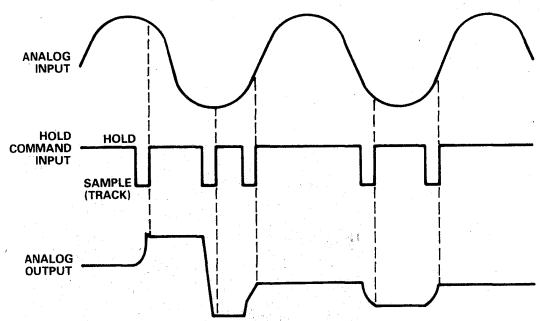


Figure 4. Sample/Hold Operation

When operating as a S/H, the signal applied to the HOLD COMMAND input (Pin 5) is usually a digital logic "1" which holds the HTS-0025 output at the input value present at the time of the sample/hold pulse.

Figure 4 shows asynchronous pulses applied to cause the output to reslew to new values. The trailing edge establishes the sample (track) mode; the leading edge returns the output to "hold".

In Figure 4, the analog input applied to the unit has changed drastically between the first and second sample (track) pulses. Smaller differences in the input values are present at the times of the second and third pulses. These differences in input show up as differences in the amount of movement of the analog output.

The acquisition time of the HTS-0025 makes it extremely attractive for sample-hold applications because of its ability to acquire new output values quickly. This characteristic of the device allows the use of a narrow sample pulse and an inherently faster sample rate, limited only by the factors enumerated earlier.

Refer to Figure 5 Settling Accuracy vs. Acquisition Time.

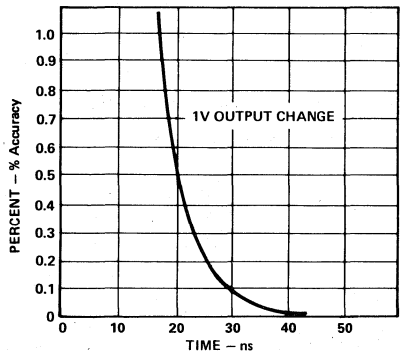


Figure 5. Settling Accuracy vs. Acquisition Time

This graph illustrates that closer accuracies require correspondingly longer amounts of time to acquire the signal. As shown, the accuracy/time relationship approaches an asymptotic curve, rather than being a linear function.

Another point to consider in Figure 5 is the illustrated output change is for a 1V change. If the output is required to change less than one volt (as it is between the second and third pulses in Figure 4, for example), the amount of time required to acquire the new value will be less than that shown.

When using the HTS-0025 or any other high-speed track-and-hold in the real world of data acquisition for fast-changing signals, the line between the device operating as a T/H or a S/H tends to "blur."

The designer using it as a T/H ahead of an A/D converter will generally vary the amount of "hold" time to obtain optimum operation for his particular application. When that performance is achieved, the HTS-0025 may, in the strictest sense of the word, be operating as a sample-and-hold. But it is useful to regard the two modes of operation separately when discussing the theory of operation of the unit.

ORDERING INFORMATION

All versions of the HTS-0025 track/hold are housed in 24-pin metal dual in-line hybrid packages. For commercial applications operating over a temperature range of 0 to +70°C, specify model HTS-0025. For a temperature range of −55°C to +100°C, specify model HTS-0025M.

Mating individual pin sockets are available from AMP. Knockout end type are part number 6-330808-0; open end type are 6-330808-3.

Typical HTS-0025 Operation

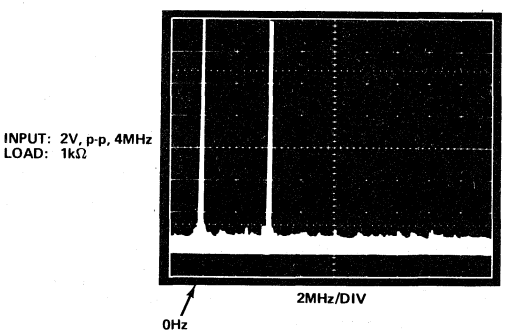


Figure 6a. Harmonic Distortion – Track Mode

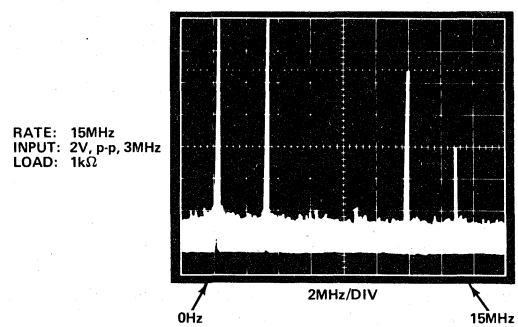


Figure 6b. Frequency Domain Outputs

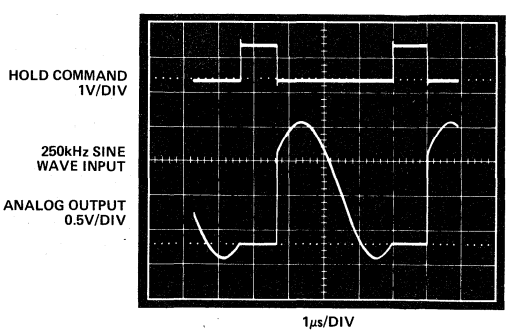


Figure 6c. Track/Hold Operation

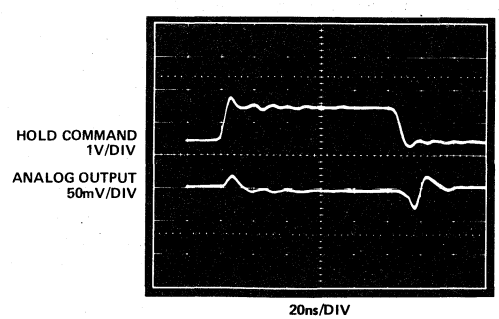


Figure 6d. Expanded View of Output Signal Showing Switching Transients and Pedestal with dc Input

Data Acquisition Subsystems

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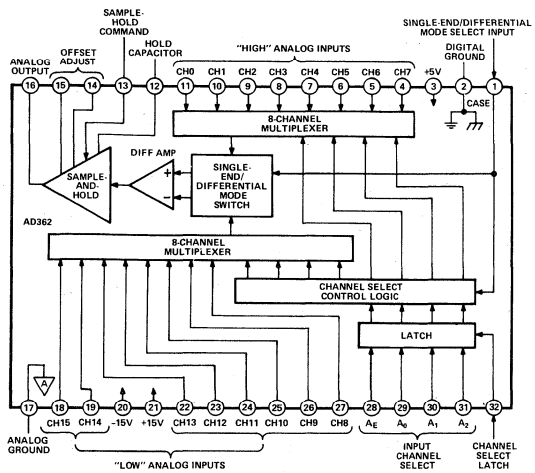
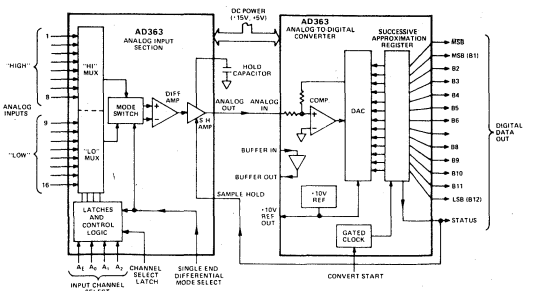
Selection Guide
Data Acquisition Subsystems



AD362

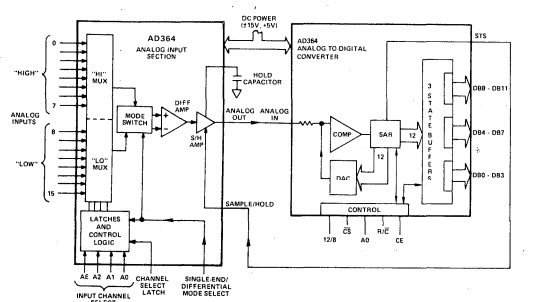
Page

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control — Vol. I 15-5
- True 12-Bit Precision: Nonlinearity ≤ ±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32-Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog-to-Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common-Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs



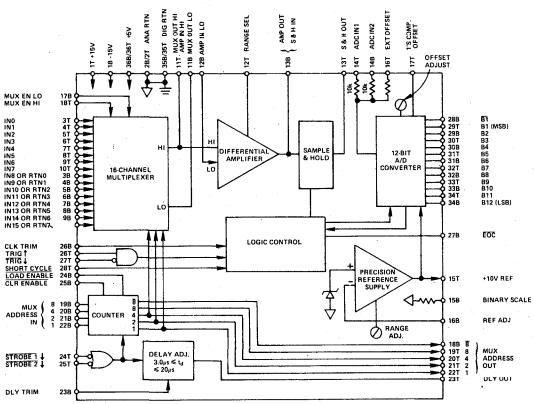
AD363

- Complete System in Reliable IC Form — Vol. I 15-13
- Small Size
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- Versatile Input/Output/Control Format
- Short-Cycle Capability
- True 12-Bit Operation: Nonlinearity ≤ ±0.012%
- Guaranteed No Missing Codes Over Temperature Range
- High Throughput Rate: 30kHz
- Low Power: 1.7W



AD364

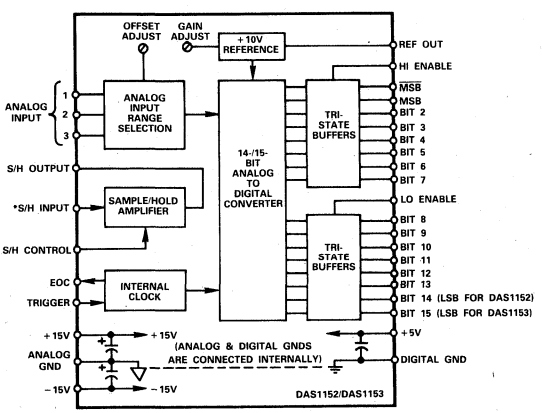
- Complete Data Acquisition System in 2-Package IC Form — Vol. I 15-17
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ≤ ±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25μs
- Buried Zener Reference for Long-Term Stablility and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short Cycle Capability
- Low Power: 1.4W



DAS1128

Page
Vol. II
15-5

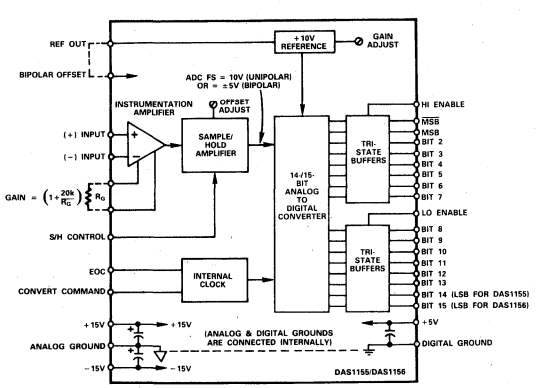
- Complete Data Acquisition System
- 12-Bit Digital Output
- 16 Single or 8 Differential Analog Inputs
- High Throughput Rate
- Selectable Analog Input Ranges
- Versatile Input/Output/Control Format
- Low 3 Watt Power Dissipation
- Small 3″ × 4.6″ × 0.375″ Module



DAS1152/DAS1153

Vol. II
15-13

- 14-Bit & 15-Bit Sampling A/D Converter
- Complete with High Accuracy Sample/Hold and A/D Converter
- Differential Nonlinearity: ±0.002% FSR max (DAS1153)
- Nonlinearity: DAS1152: ±0.005% FSR max
  DAS1153: ±0.003% FSR max
- Low Differential Nonlinearity T.C.: ±2ppm/°C max
- High Throughput Rate: 25kHz min (DAS1152)
- High Feedthrough Rejection: −96dB
- Byte-Selectable Tri-State Buffered Outputs
- Internal Gain & Offset Potentiometers
- Improved Second Source to A/D/A/M 824 and A/D/A/M 825 Modules



DAS1155/DAS1156

Vol. II
15-17

- 14-Bit & 15-Bit Low Level Data Acquisition System
- Functionally Complete:
  Includes Instrumentation Amplifier, Sample/Hold Amplifier, and Analog-to-Digital Converter
- Differential Nonlinearity: ±0.002% FSR max (DAS1156)
- Guaranteed Nonlinearity: ±0.005% FSR (DAS1155)
  ±0.003% FSR (DAS1156)
- High Common-Mode Rejection: −80dB (up to 500Hz)
- High Feedthrough Rejection: −96dB
- Resistor Programmable Gain: 1V/V to 1000V/V
- Byte Selectable Tri-State Buffer Outputs
- Internal Gain and Offset Potentiometers

ANALOG DEVICES

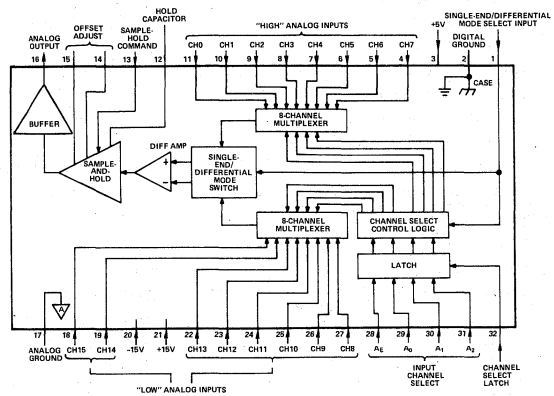
Precision Sample-and-Hold with 16-Channel Multiplexer

AD362

FEATURES

- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Precision: Nonlinearity ≤±0.005%
- High Speed: 10μs Acquisition Time to 0.01%
- Complete and Calibrated: No Additional Parts Required
- Small, Reliable: 32 Pin Hermetic Metal DIP
- Versatile: Simple Interface to Popular Analog to Digital Converters
- High Differential Input Impedance ($10^{10}\Omega$) and Common Mode Rejection (80dB)
- Fully Protected Multiplexer Inputs

AD362 FUNCTIONAL BLOCK DIAGRAM



32-PIN DIP

PRODUCT DESCRIPTION

The AD362 is a complete, precision 16-channel data acquisition system analog input section in hybrid integrated circuit form. Large-scale linear integrated circuitry, thick- and thin-film technology and active laser trimming gives the AD362 extensive applications versatility along with full 12-bit accuracy.

The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

The sample-and-hold mode control is designed to connect directly to the "Status" output of an analog to digital converter so that a convert command to the ADC will automatically put the sample-and-hold into the "Hold" mode. A precision hold capacitor is included with each AD362. The AD362 output amplifier is capable of driving the unbuffered analog input of most high-speed, 12-bit successive-approximation ADCs. Interface is thereby reduced to two simple connections with no additional components required.

When used with a 12-bit, 25-microsecond ADC such as the AD572, AD574 or AD ADC80, system throughput rate is as high as 30kHz at full rated accuracy. The AD362KD is specified for operation over a 0 to +70°C temperature range while the AD362SD operates to specification from −55°C to +125°C. Both grades are packaged in a hermetic, electrostatically shielded 32-pin metal dual-in-line package.

PRODUCT HIGHLIGHTS

1. The AD362, when used with a precision analog to digital converter, forms a complete, accurate, high-speed data acquisition system.
2. The 16-input channels may be configured in single-ended, differential or a mixture of both modes. Mode switching is provided by a user-controllable internal analog switch.
3. Multiplexers, differential amplifier, sample-and-hold and high-speed output buffer provide complete analog interfacing capabilities.
4. Internal channel address latches are provided to facilitate interfacing the AD362 to data, address or control buses.
5. All grades of the AD362 are hermetically sealed in rugged metal DIP packages.
6. A precision hold capacitor is provided with each AD362.
7. The AD362SD is specified over the entire extended temperature range, −55°C to +125°C.

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SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD362KD	AD362SD
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Range, Linear T_{min} to T_{max}	±10V min	*
Input (Bias) Current, Per Channel	±50nA	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel, Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
Offset, Channel to Channel	±2.5mV max	*
ACCURACY		
Gain Error, T_{min} to T_{max}	±0.02% FSR, max	*
Offset Error, T_{min} to T_{max}	±4mV	*
Linearity Error	±0.005% max	*
T_{min} to T_{max}	±0.01% max	*
Noise Error	1mV p-p, 0.1 to 1MHz, max	*
T_{min} to T_{max}	2mV p-p, 0.1 to 1MHz, max	*
TEMPERATURE COEFFICIENTS		
Gain, T_{min} to T_{max}	±4ppm/°C max	±2ppm/°C max
Offset, ±10V Range, T_{min} to T_{max}	±2ppm/°C max	±1.5ppm/°C max
SAMPLE AND HOLD DYNAMICS		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time, for 20V Step to ±0.01% of Final Value	18μs max (10μs typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[1]		
Input Channel Select (Pins 28-31)	4-Bit Binary, Channel Address	*
	1LS TTL Load	*
Channel Select Latch (Pin 32)	"1": Latch Transparent	*
	"0": Latched	*
	8LS TTL Loads	*
Single Ended/Differential Mode Select (Pin 1)	"0": Single-Ended Mode	*
	"1": Differential Mode (@ +4.0V min)	*
	3TTL Loads	*
Sample and Hold Command (Pin 13)	"0": Sample Mode	*
	"1": Hold Mode	*
	1TTL Load	*
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ 30mA max	*
	-15V, ±5% @ 30mA max	*
	+5V, ±5% @ 40mA max	*
Total Power Dissipation	1.1 Watts max	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[2]	-55°C to +150°C

NOTES

[1] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V. One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.

[2] AD362KD External Hold Capacitor is limited to +85°C; AD362 device itself may be stored at up to +150°C.

*Specifications same as AD362KD.

Specifications subject to change without notice.

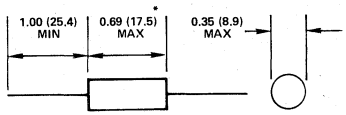
ABSOLUTE MAXIMUM RATINGS (ALL MODELS)	
+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

AD362 ORDERING GUIDE

Model	Specification Temp Range	Max Gain TC	Package Option[1]
AD362KD	0 to +70°C	±4ppm/°C	HY32D
AD362SD	-55°C to +125°C	±2ppm/°C	HY32D

NOTE
[1] See Section 19 for package outline information.

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH AD362KD

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH AD362SD IS 1.00".

AD362 PIN FUNCTION DESCRIPTION

Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Status
14	Offset Adjust (See Figure 5)
15	Offset Adjust (See Figure 5)
16	Analog Output Normally Connected to ADC "Analog In"
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch Transparent

AD362 DESIGN

The AD362 consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output buffer, channel address latches and control logic as shown in Figure 1. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single AD362 to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD362 by dynamically switching the input mode control.

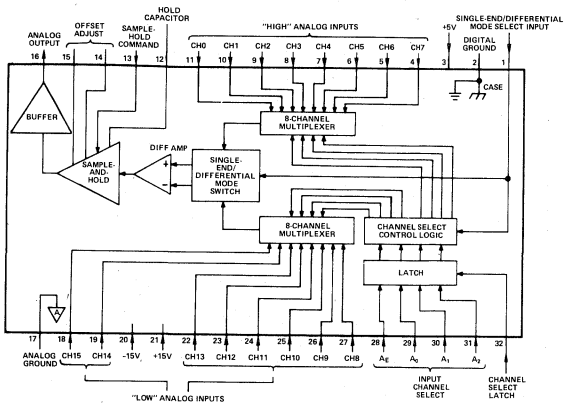


Figure 1. AD362 Analog Input Section Functional Block Diagram and Pinout

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range device (AD362KD) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD362SD). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The output buffer is a high speed amplifier whose output impedance remains low and constant at high frequencies. Therefore, the AD362 may drive a fast, unbuffered, precision ADC without loss of accuracy.

The AD362 is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

THEORY OF OPERATION

Concept

The AD362 is intended to be used in conjunction with a high-speed precision analog-to-digital converter to form a complete data acquisition system (DAS) in microcircuit form. Figure 2 shows a general AD362-with-ADC DAS application.

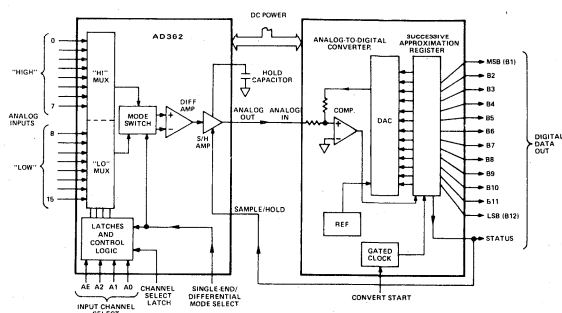


Figure 2. AD362 with ADC as a Complete Data Acquisition System

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

System Timing

Figure 3 is a timing diagram for the AD362 connected as shown in Figure 2 and operating at maximum conversion rate. The ADC is assumed to be a conventional 12 bit type such as the AD572 or AD ADC80.

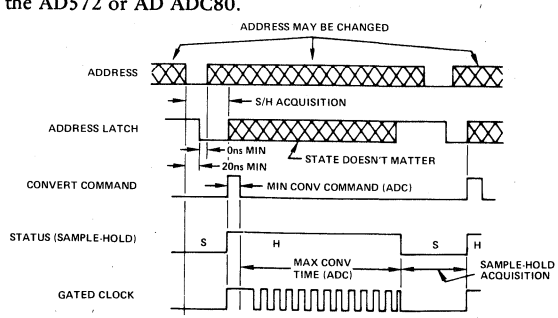


Figure 3. DAS Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start command is issued to the ADC which, in response, indicates that it is "busy" by placing a Logic "1" on its Status line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy", the sample-and-hold is in the Hold mode.
4. The ADC goes into its conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not affect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the Sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start command may be issued to the ADC.

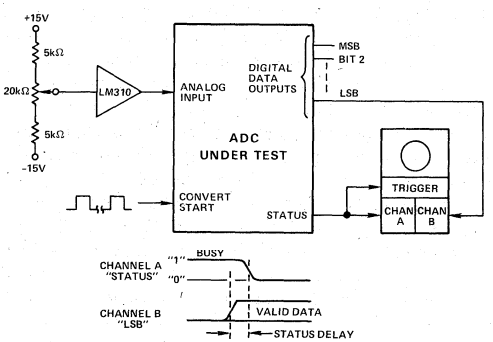


Figure 4. ADC Status Valid Test

NOTE:

Valid Output Data

Not all ADCs have all data bits available when Status indicates that the conversion is complete. Successive approximation ADCs based on the 2502/3/4 type of register must have a Status delay built in or the final data bit will lag Status by approximately 50ns. This will result in two problems:

1. The sample-and-hold will return to Sample, disturbing the analog input to the ADC as it is attempting to convert the least significant bit. This may result in an error.
2. If the falling edge of Status is being used to load the data into a register, the least significant bit will not be valid when loaded.

An external 100ns delay or use of an ADC with a valid Status output is necessary to prevent this problem. The applications shown in this data sheet ensure that all data bits will be valid.

The following test may be made to determine if the ADC Status timing is correct:

1. Connect the ADC under test as shown in Figure 4.
2. Trigger the oscilloscope on Status. Delay the display such that Status is mid-screen.
3. Observe the LSB data output of the ADC.
4. Vary the analog input control to confirm that the LSB transition precedes the Status transition.

Single-Ended/Differential Mode Control

The AD362 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels) (+4.0V min)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "Hold" mode). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexers singularly or in pairs as required.

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

15

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "Hold" mode).

Input Channel Address Latch

The AD362 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the "1"-to-"0" transition (level-triggered).

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (pin 13) is normally connected to the Status output (pin 20) from an analog to digital converter. When a conversion is initiated by applying a Convert Start command to the ADC, Status goes to Logic "1", putting the sample-and-hold into the "Hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the "Sample" mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous Sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD362. One side of this capacitor is wired to pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD362KD is Polystyrene while the wider operating temperature range of the AD362SD requires a Teflon capacitor (supplied).

Smaller capacitors will allow slightly faster operation, but only with increased noise and decreased precision. 1000pF will typically allow acquisition to 0.1% in four microseconds.

Larger capacitors may be substituted to reduce noise, and sample-to-hold offset, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD326KD only) or Teflon (AD362KD or SD). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Section Offset Adjust Circuit

Although the offset voltage of the AD362 may be adjusted, that adjustment is normally performed at the ADC. In some special applications, however, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to the AD362 voltage offset and if a gain stage was to be inserted between the AD362 and the ADC. To adjust the offset of the AD362, the circuit shown in Figure 5 is recommended.

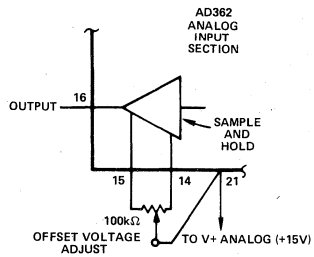


Figure 5. AD362 Offset Voltage Adjustment

Under normal conditions, all calibration is performed at the ADC Section.

Other Considerations

Grounding: Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground (pin 17) and Digital Ground (pin 2) are not connected internally; these pins must be connected externally for the system to operate properly. Preferably, this connection is made at only one point, as close to the AD362 as possible. The case is connected internally to Digital Ground to provide good electrostatic shielding. If the grounds are not tied common on the same card with the AD362, the digital and analog grounds should be connected locally with back-to-back general-purpose diodes as shown in Figure 6. This will protect the AD362 from possible damage caused by voltages in excess of ±1 volt between the ground systems which could occur if the key grounding card should be removed from the overall system. The device will operate properly with as much as ±200mV between grounds, however this difference will be reflected directly as an input offset voltage.

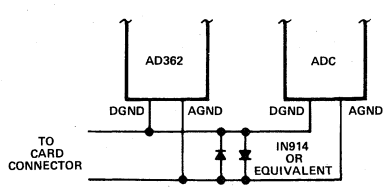


Figure 6. Ground-Fault Protection Diodes

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling since each power lead is bypassed internally with a 0.039μF ceramic capacitor.

Interfacing to Popular Analog to Digital Converters

The AD362 has been designed to interface directly to most analog to digital converters; often no additional components are required and only two interconnections must be made. The direct interface requirements for the ADC are as follows:

1. The ADC Status output must be positive-true Logic ("1" during conversion).
2. Transition from "0" to "1" must occur at least 200ns before the most significant bit decision is made (successive approximation ADC) or before input integration starts (integrating type ADC).
3. Status must not return to "0" before the LSB decision is made.
4. If Status is being used to latch output data, it must not return to Logic "0" until all output data bits are valid and available.

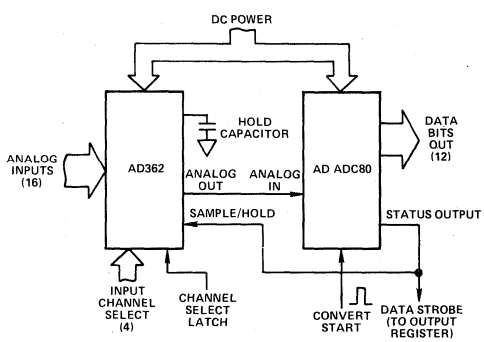
Complete system throughput performance is determined by combining the worst-case specifications of the AD362 and the ADC. If guaranteed system performance is required, the AD363 and AD364 are recommended. The AD363 includes an AD362 and an AD572 12-bit, 25-microsecond precision ADC. The AD364 consists of an AD362 and an AD574 12-bit, microprocessor-compatible, low cost ADC. Each is specified as a complete, two-package system; data sheets are available upon request.

Figure 7a shows the AD362 driving an AD ADC80. The AD ADC80 is a 12-bit, 25-microsecond, low-cost ADC that meets all of the requirements listed above. Throughput rate is typically 30kHz with no missing codes over the operating temperature range.

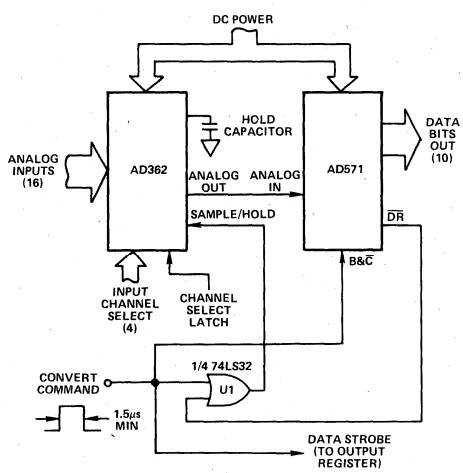
Figure 7b shows a 10-bit application based on the AD362 and the AD571, a complete low cost 10-bit, 25-microsecond ADC. In this case, two of the above requirements are not met:

1. $\overline{DR}$ ($\overline{DATA\ READY}$), as Status, is positive-true but. . .
2. $\overline{DR}$ does not indicate that a conversion is in progress until 1.5μs after conversion starts.
3. $\overline{DR}$ does indicate conversion complete after the LSB decision is made, but. . .
4. $\overline{DR}$ precedes the enabling of the AD571 output 3-state gates by 500ns.

The gating provided by U1 allows the applied convert command (CC) to initiate input hold at the AD362. CC must last for more than 1.5μs so that $\overline{DR}$ may then assume control of Hold. If conversion is continuous (consistent with multi-channel operation), the next convert command can be used to load the previously-converted data into an output register. For single conversion operation, a 1μs delay of the falling edge of $\overline{DR}$ may be used to signify valid data.



a. 12-Bit DAS Using AD362 and AD ADC80



b. 10-Bit DAS Using AD362 and AD571

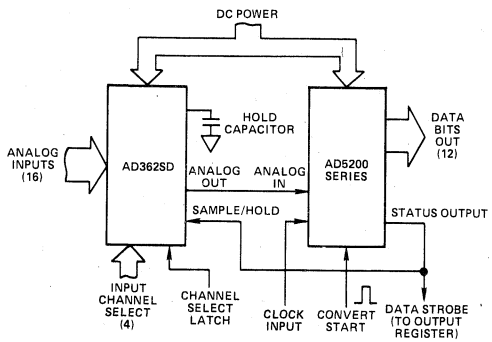
Figure 7. Data Acquisition Systems Based on the AD362 and Popular ADC's

Interfacing to Special Purpose ADCs

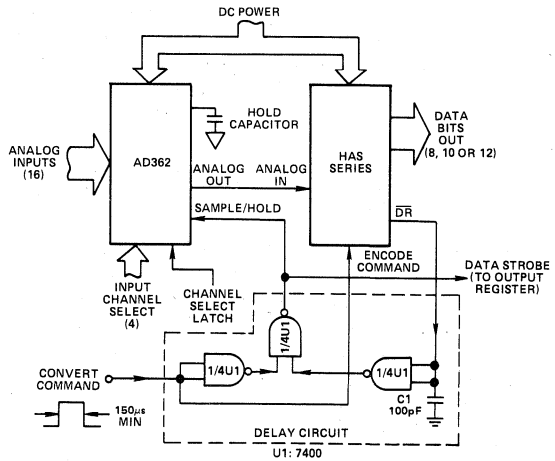
The AD5200 series of ADCs perform a 12-bit conversion in 50 microseconds and feature totally adjustment-free operation, high accuracy, and a small hermetically-sealed 24-pin package.

These ADCs are often used in high-reliability applications and, like the AD362SD, operate over the -55°C to +125°C temperature range. The AD5200 series meets all of the interfacing requirements for direct connection to the AD362 as shown in Figure 8a. System throughput rate is typically 16kHz.

The HAS series of ultra-fast ADCs are 8-bit (HAS0801), 10-bit (HAS1001) and 12-bit (HAS1202) devices that convert in 1.5, 1.7, and 2.8 microseconds (maximum) respectively. These devices are hybrid IC's, packaged in 32-pin DIPs. Since the Data Ready signal from the HAS precedes the LSB decision, $\overline{DR}$ must be delayed. Figure 8b shows the appropriate circuitry to provide that delay. Throughput rate for the 12-bit system is typically 80kHz.



a. 12-Bit High Accuracy and Reliability DAS Using AD362 and AD5200



b. High-Speed DAS Using AD362 and HAS

Figure 8. Data Acquisition Systems Based on the AD362 and Purpose ADCs

Complete 16-Channel 12-Bit Data Acquisition System

AD363

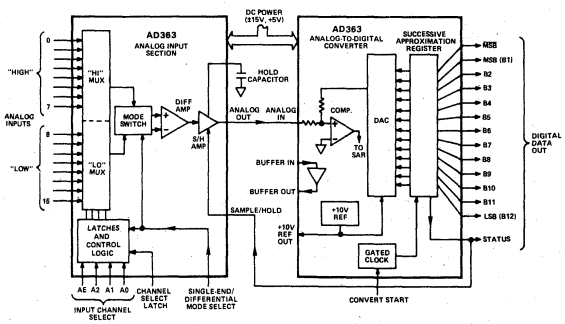
FEATURES

Versatility
- Complete DAS in Reliable IC Form
- Small Size: Two 32-Pin DIPs
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- Extended Aerospace Temperature Range: -55°C to +125°C (AD363S)
- Versatile Input/Output/Control Format
- Short-Cycle Capability

Performance
- True 12-Bit Operation: Nonlinearity ≤±0.012%
- Guaranteed No Missing Codes Over Temperature Range
- High Throughput Rate: 30kHz
- Low Power: 1.7W in Two Packages

Value
- Complete: No Additional Parts Required
- Reliable: Hybrid IC Construction. All Inputs Fully Protected.
- Precision +10.0 Volt Reference for External Application
- Fast Precision Buffer Amplifier for External Application
- Low Cost

AD363 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD363 is a complete 16 channel, 12-bit data acquisition system in integrated circuit form. It is an AD362 analog input section and an AD572 analog-to-digital converter specified as a pair. This high reliability hybrid set is available in two temperature grades for industrial and extended temperature range applications. The AD362 analog input section is in a 32-pin metal package which provides electrostatic shielding for analog input signals. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD363 by dynamically switching the input mode control.

The analog-to-digital converter section contains a complete 12-bit successive approximation analog-to-digital converter, including internal clock, precision 10 volt reference, comparator, buffer amplifier and a proprietary-design 12-bit D/A converter. Active laser trimming of the reference and D/A converter results in maximum linearity errors of ±0.012% while performing a 12-bit conversion in 25 microseconds.

Analog input voltage ranges of ±2.5, ±5.0, ±10, 0 to +5 and 0 to +10 volts are user-selectable. Adding flexibility and value are the precision 10 volt reference and the internal buffer amplifier, both of which may be used for external applications. All butone digital signals are TTL/DTL compatible and output data is positive-true in parallel and serial form.

System throughput rate is as high as 30kHz at full rated accuracy. The AD363K is specified for operation over a 0 to +70°C temperature range while the AD363S operates to specification from -55°C to +125°C. Both device grades are guaranteed to have no missing codes over their specified temperature ranges.

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AD363 ORDERING GUIDE

Model	Specification Temp Range	Max Gain T.C.	Max Reference T.C.	Guaranteed Temp Range No Missing Codes	Package Styles[1] Analog Input Section	ADC Section
AD363KD	0 to +70°C	±30ppm/°C	±20ppm/°C	0 to +70°C	HY32D	HY32G
AD363SD	-55°C to +125°C	±25ppm/°C	±20ppm/°C	-55°C to +125°C	HY32D	HY32G

NOTE
[1] See Section 19 for package outline information.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

MODEL	AD363K	AD363S
ANALOG INPUTS		
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)	*
Input Voltage Ranges		
Bipolar	±2.5V, ±5.0V, ±10.0V	*
Unipolar	0 to +5V, 0 to +10V	*
Input (Bias) Current, Per Channel	±50nA	*
Input Impedance		
On Channel	$10^{10}\Omega$, 100pF	*
Off Channel	$10^{10}\Omega$, 10pF	*
Input Fault Current (Power Off or On)	20mA, max, Internally Limited	*
Common Mode Rejection		
Differential Mode	70dB min (80dB typ) @ 1kHz, 20V p-p	*
Mux Crosstalk (Interchannel,		
Any Off Channel to Any On Channel)	-80dB max (-90dB typ) @ 1kHz, 20V p-p	*
RESOLUTION	12 BITS	*
ACCURACY		
Gain Error[1]	±0.05% FSR (Adj. to Zero)	*
Unipolar Offset Error	±10mV (Adj to Zero)	*
Bipolar Offset Error	±20mV (Adj to Zero)	*
Linearity Error	±½LSB max	*
Differential Linearity Error	±1LSB max (±½LSB typ)	*
Relative Accuracy	±0.025% FSR	*
Noise Error	1mV p-p, 0 to 1MHz	*
TEMPERATURE COEFFICIENTS		
Gain	±30ppm/°C max (±10ppm/°C typ)	±25ppm/°C max (±15ppm/°C typ)
Offset, ±10V Range	±10ppm/°C max (±5ppm/°C typ)	±8ppm/°C max (±5ppm/°C typ)
Differential Linearity	No Missing Codes Over Temperature Range	*
SIGNAL DYNAMICS		
Conversion Time[2]	25μs max (22μs typ)	*
Throughput Rate, Full Rated Accuracy	25kHz min (30kHz typ)	*
Sample and Hold		
Aperture Delay	100ns max (50ns typ)	*
Aperture Uncertainty	500ps max (100ps typ)	*
Acquisition Time		
To ±0.01% of Final Value for Full Scale Step	18μs max (10μs, typ)	*
Feedthrough	-70dB max (-80dB typ) @ 1kHz	*
Droop Rate	2mV/ms max (1mV/ms typ)	*
DIGITAL INPUT SIGNALS[4]		
Convert Command (to ADC Section, Pin 21)	Positive Pulse, 200ns min Width. Leading Edge ("0" to "1") Resets Register, Trailing Edge ("1" to "0") Starts Conversion.	*
	1TTL Load	*
Input Channel Select (To Analog Input Section, Pins 28-31)	4 Bit Binary, Channel Address.	*
	1LS TTL Load	*
Channel Select Latch (To Analog Input Section, Pin 32)	"1" Latch Transparent	*
	"0" Latched	*
	4LS TTL Loads	*

MODEL	AD363K	AD363S
DIGITAL INPUT SIGNALS, cont.		
Sample-Hold Command (To Analog Input Section Pin 13 Normally Connected To ADC "Status", Pin 20)	"0" Sample Mode "1" Hold Mode 2LS TTL Loads	* * *
Short Cycle (To ADC Section Pin 14)	Connect to +5V for 12 Bits Resolution. Connect to Output Bit n + 1 For n Bits Resolution. 1TTL Load	* * * *
Single Ended/Differential Mode Select (To Analog Input Section, Pin 1)	"0": Single-Ended Mode "1": Differential Mode (+4.0V min) 3TTL Loads	* * *
DIGITAL OUTPUT SIGNALS[4] (All Codes Positive True)		
Parallel Data		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary/Two's Complement	*
Output Drive	2TTL Loads	*
Serial Data (NRZ Format)		
Unipolar Code	Binary	*
Bipolar Code	Offset Binary	*
Output Drive	2TTL Loads	*
Status ($\overline{\text{Status}}$)	Logic "1" ("0") During Conversion	*
Output Drive	2TTL Loads	*
Internal Clock		
Output Drive	2TTL Loads	*
Frequency	500kHz	*
INTERNAL REFERENCE VOLTAGE	+10.00V, ±10mV	*
Max External Current	±1mA	*
Voltage Temp. Coefficient	±20ppm/°C, max	±20ppm/°C, max
POWER REQUIREMENTS		
Supply Voltages/Currents	+15V, ±5% @ +45mA max (+38mA typ) -15V, ±5% @ -45mA max (-38mA typ) +5V, ±5% @ +136mA max (+113mA typ)	* * *
Total Power Dissipation	2 watts max (1.7 watts typ)	*
TEMPERATURE RANGE		
Specification	0 to +70°C	-55°C to +125°C
Storage	-55°C to +85°C[3]	-55°C to +150°C

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NOTES

[1] **With 50Ω, 1% fixed resistor in place of Gain Adjust pot.**

[2] Conversion time of ADC Section.

[3] AD363K External Hold Capacitor is limited to +85°C; Analog Input Section and ADC Section may be stored at up to +150°C.

[4] One TTL Load is defined as I_{IL} = -1.6mA max @ V_{IL} = 0.4V, I_{IH} = 40μA max @ V_{IH} = 2.4V.
One LS TTL Load is defined as I_{IL} = -0.36mA max @ V_{IL} = 0.4V, I_{IH} = 20μA max @ V_{IH} = 2.7V.

***Specifications same as AD363K.**
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)	
+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

PIN FUNCTION DESCRIPTION

ANALOG INPUT SECTION	
Pin Number	Function
1	Single-End/Differential Mode Select "0": Single-Ended Mode "1": Differential Mode (+4.0V min)
2	Digital Ground
3	Positive Digital Power Supply, +5V
4	"High" Analog Input, Channel 7
5	"High" Analog Input, Channel 6
6	"High" Analog Input, Channel 5
7	"High" Analog Input, Channel 4
8	"High" Analog Input, Channel 3
9	"High" Analog Input, Channel 2
10	"High" Analog Input, Channel 1
11	"High" Analog Input, Channel 0
12	Hold Capacitor (Provided, See Figure 1)
13	Sample-Hold Command "0": Sample Mode "1": Hold Mode Normally Connected to ADC Pin 20
14	Offset Adjust (See Figure 6)
15	Offset Adjust (See Figure 6)
16	Analog Output Normally Connected to ADC "Analog In" (See Figure 1)
17	Analog Ground
18	"High" ("Low") Analog Input, Channel 15 (7)
19	"High" ("Low") Analog Input, Channel 14 (6)
20	Negative Analog Power Supply, -15V
21	Positive Analog Power Supply, +15V
22	"High" ("Low") Analog Input, Channel 13 (5)
23	"High" ("Low") Analog Input, Channel 12 (4)
24	"High" ("Low") Analog Input, Channel 11 (3)
25	"High" ("Low") Analog Input, Channel 10 (2)
26	"High" ("Low") Analog Input, Channel 9 (1)
27	"High" ("Low") Analog Input, Channel 8 (0)
28	Input Channel Select, Address Bit AE
29	Input Channel Select, Address Bit A0
30	Input Channel Select, Address Bit A1
31	Input Channel Select, Address Bit A2
32	Input Channel Select Latch "0": Latched "1": Latch "Transparent"

ANALOG TO DIGITAL CONVERTER SECTION	
Pin Number	Function
1	Data Bit 12 (Least Significant Bit) Out
2	Data Bit 11 Out
3	Data Bit 10 Out
4	Data Bit 9 Out
5	Data Bit 8 Out
6	Data Bit 7 Out
7	Data Bit 6 Out
8	Data Bit 5 Out
9	Data Bit 4 Out
10	Data Bit 3 Out
11	Data Bit 2 Out
12	Data Bit 1 (Most Significant Bit) Out
13	$\overline{\text{Data Bit 1 (MSB)}}$ Out
14	Short Cycle Control Connect to +5V for 12 Bits Connect to Bit (n+1) Out for n Bits
15	Digital Ground
16	Positive Digital Power Supply, +5V
17	$\overline{\text{Status}}$ Out "0": Conversion in Progress (Parallel Data Not Valid) "1": Conversion Complete (Parallel Data Valid)
18	+10Volt Reference Out (See Figures 3, 7, 8, 11)
19	Clock Out (Runs During Conversion)
20	Status Out "0": Conversion Complete (Parallel Data Valid) "1": Conversion in Progress (Parallel Data Not Valid)
21	Convert Start In Reset Logic : ↑ Start Convert : ↓
22	Comparator In (See Figures 3, 7, 8)
23	Bipolar Offset Open for Unipolar Inputs Connect to ADC Pin 22 for Bipolar Inputs (See Figure 8)
24	10V Span R In (See Figure 7)
25	20V Span R In (See Figure 8)
26	Analog Ground
27	Gain Adjust (See Figures 7 and 8)
28	Positive Analog Power Supply, +15V
29	Buffer Out (For External Use)
30	Buffer In (For External Use)
31	Negative Analog Power Supply, -15V
32	Serial Data Out Each Bit Valid On Trailing (↓) Edge Clock Out, ADC Pin 19

Detailed timing, connection and application information can be found in the AD572 and AD362 sections located elsewhere in this catalog.

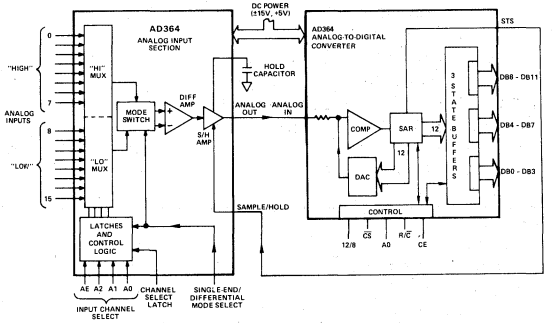
16-Channel µP Compatible 12-Bit Data Acquisition System

AD364

FEATURES

- Complete Data Acquisition System in 2-Package IC Form
- Full 8- or 16-Bit Microprocessor Bus Interface
- 16 Single-Ended or 8 Differential Channels with Switchable Mode Control
- True 12-Bit Operation: Nonlinearity ≤±0.012%
- Guaranteed No Missing Codes Over Specified Temperature Range
- High Throughput Rate: 20kHz
- Fast Successive Approximation Conversion: 25µs
- Buried Zener Reference for Long-Term Stability and Low Gain TC
- Small Size: Requires Only 2.8 Square Inches
- Short-Cycle Capability
- Low Power: 1.4 Watts
- Extended Aerospace Temperature Range: -55°C to +125°C

AD364 FUNCTIONAL BLOCK DIAGRAM



TWO DUAL IN-LINE PACKAGES

PRODUCT DESCRIPTION

The AD364 is a complete 16 channel, microprocessor compatible, 12-bit data acquisition system in integrated circuit form. The AD364 design is implemented with linear compatible LSI chips, active laser trimming and hybrid technology resulting in maximum performance and flexibility.

The AD364 consists of two separate functional blocks, each in a hermetically sealed dual-in-line package. The analog input section contains two eight-channel multiplexers, a differential amplifier, a sample-and-hold, a channel address register and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hard-wire programming and permits a mixture of single-ended and differential sources to be interfaced to an AD364 by dynamically switching the input mode control.

The ADC section contains a complete 12-bit successive approximation ADC, including internal clock, precision 10 volt reference, comparator and bus interface. The ADC uses the newly-developed LCI (Linear-Compatible Integrated Injection Logic) process to provide the low power logic necessary to make a high speed 12-bit ADC and 3-state output buffer circuitry for direct interface to an 8-, 12- or 16-bit microprocessor bus.

The AD364 is available in 4 different grades. The AD364J and K grades are specified for operation over the 0 to +70°C temperature range. The AD364S, T are specified for the -55°C to +125°C range.

PRODUCT HIGHLIGHTS

1. The precision laser-trimmed scaling and bipolar offset resistors provide three calibrated ranges; 0 to +10 volts unipolar, or -5 to +5 and -10 to +10 volts bipolar. Typical bipolar offset and full scale calibration errors of ±0.05% can be trimmed to zero each with one external component.
2. The internal buried zener reference is trimmed to 10.00 volts with a ±1% maximum error and 15ppm/°C typical TC. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.
3. The AD364 interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12 bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).

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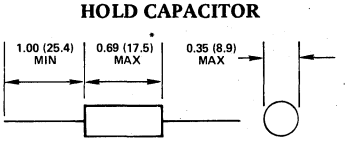
AD364 ORDERING GUIDE

Model	Linearity	Temp. Range	Analog Input Section	Package Style[1] Analog to Digital Converter
AD364JD	±0.024%	0 to +70°C	HY32D	D28A
AD364KD	±0.012%	0 to +70°C	HY32D	D28A
AD364SD	±0.024%	-55°C to +125°C	HY32D	D28A
AD364TD	±0.012%	-55°C to +125°C	HY32D	D28A

NOTE

[1] See Section 19 for package outline information.

HOLD CAPACITOR



*THIS DIMENSION IS FOR POLYSTYRENE CAPACITOR SUPPLIED WITH J AND K GRADES.

MAX BODY LENGTH OF TEFLON CAPACITOR SUPPLIED WITH S AND T GRADES IS 1.00".

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V with 2000pF hold capacitor as provided unless otherwise noted)

PARAMETER	AD364JD	AD364KD	AD364SD	AD364TD	UNITS
ANALOG INPUTS					
Number of Inputs	16 Single-Ended or 8 Differential (Electronically Selectable)				
Input Voltage Range					
T_{min} to T_{max}	±10	*	*	*	V
Input (Bias) Current per Channel	±50	*	*	*	nA
Input Impedance ON Channel	10^{10}/100	*	*	*	Ω/pF
OFF Channel	10^{10}/10	*	*	*	Ω/pF
Input Fault Current (Power ON or OFF)	20	*	*	*	mA max (Internally Limited)
Common Mode Rejection					
Differential Mode 1kHz 20Vp-p	70 min (80 typ)	*	*	*	dB
Mux Cross Talk (Any OFF Channel to Any ON Channel) 1kHz					
20V p-p	-80 max (-90 typ)	*	*	*	dB
Offset, Channel to Channel	±5	*	*	*	mV max
ACCURACY					
Gain Error[1]	0.3	*	*	*	% of FSR
Unipolar Offset Error[2]	±10	±8	*	**	mV
Bipolar Offset Error[2]	±50	±20	*	**	mV
Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Differential Linearity Error	0.024	0.012	*	**	% of FSR max
T_{min} to T_{max}	0.024	0.012	*	*	% of FSR max
Noise Error	1mV p-p 0.1Hz to 1MHz	*	*	*	
TEMPERATURE COEFFICIENTS					
Gain	54	31	*	**	ppm/°C
Offset (±10V Range)	12	7	*	**	ppm/°C
Operating Temperature Range	0 to +70°C	*	-55°C to +125°C	***	ppm/°C
SIGNAL DYNAMICS					
Conversion Time	32 max (25 typ)	*	*	*	µs
Throughput Rate, Full Accuracy	20 min (25 typ)	*	*	*	kHz
Sample Hold					
Aperture Delay	100 max (50 typ)	*	*	*	ns
Aperture Uncertainty	500 max (100 typ)	*	*	*	ps
Acquisition Time					
To 0.01% of Final Value					
For Full Scale Step	18 max (10 typ)	*	*	*	µs
Feedthrough at 1kHz	-70 max (-80 typ)	*	*	*	dB
Droop Rate	2 max (1 typ)	*	*	*	mV/ms
DIGITAL INPUT SIGNALS					
Analog Input Section					
Input Channel Select	4 Bit Binary Address	*	*	*	
	1 LS TTL Load	*	*	*	
Channel Select Latch	"1" Latch Transparent	*	*	*	
	"0" Latched	*	*	*	
	4 LS TTL Loads	*	*	*	
Single Ended/Differential	"0" Single Ended	*	*	*	
Mode Select	"1" Differential (+4V min)	*	*	*	
	3TTL Loads	*	*	*	
Sample and Hold Command	"0" Sample Mode	*	*	*	
	"1" Hold Mode	*	*	*	
	1TTL Load	*	*	*	
ADC Section[3] $4.5 \leqslant V_L \leqslant 5.5$					
Logic Input Threshold					
T_{min} to T_{max}					
Logic "1"	2.0	*	*	*	V min
Logic "0"	0.8	*	*	*	V max
Logic Input Current					
T_{min} to T_{max}					
Logic "1"	10	*	*	*	µA max
Logic "0"	10	*	*	*	µA max

PARAMETER	AD364JD	AD364KD	AD364SD	AD364TD	UNITS
DIGITAL OUTPUT SIGNALS					
Logic Outputs T_{min} to T_{max}					
Sink Current V_{OUT} = 0.4V	1.6	*	*	*	mA min
Source Current V_{OUT} = 2.4V	0.5	*	*	*	mA min
Output Leakage When In Three State	±40	*	*	*	μA max
Output Coding					
Unipolar	Positive True Binary	*	*	*	
Bipolar	Positive True Offset Binary	*	*	*	
POWER REQUIREMENTS					
Supply Voltages/Currents	+15V, ±5% @ 36mA max	*	*	*	
	-15V, ±5% @ 65mA max	*	*	*	
	+5V, ±5% @ 75mA max	*	*	*	

NOTES
[1] With 50Ω resistor from REF IN to REF OUT. Adjustable to zero.
[2] Adjustable to zero.
[3] 12/$\overline{8}$ line must be hard wired to V_{LOGIC} or digital common.
*Specifications same as AD364J.
**Specifications same as AD364K.
***Specifications same as AD364S.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (ALL MODELS)

+V, Digital Supply	+5.5V
+V, Analog Supply	+16V
-V, Analog Supply	-16V
V_{IN}, Signal	±V, Analog Supply
V_{IN}, Digital	0 to +V, Digital Supply
A_{GND} to D_{GND}	±1V

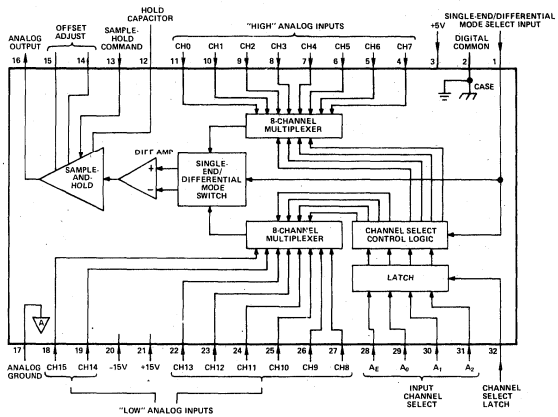


Figure 1. AD364 Analog Input Section Functional Block Diagram and Pinout

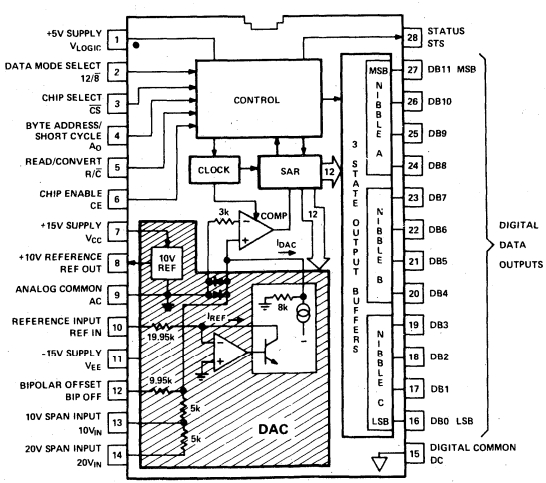


Figure 2. ADC Section Functional Block Diagram and Pinout

AD364 DESIGN

Concept

The AD364 consists of two separate functional blocks as shown in Figure 3; each is packaged in a hermetically-sealed DIP.

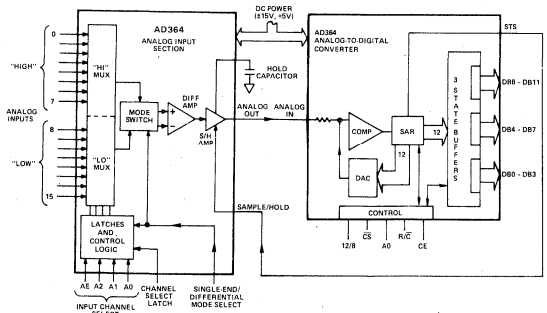


Figure 3. AD364 Functional Block Diagram

The Analog Input Section contains multiplexers, a differential amplifier, a sample-and-hold, a channel address latch and control logic. Analog-to-digital conversion is provided by a 12 bit, 35 microsecond "ADC" which is also available separately as the AD574.

By dividing the data acquisition task into two sections, several important advantages are realized. Performance of each design is optimized for its specific function. Production yields are increased thus decreasing costs. Furthermore, the standard configuration 28 and 32 pin packages plug into standard sockets and are easier to handle than larger packages with higher pin counts.

Analog Input Section Design

The AIS consists of two 8-channel multiplexers, a differential amplifier, a sample-and-hold, channel address latches and control logic. The multiplexers can be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A unique feature of the AD364 is an internal analog switch controlled by a digital input that performs switching between single-ended and differential modes. This feature allows a single product to perform in either mode without external hard-wire interconnections. Of more significance is the ability to serve a mixture of both single-ended and differential sources with a single AD364 by dynamically switching the input mode control.

Multiplexer channel address inputs are interfaced through a level-triggered ("transparent") input register. With a Logic "1" at the Channel Select Latch input, the address signals feed through the register to directly select the appropriate input channel. This address information can be held in the register by placing a Logic "0" on the Channel Select Latch input. Internal logic monitors the status of the Single-Ended/Differential Mode input and addresses the multiplexers accordingly.

A differential amplifier buffers the multiplexer outputs while providing high input impedance in both differential and single-ended modes. Amplifier gain and common mode rejection are actively laser-trimmed.

The sample-and-hold is a high speed monolithic device that can also function as a gated operational amplifier. Its uncommitted differential inputs allow it to serve a second role as the output subtractor in the differential amplifier. This eliminates one amplifier and decreases drift, settling time and power consumption. A Logic "1" on the Sample-and-Hold Command input will cause the sample-and-hold to "freeze" the analog signal while the ADC performs the conversion. Normally the Sample-and-Hold Command is connected to the ADC Status output which is at Logic "1" during conversion and Logic "0" between conversions. For slowly-changing inputs, throughput speed may be increased by grounding the Sample-and-Hold Command input instead of connecting it to the ADC status.

A Polystyrene hold capacitor is provided with each commercial temperature range system (AD364J, K) while a Teflon capacitor is provided with units intended for operation at temperatures up to 125°C (AD364S, T). Use of an external capacitor allows the user to make his own speed/accuracy tradeoff; a smaller capacitor will allow faster sample-and-hold response but will decrease accuracy while a larger capacitor will increase accuracy at slower conversion rates.

The Analog Input Section is constructed on a substrate that includes thick-film resistors for non-critical applications such as input protection and biasing. A separately-mounted laser-trimmed thin-film resistor network is used to establish accurate gain and high common-mode rejection. The metal package affords electromagnetic and electrostatic shielding and is hermetically welded at low temperatures. Welding eliminates the possibility of contamination from solder particles or flux while low temperature sealing maintains the accuracy of the laser-trimmed thin-film resistors.

"ADC" Section

The ADC Section is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the ADC is shown in Figure 2. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. (Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers). The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guaran-

tees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ±1%; it is buffered and can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

THEORY OF OPERATION

System Timing

Figure 4 is a timing diagram for the AD364 connected as shown in Figure 3 and operating at maximum conversion rate.

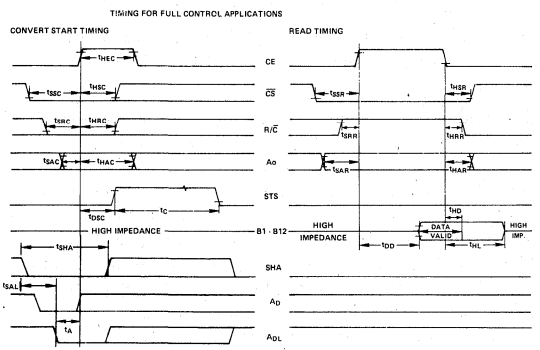


Figure 4. AD364 Timing Diagram

The normal sequence of events is as follows:

1. The appropriate Channel Select Address is latched into the address register. Time is allowed for the multiplexers to settle.
2. A Convert Start Control sequence is issued to the ADC which indicates that it is "busy" by placing a Logic "1" on its Status Line.
3. The ADC Status controls the sample-and-hold. When the ADC is "busy" the sample-and-hold is in the hold mode.
4. The ADC goes into its 35 microsecond conversion routine. Since the sample-and-hold is holding the proper analog value, the address may be updated during conversion. Thus multiplexer settling time can coincide with conversion and need not effect throughput rate.
5. The ADC indicates completion of its conversion by returning Status to Logic "0". The sample-and-hold returns to the sample mode.
6. If the input signal has changed full-scale (different channels may have widely-varying data) the sample-and-hold will typically require 10 microseconds to "acquire" the next input to sufficient accuracy for 12-bit conversion.

After allowing a suitable interval for the sample-and-hold to stabilize at its new value, another Convert Start control sequence may be issued to the ADC.

ADC Operation

There are two sets of control pins on the ADC: the general control inputs (CE, $\overline{CS}$, and R/$\overline{C}$), and the internal register control inputs (12/$\overline{8}$ and A_0). The general control pins function similarly to those on most A/D converters, performing device timing, addressing, cycle initiation and read enable functions. The internal register control inputs, which are not found on most A/D converters, select output data format and conversion cycle length.

The two major control functions, convert start and read enable, are controlled by CE, $\overline{CS}$, R/$\overline{C}$. Although all three inputs must be in the correct state to perform the function (for convert start, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 0; for read enable, CE = 1, $\overline{CS}$ = 0, R/$\overline{C}$ = 1), the sequence does not matter. For large systems, typically microprocessor controlled, standard operation for convert start would be to first set R/$\overline{C}$ = 0 (from R/$\overline{W}$ line); address the chip with $\overline{CS}$ = 0, then apply a positive start pulse to CE. A read would be done similarly but with R/$\overline{C}$ = 1.

The A_0 (byte select) and 12/$\overline{8}$ (data format) inputs work together to control the output data and conversion cycle. In almost all situations 12/$\overline{8}$ is hard-wired "high" (to V_{LOGIC}) or "low" (to Digital Common). If it is wired high, all 12 data lines will be enabled when the read function is called by the general control inputs. For an 8-bit bus interface, 12/$\overline{8}$ will be wired low. In this mode, only the 8 upper bits or the 4 lower bits can be enabled at once, as addressed by A_0. For these applications, the 4LSB's (pins 16–19) should be hard-wired to the 4MSB's (pins 24–27). Thus, during a read, when A_0 is low, the upper 8 bits are enabled and present data on pins 20 through 27. When A_0 goes high, the upper 8 data bits are disabled, the 4LSB's then present data to pins 24 to 27, and the 4 middle bits are overridden so that zeros are presented to pins 20 and 23.

The A_0 input performs an additional function of controlling conversion length. If A_0 is held low prior to cycle initiation, a full 12-bit, 25μs cycle will result; if A_0 is held high prior to cycle initiation a shortened 8-bit, 16μs cycle will result. The A_0 line must be set prior to cycle initiation and held in the desired position at least until STS goes high. Thus, for microprocessor interface applications, the A_0 line must be properly controlled during both the convert start and read functions.

STANDARD FULL CONTROL INTERFACE

The timing for the standard full control interface is shown in Figure 4. In this operating mode, $\overline{CS}$ is used as the address input which selects the particular device, R/$\overline{C}$ selects between the read data and start conversion functions, and CE is used to time the actual functions.

The left side of the figure shows the conversion start control. $\overline{CS}$ and R/$\overline{C}$ are brought low (their sequence does not matter), then the start pulse is applied to CE. The timing diagram shows a time delay for $\overline{CS}$ and R/$\overline{C}$ prior to the start pulse at CE. If less time than this is allowed, the conversion will still be started, but an appropriately longer pulse will be needed at CE. However, if the hold times for $\overline{CS}$ and R/$\overline{C}$ after the rising edge of the start pulse at CE are not followed, the conversion may not be initiated.

The A_0 line determines the conversion cycle length, and must be selected prior to conversion initiation. If A_0 is low, a 12-bit cycle results; if A_0 is high, an 8-bit short cycle results. Minimum set-up and hold times are shown. The status line goes high to indicate conversion in progress. The analog input signal is allowed to vary until the STS goes high. It must then be held

steady until STATUS again goes low at the end of conversion.

The data read function operates in a similar fashion except that R/$\overline{C}$ is now held high. The data is stored in the output register and can be recalled at will until a new conversion cycle is commanded. In addition, if the converter is arranged in the 8-bit data mode, the A_0 line now functions as the byte select address, with set-up and hold times as shown. With A_0 low, pins 20 to 27 (DB4–11) come out of three-state and present data. With A_0 high, pins 16–19 (DB0–3) come out of three-state with data and pins 20–23 present active trailing zeros. In the 8-bit mode pins 16–19 will be hard-wired directly to pins 24–27 for direct two-byte loading onto an 8-bit bus. There are two delay times for the data lines after CE is brought low: t_{HD} is the delay until data is no longer valid; t_{HL} is the delay until the outputs are fully into the high impedance state.

TIMING SPECIFICATIONS – FULL CONTROL MODE

t_{DSC}	300ns max	t_{DD}	400ns max
t_{HEC}	300ns min	t_{HD}	100ns min
t_{SSC}	300ns min	t_{SSR}	350ns min
t_{HSC}	200ns min	t_{SRR}	0 min
t_{SRC}	200ns min	t_{SAR}	200ns min
t_{HRC}	200ns min	t_{HSR}	100ns min
t_{SAC}	0 min	t_{HRR}	0 min
t_{HAC}	300ns min	t_{HAR}	100ns min
t_C	15-32μs (12 bit)	t_{HL}	600ns max
	10-20μs (8 bit)	t_{SAL}	20ns min
t_{SHA}	10-18μs	t_{SA}	0 min

STAND-ALONE OPERATION

For simpler control functions, the AD364 can be controlled with just R/$\overline{C}$. In this case, CE is wired high, $\overline{CS}$ low, 12/$\overline{8}$ high, and A_0 low. There are two ways of cycling the device with this simple hook-up. If a negative pulse is used to initiate conversion as in Figure 5, the converter will automatically bring the 12 data lines out of three-state at the end of conversion. The data will remain valid on the output lines until another pulse is applied.

If the conversion is initiated by a high pulse as shown in Figure 6, the data lines are held in three-state at the end of conversion until R/$\overline{C}$ is brought high. The next conversion cycle is initiated when R/$\overline{C}$ goes low, the data from the previous cycle will remain valid for the time t_{HDR}. An alternative to the above is to toggle R/$\overline{C}$ as needed to initiate a new cycle on read data. Data will appear when R/$\overline{C}$ is brought high, a new cycle is initiated when R/$\overline{C}$ goes low.

TIMING SPECIFICATIONS – STAND-ALONE MODE

t_{HRL}	400ns min	
t_{DS}	500ns max	
t_{HDR}	300ns max	
t_{HS}	-100ns min	+200ns max
t_{HRH}	150ns min	
t_{DDR}	350ns max	

t_C (12 bit convert) 15-35μs
t_C (8 bit convert) 10-20μs

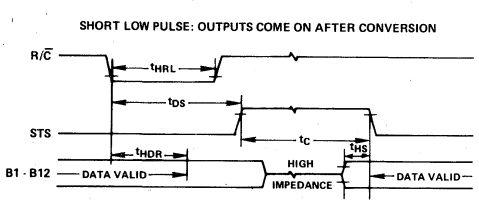


Figure 5.

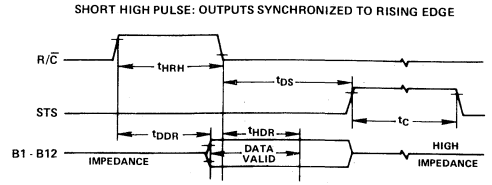


Figure 6.

AIS OPERATION

Single-Ended/Differential Mode Control

The AD364 features an internal analog switch that configures the Analog Input Section in either a 16-channel single-ended or 8-channel differential mode. This switch is controlled by a non-TTL logic input applied to pin 1 of the Analog Input Section:

"0": Single-Ended (16 channels)
"1": Differential (8 channels) (+4.0V minimum)

When in the differential mode, a differential source may be applied between corresponding "High" and "Low" analog input channels.

It is possible to mix SE and DIFF inputs by using the mode control to command the appropriate mode. Figure 10 illustrates an example of a "mixed" application. In this case, four microseconds must be allowed for the output of the Analog Input Section to settle to within ±0.01% of its final value, but if the mode is switched concurrent with changing the channel address, no significant additional delay is introduced. The effect of this delay may be eliminated by changing modes while a conversion is in progress (with the sample-and-hold in the "hold mode"). When SE and DIFF signals are being processed concurrently, the DIFF signals must be applied between corresponding "High" and "Low" analog input channels. Another application of this feature is the capability of measuring 16 sources individually and/or measuring differences between pairs of those sources.

Input Channel Addressing

Table I is the truth table for input channel addressing in both the single-ended and differential modes. The 16 single-ended channels may be addressed by applying the corresponding

ADDRESS				ON CHANNEL (Pin Number)		
					Differential	
AE	A2	A1	A0	Single Ended	"Hi"	"Lo"
0	0	0	0	0 (11)	None	
0	0	0	1	1 (10)	None	
0	0	1	0	2 (9)	None	
0	0	1	1	3 (8)	None	
0	1	0	0	4 (7)	None	
0	1	0	1	5 (6)	None	
0	1	1	0	6 (5)	None	
0	1	1	1	7 (4)	None	
1	0	0	0	8 (27)	0 (11)	0 (27)
1	0	0	1	9 (26)	1 (10)	1 (26)
1	0	1	0	10 (25)	2 (9)	2 (25)
1	0	1	1	11 (24)	3 (8)	3 (24)
1	1	0	0	12 (23)	4 (7)	5 (23)
1	1	0	1	13 (22)	5 (6)	5 (22)
1	1	1	0	14 (19)	6 (5)	6 (19)
1	1	1	1	15 (18)	7 (4)	7 (18)

Table I. Input Channel Addressing Truth Table

digital number to the four Input Channel Select address bits, AE, A0, A1, A2 (Analog Input Section, pins 28–31). In the differential mode, the eight channels are addressed by applying the appropriate digital code to A0, A1 and A2; AE must be enabled with a Logic "1". Internal logic monitors the status of the SE/DIFF Mode input and addresses the multiplexes singly or in pairs as required.

When the channel address is changed, six microseconds must be allowed for the Analog Input Section to settle to within ±0.01% of its final output (including settling times of all elements in the signal path). The effect of this delay may be eliminated by performing the address change while a conversion is in progress (with the sample-and-hold in the "hold" mode).

Input Channel Address Latch

The AD364 is equipped with a latch for the Input Channel Select address bits. If the Latch Control pin (pin 32 of the Analog Input Section) is at Logic "1", input channel select address information is passed through to the multiplexers. A Logic "0" "freezes" the input channel address present at the inputs at the time of the "1" to "0" transition.

This feature is useful when input channel address information is provided from an address, data or control bus that may be required to service many devices. The ability to latch an address is helpful whenever the user has no control of when address information may change.

Sample-and-Hold Mode Control

The Sample-and-Hold Mode Control input (Analog Input Section, pin 13) is normally connected to the Status output (pin 28) from the ADC section. When a conversion is initiated by applying a Convert Start control sequence, Status goes to Logic "1", putting the sample-and-hold into the "hold" mode. This "freezes" the information to be digitized for the period of conversion. When the conversion is complete, Status returns to Logic "0" and the sample-and-hold returns to the sample mode. Eighteen microseconds must be allowed for the sample-and-hold to acquire ("catch up" to) the analog input to within ±0.01% of the final value before a new Convert Start command is issued.

The purpose of a sample-and-hold is to "stop" fast changing input signals long enough to be converted. In this application, it also allows the user to change channels and/or SE/ DIFF mode while a conversion is in progress thus eliminating the effects of multiplexer, analog switch and differential amplifier settling times. If maximum throughput rate is required for slowly changing signals, the Sample-and-Hold Mode Control may be wired to ground (Logic "0") rather than to ADC Status thus leaving the sample-and-hold in a continuous sample mode.

Hold Capacitor

A 2000pF capacitor is provided with each AD364. One side of this capacitor is wired to the Analog Input Section pin 12, the other to analog ground as close to pin 17 as possible. The capacitor provided with the AD364J, K is Polystyrene while the wider operating temperature range of the AD364S, T demands a Teflon Capacitor (supplied).

Larger capacitors may be substituted to minimize noise, but acquisition time of the sample-and-hold will be extended. If less than 12 bits of accuracy is required, a smaller capacitor may be used. This will shorten the S/H acquisition time. In all cases, the proper capacitor dielectric must be used; i.e., Polystyrene (AD364J, K only) or Teflon (any grade). Other types of capacitors may have higher dielectric absorption (memory) and will cause errors. CAUTION: Polystyrene capacitors will be destroyed if subjected to temperatures above +85°C. No capacitor is required if the sample-and-hold is not used.

Analog Input Voltage Range Format

The AD364 may be configured for any of 2 bipolar or unipolar input voltage ranges as shown in Table II.

Range	Connect Analog Input To ADC Pin:	Connect Bipolar ADC Pin 12 To:
0 to +10V	13	–
-5V to +5V	13	8
-10V to +10V	14	8

Table II. Analog Input Voltage Range Pin Connections

15

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges; Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1 1 1	
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 1 1 0	
:	:	:	:	:	:	
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0 0 1	
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0 0 0	
:	:	:	:	:	:	
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0 0 1	
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0 0 0	

Table III. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

Analog Input Section Offset Adjust Circuit

The offset voltage of the AD364 may be adjusted at either the Analog Input Section or the ADC Section. Normally the adjustment is performed at the ADC but in some special applications, it may be helpful to adjust the offset of the Analog Input Section. An example of such a case would be if the input signals were small (<10mV) relative to Analog Input Section voltage offset and gain was inserted between the Analog Input Section and the ADC. To adjust the offset of the Analog Input Section, the circuit shown in Figure 7 is recommended. Under normal conditions, all calibration is performed at the ADC Section.

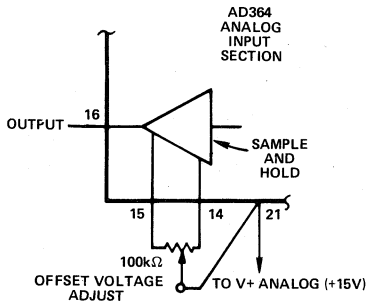


Figure 7. Analog Input Section Offset Voltage Adjustment

RANGE CONNECTIONS FOR THE ADC SECTION

The ADC contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +15, and -15 volts), the analog input, and the conversion initiation command, as discussed on page 6. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 8.

All of the thin film application resistors of the ADC are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD364K guarantees 4LSB max zero offset error and ±0.3% (8LSB) max full scale error (typical full scale error is ±2LSB). If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for an input range of 20V. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), gain trimmer R2 should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13. For a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14. The gain trim described below is now done with these trimmers. The nominal input impedance is 5kΩ into pin 13, and 10kΩ into pin 14.

Calibration

Calibration of the AD364 consists of adjusting offset and gain. Relative accuracy (linearity) is not affected by these adjustments, so if absolute zero and gain error is not important in a given application, or if system intelligence can correct for such errors, calibration may be unnecessary.

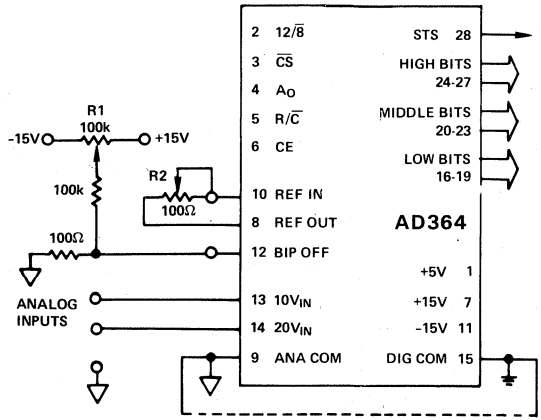


Figure 8. Unipolar Input Connections

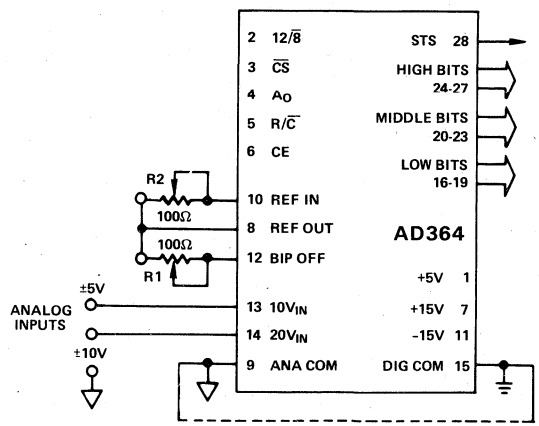


Figure 9. Bipolar Input Connections

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 8 and 9, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first, then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and -FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to +10V Range: Set analog input to +1LSB = +0.0024V. Adjust Zero for digital output = 000000000001; Zero is now calibrated. Set analog input to +FSR -2LSB = +9.9952V. Adjust Gain for 111111111110 digital output code; full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to +5.0000V; digital output code should be 100000000000.

-10V to +10V Range: Set analog input to -9.9951V; adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to +9.9902V; adjust Gain for 111111111110

digital output (offset binary) code. Half-scale calibration check: set analog input to 0.0000V; digital output (offset binary) code should be 100000000000.

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table III.

Zero and full-scale calibration can be accomplished to a precision of approximately ±¼LSB using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes", D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter II-4.*

Other Considerations

Grounding: The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the ADC; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD364 in an environment of high digital noise content, it is recommended that the analog and digital commons be connected together at the package. The digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV this noise may feed through the converter, so that some caution will be required in applying these grounds.

Power Supply Bypassing: The ±15V and +5V power leads should be capacitively bypassed to Analog Ground and Digital Ground respectively for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the system. High frequency power supply decoupling is required for the ADC section only. The AIS has power lead bypassed internally with a 0.039μF ceramic capacitor.

Applications

Transducer Interfacing

The precision +10V reference, buffer amplifier and mode switch can simplify transducer interfacing. Figure 10 illustrates how these features may be used to advantage. The AD590 is a temperature transducer that can be considered an ideal two-terminal current source with an output of one microamp per degree Kelvin (1μA/K). With an offsetting current of 273μA sourced from the +5.46 volt buffered reference through 20kΩ resistors (R1-R12) each of the 12 AD590 circuits develop -20mV/°C. The outputs are monitored with the AD364 front-end in the single-ended mode (Logic "0" on the Mode Control input).

The +5.46 volt reference is derived from the ADC +10 volt precision reference and voltage divider R13, R14. Low output impedance for this +5.46 volt reference is provided by the buffer amplifier. (The 3μV/°C offset voltage drift of the buffer amplifier contributes negligible errors.) At 0°C, each temperature transducer circuit delivers a 0 volt output. At 125°C, the output is -2.5V; at -55°C, the output is +1.10V. By using a two's complement ADC output (complementing MSB for a sign bit), the negative voltage versus temperature function is inverted and digital reading proportional to temperature in degrees centigrade is provided. Resolution is 0.061°C per least significant bit.

*Available from any Analog Devices sales office. Price is $5.95.

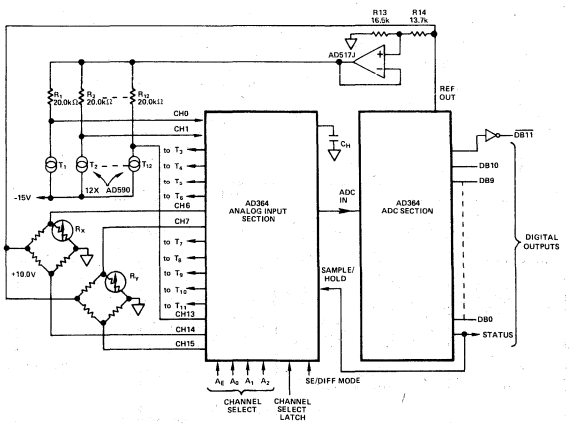


Figure 10. AD364 Transducer Interface Application

The precision +10 volt reference is also used to power several bridge circuits that require differential read-out. When addressing these bridge transducers, a Logic "1" at the mode control input will switch the AD364 to the differential mode. In many cases, this feature will eliminate the requirement for a differential amplifier for each bridge transducer.

Microprocessor Interfacing

The ADC section of the AD364 has a versatile set of control functions which will allow interface to a wide variety of microprocessor types as well as stand alone applications.

Table IV is a summary of the most poular microprocessor types and their interface requirements. Figures 11 & 12 are examples of the simplicity of the microprocessor interface, as it can be seen no additional parts are required to interface to a 6800 μP, only one gate for an 8080.

	AD574 CONTROL INPUTS			
μP	CE	R/C̄	C̄S̄	A0
MEMORY MAPPED I/O - 8080 - PROGRAMMED I/O	(MEMW • MEMR)	(MEMR)	DECODED ADDRESS	A0
	(I/OW • I/OR)	(I/OR)		
6800	ϕ_2	R/W̄	DECODED ADDRESS	A0
6502	ϕ_2	R/W̄	DECODED ADDRESS	A0
MEMORY MAPPED I/O - Z80 - PROGRAMMED I/O	(RD • WR)	(RD)	DECODED ADDRESS WITH MREQ	A0
			DECODED ADDRESS WITH IOR	
8048	(RD • WR)	(RD)	PORT 2_{0-3}*	PORT 2_{0-3}*

*Port 2, Lines 0-3 Can be Used as a 4 Bit Address Bus. System Address Decoding Requirements Vary from No Hardware to a Fully Latched 12-Bit Address, Depending on System Complexity.

Table IV. Recommended Control Signals for the ADC Section

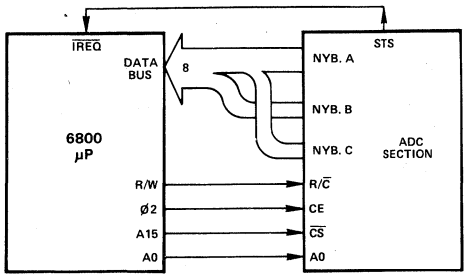


Figure 11. 6800 ⟷ ADC Interface

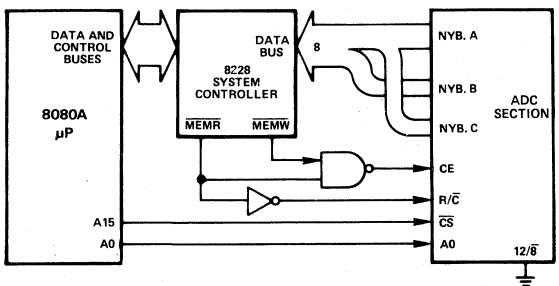
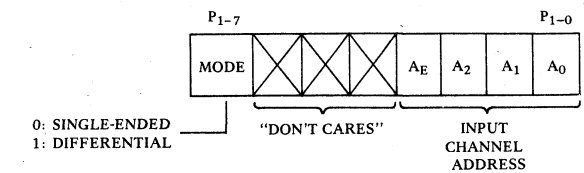


Figure 12. 8080 ⟷ ADC Interface

The single-chip microcomputers now available such as the 8048, 6801 and 3870 include fully decoded I/O ports on the chip, as well as CPU, clock, RAM and ROM. This sidesteps the need for address decoding for I/O devices in many systems. The 8048 contains 64 bytes of RAM, 1k bytes of ROM, and 2 programmable 8-bit I/O ports which can be used either as inputs or outputs. A third 8-bit port, designated BUS, is a bidirectional port which can be used for expanded I/O or memory.

The AD364 interfaces easily to an 8048 single-chip microcomputer to provide a complete data-acquisition system with minimal package count. In this system, 5 of the 8 bits of Port 1 drive the SE/DIFF MODE and channel select address inputs. Since the outputs of Port 1 are already latched, it is not necessary to use the latch built into the AD364. The LATCH input is tied to Logic "1" which causes the latch to be transparent. The set-up byte at Port 1 for the conversion takes the following format:



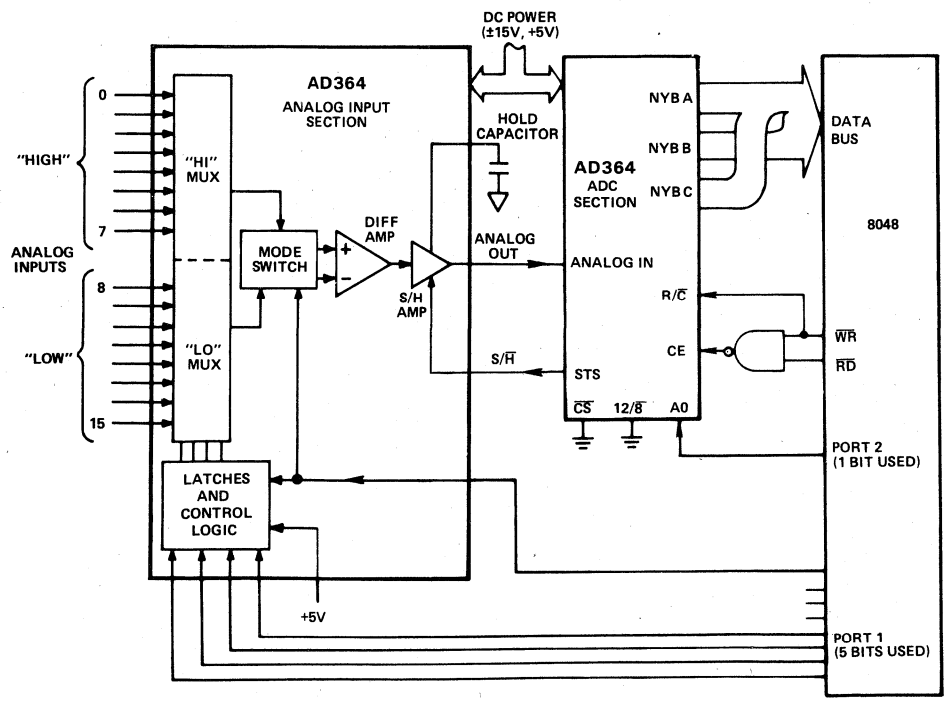


Figure 13. AD364/8048 Interface

CMOS Switches & Multiplexers

Contents

Selection Guide
CMOS Switches & Multiplexers

The devices catalogued in this section are grouped into two classes: Switches and Multiplexers. Descriptions, specifications, and application information can be found in the data sheets; definitions of the terminology can be found in the following pages.

CMOS IC SWITCHES

Type	Characteristics	Vol I Page
AD7510DI	Dielectrically Isolated Quad SPST; Address High Closes Switch	16-13
AD7511DI	Dielectrically Isolated Quad SPST; Address Low Closes Switch	16-13
AD7512DI	Dielectrically Isolated Quad SPDT	16-13
AD7590DI	Dielectrically Isolated Quad SPST; Data Latches	16-21
AD7591DI	Dielectrically Isolated Quad SPST; Data Latches	16-21
AD7592DI	Dielectrically Isolated Dual SPST; Data Latches	16-21

CMOS IC MULTIPLEXERS

Type	Characteristics	Vol I Page
AD7501	8-Channel Multiplexer, High Enables	16-5
AD7503	8-Channel Multiplexer, Low Enables	16-5
AD7502	4-Channel Differential Multiplexer	16-5
AD7506	16-Channel Multiplexer	16-9
AD7507	8-Channel Differential Multiplexer	16-9

Orientation
CMOS Switches & Multiplexers

Analog Devices offers a complete line of monolithic CMOS analog multiplexers and switches, which utilize a high-breakdown CMOS process, in conjunction with a double-layer interconnect for high density. Both 8- and 16-channel multiplexers are available, in one-line and two-line (4- and 8-channel differential) versions. The switches are dielectrically isolated duals and quads, available in a variety of contact forms. Both direct and inverted logic options are available for the most-popular types. The popular AD7510/11/12DI (quad SPST/dual SPDT), which utilize dielectric isolation, are latchup-proof and can withstand overrange to ±25V beyond the supplies.

CMOS switches have extremely low quiescent power dissipation, require little drive or supply current while switching, and are low in cost. Their R_{ON} is low and is, to a first-order, independent of applied voltage; in the off condition, leakage is quite small, both across the gate and to the drive and supply circuits. Most types respond to TTL/DTL, as well as CMOS, logic.

Definitions for terminal nomenclature used in the data sheets are given below, and a summary of device functions appears on the preceding page. General information on the nature of CMOS, its advantages, its applications, and its protection, is to be found in the *Guide to CMOS Switches and Multiplexers*, available from Analog Devices upon request.

MULTIPLEXER TERMINOLOGY

R_{ON}:	Ohmic resistance between the output and an addressed input.
R_{ON} vs. Temperature:	R_{ON} drift over the temperature range.
ΔR_{ON} between Switches:	Difference between the R_{ON}'s of any two switches.
R_{ON} vs. Temperature between Switches:	Difference between the R_{ON} drifts of any two switches.
I_S:	Current at any switch input, S1 through S_N. This is a leakage current when the switch is open.
I_{OUT}:	Current at the output. This is a leakage current when all switches are open.
$I_{OUT} - I_S$:	Difference between the current going into terminal "S" and the current going out of terminal "out" when terminal "S" is addressed.
V_{INL}:	Digital threshold voltage for the low state.
V_{INH}:	Digital threshold voltage for the high state.
C_S:	Capacitance between any open terminal "S" and ground.
C_{OUT}:	Capacitance between the output terminal and ground with all switches open.
C_{S-OUT}:	Capacitance between any open terminal "S" and the output terminal.
C_{SS}:	Capacitance between any two "S" terminals.
$t_{transition}$:	Delay time when switching from one address state to another.
t_{open}:	"OFF" time of both switches when switching from one address state to another.
t_{on} (En):	Delay time between the 50% points of the enable input and the switch "ON" condition.
t_{off} (En):	Delay time between the 50% points of the enable input and the switch "OFF" condition.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

SWITCH TERMINOLOGY

R_{DS}:	Ohmic resistance between terminals D and S.
I_D (I_S):	Current at terminals D or S. This is a leakage current when the switch is OFF.
I_{DS}:	Current flowing through the closed switch.
$I_D - I_S$:	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
V_D (V_S):	Analog voltage on terminal D (S).
C_S (C_D):	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}:	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
C_{DD} (C_{SS}):	Capacitance between terminals D (S) of any 2 switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}:	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}:	Delay time between the 50% points of the digital input and switch "OFF" condition.
V_{INL}:	Threshold voltage for the low state.
V_{INH}:	Threshold voltage for the high state.
I_{INL} (I_{INH}):	Input current of the digital input.
C_{IN}:	Input capacitance to ground of the digital input.
V_{DD}:	Most positive voltage supply.
V_{SS}:	Most negative voltage supply.
I_{DD}:	Positive supply current.
I_{SS}:	Negative supply current.

ANALOG DEVICES

CMOS 4/8 Channel Analog Multiplexers

AD7501, AD7502, AD7503

FEATURES
DTL/TTL/CMOS Direct Interface
Power Dissipation: 30μW
R_{ON}: 170Ω
Output "Enable" Control
AD7503 Replaces HI-1818

GENERAL DESCRIPTION

The AD7501 and AD7503 are monolithic CMOS, 8-channel analog multiplexers which switches one of 8 inputs to a common output depending on the state of three binary address lines and an "enable" input. The AD7503 is identical to the AD7501 except its "enable" logic is inverted. All digital inputs are TTL/DTL and CMOS logic compatible.

The AD7502 is a monolithic CMOS dual 4-channel analog multiplexer. Depending on the state of 2 binary address inputs and an "enable", it switches two output buses to two of 8 inputs.

All 3 devices are excellent examples of a high breakdown CMOS process combined with a double layer interconnect for high density. Silicon nitride passivation ensures long term stability and reliability.

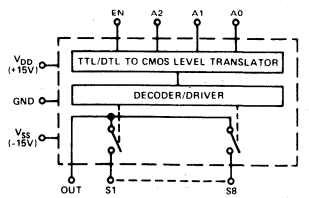
ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

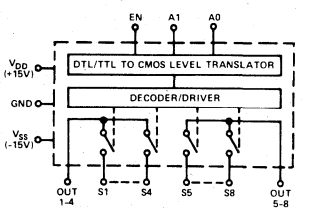
V_{DD} – GND . . . . . +17V
V_{SS} – GND . . . . . -17V
V Between Any Switch Terminals. 25V
Switch Current (I_S, Continuous) 35mA
Switch Current (I_S, Surge)
1ms duration, 10% duty cycle 50mA
Digital Input Voltage Range . . . . . V_{DD} to GND
Power Dissipation (package)
16-pin Cerdip and Ceramic DIP
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mV/°C
16-pin Plastic DIP
Up to +70°C. 670mW
Derates above +70°C by . . . . . 8.3mW/°C
Operating Temperature
Plastic (JN, KN Versions) . . . . . 0 to +70°C
Cerdip (JQ, KQ Versions) . . . . . -25°C to +85°C
Cerdip (SQ Versions) . . . . . -55°C to +125°C
Ceramic (JD, KD Versions) . . . . . -25°C to +85°C
Ceramic (SD Versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

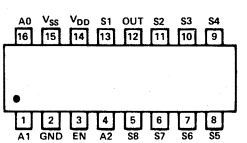
AD7501, AD7503 FUNCTIONAL BLOCK DIAGRAM



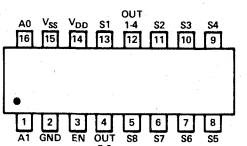
AD7502 FUNCTIONAL BLOCK DIAGRAM



AD7501, AD7503 PIN CONFIGURATION



AD7502 PIN CONFIGURATION



(NOT TO SCALE)

16-PIN DIP
TOP VIEW

16

SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER	VERSION[1]	SWITCH CONDITION	@25°C AD7501, AD7503	@25°C AD7502	OVER SPECIFIED TEMP. RANGE AD7501, AD7503	OVER SPECIFIED TEMP. RANGE AD7502	TEST CONDITIONS
ANALOG SWITCH							
R_{ON}	All	ON	170Ω typ, 300Ω max	*			-10V ≤ V_S ≤ +10V
R_{ON} vs. V_S	All	ON	20% typ	*			I_S = 1.0mA
R_{ON} vs. Temperature	All	ON	0.5%/°C typ	*			V_S = 0V, I_S = 1.0mA
ΔR_{ON} Between Switches	All	ON	4% typ	*			
R_{ON} vs. Temperature Between Switches	All	ON	±0.01%/°C	*			
I_S	J, K	OFF	0.2nA typ, 2nA max	*	50nA max	*	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V
	S	OFF	0.5nA max	*	50nA max	*	
I_{OUT}	J, K	OFF	1nA typ, 10nA max	0.6nA typ, 5nA max	250nA max	125nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V
	S	OFF	5nA max	3nA max	250nA max	125nA max	AD7501/02: Enable LOW AD7503: Enable HIGH
$\lvert I_{OUT} - I_S \rvert$	J, K	ON	12nA max	7nA max	300nA max	175nA max	V_S = 0
	S	ON	5.5nA max	3.5nA max	300nA max	175nA max	
DIGITAL CONTROL							
V_{INL}	All				0.8V max	*	
V_{INH}	J				3.0V min	*	Note 2
	K, S				2.4V min	*	
I_{INL} or I_{INH}	All		10nA typ	*			
C_{IN}	All		3pF typ	*			
DYNAMIC CHARACTERISTICS							
t_{ON}	All		0.8μs typ	*			V_{IN} = 0 to +5.0V (See Test Circuit 2)
t_{OFF}	All		0.8μs typ	*			
C_S	All	OFF	5pF typ	*			
C_{OUT}	All	OFF	30pF typ	15pF typ			
C_{S-OUT}	All	OFF	0.5pF typ	*			
C_{SS} Between Any Two Switches	All	OFF	0.5pF typ	*			
POWER SUPPLY							
I_{DD}	All		500μA max	*	500μA max	*	All Digital Inputs Low
I_{SS}	All		500μA max	*	500μA max	*	
I_{DD}	All		800μA max	*	800μA max	*	All Digital Inputs High
I_{SS}	All		800μA max	*	800μA max	*	

NOTES
*Same specifications as AD7501 and AD7503.
[1] JN, KN versions specified for 0 to +70°C; JQ, KQ, JD & KD versions for -25°C to +85°C; and SQ, SD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the AD7501J, AD7502J compatible with TTL/DTL levels. The maximum value is determined by the output leakage current of the driver gate when in the high state.

Specifications subject to change without notice.

TRUTH TABLES

AD7501				
A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8
X	X	X	0	None

AD7502			
A_1	A_0	E_N	"ON"
0	0	1	1 & 5
0	1	1	2 & 6
1	0	1	3 & 7
1	1	1	4 & 8
X	X	0	None

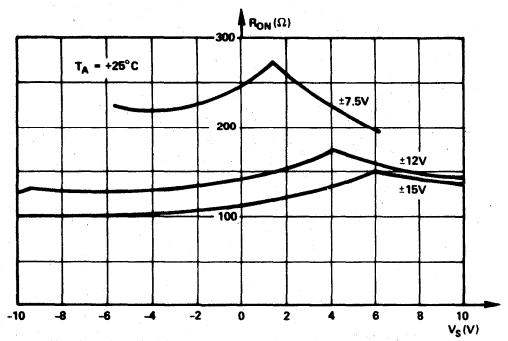
AD7503				
A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1
0	0	1	0	2
0	1	0	0	3
0	1	1	0	4
1	0	0	0	5
1	0	1	0	6
1	1	0	0	7
1	1	1	0	8
X	X	X	1	None

ORDERING INFORMATION[1]

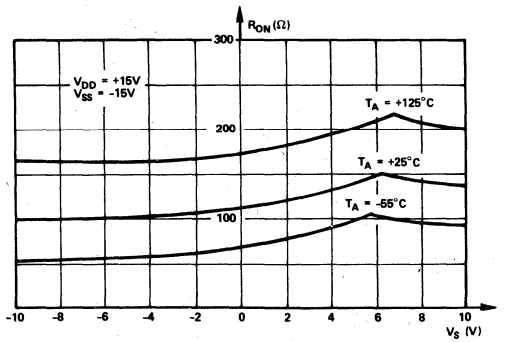
N16B Plastic (Suffix N)	Q16B Cerdip (Suffix Q)	D16B Ceramic (Suffix D)	Operating Temperature Range
AD7501JN AD7501KN AD7502JN AD7502KN AD7503JN AD7503KN			0 to +70°C
	AD7501JQ AD7501KQ AD7502JQ AD7502KQ AD7503JQ AD7503KQ	AD7501JD AD7501KD AD7502JD AD7502KD AD7503JD AD7503KD	-25°C to +85°C
	AD7501SQ AD7502SQ AD7503SQ	AD7501SD AD7502SD AD7503SD	-55°C to +125°C

NOTE
[1] See Section 19 for package outline information.

1. R_{ON} As A Function Of Switch Voltage (V_S)

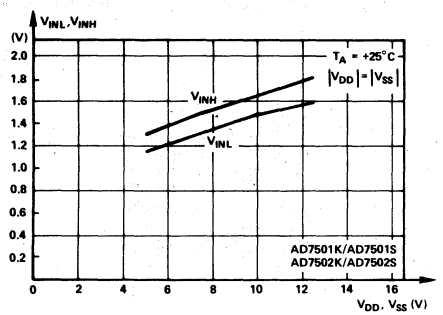


At Different Power Supplies

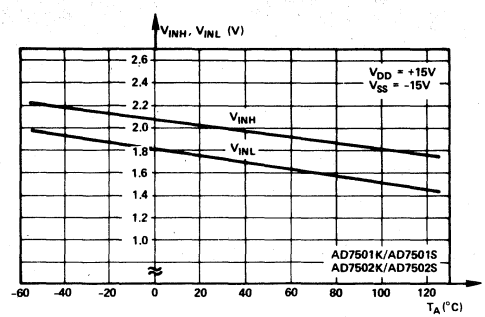


At Different Temperatures

2. Digital Threshold Voltage (V_{INH}, V_{INL})

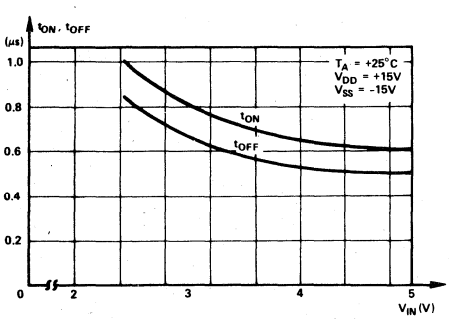


vs. Power Supply



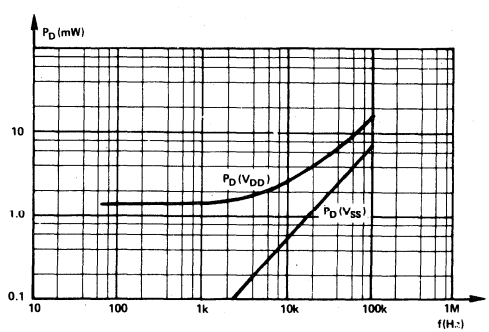
vs. Temperature

3. T_{ON}, T_{OFF}



vs. Digital Input Voltage

4. Power Dissipation

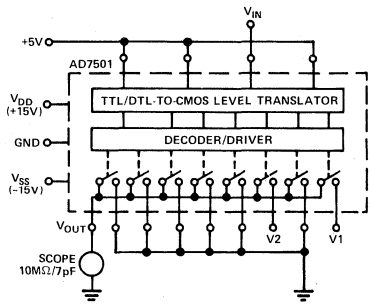


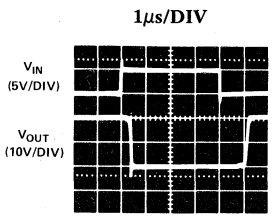
vs. Logic Frequency (50% Duty Cycle)

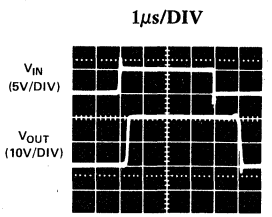
16

TYPICAL SWITCHING CHARACTERISTICS

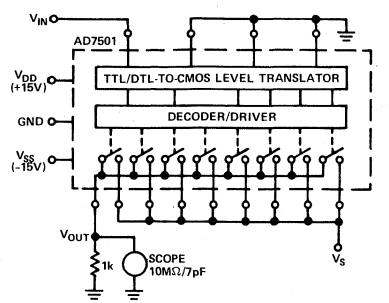
TEST CIRCUIT 1

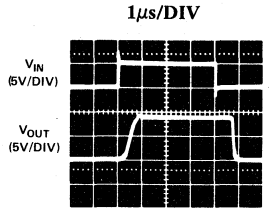


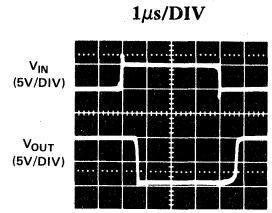


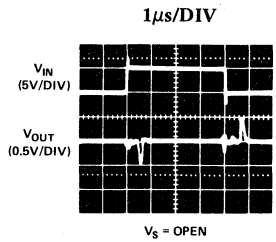


TEST CIRCUIT 2









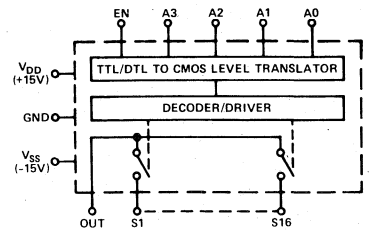
ANALOG DEVICES

CMOS 8- and 16-Channel Analog Multiplexers

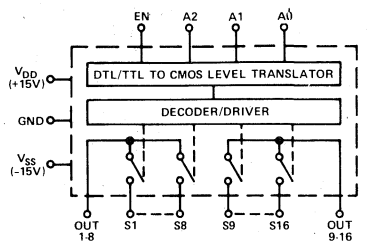
AD7506, AD7507

FEATURES
R_{ON}: 300Ω
Power Dissipation: 1.5mW
TTL/DTL/CMOS Direct Interface
Break-Before-Make Switching
Replaces DG506/DG507

AD7506 FUNCTIONAL BLOCK DIAGRAM



AD7507 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7506 is a monolithic CMOS 16-channel analog multiplexer packaged in a 28-pin DIP. It switches a common output to one of 16 inputs, depending on the state of four address lines and an "enable". The AD7507 is identical to the AD7506 except it has two outputs switched to two of 16 inputs depending on three binary address states and an "enable".

ABSOLUTE MAXIMUM RATINGS

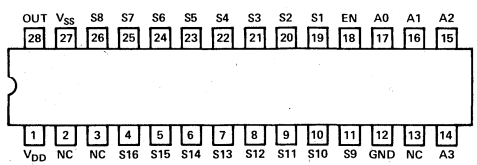
(T_A = +25°C unless otherwise noted)

V_{DD} – GND . . . . . +17V
V_{SS} – GND . . . . . -17V
V Between Any Switch Terminals 25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Switch Current (I_S, Continuous) 20mA
Switch Current (I_S, Surge)
  1ms duration, 10% duty cycle 35mA
Power Dissipation (Package)
28-pin Cerdip and Ceramic DIP
  Up to +50°C 1000mW
  Derates above +50°C by . . . . . 10mW/°C
28-pin Plastic DIP
  Up to +50°C 1200mW
  Derates above +50°C by . . . . . 12mW/°C
Operating Temperature
  Plastic (J, K versions) . . . . . 0 to +70°C
  Cerdip (J, K versions) . . . . . -25°C to +85°C
  Cerdip (S, T versions) . . . . . -55°C to +125°C
  Ceramic (J, K versions) . . . . . -25°C to +85°C
  Ceramic (S, T versions) . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C

CAUTION:

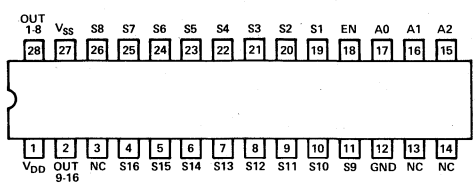
1. Do not apply voltages higher than V_{DD} and V_{SS} to any other terminal, especially when V_{SS} = V_{DD} = 0V all other pins should be at 0V.
2. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

AD7506 PIN CONFIGURATION
TOP VIEW



(NOT TO SCALE)

AD7507 PIN CONFIGURATION
TOP VIEW



(NOT TO SCALE)

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SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER		VERSION[1]	SWITCH CONDITION	@ +25°C	OVER SPECIFIED TEMP. RANGE	TEST CONDITIONS
ANALOG SWITCH						
R_{ON}		J, K	ON	300Ω typ, 450Ω max	550Ω max	V_S = -10V to +10V, I_S = 1mA
		S, T	ON	400Ω max	500Ω max	
R_{ON} vs. V_S		All	ON	15% typ		
R_{ON} vs. Temperature		All	ON	0.5%/°C typ		V_S = 0V, I_S = 1mA
ΔR_{ON} Between Switches		All	ON	4% typ		
R_{ON} vs. Temperature Between Switches		All	ON	0.05%/°C typ		
I_S (OFF)		J, K	OFF	0.05nA typ, 5nA max	50nA max	V_S = -10V, V_{OUT} = +10V and V_S = +10V, V_{OUT} = -10V "Enable" Low
		S, T	OFF	0.05nA typ, 1nA max	50nA max	
I_{OUT} (OFF)	AD7506	J, K	OFF	0.3nA typ, 20nA max	500nA max	
		S, T	OFF	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	OFF	0.3nA typ, 10nA max	250nA max	
		S, T	OFF	0.3nA typ, 5nA max	250nA max	
$I_{OUT} - I_S$ (Any Switch ON)	AD7506	J, K	ON	0.3nA typ, 20nA max	500nA max	V_S = 0
		S, T	ON	0.3nA typ, 10nA max	500nA max	
	AD7507	J, K	ON	0.3nA typ, 10nA max	250nA max	
		S, T	ON	0.3nA typ, 5nA max	250nA max	
DIGITAL CONTROL						
V_{INL}					0.8V max	Note 2
		J, S			3.0V min	
V_{INH}		K, T			2.4V min	
I_{INL} or I_{INH}		All		10µA max	30µA max	
C_{IN}		All		3pF typ		
DYNAMIC CHARACTERISTICS[3]						
$t_{TRANSITION}$		J, S		700ns typ		V_{IN}: 0 to 3.0V
		K, T		700ns typ, 1000ns max		
t_{OPEN}		All		100ns typ		
t_{ON} (En)		J, S		0.8µs typ		V_{EN}: 0 to 3.0V
		K, T		1.5µs max		
t_{OFF} (En)		J, S		0.8µs typ		
		K, T		1µs max		
"OFF" Isolation		All		70dB typ		V_{EN} = 0, R_L = 200Ω, C_L = 3.0pF, V_S = 3.0V rms, f = 50kHz
C_S		All	OFF	5pF typ		
C_{OUT}	AD7506	All	OFF	40pF typ		
	AD7507	All	OFF	20pF typ		
C_{S-OUT}		All	OFF	0.5pF typ		
C_{SS} Between Any Two Switches		All	OFF	0.5pF typ		
POWER SUPPLY						
I_{DD}		J, K	OFF	0.05mA typ, 1mA max		All Digital Inputs Low
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{SS}		J, K	OFF	0.05mA typ, 1mA max		
		S, T	OFF	0.05mA typ, 1mA max	2mA max	
I_{DD}		J, K	ON	0.3mA typ, 1mA max		All Digital Inputs High
		S, T	ON	0.3mA typ, 1mA max	2mA max	
I_{SS}		J, K	ON	0.05mA typ, 1mA max		
		S, T	ON	0.05mA typ, 1mA max	2mA max	

NOTES
[1] JN, KN versions specified for 0 to +70°C; JQ, KQ, JD and KD versions for -25°C to +85°C; and SQ, TQ, SD and TD versions for -55°C to +125°C.
[2] A pullup resistor, typically 1-2kΩ is required to make the J and S versions compatible with TTL/DTL. The maximum value is determined by the output leakage current of the driver gate when in the high state.
[3] AC parameters are sample tested to ensure conformance to specifications.

Specifications subject to change without notice.

TRUTH TABLES

AD7506

A_3	A_2	A_1	A_0	E_N	"ON"
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16
X	X	X	X	0	None

AD7507

A_2	A_1	A_0	E_N	"ON"
0	0	0	1	1 & 9
0	0	1	1	2 & 10
0	1	0	1	3 & 11
0	1	1	1	4 & 12
1	0	0	1	5 & 13
1	0	1	1	6 & 14
1	1	0	1	7 & 15
1	1	1	1	8 & 16
X	X	X	0	None

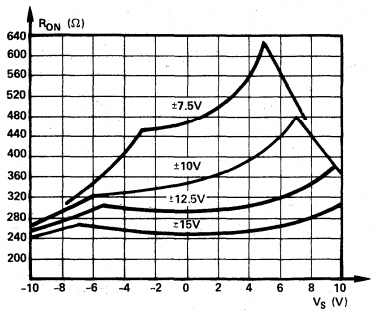
ORDERING INFORMATION[1]

N28A Plastic (Suffix N)	Q28A Cerdip (Suffix Q)	D28B Ceramic (Suffix D)	Operating Temperature Range
AD7506JN AD7506KN AD7507JN AD7507KN			0 to +70°C
	AD7506JQ AD7506KQ AD7507JQ AD7507KQ	AD7506JD AD7506KD AD7507JD AD7507KD	-25°C to +85°C
	AD7506SQ AD7506TQ AD7507SQ AD7507TQ	AD7506SD AD7506TD AD7507SD AD7507TD	-55°C to +125°C

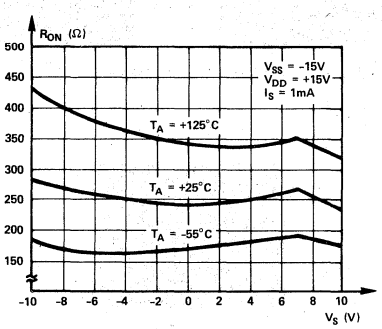
NOTE
[1] See Section 19 for package outline information.

Typical Performance Characteristics

1. R_{ON} vs. V_S

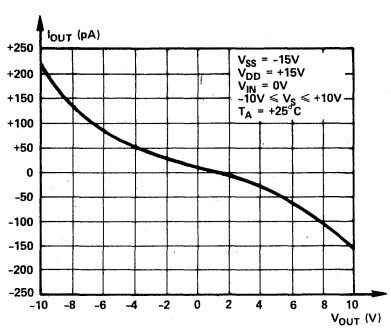


At Different Power Supplies

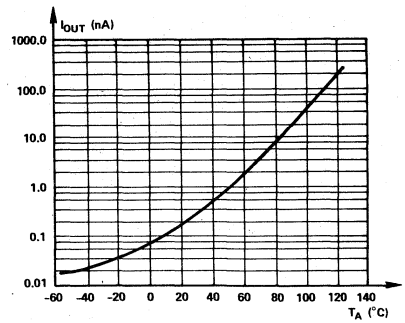


At Different Temperatures

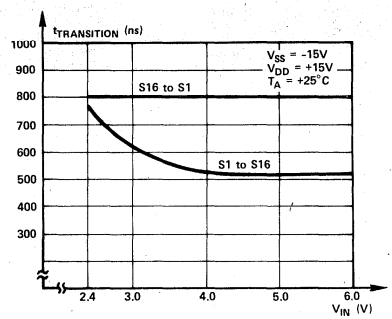
2. I_{OUT} vs. V_{OUT}



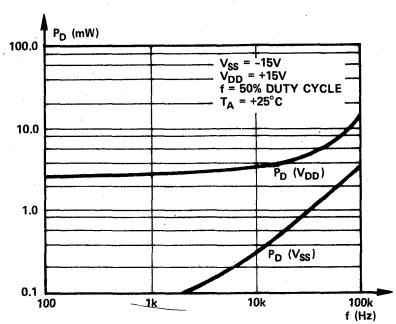
3. I_{OUT} vs. T_A



4. $t_{TRANSITION}$ vs. V_{IN}



5. P_D vs. Logic Frequency



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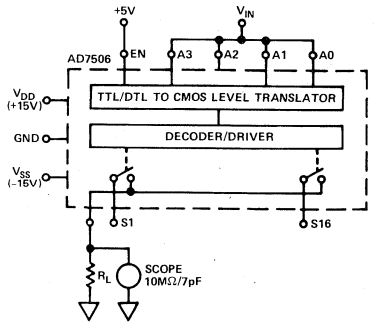
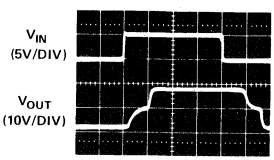
TYPICAL SWITCHING CHARACTERISTICS

TEST CIRCUIT 1

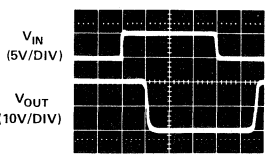


0.5μs/DIV



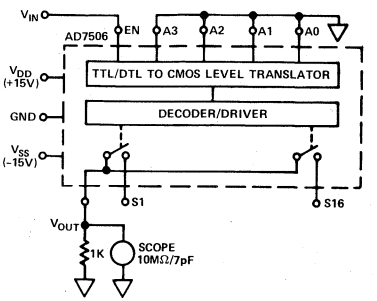
S_1 = -10V, S_{16} = +10V,
$S_2 - S_{15}$ = 0V, R_L = 1K

0.5μs/DIV

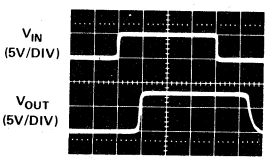


S_1 = +10V, S_2 = -10V,
$S_2 - S_{15}$ = 0V, R_L = ∞

TEST CIRCUIT 2

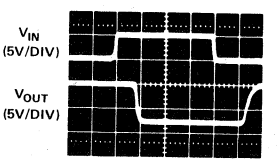


0.5μs/DIV



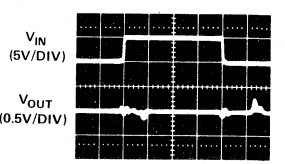
S_1 through S_{16} = +10V

0.5μs/DIV



S_1 through S_{16} = -10V

0.5μs/DIV



S_1 through S_{16} = 0V

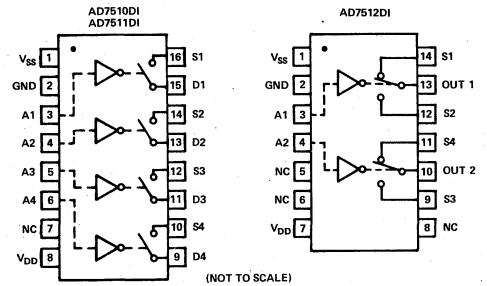
ANALOG DEVICES

DI CMOS Protected Analog Switches

AD7510DI, AD7511DI, AD7512DI

FEATURES
Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Low Dissipation: 3mW
TTL/CMOS Direct Interface
Silicon-Nitride Passivated
Monolithic Dielectrically-Isolated CMOS

AD7510DI, AD7511DI, AD7512DI
FUNCTIONAL BLOCK DIAGRAMS



16-PIN DIP TOP VIEW **14-PIN DIP TOP VIEW**

GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged in a 14-pin DIP.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP
AD7510DI, AD7511DI – (D16B)
AD7512DI – (D14B)
Suffix N: Plastic DIP
AD7510DI, AD7511DI – (N16B)
AD7512DI – (N14B)

[1] See Section 19 for package outline information.

ORDERING INFORMATION

Plastic (Suffix N)	Cerdip (Suffix Q)	Ceramic (Suffix D)	Operating Temperature Range
AD7510DIJN AD7510DIKN AD7511DIJN AD7511DIKN AD7512DIJN AD7512DIKN			0 to +70°C
	AD7510DIJQ AD7510DIKQ AD7511DIJQ AD7511DIKQ AD7512DIJQ AD7512DIKQ	AD7510DIJD AD7510DIKD AD7511DIJD AD7511DIKD AD7512DIJD AD7512DIKD	-25°C to +85°C
	AD7510DISQ AD7511DISQ AD7511DITQ AD7512DISQ AD7512DITQ	AD7510DISD AD7511DISD AD7511DITD AD7512DISD AD7512DITD	-55°C to +125°C

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

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SPECIFICATIONS (V_{DD} = +15V, V_{SS} = –15V unless otherwise noted)

COMMERCIAL VERSIONS (J, K)

PARAMETER	MODEL	VERSION	+25°C	0 to +70°C (N) –25°C to +85°C (Q, D)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	J, K	75Ω typ, 100Ω max	175Ω max	$-10V \leqslant V_D \leqslant +10V$
R_{ON} vs V_D (V_S)	All	J, K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	J, K	+0.5%/°C typ		
R_{ON} Match	All	J, K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	J, K	0.01%/°C typ		
I_D (I_S)$_{OFF}$[1]	All	J, K	0.5nA typ, 5nA max	500nA max	V_D = –10V, V_S = +10V and V_D = +10V, V_S = –10V
I_D (I_S)$_{ON}$[1]	All	J, K	10nA max		$V_S = V_D$ = +10V $V_S = V_D$ = –10V
I_{OUT}[1]	AD7512DI	J, K	15nA max	1500nA max	$V_{S1} = V_{OUT} = \pm 10V$, $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$, $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL}[1]	All	J, K		0.8V max	
V_{INH}[1]	All	J		3.0V min	
	All	K		2.4V min	
C_{IN}	All	J, K	3pF typ		
I_{INH}[1]	All	J, K	10nA max		$V_{IN} = V_{DD}$
I_{INL}[1]	All	J, K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	J, K	180ns typ		
	AD7511DI	J, K	350ns typ		V_{IN} = 0 to +3.0V
t_{OFF}	AD7510DI	J, K	350ns typ		
	AD7511DI	J, K	180ns typ		
$t_{TRANSITION}$	AD7512DI	J, K	300ns typ		
C_S (C_D)OFF	All	J, K	8pF typ		
C_S (C_D)ON	All	J, K	17pF typ		
C_{DS} (C_{S-OUT})	All	J, K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	J, K	0.5pF typ		
C_{OUT}	AD7512DI	J, K	17pF typ		
Q_{INJ}	All	J, K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to –10V
POWER SUPPLY					
I_{DD}[1]	All	J, K	800μA max	800μA max	All digital inputs = V_{INH}
I_{SS}	All	J, K	800μA max	800μA max	
I_{DD}[1]	All	J, K	500μA max	500μA max	All digital inputs = V_{INL}
I_{SS}	All	J, K	500μA max	500μA max	

NOTES
[1] 100% tested.
Specifications subject to change without notice.

EXTENDED TEMPERATURE RANGE VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	S, T	100Ω max	175Ω max	$-10V \leqslant V_D \leqslant +10V$ I_{DS} = 1mA
I_D (I_S)$_{OFF}$ [1]	All	S, T	3nA max	200nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D (I_S)$_{ON}$ [1]	All	S, T	10		$V_S = V_D$ = +10V and $V_S = V_D$ = -10V
I_{OUT} [1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	S, T		0.8V max	
V_{INH} [1,2]	AD7510DI	S		2.4V min	
	AD7511DI	T		2.4V min	
	AD7512DI	T		2.4V min	
	AD7511DI	S		3.0V min	
	AD7512DI	S		3.0V min	
I_{INH} [1]	All	S, T	10nA max		$V_{IN} = V_{DD}$
I_{INL}	All	S, T	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON} [3]	AD7510DI	S,	1.0μs max		V_{IN} = 0 to +3V
	AD7511DI	S, T	1.0μs max		
t_{OFF} [3]	AD7510DI	S, T	1.0μs max		
	AD7511DI	S, T	1.0μs max		
$t_{TRANSITION}$ [3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD} [1]	All	S, T		800μA max	All digital inputs = V_{INH}
I_{SS} [1]	All	S, T		800μA max	
I_{DD}	All	S, T		500μA max	All digital inputs = V_{INL}
I_{SS} [1]	All	S, T		500μA max	

NOTES
[1] 100% tested.
[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISD and AD7512DISD TTL compatible.
[3] Guaranteed, not production tested.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . 0V to V_{DD}
Power Dissipation (Package)
14 & 16 pin Cerdip & Ceramic DIP
Up to +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
14 & 16 pin Plastic Dip
Up to +70°C. 670mW
Derates above +75°C by . . . . . 8.3mW/°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Plastic (J, K Versions) . . . . . 0 to +70°C
Cerdip (J, K Versions) . . . . . -25°C to +85°C
Cerdip (S, T Versions) . . . . . -55°C to +125°C
Ceramic (J, K Versions) . . . . . -25°C to +85°C
Ceramic (S, T Versions) . . . . . -55°C to +125°C

CAUTION: The digital control inputs are diode protected; however, permanent damage may occur on unconnected units under high electrostatic fields. Keep unused units in conductive foam at all times. Prior to pulling the devices from the conductive foam, ground the foam to deplete any accumulated charge.

CIRCUIT DESCRIPTION

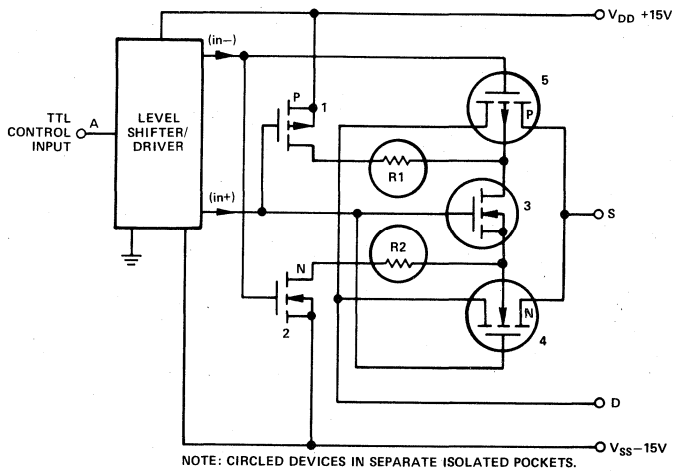


Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in–) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7510DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

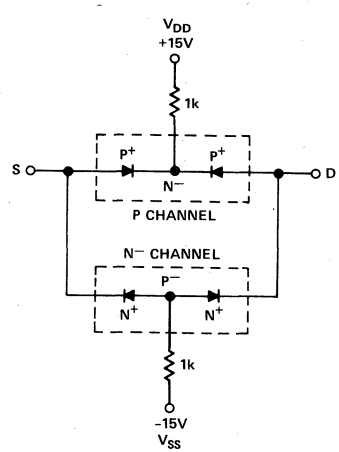
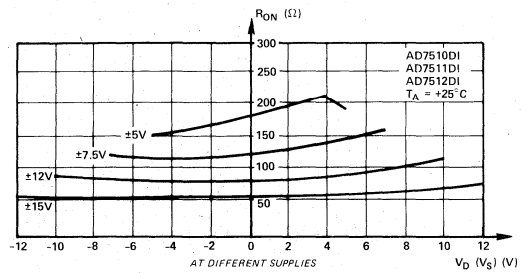
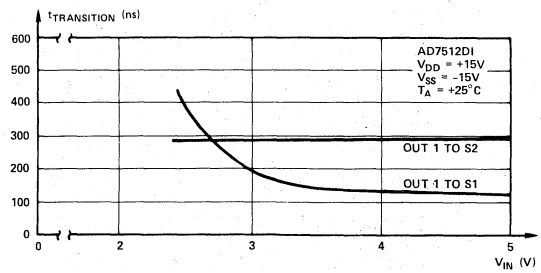


Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit

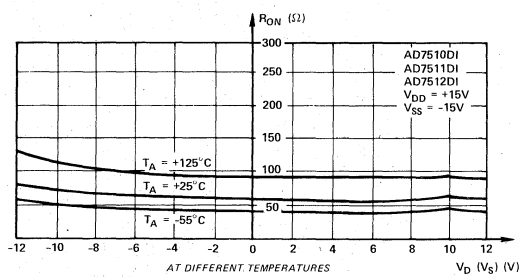
TYPICAL PERFORMANCE CHARACTERISTICS



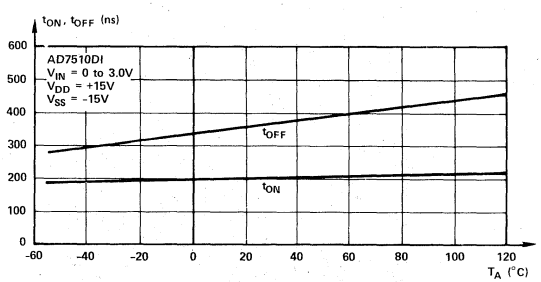
R_{ON} as a Function of V_D (V_S)



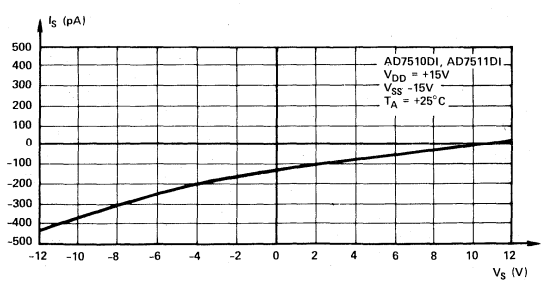
$t_{TRANSITION}$ as a Function of Digital Input Voltage



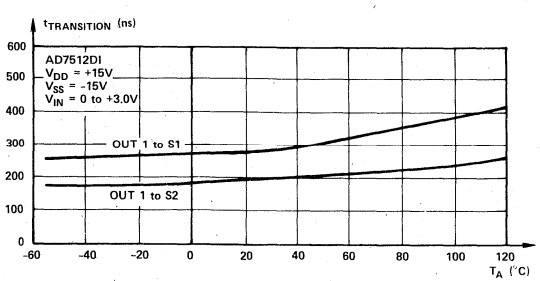
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature



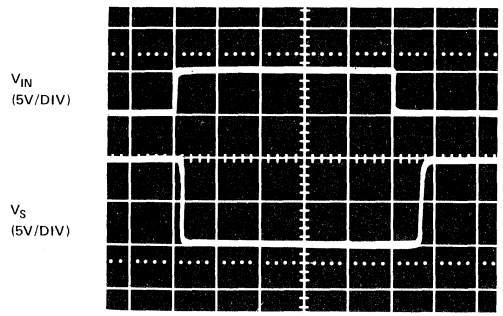
I_S, $(I_D)_{OFF}$ vs V_S



$t_{TRANSITION}$ as a Function of Temperature

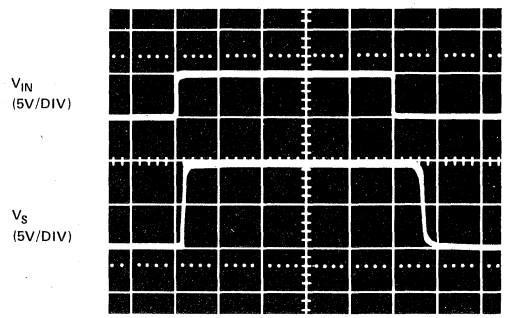
16

0.5μs/DIV



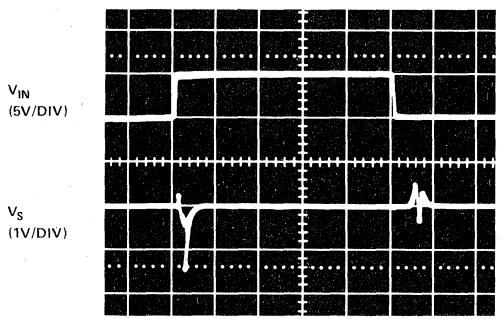
Switching Waveforms for V_D = -10V

0.5μs/DIV



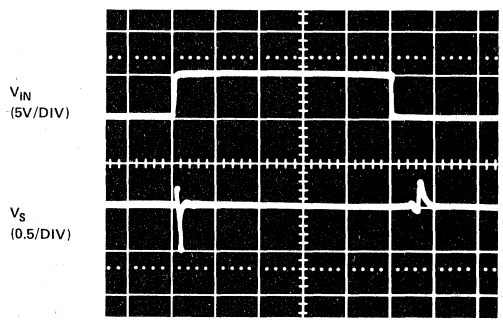
Switching Waveforms for V_D = +10V

0.5μs/DIV



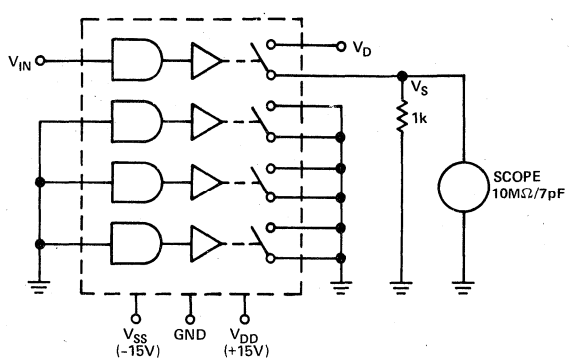
Switching Waveforms for V_D = Open

0.5μs/DIV



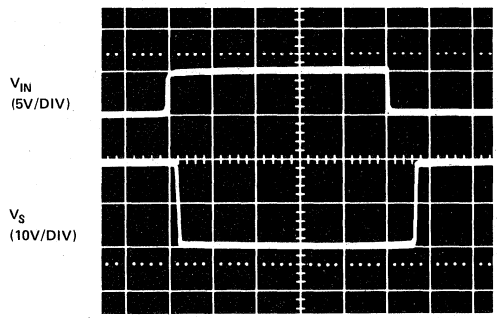
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



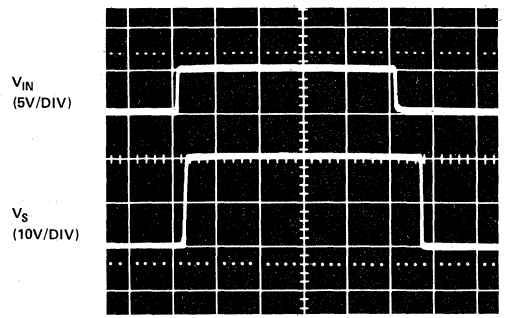
TYPICAL SWITCHING CHARACTERISTICS AD7512DI

0.5μs/DIV



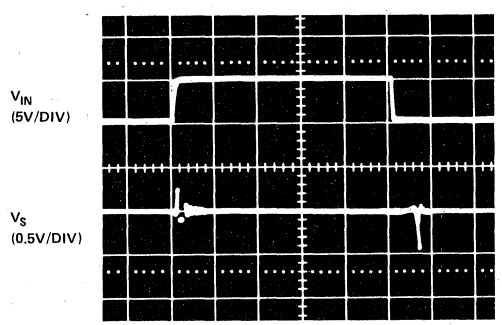
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

0.5μs/DIV



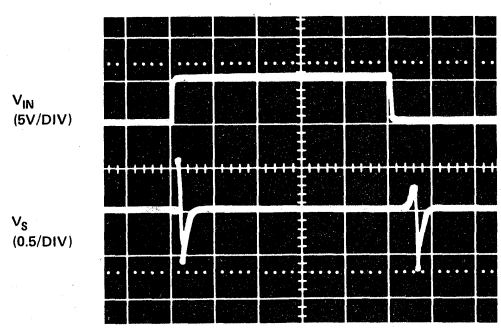
Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

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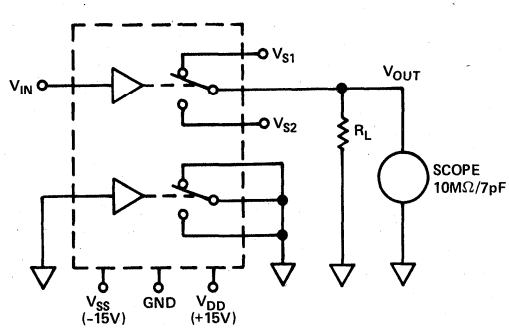
AD7512DI TEST CIRCUIT



TERMINOLOGY

R_{ON}: Ohmic resistance between terminals D and S.

R_{ON} Drift Match: Difference between the R_{ON} drift of any two switches.

R_{ON} Match: Difference between the R_{ON} of any two switches.

I_D $(I_S)_{OFF}$: Current at terminals D or S. This is a leakage current when the switch is "OFF."

I_D $(I_S)_{ON}$: Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)

V_D (V_S): Analog voltage on terminal D (S).

C_S (CD): Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)

C_{DS}: Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)

C_{DD} (C_{SS}): Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)

t_{ON}: Delay time between the 50% points of the digital input and switch "ON" condition.

t_{OFF}: Delay time between the 50% points of the digital input and switch "OFF" condition.

$t_{transition}$: Delay time when switching from one address state to another.

V_{INL}: Threshold voltage for the low state.

V_{INH}: Threshold voltage for the high state.

I_{INL} (I_{INH}): Input current of the digital input.

C_{IN}: Input capacitance to ground of the digital input.

V_{DD}: Most positive voltage supply.

V_{SS}: Most negative voltage supply.

I_{DD}: Positive supply current.

I_{SS}: Negative supply current.

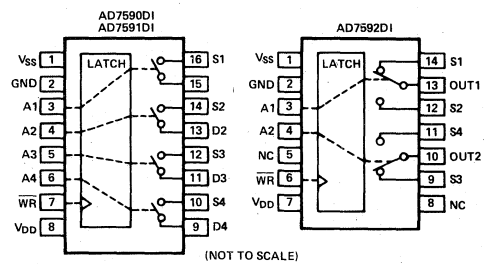
ANALOG DEVICES

DI CMOS
Analog Switches with Data Latches

AD7590DI, AD7591DI, AD7592DI

FEATURES
SCR Latch-Proof
Overvoltage-Proof: ±25V
Low R_{ON}: 75Ω
Buffered Switch Logic
TTL, CMOS Compatible
Monolithic Dielectrically-Isolated CMOS
Pin Compatible with AD7510DI Series

AD7590DI, AD7591DI, AD7592DI
FUNCTIONAL BLOCK DIAGRAMS



16-PIN DIP TOP VIEW **14-PIN DIP TOP VIEW**

GENERAL DESCRIPTION

The AD7590DI, AD7591DI and AD7592DI are a family of protected (latch proof) dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. Microprocessor interfacing is facilitated by the provision of on-chip data latches.

The AD7590DI and AD7591DI consist of four independent SPST analog switches packaged in a 16-pin DIP. They differ only in that the switch control logic is inverted. The AD7592DI has two independent SPDT switches packaged in a 14-pin DIP.

ORDERING INFORMATION

Plastic (Suffix N)	Cerdip (Suffix Q)	Ceramic (Suffix D)	Operating Temperature Range
AD7590DIKN AD7591DIKN AD7592DIKN			0 to +70°C
	AD7590DIBQ AD7591DIBQ AD7592DIBQ	AD7590DIBD AD7591DIBD AD7592DIBD	-25°C to +85°C

CONTROL LOGIC ($\overline{WR}$ HELD LOW)

AD7590DI: Switch "ON" for Address "HIGH"

AD7591DI: Switch "ON" for Address "LOW"

AD7592DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

PACKAGE IDENTIFICATION[1]

Suffix D: Ceramic DIP Package
AD7590, AD7591 – (D16B)
AD7592 – (D14B)

Suffix N: Plastic DIP Package
AD7590, AD7591 – (N16B)
AD7592 – (N14B)

NOTE
[1] See Section 19 for package outline information.

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SPECIFICATIONS (V_{DD} = +15V, V_{SS} = -15V unless otherwise noted)

PARAMETER	MODEL	T_A = +25°C	T_A = OPERATING TEMPERATURE RANGE	TEST CONDITIONS/COMMENTS
ANALOG SWITCH				
R_{ON}[1]	All	60Ω typ, 90Ω max	120Ω max	$-10V \leqslant V_D \leqslant +10V$ I_{DS} = 1.0mA
R_{ON} Match[2]	All	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Match Drift[2]	All	0.01%/°C typ		
I_D (I_S) OFF[1]	All	0.5nA typ, 5nA max	100nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D (I_S) ON[1]	All	0.5nA typ, 5nA max	100nA max	V_S = V_D = +10V and V_S = V_D = -10V
I_{OUT}[1]	AD7592DI	1.0nA typ, 10nA max	200nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
C_S (C_D) OFF[3]	All	10pF typ		
C_S (C_D) ON[3]	All	30pF typ		
C_{DS} (C_{S-OUT})[3]	All	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})[3]	All	0.5pF typ		
C_{OUT}[3]	AD7592DI	40pF typ		
DIGITAL CONTROL				
V_{INL}[1]	All	0.8V max	0.8V max	
V_{INH}[1]	All	2.4V min	2.4V min	
C_{IN}[3]	All	5pF typ	5pF typ	
I_{INH}[1,4]	All	1μA max	1μA max	V_{IN} = 0 or V_{DD}
I_{INL}[1,4]	All	1μA max	1μA max	
DYNAMIC CHARACTERISTICS				
t_{ON}[2]	AD7590DI	170ns typ, 340ns max	190ns typ, 380ns max	
	AD7591DI	300ns typ, 600ns max	380ns typ, 760ns max	
t_{OFF}[2]	AD7590DI	300ns typ, 600ns max	380ns typ, 760ns max	
	AD7591DI	170ns typ, 340ns max	190ns typ, 380ns max	
$t_{TRANSITION}$[2]	AD7592DI	300ns typ, 600ns max	380ns typ, 760ns max	
Write Pulse-Width (t_{WR})[2]	All	300ns typ, 400ns min	400ns typ, 500ns min	
Address Set Up Time (t_{AS})[2]	All	0ns min	0ns min	See Figure 1
Address Hold Time (t_{AH})[2]	All	150ns typ, 250ns min	250ns typ, 350ns min	
OFF Isolation[3] (Analog Input to Analog Output)	All	Better than -85dB at 1kHz. Feedthrough primarily dependent upon printed circuit board layout.		
Crosstalk[3] (Digital Input to Analog Output)	All	5mV peak, typ		R_L = 1MΩ, C_L = 15pF V_{INH} = 3.0V, V_{INL} = 0V t_{rise} = t_{fall} = 20ns WR held HIGH
Q_{INJ} (Charge Injection)[3]	All	40pC typ		Measured at S or D terminal, C_L = 1000pF V_{IN} = 0 to 3.0V, V_D (V_S) = +10V to -10V, WR held LOW
POWER SUPPLY				
I_{DD}[1]	All	1mA max	1mA max	All digital inputs
I_{SS}[1]	All	1mA max	1mA max	V_{IN} = V_{INH} or V_{INL}

NOTES
[1] 100% tested.
[2] Guaranteed, not production tested.
[3] Typical values for information only, not subject to test or guarantee.
[4] Inputs are MOS gates typical current less than 10nA.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . +17V
V_{SS} to GND . . . . . -17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . . V_{DD} +25V
or V_{SS} -25V
(Continuous) . . . . . V_{DD} +20V
or V_{SS} -20V
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . . -0.3V to V_{DD} +0.3V

Power Dissipation (Package)
14- & 16-pin Cerdip & Ceramic DIP
Up to +75°C. 450mW
Derates above +75°C by . . . . . 6mW/°C
14- & 16-pin Plastic Dip
Up to +70°C. 670mW
Derates above +75°C by . . . . . .8.3mW/°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature
Plastic (KN Versions). . . . . 0 to +70°C
Cerdip (BQ Versions). . . . . -25°C to +85°C
Ceramic (BD Versions) . . . . . -25°C to +85°C

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

TIMING AND CONTROL SEQUENCE

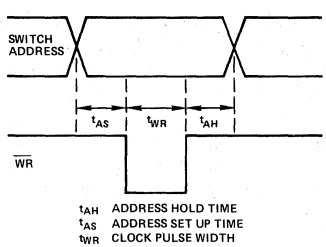

Figure 1. Timing and Control Sequence

Figure 1 shows the timing sequence for latching the switch address. The minimum data set up time is zero so that the data may change coincident with the falling edge of $\overline{WR}$. The address is latched on the rising edge of $\overline{WR}$ and address must be held for T_{AH} minimum to guarantee that it will be latched. While $\overline{WR}$ is held low the latch is transparent and the switches respond to changes in the input address.

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CIRCUIT DESCRIPTION

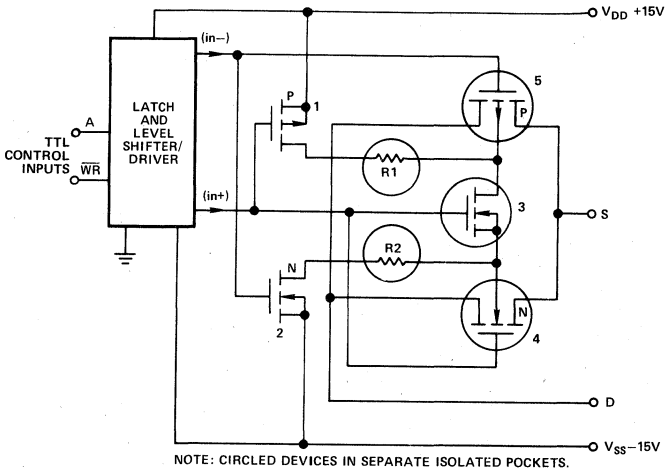


Figure 2. Typical Output Switch Circuitry of AD7590DI Series

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenum necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7590DI series switches utilize a dielectrically-isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in–) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 is "ON." Hence, the back-gates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. (The circled devices are located in separate dielectrically isolated pockets.) Floating the output switch back-gates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the back-gates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-back-gate diode is forward biased; however, R1 and R2 provide current limiting action.

Consequently, without external current limiting resistance (or increased R_{ON}), the AD7590DI series switches provide:

1. Latch-proof operation
2. Overvoltage protection 25V beyond the V_{SS} and V_{DD} supply voltage

An equivalent circuit of the output switch element in Figure 3 shows that, indeed the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices—*not* in series with the signal path between the S and D terminals.

In some applications it is possible to turn on a parasitic NPN (drain to back-gate to source of the N-channel) transistor, causing device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or current limiting devices (output of op amps) will prevent damage to the device.

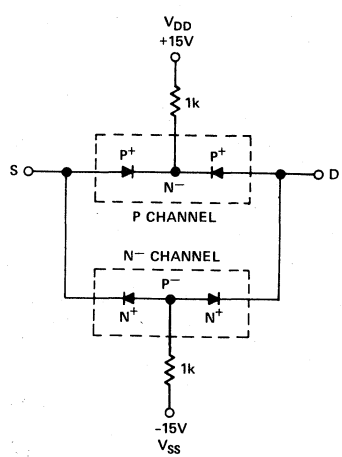
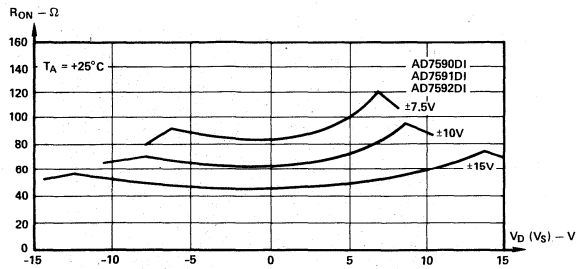
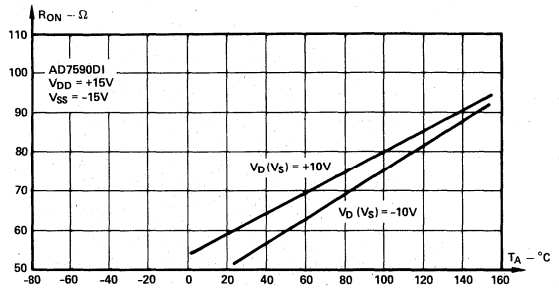


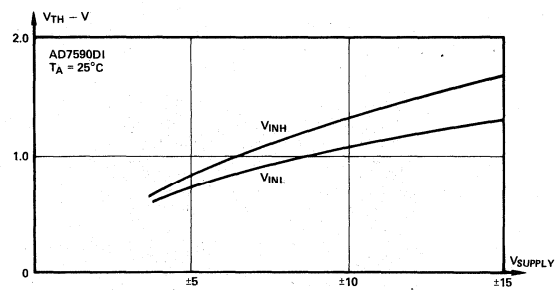
Figure 3. AD7590DI Series Output Switch Diode-Equivalent-Circuit



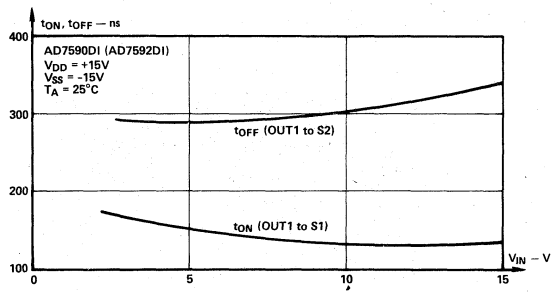
R_{ON} as a Function of V_D (V_S) for Different Supply Voltages



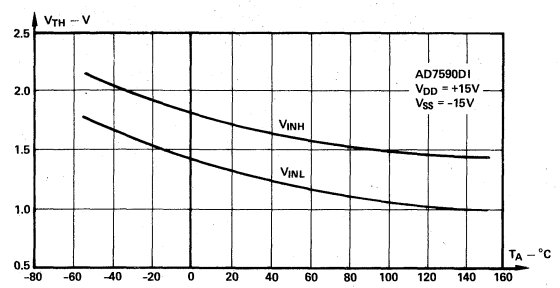
R_{ON} as a Function of Temperature



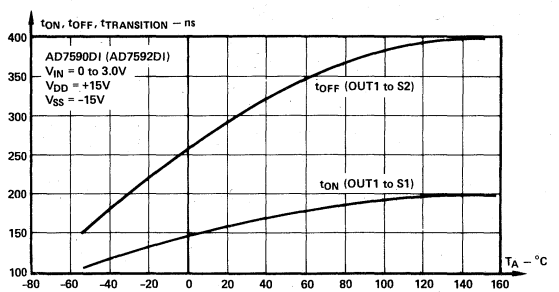
Threshold Voltage as a Function of Supply Voltage



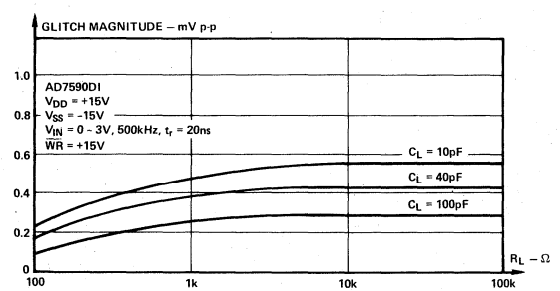
t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Digital Input Voltage



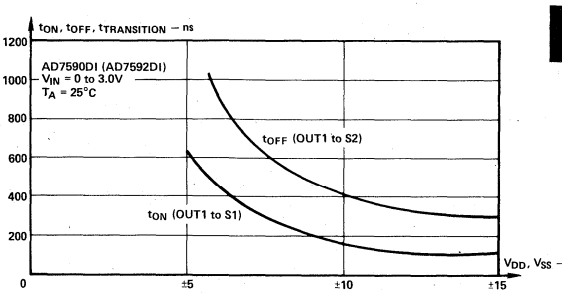
Threshold Voltage as a Function of Temperature



t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Temperature



Digital Crosstalk as a Function of Load Impedance



t_{ON}, t_{OFF} ($t_{TRANSITION}$) as a Function of Supply Voltage

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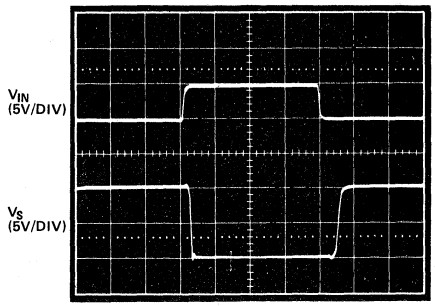
TYPICAL SWITCHING CHARACTERISTICS

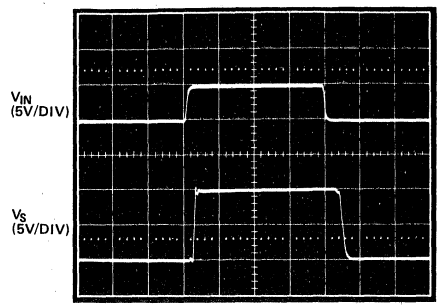
AD7590DI, AD7591DI

0.5μs/DIV



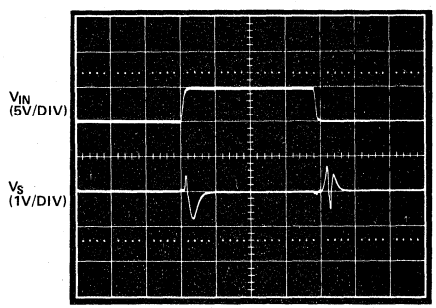
Switching Waveform for V_D = -10V

0.5μs/DIV



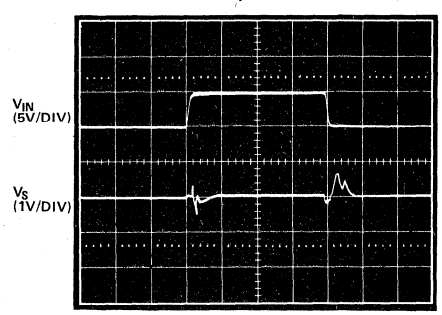
Switching Waveform for V_D = +10V

0.5μs/DIV



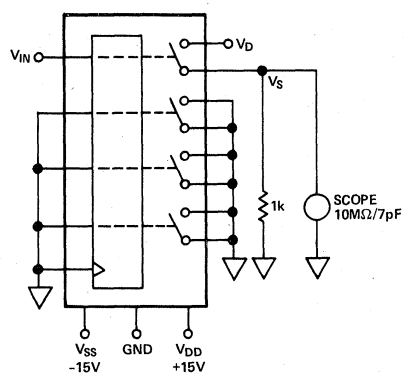
Switching Waveform for V_D = 0

0.5μs/DIV



Switching Waveform for V_D = 0V

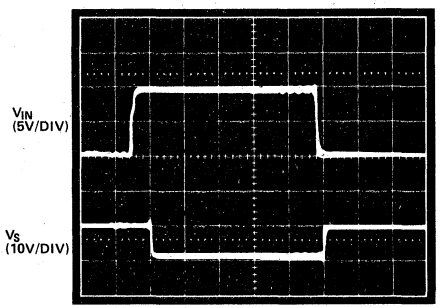
AD7590DI, AD7591DI TEST CIRCUIT



TYPICAL SWITCHING CHARACTERISTICS

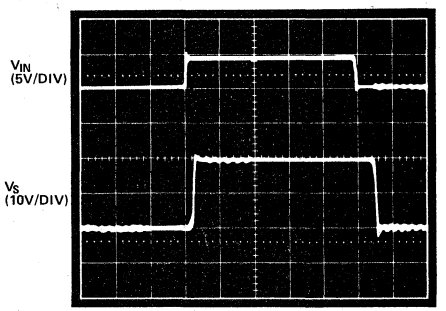
AD7592DI

0.5μs/DIV



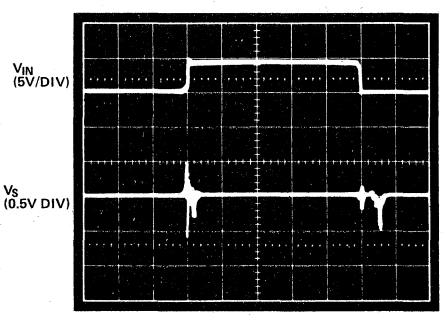
Switching Waveforms for V_{S1} = -10V, V_{S2} = +10V, R_L = 1kΩ

0.5μs/DIV



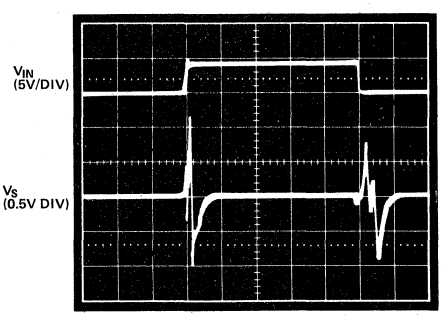
Switching Waveforms for V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



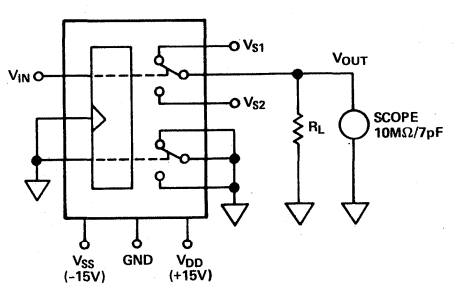
Switching Waveforms for V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for V_{S1} and V_{S2} = Open, R_L = 1kΩ

AD7592DI TEST CIRCUIT



16

Monolithic Chips

Contents

•New product since publication of the *1982–1983 Databook Update.*

DACPORT is a registered trademark of Analog Devices, Inc.

Bipolar Integrated Circuit Chips
General Information

PHYSICAL CHARACTERISTICS

Die Thickness: The standard thickness of Analog Devices Bipolar dice is 20 mils ±2 mils.

Die Dimensions: The dimensions given on the specific device data sheets have a tolerance of ±2 mils.

Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization on Analog Devices Bipolar dice is aluminum. Minimum thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows are 3.5 mils by 3.5 mils minimum.

PACKAGING

All dice are packaged in plastic waffle packs. The quantity of dice per package depends on die size.

A sheet of anti-static paper and a sheet of anti-static plastic is included in each pack.

Waffle packs are secured and shipped in cardboard shipping containers.

ASSEMBLY INFORMATION

Cleaning: Each die is cleaned prior to packaging in waffle packs. No additional cleaning is recommended.

Dice Inspection: Standard dice are 100% inspected.

Die Attach: The proper method of die attach is determined by the requirements of the particular application.

If an adhesive die attach technique is required by the constraints of the application, then package moisture content must be monitored. To insure reliability the internal moisture content of the package has to remain below 5000ppm (from 0 to 1000 hrs. minimum).

When eutectic die attach is used, Analog Devices recommends using either a 99.99% gold or a 98% gold, 2% silicon preform.

Recommended eutectic die attach temperature is 410°C ±10°C as measured at the die-substrate interface surface. Time at 410°C shall not exceed 30 seconds.

Lead Bonding: Analog Devices recommends bonding one mil 99.99% gold for gold ball bonding.

Analog Devices recommends ultra-sonic bonding for users requiring aluminum wire. One mil 99% aluminum 1% silicon wire is recommended.

Unless otherwise specified on the device data sheet, there is no required bonding sequence for bipolar chips.

Electrostatic Discharge (ESD): Bipolar integrated circuits are subject to catastrophic damage due to electrostatic charges generated by careless handling.

Furthermore, subtle shifts in transistor characteristics can occur after being subjected to lower amounts of ESD. Precision devices, trimmed to accuracies in the order of ±25 microvolts, can be shifted out of spec due to improper handling.

To preserve the accuracy of precision bipolar integrated circuits, Analog Devices recommends the following:

a. Verify proper grounding of all manufacturing equipment.
b. All workers who handle the chips should be wearing a grounded conductive wrist-strap.
c. All work-in-process, especially any work with incomplete wire-bonding, should be placed on a conductive surface.
d. Dice not in use should be stored in the original waffle pack with anti-static paper.

PACKAGE SEALING RECOMMENDATIONS

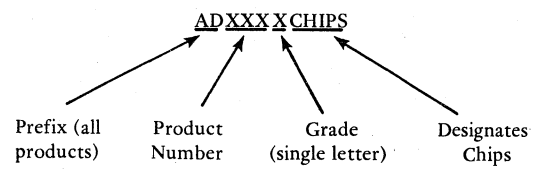
Analog Devices recommends hermetic packaging. The initial precision of trimmed thin-film integrated circuits is retained indefinitely when not subjected to high humidity or corrosive environments.

A maximum sealing temperature of 320°C for a maximum time of 3 minutes is recommended.

The sealing technique must insure that the internal moisture content remain below 5000ppm under all conditions for the life time of the product.

ORDERING INFORMATION

Analog Devices bipolar integrated circuit chips are specified in the same manner as packaged devices, except the package code letter is replaced by the word "CHIPS".



Minimum order quantity is 25 pieces per line item. Analog Devices dice are supplied only in multiples of 25 pieces.

USING DATA SHEETS

Specifications: Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly. The specific recommendations in this General Information Section are intended to assist the user in achieving specified performance of Analog Devices chips in assembled circuits. Electrical specifications are given for each product. *NOTE*: Although the specifications generally conform to those of equivalent grades of packaged product, some differences exist.

AC testing at the chip level is also not practical; therefore, ac specifications are also given as typical.

Applications Information: General applications information is not included on the chip data sheets; this information is provided on the data sheet for the packaged version of each product.

Specific application information that applies to the chip version of each product is given on the chip data sheet.

Metalization Photograph: Metalization photographs are provided for each product. Chip dimensions and pad functions are included.

ADDITIONAL PRODUCT AVAILABILITY INFORMATION

Older Products: The data sheets published in this catalog are intended to assist the user in the design of new hybrid circuits using the highest performance, most cost-effective products available from Analog Devices. There are, however, older IC products that may have been designed into circuits in the past but which are no longer the optimum choice for new designs. These products continue to be available as in the past.

If you are using one of these older Analog Devices IC chips and require technical assistance, please contact the factory. Sales-related information may be obtained from the nearest Analog Devices sales office listed on the back cover.

New Products: Analog Devices is continuously introducing new integrated circuit products. Most of these are monolithic and thus may be supplied in chip form. Although it is our policy to obtain first-hand assembly, testing and application experience with new products before introducing the chip version, we encourage potential users to contact the factory for availability information on new IC products not listed in this catalog.

Low Cost, Laser Trimmed Precision IC Op Amp

AD517 CHIPS

PRODUCT DESCRIPTION

The Analog Devices AD517 operational amplifier is laser-trimmed for ultra-low offset voltages, thus eliminating the need to trim in most applications. Other features include very low offset voltage drift and high gain. Advanced super-beta techniques provide ultra-low input currents. The AD517 is ideal for precision instrumentation applications. Protected input and output circuitry along with internal compensation for gains of one or greater minimize hybrid component count. AD517 chips are available in two grades specified for operation between 0 and +70°C and one grade specified for operation between −55°C and +125°C.

APPLICATION INFORMATION

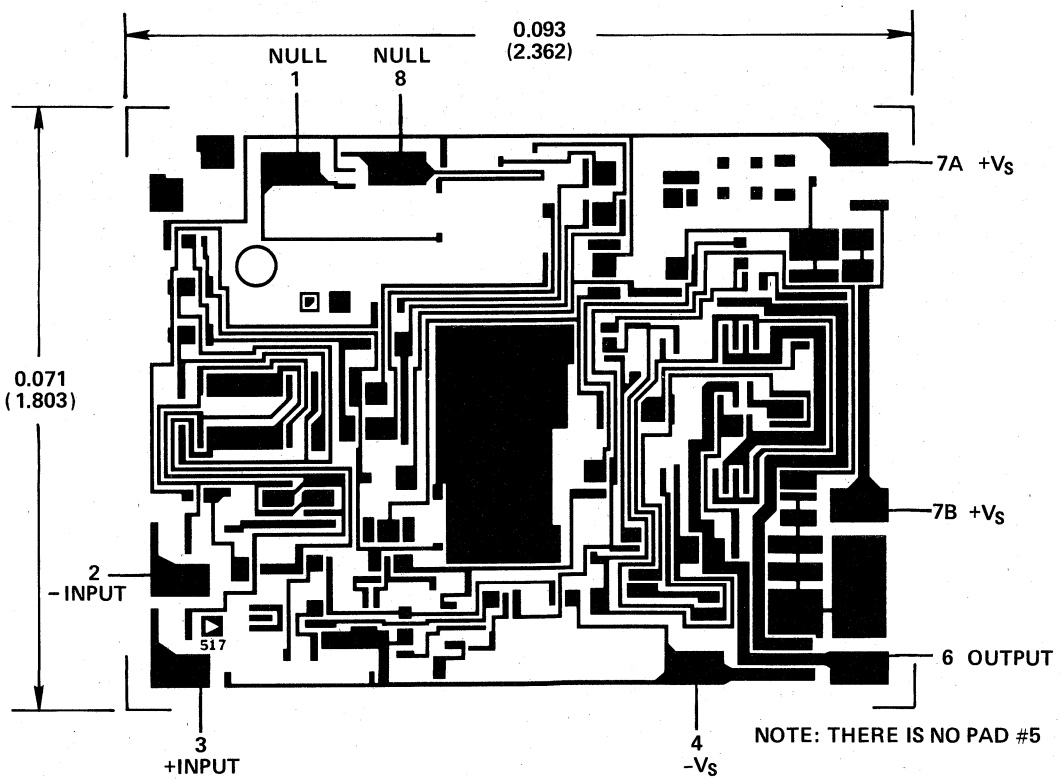
AD517 chips are functionally identical to packaged AD517 devices. For general application information, see the AD517 packaged product catalog data sheet.

The following additional application information applies to AD517 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD517 chip must be connected to $-V_S$, device pad number 4.
4. Pads 7A and 7B must *both* be connected to $+V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS [1] (typical @+25°C and ±15V dc unless otherwise noted)

MODEL	AD517J	AD517K	AD517S
OPEN LOOP GAIN			
V_O = ±10V, $R_L \geq 2k\Omega$	10^6	*	*
T_A = +25°C to T_{max}	500,000 min	*	250,000
T_A = T_{min} to +25°C	500,000	*	250,000
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_{min} to T_{max}	±10V min	*	*
Load Capacitance	1000pF	*	*
Output Current	10mA min	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	250kHz	*	*
Full Power Response	1.5kHz	*	*
Slew Rate, Unity Gain	0.10V/μs	*	*
INPUT OFFSET VOLTAGE			
Initial Offset, $R_S \leq 10k\Omega$	150μV max	75μV max	**
vs. Temp, T_A = +25°C to T_{max}	3.0μV/°C max	1.8μV/°C max	**
T_A = T_{min} to +25°C	3.0μV/°C	1.8μV/°C	**
vs. Supply	25μV/V max	10μV/V max	**
T_A = +25°C to T_{max}	40μV/V max	15μV/V max	20μV/V max
T_A = T_{min} to +25°C	40μV/V	15μV/V	20μV/V
INPUT OFFSET CURRENT			
Initial	1nA max	0.75nA max	**
T_A = +25°C to T_{max}	1.5nA max	1.25nA max	2nA max
T_A = T_{min} to +25°C	1.5nA	1.25nA	2nA
INPUT BIAS CURRENT			
Initial	5nA max	2nA max	**
T_A = +25°C to T_{max}	8nA max	3.5nA max	10nA max
T_A = T_{min} to +25°C	8nA	3.5nA	10nA
vs. Temp, T_{min} to T_{max}	±20pA/°C	±10pA/°C	**
INPUT IMPEDANCE			
Differential	$15M\Omega \| 1.5pF$	$20M\Omega \| 1.5pF$	**
Common Mode	$2.0 \times 10^{11}\ \Omega$	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	2μV p-p	*	*
f = 10Hz	$35nV/\sqrt{Hz}$	*	*
f = 100Hz	$25nV/\sqrt{Hz}$	*	*
f = 1kHz	$20nV/\sqrt{Hz}$	*	*
Current, f = 10Hz	$0.05pA/\sqrt{Hz}$	*	*
f = 100Hz	$0.03pA/\sqrt{Hz}$	*	*
f = 1kHz	$0.03pA/\sqrt{Hz}$	*	*
INPUT VOLTAGE RANGE			
Differential or Common Mode, max safe	$\pm V_S$	*	*
Common Mode Rejection, V_{IN} = ±10V	94dB min	110dB	**
Common Mode Rejection, T_A = +25°C to T_{max}	94dB min	100dB min	**
T_A = T_{min} to +25°C	94dB	100dB	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Current, Quiescent	4mA max	3mA max	**
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested			
(T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES

*Specifications same as AD517J.
**Specifications same as AD517K.
[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, High Speed, IC Op Amp

AD518 CHIPS

PRODUCT DESCRIPTION

The AD518 is a low cost, high speed operational amplifier designed as an improved functional replacement for 118-type devices. It is internally compensated for unity gain, but has the capability of accepting feed-forward compensation for increased slew rate and bandwidth. AD518 chips are available in two grades specified for operation between 0 and +70°C and one grade for operation between -55°C and +125°C.

APPLICATION INFORMATION

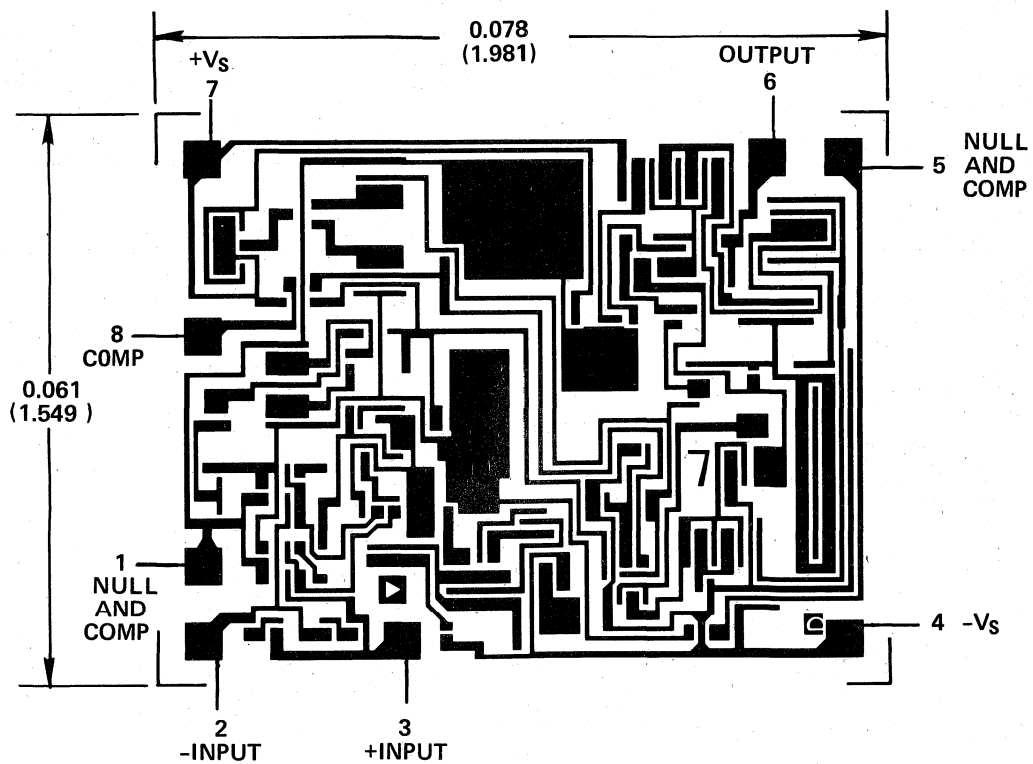
AD518 chips are functionally identical to packaged AD518 devices. For general application information, see the AD518 packaged product catalog data sheet.

The following additional application information applies to AD518 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD518 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

PARAMETER	AD518J	AD518K	AD518S
OPEN LOOP GAIN			
$R_L \geq 2k\Omega$, V_O = ±10V	25,000 min (100,000 typ)	50,000 min (100,000 typ)	**
T_A = +25°C to T_{max}	20,000 min	25,000 min	**
T_A = T_{min} to +25°C	20,000	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L \geq 2k\Omega$, T_A = min to max	±12V min (±13V typ)	*	*
Current @ V_O = ±10V	±10mA	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	12MHz	*	*
Slew Rate, Unity Gain	50V/μs	*	*
Settling Time to 0.1% (Single Capacitor Compensation)	800ns	*	*
Phase Margin, Uncompensated at Unity Gain Crossover Frequency	60°	*	*
INPUT OFFSET VOLTAGE			
Initial, $R_S \leq 10k\Omega$	10mV max (4mV typ)	4mV max (2mV typ)	**
T_A = +25°C to T_{max}	15mV max	6mV max	**
T_A = T_{min} to +25°C	15mV	6mV	**
Avg vs. Temp, T_A = 25°C to T_{max}	10μV/°C	15μV/°C max (5μV/°C typ)	20μV/°C max (10μV/°C typ)
T_A = T_{min} to +25°C	10μV/°C	5μV/°C	*
Avg vs. Supply, T_A = +25°C to T_{max}	65dB min (80dB typ)	80dB min (90dB typ)	**
T_A = T_{min} to +25°C	80dB	90dB	**
INPUT BIAS CURRENT			
Initial	500nA max (120nA typ)	250nA max (120nA typ)	**
T_A = +25°C to T_{max}	750nA max	400nA max	**
T_A = T_{min} to +25°C	750nA	400nA	**
INPUT OFFSET CURRENT			
Initial	200nA max (30nA typ)	50nA max (6nA typ)	**
T_A = +25°C to T_{max}	300nA max	100nA max	**
T_A = T_{min} to +25°C	300nA	100nA	**
INPUT IMPEDANCE			
Differential	0.5MΩ min (3.0MΩ typ)	*	*
INPUT VOLTAGE RANGE†			
Common Mode, max safe	±V_S	*	*
Operating, V_S = ±15V	±11.5V	*	*
Common Mode Rejection Ratio	70dB min (100dB typ)	80dB min (100dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 20)V	*	*
Current, Quiescent	10mA max (5mA typ)	7mA max (5mA typ)	**
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES

†The inputs are shunted with back-to-back diodes; if the differential input may exceed ±1 volt, a resistor should be used to limit the input current to 10mA.

*Specifications same as AD518J.

**Specifications same as AD518K.

Specifications subject to change without notice.

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

ANALOG DEVICES

Precision Instrumentation Amplifier

AD521 CHIPS

PRODUCT DESCRIPTION

The AD521 is a second generation, low cost monolithic instrumentation amplifier. As a true IA, it exhibits high input impedance, balanced differential inputs, low bias currents and high CMR. Gain is programmed for values between 0.1 and 1000 by two external resistors. The AD521 is internally compensated and input and output protected. Two AD521 chip grades are specified for operation between 0 and +70°C while one grade is specified over the -55°C to +125°C range.

APPLICATION INFORMATION

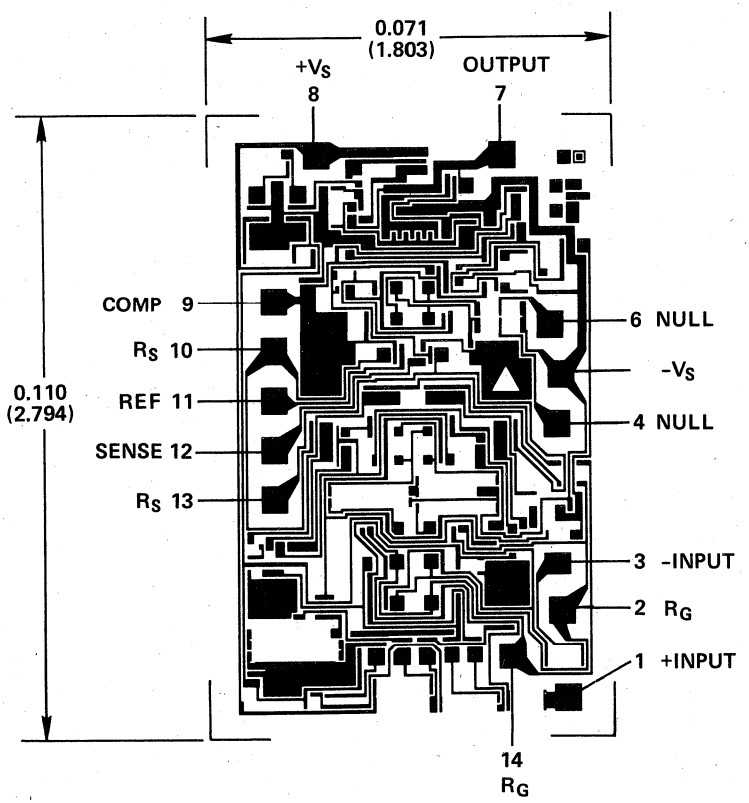
AD521 chips are functionally identical to packaged AD521 devices. For general application information, see the AD521 packaged product catalog data sheet.

The following additional application information applies to AD521 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD521 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14 PIN CERAMIC PACKAGE.

17

SPECIFICATIONS *** (typical @ V_S = ±15V, R_L =2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521J	AD521K	AD521S
GAIN			
Range (For Specified Operation, Note 1)	1 to 1000	*	*
Equation	$G = R_S/R_G$ V/V	*	*
Error from Equation	(±0.25−0.004G)%	*	*
Nonlinearity (Note 2)			
1≤G≤1000	0.2% max	*	*
Gain Temperature Coefficient	±(3 ±0.05G)ppm/°C	*	±(15 ±0.4G)ppm/°C
OUTPUT CHARACTERISTICS			
Rated Output	±10V, ±10mA min	*	*
Output at Maximum Operating Temperature	±10V @ 5mA min	*	*
Impedance	0.1Ω	*	*
DYNAMIC RESPONSE			
Small Signal Bandwidth (±3dB)			
G = 1	>2MHz	*	*
G = 10	300kHz	*	*
G = 100	200kHz	*	*
G = 1000	40kHz	*	*
Small Signal, ±1.0% Flatness			
G = 1	75kHz	*	*
G = 10	26kHz	*	*
G = 100	24kHz	*	*
G = 1000	6kHz	*	*
Full Peak Response (Note 3)	100kHz	*	*
Slew Rate, 1≤G≤1000	10V/μs	*	*
Settling Time (any 10V step to within 10mV of Final Value)			
G = 1	7μs	*	*
G = 10	5μs	*	*
G = 100	10μs	*	*
G = 1000	35μs	*	*
Differential Overload Recovery (±30V Input to within 10mV of Final Value) (Note 4)			
G = 1000	50μs	*	*
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)			
G = 1000	10μs	*	*
VOLTAGE OFFSET (may be nulled)			
Input Offset Voltage (V_{OS_1})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	**
vs. Temperature, T_A = +25°C to T_{max}	15μV/°C max (7μV/°C typ)	5μV/°C max (1.5μV/°C typ)	**
T_A = T_{min} to +25°C	7μV/°C	1.5μV/°C	**
vs. Supply	3μV/%	*	
Output Offset Voltage (V_{OS_0})	400mV max (200mV typ)	200mV max (30mV typ)	**
vs. Temperature, T_A = +25°C to T_{max}	400μV/°C max (150μV/°C typ)	150μV/°C max (50μV/°C typ)	**
T_A = T_{min} to +25°C	150μV/°C	50μV/°C	**
vs. Supply (note 6)	$0.005V_{OS_0}$/%	*	*
INPUT CURRENTS			
Input Bias Current (either input)	80nA max	40nA max	**
vs. Temperature, T_A = +25°C to T_{max}	1nA/°C max	500pA/°C max	**
T_A = T_{min} to +25°C	1nA/°C	500pA/°C	**
vs. Supply	2%/V	*	*
Input Offset Current	20nA max	10nA max	**
vs. Temperature, T_A = +25°C to T_{max}	250pA/°C max	125pA/°C max	**
T_A = T_{min} to +25°C	250pA/°C	125pA/°C	**
INPUT			
Differential Input Impedance (Note 7)	$3 \times 10^9 \Omega \| 1.8pF$	*	*
Common Mode Input Impedance (Note 8)	$6 \times 10^{10} \Omega \| 3.0pF$	*	*
Input Voltage Range for Specified Performance (with respect to ground)	±10V	*	*
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	*	*
Voltage at either input (Note 9)	V_S ±15V	*	*
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance			
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**
G = 100	100dB min (104dB typ)	104dB min (114dB typ)	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**
NOISE			
Voltage RTO (p-p) @ 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.5G)^2 + (225)^2}\ \mu V$	*	*
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (50)^2}\ \mu V$	*	*
Input Current, rms, 10Hz to 10kHz	15pA (rms)	*	*
REFERENCE TERMINAL			
Bias Current	3μA	*	*
Input Resistance	10MΩ	*	*
Voltage Range	±10V	*	*
Gain to Output	1	*	*
POWER SUPPLY			
Operating Voltage Range	±5 to ±18	*	*
Quiescent Supply Current	5mA max	*	
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested			
(T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES

All Numbered Notes Refer to AD521 Packaged Product Catalog Data Sheet in Section 5.

*Specifications same as AD521J.

**Specifications same as AD521K.

***Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

Specifications subject to change without notice.

ANALOG DEVICES

Precision Instrumentation Amplifier

AD524 CHIPS

PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

APPLICATION INFORMATION

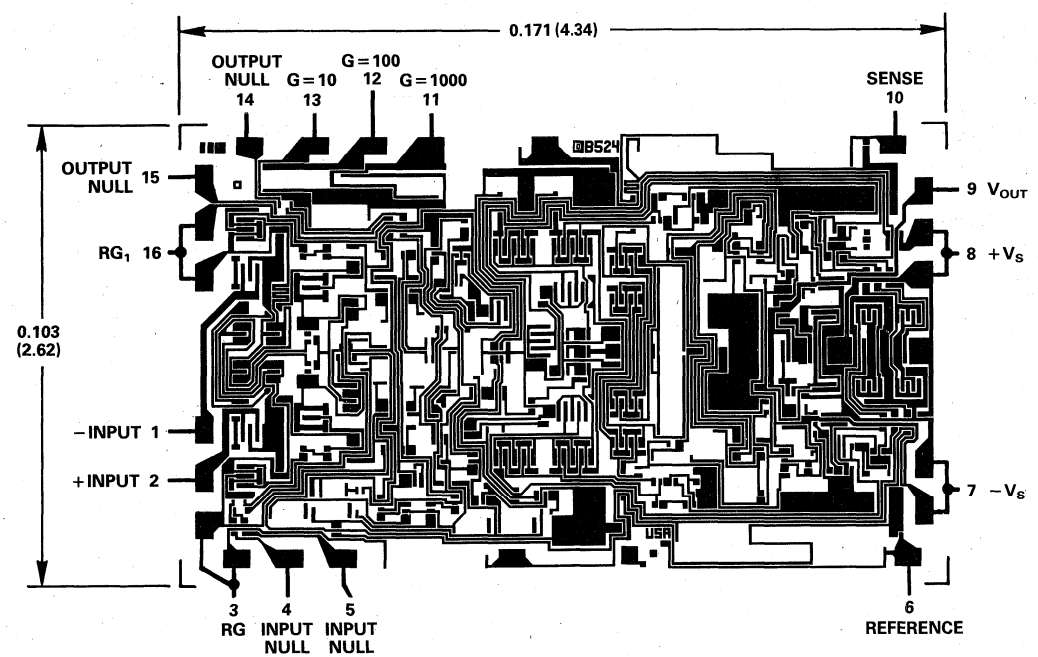
AD524 chips are functionally identical to packaged AD524 devices. For general application information, see the AD524 packaged product catalog data sheet.

The following additional application information applies to AD524 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD524 chip must be connected to $-V_S$, device pad number 7.
4. Do not connect any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D16A 16-PIN CERAMIC PACKAGE.

17

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD524A Min	AD524A Typ	AD524A Max	Units
GAIN				
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]$ ±20%		
Gain Range (Pin Programmable)	1 to 1000			
Gain Error				
G = 1			±0.05	%
G = 10			±0.25	%
G = 100			±0.5	%
G = 1000			±2.0	%
Nonlinearity				
G = 1			±0.01	%
G = 10, 100			±0.01	%
G = 1000			±0.01	%
Gain vs. Temperature				
G = 1			5	ppm/°C
G = 10			15	ppm/°C
G = 100			35	ppm/°C
G = 1000			100	ppm/°C
VOLTAGE OFFSET (May be Nulled)				
Input Offset Voltage			250	µV
vs. Temperature			2	µV/°C
Output Offset Voltage			5	mV
vs. Temperature			100	µV/°C
Offset Referred to the Input vs. Supply				
G = 1	70			dB
G = 10	85			dB
G = 100	95			dB
G = 1000	100			dB
INPUT CURRENT				
Input Bias Current			±150	nA
vs. Temperature		±100		pA/°C
Input Offset Current			±35	nA
vs. Temperature		±100		pA/°C
INPUT				
Input Impedance				
Differential Resistance		10^9		Ω
Differential Capacitance		10		pF
Common Mode Resistance		10^9		Ω
Common Mode Capacitance		10		pF
Input Voltage Range				
Max Differ. Input Linear (V_D)		±10		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance				
G = 1	70			dB
G = 10	90			dB
G = 100	100			dB
G = 1000	110			dB

Model	AD524A Min	AD524A Typ	AD524A Max	Units
OUTPUT RATING				
V_{OUT}, R_L = 2kΩ		±10		V
DYNAMIC RESPONSE				
Small Signal – 3dB				
G = 1		1		MHz
G = 10		400		kHz
G = 100		150		kHz
G = 1000		25		kHz
Slew Rate		5.0		V/µs
Settling Time to 0.01%, 20V Step				
G = 1 to 100		15		µs
G = 1000		75		µs
NOISE				
Voltage Noise, 1kHz				
R.T.I.		7		$nV/\sqrt{Hz}$
R.T.O.		90		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz				
G = 1		15		µV p-p
G = 10		2		µV p-p
G = 100, 1000		0.3		µV p-p
Current Noise				
0.1Hz to 10Hz		60		pA p-p
SENSE INPUT				
R_{IN}		20		kΩ ±20%
I_{IN}		15		µA
Voltage Range	±10			V
Gain to Output		1		
REFERENCE INPUT				
R_{IN}		40		kΩ ±20%
I_{IN}		15		µA
Voltage Range	±10			V
Gain to Output		1		
TEMPERATURE RANGE				
Specified Performance	–25		+85	°C
Storage	–65		+150	°C
POWER SUPPLY				
Power Supply Range	±6	±15	±18	V
Quiescent Current		3.5	5.0	mA

NOTE
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite

ANALOG DEVICES

Trimmed IC Multiplier

AD532 CHIPS

PRODUCT DESCRIPTION

The AD532 is a complete laser-trimmed analog multiplier/divider that performs to specification without any external trims or additional components. In hybrid applications, AD532 chips can eliminate the need to design and operate complicated trim and test equipment while conserving valuable substrate area. As a multiplier, the AD532 operates as a full four-quadrant device; division is performed in two quadrants. AD532 chips are available in two grades specified for 0 to +70°C operation and one grade for -55°C to +125°C.

APPLICATION INFORMATION

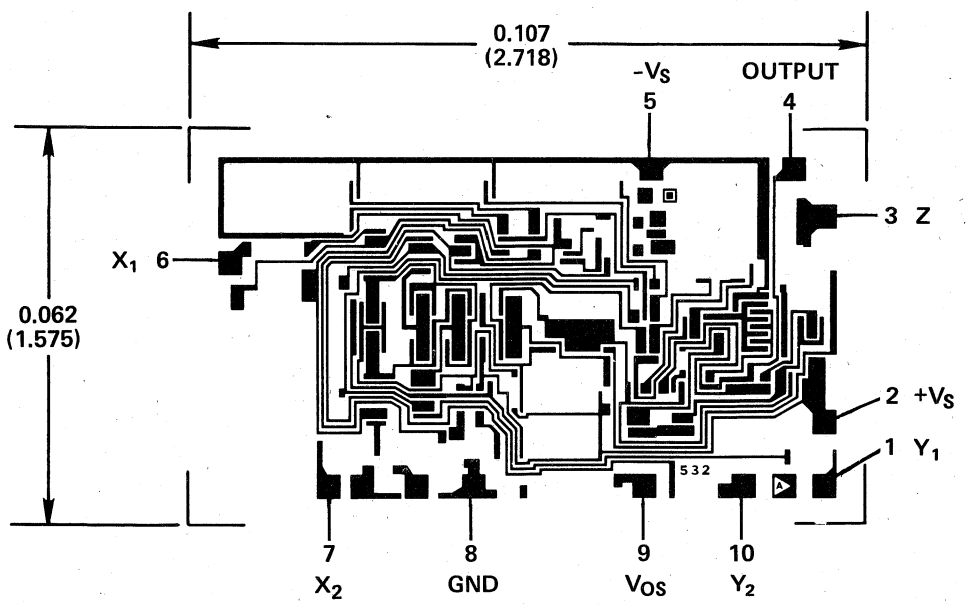
AD532 chips are functionally identical to packaged AD532 devices. For general application information, see the AD532 packaged product catalog data sheet and the Analog Devices "Multiplier Application Guide".

The following additional application information applies to AD532 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD532 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

17

SPECIFICATIONS [1] (typical @ +25°C with V_S = ±15V dc, V_{OS} grounded, unless otherwise specified)

PARAMETER	CONDITIONS	AD532J	AD532K	AD532S
ABSOLUTE MAX RATINGS				
Supply Voltage		±18V	*	±22V
Internal Power Dissipation		500mW	*	*
Input Voltage[2]				
X, Y, V_{OS}, Z		$\pm V_S$	*	*
Output Short Circuit	To Ground	Indefinite	*	*
MULTIPLIER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)(Y_1-Y_2)/10$	*	*
Total Error (% F.S.)	V_X = 0/±10V, V_y = 0/±10V	±2.0% max [±1.5% typ]	±1.0% max [±0.7% typ]	±1.0% max [±0.5% typ]
	T_A = +25°C to T_{max}	±2.5%	±1.5%	±4.0% max
	T_A = T_{min} to +25°C	±2.5%	±1.5%	±4.0%
vs. Temperature	T_A = +25°C to T_{max}	±0.04%/°C	±0.03%/°C	±0.04%/°C max [±0.01%/°C typ]
	T_A = T_{min} to +25°C	±0.04%/°C	±0.03%/°C	±0.01%/°C
Nonlinearity				
X Input	V_X = 20V(p-p), V_y = ±10V	±0.8%	±0.5%	**
Y Input	V_y = 20V(p-p), V_X = ±10V	±0.3%	±0.2%	**
Feedthrough				
X Input	V_X = 20V(p-p), V_y = 0, f = 50Hz	200mV(p-p) max [50mV(p-p) typ]	100mV(p-p) max [30mV(p-p) typ]	**
Y Input	V_y = 20V(p-p), V_X = 0, f = 50Hz	150mV(p-p) max [30mV(p-p) typ]	80mV(p-p) max [25mV(p-p) typ]	**
vs. Temperature	T_A = min to max	2.0mV(p-p)/°C	1.0mV(p-p)/°C	**
DIVIDER SPECIFICATIONS				
Transfer Function		$10Z/(X_1-X_2)$	*	*
Total Error[3]	V_X = −10V, V_Z = ±10V	±2%	±1%	**
	V_X = −1V, V_Z = ±10V	±4%	±3%	**
SQUARER SPECIFICATIONS				
Transfer Function		$(X_1-X_2)^2/10$	*	*
Total Error		±0.8%	±0.4%	**
SQUARE ROOTER SPECIFICATIONS				
Transfer Function		$-\sqrt{10Z}$	*	*
Total Error[3]	V_Z = 0/+10V	±1.5%	±1.0%	**
INPUT SPECIFICATIONS				
Input Resistance				
X, Y Inputs		10MΩ	*	*
Z Input		36kΩ	*	*
Input Bias Current				
X, Y Inputs		3μA	4μA max [1.5μA typ]	**
Z Input		±10μA	±15μA max [±5μA typ]	**
X, Y Inputs	T_A = min to max	10μA	8μA	**
Z Input	T_A = min to max	±30μA	±25μA	**
Input Offset Current				
X, Y Inputs		±0.3μA	±0.1μA	**
Input Voltage Diff/CM	T_A = min to max			
X, Y, Z Inputs	For Rated Accuracy	±10V	*	*
CMRR (X or Y Inputs)	X or Y = ±10V	40dB min	50dB min	**
DYNAMIC SPECIFICATIONS				
Small Signal, Unity Gain		1.0MHz	*	*
Full Power Bandwidth		750kHz	*	*
Slew Rate		45V/μs to 2%	*	*
Small Signal Amplitude Error		1% at 75kHz	*	*
Small Signal 1% Vector Error	0.5° phase shift	5kHz	*	*
Settling Time	±10V step	1μs to 2%	*	*
Overload Recovery		2μs to 2%	*	*
OUTPUT AMPLIFIER SPECIFICATIONS				
Output Impedance	Closed Loop	1Ω	*	*
Output Voltage Swing	T_A = min to max			
	$R_L \geq 2k\Omega$, $C_L \leq 1000pF$	±10V min [±13V typ]	*	*
Output Noise	f = 5Hz to 10kHz	0.6mV(rms)	*	*
	f = 5Hz to 5MHz	3.0mV(rms)	*	*
Output Offset Voltage				
Initial Offset	Trimmable To Zero	±40mV	±30mV max	**
vs. Temperature	T_A = +25°C to T_{max}	0.7mV/°C	*	2.0mV/°C max
	T_A = T_{min} to +25°C	0.7mV/°C	*	*
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±10V to ±18V	*	±10V to ±22V
Supply Current	Quiescent	±6mA max [±4mA typ]	*	*
Power Supply Variation				
Multiplier Accuracy		±0.05%/%	*	*
Output Offset		±2.5mV/%	*	*
Scale Factor		−0.03%/%	*	*
Feedthrough		±0.25mV/%	*	*
TEMPERATURE				
Operating,	tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
	guaranteed, not tested (T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage		−65°C to +150°C	*	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Max input voltage is zero when supplies are turned off.

[3] With recommended external trim (see packaged AD532 data sheet).

*Specifications same as AD532J.

**Specifications same as AD532K.

Specifications subject to change without notice.

ANALOG DEVICES

Trimmed Precision IC Multiplier

AD534 CHIPS

AD535 NOTE:
The AD534 is a functional equivalent to the AD535 divider. Since the AD535 is not available in chip form, AD534 chips are recommended for divider as well as multiplier applications; see the AD535 packaged product data sheet for application recommendations.

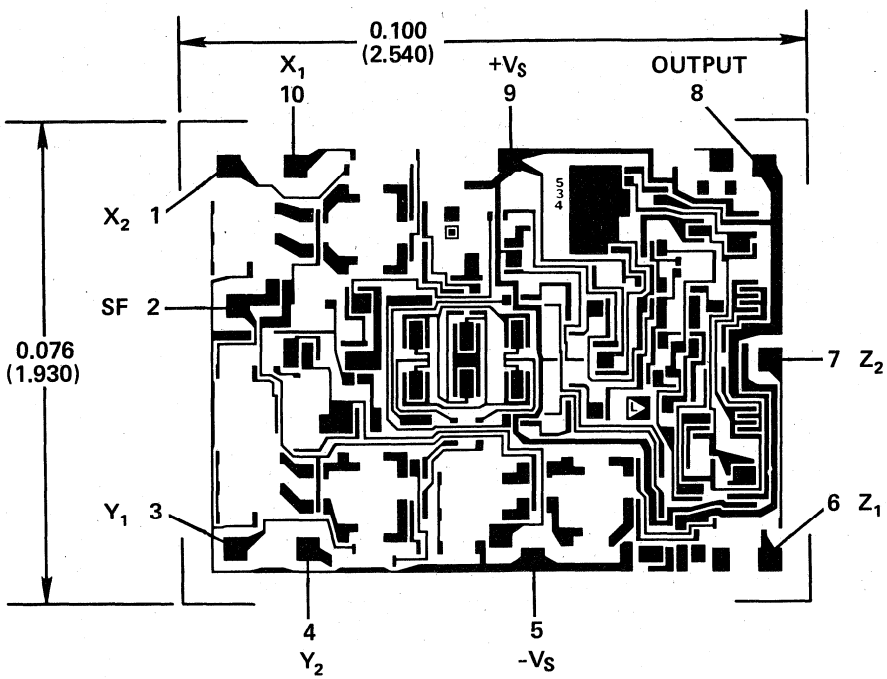
PRODUCT DESCRIPTION
The AD534 is a precision laser-trimmed four-quadrant multiplier/two-quadrant divider that requires no external components to achieve accuracies usually found in expensive assemblies. As a hybrid building-block, AD534 chips can guarantee errors as small as ±0.50%. Differential inputs, internal calibrated reference, output amplifier and a versatile configuration are all features of the AD534. AD534 chips are available in two grades specified for operation between 0 and +70°C and one grade specified for −55°C to +125°C.

APPLICATION INFORMATION
AD534 chips are functionally identical to packaged AD534 and AD535 devices. For general application information, see the AD534 and AD535 packaged product catalog data sheets and the Analog Devices "Multiplier Application Guide."

The following additional application information applies to AD534 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD534 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH
Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical at +25°C, with ±V_S = 15V, $R_L \geq$ 2k, unless otherwise stated)

PARAMETER	CONDITIONS	AD534J	AD534K	AD534S
MULTIPLIER PERFORMANCE				
Transfer Function		$\frac{(X_1 - X_2)(Y_1 - Y_2)}{10} + Z_2$	*	*
Total Error[2]	$-10V \leq X, Y \leq +10V$	±1.0% max	±0.5%	*
	V_S = ±14V to ±16V T_A = +25°C to T_{max}	±1.5%	±1.0%	±2.0% max
	V_S = ±14V to ±16V T_A = T_{min} to +25°C	±1.5%	±1.0%	±2.0%
vs. Temperature	T_A = +25°C to T_{max}	±0.022%/°C	±0.015%/°C	±0.02%/°C max
	T_A = T_{min} to +25°C	±0.022%/°C	±0.015%/°C	±0.02%/°C
Scale Factor Error	SF = 10.00 nominal[3]	±0.25%	±0.1%	*
Temperature-Coefficient of Scaling-Voltage	T_A = min to max	±0.02%/°C	±0.01%/°C	*
Supply Related Error	$\pm V_S$ = (15V) ±1V	±0.01%	*	*
Nonlinearity, X	X = 20V pk-pk Y = ±10V	±0.4%	±0.2% (0.3% max)	*
Nonlinearity, Y	Y = 20V pk-pk X = ±10V	±0.01%	±0.01% (±0.1% max)	*
Feedthrough[4], X	Y nulled X = 20V pk-pk 50Hz	±0.3%	±0.15% (0.3% max)	*
Feedthrough[4], Y	X nulled Y = 20V pk-pk 50Hz	±0.01%	±0.01% (±0.1% max)	*
Output Offset Voltage Drift	T_A = +25°C to T_{min}	±5mV (±30mV max) 200µV/°C	±2mV (±15mV max) 100µV/°C	* 500µV/°C max
	T_A = T_{min} to +25°C	±5mV 200µV/°C	±2mV 100µV/°C	* 500µV/°C
DYNAMICS				
Small-Signal BW	V_{OUT} = 0.1V rms	1MHz	*	*
1% Amplitude Error	C_{LOAD} = 1000pF	50kHz	*	*
Slew Rate	V_{OUT} 20V pk-pk	20V/µs	*	*
Settling Time to ±1%	ΔV_{OUT} = 20V	2µs	*	*
NOISE				
Noise Spectral-Density	SF = 10	$0.8\mu V/\sqrt{Hz}$	*	*
	SF = 3 (Note 5)	$0.4\mu V/\sqrt{Hz}$	*	*
Wideband Noise	f = 10Hz to 5MHz	1mV rms	*	*
	f = 10Hz to 10kHz	90µV rms	*	*
	f = 10Hz to 10kHz, SF = 3 (Note 5)	60µV rms	*	*
OUTPUT				
Output Voltage Swing	T_A = min to max	±11V min	*	*
Output Impedance	Unity-Gain, f ≤ 1kHz	0.1Ω	*	*
Amplifier Open-Loop Gain	f = 50Hz	70dB	*	*
Maximum Output Current	R_L = 0, T_A = min to max	30mA	*	*
INPUT AMPLIFIERS (X, Y and Z)[6]				
Signal Voltage Range	Rated Accuracy (Diff. or CMR)	±10V	*	*
	Operating (Diff.)	±12V	*	*
Offset Voltage, X, Y	T_A = T_{min} to T_{max}	±5mV (±20mV max)	±2mV (±10mV max)	*
Drift		100µV/°C	50µV/°C	*
Offset Voltage, Z	T_A = +25°C to T_{max}	±5mV (±30mV max) 200µV/°C	±2mV (±15mV max) 100µV/°C	* 500µV/°C max
Drift	T_A = T_{min} to +25°C	±5mV 200µV/°C	±2mV 100µV/°C	* 500µV/°C
CMRR (X, Y, Z)	50Hz, 20V pk-pk	80dB (60dB min)	90dB (70dB min)	*
Bias Current	Diff. Input = 0	0.8µA (2µA max)	*	*
Offset Current	Diff. Input = 0	0.1µA	*	*
Differential Resistance		10MΩ	*	*
DIVIDER PERFORMANCE				
Transfer Function	$X_1 > X_2$	$10\frac{(Z_2 - Z_1)}{(X_1 - X_2)} + Y_1$	*	*
Total Error[2]	X = 10V $-10V \leq Z \leq +10V$	±0.75%	±0.35%	*
	X = 1V $-1V \leq Z \leq +1V$	±2.0%	±1.0%	*
	0.1V ≤ X ≤ 10V $-10V \leq Z \leq +10V$	±2.5%	±1.0%	*
SQUARER PERFORMANCE				
Transfer Function		$\frac{(X_1 - X_2)^2}{10} + Z_2$	*	*
Total Error[2]	$-10V \leq X \leq +10V$	±0.6%	±0.3%	*
SQUARE-ROOTER PERFORMANCE				
Transfer Function	$Z_1 \leq Z_2$	$\sqrt{10(Z_2 - Z_1)} + X_2$	*	*
Total Error[1]	1V ≤ Z ≤ 10V	±1.0%	±0.5%	*
POWER SUPPLY SPECIFICATIONS				
Supply Voltage	Rated Performance	±15V	*	*
	Operating	±8V to ±18V	*	±8V to ±22V
Supply Current	Quiescent	4mA (6mA max)	*	*
TEMPERATURE				
Operating, tested	(T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
guaranteed, not tested	(T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage		−65°C to +150°C	*	*
ABSOLUTE MAXIMUM RATINGS				
Internal Power Dissipation		500mW	*	*
Supply Voltage		±15V	*	±22V
Output Short-Circuit to Ground		Indefinite	*	*
Input Voltages, X_1, X_2, Y_1, Y_2, Z_1, Z_2		$\pm V_S$	*	*

NOTES
*Same as AD534J specs.
[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.
[2] Figures given are percent of full-scale, ±10V (i.e., 0.01% = 1mV).
[3] May be reduced to 3V using external resistor between $-V_S$ and SF.
[4] Irreducible component due to nonlinearity; excludes effect of offsets.
[5] Using external resistor adjusted to give SF = 3.
[6] See Functional Block Diagram, Figure 1 of packaged AD534 data sheet for definition of sections.
[7] With external Z-offset adjustment, Z ≤ ±X.

Specifications subject to change without notice.

ANALOG DEVICES

IC True rms-to-dc Converter

AD536A CHIPS

PRODUCT DESCRIPTION

The AD536A is a complete true rms-to-dc converter. As a single-chip IC, it is ideally suited to hybrid circuits as it requires only one external capacitor for operation. Features include factory calibration by laser trimming, dB output with 60dB range, low power (1mA) single or dual supply operation, wide bandwidth and 1% errors at crest factors of 7. One grade of the AD536A chip is specified for operation between 0 and +70°C, one grade for -55°C to +125°C.

APPLICATION INFORMATION

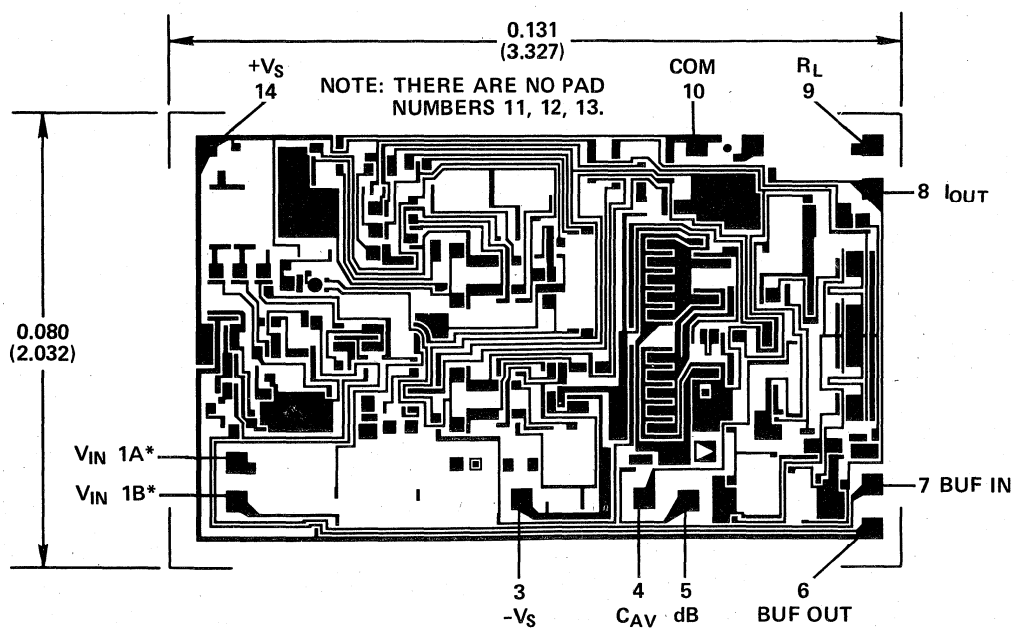
The AD536A chips are functionally identical to packaged AD536A devices. For general application information, see the AD536A packaged product catalog data sheet.

The following additional application information applies to AD536A chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD536A chip must be connected to $-V_S$, device pad number 3.
4. Pads 1A and 1B must *both* be connected to V_{IN}.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-116 14 PIN CERAMIC DIP PACKAGE.

NOTE:
*BOTH PADS SHOWN MUST BE CONNECTED TO V_{IN}.

17

SPECIFICATIONS[1] (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	AD536AJ	AD536AS
TRANSFER EQUATION	$V_{OUT} = \sqrt{avg.\ (V_{IN})^3}$	*
CONVERSION ACCURACY		
Total Error, Internal Trim[2] (Fig. 1)†	±5mV ±0.5% of Reading, max	*
vs. Temperature, T_A = +25°C to +70°C	±(0.1mV ±0.01% Reading)/°C, max	±(0.1mV ±0.005% Reading)/°C, max
T_A = +70°C to +125°C	—	±(0.3mV ±0.005% Reading)/°C, max
$T_A = T_{min}$ to +25°C	±(0.1mV ±0.01% Reading)/°C,	±(0.1mV ±0.005% Reading)/°C
vs. Supply Voltage	±(0.1mV ±0.01% Reading)/V	*
dc Reversal Error	±0.05% of Reading	*
Total Error, External Trim[2] (Fig. 2)†	±3mV ±0.3% of Reading	*
ERROR vs CREST FACTOR[3]		
Crest Factor 1 to 2	Specified Accuracy	*
Crest Factor = 3	−0.1% of Reading	*
Crest Factor = 7	−1% of Reading	*
FREQUENCY RESPONSE[4]		
Bandwidth for 1% additional error (0.1dB)		
$10mV < V_{IN} \leq 100mV$	6kHz	*
$100mV < V_{IN} \leq 1V$	40kHz	*
$1V < V_{IN} \leq 7V$	100kHz	*
±3dB Bandwidth		
$10mV < V_{IN} \leq 100mV$	50kHz	*
$100mV < V_{IN} \leq 1V$	300kHz	*
$1V < V_{IN} \leq 7V$	2MHz	*
AVERAGING TIME CONSTANT (Fig. 5)†	25ms/μF C_{AV}	*
INPUT CHARACTERISTICS		
Signal Range, ±15V Supply	±20V Peak	*
Signal Range, +5V Supply (Fig. 17)†	±5V Peak	*
Safe Input, All Supply Voltages	±25V max	*
Input Resistance	16.7kΩ ±25%	*
Input Offset Voltage	±2mV max	*
OUTPUT CHARACTERISTICS		
Offset Voltage	±2mV max	*
vs. Temperature, T_A = +25°C to T_{max}	±0.1mV/°C	±0.2mV/°C, max
$T_A = T_{min}$ to +25°C	±0.1mV/°C	±0.2mV/°C
vs. Supply Voltage	±0.1mV/V	±0.2mV/V max
Voltage Swing, ±15V Supplies	0 to +10V min	*
±5V Supply	0 to +2V min	*
Output Current	(+5mA, −130μA) min	*
Short Circuit Current	+20mA	*
Resistance	0.5Ω max	*
dB OUTPUT (Fig. 13)†		
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms	±0.5dB	*
Scale Factor	−3mV/dB	*
Scale Factor TC (Uncompensated, see Fig. 13† for Temperature Compensation)	−0.3% Reading/°C (−0.03dB/°C)	*
I_{REF} for 0dB = 1V rms	20μA (5μA min, 80μA max)	*
I_{REF} Range	1μA to 100μA	*
I_{OUT} TERMINAL		
I_{OUT} Scale Factor	40μA/Volt rms	*
I_{OUT} Scale Factor Tolerance	±25%	*
Output Resistance	10^8Ω	*
Voltage Compliance	$-V_S$ to $(+V_S - 2.5V)$	*
BUFFER AMPLIFIER		
Input and Output Voltage Range	$-V_S$ to $(+V_S - 2.5V)$min	*
Input Offset Voltage, R_S = 25k	±4mV max	*
Input Current	100nA typ, 300nA max	*
Input Resistance	10^8Ω	*
Output Current	(5mA, −130μA) min	*
Short Circuit Current	+20mA	*
Small Signal Bandwidth	1MHz	*
Slew Rate[5]	5V/μs	*
POWER SUPPLY		
Voltage, Rated Performance		
Dual Supply	±3.0V to ±18V	*
Single Supply	+5V to +36V	*
Quiescent Current		
Total V_S, 5V to 36V, T_{min} to T_{max}	2mA max (1mA typ)	*
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested		
($T_A = T_{min}$ to +25°C)	0 to +25°C	−55°C to +25°C
Storage	−55°C to +150°C	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in Figure 1.

[3] Error vs. crest factor is specified for 1V rms rectangular pulse input, pulse width - 200μs.

[4] Input voltages are expressed in volts rms.

[5] With 2K external puildown resistor.

†Figure references refer to figures on AD536A packaged product catalog data sheet in Section 6.

*Specifications same as AD536AJ.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost IC V-to-F Converter

AD537 CHIPS

PRODUCT DESCRIPTION

The AD537 is a V to F converter consisting of an input amplifier, precision oscillator, accurate voltage reference and a high current output stage. Only a single external RC network is required to set up any full scale frequency up to 100kHz and any full scale input voltage up to ±30V. AD537 chips feature a precision reference output, low quiescent current (1.2mA), high linearity and excellent stability. The device operates from single or dual supplies from 4.5 to 36 volts. The AD537 chip is specified for 0 to +70°C operation.

APPLICATION INFORMATION

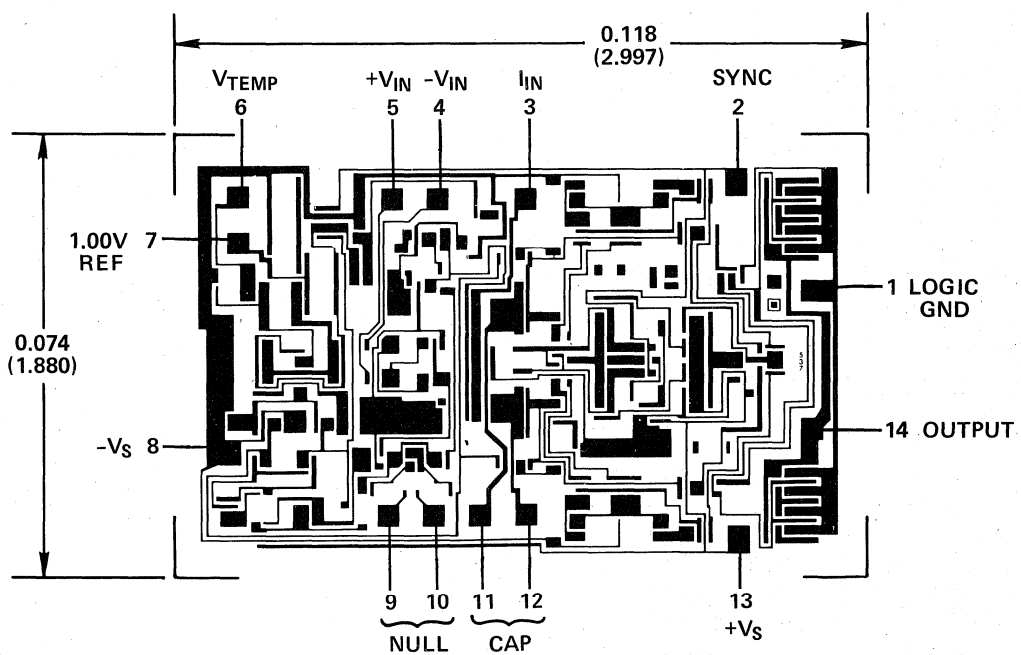
AD537 chips are functionally identical to dual-in-line packaged AD537 devices. For general application information, see the AD537 packaged product catalog data sheet.

The following additional application information applies to AD537 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD537 chip must be connected to $-V_S$, device pad number 8.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 14 PIN CERAMIC PACKAGE.

17

SPECIFICATIONS [1] (typical @ +25°C with V_S (total) = 5 to 36V, unless otherwise noted)

MODEL	AD537J
ANALOG INPUT AMPLIFIER	
(Voltage-to-Current Converter)	
Voltage Input Range	
Single Supply	0 to ($+V_S$ - 4) Volts (min)
Dual Supply	$-V_S$ to ($+V_S$ - 4) Volts (min)
Input Bias Current	
(Either Input)	100nA
Input Resistance (Non-Inverting)	250MΩ
Input Offset Voltage	
(Trimmable to Zero)	5mV max
vs. Supply	100μV/V max
vs. Temp, $T_A = T_{min}$ to T_{max}	5μV/°C
Safe Input Voltage [2]	$\pm V_S$
CURRENT-TO-FREQUENCY CONVERTER	
Frequency Range	0 to 150kHz
Nonlinearity [3]	
f_{max} = 10kHz	0.1%
f_{max} = 100kHz	0.15%
Full Scale Calibration Error	
C = 0.0100μF, I_{IN} = 1.000mA	±7% max
vs. Supply, ($f_{max} < 100$kHz)	±0.1%/V max (0.01% typ)
vs. Temp, $T_A = T_{min}$ to T_{max}	50ppm typ
REFERENCE OUTPUTS	
Voltage Reference	
Absolute Value	1.00 Volt ±5% max
vs. Temp, $T_A = T_{min}$ to T_{max}	50ppm/°C
vs. Supply	±0.03%/V max
Output Resistance [4]	380Ω
Absolute Temperature Reference	
Nominal Output Level	1.00mV/°K
Initial Calibration @ +25°C	298mV ±5mV typ
Slope Error from 1.00mV/°K	±0.02mV/°K
Slope Nonlinearity	±0.1°K
Output Resistance [4]	900Ω
OUTPUT INTERFACE (Open Collector Output)	
(Symmetrical Square Wave)	
Output Sink Current in Logic "0"	
(V_{OUT} = 0.4V max, T_{min} to T_{max})	20mA min
Output Leakage Current in Logic "1"	
(T_{min} to T_{max})	200nA max
Logic Common Level Range	$-V_S$ to ($+V_S$ - 4) Volts
Rise/Fall Times (C_T = 0.01μF)	
I_{IN} = 1mA	0.2μs
I_{IN} = 1μA	1μs
POWER SUPPLY	
Voltage, Rated Performance	
Single Supply	4.5 to 36V
Dual Supply	±5 to ±18V
Quiescent Current	1.2mA
TEMPERATURE RANGE	
Operating	
Tested (T_A = +25°C to T_{max})	+25°C to +70°C
Guaranteed, Not Tested	
($T_A = T_{min}$ to +25°C)	0 to +25°C
Storage	-65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Maximum voltage input level is equal to the supply on either input terminal. However, large negative voltage levels can be sensed at the negative terminal if the input is scaled to a nominal 1mA full scale through an appropriate value resistor.

[3] Nonlinearity is specified for a current input level (I_{IN}) to the converter from 0.1 to 1000μA. Converter has 100% overrange capability up to I_{IN} = 2000μA with slightly reduced linearity. Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a percentage of full scale.

[4] Loading the 1.0 volt or 1mV/°K outputs can cause a significant change in overall circuit performance, as indicated in the applications section of the packaged AD537 catalog data sheet. To maintain normal operation, these outputs should be operated into the internal buffer or an external amplifier.

Specifications subject to change without notice.

ANALOG DEVICES

High Accuracy Low Cost FET-Input Op Amp

AD540 CHIPS

PRODUCT DESCRIPTION

The AD540 is a low cost, high accuracy FET input operational amplifier. The low maximum bias current of 25pA (K-grade) is specified warmed up. The device is latch-up proof and short circuit protected. It is internally compensated for gains of one or greater. Two grades of AD540 chips are specified for operation over the 0 to +70°C temperature range and one grade is specified for operation between -55°C and +125°C.

APPLICATION INFORMATION

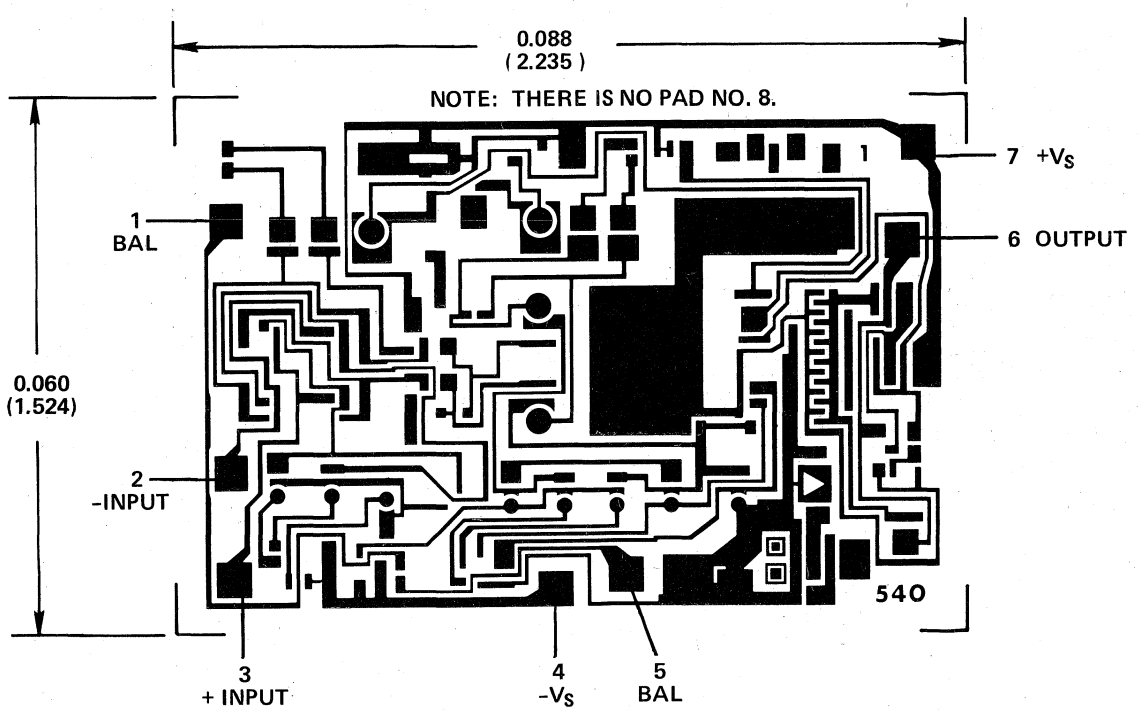
AD540 chips are functionally identical to packaged AD540 devices. For general application information, see the AD540 packaged product catalog data sheet.

The following additional application information applies to AD540 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD540 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

17

SPECIFICATIONS [1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN[2]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min	50,000	**
T_A = +25°C to T_{max}	15,000 min	25,000 min	**
T_{min} to +25°C	15,000	25,000	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	50mV max	20mV max	**
vs. Temp, T_A = +25°C to T_{max}	75μV/°C max	25μV/°C max	50μV/°C max
T_A = T_{min} to +25°C	75μV/°C	25μV/°C	50μV/°C
vs. Supply, T_A = +25°C to T_{max}	400μV/V max	300μV/V max	**
T_A = T_{min} to +25°C	400μV/V	300μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested			
(T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD540J

**Specifications same as AD540K.

Specifications subject to change without notice.

ANALOG DEVICES

Precision Low Cost BIFET Op Amp

AD542 CHIPS

PRODUCT DESCRIPTION

The AD542 is a precision FET-input operational amplifier fabricated with the most advanced BIFET and laser-trimming technologies. Bias currents as low as 25pA max, warmed-up, and offset voltages as low as 1.0mV max and offset voltage drifts as low as 10μV/°C max make the AD542 ideal for precision instrumentation applications. This precision is gained without sacrificing the low cost, high-speed features of other BIFET amplifiers. Two grades of AD542 chips are specified for operation between 0 and +70°C and one grade is specified for the −55°C to +125°C temperature range.

APPLICATION INFORMATION

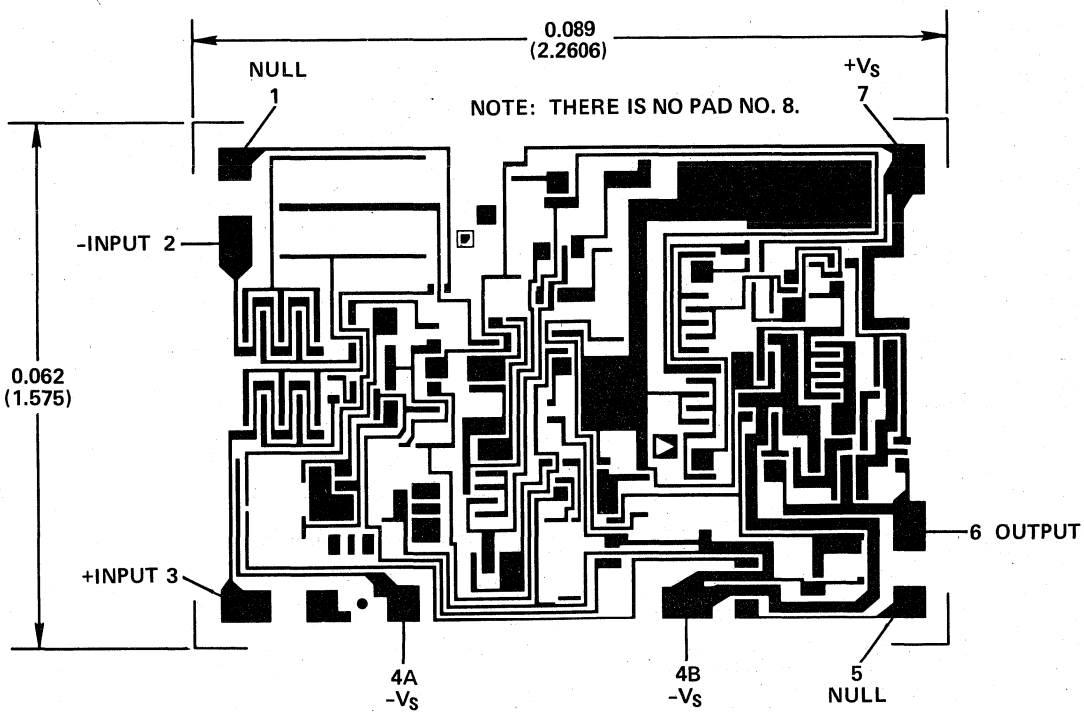
AD542 chips are functionally identical to packaged AD542 devices. For general application information, see the AD542 packaged product catalog data sheet.

The following additional application information applies to AD542 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD542 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD542J	AD542K	AD542S
OPEN LOOP GAIN[2]			
V_{out} = ±10V, $R_L \geq 2k\Omega$	100,000 min	300,000 min	**
T_A = +25°C to T_{max}	100,000 min	300,000 min	**
T_A = T_{min} to +25°C	100,000	300,000	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = T_{min} to T_{max}	±10V min (±12V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = T_{min} to T_{max}	±12V min (±13V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	50kHz	*	*
Slew Rate, Unity Gain	3.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	**
vs. Temp, T_A = +25°C to T_{max}	20μV/°C max	10μV/°C max	15μV/°C max
T_A = T_{min} to +25°C	20μV/°C	10μV/°C	15μV/°C
vs. Supply, T_A = +25°C to T_{max}	200μV/V max	100μV/V max	**
T_A = T_{min} to +25°C	200μV/V	100μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
Input Offset Current	5pA	2pA	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	76dB min	80dB min	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	1.5mA max	*	*
VOLTAGE NOISE			
0.1-10Hz	2μV p-p	*	*
10Hz	$70nV/\sqrt{Hz}$	*	*
100Hz	$45nV/\sqrt{Hz}$	*	*
1kHz	$30nV/\sqrt{Hz}$	*	*
10kHz	$25nV/\sqrt{Hz}$	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested			
(T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD542J.

**Specifications same as AD542K.

Specifications subject to change without notice.

ANALOG DEVICES

Precision High Speed BIFET Op Amp

AD544 CHIPS

PRODUCT DESCRIPTION

The AD544 is a precision, high speed, FET-input operational amplifier fabricated with the most advanced BIFET and laser-trimming technologies. Bias currents as low as 25pA max, warmed-up, offset voltages as low as 1.0mV max and offset voltage drifts as low as 10μV/°C max and fast settling time of 3μs to ±0.01% make the AD544 ideal for use as a precision output amplifier for digital to analog converters. Two grades of AD544 chips are specified for operation between 0 and +70°C and one grade is specified for the -55°C to +125°C temperature range.

APPLICATION INFORMATION

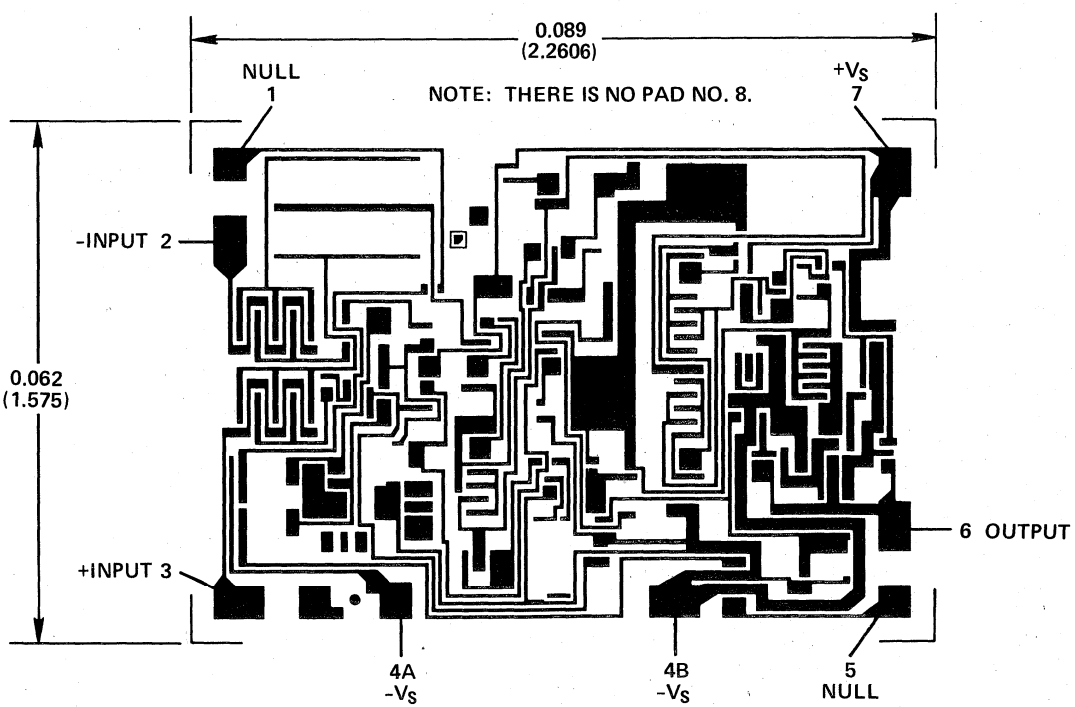
AD544 chips are functionally identical to packaged AD544 devices. For general application information, see the AD544 packaged product catalog data sheet.

The following additional application information applies to AD544 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD544 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD544J	AD544K	AD544S
OPEN LOOP GAIN[2]			
V_{out} = ±10V, $R_L \geq 2k\Omega$	30,000 min	50,000 min	**
T_A = +25°C to T_{max}	20,000 min	40,000 min	**
T_A = T_{min} to +25°C	20,000	40,000	**
OUTPUT CHARACTERISTICS			
Voltage @ $R_L = 2k\Omega$, $T_A = T_{min}$ to T_{max}	±10V min (±12V typ)	*	*
Voltage @ $R_L = 10k\Omega$, $T_A = T_{min}$ to T_{max}	±12V min (±13V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	2.0MHz	*	*
Full Power Response	200kHz	*	*
Slew Rate, Unity Gain	13.0V/μs	*	*
INPUT OFFSET VOLTAGE[3]	2.0mV max	1.0mV max	**
vs. Temp, T_A = +25°C to T_{max}	20μV/°C max	10μV/°C max	15μV/°C max
T_A = T_{min} to +25°C	20μV/°C	10μV/°C	15μV/°C
vs. Supply, T_A = +25°C to T_{max}	200μV/V max	100μV/V max	**
T_A = T_{min} to +25°C	200μV/V	100μV/V	**
INPUT BIAS CURRENT			
Either Input[4]	50pA max	25pA max	**
Input Offset Current	5pA	2pA	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	74dB min	80dB min	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	2.5mA max (1.8mA typ)	*	*
VOLTAGE NOISE			
0.1-10Hz	2μV p-p	*	*
10Hz	$35nV/\sqrt{Hz}$	*	*
100Hz	$22nV/\sqrt{Hz}$	*	*
1kHz	$18nV/\sqrt{Hz}$	*	*
10kHz	$16nV/\sqrt{Hz}$	*	*
TEMPERATURE RANGE			
Operating			
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	*	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	*	−55°C to +25°C
Storage	−65°C to +150°C	*	*

NOTES
[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.
[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.
[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

*Specifications same as AD544J.
**Specifications same as AD544K.
Specifications subject to change without notice.

Ultra Low Drift BIFET Operational Amplifier

AD547 CHIPS

PRODUCT DESCRIPTION

The AD547 is a monolithic, FET input operational amplifier combining the very low input bias current advantages of a BIFET op amp with offset and drift performance previously available only in high quality bipolar amplifiers.

The exclusive Analog Devices laser wafer trim process trims both the input offset voltage and offset voltage drift to levels far lower than any competing BIFET amplifier (1mV, 5μV/°C).

In addition to superior low drift performance, the AD547 offers the lowest guaranteed input bias currents of any BIFET amplifier (50pA max warmed-up).

APPLICATION INFORMATION

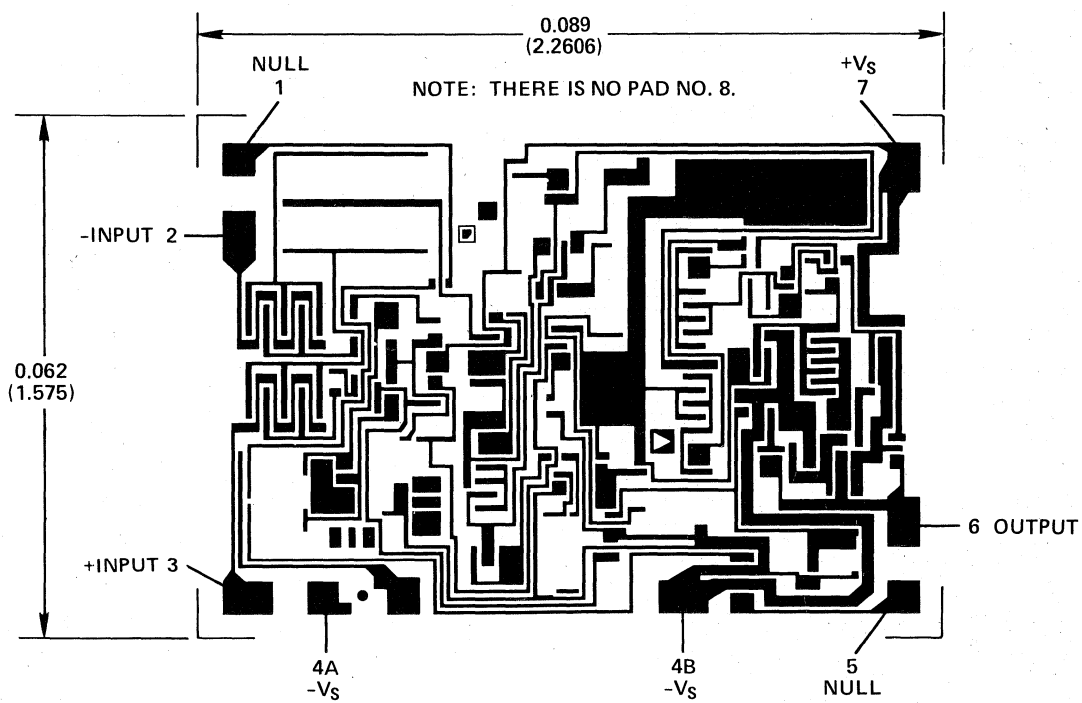
AD547 chips are functionally identical to packaged AD547 devices. For general application information, see the AD547 packaged product catalog data sheet.

The following additional application information applies to AD547 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD547 chip must be connected to $-V_S$, device pad numbers 4A and 4B.
4. Pads 4A and 4B must *both* be connected to $-V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8 PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD547J
OPEN LOOP GAIN[2]	
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	100,000 min
T_A = +25°C to T_{max}	100,000 min
T_A = T_{min} to +25°C	100,000
OUTPUT CHARACTERISTICS	
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±12V typ)
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±13V typ)
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.0MHz
Full Power Response	50kHz
Slew Rate, Unity Gain	3.0V/μs
INPUT OFFSET VOLTAGE[3]	1.0mV max
vs. Temperature, T_A = +25°C to T_{max}	5μV/°C max
T_A = T_{min} to +25°C	5μV/°C
vs. Supply, T_A = +25°C to T_{max}	200μV/V max
T_A = T_{min} to +25°C	200μV/V
INPUT BIAS CURRENT	
Either Input[4]	10pA (50pA max)
Input Offset Current	5pA
INPUT IMPEDANCE	
Differential	$10^{12}\Omega \| 6pF$
Common Mode	$10^{12}\Omega \| 6pF$
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±10V min (±12V typ)
Common Mode Rejection, V_{in} = ±10V	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	1.5mA max (1.1mA typ)
VOLTAGE NOISE	
0.1-10Hz	2μV p-p typ
10Hz	$70nV/\sqrt{Hz}$
100Hz	$45nV/\sqrt{Hz}$
1kHz	$30nV/\sqrt{Hz}$
10kHz	$25nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Tested (T_A = +25°C to T_{max})	+25°C to +70°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C
Storage	−65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Open Loop Gain is specified with V_{OS} both nulled and unnulled.

[3] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[4] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from around.

Specifications subject to change without notice.

ANALOG DEVICES

DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

AD558 CHIPS

PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range, while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558J is specified for use over the 0 to +70°C temperature range and the AD558T is specified for the −55°C to +125°C range.

APPLICATION INFORMATION

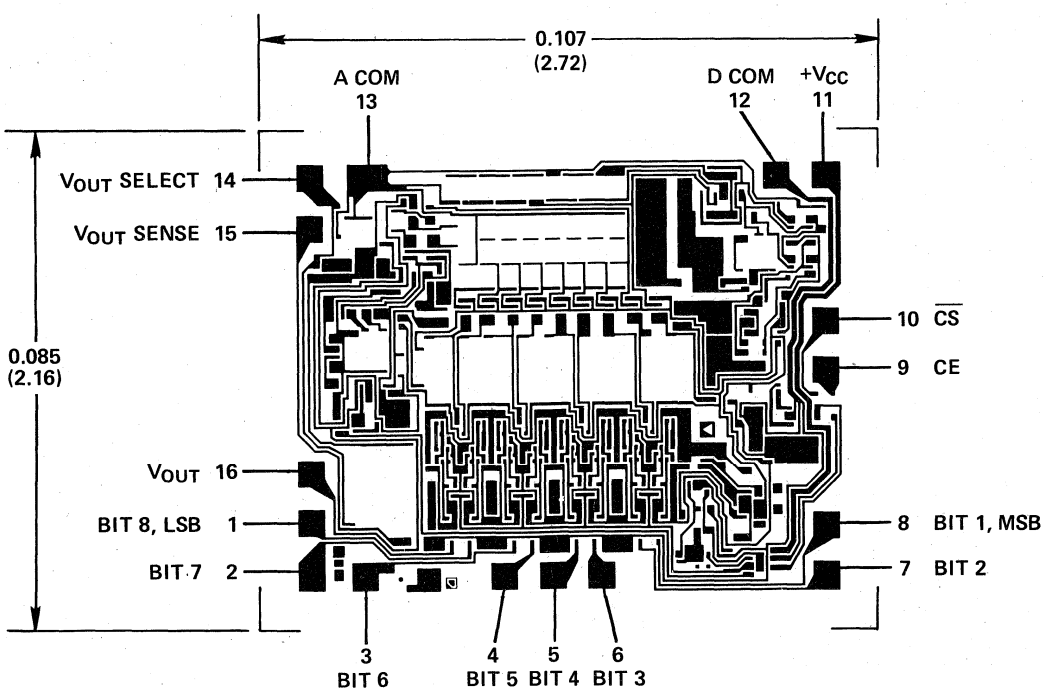
AD558 chips are functionally identical to packaged AD558 devices. For general application information, see the AD558 packaged product catalog data sheet.

The following additional application information applies to AD558 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD558 chip must be connected to analog ground, device pad number 13.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



DACPORT is a registered trademark of Analog Devices, Inc.

SPECIFICATIONS[1] (typical @ +25°C, V_{CC} = +5V to +15V unless otherwise specified)

MODEL	AD558J	AD558T
RESOLUTION	8 Bits	*
RELATIVE ACCURACY[2]		
$T_A = T_{min}$ to T_{max}	±1/2LSB max	±3/8LSB max
OUTPUT		
Ranges	0V to +2.56V	*
	0V to +10V[3]	*
Current, Source	+5mA	+5mA min
Sink	Internal Passive Pull-Down to Ground[4]	*
OUTPUT SETTLING TIME[5]		
0 to 2.56 volt range	0.8μs	*
0 to 10 volt range[3]	2.0μs	*
FULL SCALE ACCURACY		
@ 25°C	±1.5LSB (±0.6%) max	*
$T_A = +25°C$ to T_{max}	±2.5LSB (±1.0%) max	*
$T_A = T_{min}$ to +25°C	±2.5LSB (±1.0%)	*
ZERO ERROR		
@ 25°C	±1LSB max	*
$T_A = +25°C$ to T_{max}	±2LSB max	*
$T_A = T_{min}$ to +25°C	±2LSB	*
MONOTONICITY[6]	Guaranteed, $T_A = +25°C$ to T_{max}	*
	Typical, $T_A = T_{min}$ to +25°C	*
DIGITAL INPUTS		
T_{min} to T_{max}		
Input Current	±100μA max	*
Data Inputs, Voltage		
Bit On – Logic "1"	2.0V min	*
Bit Off – Logic "0"	0.8V max	*
Control Inputs, Voltage		
On – Logic "1"	2.0V min	*
Off – Logic "0"	0.8V max	*
Input Capacitance	4pF	*
TIMING		
T_{min} to T_{max}		
t_W (Strobe Pulse Width)	100ns min	*
t_{DH} (Data Hold Time)	10ns max	*
t_{DS} (Data Set-Up Time)	100ns min	*
POWER SUPPLY		
Operating Voltage Range (V_{CC})		
2.56 Volt Range	+4.5V to +16.5V	*
10 Volt Range	+11.4V to +16.5V	*
Current (I_{CC})	15mA typ, 25mA max	*
Rejection Ratio	0.03%/% max	*
POWER DISSIPATION, V_{CC} = 5V	75mW (125mW max)	*
V_{CC} = 15V	225mW (375mW max)	*
TEMPERATURE RANGE		
Operating		
Tested ($T_A = +25°C$ to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested ($T_A = T_{min}$ to +25°C)	0 to +25°C	−55°C to +25°C
Storage	−65°C to +150°C	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative Accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Operation of the 0 to 10 volt output range requires a minimum supply voltage of +11.4 volts.

[4] Passive pull-down resistance is 2kΩ for 2.56 volt range, 10kΩ for 10 volt range.

[5] Settling time is specified for a positive-going full-scale step to ±1/2LSB. Negative-going steps to zero are slower, but can be improved with an external pull-down.

[6] A monotonic converter has a maximum differential linearity error of ±1LSB.

*Specifications same as AD558J.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, High Speed 10-Bit D-to-A Converter with Reference

AD561 CHIPS

PRODUCT DESCRIPTION

The AD561 is a low-cost, high-speed complete current output D to A converter. An on-chip buried zener reference, laser-wafer-trimmed resistors, high-speed switches and control amplifier make the AD561 chip ideal for adjustment-free 10-bit hybrid applications. Monotonicity to 10 bits (guaranteed +25°C to T_{max}) along with a 250ns settling time are among the performance features of the AD561. One grade of the AD561 chip is specified for 0 to +70°C operation and one is specified for -55°C to +125°C.

APPLICATION INFORMATION

The AD561 chip has several features not accessible to users of packaged AD561 devices.

1. On AD561 chips, the internal reference is not permanently connected. This allows the use of an external reference and also makes the internal reference available for external use.
2. The control amplifier summing point is accessible on the AD561 chip. Thus the user may connect an external reference voltage-to-current conversion resistor that may be specified to match an external feedback (range-setting) resistor. This enables the user to set his own output range without degrading the gain temperature coefficient.
3. An additional output span resistor is accessible. This permits the user to connect the AD561 chip for ±5, ±10 or ±20 volt spans.

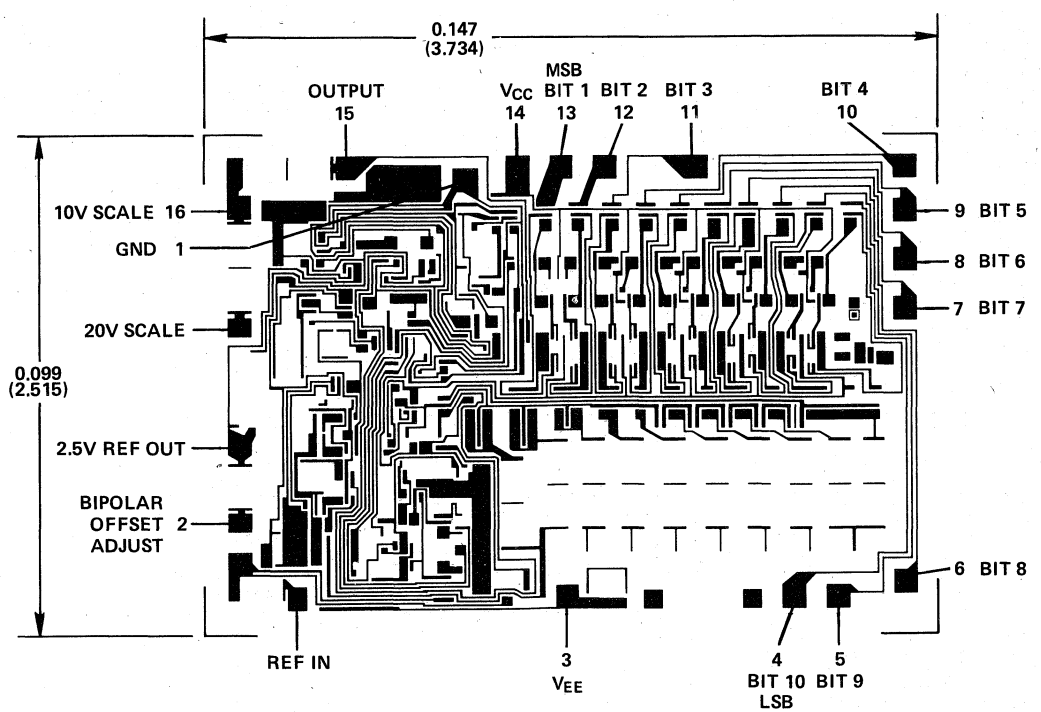
All other general application information on the AD561 packaged product catalog data sheet applies to AD561 chips.

The following additional application information applies to AD561 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD561 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (T_A = +25°C, V_{CC} = +5V, V_{EE} = -15V, unless otherwise specified)

MODEL	AD561J MIN	AD561J TYP	AD561J MAX	AD561T MIN	AD561T TYP	AD561T MAX	UNITS
RESOLUTION		10 Bits			10 Bits		
ACCURACY (Error Relative to Full Scale)		±1/4 (0.025)	±1/2 (0.05)		±1/8 (0.012)	±1/4 (0.025)	LSB % of F.S.
DIFFERENTIAL NONLINEARITY		±1/2			±1/2		LSB
DATA INPUTS							
TTL, V_{CC} = +5V							
Bit ON Logic "1"	+2.0			+2.0			V
Bit OFF Logic "0"			+0.8			+0.8	V
CMOS, 10V ≤ V_{CC} ≤ 16.5V (See Figure 1)							
Bit ON Logic "1"	70% V_{CC}			70% V_{CC}			V
Bit OFF Logic "0"			30% V_{CC}			30% V_{CC}	V
Logic Current (Each Bit) (T_{min} to T_{max})							
Bit ON Logic "1"		+5	+100		+20	+100	nA
Bit OFF Logic "0"		-5	-25		-25	-100	μA
OUTPUT							
Current							
Unipolar	1.5	2.0	2.4	1.5	2.0	2.4	mA
Bipolar	±0.75	±1.0	±1.2	±0.75	±1.0	±1.2	mA
Resistance (Exclusive of Application Resistors)		40M			40M		Ω
Unipolar Zero (All Bits OFF)		0.01	0.05		0.01	0.05	% of F.S.
Capacitance		25			25		pF
Compliance Voltage	-2	-3	+10	-2	-3	+10	V
SETTLING TIME TO 1/2LSB							
All Bits ON-to-OFF or OFF-to-ON		250			250		ns
POWER REQUIREMENTS							
V_{CC}, +4.5V dc to +16.5V dc		8	10		6	10	mA
V_{EE}, -10.8V dc to -16.5V dc		12	16		11	16	mA
POWER SUPPLY GAIN SENSITIVITY							
V_{CC}, +4.5V dc to +16.5V dc		2	10		2	10	ppm of F.S./%
V_{EE}, -10.8V dc to -16.5V dc		4	25		4	25	ppm of F.S./%
TEMPERATURE RANGE							
Operating							
Tested (T_A = +25°C to T_{max})		+25 to +70			+25 to +125		°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)		0 to +25			-55 to +25		°C
Storage		-65 to +150			-65 to +150		°C
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero, T_A = +25°C to T_{max}		1	10		1	5	ppm of F.S./°C
T_A = T_{min} to +25°C		1			1		ppm of F.S./°C
Bipolar Zero, T_A = +25°C to T_{max}		2	25		2	10	ppm of F.S./°C
T_A = T_{min} to +25°C		2			2		ppm of F.S./°C
Full Scale, T_A = +25°C to T_{max}		15	80		15	30	ppm of F.S./°C
T_A = T_{min} to +25°C		15			15		ppm of F.S./°C
Differential T_A = +25°C to T_{max}		2.5			2.5		ppm of F.S./°C
Nonlinearity, T_A = T_{min} to +25°C		2.5			2.5		ppm of F.S./°C
MONOTONICITY	Guaranteed, T_A = +25°C to T_{max} Typical, T_A = T_{min} to +25°C			Guaranteed, T_A = +25°C to T_{max} Typical, T_A = T_{min} to +25°C			
PROGRAMMABLE OUTPUT RANGES	0 to +5, 0 to +10, 0 to +20 -2.5 to +2.5, -5 to +5, -10 to +10			0 to 15, 0 to +10, 0 to +20 -2.5 to +2.5, -5 to +5, -10 to +10			V V
CALIBRATION ACCURACY							
Full Scale Error with Fixed 25Ω Resistor		±0.1			±0.1		% of F.S.
Bipolar Zero Error with Fixed 10Ω Resistor		±0.1			±0.1		% of F.S.
CALIBRATION ADJUSTMENT RANGE							
Full Scale (With 50Ω Trimmer)		±0.5			±0.5		% of F.S.
Bipolar Zero (With 50Ω Trimmer)		±0.5			±0.5		% of F.S.
REFERENCE							
Output Voltage, I_L = 0 to 1mA†	2.490	2.500	2.510	2.490	2.500	2.505	V
Maximum Current Out †		5.0			5.0		mA
Temperature Coefficient							
T_A = +25°C to T_{max}		10	80		10	60	ppm of F.S./°C
T_A = T_{min} to +25°C		10			10		ppm of F.S./°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

†Referent current out is in addition to reference current required by D-to-A REF IN and BIPOLAR OFFSET.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost, Complete 8- and 10-Bit A-to-D Converters

AD570/AD571 CHIPS

PRODUCT DESCRIPTION

The AD570 is a low-cost 8-bit successive approximation A-to-D converter consisting of a DAC, reference, clock, comparator, successive approximation register and output buffers on a single chip. The AD571 is the 10-bit version of the same chip. Since no additional components or trimming is required to perform a full-accuracy 8-bit conversion in 25μs, AD570/AD571 chips are ideal for hybrid applications. AD570J/AD571J chips are specified for operation between 0 and +70°C, AD570S/AD571S chips for −55°C to +125°C.

APPLICATION INFORMATION

AD570 and AD571 chips have one bonding pad accessible to the user that is not pinned out on packaged AD570 and AD571 devices. That pad provides two additional input ranges thus:

1. If pad 13A or 13B is used alone as the analog input, the input voltage span is 20 volts (for 0V to +20V, or −10V to +10V ranges).
2. If pads 13A and 13B are tied together and used as the analog input, the input voltage span is 10 volts (for 0V to +10V or −5V to +5V ranges) as in packaged AD570/AD571 devices.

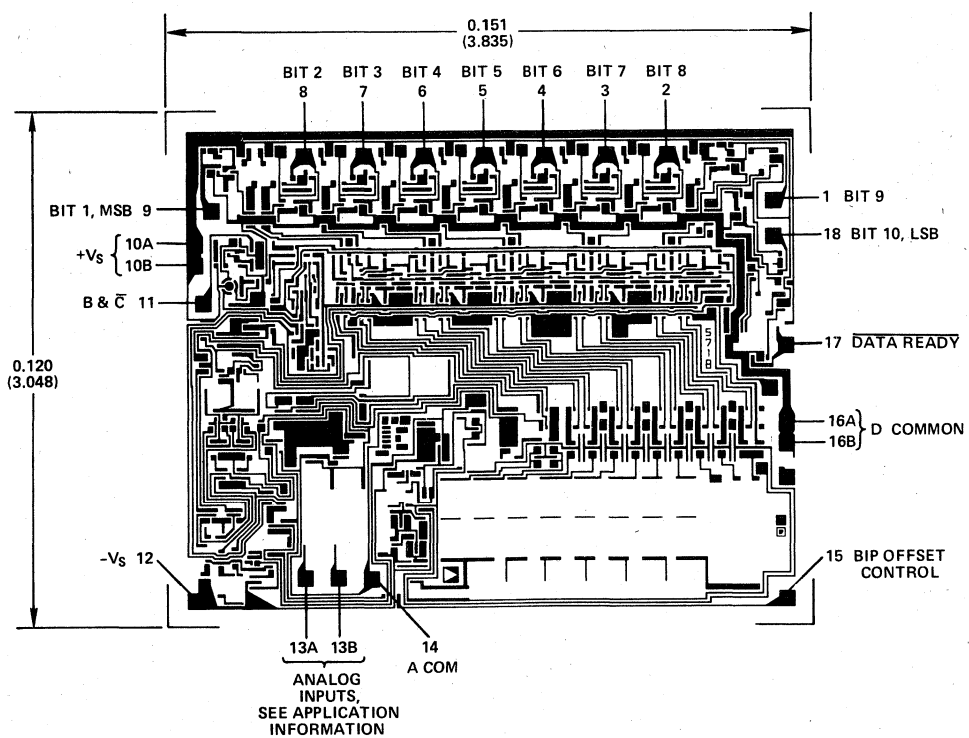
Otherwise, AD570 and AD571 chips are functionally identical to packaged AD570 and AD571 devices. For general application information, see the AD570 or AD571 packaged product catalog data sheets.

The following additional application information applies to AD570 and AD571 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD570 and AD571 chip must be connected to $-V_S$, device pad number 12.
4. Pads 10A and 10B must both be connected to $+V_S$. Pads 16A and 16B must both be connected to Digital Common.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 18-PIN CERAMIC PACKAGE.

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SPECIFICATIONS [1]

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD570J	AD571J	AD570S	AD571S
RESOLUTION	8 Bits	10 Bits	*	**
RELATIVE ACCURACY @ 25°C[2]	±1/2LSB max	±1LSB max	*	**
T_A = +25°C to T_{max}	±1/2LSB max	±1LSB max	*	**
T_A = T_{min} to +25°C	±1/2LSB	±1LSB	*	**
FULL SCALE CALIBRATION[3] (With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	±2LSB (typ)	*	**
UNIPOLAR OFFSET (max)	±1/2LSB	±1LSB	*	**
BIPOLAR OFFSET (max)	±1/2LSB	±1LSB	*	**
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)				
T_A = +25°C	8 Bits	10 Bits	*	**
T_A = +25°C to T_{max}	8 Bits	9 Bits	*	10 Bits
T_A = T_{min} to +25°C	8 Bits	9 Bits, typ	*	10 Bits, typ
TEMPERATURE RANGE				
Operating				
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +70°C	+25°C to +125°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	0 to +25°C	-55°C to +25°C	-55°C to +25°C
TEMPERATURE COEFFICIENTS				
Guaranteed max Change				
T_A = +25°C to T_{max}				
Unipolar Offset	±1LSB (88ppm/°C)	±2LSB (44ppm/°C)	±1LSB (44ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±1LSB (88ppm/°C)	±2LSB (44ppm/°C)	±1LSB (40ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±2LSB (176ppm/°C)	±4LSB (88ppm/°C)	±2LSB (80ppm/°C)	±5LSB (50ppm/°C)
Typical Change				
T_A = T_{min} to +25°C				
Unipolar Offset	±1LSB	±2LSB	*	±2LSB
Bipolar Offset	±1LSB	±2LSB	*	±2LSB
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±2LSB	±4LSB	*	±5LSB
POWER SUPPLY REJECTION				
Max Change In Full Scale Calibration				
TTL Positive Supply				
+4.5V≤V+≤+5.5V	±2LSB max	±2LSB max	*	**
Negative Supply				
-16.5V≤V+≤-13.5V	±2LSB max	±2LSB	*	**
ANALOG INPUT RESISTANCE				
10 Volt Span	3kΩ min	3kΩ min	*	**
	5kΩ min	5kΩ typ	*	**
	7kΩ min	7kΩ max	*	**
20 Volt Span	6kΩ min	6kΩ min	*	**
	10kΩ typ	10kΩ typ	*	**
	14kΩ max	14kΩ max	*	**
ANALOG INPUT RANGES				
(Analog Input to Analog Common)				
Unipolar	0 to +10V, 0 to +20V	0 to +10V, 0 to +20V	*	**
Bipolar	-5V to +5V, -10V to +10V	-5V to +5V, -10V to +10V	*	**
OUTPUT CODING				
Unipolar	Positive True Binary	Positive True Binary	*	**
Bipolar	Positive True Offset Binary	Positive True Offset Binary	*	**
LOGIC OUTPUT[6]				
Bit Outputs and Data Ready				
Output Sink Current (V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2mA min (2TTL Loads)	3.2mA min (2TTL Loads)	*	**
Output Source Current (Bit Outputs)[5] (V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	0.5mA min	*	**
Output Leakage When Blanked	±40μA max	±40μA max	*	**
LOGIC INPUT[6]				
Blank and Convert Input				
0≤V_{in}≤V+	±40μA max	±40μA max	*	**
Blank – Logic "1"	2.0V min	2.0V min	*	**
Convert – Logic "0"	0.8V max	0.8V max	*	**
CONVERSION TIME	15μs min	15μs min	*	**
	35μs typ	35μs typ	*	**
	40μs max	40μs max	*	**
POWER SUPPLY				
Absolute Maximum				
V+	+7V	+7V	*	**
V-	-16.5V	-16.5V	*	**
Specified Operating – Rated Performance				
V+	+5V	+5V	*	**
V-	-15V	-15V	*	**
Operating Range				
V+	+4.5V to +5.5V	+4.5V to +5.5V	*	**
V-		-12V to -16.5V	*	**
Operating Current				
Blank Mode				
V+ = +5V	2mA typ (10mA max)	2mA typ (10mA max)	*	**
V- = -15V	9mA typ (15mA max)	9mA typ 15mA max)	*	**
Convert Mode				
V+ = +5V	5mA	5mA	*	**
V- = -15V	10mA	10mA	*	**

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[4] Full-scale calibration temperature coefficient includes the effects of unipolar offset drift as well as gain drift.

[5] The data output lines have active pull-ups to source 0.5mA. The DATA READY line is open collector with a nominal 6kΩ internal pull-up resistor.

[6] Logic Input and Output Thresholds and Levels are tested T_A = +25°C to T_{max}, not tested but guaranteed T_A = T_{min} to +25°C.

*Specifications same as AD570J.
**Specifications same as AD571J.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . .0 to +7V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (Blank Mode). . . . . .0 to V+

ANALOG DEVICES

Fast, Complete 10-Bit A-to-D Converter With Microprocessor Interface

AD573 CHIPS

PRODUCT DESCRIPTION

The AD573 is a 10-bit successive approximation A-to-D converter consisting of a DAC, reference, clock, comparator, successive approximation register and 3 state output buffers on a single chip. Since no additional components or trimming is required to perform a full-accuracy 10-bit conversion in 1.5μs, AD573 chips are ideal for precision hybrid applications. AD573 chips are available in one grade specified for 0 to +70°C operation, and another grade for -55°C to +125°C operation.

APPLICATION INFORMATION

AD573 chips have one bonding pad accessible to the user that is not pinned out on packaged AD573 devices. That pad provides two additional input ranges thus:

1. If pad 14A or 14B is used alone as the analog input, the input voltage span is 20 volts (for 0V to +20V or -10V to +10V ranges).
2. If pads 14A and 14B are tied together and used as the analog input, the input voltage span is 10 volts (for 0V to +10V or -5V to +5V ranges) as in packaged AD573 devices.

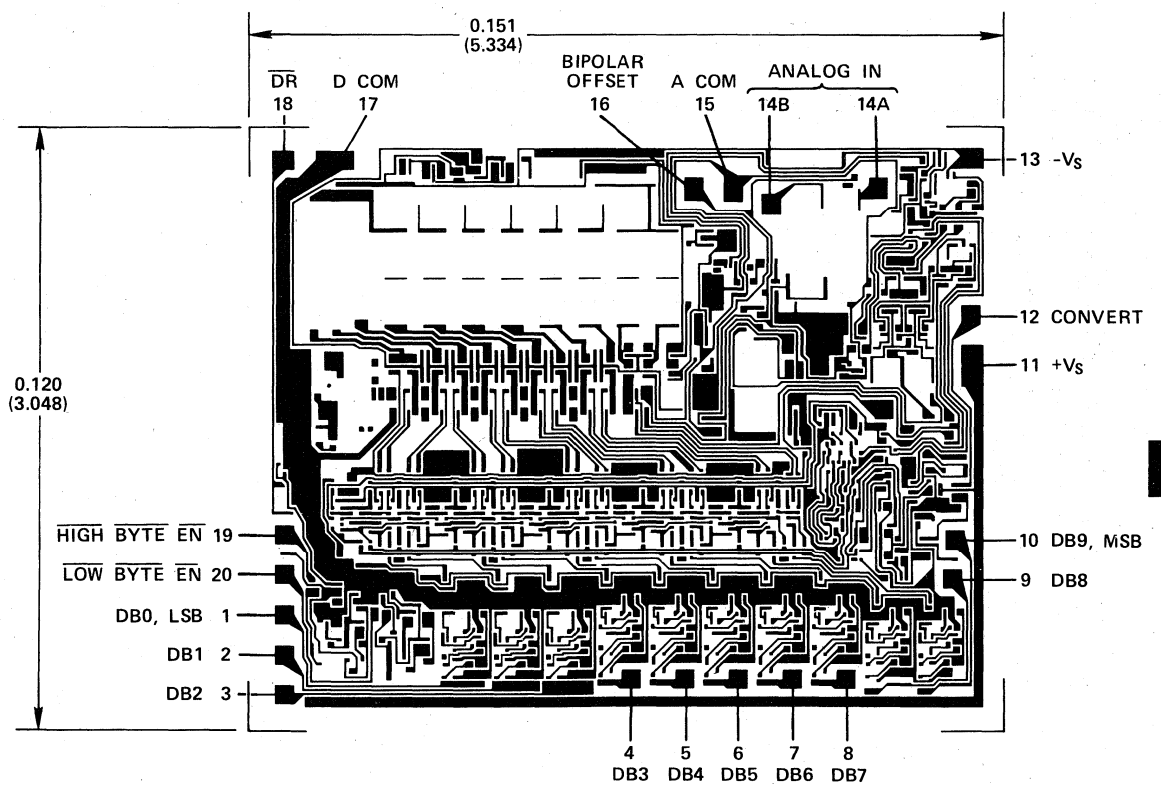
Otherwise, AD573 chips are functionally identical to packaged AD573 devices. For general application information, see the AD573 packaged product catalog data sheet.

The following additional application information applies to AD573 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD573 chip must be connected to $-V_S$, device pad number 13.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 20-PIN PACKAGE.

SPECIFICATIONS[1]

(typical @ +25°C with V+ = +5V, V- = -15V, all voltages measured with respect to digital common, unless otherwise indicated)

MODEL	AD573J	AD573S
RESOLUTION	10 Bits	*
RELATIVE ACCURACY @ 25°C[2]	±1LSB max	±1LSB max
T_A = +25°C to T_{max}	±1LSB max	±1LSB max
T_A = T_{min} to +25°C	±1LSB	±1LSB
FULL SCALE CALIBRATION[3]		
(With 15Ω Resistor In Series With Analog Input	±2LSB (typ)	*
UNIPOLAR OFFSET (max)	±1LSB	*
BIPOLAR OFFSET (max)	±1LSB	*
DIFFERENTIAL NONLINEARITY (Resolution for Which no Missing Codes are Guaranteed)		
T_A = +25°C	10 Bits	*
T_A = +25°C to T_{max}	10 Bits	10 Bits
T_A = T_{min} to +25°C	10 Bits, typ	10 Bits, typ
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	-55°C to +25°C
TEMPERATURE COEFFICIENTS		
Guaranteed max Change		
T_A = +25°C to T_{max}		
Unipolar Offset	±2LSB (44ppm/°C)	±2LSB (20ppm/°C)
Bipolar Offset	±2LSB (44ppm/°C)	±2LSB (20ppm/°C)
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB (88ppm/°C)	±5LSB (50ppm/°C)
Typical Change		
T_A = T_{min} to +25°C		
Unipolar Offset	±2LSB	±2LSB
Bipolar Offset	±2LSB	±2LSB
Full Scale Calibration[4] (With 15Ω Fixed Resistor or 50Ω Trimmer)	±4LSB	±5LSB
POWER SUPPLY REJECTION		
Max Change In Full Scale Calibration		
TTL Positive Supply		
+4.5V≤V+≤+5.5V	±2LSB max	*
Negative Supply		
-15.75V≤V-≤-14.25V	±2LSB max	*
-12.6V≤V-≤-11.4V	±2LSB max	*
ANALOG INPUT RESISTANCE		
10 Volt Span	3kΩ min	*
	5kΩ typ	*
	7kΩ max	*
20 Volt Span	6kΩ min	*
	10kΩ typ	*
	14kΩ max	*
ANALOG INPUT RANGES		
(Analog Input to Analog Common)		
Unipolar	0 to +10V, 0 to +20V	*
Bipolar	-5V to +5V, -10V to +10V	*
OUTPUT CODING		
Unipolar	Positive True Binary	*
Bipolar	Positive True Offset Binary	*
LOGIC OUTPUT[5]		
Bit Outputs and Data Ready		
Output Sink Current (V_{OUT} = 0.4V max, T_{min} to T_{max})	3.2mA min (2TTL Loads)	*
Output Source Current (Bit Outputs)[5] (V_{OUT} = 2.4V min, T_{min} to T_{max})	0.5mA min	*
Output Leakage When Blanked	±40μA max	*
LOGIC INPUT (Convert, $\overline{HBE}$, $\overline{LBE}$)		
0≤V_{IN}≤V+	±100μA max	*
Logic "1"	2.0V min	*
Logic "0"	0.8V max	*
CONVERSION TIME	10μs min	*
	15μs typ	*
	20μs max	*
POWER SUPPLY		
Absolute Maximum		
V+	+7V	*
V-	-16.5V	*
Specified Operating – Rated Performance		
V+	+5V	*
V-	-15V	*
Operating Range		
V+	+4.5V to +5.5V	*
V-	-11.4V to -15.75V	*
Operating Current		
V+ = +5V	7mA typ (25mA max)	*
V- = -15V	9mA typ (15mA max)	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Relative accuracy is defined as the deviation of the code transition points from the ideal transfer point on a straight line from the zero to the full scale of the device.

[3] Full scale calibration is guaranteed trimmable to zero with an external 50Ω potentiometer in place of the 15Ω fixed resistor. Full scale is defined as 10 volts minus 1LSB, or 9.990 volts.

[4] Full-scale calibration temperature coefficient includes the effects of unipolar offset drift as well as gain drift.

[5] The Data output lines have active pull-ups to source 0.5mA. The $\overline{DATA\ READY}$ line is open collector with a nominal 6kΩ internal pull-up resistor.

*Specifications same as AD573J.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common . . . . . .0 to +7V
V- to Digital Common . . . . . .0 to -16.5V
Analog Common to Digital Common. . . . . .±1V
Analog Input to Analog Common. . . . . ±15V
Control Inputs . . . . . 0 to V+
Digital Outputs (High Impedance State). . . . . 0 to V+

ANALOG DEVICES

Precision 2.5 Volt Reference

AD580 CHIPS

PRODUCT DESCRIPTION

The AD580 is a three-terminal, low-cost voltage reference that provides a fixed 2.5V output for inputs between 4.5V and 30V. Based on the bandgap principle and implemented with thin film resistors, temperature coefficients as low as 10ppm/°C can be guaranteed. One version of the AD580 chip is specified for 0 to +70°C operation, one grade for −55°C to +125°C.

APPLICATION INFORMATION

AD580 chips are functionally identical to packaged AD580 devices. For general application information, see the AD580 packaged product catalog data sheet.

The following additional application information applies to AD580 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD580 chip must be connected to −E.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-52, 3 PIN, METAL PACKAGE.

SPECIFICATIONS[1] (typical @ E_{IN} = +15V and 25°C unless otherwise specified)

MODEL	AD580J	AD580S
ABSOLUTE MAX RATINGS		
Input Voltage	40V	*
Operating Junction Temp Range	−55°C to +150°C	*
Storage Temperature Range	−65°C to +175°C	*
Operating Temperature Range		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested		
(T_A = T_{min} to +25°C)	0 to +25°C	−55°C to +25°C
OUTPUT VOLTAGE	2.425V min	2.490V min
	(2.575V max)	2.510V max
OUTPUT VOLTAGE CHANGE		
T_A = +25°C to T_{max}	15mV max	11mV max
	(85ppm/°C)	(25ppm/°C)
T_A = T_{min} to +25°C	15mV	11mV
LINE REGULATION		
7V ≤ V_{IN} ≤ 30V	6mV max	2mV max
	(0.6mV typ)	
4.5V ≤ V_{IN} ≤ 7V	3mV max	1mV max
	(0.3mV typ)	
LOAD REGULATION		
Δ I = 10mA	10mV max	*
QUIESCENT CURRENT	1.5mA max	*
	(1.0mA typ)	*
NOISE (0.1 to 10Hz)	60μV(p-p)	*
STABILITY		
Long Term	250μV	*
Per Month	25μV	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

*Specification same as AD580J.

Specifications subject to change without notice.

ANALOG DEVICES

Programmable Precision Low-Drift Reference

AD581/AD584 CHIPS

AD581 NOTE: An AD584 is an AD581 with additional specified versatility. When connected in the 10.0 volt configuration, the AD584 is functionally identical to the AD581. In hybrid circuits, AD584 chips may be substituted directly for AD581 chips without any electrical or mechanical design modifications.

AD581 chips will not be offered as a standard product.

PRODUCT DESCRIPTION

The AD584 is a precision voltage reference, "pin" programmable to any of four output voltages: 10.000V, 7.500V, 5.000V and 2.500V. Other voltages, above 10.000V or below 2.500V, can be programmed with an external resistor pair. The initial tolerances and temperature coefficients are laser-trimmed at the factory to provide precise and stable adjustment-free operation. One grade of the AD584 chip is specified for 0 to +70°C operation, one for −55°C to +125°C.

APPLICATION INFORMATION

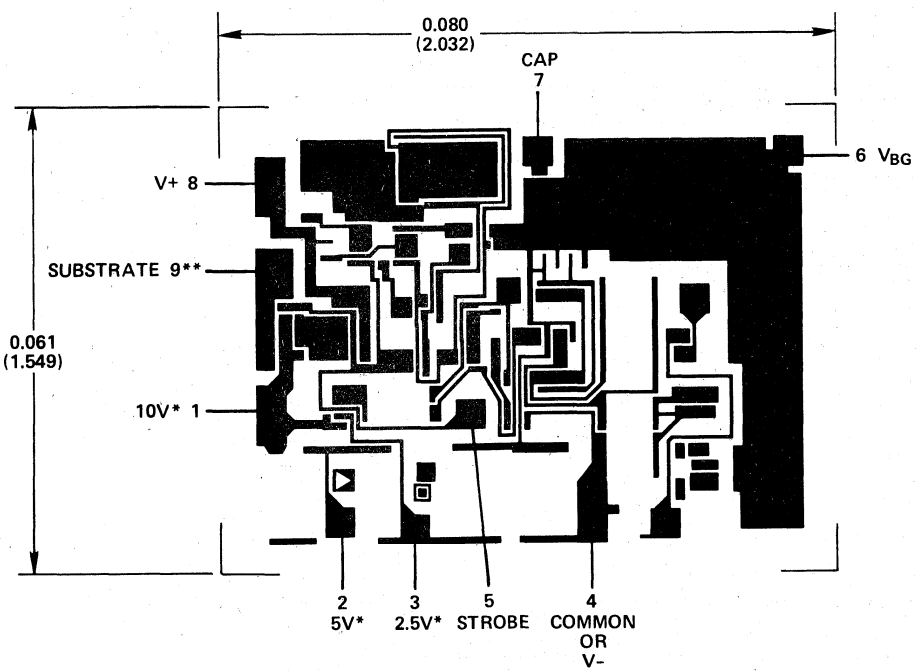
AD584 chips are functionally identical to packaged AD584 devices. For general application information, see the AD584 packaged product catalog data sheet.

The following additional application information applies to AD584 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD584 chip must be connected to V− and substrate, pads number 4 and 9.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99, 8 PIN METAL PACKAGE.

***CAUTION: INTERCONNECTIONS REQUIRED; SEE PACKAGED AD584 CATALOG DATA SHEET FOR INFORMATION.**
****NOT BROUGHT OUT ON PACKAGED DEVICE.**

17

SPECIFICATIONS [1] (typical @ V_{IN} = +15V and +25°C unless otherwise noted)

MODEL	AD584J	AD584T
ABSOLUTE MAX RATINGS		
Input Voltage V_{IN} to Ground	40V	*
Operating Junction Temp. Range	−55°C to +150°C	*
Storage Temperature Range	−65°C to +175°C	*
Operating Temperature Range		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested		
(T_A = T_{min} to +25°C	0 to +25°C	−55°C to +25°C
OUTPUT VOLTAGE TOLERANCE		
Maximum Error[2] for Nominal		
Outputs of:		
10.000V	±30mV	±10mV
7.500V	±22mV	±8mV
5.000V	±15mV	±6mV
2.500V	±7.5mV	±3.5mV
OUTPUT VOLTAGE CHANGE		
Maximum Deviation from +25°C		
Value, T_A = +25°C to T_{max}[3]		
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C
2.500V Output	30ppm/°C	20ppm/°C
Typical Deviation from +25°C		
Value, T_A = T_{min} to +25°C[3]		
10.000, 7.500, 5.000V Outputs	30ppm/°C	15ppm/°C
2.500V Output	30ppm/°C	20ppm/°C
Differential Temperature		
Coefficients Between Outputs	5ppm/°C typ	3ppm/°C typ
QUIESCENT CURRENT	1.0mA max	*
	750μA typ	*
Temperature Variation	1.5μA/°C typ	*
TURN-ON SETTLING TIME TO 0.1%	200μs	*
NOISE		
(0.1 to 10Hz)	50μV p-p	*
LONG-TERM STABILITY	25ppm/1000 Hrs. (Non-Cumulative)	*
SHORT CIRCUIT CURRENT	30mA	*
LINE REGULATION (No Load)		
15V ≤ V_{IN} ≤ 30V	0.002%/V	*
(V_{OUT} +2.5V) ≤ V_{IN} ≤ 15V	0.005%/V	*
LOAD REGULATION		
0 ≤ I_{OUT} ≤ 5mA, All Outputs	50ppm/mA max	*
	(20ppm/mA typ)	*
OUTPUT CURRENT[4]		
V_{IN} ≥ V_{OUT} +2.5V		
Source @ +25°C	10mA min	*
Source T_{min} to T_{max}	5mA min	*
Sink T_{min} to T_{max}	5mA min	200μA min
Sink −55°C to +85°C	—	5mA min

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] At Pad 1.

[3] Calculated as average over the specified operating temperature range.

[4] Tested T_A = +25°C to T_{max}. Not tested but guaranteed T_{min} to +25°C.

*Specifications same as AD584J.

Specifications subject to change without notice.

ANALOG DEVICES

Low Cost Precision Sample-and-Hold

AD582 CHIPS

PRODUCT DESCRIPTION

The AD582 is a low-cost precision sample-and-hold amplifier consisting of an operational amplifier, low-leakage analog switch and a JFET integrating amplifier. The only external component required is a holding capacitor. The AD582 may be connected in any popular op amp configuration giving the user control of gain and frequency response. The sample/hold mode control may be operated from any popular logic family. AD582 chips are available in one grade specified for 0 to +70°C operation and one for −55°C to +125°C.

APPLICATION INFORMATION

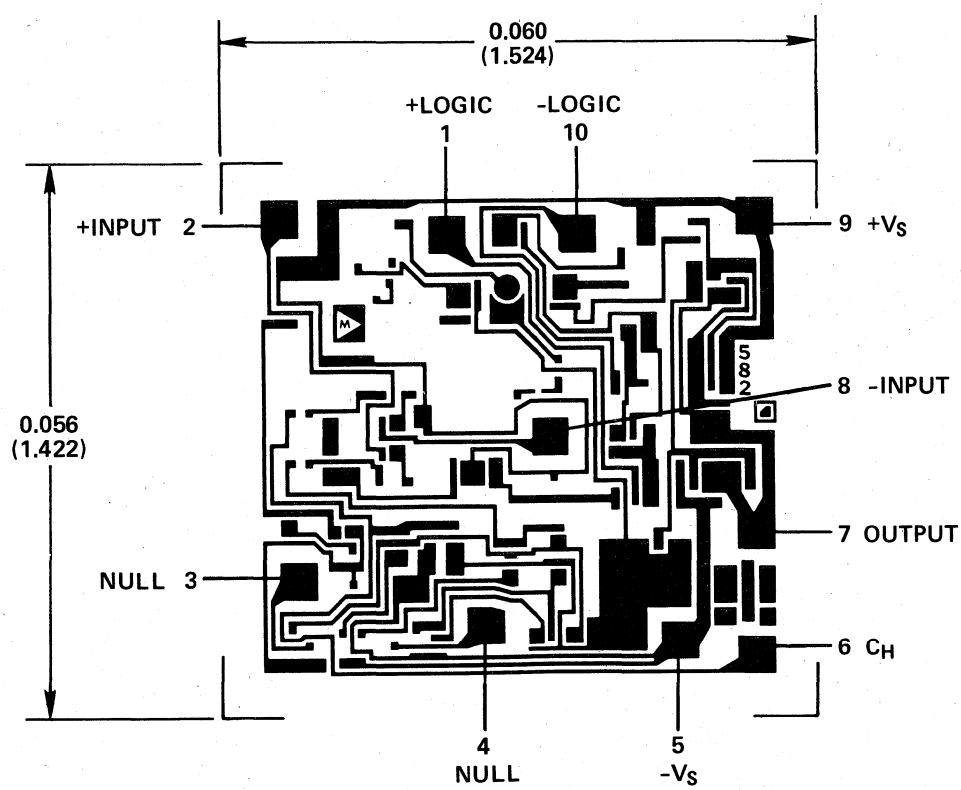
AD582 chips are functionally identical to packaged AD582 devices. For general application information, see the AD582 packaged product catalog data sheet.

The following additional application information applies to AD582 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD582 chip must be connected to $-V_S$, device pad number 5.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-100 10 PIN METAL PACKAGE.

17

SPECIFICATIONS [1] (typical @ +25°C, V_S = ±15V and C_H = 1000pF, A = +1 unless otherwise specified)

MODEL	AD582K	AD582S
SAMPLE/HOLD CHARACTERISTICS		
Acquisition Time, 10V Step to 0.1%, C_H = 100pF	6μs	*
Acquisition Time, 10V Step to 0.01%, C_H = 1000pF	25μs	*
Aperture Time, 20V p-p Input, Hold 0V	150ns	*
Aperture Jitter, 20V p-p Input, Hold 0V	15ns	*
Settling Time, 20V p-p Input, Hold 0V, to 0.01%	0.5μs	*
Droop Current, Steady State, ±10V_{OUT}	100pA max	*
Droop Current, T_A = +25°C to T_{max}	1nA	150nA max
T_A = T_{min} to +25°C	1nA	100nA
Charge Transfer	5pC max (1.5pC typ)	*
Sample to Hold Offset	0.5mV	*
Feedthrough Capacitance 20V p-p, 10kHz Input	0.05pF	*
TRANSFER CHARACTERISTICS		
Open Loop Gain V_{OUT} = 20V p-p, R_L = 2k	50k (25k min)	*
Common Mode Rejection V_{CM} = 20V p-p, F = 50Hz	70dB (60dB min)	*
Small Signal Gain Bandwidth V_{OUT} = 100mV p-p, C_H = 200pF	1.5MHz	*
Full Power Bandwidth V_{OUT} = 20V p-p, C_H = 200pF	70kHz	*
Slew Rate V_{OUT} = 20V p-p, C_H = 200pF	3V/μs	*
Output Resistance Hold Mode, I_{OUT} = ±5mA	12Ω	*
Linearity V_{OUT} = 20V p-p, R_L = 2k	±0.01%	*
Output Short Circuit Current	±25mA	*
ANALOG INPUT CHARACTERISTICS		
Offset Voltage	2mV (6mV max)	*
Offset Voltage, T_A = +25°C to T_{max}	4mV	5mV (8mV max)
T_A = T_{min} to +25°C	4mV	5mV
Bias Current	3μA max (1.5μA typ)	*
Offset Current	300nA max (75nA typ)	*
Offset Current, T_A = +25°C to T_{max}	100nA	100nA (400nA max)
T_A = T_{min} to +25°C	100nA	100nA
Input Capacitance, f = 1MHz	2pF	*
Input Resistance, Sample or Hold 20V p-p Input, A = +1	30MΩ	*
Absolute Max Diff Input Voltage	30V	*
Absolute Max Input Voltage, Either Input	±V_S	*
DIGITAL INPUT CHARACTERISTICS		
+Logic Input Voltage		
Hold Mode, T_{min} to T_{max}, -Logic @ 0V	+2V min	*
Sample Mode, T_{min} to T_{max}, -Logic @ 0V	+0.8V max	*
+Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	1.5μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	1nA	*
-Logic Input Current		
Hold Mode, +Logic @ +5V, -Logic @ 0V	24μA	*
Sample Mode, +Logic @ 0V, -Logic @ 0V	4μA	*
Absolute Max Diff Input Voltage, +L to -L	+15V/-6V	*
Absolute Max Input Voltage, Either Input	±V_S	*
POWER SUPPLY CHARACTERISTICS		
Operating Voltage Range	±9V to ±18V	±9V to ±22V
Supply Current, R_L = ∞	3mA (4.5mA max)	*
Power Supply Rejection, ΔV_S = 5V, Sample Mode	75dB (60dB min)	*
TEMPERATURE RANGE		
Operating		
Tested (T_A = +25°C to T_{max})	+25°C to +70°C	+25°C to +125°C
Guaranteed, Not Tested (T_A = T_{min} to +25°C)	0 to +25°C	-55°C to +25°C
Operating	-25°C to +85°C	-55°C to +125°C
Storage	-65°C to +150°C	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

*Specifications same as AD582K.

Specifications subject to change without notice.

Two-Terminal IC 1.2 Volt Reference

AD589 CHIPS

PRODUCT DESCRIPTION

The AD589 is a two-terminal, low cost, temperature compensated bandgap voltage reference which provides a fixed 1.23V output voltage for input currents between 50μA and 5.0mA.

The high stability of the AD589 is primarily dependent upon the matching and thermal tracking of the on-chip components. Analog Devices' precision bipolar processing and thin-film technology combine to provide excellent performance at low cost.

Additionally, the active circuit produces an output impedance ten times lower than typical low-TC zener diodes. This feature allows operation with no external components required to maintain full accuracy under changing load conditions.

The AD589J is specified for use over the 0 to +70°C temperature range and the AD589T is specified for −55°C to +125°C range.

APPLICATION INFORMATION

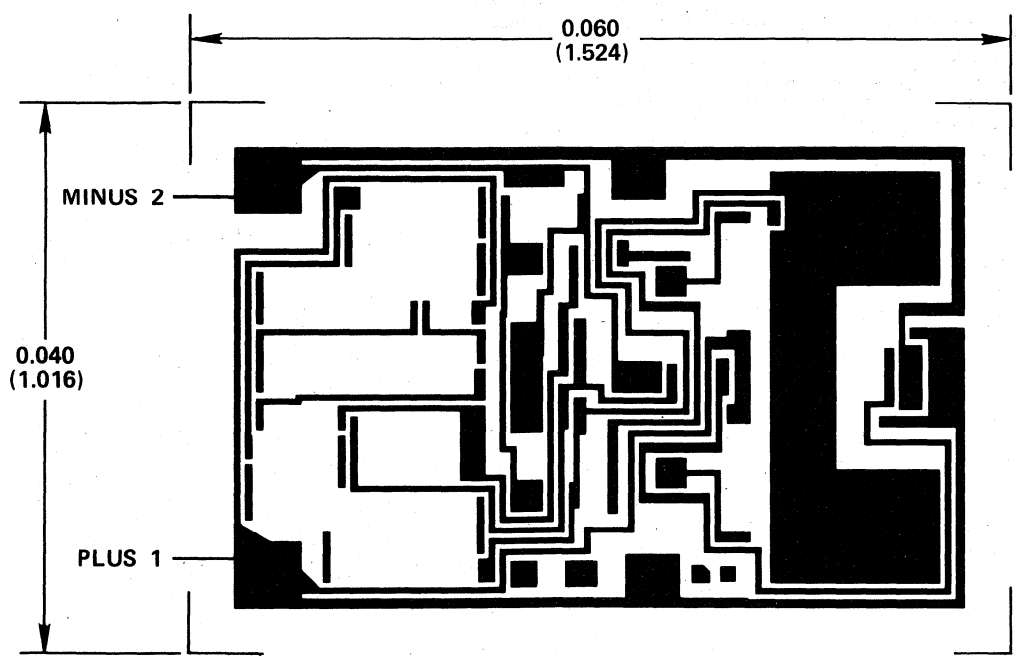
AD589 chips are functionally identical to packaged AD589 devices. For general application information, see the AD589 packaged product catalog data sheet.

The following additional application information applies to AD589 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD589 chip must be connected to the minus pad.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



17

SPECIFICATIONS[1] (typical @ I_{IN} = 500μA and T_A = 25°C unless otherwise noted)

Model	AD589J	AD589T
ABSOLUTE MAXIMUM RATINGS		
Current	10mA	*
Reverse Current	10mA	*
Power Dissipation[2]	125mW	*
Storage Temperature Range	−65°C to +175°C	*
Operating Junction Temperature Range	−55°C to +150°C	*
Lead Temperature (Soldering, 10sec)	300°C	*
Operating Temperature Range	0 to +70°C	−55°C to +125°C
OUTPUT VOLTAGE	1.200V min	*
	1.235V typ	*
	1.250V max	*
OUTPUT VOLTAGE CHANGE vs. CURRENT (50μA - 5mA)	5mV max	*
DYNAMIC OUTPUT IMPEDANCE	0.6Ω	*
	2Ω max	*
RMS NOISE VOLTAGE 10Hz < f < 10kHz	5μV	*
TEMPERATURE COEFFICIENT − ppm/°C	100 max	50 max
TURN-ON SETTLING TIME TO 0.1%	25μs	*
OPERATING CURRENT[3]	50μA min	*
	5mA max	*

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Absolute maximum power dissipation is limited by maximum current through the device. Maximum rating at elevated temperatures must be computed assuming $T_J \leq 150°C$, and θ_{JA} = 400°C/W.

[3] Optimum performance is obtained at currents below 500μA. Stray shunt capacitances should be minimized. If strays cannot be avoided, a shunt capacitor of at least 1000pF is recommended.

*Specifications same as AD589J.

Specifications subject to change without notice.

ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590 CHIPS

PRODUCT DESCRIPTION

The AD590 is a two-terminal temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V, the AD590 acts as a high impedance, constant current regulator passing 1μA/K from −55°C to +150°C. Laser-trimming of on-chip thin-film resistors calibrates the AD590 to provide a 298.2μA output at 298.2K (+25°C). Low cost, linearity and ease of application make AD590 chips ideal for monitoring temperatures at critical locations in hybrid assemblies.

APPLICATION INFORMATION

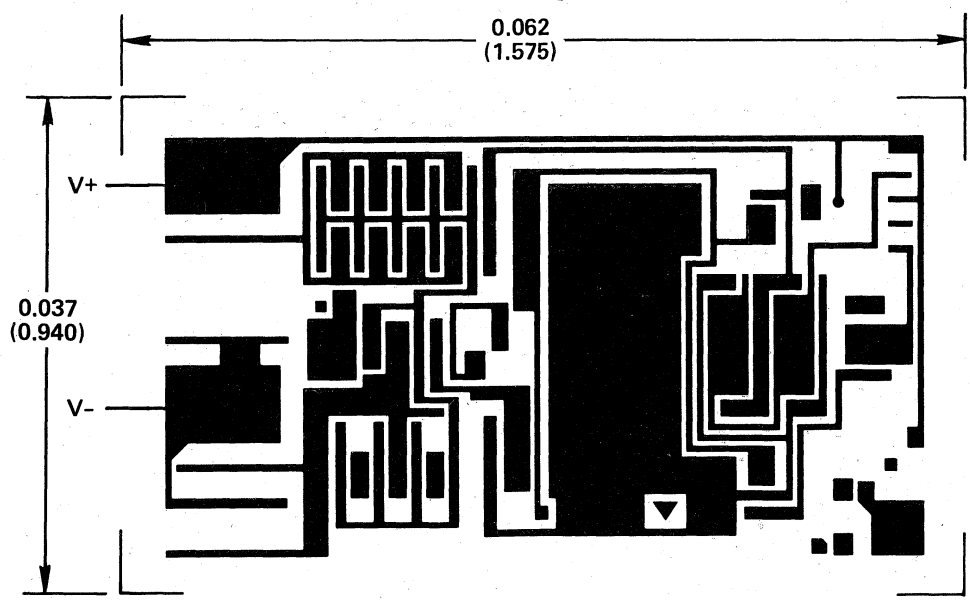
AD590 chips are functionally identical to packaged AD590 devices. For general application information, see the AD590 packaged product catalog data sheet.

The following additional application information applies to AD590 chips:

1. *IMPORTANT!* Unlike other bipolar integrated circuit chips, the AD590 substrate *must* be electrically isolated (floating). The mounting pad or header should be nonconductive, insulated or isolated.
2. No particular wire-bonding sequence must be followed.
3. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



SPECIFICATIONS[1] (typical @ +25°C and V_S = 5V unless otherwise noted)

MODEL	AD590J
ABSOLUTE MAXIMUM RATINGS	
Forward Voltage (E+ to E–)	+44V
Reverse Voltage (E+ to E–)	–20V
Rated Performance Temperature Range[2]	–55°C to +150°C
Storage Temperature Range[2]	–65°C to +175°C
POWER SUPPLY	
Operating Voltage Range	+4V to +30V
OUTPUT	
Nominal Current Output @ +25°C (298.2K)	298.2μA
Nominal Temperature Coefficient	1μA/°C
Calibration Error @ +25°C	±5.0°C max
Absolute Error[3] (over rated performance temperature range)	
Without External Calibration Adjustment	±10.0°C max
With +25°C Calibration Error Set to Zero	±3.0°C max
Nonlinearity	±1.5°C max
Repeatability[4]	±0.1°C max
Long Term Drift[5]	±0.1°C max
Current Noise	40pA/$\sqrt{\text{Hz}}$
Power Supply Rejection	
+4V ≤ V_S ≤ +5V	0.5μA/V
+5V ≤ V_S ≤ +15V	0.2μA/V
+15V ≤ V_S ≤ +30V	0.1μA/V
Case Isolation to Either Lead	$10^{10}\Omega$
Effective Shunt Capacitance	100pF
Electrical Turn-On Time[6]	20μs
Reverse Bias Leakage Current[7] (Reverse Voltage = 10V)	10pA

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] The AD590 has been used at –100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[3] See page 8–18 for explanation of error components. Note that ±1°C error is the equivalent of ±1μA error.

[4] Maximum deviation between +25°C readings after temperature cycling between –55°C and +150°C; guaranteed not tested.

[5] Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[6] Does not include self-heating effects; see page 8–19 for explanation of these effects.

[7] Leakage current doubles every 10°C.

Specifications subject to change without notice.

ANALOG DEVICES

Balanced Modulator/Demodulator

AD630 CHIPS

PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.15% accuracy (AD630A). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application note on AD630 data sheet). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

APPLICATION INFORMATION

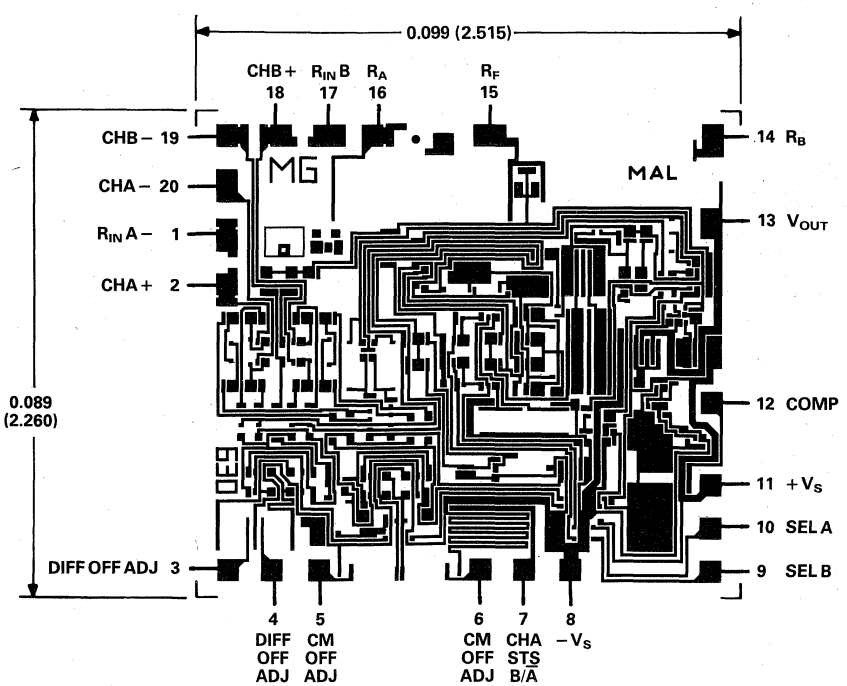
AD630 chips are functionally identical to packaged AD630 devices. For general application information, see the AD630 packaged product catalog data sheet.

The following additional application information applies to AD630 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD630 chip must be connected to $-V_S$, device pad number 8.
4. Do not connect any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D20A 20-PIN CERAMIC PACKAGE.

SPECIFICATIONS (@ +25°C and $\pm V_S = \pm 15V$ unless otherwise specified)

Model	AD630A Min	AD630A Typ	AD630A Max	Units
GAIN				
Open Loop Gain	90	110		dB
±1, ±2 Closed Loop Gain Error		0.1		%
Closed Loop Gain Match		0.1		%
Closed Loop Gain Drift		2		ppm°C
CHANNEL INPUTS				
V_{IN} Operational Limit[1]	$(-V_S + 4V)$ to $(+V_S - 1V)$			Volts
Input Offset Voltage			500	μV
Input Offset Voltage T_{min} to T_{max}[4]			800	μV
Input Bias Current		100	300	nA
Input Offset Current		10	50	nA
Channel Separation @ 10kHz		100		dB
COMPARATOR				
V_{IN} Operational Limit[1]	$(-V_S + 3V)$ to $(+V_S - 1.5V)$			Volts
Switching Window			±1.5	mV
Switching Window T_{min} to T_{max}[4]			±2.0	mV
Input Bias Current		100	300	nA
Response Time (−5mV to +5mV step)		200		ns
Channel Status I_{SINK} @ $V_{OL} = -V_S + 0.4V$[2]	1.6			mA
Pull-Up Voltage			$(-V_S + 33V)$	Volts
DYNAMIC PERFORMANCE				
Unity Gain Bandwidth		2		MHz
Slew Rate[3]		45		V/μs
Settling Time to 0.1% (20V step)		3		μs
OPERATING CHARACTERISTICS				
Common-Mode Rejection	85	105		dB
Power Supply Rejection	90	110		dB
Supply Voltage Range	±5		±16.5	Volts
Supply Current		4	5	mA
OUTPUT VOLTAGE, @ $R_L = 2k\Omega$ T_{min} to T_{max}	±10			Volts
Output Short Circuit Current		25		mA
TEMPERATURE RANGES				
Rated Performance – N Package		N/A		°C
D Package	−25		+85	°C

NOTES
[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.
[2] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.
[3] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/μs.
[4] This parameter guaranteed but not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation 600mW
Output Short Circuit to Ground . . . . . Indefinite
Max Junction Temperature . . . . . +150°C

ANALOG DEVICES

Precision Low Cost Dual BIFET Op Amp

AD642 CHIPS

PRODUCT DESCRIPTION

The AD642 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The AD642 offers matched bias currents that are significantly lower than currently available monolithic dual FET input operational amplifiers: 75pA max, matched to 25pA.

The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. Ion-implantation permits the fabbrication of precision, matched JFETs on a monolithic bipolar chip. This optimizes the process to produce matched bias currents which have lower initial bias currents than other popular FET input op amps. Laser-wafer trimming each amplifier's input offset voltage assures a tight initial match, this combined with superior IC processing guarantees offset voltage tracking over the temperature range.

APPLICATION INFORMATION

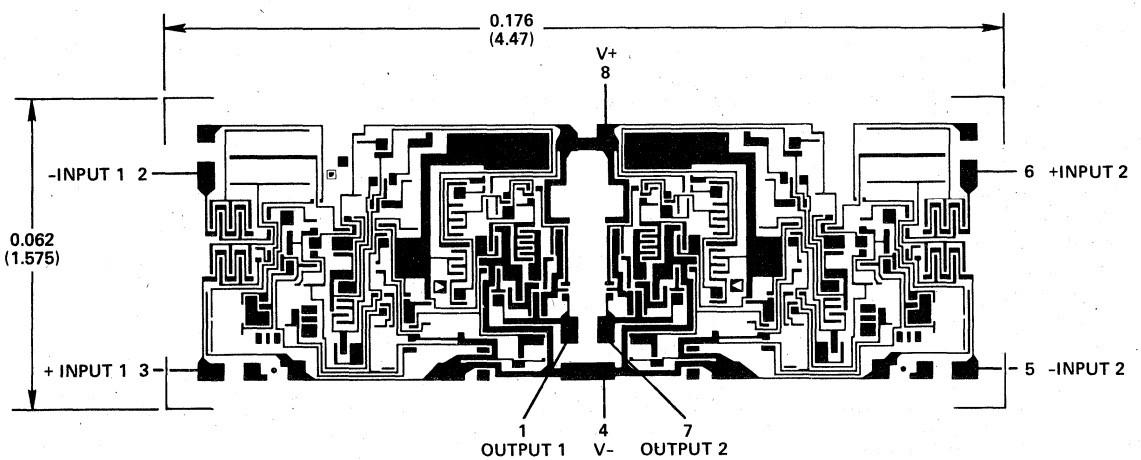
AD642 chips are functionally identical to packaged AD642 devices. For general application information, see the AD642 packaged product catalog data sheet.

The following additional applications information applies to AD642 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD642 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD642J
OPEN LOOP GAIN	
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	100,000 min
T_A = +25°C to T_{max}	100,000 min
T_{min} to +25°C	100,000
OUTPUT CHARACTERISTICS	
Voltage @ R_L = 2kΩ, T_A = min to max	(±12V) ±10V min
Voltage @ R_L = 10kΩ, T_A = min to max	(±13V) ±12V min
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	1.0MHz
Full Power Response	50kHz
Slew Rate, Unity Gain	3.0V/μs
INPUT OFFSET VOLTAGE[2]	2.0mV max
vs. Supply, T_A = +25°C to T_{max}	200μV/V max
T_{min} to +25°C	200μV/V
INPUT BIAS CURRENT	
Either Input[3]	10pA, 75pA max
Input Offset Current	5pA
MATCHING CHARACTERISTICS[4]	
Offset Voltage	1.0mV
Offset Voltage T_{min}-T_{max}	3.5mV max
Input Bias Current	35pA max
Crosstalk—1kHz 20V p-p	-124dB
INPUT IMPEDANCE	
Differential	$10^{12}\Omega$||6pF
Common Mode	$10^{12}\Omega$||6pF
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±12V (±10V min)
Common Mode Rejection, V_{IN} = ±10V	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	2.8mA max
VOLTAGE NOISE	
0.1-10Hz	2μV p-p
10Hz	$70nV/\sqrt{Hz}$
100Hz	$45nV/\sqrt{Hz}$
1kHz	$30nV/\sqrt{Hz}$
10kHz	$25nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Operating, Rated Performance	0 to +70°C
Storage	-65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3] Bias current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as the maximum safe voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

Dual High Speed Implanted FET-Input Op Amp

AD644 CHIPS

PRODUCT DESCRIPTION

The AD644 is a pair of matched high speed monolithic FET-input operational amplifiers fabricated with the most advanced bipolar, JFET and laser trimming technologies. The tight matching and temperature tracking between the operational amplifiers is achieved by ion-implanted JFETs and laser-wafer trimming. The AD644 is recommended for applications where both high speed and dc performance are required.

APPLICATION INFORMATION

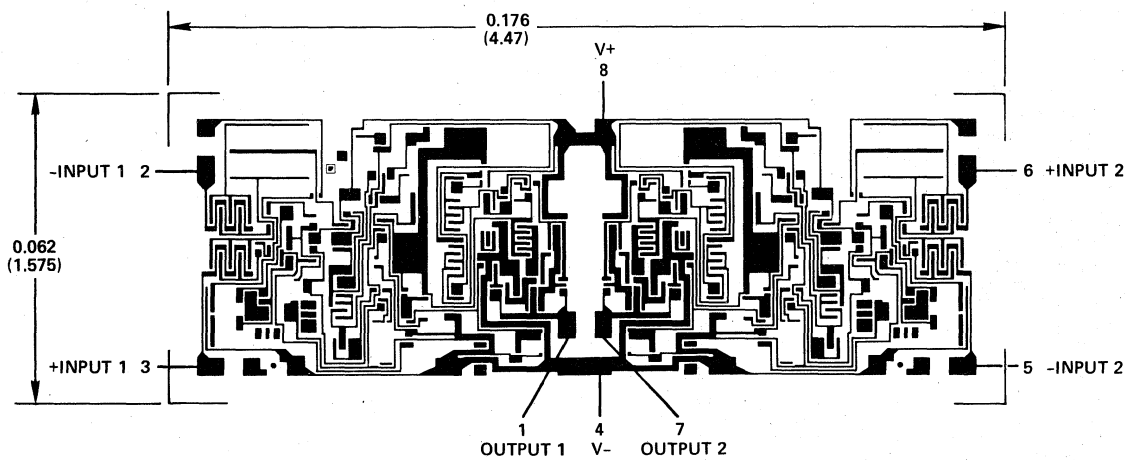
AD644 chips are functionally identical to packaged AD644 devices. For general application information, see the AD644 packaged product catalog data sheet.

The following additional application information applies to AD644 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD644 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

17

SPECIFICATIONS[1] (typical @ +25°C and V_S = ±15V dc unless otherwise specified)

MODEL	AD644J
OPEN LOOP GAIN	
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	30,000 min
T_A = +25°C to T_{max}, R_L = 2kΩ	20,000 min
$T_A = T_{min}$ to +25°C, R_L = 2kΩ	20,000
OUTPUT CHARACTERISTICS	
Voltage @ R_L = 2kΩ, T_A = min to max	±12V (±10V min)
Voltage @ R_L = 10kΩ, T_A = min to max	±13V (±12V min)
Short Circuit Current	25mA
FREQUENCY RESPONSE	
Unity Gain, Small Signal	2.0MHz
Full Power Response	200kHz
Slew Rate, Unity Gain	13.0V/μs
Total Harmonic Distortion, f = 1kHz	0.0015%
INPUT OFFSET VOLTAGE[2]	2.0mV max
vs. Supply, T_A = +25°C to T_{max}	200μV/V max
$T_A = T_{min}$ to +25°C	200μV/V
INPUT BIAS CURRENT	
Either Input[3]	10pA (75pA max)
Input Offset Current	10pA
MATCHING CHARACTERISTICS[4]	
Input Offset Voltage	1.0mV max
Input Offset Voltage $T_{min} - T_{max}$	3.5mV max
Input Bias Current	35pA max
Crosstalk	-124dB
INPUT IMPEDANCE	
Differential	$10^{12}\Omega \| 6pF$
Common Mode	$10^{12}\Omega \| 3pF$
INPUT VOLTAGE RANGE	
Differential[5]	±20V
Common Mode	±12V (±10V min)
Common Mode Rejection, V_{IN} = ±10V	76dB min
POWER SUPPLY	
Rated Performance	±15V
Operating	±(5 to 18)V
Quiescent Current	3.5mA (4.5mA max)
VOLTAGE NOISE	
0.1-10Hz	2μV p-p
10Hz	$35nV/\sqrt{Hz}$
100Hz	$22nV/\sqrt{Hz}$
1kHz	$18nV/\sqrt{Hz}$
10kHz	$16nV/\sqrt{Hz}$
TEMPERATURE RANGE	
Operating, Rated Performance	0 to +70°C
Storage	-65°C to +150°C

NOTES

[1] Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

[3] Bias Current specifications are guaranteed maximum at either input after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

[4] Matching is defined as the difference between parameters of the two amplifiers.

[5] Defined as voltage between inputs, such that neither exceeds ±10V from ground.

Specifications subject to change without notice.

ANALOG DEVICES

High Speed 8-Bit D-to-A Converter

AD DAC-08 CHIPS

PRODUCT DESCRIPTION

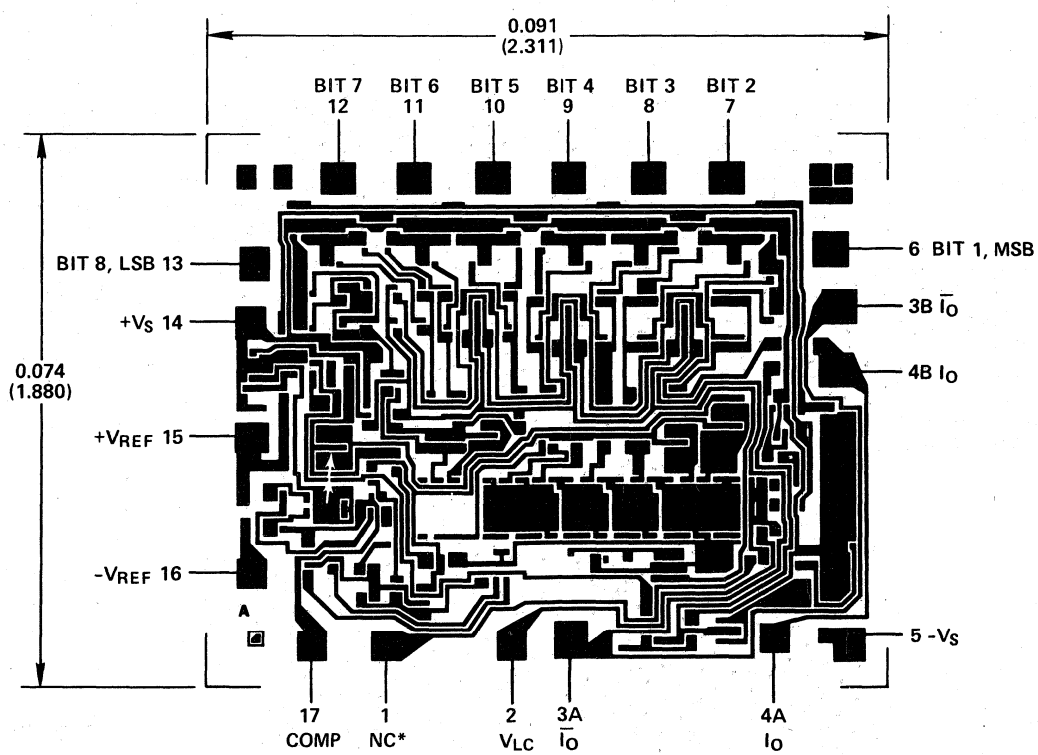
The AD DAC-08 is a high-speed 8-bit two-quadrant multiplying D-to-A converter, consisting of matched bipolar switches, a control amplifier and a precision resistor network. Advanced design and manufacturing techniques result in 85 nanosecond settling time, and compatibility with older industry standard DAC-08 devices. One accuracy grade is specified for 0 to +70°C, one for -55°C to +125°C.

APPLICATION INFORMATION

1. I_O and $\overline{I_O}$ are provided at two alternate locations.
   a.) Do not use both I_O (or both $\overline{I_O}$) locations for different functions. They are merely the same output wired to two different locations.
   b.) If $\overline{I_O}$ (or I_O) is to be unused in both locations, it should be grounded at one of the two locations.
2. No particular wire-bonding sequence must be followed.
3. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
4. For performance to device specifications, the metal substrate pad or header beneath the AD DAC-08 chip must be connected to $-V_S$, device pad number 5.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph. On AD DAC-08 chips, specifically do not connect to bonding pad area marked number 1 on metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



*NOTE: DO NOT CONNECT TO PAD NUMBER 1.
PAD NUMBERS DO NOT CORRESPOND TO PACKAGED DEVICE PIN NUMBERS.

17

SPECIFICATIONS[1] (V_S = ±15V and I_{REF} = 2.0mA unless otherwise noted)

CHARACTERISTIC	SYMBOL	CONDITIONS	T_A = 25°C to T_{MAX} MIN	TYP	MAX	T_A = T_{MIN} to +25°C MIN	TYP	MAX	UNITS
NONLINEARITY									
AD DAC-08A					±0.1		±0.1		%FS
AD DAC-08C					±0.39		±0.39		%FS
SETTLING TIME	t_s	Full-Scale Step to 1/2LSB		85			85		ns
PROPAGATION DELAY	t_{PLH}, t_{PHL}	All Bits Switched		35			35		ns
FULL SCALE TEMPCO	TC I_{FS}								
AD DAC-08A				±10	±50		±10		ppm/°C
AD DAC-08C				±10	±80		±10		ppm/°C
OUTPUT VOLTAGE COMPLIANCE	V_{OC}	$\Delta I_{FS} < 1/2LSB$ $R_{OUT} > 20M\Omega$	-10		+18	-10		+18	V
FULL SCALE CURRENT	I_{FS4}	V_{REF} = 10.000V $R_{14} = R_{15}$ = 5.000kΩ T_A = 25°C							
AD DAC-08C			1.94	1.99	2.04		1.99		mA
AD DAC-08A			1.984	1.992	2.000		1.992		mA
FULL SCALE SYMMETRY	I_{FSS}	($I_{FS4} - I_{FS2}$)							
AD DAC-08A				±0.5	±4.0		±0.5		µA
AD DAC-08C				±2.0	±16.0		±2.0		µA
ZERO SCALE CURRENT	I_{ZS}								
AD DAC-08A				0.1	1.0		0.1		µA
AD DAC-08C				0.2	4.0		0.2		µA
OUTPUT CURRENT RANGE	I_{FSR}	V- = -5.0V	0	2.0	2.1		2.0		mA
		V- = -7.0 to -18V	0	2.0	4.2		2.0		mA
LOGIC INPUT LEVELS									
Logic "0"	V_{IL}	V_{LC} = 0V			0.8		0.8		V dc
Logic "1"	V_{IH}	V_{LC} = 0V	2.0				2.0		V dc
LOGIC INPUT CURRENTS									
Logic "0"	I_{IL}	$-10V < V_{IN} < +0.8V$		-2.0	-10		-2.0		µA
Logic "1"	I_{IH}	$2.0V < V_{IN} < 18V$		0.002	10		0.002		µA
LOGIC INPUT SWING	V_{IS}	V- = -15V	-10		+18	-10		+18	V
LOGIC THRESHOLD RANGE	V_{IHL}	V_S = ±15V	-10		+13.5	-10		+13.5	V
REFERENCE BIAS CURRENT	I_{REF}		+0.1	-1.0	-3.0		-1.0		µA
REFERENCE INPUT SLEW RATE	dI/dt		4.0	8.0			8.0		mA/µs
POWER SUPPLY SENSITIVITY	$PSSI_{FS+}$	V+ = 4.5V to 18V		±0.003	±0.01		±0.0003		%/%
	$PSSI_{FS-}$	V- = -4.5V to -18V		±0.002	±0.01		±0.002		%/%
		I_{REF} = 1.0mA							
POWER SUPPLY CURRENT	I+	From $+V_S$	0.4	2.3	3.8		2.3		mA
	I-	From $-V_S$	-0.8	-6.4	-7.8		-6.4		mA
POWER DISSIPATION	P_D	±5V, I_{REF} = 1.0mA		33	48		33		mW
		+5V, -15V, I_{REF} = 2.0mA		108	136		108		mW
		±15V, I_{REF} = 2.0mA		135	174		135		mW

NOTES
[1] AD DAC-08A specifications apply for the -55°C to +125°C range. The AD DAC-08C specifications apply for T_A = 0 to +70°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- AD DAC-08A . . . . . -55°C to +125°C
- AD DAC-08C . . . . . 0 to +70°C

Storage Temperature . . . . . -65°C to +150°C
Power Dissipation 500mW
Above 100°C Derate by . . . . . 10mW/°C
$-V_S$ Supply to $+V_S$ Supply 36V
Logic Inputs . . . . . $-V_S$ to ($-V_S$ +36V)
V_{LC} . . . . . $-V_S$ to $+V_S$
Reference Inputs (V_{14}, V_{15}) . . . . . $-V_S$ to $+V_S$
Reference Input Differential Voltage (V_{14} to V_{15}) . . . . . ±18V
Reference Input Current (I_{14}) 5.0mA

ANALOG DEVICES

Ultra-Low Offset Voltage Op Amp

AD OP-07 CHIPS

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard. OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 1,200,000 affords increased accuracy in high closed loop gain applications. Input offset voltages of 60μV, bias currents of 1.8nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of 0.4μV/°C and long-term stability of 0.4μV/month eliminate recalibration or loss of initial accuracy. Two grades of AD OP-07 chips are specified for 0 to +70°C operation.

APPLICATION INFORMATION

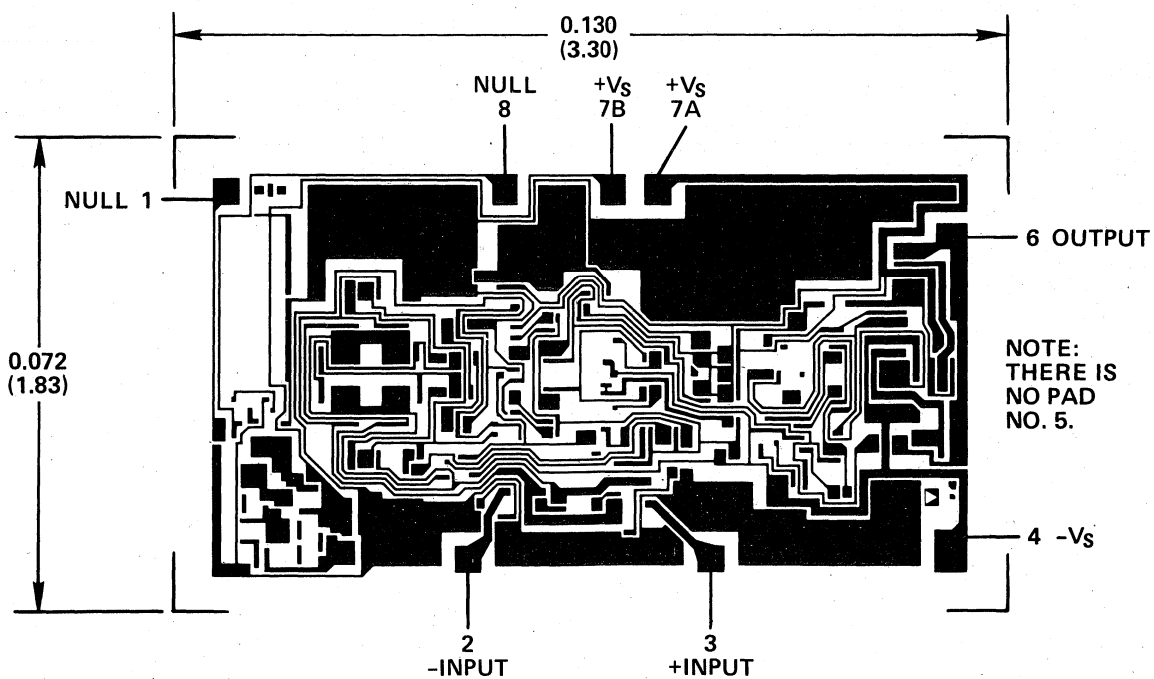
AD OP-07 chips are functionally identical to packaged AD OP-07 devices. For general application information, see the AD OP-07 packaged product catalog data sheet.

The following additional application information applies to AD OP-07 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD OP-07 chip must be connected to $-V_S$, device pad number 4.
4. Pads 7A and 7B must *both* be connected to $+V_S$.
5. Do not connect to any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBER CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGES.

17

SPECIFICATIONS [1] (T_A = +25°C, V_S = ±15V, unless otherwise specified)

Model			AD OP-07C			AD OP-07D			
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
OPEN LOOP GAIN	A_{VO}	$R_L \geq 2k\Omega$, V_O = ±10V	1,200	4,000		1,200	4,000		V/mV
		$R_L \geq 2k\Omega$, V_O = ±10V							
		T_A = +25°C to T_{max}	1,000	4,000		1,000	4,000		V/mV
		T_A = T_{min} to +25°C		1,000			1,000		V/mV
		$R_L \geq 500\Omega$, V_O = ±0.5V, V_S = ±3V	300	1,000		300	1,000		V/mV
OUTPUT CHARACTERISTICS									
Maximum Output Swing	V_{OM}	$R_L \geq 10k\Omega$	±12.0	±13.0		±12.0	±13.0		V
		$R_L \geq 2k\Omega$	±11.5	±12.8		±11.5	±12.8		V
		$R_L \geq 1k\Omega$		±12.0					V
Open Loop Output Resistance	R_O	V_O = 0, I_O = 0		60			60		Ω
FREQUENCY RESPONSE									
Closed Loop Bandwidth	BW	A_{VCL} = +1.0		0.6			0.6		MHz
Slew Rate	SR	$R_L \geq 2k$		0.17			0.17		V/μs
INPUT OFFSET VOLTAGE									
Initial	V_{OS}	Note 2		60	150		60	150	μV
		Note 2, T_A = +25°C to T_{max}		85	250		85	250	μV
		T_A = T_{min} to +25°C		85			85		μV
Adjustment Range		R_P = 20kΩ		±4			±4		mV
INPUT OFFSET CURRENT									
Initial	I_{OS}			0.8	6.0		0.8	6.0	nA
INPUT BIAS CURRENT									
Initial	I_B			±1.8	±7.0		±2.0	±12	nA
INPUT RESISTANCE									
Differential	R_{IN}		8	33		7	31		MΩ
Common Mode	R_{IN} CM			120			120		GΩ
INPUT VOLTAGE RANGE									
Common Mode	CMVR		±13.0	±14.0		±13.0	±14.0		V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±CMVR	100	120		94	110		dB
		V_{CM} = ±CMVR, T_{min} to T_{max}	97	120		94	106		dB
POWER SUPPLY									
Current, Quiescent	I_Q	V_S = ±15V		3.5	5.0		3.5	5.0	mA
Power Consumption	P_D	V_S = ±15V		105	150		105	150	mW
		V_S = ±3V		6.0	8.4		6.0	8.4	mW
Rejection Ratio	PSRR	V_S = ±3V to ±18V	90	104		90	104		dB
OPERATING TEMPERATURE RANGE	T_{min}, T_{max}		0		+70	0		+70	°C

NOTES

[1] Electrical tests are performed at wafer prove, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

[2] Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

Specifications subject to change without notice.

ANALOG DEVICES

Ultra-Low Noise, Precision Op Amp

AD OP-27 CHIPS

PRODUCT DESCRIPTION

The AD OP-27 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. State-of-the-art performance for high accuracy amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-27. As a device directly compatible with other low noise op amps, the AD OP-27 features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-27 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of $3.0nV/\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. AC specifications including a 2.8V/μs slew rate and an 8MHz gain bandwidth product are possible without sacrificing dc accuracy. Long term stability is assured by an input offset voltage drift specification of 0.2μV/month.

Source resistance related errors with the AD OP-27 are minimized by a low input bias current at ambient of ± 10nA and an input offset current of 7nA. An input bias current cancellation circuit limits bias and offset currents over the extented temperature range to ± 20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

APPLICATION INFORMATION

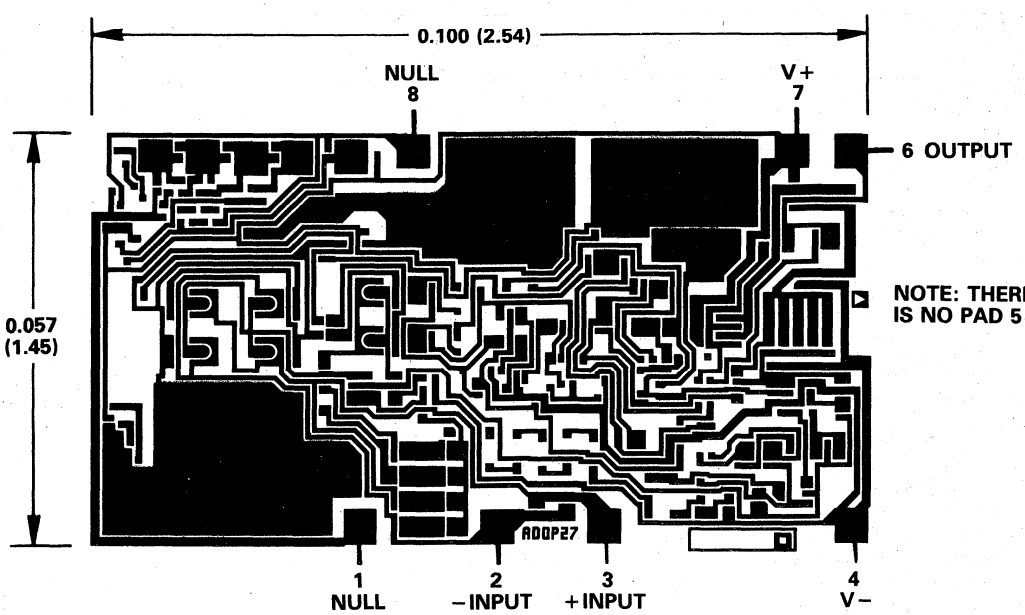
AD OP-27 chips are functionally identical to packaged AD OP-27 devices. For general application information, see the AD OP-27 packaged product catalog data sheet.

The following additional application information applies to AD OP-27 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD OP-27 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

17

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-27G			UNITS
PARAMETER	SYMBOL	MIN	TYP	MAX	
OPEN LOOP GAIN	A_{VO}	700	1,500		V/mV
		–	1,500		V/mV
		200	500		V/mV
		450	1,000		V/mV
OUTPUT CHARACTERISTICS					
Voltage Swing	V_O	±11.5	±13.5		V
		±10.0	±11.5		V
		±11.0	±13.3		V
Open-Loop Output Resistance	R_O		70		Ω
FREQUENCY RESPONSE					
Gain Bandwidth Product	GBW	5.0	8.0		MHz
Slew Rate	SR	1.7	2.8		V/μs
INPUT OFFSET VOLTAGE					
Initial	V_{OS}		30	100	μV
			55	220	μV
Average Drift	TCV_{OS}		0.4	1.8	μV/°C
Long Term Stability	V_{OS}/Time		0.4	2.0	μV/month
Adjustment Range			±4.0		mV
INPUT BIAS CURRENT					
Initial	I_B		±15	±80	nA
			±25	±150	nA
INPUT OFFSET CURRENT					
Initial	I_{OS}		12	75	nA
			20	135	nA
INPUT NOISE					
Voltage	e_n p-p		0.09	0.25	μV p-p
Voltage Density	e_n		3.8	8.0	nV/$\sqrt{Hz}$
			3.3	5.6	nV/$\sqrt{Hz}$
			3.2	4.5	nV/$\sqrt{Hz}$
Current Density	i_n		1.7	–	pA/$\sqrt{Hz}$
			1.0	–	pA/$\sqrt{Hz}$
			0.4	0.6	pA/$\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common Mode	CMVR	±11.0	±12.3		V
		±10.5	±11.8		V
Common-Mode Rejection Ratio	CMRR	100	120		dB
		96	118		dB
INPUT RESISTANCE					
Differential	R_{IN}	0.8	4		MΩ
Common Mode	R_{INCM}		2		GΩ
POWER SUPPLY					
Rated Performance			±15		V
Operating			±(4–18)		V
Current, Quiescent	I_Q		3.3	5.6	mA
Rejection	PSR		2	20	μV/V
			2	32	μV/V
Power Consumption	P_d		100	170	mW
OPERATING TEMPERATURE RANGE					
T_{MIN}, T_{MAX}		−25		+85	°C

NOTES

Note 1: For supply voltages less than ±18V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The AD OP-27's inputs are protected by back-to-back diodes. To achieve low noise current limiting resistors could not be used. If the differential input voltage exceeds ±0.7V, the input current should be limited to 25mA.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Internal Power Dissipation 500mW
Input Voltage (Note 1) . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage (Note 2) . . . . . ±0.7V
Differential Input Current (Note 2) . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C

ANALOG DEVICES

Ultra-Low Noise, High Speed Precision Op Amp

AD OP-37 CHIPS

PRODUCT DESCRIPTION

The AD OP-37 offers the combined features of high precision, ultra-low noise and high speed in a monolithic bipolar operational amplifier. High speed accurate amplification of very low level signals, where inherent device noise can be the limiting factor, is attainable with the AD OP-37 in applications requiring gains greater than five. This instrumenation grade op amp features industry standard dc performance; input offset voltages of 10μV and input offset voltage temperature coefficients of 0.2μV/°C. The super low input voltage noise performance of the AD OP-37 is characterized by an e_n p-p of 80nV (0.1Hz to 10Hz), an e_n of $3.0nV/\sqrt{Hz}$ (at 1kHz) and a 1/f noise corner frequency of 2.7Hz. High speed performance is assured by a 17V/μs slew rate and a 63MHz gain bandwidth product. Long term stability is guaranteed by an input offset voltage drift specification of 0.2μV/month.

Source resistance related input errors with the AD OP-37 are minimized by a low input bias current of ±10nA and an input offset current of 7nA. An input bias current cancellation circuit restricts bias and offset currents over the extended temperature range to ±20nA and 15nA, respectively. Other factors inducing input referred errors such as power supply variations and common-mode voltages are attenuated by a PSRR and CMRR of at least 120dB.

APPLICATION INFORMATION

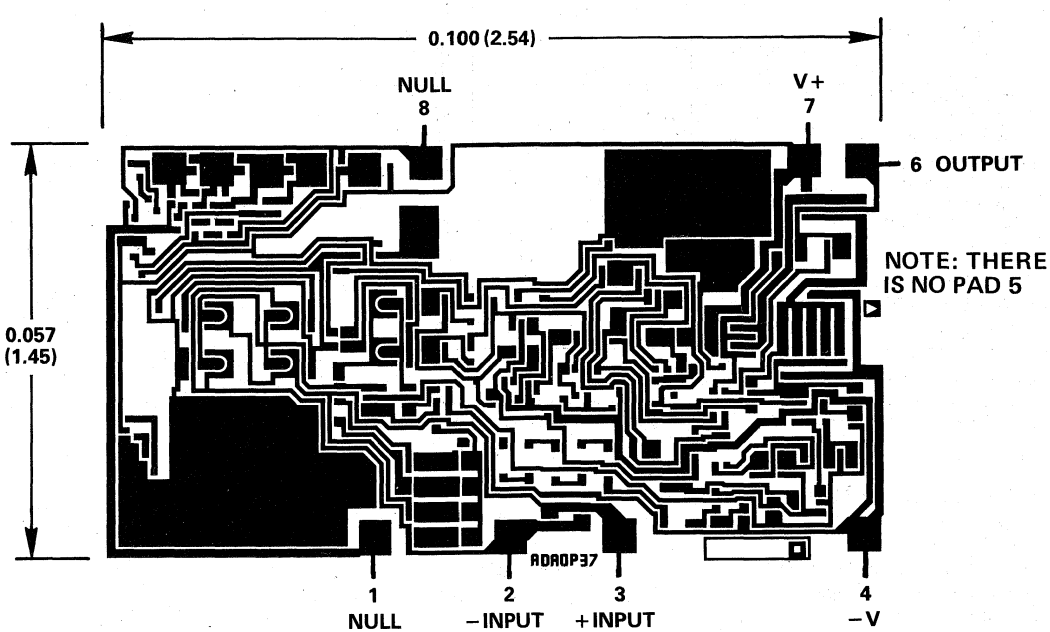
AD OP-37 chips are functionally identical to packaged AD OP-37 devices. For general application information, see the AD OP-37 packaged product catalog data sheet.

The following additional application information applies to AD OP-37 chips:

1. No particular wire-bonding sequence must be followed.
2. For assembly information, see the Bipolar Integrated Circuit Chips General Information Section.
3. For performance to device specifications, the metal substrate pad or header beneath the AD OP-37 chip must be connected to $-V_S$, device pad number 4.
4. Do not connect any bonding pads or metalization not indicated as a functional bonding pad on the metalization photograph.

METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE TO-99 8-PIN METAL PACKAGE.

SPECIFICATIONS ($T_A = +25°C$, $V_S = \pm 15V$, unless otherwise specified)

MODEL		AD OP-37G			UNITS
PARAMETER	SYMBOL	MIN	TYP	MAX	
OPEN LOOP GAIN	A_{VO}	700	1,500		V/mV
		400	1,500		V/mV
		200	500		V/mV
		450	1,000		V/mV
OUTPUT CHARACTERISTICS					
Voltage Swing	V_O	±11.5	±13.5		V
		±10.0	±11.5		V
		±11.0	±13.3		V
Open-Loop Output Resistance	R_O		70		Ω
FREQUENCY RESPONSE					
Gain Bandwidth Product	GBW	45	63		MHz
		–	40		MHz
Slew Rate	SR	11	17		V/μs
INPUT OFFSET VOLTAGE					
Initial	V_{OS}		30	100	μV
			55	220	μV
Average Drift	TCV_{OS}		0.4	1.8	μV/°C
Long Term Stability	V_{OS}/Time		0.4	2.0	μV/month
Adjustment Range			±4.0		mV
INPUT BIAS CURRENT					
Initial	I_B		±15	±80	nA
			±25	±150	nA
INPUT OFFSET CURRENT					
Initial	I_{OS}		12	75	nA
			20	135	nA
INPUT NOISE					
Voltage	e_n p-p		0.09	0.25	μV p-p
Voltage Density	e_n		3.8	8.0	nV/√Hz
			3.3	5.6	nV/√Hz
			3.2	4.5	nV/√Hz
Current Density	i_n		1.7	–	pA/√Hz
			1.0	–	pA/√Hz
			0.4	0.6	pA/√Hz
INPUT VOLTAGE RANGE					
Common Mode	CMVR	±11.0	±12.3		V
		±10.5	±11.8		V
Common-Mode Rejection					
Ratio	CMRR	100	120		dB
		96	118		dB
INPUT RESISTANCE					
Differential	R_{IN}	0.8	4		MΩ
Common Mode	R_{INCM}		2		GΩ
POWER SUPPLY					
Rated Performance			±15		V
Operating			±(4–18)		V
Current, Quiescent	I_Q		3.3	5.6	mA
Rejection	PSR		2	20	μV/V
			2	32	μV/V
Power Consumption	P_d		100	170	mW
OPERATING TEMPERATURE RANGE					
T_{MIN}, T_{MAX}		−25		+85	°C

NOTE
Specifications subject to change without notice.

Electrical tests are performed at wafer probe, before the wafer is separated into individual dice. Maintaining chip performance to specification requires great care in handling and assembly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±18V
Input Voltage . . . . . ±18V
Output Short Circuit Duration . . . . . Indefinite
Differential Input Voltage . . . . . ±0.7V
Differential Input Current . . . . . ±25mA
Storage Temperature Range . . . . . −65°C to +150°C
Operating Temperature Range . . . . . −25°C to +85°C

CMOS Integrated Circuit Chips
General Information

PHYSICAL CHARACTERISTICS

Die Thickness: The thickness of Analog Devices CMOS dice is 20 mils ±1 mil except dielectrically isolated CMOS, which is 20 mils ±3 mils.

Die Dimensions: The dimensions given on the specific device data sheets have a tolerance of ±3 mils.

Backing: The backside surface of Analog Devices CMOS dice is silicon (not plated). Analog Devices has determined that an unplated backing allows thinner dice, better controlled thickness, better thermal transfer and more reliable die attach. Gold backing is not available for CMOS die.

Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.

Top Surface: The top surface of the dice is covered by a layer of Phosphorous-doped-Vapox glassivation. All areas are covered except bonding pads and scribe lines.

Surface Metalization: The metalization on Analog Devices CMOS dice is aluminum. Minimum metalization thickness is 10,000Å.

Bonding Pads: All bonding pads have a minimum size of 4 mils by 4 mils. The passivation windows are 3.5 mils minimum.

VISUAL INSPECTION

All Analog Devices CMOS dice are 100% inspected. In addition, Quality Assurance performs a sample audit to the same visual criteria to an AQL of 0.65%.

PROCESS FLOW

The process flow chart for Analog Devices CMOS dice is shown on page 17-58. All CMOS dice are 100% probed to +25°C functional and dc parametic limits as per the data sheet limits for the equivalent packaged version. (See page 17-59 for the packaged product equivalent of CMOS dice). Reject die are inked.

Additionally, all CMOS dice are 100% inspected. Quality Assurance audits to the same visual criteria to an AQL of 0.65%.

Following visual inspection, a sample of the die lot is assembled in ceramic packages and submitted to opens/shorts testing to cull out any assembled-related failures.

Following open/short testing, the remaining packaged sample is submitted to 100% temperature testing of dc parameters. The limits used are the upper temperature limits of the similar grade packaged product (see page 17-59). The lot is rejected if the temperature test PDA (percent defective allowable) is greater than 15%.

Special electrical sorts or sample plans can sometimes be accommodated at extra cost if volume warrants.

ELECTRICAL TESTS

All chips are 100% tested at wafer sort per published +25°C dc parameters for the equivalent grade packaged product (see page 17-59) before the wafer is separated into individual dice.

Additionally, a packaged sample of each die lot is submitted to hot temperature testing. A maximum PDA of 15% is required for lot acceptance by Q.A.

Maintaining chip performance to specifications requires great care in handling and assembly. The specific recommendations in this general information section are intended to assist the user in achieving specified performance of Analog Devices CMOS chips in assembled circuits.

ELECTRICAL GUARANTEES

Analog Devices CMOS chips are guaranteed to provide an 85% yield to standard packaged product data sheet performance specifications over the operating temperature range indicated on the data sheet for the equivalent packaged grade.

PACKAGING

All dice are packaged in plastic waffle packs. The quantity of dice per package depends on die size.

A sheet of anti-static paper is included in each pack.

The waffle pack is sealed in a plastic vacuum-sealed package. The package is back-filled with nitrogen.

ASSEMBLY INFORMATION

Cleaning: Each die is cleaned prior to packaging in waffle packs. No additional cleaning is recommended.

Die Inspection: All Analog Devices CMOS dice are 100% inspected.

No further inspection is required.

Die Attach: The proper method of die attach is determined by the requirements of the particular application.

When eutectic die attach is indicated, Analog Devices recommends using either a 99.99% gold or a 98% gold 2% silicon preform.

When conductive epoxy die attach is indicated, Analog Devices recommends the use of Able Bond 36-2 or equivalent.

Die attach temperature should be as low as possible and should never exceed 400°C as measured at the die-substrate interface surface. Time at 400°C shall not exceed 120 seconds.

Lead Bonding: Analog Devices recommends using thermosonic or thermo-compression bonding for users requiring gold wire. One mil 99.99% gold wire is recommended.

Analog Devices recommends using ultra-sonic bonding for users requiring aluminum wire. One mil 99% aluminum 1% silicon wire is recommended.

To prevent damage from electrostatic discharge, bond the GND pin first. If a device has both an analog and a digital ground, bond DGND first.

Electrostatic Discharge (ESD): CMOS integrated circuits may be catastrophically damaged by ESD if not handled properly.

Furthermore, subtle shifts in transistor characteristics can be caused by a more limited exposure to ESD, causing the performance of a precision device to become degraded.

To prevent damage caused by ESD, Analog Devices recommends the following:

a. Verify proper grounding of all manufacturing equipment.

b. All workers who handle the chips should be wearing a grounded conductive wrist-strap.

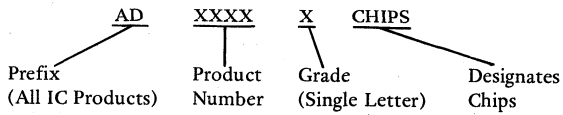
c. All work-in-process, especially any work with incomplete wire-bonding, should be placed on a conductive surface.

d. Dice not in use should be stored in the original waffle pack with anti-static paper.

Specific data sheets in this catalog describe the recommended bonding sequence for each CMOS device.

ORDERING INFORMATION

Analog Devices CMOS integrated circuit chips are specified in the same manner as packaged devices, except the package code letter is replaced by the word "CHIPS".



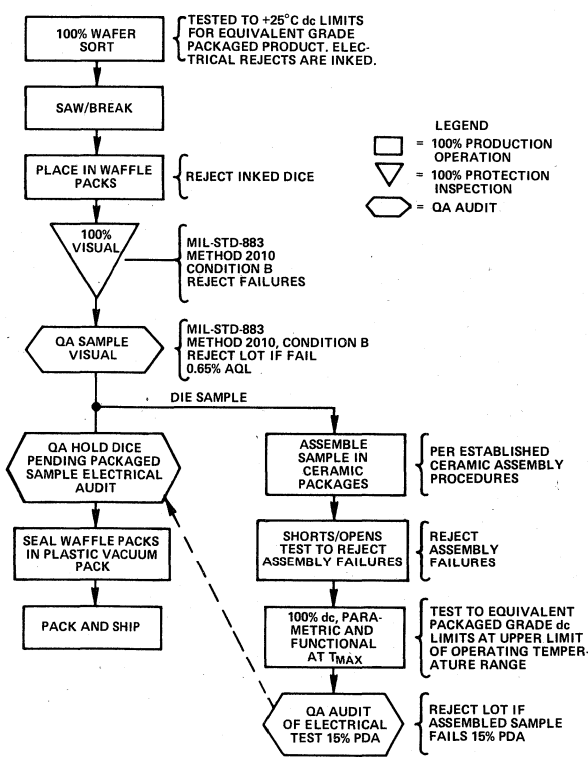
Minimum order quantity for CMOS chips is 50 pieces per line item. Additionally, Analog Devices CMOS dice are supplied in multiples of 25 pieces.

Not all packaged product generics, grades or temperature ranges can be supplied in chip form. See page 17-63 for available CMOS chips.

Bonding Diagrams: Bonding diagrams are provided for each product. Dimensions are given in inches and millimeters. See pages 17-64 through 17-68.

APPLICATIONS INFORMATION

Product descriptions, features and applications information is available for CMOS chips in the packaged product data sheets of this catalog.



ANALOG DEVICES CMOS INTEGRATED CIRCUIT CHIP PROCESS FLOW DIAGRAM "COM" PROCESS

CMOS CHIPS AVAILABLE

Due to limitations imposed on testing and grading devices in chip form, not all packaged product grades or temperature ranges are available at this time as standard product.

Following is a list of CMOS chip standard product offerings which are presently available. Refer to the packaged-product data sheet shown to determine the chip's dc performance characteristics.

LEADLESS CHIP CARRIERS FOR FULLY TESTED AND GUARANTEED PERFORMANCE

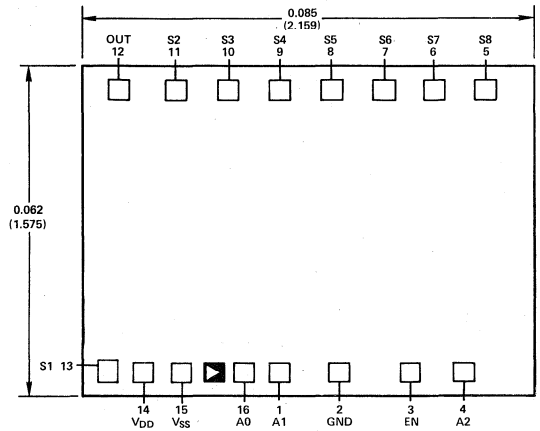
Due to test limitations, it is often difficult (or impossible) to provide the exhaustive testing required to guarantee chips to the equivalent grade packaged-product performance over the MILITARY temperature range.

Consequently, Analog Devices offers many CMOS devices packaged in leadless chip carriers. Chip carriers offer the advantage of fully specified, 100% tested, guaranteed performance in a package not much larger than the chip itself. Contact Analog Devices for further information on products available in chip carriers.

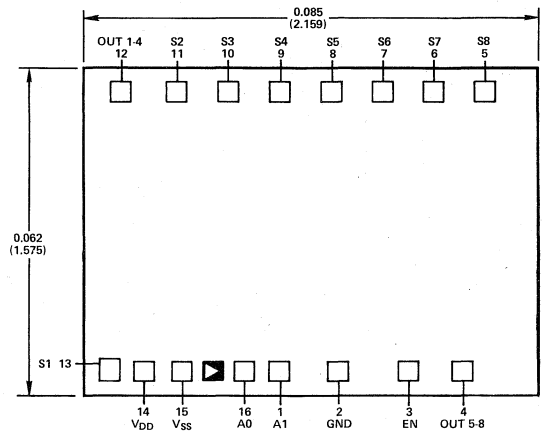
Chip Model Number	Equivalent Packaged Product to Determine dc Performance (Vol. I)	Operating Temperature Range for Rated dc Performance
CMOS MULTIPLEXERS		
AD7501 J CHIP	AD7501JD ; page 16-5	-25°C to +85°C
AD7502 J CHIP	AD7502JD ; page 16-5	-25°C to +85°C
AD7503 J CHIP	AD7503JD ; page 16-5	-25°C to +85°C
AD7506 J CHIP	AD7506JD ; page 16-9	-25°C to +85°C
AD7507 J CHIP	AD7507JD ; page 16-9	-25°C to +85°C
CMOS SWITCHES		
AD7510DI J CHIP	AD7510DIJD ; page 16-13	-25°C to +85°C
AD7511DI J CHIP	AD7511DIJD ; page 16-13	-25°C to +85°C
AD7512DI J CHIP	AD7512DIJD ; page 16-13	-25°C to +85°C
AD7590DI B CHIP	AD7590DIBD ; page 16-21	-25°C to +85°C
AD7591DI B CHIP	AD7591DIBD ; page 16-21	-25°C to +85°C
AD7592DI B CHIP	AD7592DIBD ; page 16-21	-25°C to +85°C
CMOS D/A CONVERTERS		
AD7524 A CHIP	AD7524AD ; page 9-173	-25°C to +85°C
AD7533 A CHIP	AD7533AD ; page 9-197	-25°C to +85°C
AD7541A A CHIP	AD7541A AD ; page 9-211	-25°C to +85°C
AD7542 A CHIP	AD7542AD ; page 9-217	-25°C to +85°C
AD7543 A CHIP	AD7543AD ; page 9-225	-25°C to +85°C
AD7545 A CHIP	AD7545AD ; page 9-233	-25°C to +85°C
CMOS A/D CONVERTERS		
AD7574 A CHIP	AD7574AD ; page 10-151	-25°C to +85°C

BONDING DIAGRAMS

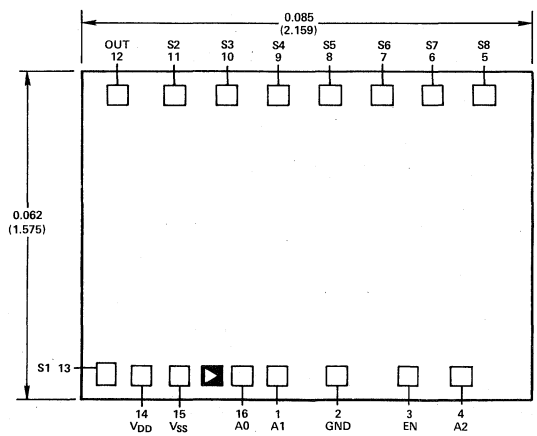
Dimensions shown in inches and (mm).



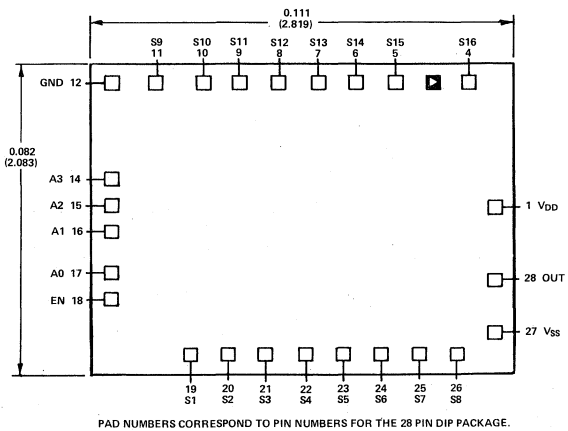
AD7501



AD7502



AD7503



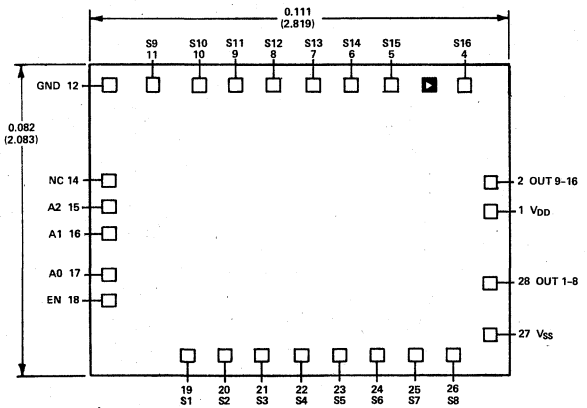
PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 28 PIN DIP PACKAGE.

AD7506

LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

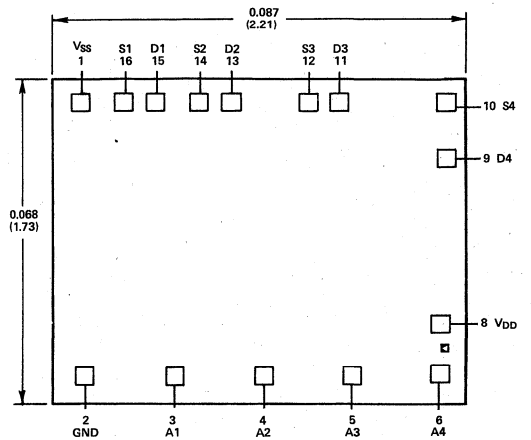
BONDING DIAGRAMS

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 28 PIN DIP PACKAGE.

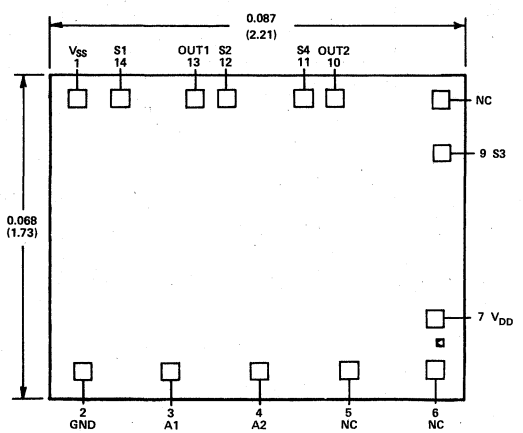
AD7507



NOTE: AD7510DI: SWITCH "ON" FOR ADDRESS "HIGH"
AD7511DI: SWITCH "ON" FOR ADDRESS "LOW"

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 16 PIN DIP PACKAGE.

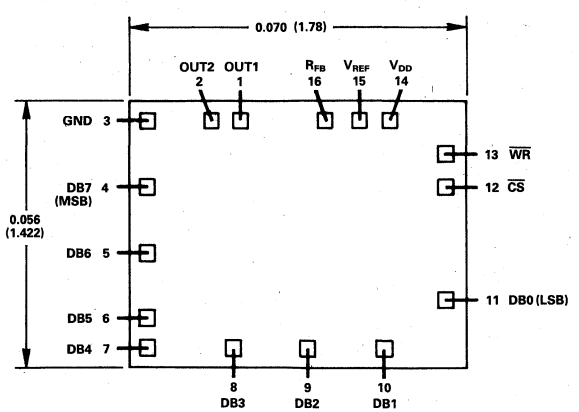
AD7510, 11



NOTE: AD7512DI: ADDRESS "HIGH" MAKES
S1 TO OUT1 AND S3 TO OUT2

PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE 16 PIN DIP PACKAGE.

AD7512



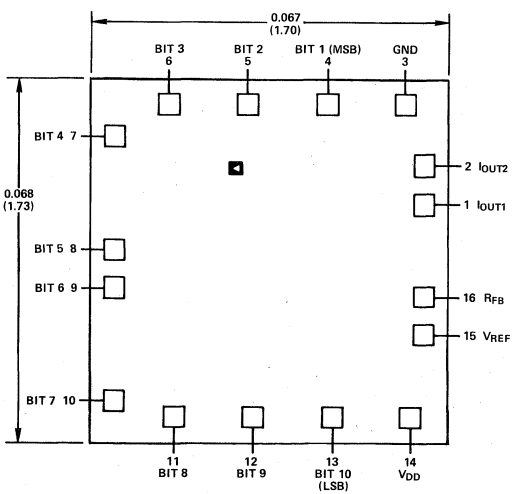
AD7524

17

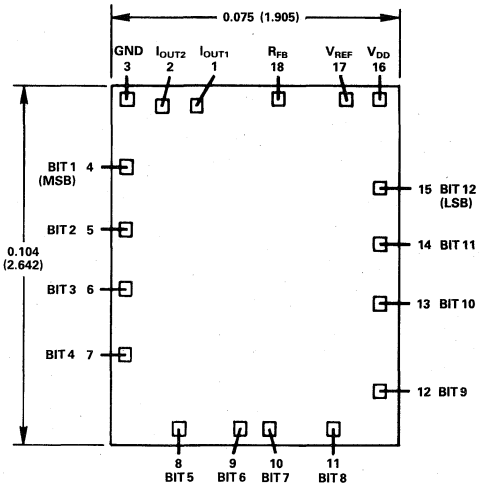
LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

BONDING DIAGRAMS

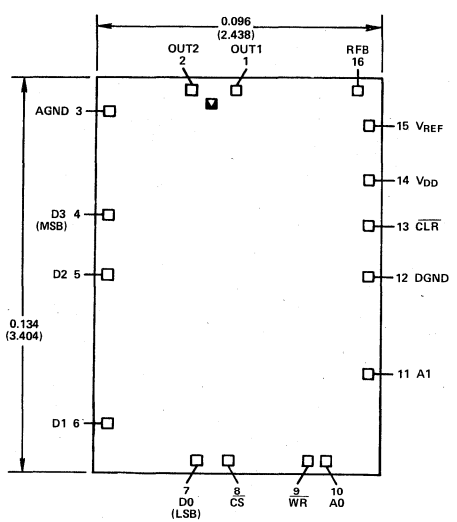
Dimensions shown in inches and (mm).



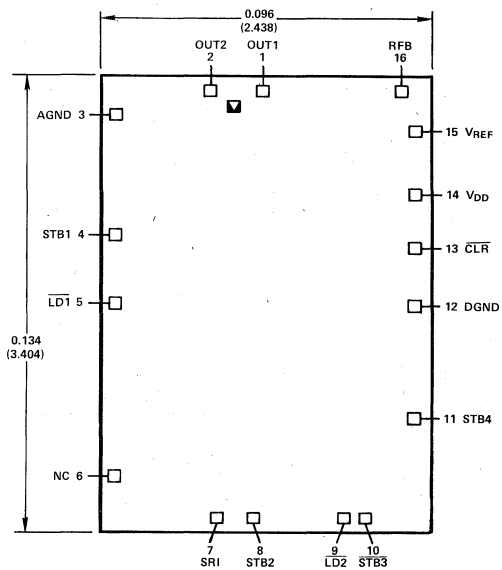
AD7533



AD7541A



AD7542

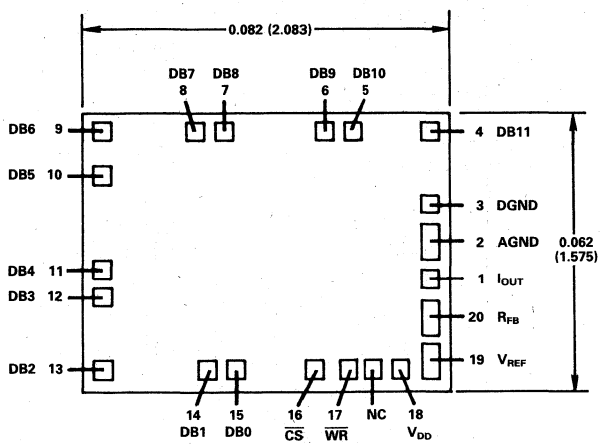


AD7543

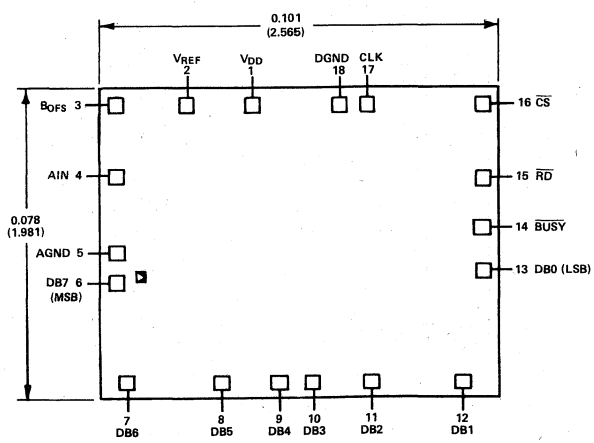
LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

BONDING DIAGRAMS

Dimensions shown in inches and (mm).



AD7545



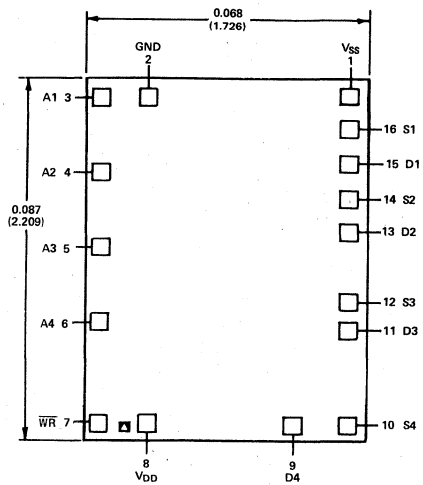
AD7574

LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

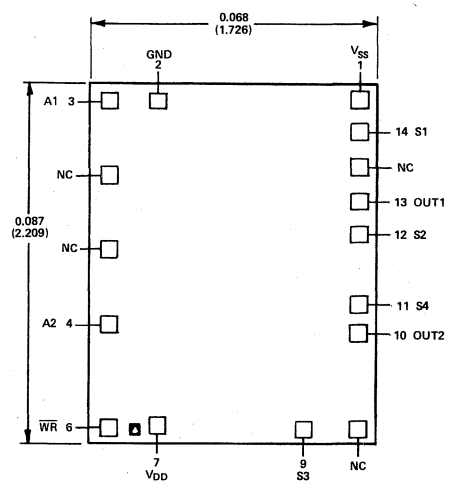
17

BONDING DIAGRAMS

Dimensions shown in inches and (mm).



AD7590, 91

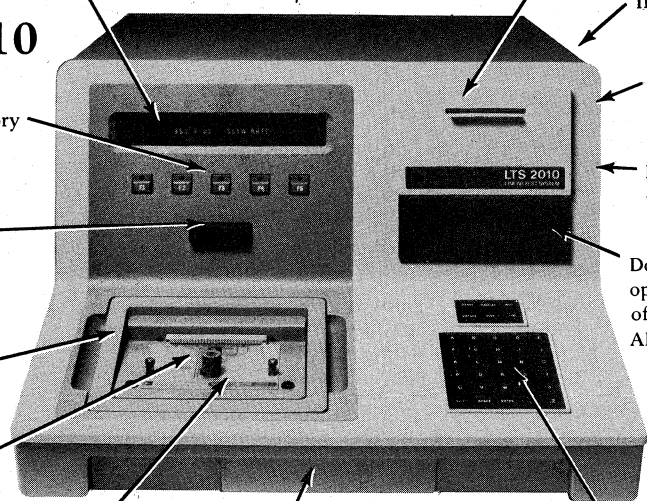


AD7592

LINES FROM BONDING PADS IN ALL DIAGRAMS DO NOT INDICATE BOND WIRES

Component Test Systems

TEST LINEAR, DIGITAL, DISCRETE & PASSIVE DEVICES WITH 16-BIT ACCURACY



Large easy-to-read programmable display for pass/fail information, messages, binning, grading, etc.

Uni-directional RS-232 port for optional printer.

Integral printer for permanent record of test results.

IEEE 488 port.

LTS-2010

Function switches can be programmed to select category from prompt on display.

Bi-directional RS-232 port for communicating with any RS-232 device.

Handler interface for handler control signals.

Go button—Operator installs device in the socket and merely pushes the button. The LTS-2010 does the rest.

Double sided floppy disk for operating system, mass storage of data, user programs, and ADI supplied programs.

Plug-in socket assembly.

Sockets for specific device mounted on plug-in P.C. socket board.

Keyboard for entering data to fill-in-the-blanks on ADI supplied device programs.

Socket P.C. board for specific device.

Plug-in Family Board Module (i.e., A/D, Op Amp, D/A, Digital, Discrete, Passive)

THE LTS SYSTEM CONCEPT

The LTS systems are easy-to-use, flexible component test systems that allow you to test any component to the manufacturer's own specifications, linear, digital, passive and discrete devices. The system also offers such features as datalogging, statistical analysis, yield analysis and two RS-232 interfaces, IEEE interface and a handler interface.

The computing power of the LTS-systems lies in their 16-bit central processing unit. The microprocessor incorporates a minicomputer instruction set which includes hardware multiply and divide as well as 15 prioritized interrupts for the system keypad, function switches, floppy disk drive, and the IEEE 488 interface.

A real time, 3MHz, four-phase crystal stabilized system clock generates system timing, allowing the implementation of a real time clock. The system memory includes 60K bytes of dynamic RAM, of which 32K bytes are available for program generation by the user.

The LTS-systems not only provide for several data output formats—data log, yield analysis or statistical analysis—they also provide a choice of data display. If desired, the data may be presented via the single line LED display, the integral 20-column thermal printer, through either of the RS-232 ports or the IEEE port. (All data outputs are standard features on the LTS-2000 series.)

LTS-2010, 2012, 2015

The LTS-2000 series are the first benchtop testers that are programmable in BASIC, as well as "Fill-in-the-Blanks" programming, and their 16-bit CPU and 64K bytes of memory offer a new level of programmable sophistication.

Far more than just comprehensive production testers, they can handle complex engineering analysis, and even incoming inspection. They are the first systems that can provide all the capabilities of today's large, centralized test systems at a cost that is approximately one-third the "bit system" price.

The LTS-2000 series not only provide the flexibility of distributed or decentralized testing, they allow for cost-effective multiple system purchases. And they increase overall test reliability, since the threat of a single big system failure is eliminated in a distributed testing environment.

LTS-2010, Single Disk Drive
LTS-2012, Dual Disk Drives
LTS-2015, Dual Disk Drives and Numerics Processor

LTS SPECIFICATIONS

MEASUREMENT ACCURACY

High Accuracy	±(0.0015% of Reading +0.025% of Range +100μV)
Direct	±(0.025% of Reading +0.025% of Range +100μV)
Null and Difference	±(0.025% of Reading +0.025% of [Diff Range + Null Range] +100μV)
Input Voltage Range	±10V (64 Different Ranges)

REFERENCE DAC

Range	Resolution	Software Corrected Accuracy
0 to 10V	2.5mV	RDVO ± 150μV
-5V to 5V	2.5mV	RDVO ± 150μV
-10V to 10V	5mV	RDVO ± 300μV

SYSTEM REFERENCE

Short Term	10V Adjustable in hardware or software
Long Term	10V ±50ppm/1000 hrs, noncumulative

SOURCES

Source	Voltage Range	Resolution	Software Corrected Accuracy
SA	0 to 20V	±0.1V	SAVO ± 0.05V
SB	0 to 20V	±0.1V	SBVO ± 0.05V
SC	0 to -20V	±0.1V	SCVO ± 0.05V
SD	0 to -20V	±0.1V	SDVO ± 0.05V
TH	0 to 10V	±0.05V	THVO ± 0.025V
SR	-10V to 10V	±0.001V	SRVO ± 0.0005V

Source	Current Range	Accuracy of Measurement
SA	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SB	-10mA to 150mA	±(2.5% of Reading + 10μA/V + 15μA)
SC	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
SD	10mA to -150mA	±(2.5% of Reading + 10μA/V + 15μA)
TH	-10mA to +10mA	±(0.5% of Reading + 10μA)
SR	-10mA to +10mA	±(0.5% of Reading + 10μA)

OPERATING TEMPERATURE

At Rated Accuracy after 1 hr warm-up
0 to 40°C
32°F to 104°F

OPERATING VOLTAGE

105V ac to 125V ac @ 50Hz to 60Hz
210V ac to 250V ac @ 50Hz to 60Hz

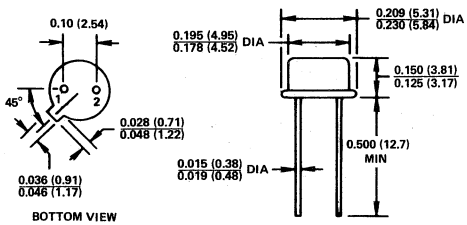
Specifications subject to change without notice.

Package Information

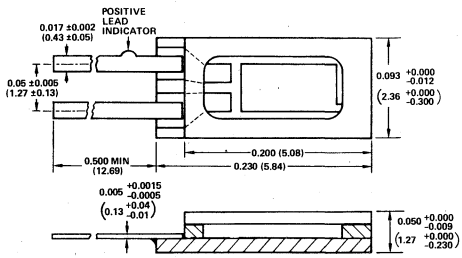
Contents

2-PIN PACKAGES

H2A
2-Lead Metal Can Package

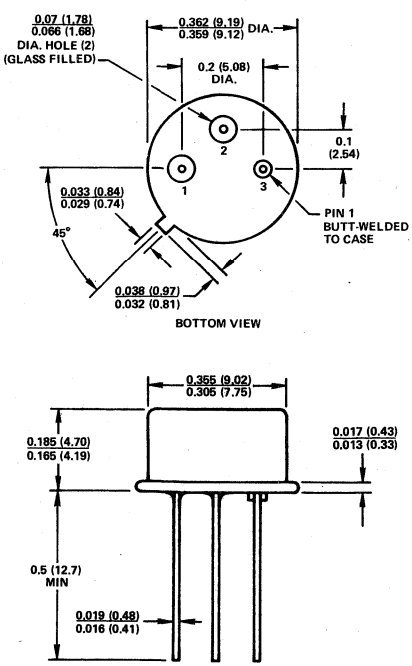


F2A
2-Lead Flat Package

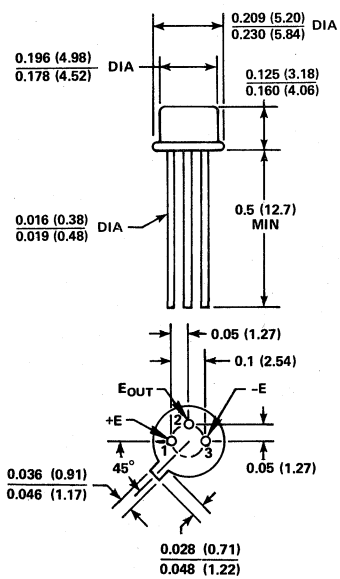


3-PIN PACKAGES

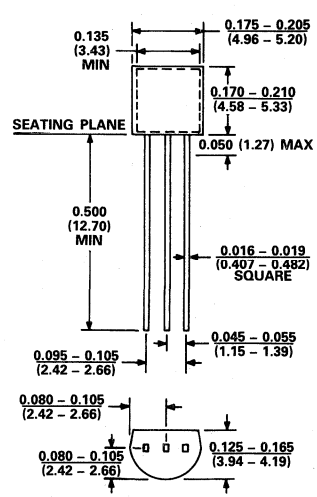
TO-5 Package



TO-52 Package



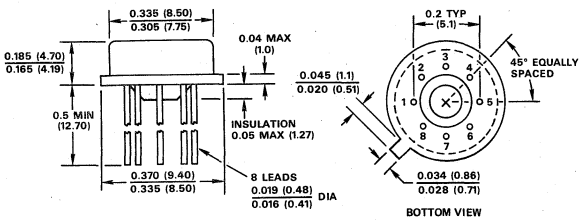
TO-92 Package



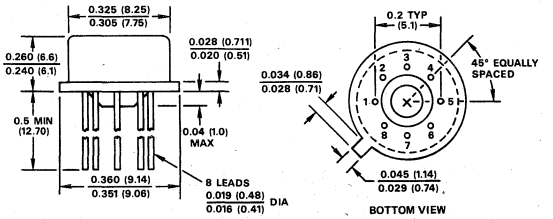
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

8-PIN PACKAGES

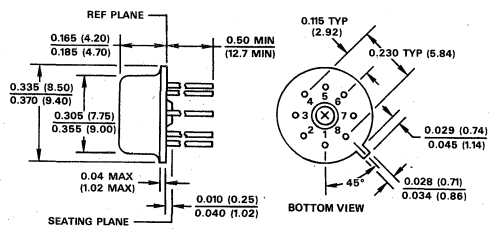
TO-99 Package



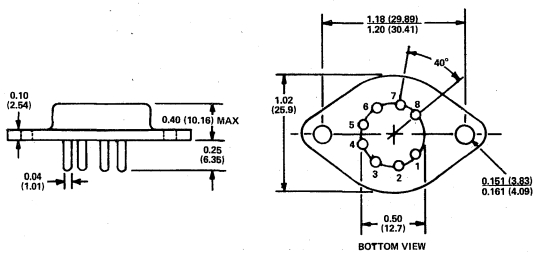
H08A Package (TO-99 Style)
(JEDEC REF MO-002AB)



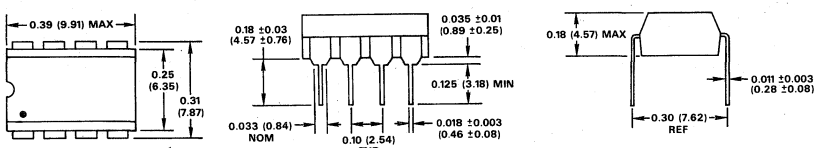
H08B Package (TO-99 Style)
(JEDEC REF MO-006AH)



H08C Package (TO-3 Style)

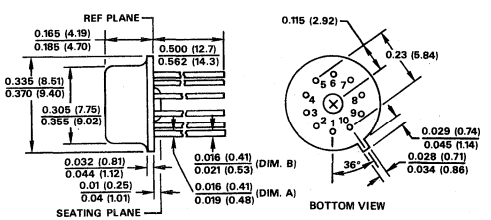


N8A Package



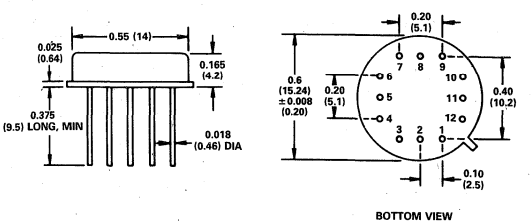
10-PIN PACKAGE

TO-100 Package



12-PIN PACKAGE

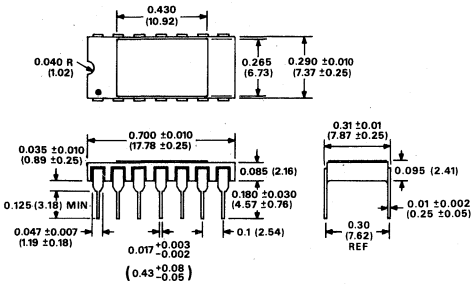
H12A
12-Lead Metal Can Package
(TO-8 Style)



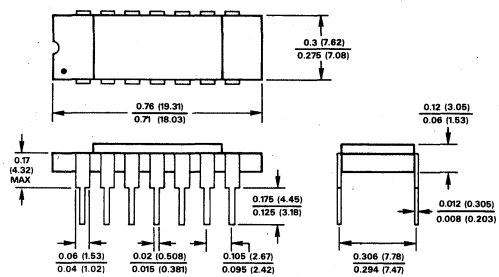
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

14-PIN PACKAGES

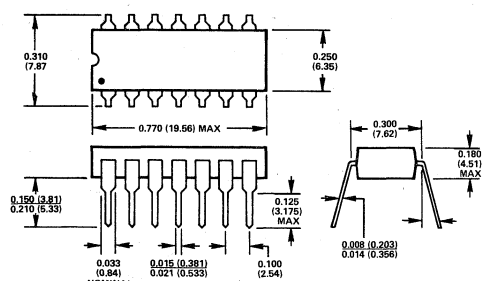
D14A
14-Lead Ceramic Package



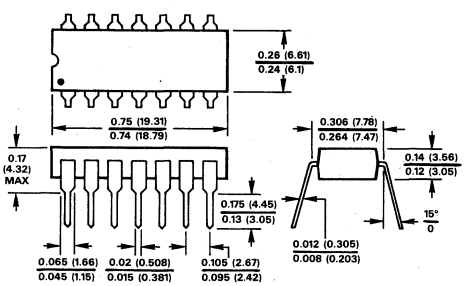
D14B
14-Lead Ceramic DIP Package



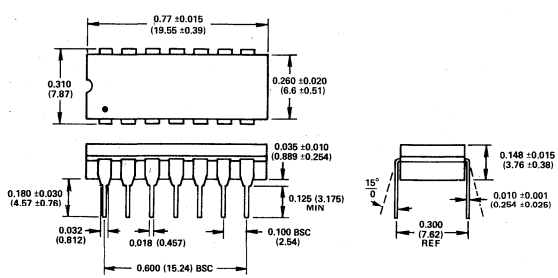
N14A
14-Pin Plastic DIP Package



N14B
14-Pin Plastic Package



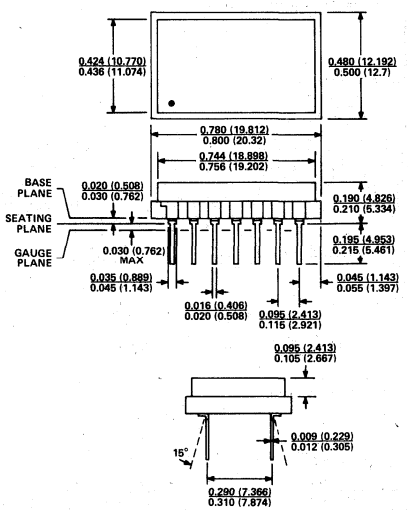
Q14A
14-Pin CERDIP Package



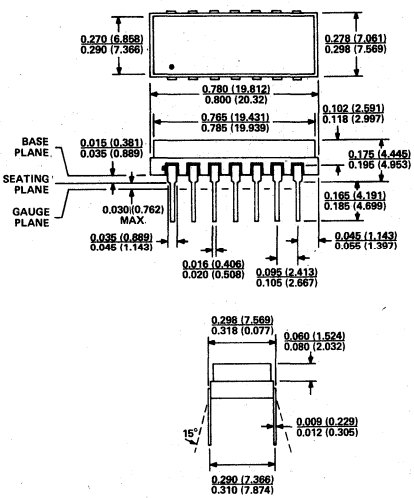
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

14-PIN PACKAGES
(Continued)

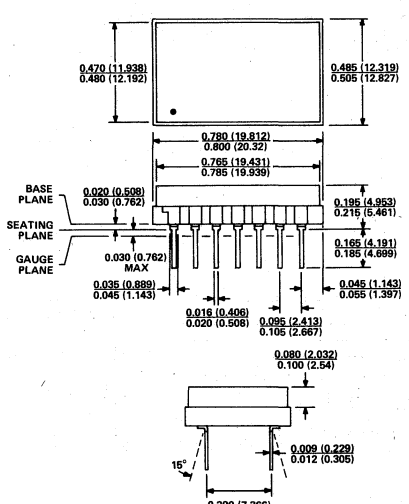
HY14A
14-Pin Hybrid Package



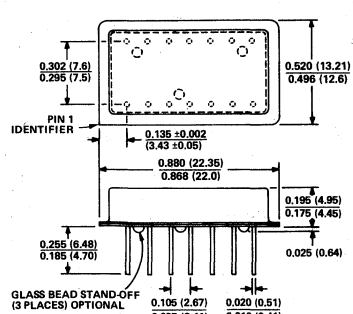
HY14B
14-Pin Hybrid Package



HY14C
14-Pin Hybrid Package



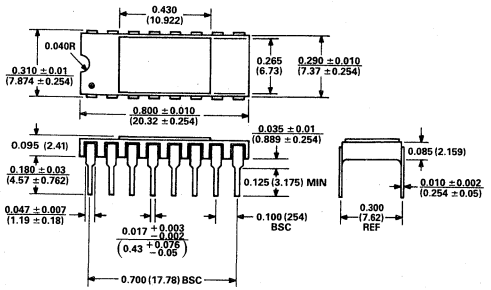
HY14D
14-Pin Metal DIP Package



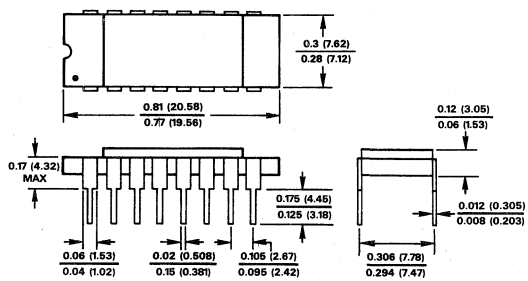
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

16-PIN PACKAGES

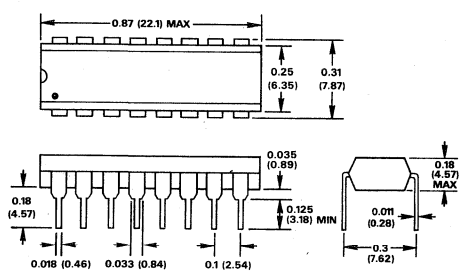
D16A
16-Pin Ceramic DIP Package



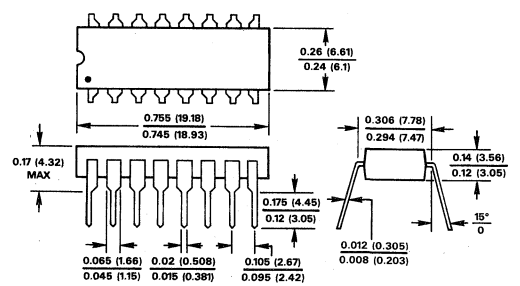
D16B
16-Pin Ceramic DIP Package



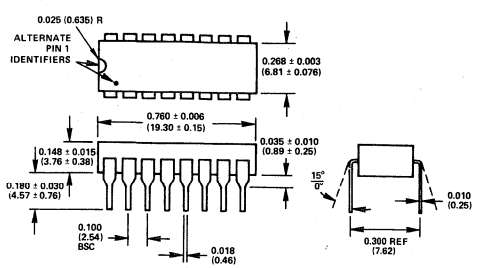
N16A
16-Pin Plastic DIP Package



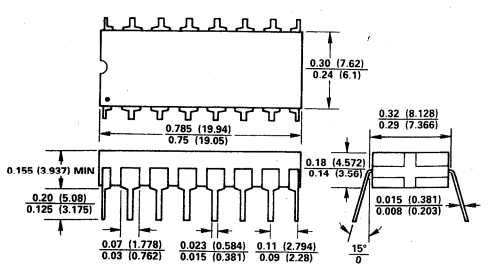
N16B
16-Pin Plastic DIP Package



Q16A
16-Pin CERDIP Package



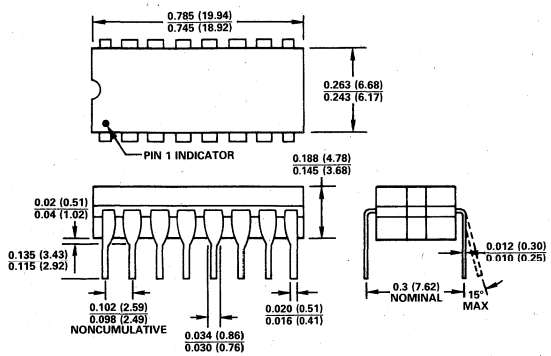
Q16B
16-Pin CERDIP Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

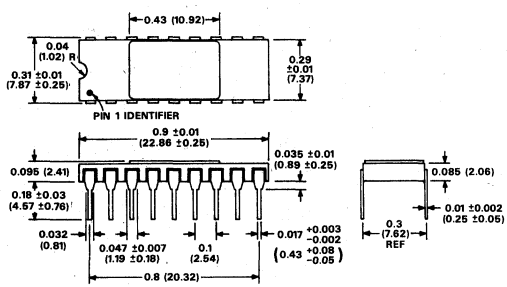
16-PIN PACKAGES
(Continued)

Q16C
16-Pin CERDIP Package

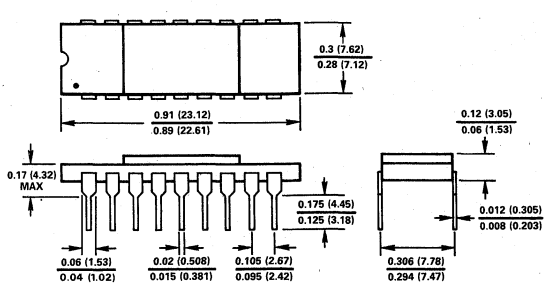


18-PIN PACKAGES

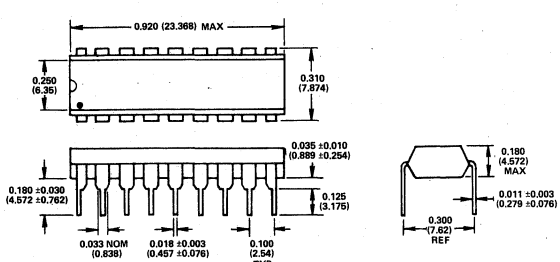
D18A
18-Pin Ceramic DIP Package



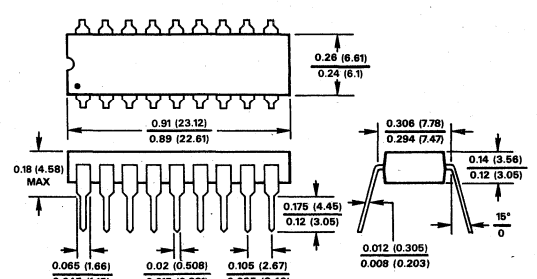
D18B
18-Pin Ceramic DIP Package



N18A
18-Pin Plastic DIP Package



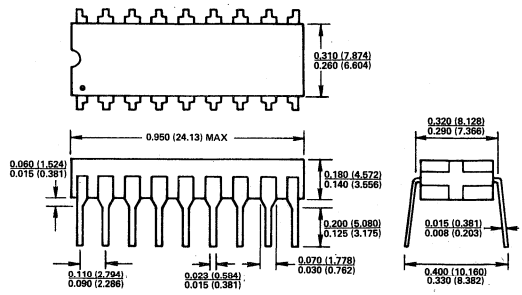
N18B
18-Pin Plastic Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

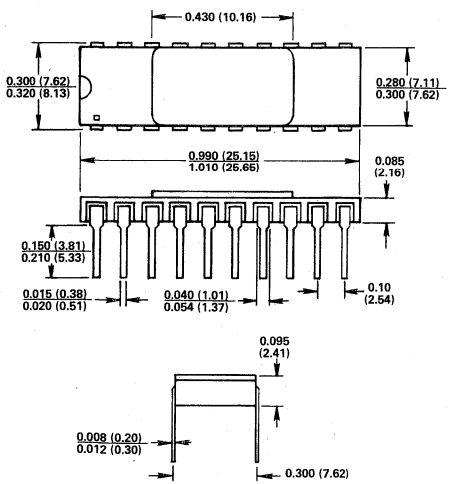
18-PIN PACKAGES
(Continued)

Q18A
18-Pin CERDIP Package

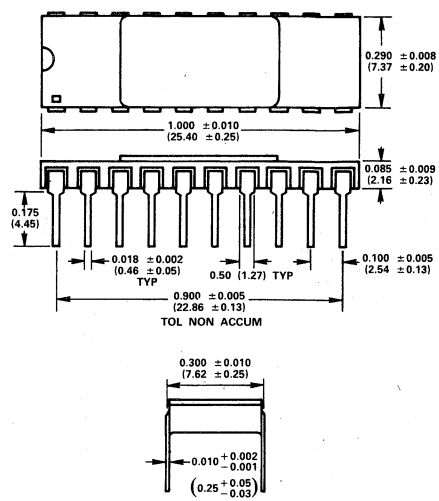


20-PIN PACKAGES

D20A
20-Pin Ceramic DIP Package



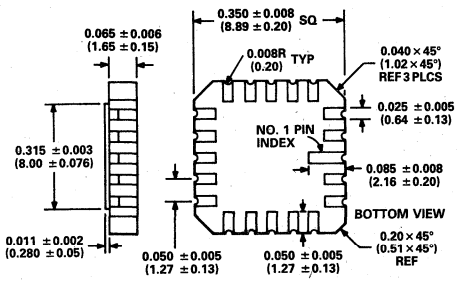
D20B
20-Pin Ceramic DIP Package



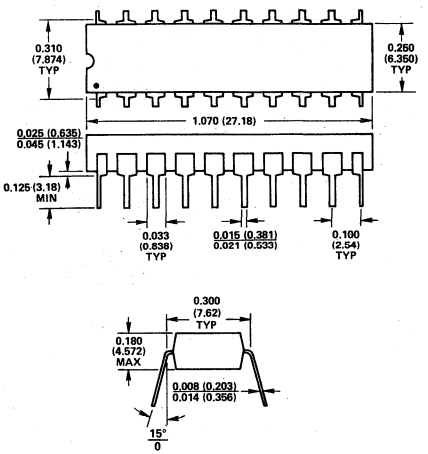
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

20-PIN PACKAGES
(Continued)

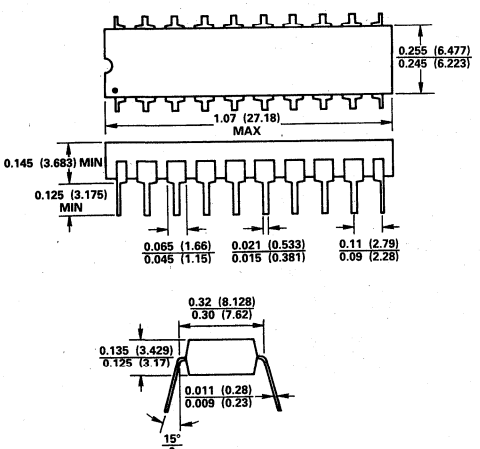
E20A
20-Terminal Leadless Chip Carrier



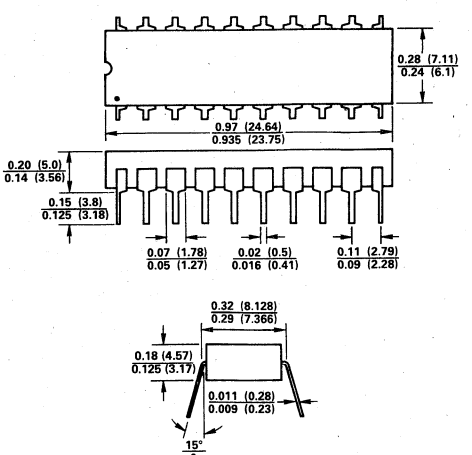
N20A
20-Pin Plastic DIP Package



N20B
20-Pin Plastic DIP Package



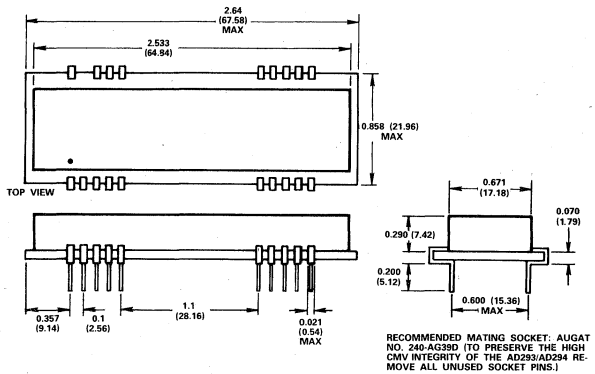
Q20B
20-Pin CERDIP Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

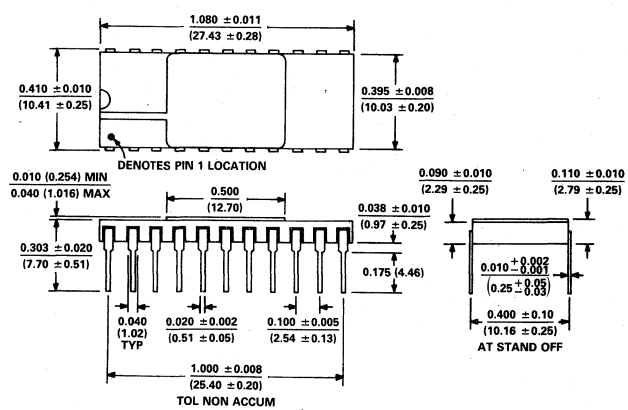
20-PIN PACKAGES
(Continued)

HY20A
20-Pin Hybrid Package



22-PIN PACKAGE

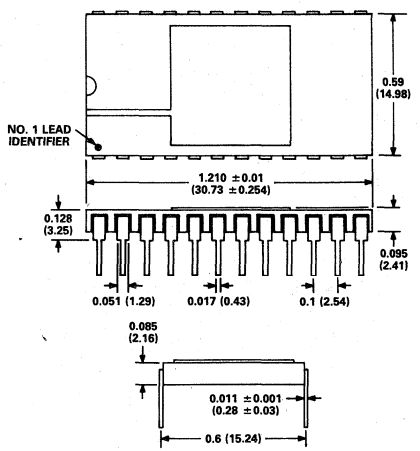
D22A
22-Pin Ceramic DIP Package



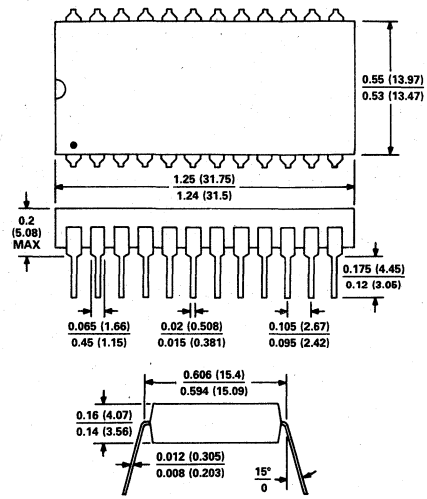
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

24-PIN PACKAGES

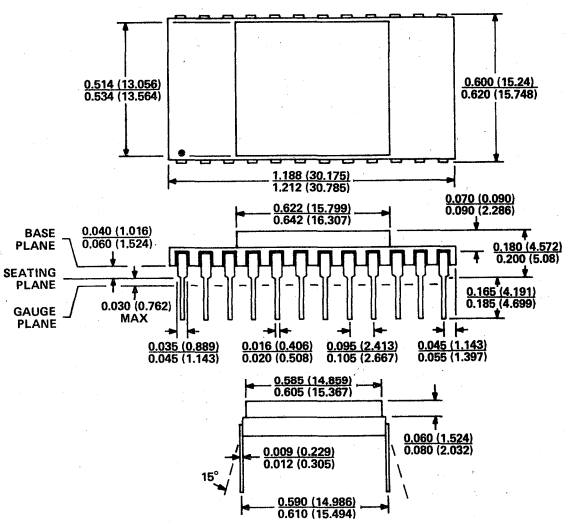
D24A
24-Lead Ceramic DIP Package



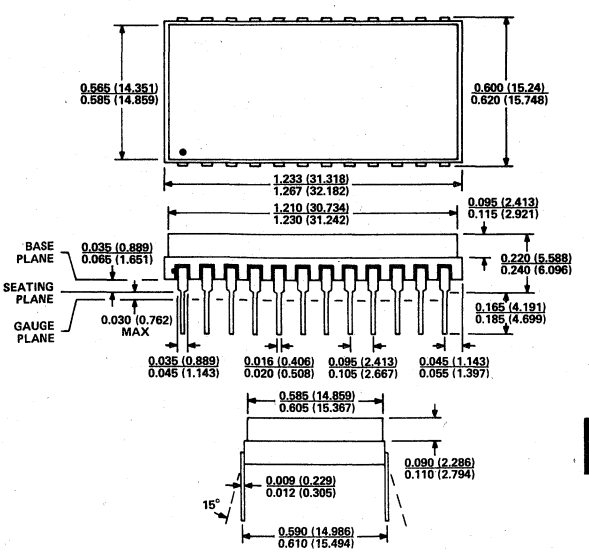
N24A
24-Lead Plastic Package



HY24A
24-Pin Hybrid Package



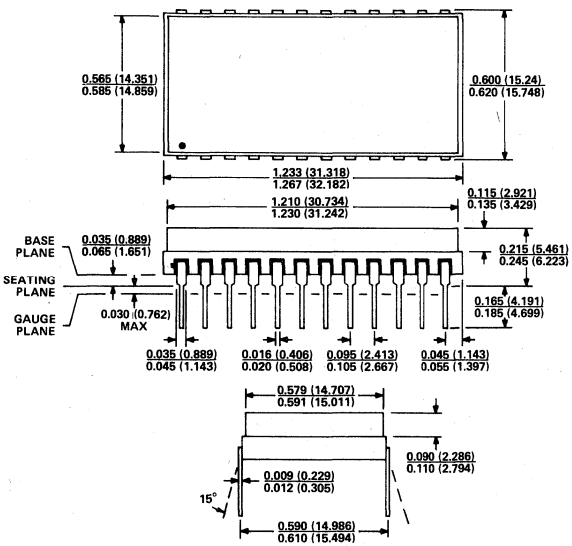
HY24B
24-Pin Hybrid Package



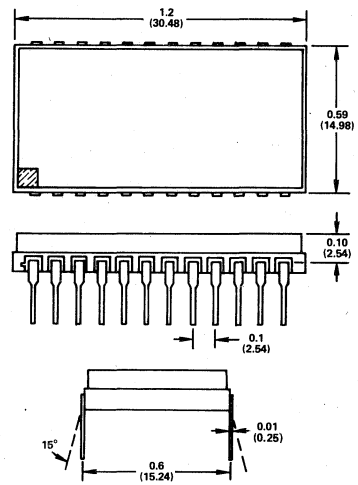
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

24-PIN PACKAGES
(Continued)

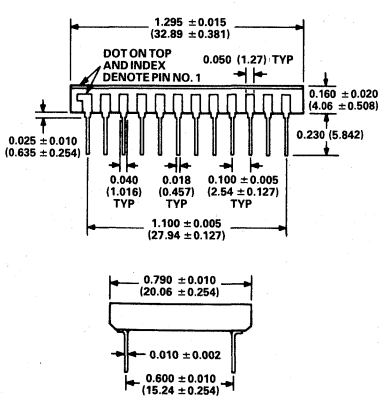
HY24C
24-Pin Hybrid Package



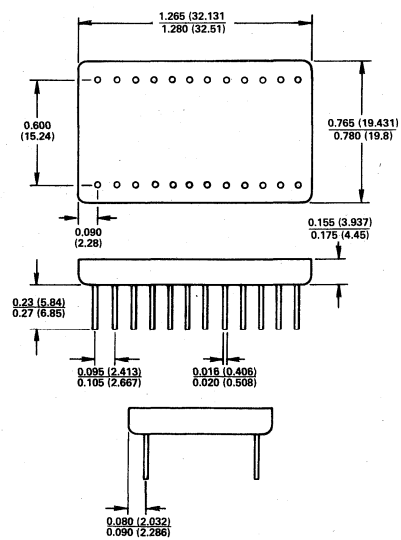
HY24D
24-Pin Hybrid Package



HY24E
24-Pin Hybrid Package



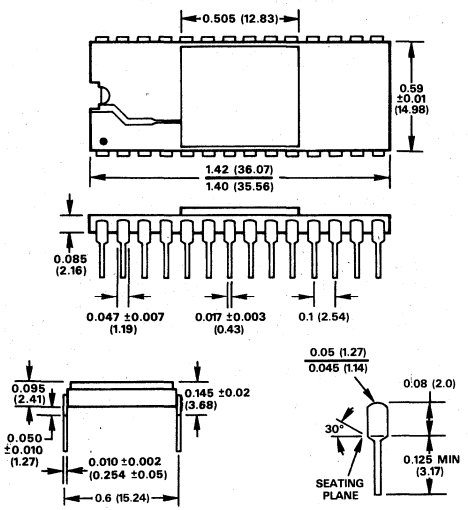
HY24G
24-Pin Hybrid Package



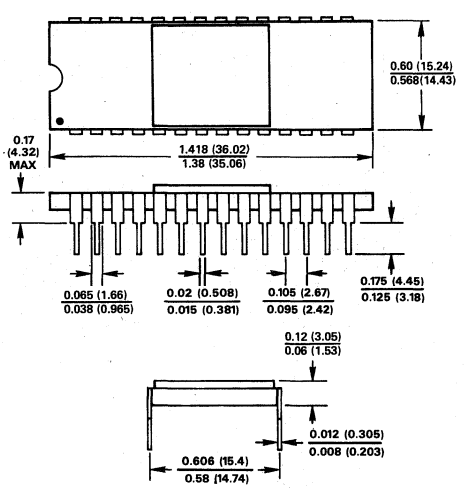
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

28-PIN PACKAGES

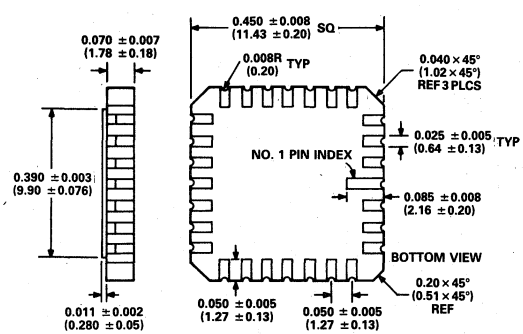
D28A
28-Pin Ceramic DIP Package



D28B
28-Pin Ceramic Package



E28A
28-Terminal Leadless Chip Carrier



N28A
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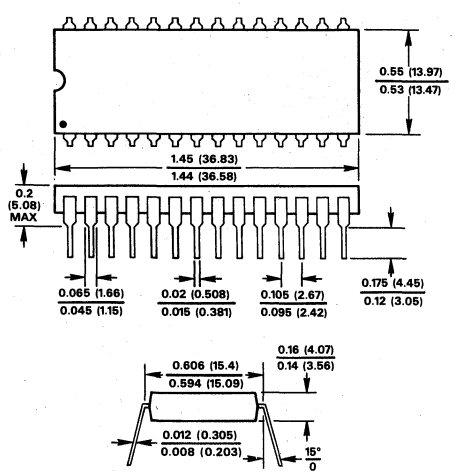
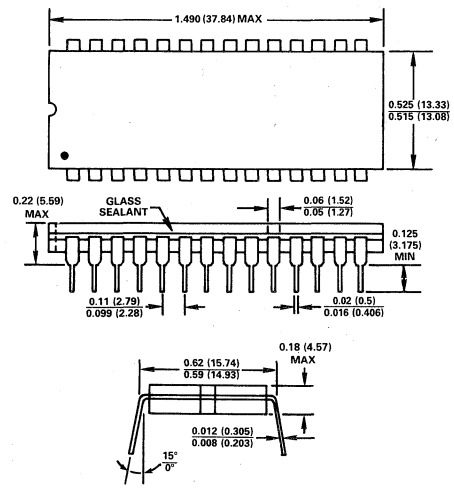


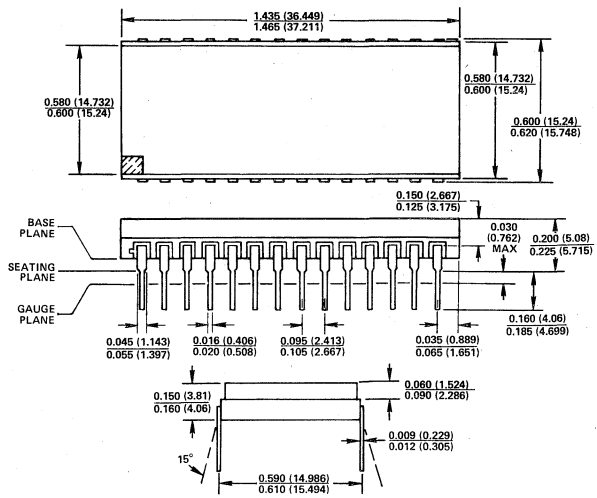
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

28-PIN PACKAGES
(Continued)

Q28A
28-Pin CERDIP Package

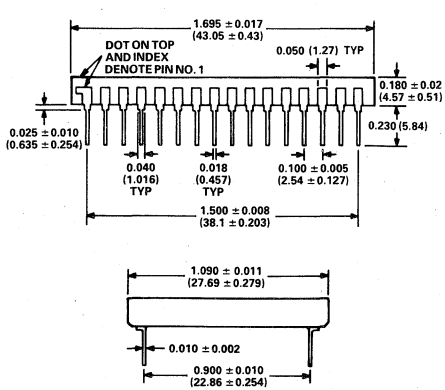


HY28B
28-Pin Hybrid Package

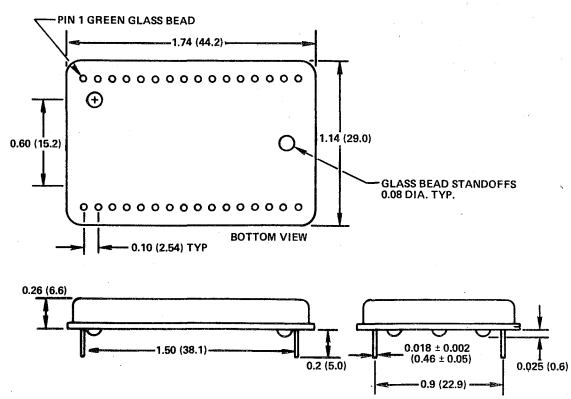


32-PIN PACKAGES

HY32A
32-Pin Hybrid Package



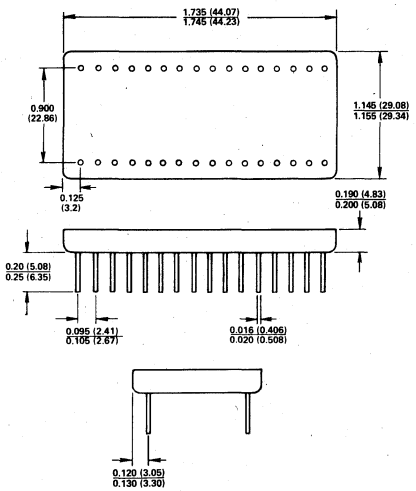
HY32B
32-Pin Hybrid Package



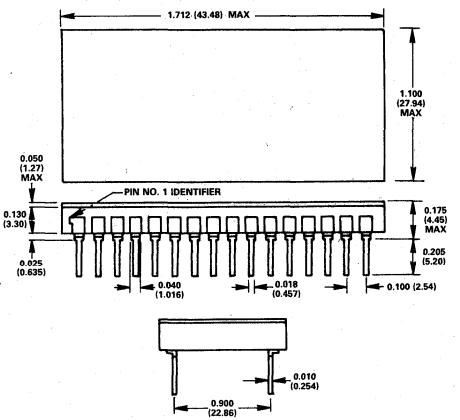
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

32-PIN PACKAGES
(Continued)

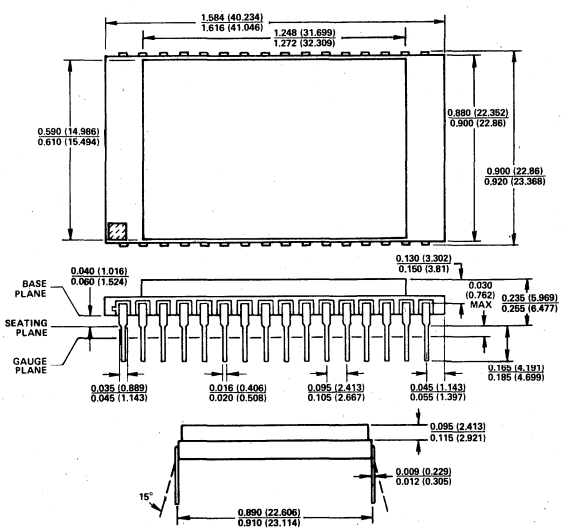
HY32C
32-Pin Hybrid Package



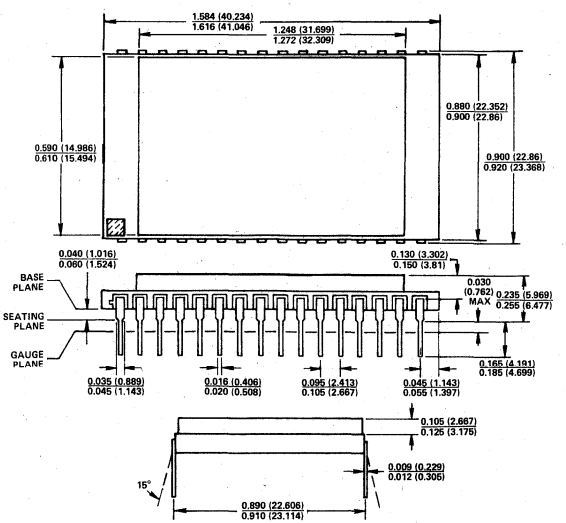
HY32D
32-Pin Metal DIP Package



HY32E
32-Pin Hybrid Package



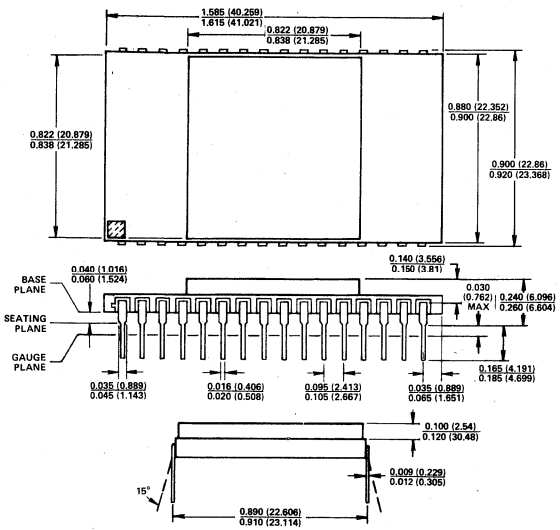
HY32F
32-Pin Hybrid Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

32-PIN PACKAGES
(Continued)

HY32G
32-Pin Hybrid Package



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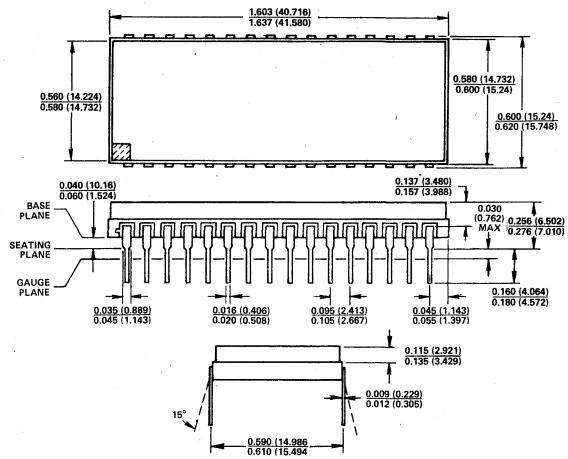
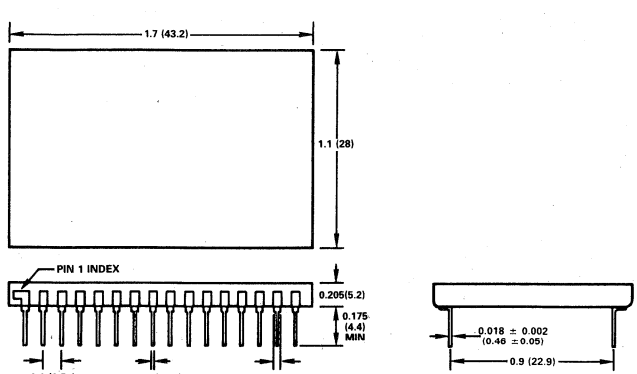
32-Pin Hybrid Package



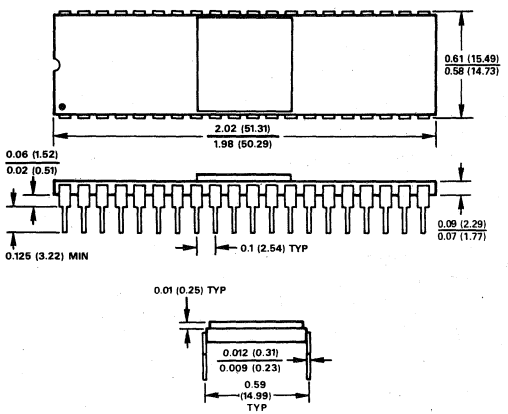
HY32J
32-Pin Hybrid Package



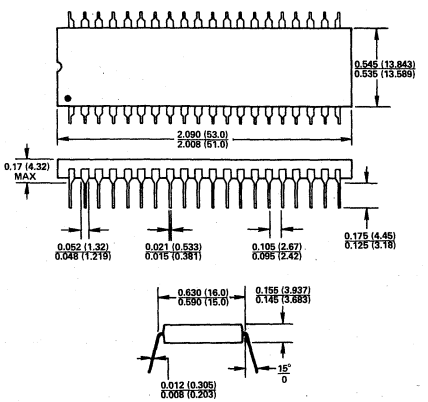
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

40-PIN PACKAGES

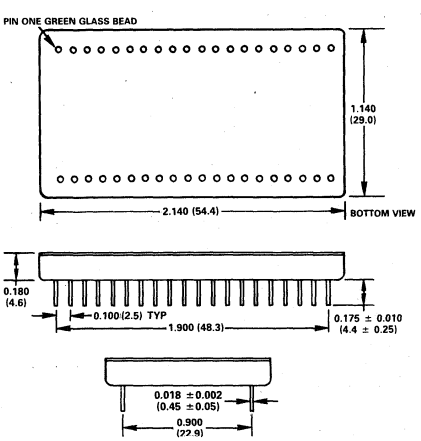
D40A
40-Pin Ceramic DIP Package



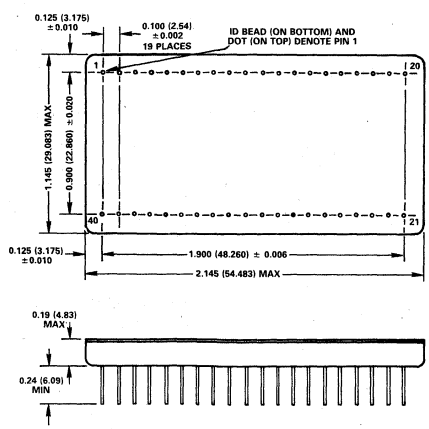
N40A
40-Pin Plastic DIP Package



HY40A
40-Pin Hybrid Package



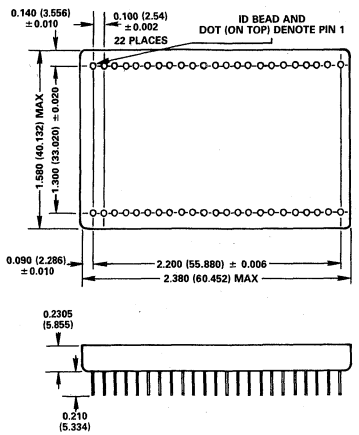
HY40B
40-Pin Hybrid Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

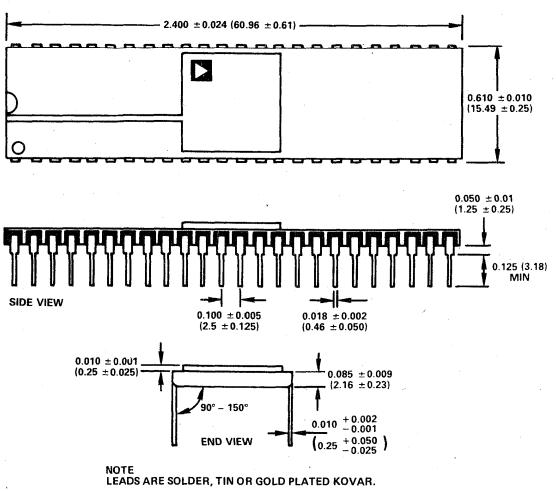
46-PIN PACKAGE

HY46A
46-Pin Hybrid Package



48-PIN PACKAGE

D48A
48-Pin DIP Package

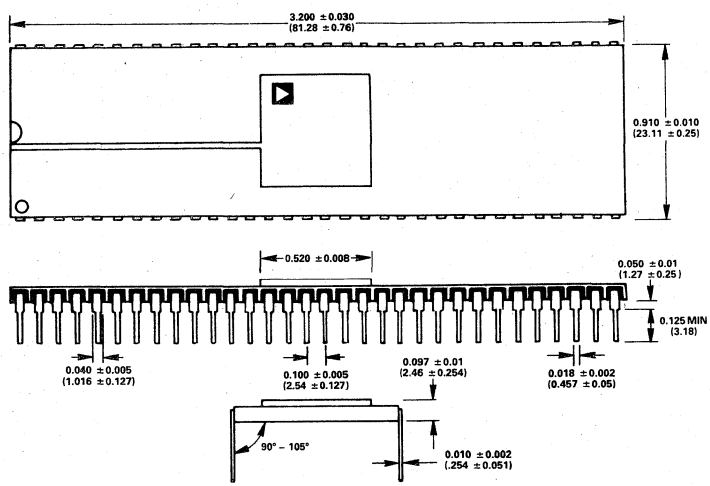


NOTE
LEADS ARE SOLDER, TIN OR GOLD PLATED KOVAR.

Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

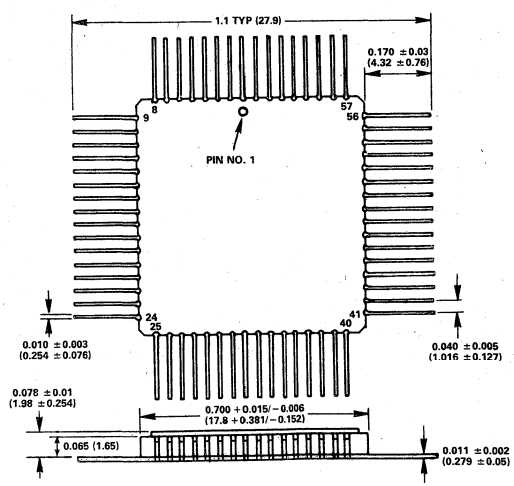
64-PIN PACKAGES

D64A
64-Pin Dual-In Line Package



NOTE
LEADS ARE SOLDER, TIN OR GOLD PLATED KOVAR.

F64A
64-Pin Flat Pack Package

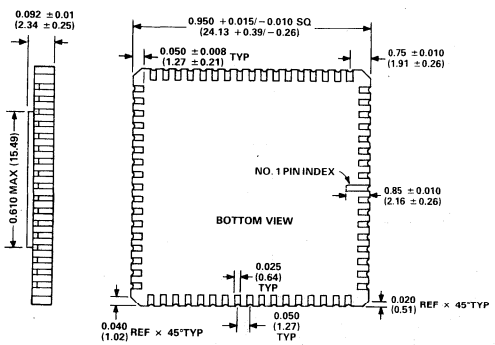


*EQUIVALENT FLAT PACK AND DIP PIN NUMBERS
PROVIDE THE SAME FUNCTION.

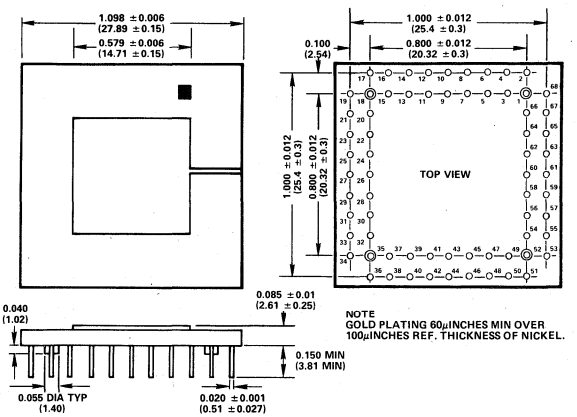
Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

68-PIN PACKAGES

E68C
68-Terminal Leadless Chip Carrier

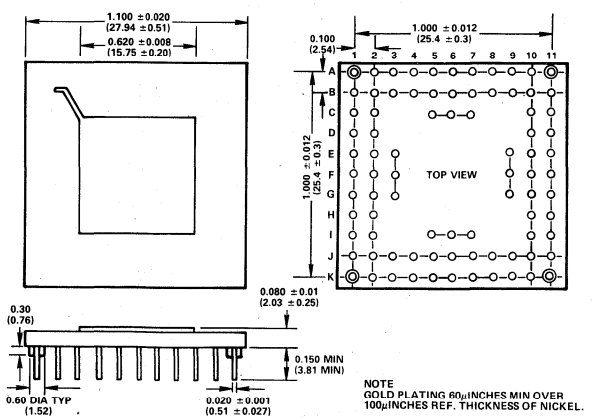


G68A
68-Pin Grid Array Package



84-PIN PACKAGE

G84A
84-Pin Grid Array Package



Dimensions shown in inches and (mm).
Lead No. 1 Identified by Dot or Notch.

Application Notes

Contents

How to Select Operational Amplifiers

INTRODUCTION

In selecting the right device for a specific application, you should have clearly in mind your design objectives and a firm understanding of what published specifications mean. Beyond this, you should detail the significant variables that are pertinent to your application. The purpose of this section is to put these many decision factors into perspective to help you make the most meaningful buying decisions.

To properly choose an operational amplifier for any given set of requirements, the designer must have:

1. *A complete definition of the design objectives.* Signal levels, accuracy desired, bandwidth requirements, circuit impedance, environmental conditions and several other factors must be well defined before selection can be effectively undertaken.

2. *Firm understanding of what the manufacturer means by the numbers published for the parameters.* Frequently, any two manufacturers may have comparable published specifications, which may have been arrived at using differing measurement techniques. This creates a pitfall in op amp selection. To avoid these difficulties, the designer must know what the published specifications mean and how these parameters are measured. He then must be able to translate these published specifications in terms meaningful to his design requirements. In the following discussion, Analog Devices provides the designer: 1) a checklist which he can apply to his application to assure that all significant factors are taken into account; 2) meaningful definitions for each of our published specifications; and 3) illustrations of how the requirements of his design are translated in terms of these specifications to help make an effective and economical choice.

APPLICATION CHECKLIST

By way of an application checklist, the designer will need to account for the following:

Character of the application: The character of the application (inverter, follower, differential amplifier, etc.) will often influence the choice of amplifier. Chopper stabilized amplifiers, for example, are not generally applicable where differential inputs are required.

Accurate description of the input signal: It is extremely important that the input signal be thoroughly characterized. Is the input a voltage source or current source? Range of amplitude? Source impedance? Time/frequency characteristics?

Environmental conditions: What is the maximum range of temperature, time, and supply voltage over which the circuits must operate (to the required accuracy) without readjustment?

Accuracy desired: The accuracy requirement determines the extent to which the foregoing considerations are critical, and ultimately points the way to a device (or series of devices) which are acceptable. Accuracy must, of course, be defined in terms meaningful to the application with regard to bandwidth, dc offset, and other parameters.

SELECTION PROCESS

In general, the objective of amplifier selection should be to choose the least expensive device which will meet the physical, electrical, and environmental requirements imposed by the application. This suggests that a "General Purpose" amplifier will be the best choice in all applications where the desired performance requirements can be met. Where this is not possible, it is generally because of limitations encountered in two areas – bandwidth requirements, and/or offset and drift parameters.

To make it easier to relate bandwidth requirements with the drift and offset characteristics, a capsule view of bandwidth considerations precedes the dc discussions below. The reader is then returned to an expanded discussion of gain-bandwidth considerations.

Gain Bandwidth Considerations, A Capsule View

Although all selection criteria must be met simultaneously, determination of the bandwidth requirements is a logical starting point because:

A) If dc information is not of interest, a suitable

blocking capacitor can usually be connected at the amplifier input and all of the "drift" specifications may be ignored, and

B) Where high frequency (>10MHz) characteristics are of primary importance, the choice will be limited to those amplifiers designated "Wide Bandwidth/Fast Settling."

Where dc information is required and where frequency requirements are relatively modest (full power response below 100kHz, unity gain of less than 1.5MHz) other criteria will probably influence the final choice. It is important, however, to choose an amplifier with which an adequate value of loop gain is assured (at the maximum frequency of interest) to obtain the desired accuracy. Loop gain is the excess of open loop gain over closed loop gain, and is responsible for the diminishing error due to fluctuations in the open loop gain due to time, temperature, etc. Typically, a loop gain of 100 will yield an error of no more than 1%, 0.1% from loop gain of 1000, etc. Where undistorted response is required, the specifications for full linear response and slewing rate should be chosen such that they are not exceeded at the highest frequency of operation.

Offset and Drift Considerations

In the majority of op-amp applications, final selection is determined by the dc offset and drift characteristics. To undertake amplifier selection in these cases, it is necessary to translate the requirements listed above as follows. (It is assumed that bandwidth requirements have been established at this point.)

1. *What input impedance must the circuit present to the signal source?* This depends primarily on the source impedance, R_S, and the amount of loading error which is acceptable. Most amplifier circuits are designed around either the inverting or noninverting circuit of Figure 1. The choice is often made between the two to accommodate the impedance requirement. Input impedance for the inverting circuit is approximately equal to the summing impedance, R_i and the upper limit on the magnitude of R_i is determined by the allowable drift error because of input bias current as discussed below. The noninverting circuit offers inherently higher input impedance than the inverting circuit (due to "bootstrapping" feedback) and in this case input impedance is approximately equal to the common mode impedance of the amplifier R_{CM}.

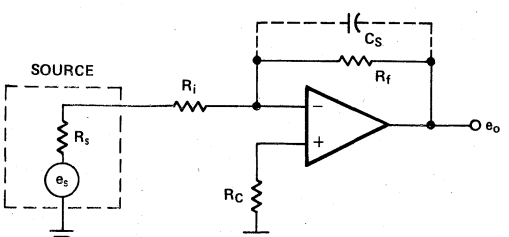
2. *How much drift error can be tolerated?* The question is related to the input signal level, e_s, and the required accuracy. For example, to amplify or otherwise manipulate a dc input signal of one volt with an accuracy of 0.1%, the offset drift error, V_d, must be one millivolt or less. (This assumes that other sources of error such as input loading, noise and gain error have already been allowed for.) By the same reasoning, the allowable drift error for a 1 volt signal and 0.01% accuracy would be 100μV.

When this has been defined, the allowable limits of offset voltage (e_{os}), bias current (i_b), and difference current can be calculated by the equations of Figure 1.

Figure 1 gives the equations which relate offset voltage (e_{os}), bias current (i_b), difference current (i_d) and the external circuit impedances to the drift error, V_d, for both the inverting and the noninverting circuits. From these equations it can be seen how the input impedance requirements of the foregoing paragraphs are related to the drift error.

For example, in the case of the inverting circuit, an offset error voltage, i_bR_i, is generated by the bias current flowing through the summing impedance. This error increases for increasing R_i. Since R_i also sets the input impedance, there is a conflict between high input impedance and low offset errors. Likewise, for a given offset error, higher values for R_i can be used with an amplifier which has lower bias current.

Where it will otherwise function properly, the noninverting circuit generally makes a better choice for high input impedance circuits. Also, for the same source and input impedance requirement, a given amplifier will generate lower offset errors for the noninverting circuit than for the inverting circuit. This is so because the bias current flows only through R_s for the noninverter and this will always be less than the input impedance, R_i, of the inverter. Input imped-



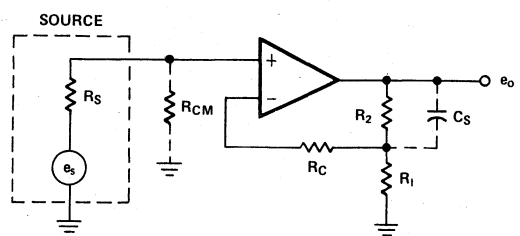
$$e_o = -\frac{R_f}{R_i}\left[e_s + \underbrace{e_{os}\left(\frac{R_f + R_i}{R_f}\right) + I_b R_i}_{\text{Signal Input Drift Error} = V_d}\right] \quad \text{For } R_C = 0 \text{ and } R_S \ll R_i$$

$$e_o = -\frac{R_f}{R_i}\left[e_s + \underbrace{e_{os}\frac{R_f + R_i}{R_f} + i_d R_i}_{\text{Signal Input Drift Error} = V_d}\right] \quad \text{For } R_C = R_i R_f/R_i + R_f \text{ and } R_S \ll R_i$$

Input Impedance $R_{IN} \approx R_i$

$$\%\ \text{Drift Error} = \frac{100V_d}{e_s}$$

Figure 1A. Inverting Configuration



$$e_o = \frac{R_2 + R_i}{R_i}\left[\underbrace{e_s + e_{os} + i_b R_s}_{\text{Signal Drift Error} = V_d}\right] \quad \text{for } R_C = 0$$

$$e_o = \frac{R_2 + R_i}{R_i}\left[\underbrace{e_s + e_{os} + i_d R_s}_{\text{Signal Drift Error} = V_d}\right] \quad \text{for } R_C = R_s \ \frac{R_i R_2}{R_i + R_2}$$

Input Impedance $R_{IN} \approx R_{CM}$

$$\%\ \text{Drift Error} = \frac{100V_d}{e_s}$$

Figure 1B. Noninverting Configuration

ance of the noninverter (approximately R_{CM}) is typically 10^7 ohms even for the least expensive bipolar amplifiers and up to 10^{11} ohms for FET types.

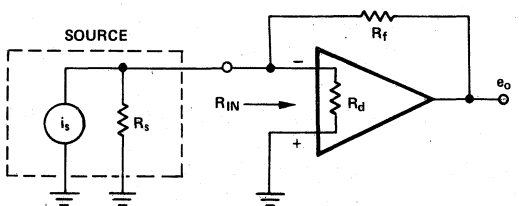
Unfortunately, however, the noninverting configuration can not always be used since it will not perform many circuit functions such as integration or summation. A further limitation occurs in high accuracy applications, where common mode errors may rule out this circuit configuration.

Initial offsets can usually be zeroed at room temperature so that only the maximum temperature excursion (ΔT) from +25°C need be considered. For example, over the range of −25°C to +85°C, the maximum temperature excursion (ΔT) from +25°C would be 60°C. As a practical matter, offset errors due to supply voltage and time drift can generally be neglected since errors due to temperature drift are usually much greater.

Current Amplifier Considerations

Before leaving the subject of offset errors, we shall discuss briefly the current amplifier configuration which is shown in Figure 2A. The obvious approach to measuring current is to develop a voltage drop across a load resistor, R_f, and to measure this potential with a high impedance amplifier as shown in Figure 2B.

This approach has several disadvantages as compared to the circuit of Figure 2A. First the noninverting amplifier introduces common mode errors which do not occur for Figure 2A. Second, an ideal current meter would have zero impedance whereas, R_f in Figure 2B may become very large since this resistor determines the sensitivity of the measurement. Third, the changes of input impedance, R_{CM}, for the noninverting amplifier with temperature will cause variable loading on R_f and hence a change in sensitivity.



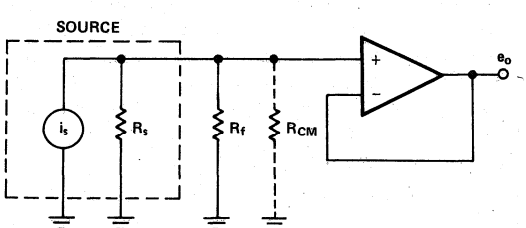
$$e_o = -R_f\left[i_s + e_{os}\left(\frac{R_f + R_s}{R_s R_f}\right) + i_b\right]$$

Signal — Drift error = I_ϵ

$$\text{Input Impedance } R_{IN} = \left(\frac{R_f R_d}{R_f + R_d}\right)\left(\frac{1}{1 + A\beta}\right)$$

$$\text{where } 1/\beta = 1 + \frac{R_f (R_s + R_d)}{R_s R_d} \quad \% \text{ Drift Error} = \frac{100\, I_\epsilon}{i_s}$$

Figure 2A. Current Amplifier



$$e_o = \underbrace{R_f i_s}_{\text{Signal}} + \underbrace{e_{os} + i_b R_f}_{\text{Drift Error} = V_d} \text{ for } R_s > R_f$$

$$\text{Input Impedance } R_{IN} \approx R_f$$

$$\% \text{ Drift Error} = \frac{100\, V_d}{R_f\, i_s}$$

Figure 2B. Voltage Amplifier With Sampling Resistor

The current amplifier of Figure 2A circumvents all of these difficulties and approaches an ideal current meter; that is, there is essentially no voltage drop across the measuring circuit, since with enough open loop gain, A, the input impedance R_{IN} becomes very small.

In selecting a current amplifier, the most important consideration is current noise, and bias current drift. Measuring accuracy is largely the ratio of current noise and drift to signal current, i_s. To obtain the drift of error current I_ϵ referred to the input, use the following expression.

$$\Delta I_\epsilon = \left[\frac{\Delta e_{os}}{\Delta T}\left(\frac{R_f + R_s}{R_f R_s}\right) + \frac{\Delta i_B}{\Delta T}\right]\Delta T$$

Now, to make a proper selection you must pick an amplifier with an error current, I_ϵ, over the operating temperature which is small compared to the signal current, i_s. Do not overlook current noise which may be more important than current drift in many applications.

Gain Bandwidth Considerations, Expanded Discussion

From the previous discussion, it is apparent that most general purpose operational amplifiers will usually give adequate performance for the dc and audio frequency range applications. However, to obtain unity gain bandwidth above 2MHz, full power response above 20kHz and slewing rate above 6V/μs, in general, requires special design techniques. All amplifiers with wideband, fast response characteristics have been listed in the wide bandwidth group to simplify the selection for higher frequency applications.

One factor often overlooked is that stray capacitance and impedance levels of the external feedback circuit can be the major limitation in high frequency applications. For example, in Figure 1A, if R_f were one megohm and stray capacitance, C_s, were one picofarad then the closed loop bandwidth would be limited to 160kHz ($1/(2\pi R_F C_S)$) regardless of how fast the amplifier is. Moreover, output slewing rate will be limited by how fast C_S can be charged which in trun is related to signal level, e_s, and input impedance, R_i, by $de_o/dt = -e_s/R_i C_s$. For these reasons it is usually not possible to obtain both fast response and high input impedance for an inverting circuit since both R_i and R_f must be large to obtain high input impedance.

Another advantage of the noninverting circuit (Figure 1B) is that input impedance, being determined by potentiometric feedback, does not depend on the impedance levels for R_1 and R_2. Therefore, a low impedance can be used for R_2 so that stray capacitance of C_S will not limit the circuit's bandwidth. In this case the minimum value for R_2 is constrained only by the output current rating of the amplifier. Again the trade-off between the frequency response and input impedance of the inverting and noninverting circuits must be evaluated in light of the common mode rejection error introduced by the noninverter.

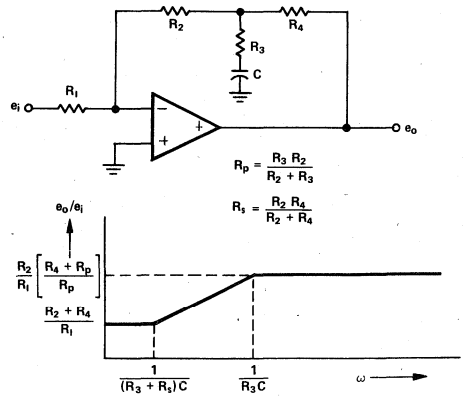


Figure 3. DC Feedback Minimizes Output Offset for AC Applications

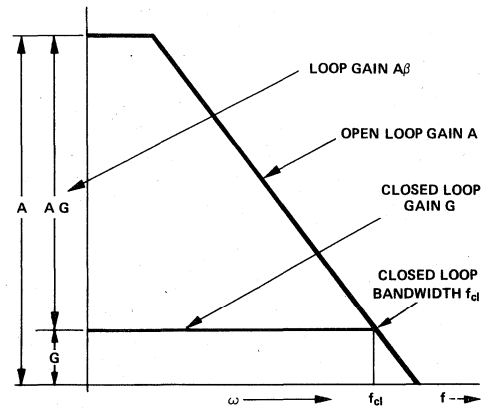


Figure 4. Closed Loop Bandwidth and Loop Gain

In the past, many wideband amplifiers, especially chopper stabilized units, did not offer fast response on the positive input and therefore were restricted to use in inverting circuits. However, new FET amplifiers from Analog Devices are available to meet the needs for high speed performance for either configuration.

For greater emphasis wideband applications can be separated into two categories — steady state and transient. Since the amplifier requirements for the two are somewhat different, these categories will be discussed separately.

A. Steady State Applications

Steady state applications involve amplifying or otherwise manipulating *continuous* sinusoidal, complex or random waveforms. In these applications the significant issues in choosing an amplifier are as follows:

1. *Is dc coupling required?* If dc information is of no consequence, then the offset drift errors are not usually important and a capacitor can be used if necessary to block the output dc offset. Your only concern here is that dc offset at the output does not become so large, as might be the case with a high gain stage, that the output is saturated or the dynamic swing for ac signals is limited. One way to circumvent the latter problem is to use feedback to limit the gain at dc as shown in Figure 3. The gain of these circuits can be small at dc but large at high frequencies.

2. *What closed loop gain and bandwidth are required?* Closed loop gain, G, is dictated by the application. To a first approximation the intersection of the open and closed loop gain curves in Figure 4 gives the closed loop bandwidth, f_{cl} (−3dB). For high gain, wideband requirements, it may be necessary, or more economical, to use two amplifiers in cascade, each at lower gain.

3. *What loop gain is required or alternatively what gain stability, output impedance and/or linearity are necessary?* The available loop gain at a particular frequency or over a range of frequencies is very often more important than closed loop bandwidth in selecting an amplifier. Loop gain as illustrated in Figure 4, is defined as the difference, in dB, or as the ratio, arithmetically, of the open to closed loop gain ($A\beta = A/G$). You will find in most of the equations defining the closed loop characteristic of a feedback amplifier that the loop gain ($A\beta$) is the determining factor in performance. Some of the more notable examples of this point are as follows:

a. Closed loop gain stability = $\Delta G/G$
$\Delta G/G = (\Delta A/A)\ [1/(1 + A\beta)]$ where $\Delta A/A$ is the open loop gain stability, usually about 1%/°C.

b. Closed loop output impedance = $Z_{ocl} = Z_o/(1 + A\beta)$, where Z_o is the open loop output impedance, usually 200 to 5000 ohms.

c. Closed loop nonlinearity = $L_{cl} = L_{ol}/(1 + A\beta)$, where L_{ol} is the open loop linearity, usually less than 5%.

Loop gain of 100, or 40dB, is adequate for most applications and this is readily achievable at dc and low frequencies. But note that loop gain decreases with increasing frequency which makes it difficult to obtain large loop gains at high frequencies. For this reason it may be necessary to use a 10MHz unity gain amplifier in order to obtain adequate feedback over a 10kHz bandwidth.

4. *What full power response and/or slew rate are required?* You should examine your expected output waveform and select an amplifier whose slewing rate exceeds the maximum rate of change of output signal. For a sinusoidal waveform with a peak voltage output equal to the rated amplifier output the frequency should not exceed f_p, the full power response of the amplifier. As the output signal voltage is reduced below the rated output voltage, the usable maximum frequency can be extended proportionately. If you do not observe these restrictions you will get distortion and unexpected dc offsets at the output of the amplifier.

There are many monolithic amplifier designs available today whose frequency response is not a simple 6dB roll-off and which may be shaped with external RC components for improved performance. Using feed-forward or phase lag compensation networks, gain-bandwidth product and/or full power response may be shaped to meet varying design requirements. Most discrete op amps offer the stable 6dB roll-off with specified unity gain-bandwidth and slew rate thereby limiting maximum speed and response to those published specifications.

B. Transient Applications

In applications such as A/D and D/A converters and pulse amplifiers, the *transient response* of the wideband amplifier is generally more important than the *gain bandwidth* characteristic described above. Slewing rate, overload recovery and settling time are the specifications which determine the transient response.

When applying the high frequency amplifier, it is important to understand how amplifier performance is affected by component selection as well as impedance levels used around the amplifier.

Settling Time

The time and frequency response of a linear, bilateral network or amplifier are related by well known mathematics. For example, the step response for a well behaved, linear, 6dB/octave amplifier with a closed loop bandwidth of ω_{cl} is shown in Figure 5.

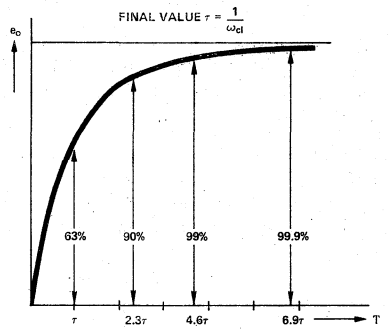


Figure 5. Step Response for Linear 6dB/Octave Amplifier

To a first approximation, the curve in Figure 5 can be used to relate settling time to closed loop bandwidth of Figure 4. *Settling time* is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value (Figure 6). Settling time therefore includes the time required for the amplifier to slew from the initial value, recover from slew rate limited overload, and settle to a given error in the linear range.

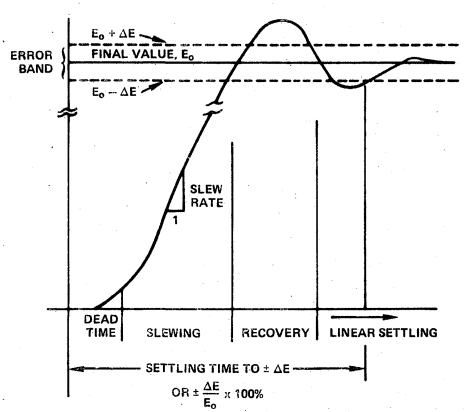


Figure 6. Typical Settling Time Characteristics

However, the approximation soon breaks down since settling time is determined by a combination of amplifier characteristics (both linear and nonlinear) and because it is a closed loop parameter. Therefore, it cannot be readily predicted from the open loop specifications such as slew rate, small signal bandwidth, etc.

Analog Devices specifies settling time for the condition of unity gain, relatively low impedance levels, and no capacitive loading. A full-scale step input is used to determine settling time and the step is generally unipolar – i.e.: from zero to plus or minus full scale. The settling time indicated is generally the longest time resulting from a step of either polarity and is given as a percentage of the full scale step transition.

Settling time is a nonlinear function. It varies with the input signal level and it is greatly affected by impedances external to the amplifier. The nonlinear dependence of settling time on these two parameters can be demonstrated by an examination of experimental data from Analog Devices' wide bandwidth AD544 op amp.

Settling Time vs. Signal Swing

The curves in Figure 7 illustrate the AD544 settling time error versus input signal level. These "V" curves are useful as a design aid for bracketing settling time versus step input level.

Because of nonlinear factors, extrapolation of settling times from one set of conditions to another becomes very difficult, if not impossible. This point becomes very apparent, in Figure 7, when reviewing settling time as a function of input signal swing. Using this measurement technique, the settling time error voltage, measured at point V, is equal to one-half of the null voltage between the input signal and the output signal.

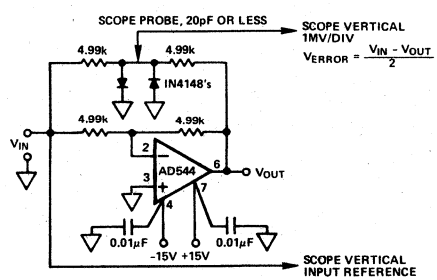


Figure 7A. Settling Time Test Circuit

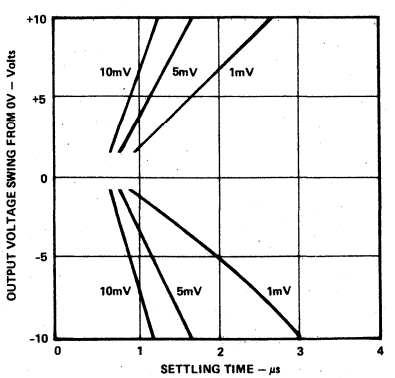


Figure 7B. Output Settling Time vs. Output Swing and Error

ERRORS DUE TO NOISE

A major criterion in the selection of an amplifier for low level signals is the amplifier input noise, since this is usually the limiting factor on system resolution. In the general case, amplifier noise can be characterized by a voltage source in series with the summing junction and a current source in parallel with the summing junction. Whenever high source impedance is encountered, current noise flowing through the source impedance will appear as an additional voltage noise, combining with the amplifier voltage noise. The sum of these noise sources will then be amplified along with the desired signal. For this reason, selection of a particular amplifier must consider both the amplifier noise performance as well as the source impedance.

Consideration must also be given to noise sources other than the amplifier whenever determining total system noise. RF noise may be fed into an amplifier through any connecting wire, including power supply and output leads. Adequate shielding and low-pass filters on all incoming leads will usually prevent noise pick-up.

Thermal noise is generated in any conductor or resistor as a result of thermal agitation of the electrons. This noise voltage source, sometimes referred to as "Johnson Noise", is generated in the resistive component of any impedance and has a value:

$e_n = \sqrt{4KTBR}$

where e_n = the rms value of the noise voltage

K = Boltzman's Constant (1.38×10^{23} joules/°K)

T = absolute temperature of the resistance, °K

B = the bandwidth in which the noise is measured

Since noise is related to the bandwidth over which the measurement is made, no noise specification is meaningful unless the bandwidth for the specification is given. Although the Thermal Noise equation may appear unwieldly for practical noise calculations, all that is required to enable rapid approximations is to apply a few simple rules of thumb.

Rules of Thumb

(1) Remember that a 100kΩ resistor generates 40nV rms in a 1Hz bandwidth. The noise voltages generated by other values of resistances in other bandwidths can be calculated by remembering that the noise is proportional to the square root of the resistance and the bandwidth; i.e.

$$e_n \text{ (rms)} = (40nV/\sqrt{Hz})\left(\sqrt{\frac{R}{100k\Omega}\ (BW)}\right)$$

(2) To convert the rms noise to a p-p value, a conversion factor of 6.6μV p-p/μV rms is applied for less than 0.1% probability of noise peaks exceeding calculated limits.

(3) The total rms noise contribution due to several noise sources is determined by the square root of the sum of the squares:

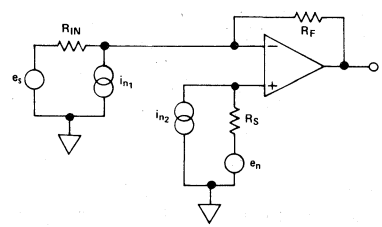
$$e_t = \sqrt{e_a^2 + e_b^2 + e_c^2 + \ldots e_n^2}$$

If any noise source is less than a third of another, it may be neglected. The resulting error will be approximately 5%.

(4) Restricting the bandwidth of a system to the minimum usable and using the lowest impedances possible are ways to reduce noise.

DESIGN EXAMPLE

Figure 8 illustrates a typical circuit with noise calculations shown for each noise source. The total of the noise sources is obtained by adding each of the individual sources in a rms fashion.



COMPONENT	CAUSE	OUTPUT CONTRIBUTION
R_{IN}	Johnson Noise	$\sqrt{4KTBR_{IN}}\ (R_F/R_{IN})$
R_S	Johnson Noise	$\sqrt{4KTBR_S}\ (R_F/R_{IN}+1)$
R_F	Johnson Noise	$\sqrt{4KTBR_F}$
i_{n_1}	Amp. Current Noise	$i_{n_1} R_F$
i_{n_2}	Amp. Current Noise	$(i_{n_2} R_S)\ (R_F/R_{IN}+1)$
e_n	Amp. Voltage Noise	$e_n\ (R_F/R_{IN}+1)$

$$\text{TOTAL NOISE} = \sqrt{(e_{R_{IN}} G)^2 + [e_{R_S}(G+1)]^2 + e^2_{R_F} + [(i_{n_1} R_F)^2] + [(i_{n_2} R_S)(G+1)]^2 + [e_n (G+1)]^2}$$

Figure 8. Noise Components

How to Test Basic Operational Amplifier Parameters

THE REAL OP AMP

Input Imperfections

The characteristics of op amps are, of course, considerably more complicated than can be shown in Figure 1. The real op amp has a number of sources of error which must be tested independently to determine the true quality of the device. The active errors at the input can be modeled as a dc current source (I_B) and a series dc voltage source (V_{OS}). An impedance (Z_{IN} Diff) appears between the inputs, and another (Z_{INCM}) appears between the inputs and ground. These impedances usually consist of a resistance and capacitance in parallel, and the finite Z_{CM} will introduce errors due to common-mode input voltages.

There are two additional input error sources. In addition to the dc voltage and current sources, small ac sources representing the noise components must be included in the model.

Output Obstacles

The output side of the model is also nonideal. First, an output impedance, R_O, is added in series with the voltage source. The "A" term (infinite in the ideal model) is both finite and a function of frequency in a real amplifier A'(s). It is also obvious that the output voltage and current capabilities of a real op amp are bounded.

The real amplifier, thus, can be modeled as shown below.

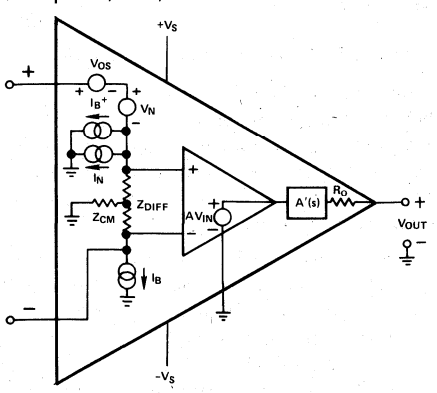


Figure 1. Real Op Amp

OP AMP SPECIFICATIONS

Offset Voltage

Each of these nonideal specifications should be examined in some detail. Consider first the dc errors. Offset voltage is the result of a mismatch in the base-emitter voltages of the differential input transistors (or gate-source voltage mismatch in FET-input amplifiers). This offset voltage is indistinguishable from an input signal as far as the amplifier is concerned. Usually this offset can be trimmed to zero by the user by means of an external potentiometer, which adjusts the balance of the operating currents in the input stage until the V_{BE}'s (or V_{GS}'s) are equal. Of course, this trim will be effective only at one temperature, since offset voltage changes as a function of temperature.

Many circuits exist for testing offset voltage. If V_{OS} is redefined as the voltage at the op amp input which will drive the output to zero in an open-loop circuit, a servo loop can be built around the device under test to determine that voltage. In the circuit shown below, a second amplifier is used to provide feedback. This feedback amplifier must have very high gain and low offset. In operation, the control voltage, V_C, is set to zero. This forces the output of the device under test (D.U.T.) to also go to zero, because no dc current can flow through the amplifier's feedback capacitor. Since the output of the D.U.T. will only go to zero when a voltage equal to its input offset voltage is applied to its input, then V_A must equal V_{OS}. Thus, the output of the feedback amplifier is equal to $V_{OS} \times (1 + R_F/100\Omega)$.

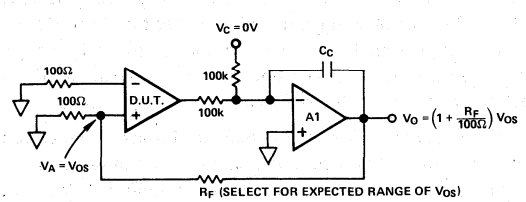


Figure 2. Op Amp Offset Voltage Test Circuit

An alternate method for offset voltage measurement can also be used. This alternate circuit is simpler to build and is only slightly less accurate. If it is assumed that V_{OS} can

be modeled as a source connected in series with one input, configuring the amplifier for a fairly high closed-loop gain will allow reasonably accurate measurement of offset voltage with an inexpensive voltmeter.

In order to maintain accuracy in this measurement, R_{IN} should be low enough that I_{OS} flowing through R_{IN} is at least ten times lower than the expected value of V_{OS}. R_C causes an equal voltage to be developed at each input due to I_B. This common-mode voltage effect can be neglected due to the common mode rejection of the op amp. Reasonable values for R_{IN}, R_C, and R_{FB} are 100Ω, 100Ω, and 9.9kΩ, respectively.

Another error arises in this circuit due to the finite open loop gain of the amplifier. Assuming a test circuit gain of 100, the amplifier must have a dc open-loop gain of at least 10,000 for a 1% accurate V_{OS} measurement.

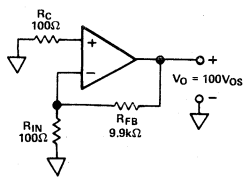


Figure 3. Simple V_{OS} Test Circuit

Input Bias Current

Another dc error term is the input bias current. As a consequence of the practical characteristics of transistors, base current must be supplied to the input transistors to bias them into their active operating region. This current must also return to its originating point through some dc path. Thus operational amplifiers cannot be used with input signal sources which are not referred to the same power source as the amplifier. It is possible to reduce bias current-induced errors by providing a source (other than the signal path) which can leak this current.

In many applications, the errors due to bias current are actually less annoying than the errors caused by the mismatch of the bias circuits of the two inputs. This difference between the bias currents is called the input offset current, and is usually specified along with the bias current.

Input currents, like input offset voltage, vary as a function of temperature. In the case of a bipolar-input amplifier, bias current decreases at elevated temperature. This is because the transistors' β increases, and since the emitter current is constant, the base current decreases. In the case of a FET-input amplifier, the bias current is due to JFET gate leakage, which is in reality a reverse-biased junction leakage current. Such currents have the characteristic of doubling for every 10°C rise in junction temperature.

It is important to consider the test conditions under which bias current is specified, particularly in the case of a FET-input op amp. Some manufacturers specify bias current at a junction temperature of 25°C. This corresponds roughly to the bias current immediately after power is applied to the amplifier. Unfortunately most circuits are not operated in a pulsed mode, and the effects of component self-heating must be considered. This effect is, in many cases, not trivial. For example, an amplifier which draws 5mA of supply current from ±15V supplies dissipates 150mW. The thermal resistance from junction to ambient for an 8-lead IC package is typically 150°C/W. This means that the junction temperature of the amplifier in question will be 22.5°C above ambient temperature, and the bias current will be over four times as high as a specification based on 25°C junction temperature.

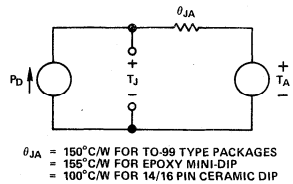


Figure 4. Thermal Circuit Model for IC Op Amp

Consider an op amp specified for 50pA I_B at T_J = 25°C. If the amplifier draws 5mA from ±15V, as in the previous example,

$$P_D = 30V \times 5mA = 150mW$$
$$T_J = T_A + (150mW \times 150°C/W)$$
$$= 25°C + 22.5°C$$

Therefore, I_B will be four times higher than the specification.

Bias current can be measured with essentially the same method used to measure offset voltage. The difference is that a large resistance is inserted in series with the input under test, creating an additional offset voltage equal to $I_B \times R_S$. Assuming the actual V_{OS} has been measured and recorded, the change in apparent V_{OS} due to the change in R_S can be determined and I_B easily computed. Offset current is tested by computing the difference between the bias current on the inverting input and the bias current on the noninverting input.

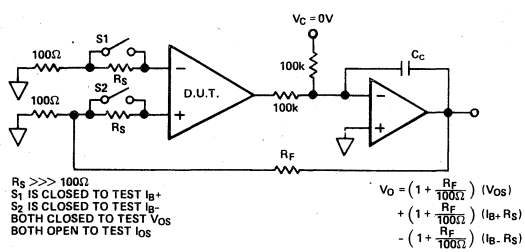


Figure 5. Bias/Offset Current Test Circuit

Open Loop Voltage Gain

Another op amp parameter which distinguishes a real amplifier from an ideal amplifier is open-loop gain. In the ideal op amp model, open loop gain is assumed to be infinite. The same assumption is also sometimes made when dealing with real amplifiers.

Open-loop gain of an operational amplifier is an interesting parameter to attempt to measure. It is generally not practical to measure open loop gain directly by applying a signal at the input and observing the output change. However, by using the device under test inside a feedback loop, it is possible to measure the change in input voltage required to produce a known change in output voltage.

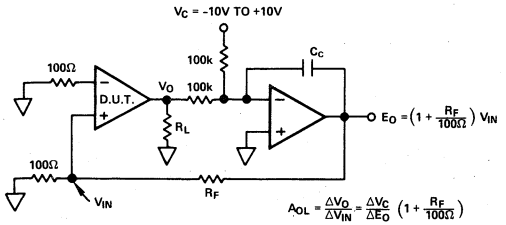


Figure 6. Open Loop Gain Test Circuit

In this circuit, the control voltage, V_C, is varied from −10V to +10V, causing the D.U.T. output, V_O, to vary from +10V to −10V. The D.U.T. output is varied by a change in V_{IN} produced by the second amplifier. Since V_{IN} is attenuated from E_O by the $R_F/100\Omega$ voltage divider, E_O is easily measured, and open-loop gain can readily be computed.

Frequency Response

Open-loop gain versus frequency is another difficult-to-test specification. Bandwidth is usually specified in terms of gain-bandwidth product or unity-gain small signal bandwidth. It is assumed that the amplifier under test has an open-loop gain versus frequency plot which decreases with a −20dB/decade slope. It is therefore possible to measure the open-loop gain at some known frequency and predict the frequency at which the open-loop gain will be unity.

In the circuit shown, the D.U.T. dc output is held to 0V by V_C and the integrator amplifier. A low amplitude 10kHz ac input signal is applied to the D.U.T. Since the integrator has very low gain at 10kHz, the D.U.T. is effectively running open-loop for the ac signal. The ac output from the D.U.T. can be measured and the gain at 10kHz can be computed. For example, a 741-type amplifier has an open loop gain of approximately 100k at 10kHz. Thus, an easily generated 100mV input at the D.U.T. input will produce an easily measured 10V output. This corresponds to a 1MHz gain-bandwidth product.

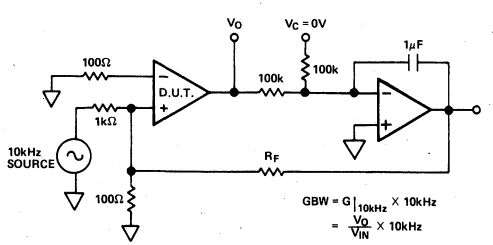


Figure 7. Gain-Bandwidth Product Test Circuit

Common-Mode Rejection Ratio

The ideal operational amplifier is a pure differential amplifier and is insensitive to the absolute voltage on the inputs with respect to ground. The real amplifier has several nonideal characteristics associated with input levels. First, of course, is the allowable range of input voltage. Most IC op amps will only operate when the voltage on the input terminal is within the range bounded by the supply voltages. The second, and perhaps more subtle, characteristic is the common-mode rejection ratio (CMRR). CMRR is defined as the ratio of the change in common mode to the resulting change in input offset voltage. It is often convenient to specify this parameter logarithmically in dB: CMR = 20 log (CMRR).

Common-mode rejection can be measured several ways. One method uses four precision resistors to configure the op amp as a subtractor amplifier. The disadvantage inherent in this circuit is that the ratio match of the resistors also determines the subtractor's CMRR. A mismatch of 0.1% between resistor pairs will result in a CMR of only 60dB. Since most amplifiers exhibit CMR in excess of 80dB (some as high as 120dB), it is clear that this circuit is only marginally useful.

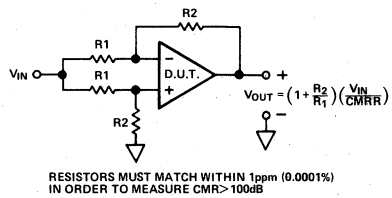


Figure 8. Simple CMR Test Circuit

A better circuit uses the same technique used for measuring offset voltage with one exception. Rather than applying a fixed zero volt input to the D.U.T. operating on ±15V supplies, the same input is applied to the D.U.T. with asymmetrical power supplies, such as +5V and −25V. The output of the amplifier is forced to remain centered between the supplies and the input voltage to the D.U.T. which forces this to occur is measured.

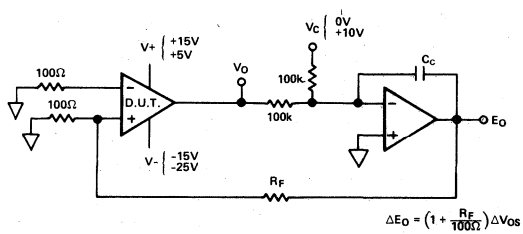


Figure 9. Common-Mode Rejection Test Circuit

The change in V_{OS} can be readily translated into CMR. If this 10V change in CMV creates a 1mV change in V_{OS}, the CMRR is 10,000 and the CMR is 80dB.

ANALOG DEVICES

APPLICATION NOTE

An I.C. Amplifier Users' Guide To Decoupling, Grounding, And Making Things Go Right For A Change

by Paul Brokaw

"There once was a breathy baboon
Who always breathed down a bassoon,
For he said "It appears
that in billions of years
I shall certainly hit on a tune"
(Sir Arthur Eddington)

This quotation seemed a proper note with which to begin on a subject which has made monkeys of most of us at one time or another. The struggle to find a suitable configuration for system power, ground, and signal returns too frequently degenerates into a frustrating glitch hunt. While a strictly experimental approach can be used to solve simple problems, a little forethought can often prevent serious problems and provide a plan of attack if some judicious tinkering is later required.

The subject is so fragmented that a completely general treatment is too difficult for me to tackle. Therefore, I'd like to state one general principle and then look a bit more narrowly at the subject of decoupling and grounding as it relates to integrated circuit amplifiers.

. . . Principle: Think—where the currents will flow.

I suppose this seems pretty obvious, but all of us tend to think of the currents we're interested in as flowing "out" of some place and "through" some other place but often neglect to worry how the current will find its way back to its source. One tends to act as if all "ground" or "supply voltage" points are equivalent and neglect (for as long as possible) the fact that they are parts of a network of conductors through which currents flow and develop finite voltages.

In order to do some advance planning it's important to consider where the currents originate and to where they will return and to determine the effects of the resulting voltage drops. This in turn requires some minimum amount of understanding of what goes on inside the circuits being decoupled and grounded. This information may be lacking or difficult to interpret when integrated circuits are part of the design.

Operational amplifiers are one of the most widely used linear I.C.'s, and fortunately most of them fall into a few classes, so far as the problems of power and grounding are concerned. Although the configuration of a system may pose formidable problems of decoupling and signal returns, some basic methods to handle many of these problems can be developed from a look at op-amps.

OP AMPS HAVE FOUR TERMINALS:

A casual look through almost any operational amplifier text might leave the reader with the impression that an ideal op-amp has three terminals: a pair of differential inputs and an output as shown in Figure 1. A quick review of fundamentals, however, shows that this can't be the case. If the amplifier has an output voltage it must be measured with respect to some point . . . a point to which the amplifier has a reference. Since the ideal op-amp has infinite common mode rejection, the inputs are ruled out as that reference so that there must be a fourth amplifier terminal. Another way of looking at it is that if the amplifier is to supply output current to a load, that current must get into the amplifier somewhere. Ideally, no input current flows, so again the conclusion is that a fourth terminal is required.

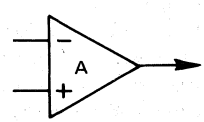


Figure 1. Conventional "Three Terminal" Op Amp

A common practice is to say, or indicate in a diagram, that this fourth terminal is "ground." Well, without getting into a discussion of what "ground" may be we can observe that most integrated circuit op-amps (and a lot of the modular ones as well) don't have a "ground" terminal. With these circuits the fourth terminal is one or both of the power supply terminals. There's a temptation here to lump together both supply voltages with the ubiquitous ground. And, to the extent that the supply lines really do present a low impedance at all frequencies within the amplifier bandwidth, this is probably reasonable. When the impedance requirement isn't satisfied, however, the door is left open to a variety of problems including noise, poor transient response, and oscillation.

DIFFERENTIAL TO SINGLE-ENDED CONVERSION:

One fundamental requirement of a simple op-amp is that an applied signal which is fully differential at the input must be converted to a single-ended output. Single ended, that is, with respect to the often neglected fourth terminal. To see how this can lead to difficulties, take a look at Figure 2.

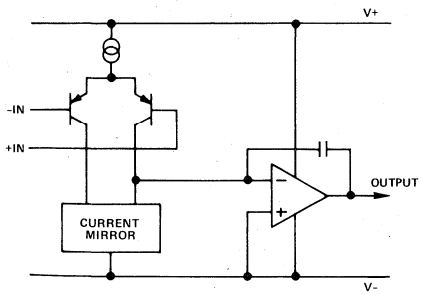


Figure 2. Simplified "Real" Op Amp

The signal flow illustrated by Figure 2 is used in several popular integrated circuit families. Details vary, but, the basic signal path is the same as the 101, 741, 748, 777, 4136, 503, 515, and other integrated circuit amplifiers. The circuit first transforms a differential input voltage into a differential current. This input stage function is represented by PNP transistors in Figure 2. The current is then converted from differential to single-ended form by a current mirror which is connected to the negative supply rail. The output from the current mirror drives a voltage amplifier and power output stage which is connected as an integrator. The integrator controls the open-loop frequency response, and its capacitor may be added externally, as in the 101, or may be self-contained, as in the 741. Most descriptions of this simplified model don't emphasize that the integrator has, of course, a differential input. It's biased positive by a couple of base emitter voltages, but, the non-inverting integrator input is referred to the negative supply.

It should be apparent that most of the voltage difference between the amplifier output and the negative supply appears across the compensation capacitor. If the negative supply voltage is changed abruptly the integrator amplifier will *force* the output to follow the change. When the entire amplifier is in a closed loop configuration the resulting error signal at its input will tend to restore the output, but, the recovery will be limited by the slew rate of the amplifier. As a result, an amplifier of this type may have outstanding low frequency power supply rejection, but, the negative supply rejection is fundamentally limited at high frequencies. Since it is the feedback signal to the input that causes the output to be restored, the negative supply rejection will approach zero for signals at frequencies above the *closed loop* bandwidth. This means that high-speed, high-level circuits can "talk to" low-level circuits through the common impedance of the negative supply line.

Note that the problem with these amplifiers is associated with the negative supply terminal. Positive supply rejection may also deteriorate with increasing frequency, but, the effect is less severe. Typically, small transients on the positive supply have only a minor effect on the signal output. The difference between these sensitivities can result in an apparent asymmetry in the amplifier transient response. If the amplifier is driven to produce a positive voltage swing across its rated load it will draw a current pulse from the positive supply. The pulse may result in a supply voltage transient, but, the positive supply rejection will minimize the effect on the amplifier output signal. In the opposite case, a negative output signal will extract a current from the negative supply. If this pulse results in a "glitch" on the buss, the poor negative supply rejection will result in a similar "glitch" at the amplifier output. While a positive pulse test may give the amplifier transient response, a negative pulse test may actually give you a pretty good look at your negative supply line transient response, instead of the amplifier response!

Remember that the impulse response of the power supply itself is not what is likely to appear at the amplifier. Thirty or forty centimeters of wire can act like a high Q inductor to add a high-frequency component to the normally overdamped supply response. A decoupling capacitor near the amplifier won't always cure the problem either, since the supply must be decoupled *to* somewhere. If the decoupled current flows through a long path, it can still produce an undesirable glitch.

Figure 3 illustrates three possible configurations for negative supply decoupling. In 3a the dotted line shows the negative signal current path through the decoupling and along the ground line. If the load "ground" and decoupled "ground" actually join at the power supply the "glitch" on the ground lines is similar to the "glitch" on the negative supply buss. Depending upon how the feedback and signal sources are "grounded" the effective disturbance *caused* by the decoupling capacitor may be larger than the disturbance which it was intended to prevent. Figure 3b shows how the decoupling capacitor can be used to minimize disturbance of V– and ground busses. The high-frequency component of the load current is confined to a loop which doesn't include any part of the ground path. If the capacitor is of sufficient size and quality, it will minimize the glitch on the negative supply without disturbing input or output signal paths. When the load situation is more complex, as in 3c, a little more thought is required. If the amplifier is driving a load that goes to a virtual ground, the actual load current does not return to ground. Rather, it must be supplied by the amplifier creating the virtual ground as shown in the figure. In this case, decoupling the negative supply of the first amplifier to the positive supply of the second amplifier closes the fast signal current loop without disturbing ground or signal paths. Of course, it's still important to provide a low impedance path from "ground" to V– for the second amplifier to avoid disturbing the input reference.

The key to understanding decoupling circuits is to note where the actual load and signal currents will flow. The key to optimizing the circuit is to bypass these currents around ground and other signal paths. Note, that as in figure 3a, "single point grounding" may be an oversimplified solution to a complex problem.

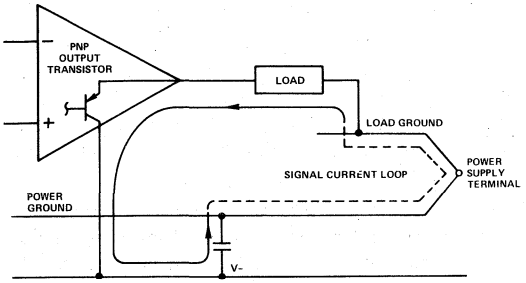


Figure 3a. Decoupling for Negative Supply Ineffective

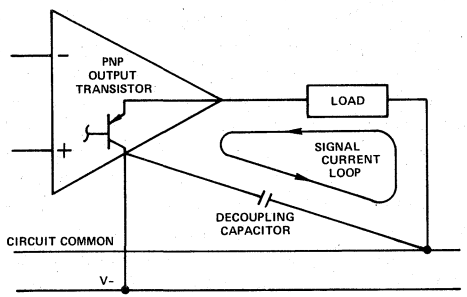


Figure 3b. Decoupling Negative Supply Optimized for "Grounded" Load

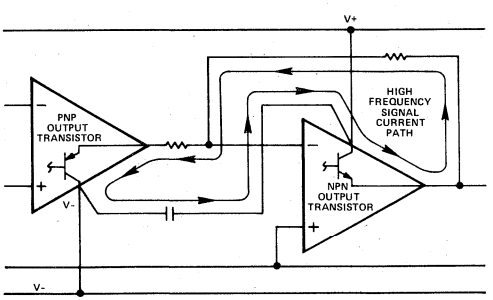


Figure 3c. Decoupling Negative Supply Optimized for "Virtual Ground" Load

Figure 3b and 3c have been simplified for illustrative purposes. When an entire circuit is considered conflicts frequently arise. For example, several amplifiers may be powered from the same supply, and an individual decoupling capacitor is required for each. In a gross sense the decoupling capacitors are all paralleled. In fact, however, the inductance of the interconnecting power and ground lines convert this harmless-looking arrangement into a complex L-C network that often rings like the "Avon Lady". In circuits handling fast signal wavefronts, decoupling networks paralleled by more than a few centimeters of wire generally mean trouble. Figure 4 shows how small resistors can be added to lower the Q of the undesired resonant circuits. The resistors can generally be tolerated since they convert a bad high-frequency jingle to a small damped signal at the op amp supply terminal. The residual has larger *low frequency* components, but, these can be handled by the op-amp supply rejection.

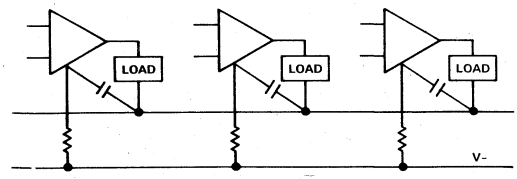


Figure 4. Damping Parallel Decoupling Resonances

FREQUENCY STABILITY:

There's a temptation to forget about decoupling the negative supply when the system is intended to handle only low-frequency signals. Granted that decoupling may not be required to handle low-frequency signals, but it may still be required for frequency stability of the op-amps.

Figure 5 is a more-detailed version of Figure 2 showing the output stage of the I.C. separated from the integrator (since this is the usual arrangement) and showing the negative power supply and wiring impedance lumped together as a single constant. The amplifier is connected as a unity gain follower. This makes a closed-loop path from the amplifier output through the differential input to the integrator input. There is a second feedback path from the collector of the output PNP transistor back to the other integrator input. The net input to the integrator is the difference of the signals through these two paths. At low frequencies this is a net, negative feedback. The high-frequency feedback depends upon both the load reactance and the reactance of the V– supply.

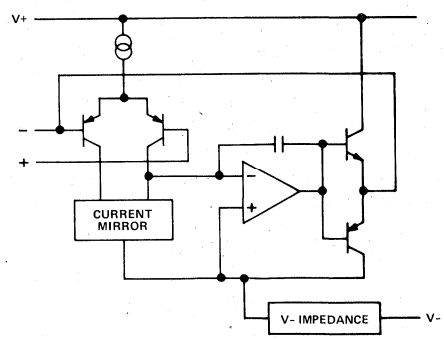


Figure 5. Instability Can Result from Neglecting Decoupling

When the supply lead reactance is inductive, it tends to destabilize the integrator. This situation is aggravated by a capacitive load on the amplifier. Although it's difficult to predict under exactly what circumstances the circuit will become unstable, it's generally wise to decouple the negative supply if there is any substantial lead inductance in the V– lead *or* in the common return to the load and amplifier input signal source. If the decoupling is to be effective, of course, it must be with respect to the *actual* signal returns, rather than to some vague "ground" connection.

POSITIVE SUPPLY DECOUPLING:

Up to this point we haven't considered decoupling the positive supply line, and with amplifiers typified by Figures 2

and 5 there may be no need to. On the other hand, there are a number of integrated circuit amplifiers which refer the compensating integrator to the positive supply. Among these are the 108, 504, and 510 families. When these circuits are used, it's the positive supply which requires most attention. The considerations and techniques described for the class of circuits shown in Figure 2 apply equally to this second class, but, should be applied to the positive supply rather than the negative.

FEED-FORWARD:

A technique which is most frequently used to improve bandwidth is called feed-forward. Generally, feed-forward is used to bypass an amplifier or level translator stage which has poor high frequency response. Figure 6 illustrates how this may be done. Each of the amplifiers shown is really a subcircuit, usually a single stage, in the overall amplifier. In the illustration, the input stage converts the differential input to a single-ended signal. The signal drives an intermediate stage (which in practice often includes level translator circuitry) which has low-frequency gain, but, limited bandwidth. The output of this stage drives an integrator-amplifier and output stage. The overall compensation capacitor feeds back to the input of the second stage and includes it in the integrator loop. The compromises necessary to obtain gain and level translation in the intermediate stage often limit its bandwidth and slow down the available integrator response. A feed-forward capacitor permits high-frequency signals to bypass this stage. As a result, the overall amplifier combines the low-frequency gain available from 3 stages with the improved frequency response available from a 2-stage amplifier. The feed-forward capacitor also feeds back to the non-inverting input of the intermediate stage. Note that the second stage is not an integrator, as it may appear at first glance, but actually has a positive feedback connection. Fed-forward amplifiers must be carefully designed to avoid internal oscillations resulting from this connection. Improper decoupling can upset this plan and permit this loop to oscillate.

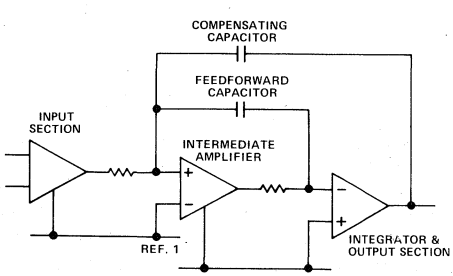


Figure 6. Fast Fed-Forward Amplifier

Note that the internal input stages are shown as being referred to separated reference points. Ideally, these will be the same reference so far as signals are concerned, although they may differ in bias level. In practice this may not be the case. Examples of fed-forward amplifiers are the AD518, the AD118, and the OP-05. In these amplifiers, signal Reference 1 is the positive supply, while signal Reference 2 is the negative supply. Signals appearing between the positive and negative supply terminals are effectively inserted inside the integrator loop!

Obviously, while feed-forward is a valuable tool for the high-speed amplifier designer, it poses special problems in application. A thoughtful approach to decoupling is required to maximize bandwidth and minimize noise, error, and the likelihood of oscillation.

Some fed-forward amplifiers have other arrangements, which include the "ground" terminal in inverting only amplifiers. Almost without exception, however, signals between some combination of the supply terminals get "inside" the amplifier. It is vital to proper operation that the involved supply terminals present a common low impedance at high frequencies. Many high-speed modular amplifiers include appropriate capacitive decoupling within the amplifier, but, with I.C. op amps this is impossible. The user must take care to provide a cleanly decoupled supply for fed-forward amplifiers. Figure 7 shows a decoupling method which may be applied to the AD518 as well as to other fast fed-forward amplifiers such as the 118. One capacitor is used to provide a low-impedance path between the supply terminals at high frequencies. The resistor in the V+ lead insures that noise on the supply lines will be rejected *and* prevents the establishment of resonances with other decoupling circuits. The second capacitor decouples the low side of the integrator to the load.

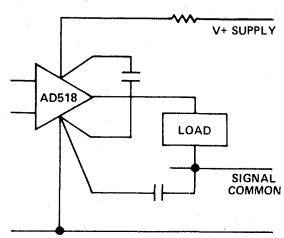


Figure 7. Decoupling for a Fed-Forward Amplifier

Alternatives include a resistor in both supply leads and/or decoupling from V+ to the load. In principle, the positive and negative supply should be tied in a "tight knot" with the signal return. To the extent that this cannot be done, there is a slight advantage to favoring the negative supply due to the high frequency limitations of PNP transistors used in junction-isolated I.C.'s.

OTHER COMPENSATION:

While most integrated circuit amplifiers use one of the three compensation schemes already described, a significant fraction use some other plan. The 725 type amplifiers combine a V– referred integrator with a network which the manufacturers recommend to be connected from signal ground to the integrator input. This makes the circuit extremely liable to pick up noise between V– and ground. In many circumstances it may be wiser to connect the external compensation to the negative supply, rather than to signal ground.

One more class of amplifiers is typified by the Analog Devices AD507 and AD509. In these circuits, a single capaci-

tor may be used to induce a dominant pole of response without resorting to an integrator connection. The high-frequency response of the amplifier will appear with respect to the "ground" end of the compensation capacitor. In these amplifiers a small internal capacitance is connected between V+ and the compensation point. Unity gain compensation can be added in parallel and the pin-out is arranged to make this simple. The free end of the compensation capacitor can also be connected either to V– or signal common. It is extremely important that the signal common and the compensation connect directly or through a low-impedance decoupling.

Although the main signal path of these amplifiers can be compensated in a variety of ways, some care is required to insure the stability of internal structures. It's always wise to use extra care in decoupling wideband amplifiers to avoid problems with the output stage and other subcircuits which are similar to the main integrator problem illustrated by Figure 5. An effective compensation and decoupling circuit for the AD509 is shown in Figure 8. This arrangement is similar to Figure 7, and one of these two circuits is likely to be suitable for many types of wideband amplifier. Depending upon the power distribution, a small (10Ω to 50Ω) resistor may be appropriate in both of the supply leads to reduce power lead resonance and interference both to and from circuits sharing the power supply.

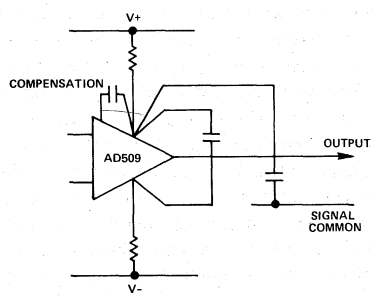


Figure 8. Decoupling a Wideband Amplifier

GROUNDING ERRORS:

Ground in most electronic equipment is not an actual connection to earth ground, but a common connection to which signals and power are referred. It is frequently immaterial to the function of the equipment whether or not the point actually connects to earth ground. I myself prefer some distinguishing name or names for these common points to emphasize that they must be *made* common. The term "ground" too often seems to be associated with a sort of cure-all concept, like snake oil, money or motherhood. If you're one of those who regards ground with the same sort of irrational reverence that you hold for your mother, remember that while you can always trust your mother, you should *never* trust your "ground." Examine and think about it.

It's important to have a look at the currents which flow in the ground circuit. Allowing these currents to share a path with a low-level signal may result in trouble. Figure 9 illustrates how careless grounding can degrade the performance of a simple amplifier. The amplifier drives a load which is represented by the load resistor. The load current comes from the power supply and is controlled by the amplifier as it amplifies the input signal. This current must return to the supply by some path; suppose that points A and B are alternative power supply "ground" connections. Assuming that the figure represents the proper topology or ordering of connections along the "ground" bus, connecting the supply at A will cause the load current to share a segment of wire with the input signal connection. Fifteen centimeters of number 22 wire in this path will present about 8 milliohms of resistance to the load current. With a 2k load, a 10-volt output signal will result in about 40 microvolts between the points marked "ΔV." This signal acts in series with the non-inverting input and can result in significant errors. For example, the typical gain of an AD510 amplifier is 8 million so that only 1¼μV of input signal is required to produce a 10 volt output. The 40μV ground error signal will result in a 32 times increase in the circuit gain error! This degradation could easily be the most serious error in a high-gain precision application. Moreover, the error represents positive feedback so that the circuit will latch up or oscillate for large closed-loop gains with R_f/R_i greater than about 250k.

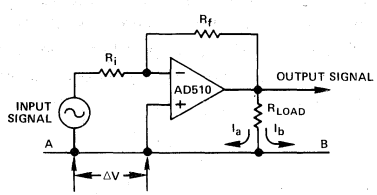


Figure 9. Proper Choice of Power Connections Minimizes Problems

Reconnecting the power supply to point B will correct the problem by eliminating the common impedance feedback connection. In a real system, the problem may be more complex. The input signal source, which is represented as floating in Figure 9, may also produce a current which must return to the power supply. With the supply at point B, any current which flows in additional loads (other than R_i) may interfere with the operation of the amplifier shown. Figure 10 illustrates how amplifiers can be cascaded and still drive auxiliary loads without common impedance coupling. The

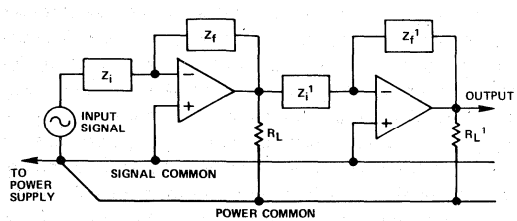


Figure 10. Minimizing Common Impedence Coupling

output currents flow through the auxiliary loads and back to the power supply through power common. The currents in the input and feedback resistors are supplied from

the power supply by way of the amplifiers as previously illustrated in Figure 3c. The only current flowing in signal common is the amplifier's input current, and its effect is generally negligibly small.

Having given an example of a simple "grounding error" and its solution, I will now get back on my soap box and say that grounding errors result from neglect based on the assumption that a ground, is a ground, is a ground. *Some* impedance will be present in any interconnection path, and its effect should be considered in the overall design of a system. Quantitative approaches are quite useful in specialized applications. In fast TTL and ECL logic circuitry the characteristic impedance of interconnections is controlled so that proper terminations can reduce problems. In RF circuitry the unavoidable impedances are taken into account and incorporated into the design of the circuit. With op-amp circuitry, however, impedance levels do not lend themselves to transmission line theory, and the power and ground impedances are difficult to control or analyze. The most expedient procedure, short of difficult and restrictive quantitative analysis, seems to be to arrange the unavoidable impedances so as to minimize their effects and arrange the circuitry to overcome the effects. Figures 9 and 10 illustrate the sort of simple considerations which can substantially reduce practical ground problems. Figure 11 illustrates how circuitry can be used to reduce the effect of ground problems which can't be corrected by topological tricks.

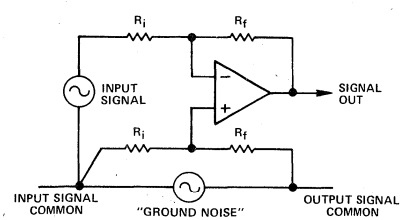


Figure 11. Subtractor Amplifier Rejects Common Mode Noise

GETTING AROUND THE PROBLEM:

In Figure 11 a subtractor circuit is used to amplify a normal mode input signal and reject a ground noise signal which is common to both sides of the input signal. This scheme uses the common-mode rejection of the amplifier to reduce the noise component while amplifying the desired signal. An important aspect of this arrangement, which is often overlooked, is that the amplifier should be powered with respect to the *output* signal common. If its power pins are exposed to the high-frequency noise of the input common, the compensation capacitor will direct the noise right to the output and defeat the purpose of the subtractor. It's just this kind of effect which makes it important to use care in grounding and decoupling. A subtractor or dynamic bridge, like Figure 11, will be ineffective in correcting a grounding problem if the amplifier itself is carelessly decoupled. In general, an op-amp should be decoupled to the point which is the reference for measuring or using its output signal. In "single-ended" systems it should also be decoupled to the input signal return as well. When it is impossible to satisfy both these requirements at once, there's a high probability of either a noise or oscillation problem or both. Frequently the difficulty can be resolved with a subtractor, like Figure 11, where a network like the single-ended feedback network (which needn't be all resistive) joins the input and output signal reference points and provides a "clean" reference point for the non-inverting input of the amplifier.

A problem with the subtractor is that it uses a balanced bridge to reject the common mode signal between the input and output reference points. The arms of the network must be carefully balanced, since to the extent they don't match, the unwanted signal will be amplified. Although even a poorly matched network will probably eliminate oscillation problems, noise rejection will suffer in direct proportion to any mismatches. An easier way to reject large "ground noise" signals is to use a true instrumentation amplifier.

INSTRUMENTATION AMPLIFIERS:

A true instrumentation amplifier has a very visible "fourth terminal." The output signal is developed with respect to a well defined reference point which is usually a "free" terminal that may be tied to the output signal common. The instrumentation amplifier also differs from an op amp in that the gain is fixed and well defined, but there is no feedback network coupling input and output circuits. Figure 12 shows how an instrumentation amplifier can be used to translate a signal from one "ground reference" to another. The normal mode input signal is developed with respect to one reference point which may be common to its generating circuits. The signal is to be used by a system which has an interfering signal between its own common and the signal source. The instrumentation amplifier has a high impedance differential input to which the desired signal is applied. Its high common mode rejection eliminates the unwanted signal and translates the desired signal to the output reference point. Unlike the dynamic bridge circuit, the gain and common mode rejection don't depend on a network connecting the input and output circuits. The gain is set, in Figure 12, by the ratio of a pair of resistors which are connected inside the amplifier. The amplifier has a very high input impedance, so that gain and common mode rejection are not greatly affected by variations or unbalance in source impedance.

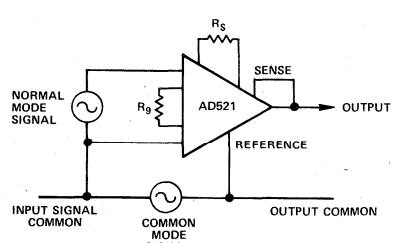


Figure 12. Applying an In-Amp

Since instrumentation amplifiers have a reference or "ground" terminal, they have the potential to be free of the power supply sensitivities of op amps. In practice, however, most instrumentation amplifiers have internal frequency

compensation which is referred to the power supply. In the case of the AD521, the compensation integrator is referred to the negative supply terminal. The decoupling of this terminal is particularly important, and it should be decoupled with respect to the output reference terminal, or actually to the point to which this terminal refers. The AD520 instrumentation amplifier, on the other hand, has an internal integrator which is referred to the positive supply terminal. For best results both the V+ and V– terminals should be decoupled to the output reference point.

THE "OTHER" INPUT:

Most I.C. op-amps and in-amps include offset voltage nulling terminals. These terminals generally have a small voltage on them and by loading the terminals with a potentiometer the amplifier offset voltage can be adjusted. While their impedance level is much lower than the normal input, the null terminals can act as another differential input to the amplifier. Although the null terminals aren't generally looked at as inputs, most amplifiers are quite sensitive to signals applied here. For example, in 741 family amplifiers the output voltage gain from the null terminals is greater than the gain from the normal input!

An illustration of the type of problems that can arise with the "other" input is shown in Figure 13. The figure is an op-amp circuit with some of the offset null detail shown.

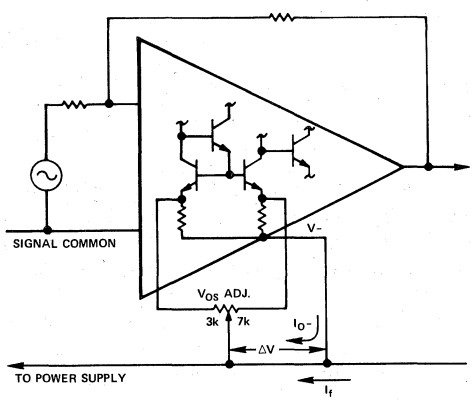


Figure 13. Details of V_{OS} Nulling – the "Other" Input

As it's drawn, the V_{OS} null pot wiper connects to a point along a V– "clothesline" which carries both the return current from the amplifier and currents from other circuits back to the power supply. These currents will develop a small voltage, ΔV, along the conductor between the amplifier V– terminal and the null pot wiper. If the null pot is set on center, the equal halves will form a balanced bridge with the resistors inside the amplifier. The effect of the voltage generated along the wire is balanced at the V_{OS} terminals and will have little effect on the amplifier output. On the other hand, if the null pot is unbalanced, to correct an amplifier offset, the bridge will no longer balance. In this case voltages developed along the "clothesline" will result in a difference voltage at the V_{OS} terminals. For instance, suppose that a 10k null pot balances out the op amp offset when it is set with 3k and 7k branches as shown in the figure. In a 741 the internal resistors are about 1k so that the difference signal at the V_{OS} terminals will be about 1/8 ΔV. The gain from these terminals is about twice the gain from the normal input, so that the disturbance acts as if it were an input signal of about 1/4 ΔV. Using the same assumptions as in the discussion of Figure 9. the current I_O– will result in a 10 microvolt input error signal. In this case, however, the error will appear *only* when the amplifier load current comes from the negative supply. When the load is driven positive the error will disappear. As a result, the V_{OS} input signal will result in distortion rather than a simple gain error!

An additional problem is created by I_f, a current returning to the power supply from other circuits. The current from other circuits is not generally related to the op amp signal, and the voltage developed by it will manifest itself as noise. This signal at the null terminals can easily be the dominant noise in the system. A few milliamps of V– current through a few centimeters of wire can result in interference which is orders of magnitude larger than the inherent input noise of the amplifier. The remedy is to make the connection from the null pot wiper direct to the V– pin of the amplifier, as shown in Figure 14. Some amplifiers such as the AD504 and AD510 refer to the null offset terminals to V+. Obviously, the pot wiper should go to the V+ terminal of this type of amplifier. It's important to connect the line directly to the op amp terminal so as to minimize the common impedance shared by the op amp current and the null pot connection.

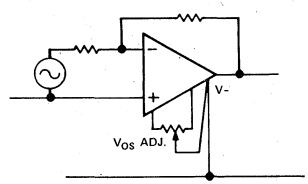


Figure 14. Connecting the Null Pot for Trouble Free Operation

The considerations for op-amp null pots also apply to the similar trimmers on almost all types of integrated circuits. For example, the AD521 In-Amp null terminals exhibit a gain of about 30 to the output. Although this is much less than in the case of most op-amps, it still warrants care in controlling the null pot wiper return. Table I lists the integrated circuits manufactured by Analog Devices, including some popular second-source families, and indicates how internal conversions from differential to single ended are referred. That is, the signals are made to appear with respect to the terminal(s) listed.

	Internal Integrator Referred to:	Comments
AD502	V-	
AD503	V-	
AD504	V+	External Cap
AD506	V-	
AD507	—	External Cap to Signal Common or V+
AD509	—	External Cap to Signal Common or V+
AD510	V+	
AD511	V-	
AD512	V-	
	V-, -in	External Caps, Optional Feedforward to -in
AD514	V-	
AD515	V-	
AD517	V+	
AD518	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD520	V+, V-	Internal Integrator Refers to V+, Internal Input Stage Cap Refers to V-, External Output Caps Refer to V+ and Common
AD521	V-	Output Amplifier Integrator Refers to V-
AD522	V+, V-	Input Amplifier Refers to V+ Output Amplifier Refers to V-
AD523	V-	
AD528	V+, V-	Internal Feedforward Cap V+ to V- and Integrator to Output
AD530	V+	Multiplier Output Amplifier Integrator Refers to V+
AD531	V+	Multiplier Output Amplifier Integrator Refers to V+
AD532	V+	Multiplier Output Amplifier Integrator Refers to V+
AD533	V+	Multiplier Output Amplifier Integrator Refers to V+
AD534	V-	Output Amplifier
AD535	V-	Output Amplifier
AD536A	V-, V+, Common	External Integrator to V+, Internal Feedforward V- to Common
AD537	V-	Internal Buffer Amp

	Internal Integrator Referred To:	Comments
AD540	V-	
AD542	V-	
AD544	V-	
AD545	V-	
AD559	V-, Common	DAC Control Loop Integrator Referred Between V- and Common
AD561	V-, Common	DAC Control Loop Integrator and Ref. Amp Refer to Common Ref. Bias Amp Refers to V-
AD562	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD563	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD565	V-	DAC Control Loop Integrator Referred to V-. Reference Input Common to Control Loop Isolated from DAC Output Common
AD566	V-	DAC Control Loop Integrator Referred to V-, Reference Input Common to Control Loop Isolated from DAC Output Common
AD580	V-	
AD581	V-	
AD582	V-	
AD584	V-	
AD101A	V-	External Cap (Includes AD201A, AD301A, etc.)
AD108	V+	External Cap (Includes AD208, AD308, etc.)
AD741	V-	Internal Cap (Includes 741J, K, L, etc.)

This collection of examples won't solve all your potential grounding problems. I hope that it will give you some good ideas about how to prevent some of them, and it should also give you some of the "inside story" on I.C.'s which you can put to work in very practical ways. There is no general grounding method which will prevent all possible problems. The only generally applicable rule is attention to detail, and remember that you can always trust your mother, but. . .

Table I.

ANALOG DEVICES

APPLICATION NOTE

A User's Guide to IC Instrumentation Amplifiers

by Jeffrey R. Riskin
Manager of Microcircuits Applications Engineering

INTRODUCTION

It is traditional to begin a discussion of instrumentation amplifiers by saying that an IA is not an operational amplifier. As obvious as this statement is to the informed user, and as awkward as a description by exclusion may be, such an approach is inevitable and perhaps necessary. When an engineer needs a signal conditioning gain block, the first thought that springs to mind is the nearly ultimate flexibility provided by the currently available assortment of low-cost IC op amps. It may well be that an op amp will suffice as an element in a given gain block, but in demanding applications, op amp circuitry will often require extensive and expensive additional circuit elements, specialized manufacturing and/or test instrumentation together with highly skilled personnel to make it all work. The purpose of this article is to explain when and where an instrumentation amplifier may best be employed and where its unique virtues give it an advantage over the more flexible op amp.

WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a precision differential voltage gain device that is optimized for operation in an environment hostile to precision measurement. The real world is characterized by deviations from the ideal; temperature fluctuates, electrical noise exists, and voltage drops caused by current through the resistance of leads from remote locations are dictated by the laws of physics. Furthermore, real transducers rarely exhibit zero output impedance and nice neat zero-to-ten-volt ranges. Induced, leaked or coupled electrical interference (noise) is always present to some extent. In brief, even the best "cookbook" must be taken with a grain of salt.

Instrumentation amplifiers are intended to be used whenever acquisition of a useful signal is difficult. IA's must have extremely high input impedances because source impedances may be high and/or unbalanced. Bias and offset currents are low and relatively stable so that the source impedance need not be constant. Balanced differential inputs are provided so that the signal source may be referenced to any reasonable level independent of the IA output load reference. Common mode rejection, a measure of input balance, is very high so that noise pickup and ground drops, characteristic of remote sensor applications, are minimized.

Care is taken to provide high, well-characterized stability of critical parameters under varying conditions, such as changing temperatures and supply voltages. Finally, all components that are critical to the performance of the IA are internal to the device (with the exception of a single gain-determining resistor or resistor-pair). The manufacturer may then optimize, characterize and guarantee the specifications, while the user may in turn depend on a certain level of performance without having to provide his own precision application components or design expertise.

The precision of an IA is provided at the expense of flexibility. By committing to the one specific task of amplifying voltage, the IA manufacturer may optimize performance in this area. An IA is not intended to perform integration, differentiation, rectification, or any other non-voltage-gain function; although possible with an IA, these tasks are best left to operational amplifiers.

To put an instrumentation amplifier to work, the potential user does not require an intimate knowledge of its internal construction. Figure 1, a functional diagram of a basic IA, provides sufficient information for many applications.

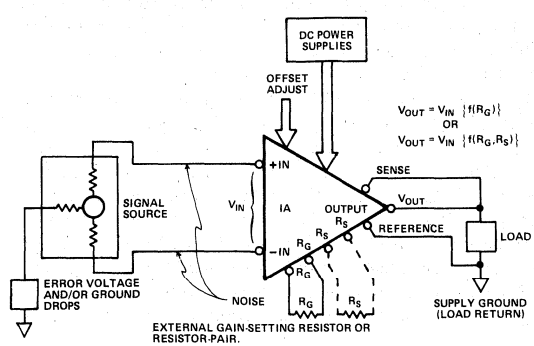


Figure 1. Basic Instrumentation Amplifier Functional Diagram

The two inputs shown permit direct interface to "floating" signal sources. The IA, being truly differential, detects only the difference in voltage between its inputs; any common-mode signals (signals present on both inputs), such as noise

and voltage drops in ground lines, are subtracted and cancelled at the inputs before amplification takes place.*

A single resistor or resistor-pair is used to program the IA for the desired gain. The manufacturer will provide a transfer function or gain equation that allows the user to calculate the required values of resistance for a given gain. Special requirements for that resistor or resistors, if any, are also spelled out by the manufacturer.

The output is single-ended and is designed to drive ground-referenced loads as normally found in measurement equipment. The load reference is common to the power supply return although careful consideration must be given to the overall grounding system (more on that later).

Of course, power must be supplied to the IA; as with op amps, this is normally a differential balanced voltage that may be varied over a specified range.

Most instrumentation amplifiers provide some means of adjusting offset voltage (that dc error voltage present at the output when both inputs are grounded). This adjustment is usually made by varying the setting of an external potentiometer. Sense and reference terminals allow remote sensing of output voltage so that effects of IR drops and ground drops may be minimized. For low current non-remote loads, the sense terminal may be tied directly to the output while the reference terminal may be tied to power supply common. There are other uses for sense and reference that will be discussed in the applications section of this article.

INSIDE AN INSTRUMENTATION AMPLIFIER

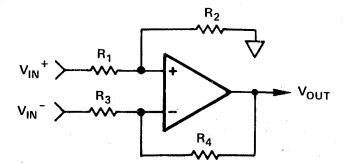
While there are many ways of designing an instrumentation amplifier, most such designs can be classified into one of two categories. The most common configuration consists of a number of interconnected operational amplifiers and a precision resistor network. This technique is popular in modular and hybrid instrumentation amplifiers where most practical designs utilize a minimum number of components. Examples are the modular Analog Devices model 605 and hybrid AD522 IA's.

In the other category are designs that, instead of employing op amps, use fundamental active-circuit elements, such as differential circuits and controlled current sources and reflectors; this eliminates all unnecessary or redundant features and tends to minimize active device (transistor) count and decrease the dependence upon accurate resistor matching. This technique is most often employed in the design of monolithic IA's where cost is inversely proportional to chip size. Examples are the monolithic Analog Devices AD520 and AD521 IC IA's. Some older modular IA's (such as the Analog Devices models 602 & 603) also use this technique because suitably precise IC op amps have only recently become readily available. Newer modular IA's may also use this technique because nonlinearity tends to be lower at high gains, although some sacrifice of linearity may exist at lower gains. Examples are the Analog Devices models 606 & 610.

Op Amp Based IA's

The most simple (and crude) method of implementing a differential gain block with op amps is shown in Figure 2.

*For applications involving extremely high common-mode voltages, or requiring complete galvanic isolation, *isolation amplifiers* should be used. Analog Devices manufactures a complete line of single and multi-channel isolators.



$$V_{OUT} = V_{IN}^{+}\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_3+R_4}{R_3}\right) - V_{IN}^{-}\left(\frac{R_4}{R_3}\right)$$

Figure 2. Differential Input Voltage Gain Block (Simple Subtractor)

In this circuit, an expressions for V_{OUT} can be derived by superposition.

The output for V_{IN}^{+} (V_{IN}^{-} grounded) is:

$$V_{O_1} = V_{IN}^{+}\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_3+R_4}{R_3}\right) \quad (1)$$

The output for V_{IN}^{-} (V_{IN}^{+} grounded) is:

$$V_{O_2} = -V_{IN}^{-}\left(\frac{R_4}{R_3}\right) \quad (2)$$

By superposition:

$$V_O = V_{O_1} + V_{O_2}$$
$$= V_{IN}^{+}\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_3+R_4}{R_3}\right) - V_{IN}^{-}\left(\frac{R_4}{R_3}\right) \quad (3)$$

If $R_2 = R_4$, $R_1 = R_3$:

$$V_O = \left(V_{IN}^{+} - V_{IN}^{-}\right)\frac{R_4}{R_3} \quad (4)$$

Thus, we have created a simple differential voltage amplifier. The input impedances, however, are low and unequal. Furthermore, all 4 resistors have to be carefully ratio-matched to maintain good common mode rejection:

$$V_{OUT\,CM} = V_{OUT} \text{ for } V_{IN}^{+} = V_{IN}^{-}$$
$$= V_{IN}\left[\left(\frac{R_2}{R_1+R_2}\right)\left(\frac{R_3+R_4}{R_3}\right) - \left(\frac{R_4}{R_3}\right)\right] \quad (5)$$

If we are looking for a gain of 1, all resistors will be equal. For a 0.1% mismatch in just one of the resistors:

$$R_1 = R_3 = R_4 = R$$
$$R_2 = 0.999R$$
$$V_{O\,CM} = V_{IN}\left[\left(\frac{0.999R}{1.999R}\right)\left(\frac{2R}{R}\right) - \left(\frac{R}{R}\right)\right]$$
$$= 0.0005V_{IN} \quad (6)$$
$$CMR = 66dB$$

(Note that if the source resistance is not low and balanced, gain and CMR will be further degraded.)

Considering what is available in the way of reasonably priced standard resistors, one can hardly expect to improve upon this mediocre level of performance. Considering the several serious drawbacks, it is not surprising that this configuration is not used in true instrumentation amplifier designs.

The two-amplifier approach shown in Figure 3 overcomes some of the weaknesses inherent in the simple subtractor of Figure 2.

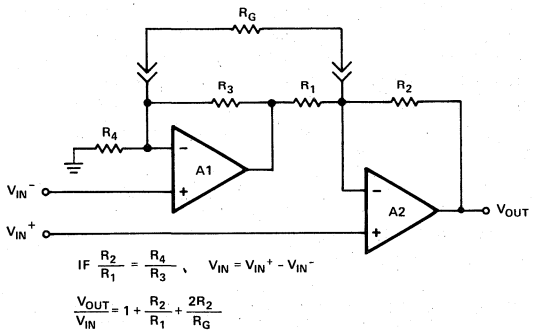


Figure 3. "Two-Amplifier" Instrumentation Amplifier

Input resistance is high, thus permitting the signal sources to have unbalanced, non-zero output impedance. Furthermore, gain may be changed by switching only one resistor thus allowing CMR to remain constant once initial trimming is accomplished. (CMR is still dependent upon the ratio-matching of four resistors.) The major disadvantage to this design is that the common mode voltage input range is a function of gain and can thus be very poor. By referring to Figure 3, it can be seen that A1 is called upon to amplify a common mode signal by the ratio $(R_3 + R_4)/R_4$; this could lead to saturation of A1 thus leaving no "headroom" to amplify the differential signal of interest. A few modules and hybrids use this configuration because of its simplicity, but it is not optimal.

The most popular configuration for op-amp based instrumentation amplifiers is shown in Figure 4:

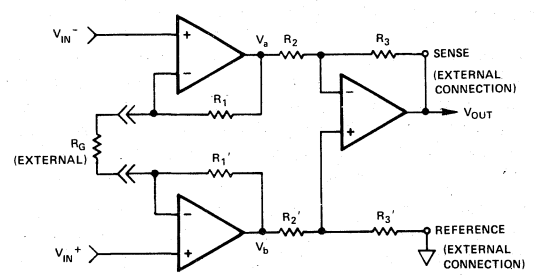


Figure 4. "Classic" 3 Op Amp Instrumentation Amplifier

The transfer function of this circuit can be calculated by superposition.

For $V_{IN}^+ = 0$

$$V_a = V_{IN}^- \left(\frac{R_1 + R_G}{R_G}\right) \quad (7)$$

$$V_b = V_{IN}^- \left(\frac{R_1'}{R_G}\right) \quad (8)$$

For $V_{IN}^- = 0$

$$V_a = V_{IN}^+ \left(\frac{R_1}{R_G}\right) \quad (9)$$

$$V_b = V_{IN}^+ \left(\frac{R_1' + R_G}{R_G}\right) \quad (10)$$

$$\therefore \quad V_a = V_{IN}^- \left(\frac{R_1 + R_G}{R_G}\right) - V_{IN}^+ \left(\frac{R_1}{R_2}\right) \quad (11)$$

$$\text{and } V_b = V_{IN}^+ \left(\frac{R_1' + R_G}{R_G}\right) - V_{IN}^- \left(\frac{R_1'}{R_G}\right) \quad (12)$$

$$V_{OUT} = -\left(\frac{R_3}{R_2}\right) V_a + V_b \left(\frac{R_3'}{R_2' + R_3'}\right)\left(\frac{R_3 + R_2}{R_2}\right) \quad (13)$$

If $R_3 = R_3'$, $R_2 = R_2'$, and $R_1 = R_1'$

$$V_{OUT} = (V_b - V_a)\left(\frac{R_3}{R_2}\right) \quad (14)$$

substituting for V_b and V_a and simplifying

$$V_{OUT} = (V_{IN}^+ - V_{IN}^-)\left(\frac{2R_1}{R_G} + 1\right)\left(\frac{R_3}{R_2}\right) \quad (15)$$

In this configuration, gain accuracy and CMR still depends upon the ratio-matching of R_2, R_2', R_3 and R_3'. It can be shown, however, that CMR does *not* depend on the matching of R_1 and R_1'.

$$V_{CM\ OUT} = (V_a - V_b) = V_{IN}^+ \left(\frac{R_1 + R_G}{R_G}\right) - V_{IN}^- \left(\frac{R_1}{R_G}\right) - V_{IN}^- \left(\frac{R_1' + R_G}{R_G}\right) + V_{IN}^+ \left(\frac{R_1'}{R_G}\right) \quad (16)$$

but $V_{CM\ IN} = V_{IN}^+ = V_{IN}^-$

$$V_{CM\ OUT} = V_{CM\ IN}\left[\frac{R_1 + R_G}{R_G} - \frac{R_1}{R_G} - \frac{R_1' + R_G}{R_G} + \frac{R_1'}{R_G}\right] \quad (17)$$

$$= V_{CM\ IN}\left[\frac{R_1}{R_G} - \frac{R_1}{R_G} + 1 - \frac{R_1'}{R_G} + \frac{R_1'}{R_G} - 1\right] \quad (18)$$

$$= V_{CM\ IN}\left[0\right]$$

$$= 0$$

Therefore, in theory at least, the user may take as much gain in the front end as he wishes (as determined by R_G) without increasing the common mode error signal. Thus, CMRR will theoretically increase in direct proportion to gain, a very useful property. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain because no common-mode voltage will appear across R_G, hence, no common-mode current will flow in it (the input terminals of an op-amp operating normally will have no significant potential difference between them). This means that large common-mode signals may be handled independent of gain.

Finally, because of the symmetry of this configuration, first order common-mode error sources in the input amplifiers, if they track, tend to be cancelled out by the output stage subtractor. These features explain the popularity of this IA design technique; examples include the Analog Devices

module model 605 and the hybrid AD522. Both of these products are characterized by their extremely high precision.

IA's of this type may use either FET or Bipolar input operational amplifiers. FET input devices have very low bias currents and are well-suited for use with very high source impedances. FET input op amps, however, generally have poorer CMR than bipolar amplifiers due to non-geometry related mis-matches. (In other words, matching of FET's is largely a function of process control; matching bipolar transistors is less process dependent.) This will manifest itself in lower linearity and CMR for large input voltages. Furthermore, these mis-matches usually cause larger input offset voltage drifts. For these reasons, Analog Devices instrumentation amplifiers use bipolar input stages thus sacrificing low bias currents to achieve high linearity and CMR along with low input offset voltage drift. As technology develops, FET input IA's may become more viable.

Dedicated Design IA's

The second category of IA design is based on minimum active device count; a virtue for monolithic IC circuits. The basic schematic for such a design is shown in Figure 5.

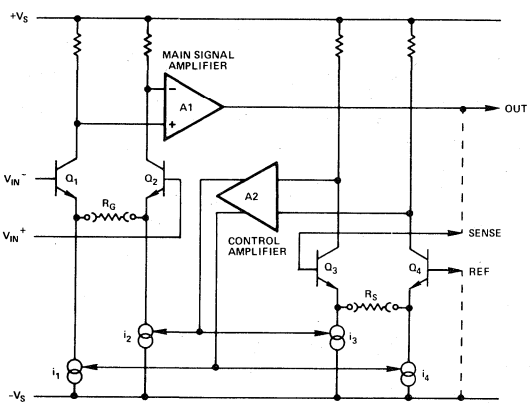


Figure 5. Typical IC IA Basic Schematic

Forward gain is provided by the input differential stage Q_1 and Q_2 whose current gain (transconductance) is $1/R_G$ (amps/volt) and the main signal amplifier A_1 which senses differences in input stage collector currents. When the output is connected back to sense (with reference grounded) differential stage Q_3 and Q_4 acts as a feedback error-sensing amplifier with a transconductance of $1/R_S$ (amps/volt). A_2 senses the collector current imbalance in that stage.

When a differential voltage is applied to the inputs, the collector currents of Q_1 and Q_2 tend to become unbalanced by $(V_{IN}^+ - V_{IN}^-)/R_G$. This is sensed by A_1 which develops an error voltage between the sense and reference points. This, in turn, tries to unbalance the collector currents in Q_3 and Q_4 by $(V_{SENSE} - V_{REF})/R_S$. That unbalance is sensed by A_2 which then adjusts I_3 and I_4 to equalize the collector currents in Q_3 and Q_4 ($I_4 - I_3 = (V_S - V_R)/R_S$). A_2 simultaneously adjusts I_1 and I_2 such that $I_1 - I_2 = I_4 - I_3$. Balance is reached when:

$$\frac{V_S - V_R}{(I_4 - I_3)\,R_S} = \frac{V_1 - V_2}{(I_1 - I_2)\,R_G} \qquad (19)$$

$$\text{if } \frac{V_S - V_R}{V_1 - V_2} = \frac{V_{OUT}}{V_{IN}} = \text{Gain} \qquad (20)$$

and $I_4 - I_3 = I_1 - I_2$

$$\text{Gain} = \frac{R_{SCALE}}{R_{GAIN}} \qquad (21)$$

It is apparent from this analysis that the requirement for carefully matched resistors changes to a requirement for carefully matched active devices. In IC technology, this is possible by utilization of precision photographic techniques along with careful design layout and well-controlled processing. The result is a good trade-off between high performance and low cost.

This design configuration describes the Analog Devices AD520, the industry's first monolithic IC IA. The AD521 is a second-generation monolithic IA offering improved performance at a reduced cost.*

INSTRUMENTATION AMPLIFIER SPECIFICATIONS

To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a spec sheet are of little value if the user doesn't have a clear picture of what each spec means. In this section, a typical instrumentation amplifier specification sheet will be reviewed. Each individual specification will be discussed in terms of how it is measured and what error it might contribute to the overall performance of the circuit. In some cases, a given specification may not affect a particular application; the more common situations of this type will be discussed.

Table I is the specification sheet for the Analog Devices AD522 instrumentation amplifier, chosen for its rather complete characterization and its variety of available versions.

At the top of the spec sheet is the statement that the listed specs are typical @ $V_S = \pm 15V$, $R_L = 2k\Omega$ and $T_A = +25^\circ C$ unless otherwise specified. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature) the significant effects are usually indicated within the specs. This statement also tells us that all numbers are typical unless noted; "typical" means that the manufacturers characterization process has shown this number to be average, but individual devices may vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Those specs do not apply uniquely to instrumentation amplifiers.

Gain

These specs relate to the transfer function of the device.

$$\text{Gain Equation: } G = 1 + \frac{2(10^5)}{R_G} \qquad (22)$$

To select an R_G for a given gain, solve the equation for R_G

$$\text{(in ohms): } R_G = \frac{200{,}000}{G - 1} \qquad (23)$$

*The AD521 data sheet, available from Analog Devices, offers a complete circuit description along with specifications and applications of this versatile device.

TABLE I.
AD522 SPECIFICATIONS

(Typical @ $+V_S = \pm 15V$, $R_L = 2k\Omega$ & $T_A = +25^\circ C$ unless otherwise specified)

MODEL	AD522A	AD522B	AD522S
GAIN			
Gain Equation	$1 + \frac{2(10^5)}{R_G}$	*	*
Gain Range	1 to 1000	*	*
Equation Error			
G = 1	0.2% max	0.05% max	**
G = 1000	1.0% max	0.2% max	**
Nonlinearity, max			
G = 1	0.005% of F.S. (±10V)	0.001%	**
G = 10	0.006% of F.S. (±10V)	0.0025%	**
G = 100	0.01% of F.S. (±10V)	0.005%	**
Gain vs. Temp, max			
G = 1	2ppm/°C (1ppm/°C typ)	*	*
G = 1000	50ppm/°C (25ppm/°C typ)	*	*
OUTPUT CHARACTERISTICS			
Output Rating	±10V @ 5mA min	*	*
DYNAMIC RESPONSE			
Small Signal (-3dB)		*	*
G = 1	300kHz	*	*
G = 100	3kHz	*	*
Full Power GBW	1.5kHz	*	*
Slew Rate	0.1V/μs	*	*
Settling Time to 0.1%, G = 100	0.5ms	*	*
to 0.01%, G = 100	5ms	*	*
to 0.01%, G = 10	2ms	*	*
to 0.01%, G = 1	0.5ms	*	*
VOLTAGE OFFSET			
Offsets Referred to Input			
Initial Offset Voltage (adj. to 0)			
G = 1	±400μV max (±200μV typ)	±200μV max (±100μV typ)	±200μV max (±100μV typ)
vs. Temperature, max			
G = 1	±50μV/°C(±10μV/°C typ)	±25μV/°C(±5μV/°C typ)	±100μV/°C(±10μV/°C typ)
G = 1000	±6μV/°C	±2μV/°C	±6μV/°C
1<G<1000	$\pm\left(\frac{50}{G} + 6\right)\mu V/^\circ C$	$\pm\left(\frac{25}{G} + 2\right)\mu V/^\circ C$	$\pm\left(\frac{100}{G} + 6\right)\mu V/^\circ C$
vs. Supply, max			
G = 1	±20μV/%	*	*
G = 1000	±0.2μV/%	*	*
INPUT CURRENTS			
Input Bias Current			
Initial max, +25°C	±25nA	±15nA	±25nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
Input Offset Current			
Initial max, +25°C	±20nA	±10nA	±20nA
vs. Temperature	±100pA/°C	±50pA/°C	±100pA/°C
INPUT			
Input Impedance			
Differential	$10^9\ \Omega$	*	*
Common Mode	$10^9\ \Omega$	*	*
Input Voltage Range			
Minimum Differential Input	±10V	*	*
Maximum Differential Input	±20V	*	*
Maximum Common Mode Linear	±10V	*	*
Maximum Common Mode Input	±15V	*	*
Common Mode Rejection			
Min @ ±10V, 1kΩ Source Imbalance			
G = 1 (dc to 30Hz)	75dB (90dB typ)	80dB (100dB typ)	75dB (90dB typ)
G = 10 (dc to 10Hz)	90dB (100dB typ)	95dB (110dB typ)	90dB (110dB typ)
G = 100 (dc to 3Hz)	100dB (110dB typ)	100dB (120dB typ)	100dB (120dB typ)
G = 1000 (dc to 1Hz)	100dB (120dB typ)	110dB (>120dB typ)	100dB (>120dB typ)
G = 1 to 1000 (dc to 60Hz)	75dB (88dB typ)	80dB (88dB typ)	*
NOISE			
Voltage Noise, RTI			
0.1Hz to 100Hz (p-p)			
G = 1	15μV	*	*
G = 1000	1.5μV	*	*
10Hz to 10kHz (rms)			
G = 1	15μV	*	*
TEMPERATURE RANGE			
Specified Performance	-25°C to +85°C	*	-55°C to +125°C
Operating	-55°C to +125°C	*	*
Storage	-65°C to +150°C	*	*
POWER SUPPLY			
Power Supply Range	±(5 to 18)V	*	*
Quiescent Current, max @ ±15V	±10mA	±8mA	±8mA

*Specifications same as AD522A **Specifications same as AD522B Specifications subject to change without notice.

For example:

$G = 1 \quad : R_G = \infty$ (open circuit)

$G = 10 \quad : R_G = 22{,}222\Omega$

$G = 100 \quad : R_G = 2020.2\Omega$

$G = 1000: R_G = 200.20\Omega$

Of course the user must provide a very clean circuit board to realize an accurate gain of 1 since 200MΩ leakage resistance will cause a gain error or 0.1%.

Gain Range

Specified at 1 to 1000, this device may (and in fact will) work at higher gains, but the manufacturer will not promise any particular level of performance. In practice, noise and drift may make higher gains impractical for this device.

Equation Error

The number given by this specification describes maximum deviation from the gain equation. The user can trim the gain (above unity) or can compensate elsewhere in his design. If his data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), he might be able to correct for gain errors by measuring a reference and multiplying by a constant.

Nonlinearity

Nonlinearity is defined as the deviation from a straight line on the plot of output versus input. Figure 6a shows the transfer function of a device with exaggerated nonlinearity. The magnitude of this error can be calculated thus:

$$\text{N. L.} = \left[\frac{\text{Actual Output - Calculated Output}}{\text{Rated Full-Scale Output Range}} \right]$$

To confuse matters, this deviation can be specified relative to *any* straight line or to a specific straight line. There are two commonly-used methods of specifying this ideal straight line relative to the performance of a precision measurement device.

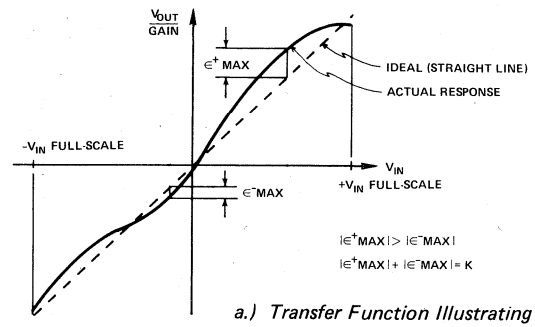
The "Best Straight Line" method of nonlinearity specification consists of measuring the peak positive and negative deviations and adjusting the slope of the device transfer function (by adjusting the gain and offset) so that these maximum positive and negative errors are equal. This method yields the best specifications but is difficult to implement in that it requires that the user examine the entire output signal range to determine these maximum positive and negative deviations. The results of a best-straight-line calibration is shown by the transfer function of Figure 6b.

The "End-Point" method of specifying nonlinearity requires that the user perform his offset and/or gain calibrations at the extremes of the output range. This is much easier to implement but may result in nonlinearity errors of up to twice these attained with best-straight-line techniques. This worst case will occur when the transfer function is "bowed" in one direction only. Figure 8c shows the results of end-point calibration.

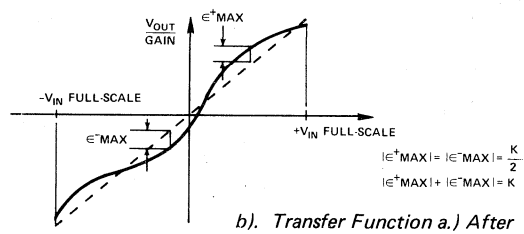
Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. The user must take this into consideration when evaluating the error budget for his application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say that these errors are neither fixed nor proportional to input or output voltage and can not be reduced by adjustment.

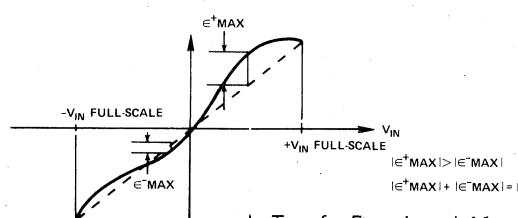
Referring to the AD522 specifications, the larger number at G = 100 indicates that in the AD522, nonlinearity increases with gain.



a.) Transfer Function Illustrating Exaggerated Nonlinearity



b). Transfer Function a.) After Calibration by Best-Straight-Line Method



c). Transfer Function a.) After Calibration by End-Point Method

Figure 6. Nonlinear Transfer Function

Gain vs. Temperature

These numbers give both maximum and typical deviations from the gain equation as a function of temperature. An intelligent system can correct for this with an "auto-gain" cycle (measure a reference and re-normalize).

Settling Time

Settling time is defined as that length of time required for the output voltage to approach and remain within a certain tolerance of its final value. It is usually specified for a fast full scale input step and includes output slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% doesn't necessarily mean proportionally fast-settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors

include slew rate limiting, under-damping (ringing) and thermal gradients ("long tails").

Voltage Offset

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage could cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

Input Bias Currents

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. FET input devices have lower bias currents, but those currents increase dramatically with temperature, doubling approximately every 11°C. Since bias currents can be considered as a source of voltage offset (when multiplied by source resistance), the change in bias currents is of more concern than the magnitude of the bias currents. Input offset current is the difference between the two input bias currents.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.

Common-Mode Rejection

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-mode rejection ratio" (CMRR) is a ratio expression while "common-mode rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In most IA's the CMRR increases with gain. This is because most designs have a front-end configuration that does not amplify common-mode signals. Since the standard for CMRR specifications is referred to the output (RTO), a gain for differential signals in the total absence of gain for common-mode output signals will yield a 1-to-1 improvement of CMRR with gain. This means that the common-mode output error signal will not increase with gain, it does not mean that it decreases with gain! At higher gains, however, amplifier bandwidth decreases. Since differences in phase-shift through the differential input stage will show up as a common-mode error, CMRR becomes more frequency dependent at high gains.

Error Budget Analysis

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD522 is required to amplify the output of an unbalanced transducer.

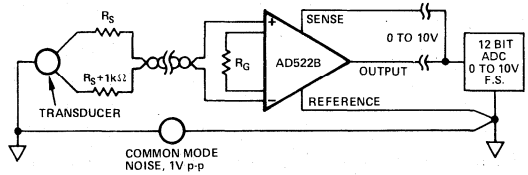


Figure 7. Typical AD522B Application

Figure 7 shows a differential transducer, unbalanced by 1kΩ, supplying a 0 to 1 volt signal to a remotely located AD522B. The output of the IA feeds a 12 bit A to D converter with a 0 to 10 volt input voltage range. There is 1 volt of peak-to-peak 0 to 10Hz noise on the ground return appearing as a common-mode signal at the inputs of the IA. The operating temperature range is -25°C to +85°C; calibration is performed at +25°C.

The input signal must be amplified by a factor of 10 in order to utilize the full resolution of the A to D converter. Solving the gain equation for G = 10 gives a value of 22.22kΩ for R_G.

Table II lists all applicable error sources and their corresponding effects on accuracy. Initial errors are defined as those errors that can be reduced to a negligible amount by performance of an initial calibration.

Reducible errors include these initial errors along with other errors that occur during normal operation that may be corrected by an adaptive or "intelligent" system. For example, changes in gain or offset may be measured during an auto-zero/auto-gain cycle by measuring two known voltages (a precision reference and ground, for example). This is a common practice in computer or processor-controlled equipment.

Irreducible errors are errors which can not be readily corrected either at initial calibration or in use. It could be argued that an array of precision references would permit a software linearity correction, but in most applications that would be unrealistically cumbersome.

The total error "as built" is approximately 5540ppm or 0.55%. If an initial calibration is performed, this number is reduced by 2210ppm to 3330ppm = 0.33%. Note that 3000ppm of this is gain drift.

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (57.8ppm = 0.006%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.006%.

In the above example, the system can justifiably make use of a 13 bit A to D converter for its differential linearity and

TABLE II.
AD522B ERRORS

Error Source	AD522B Specs	Calculation	Initial Effects on Accuracy (May be Calibrated)	Reducible Effects on Accuracy (Correctable by "Intelligent" System)	Irreducible Effects on Accuracy
Gain Error	±0.2%	±0.2% = ±2000ppm	±2000ppm	±2000ppm	–
Gain Instability	±50ppm/°C	(±50ppm)(85°C -25°C) = ±3000ppm	–	±3000ppm	–
Gain Nonlinearity	±0.0025%	±0.0025% = ±25ppm	–	–	±25ppm
Offset Voltage	±200μV, RTI	±200μV/1V = ±200ppm	±200ppm	±200ppm	–
Offset Voltage Drift	±4.5μV/°C	(4.5μV/°C)(85°C -25°C) = 270μV/1V = 270ppm	–	±270ppm	–
Offset Current	±10nA	[±10nA][1kΩ] = ±10μV = ±10ppm	±10ppm	±10ppm	–
Offset Current Drift	±50pA/°C	[±50pA][85°C -25°C][1kΩ] = ±3μV = ±3ppm	–	±3ppm	–
Common Mode Rejection	95dB	-95dB = 20 log ϵ ϵ = 0.0000178 = 17.8ppm	–	–	±17.8ppm
Noise	15μV p-p (0.1Hz to 100Hz)	15μV/1V = 15ppm	–	–	±15ppm
Totals			2210ppm	5483ppm	57.8ppm

resolution. Dynamic range exceeds 84dB (14 bits). Absolute accuracy depends on calibration and system interaction capabilities; it might be as good as the resolution (0.006%) or as poor as the initial accuracy (0.55%).

INSTRUMENTATION AMPLIFIER APPLICATIONS

General Considerations

Whenever a precision high-gain device—such as an instrumentation amplifier—is used, certain precautions apply. Obviously, it is wise to have a clean layout, short wire runs where possible and a carefully considered grounding scheme. Figure 8 shows a well-thought out approach to IA interconnection.

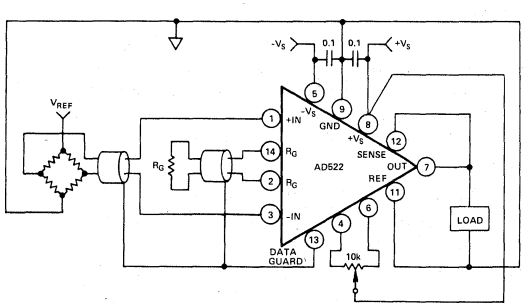


Figure 8. AD522 Interconnection

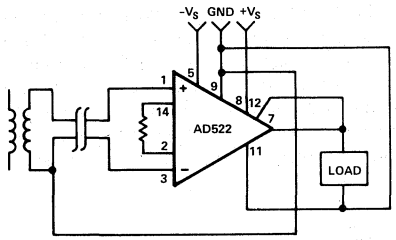
A properly designed instrumentation amplifier exhibits low sensitivity to power supply variations; the AD522, for example, shows an RTI offset variation of only 0.2μV per percent of power supply change at G = 1000. At increasing frequencies, however, this rejection factor will degrade as internal capacitances permit more power supply noise to find its way into the signal path. This effect can be minimized by bypassing the power supplies, as close to the IA as possible, with 0.1μF ceramic disc capacitors. Larger tantalum capacitors would be effective against lower frequency variations, but a competent IA is capable of rejecting most of these slower changes.

The offset adjustment pot usually affects the balance of the high gain differential input stage. Short wire runs to this pot will minimize injection of noise into a sensitive location.

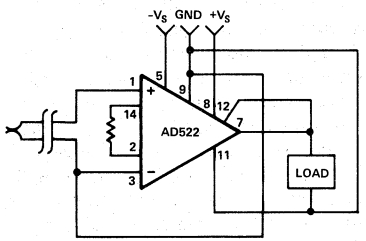
The gain-determining resistor, R_G, is often remotely located for purposes of gain switching. A well-designed IA will tolerate this to a certain extent, but stray capacitances and wiring inductance may disturb the frequency compensation of the device. Sometimes it becomes necessary to install a series RC right at the R_G terminals of the IA to add a compensating zero to correct for LC resonances caused by stray inductances and capacitances. This lead compensation may improve stability at the cost of a peak in the frequency response curve at the high end. Unfortunately, this compensation, if required, depends on the individual application and is usually determined experimentally.

Most IA's are provided with "sense" and "reference" outputs. While there are several interesting uses for these features (to be discussed later), the most basic application is remote load sensing. This essentially puts the IR drops "inside the loop" of the IA and is most useful when driving remote and/or heavy loads or when the load ground is not firmly "anchored" to the power supply returns.

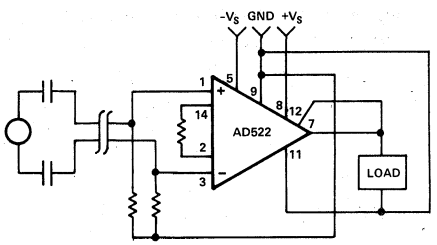
Grounding is a topic worthy of its own application note (see "An IC Amplifier User's Guide to Decoupling, Grounds, etc." by A. P. Brokaw). In the case of instrumentation amplifiers, the main thing to remember is that all signal and power returns must eventually have a direct or indirect common point. Direct coupling of IA inputs make it necessary to provide signal ground returns for input amplifier bias currents. Figure 8 shows a direct connection. If a "floating" source or ac coupling is used, indirect returns similar to those shown in Figure 9 must be provided.



a). Transformer Coupled



b). Thermocouple



c). AC Coupled

Figure 9. Indirect Ground Returns for "Floating" Transducers

Signals from remote transducers are often transmitted to the IA through shielded cables. While this may well serve to reduce noise pick-up, the distributed RC's in such cabling can cause differential phase shifts in those lines. When ac common-mode signals are present, these phase shifts will reduce common-mode rejection. The same effect will occur with remote R_G's located at the end of shielded cables. If the shields could be driven by the common-mode signal, the cable capacitance could be "boot-strapped" thus making the capacitance effectively zero for common-mode signals. The data guard output of the AD522 provides the common-mode component of the input signals and can be used to drive the shields of coaxial input cables and increase ac CMR. Figure 8 illustrates this connection; if not used, the data guard should be left unconnected.

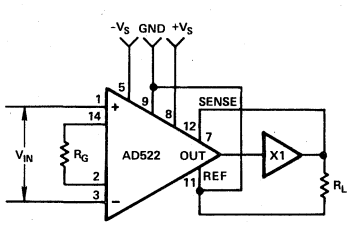


Figure 10. Current-Booster Output

Boosted Output

In the previous section, use of the sense terminal for remote load sensing was discussed. Another use of that terminal is illustrated in Figure 10.

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 10 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

Offset Load

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset.

Two caveats apply to the use of the reference pin. When the IA is of the three-amplifier configuration shown in Figure 4 (as is the AD522), it is necessary that nearly zero impedance be presented to the reference terminal. It can be shown that any significant resistance from the reference terminal to ground increases the gain of the non-inverting signal path thereby upsetting the common-mode rejection of the IA. An operational amplifier may be used to provide that low impedance reference point as shown in Figure 11. The input offset voltage characteristics of that amplifier will add directly to the offset voltage performance of the IA.

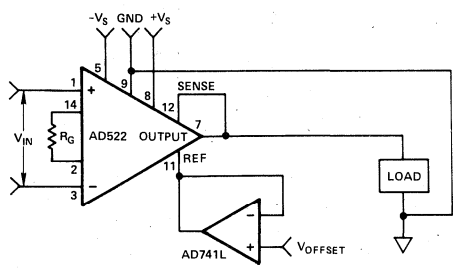


Figure 11. Use of Reference Terminal to Provide Output Offset

The other precaution is more obvious. The output voltage range of an IA is clearly specified; if that range is mostly used up by offset at the reference terminal not much range is left for the signal. In other words, the sum of the offset and signal may not exceed the specified output voltage range of the IA.

CMR Trim

The effect of resistance in the reference termination may be used to advantage. A short-term CMR improvement can be realized with the circuit shown in Figure 12.

While applying a low-frequency 20 volt peak-to-peak input signal to both inputs, the pot should be adjusted for an output null. In many cases this adjustment will not improve matters on a long-term basis since the common-mode rejection of the device is determined by the long-term stability of internal components (which will drift regardless of what happens externally).

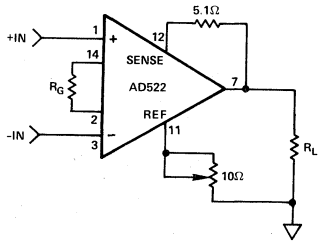


Figure 12. Common Mode Rejection Trim

Controlled Currents

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 13.

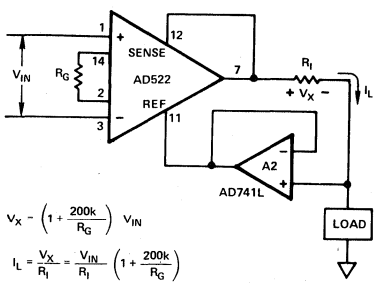


Figure 13. Voltage-To-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

CONCLUSIONS

Thus characterized, the instrumentation amplifier stands ready to take its place in the Grand Order of Things. The preliminary contention that an IA is not a special sort of operational amplifier should now be obvious. Its versatility is limited in scope but its applications are limited only by the imagination of the potential user. As a precision linear device, an IA is qualified mainly by its specifications, a full understanding of which is necessary to successfully use it to advantage. Analog Devices, as a long time supplier of components for precision measurement applications, offers a full spectrum of instrumentation amplifiers in modular, hybrid and monolithic IC form, each ideally suited to particular applications. We hope that this article will help clarify the issues involved and will aid in the selection of a suitable device for a particular application.

Interfacing the AD558 DACPORT™ to Microprocessors

by Doug Grant

The AD558 represents a major breakthrough in monolithic DAC technology. It is a true complete 8-bit unit including reference, output amplifier, and data latch on a single chip designed to operate from a single positive power supply. Figure 1 shows the block diagram of the device. The internal reference is a 1.2 volt bandgap type. The actual digital-to-analog conversion is accomplished by means of eight PNP current switches driving a precision thin-film R/2R ladder network to produce a direct unbuffered 0 to 400 millivolt analog signal. The high-speed output amplifier provides pin-selectable output scales of 0 to 2.56 volts and 0 to 10.00 volts. Settling time of the voltage output is typically 700 nanoseconds for a full-scale step, and the resistive pulldown output stage with a proprietary anti-saturation driver provides single-supply operation.

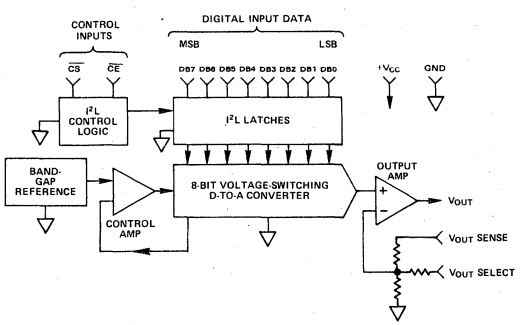


Figure 1. AD558 Functional Block Diagram

The PNP current switches are driven from the outputs of the octal data latch. This latch is fabricated using Analog Devices' linear-compatible-I^2L technology. This process provides a dense, low-power logic family which can be produced without compromising the linear components necessary for converter design.

The latch is operated from two TTL-compatible control signals, $\overline{CS}$ and $\overline{CE}$. Figure 2 shows the truth table for the latch. The $\overline{CS}$ and $\overline{CE}$ inputs are interchangeable, and the latch is transparent when both $\overline{CS}$ and $\overline{CE}$ are low. When either control input returns high, the eight-bit data word is latched and the analog output is unaffected by further activity on the data lines. This latch permits simple interface to many popular microprocessors, as will be shown in the remainder of this application note.

Input Data	$\overline{CE}$	$\overline{CS}$	DAC Data	Latch Condition
0	0	0	0	"transparent"
1	0	0	1	"transparent"
0	↓	0	0	latching
1	↓	0	1	latching
0	0	↓	0	latching
1	0	↓	1	latching
X	1	X	previous data	latched
X	X	1	previous data	latched

Notes: X = Does not matter

↓ = Logic Threshold at Positive-Going Transition

Figure 2. AD558 Control Logic Truth Table

GENERAL CONCEPTS

While microprocessor control signals vary widely from one architecture to the next, two conditions must be signalled to the AD558. First, the processor must indicate which memory (or I/O) location is being operated upon. An address decoder is used to provide a unique signal for each distinct address. This signal is normally applied to $\overline{CS}$ (Chip Select). Depending on system complexity, this decoding may range from direct connection to an address line to a complete decoding of all memory locations. The second signal necessary is an indication of whether the data on the bus is flowing from processor to memory (WRITE) or from memory to processor (READ). In the case of a DAC, where data is flowing from the processor, a WRITE signal is used. This signal is normally applied to the DACPORT $\overline{CE}$ (Chip Enable).

8080A Interface

The 8080A microprocessor provides two possible methods of sending data to an AD558 or other I/O port: memory-mapped or isolated I/O. Both types are useful and will be examined. In memory-mapped I/O, the I/O devices are treated as part of the memory array. This allows the full range of memory reference instructions and addressing modes to be used to manipulate the data.

The isolated I/O technique treats the I/O devices as separate system elements, accessed by READ and WRITE signals distinct from the memory READ and WRITE signals. In the 8080A, while there are 64K memory locations, there are only 256 dedicated I/O addresses. This permits simpler address decoding in some systems. The primary disadvantage of isolated I/O is that all data must pass through the accumulator. Direct transfer of data from a register (or memory) to an I/O device is not possible.

READ and WRITE signals for memory and I/O are available on the 8080A data bus at the beginning of each machine cycle and are latched externally. The latch function can be accomplished with dedicated chips such as the 8228 (see Figure 3) or a few packages of random logic (Figure 4). If an active low decoded address signal is applied to pin 10 of the AD558 ($\overline{CS}$) and the $\overline{MEMW}$ (or $\overline{OUT}$) is applied to pin 9 ($\overline{CE}$), the data will be latched and the analog output updated whenever the processor writes into the chosen address.

If, for example, a previous subroutine has generated a byte of data to be sent to the DAC, and returned this byte in the B register, a simple routine such as:

```
MOV A, B
OUT F1
```

will send the data to an AD558 residing at I/O address F1. If memory-mapped I/O is used instead, the move to the accumulator is unnecessary, and the code becomes simply:

```
LXI H, (16 BIT DAC ADDRESS)
MOV M, B
```

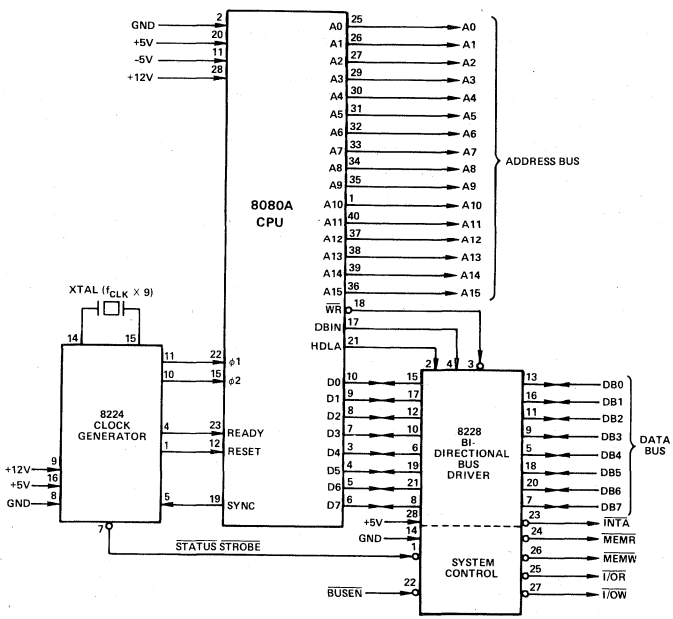


Figure 3. Control Signal Generation with 8228 System Controller

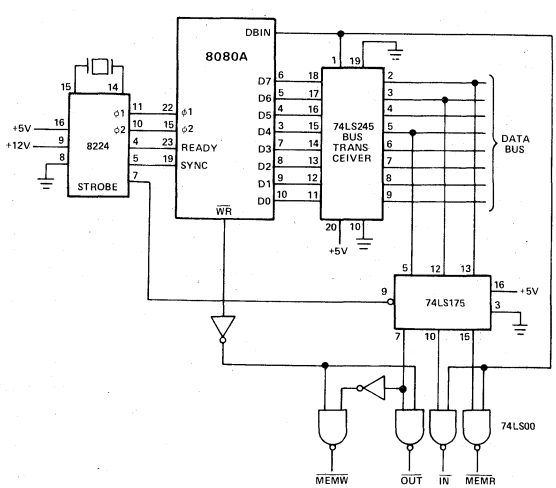


Figure 4. Control Signal Generation with Standard Logic

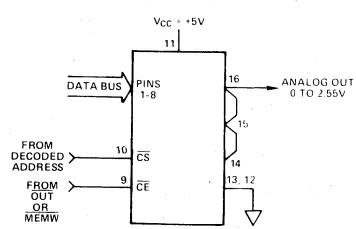


Figure 5. Control Signal Connections to AD558

8085A Interface

The 8085A is a somewhat improved version of the 8080A. It includes an on-chip clock generator requiring only a crystal (or LC or RC tuned circuit) to establish the oscillator frequency. In addition to more flexible interrupt handling capability, higher speed, and on-chip serial I/O capability, the 8085A operates from a single 5 volt power

supply. Since a complete family of 8085A compatible peripheral components and memory devices are also available for single-supply operation, it is unnecessary and inconvenient to add a negative power supply to a system just to support a DAC. For this reason, the AD558 with its single power requirement is clearly the best choice for an analog output port.

The 8085A uses a multiplexed Address/Data bus, which contains the lower 8 bits of the desired address during the first clock cycle of a machine cycle. The ALE signal is used to latch the lower half of the address. For the second and third clock cycles, the bus contains the data word.

As with the 8080A, there are two possible I/O techniques: isolated and memory-mapped. Since the upper and lower 8 bits of the address are identical in I/O operations, it is not necessary to latch the lower 8 bits and decode all 16. The IO/$\overline{M}$ signal can be used in the address decoder to signify that the address on the bus is an I/O address, not a memory location. The active low decoded address can then be applied to the AD558 $\overline{CS}$.

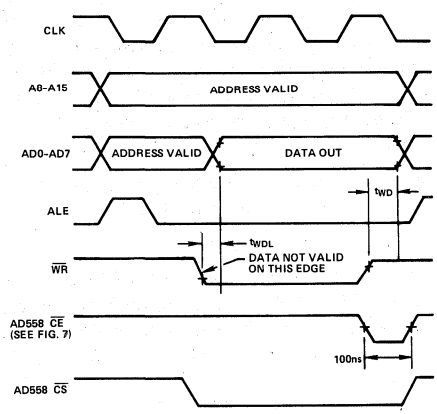


Figure 6. 8085A – AD558 Timing Diagram

The address decoding for memory-mapped I/O is slightly more complex since the total 16-bit address must be dealt with. System complexity will dictate exactly how many distinct addresses must be decoded, and in smaller systems it may be possible to locate an AD558 in a large block of otherwise vacant locations. Of course, memory-mapped I/O allows the full range of memory reference instructions to be used, while isolated I/O requires data to pass through the accumulator before being sent to the DAC.

Data validity is a subtle point when considering memory-mapped I/O, where the DAC appears as a write-only-memory. When writing to a RAM, it is permissible to have bad data on the bus during the WRITE cycle (as long as it becomes valid by the end of the operation), since the outside world is not affected by this data. However, unstable data during writes to a DAC can cause observable (and usually undesirable) activity on the output. Thus, WRITE timing for a particular processor must be closely examined to determine data validity.

The $\overline{CE}$ input of the AD558 can be driven directly from the $\overline{WR}$ of the 8085A, even though the data bus is not stable until 40 nanoseconds after the falling edge of $\overline{WR}$. Since the AD558 internal circuitry does not respond to pulses less than 60 nanoseconds wide on the data inputs, any invalid data during this 40 nanosecond period does not produce an erroneous output.

In the case of an 8085A with a heavily-loaded bus, t_{WDL} may be extended long enough to cause bad data to reach the AD558 and produce an incorrect analog output. If this temporary anomaly can be tolerated, then $\overline{WR}$ can be used to provide the DACPORT's $\overline{CE}$ input. If the output glitch is undesirable, the circuits of Figure 7 will provide valid signals for $\overline{CE}$.

Systems using the 5MHz 8085A-2 can use $\overline{WR}$ directly for $\overline{CE}$, since t_{WDL} is only 20 nanoseconds maximum. Furthermore, since t_{WD} is only 60 nanoseconds, the one-shot method shown in Figure 7a does not apply.

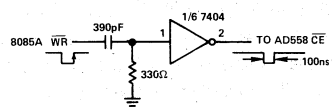


Figure 7a. AD558 $\overline{CE}$ Generated from 8085A $\overline{WR}$ Rising Edge

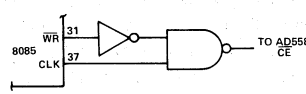


Figure 7b. $\overline{CE}$ Generated from $\overline{WR}$ and $\overline{CLK}$

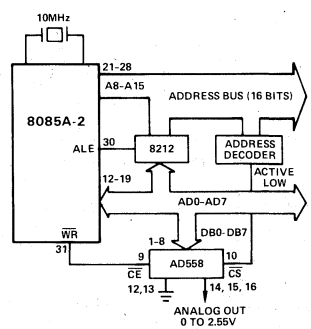


Figure 8. AD558 – 8085A Interface

8048/8748 Interface

The 8048 series of single-chip microcomputers offers two methods of I/O interfacing. The first is a modified version of the isolated I/O described for the 8080A. It differs in that the 8048 contains two decoded and latched I/O ports on the chip. The instructions OUTL P1,A and OUTL P2,A perform the functions of sending the accumulator contents to PORT 1 or PORT 2, respectively. The AD558 can reside directly on either port if pins 9 and 10 are hard-wired to a logic 0*. In this mode, the internal latch appears transparent, and activity on the data inputs causes the DAC output to change. Figure 9 shows a typical connection scheme.

*The technique of hard-wiring $\overline{CS}$ and $\overline{CE}$ low can be used with other single-chip microcomputers (such as the 6801, 3870, 6500/1, PIC1650) which feature built-in latched I/O ports. The 8048 is chosen as a representative example. The AD558 can also be used in this mode in non-μP applications.

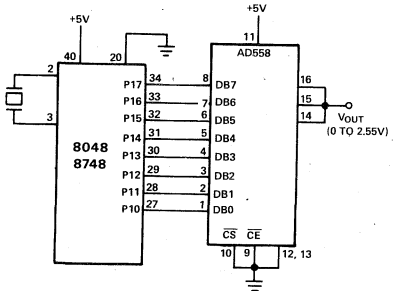


Figure 9. AD558 Connected to Dedicated I/O Port of 8048 Microcomputer

A second method of interface is necessary in 8048-based systems with more than two I/O devices. The 8048 BUS port allows system memory and I/O expansion, with the $\overline{RD}$ and $\overline{WR}$ signals controlling data flow on this bus. During a WRITE to external memory (or memory-mapped I/O devices) the falling edge of ALE latches the address from the bus. The decoded address (active low) is then applied to $\overline{CS}$ of the AD558. Since this control scheme is very similar to 8085 operation, many 8085 system components may be used. However, as with the 8085, when the $\overline{WR}$ of the 8048 goes low, data is not yet valid on the bus. The falling edge of $\overline{WR}$ occurs at least 200 nanoseconds before data is valid. The rising edge of $\overline{WR}$ should be used to trigger a one-shot whose low-going output drives the $\overline{CE}$ of the AD558.

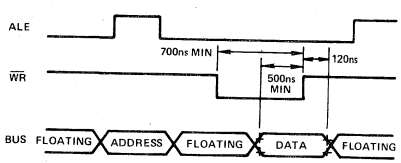


Figure 10. 8048 Timing for External Memory Write

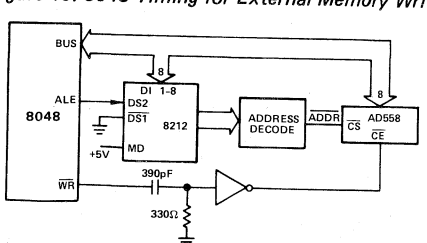


Figure 11. AD558 as External Data Memory

In this external memory mode, data is sent from the accumulator to the external memory using MOVX @ Rr, A instructions. These instructions use the RAM pointer registers R0 and R1 to point to one of 256 external memory addresses. Figures 10 and 11 demonstrate this operating mode.

6800/650X Series Interface*

The 6800 microprocessor family has only one method of data exchange to peripheral devices: memory mapping. Thus it is possible to use any address in the full 64K memory space for I/O devices. Since the address bus of the 6800 is three-state, a signal called VMA is provided to indicate that the bus contains a valid memory address. This signal normally used as a part of the address decoding logic to prevent inadvertent writes to memory at times when the address bus is being controlled by an external device (such as a DMA controller).

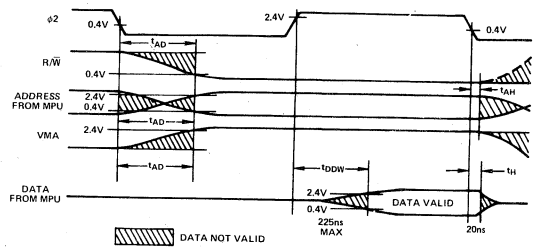


Figure 12. 6800 System Write Timing

Read/Write signaling is accomplished by use of two signals, R/$\overline{W}$ and ϕ2. The state of R/$\overline{W}$ during the up time of ϕ2 (E on 6802) determines whether a Read or Write is in progress. This requires validity of both $\overline{W}$ and ϕ2 rather than simply a $\overline{WR}$ to operate the AD558 $\overline{CE}$ input. To further complicate matters, Figure 12 shows that there is a period of time when all control signals are valid, but data is *not*. In systems where spurious outputs can be tolerated (such as de-glitched systems or systems unable to respond to sub-microsecond pulses) the control signal connection scheme of Figure 13a is sufficient.

This scheme produces a $\overline{CS}$ signal for the AD558 when VMA, ϕ2 and A15 are all high. The R/$\overline{W}$ signal is used for $\overline{CE}$.

The circuit of Figure 13b uses a 74LS221 dual one-shot triggered by ϕ2 and $\overline{W}$ validity to produce the delayed pulse necessary to operate the AD558 $\overline{CE}$ input. This delayed pulse allows only valid data into the AD558 data latch.

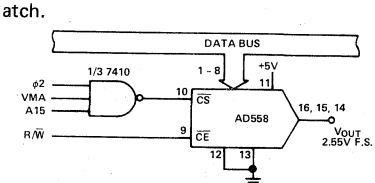


Figure 13a. Simple 6800 Interface

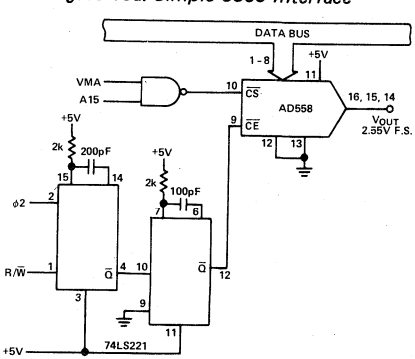


Figure 13b. Glitch-Free 6800 Interface

*Although this discussion will refer to 6800 control signals, the 650X series bus architecture is similar (with the exception of VMA which is not available on the 650X). For example, t_{DDW} (see Figure 12) is 200 nanoseconds max on the 650X.

Z80 Interface

The Z80 processor uses an instruction set which includes all the 8080A instructions as well as several other operations. It operates from a single +5 volt supply; therefore Z80-based systems do not generally have negative power supplies available to power a DAC. The AD558 is thus well suited to serve as an analog output port for such a system.

As with the 8080A, both isolated and memory-mapped I/O are possible. The isolated I/O instructions are more flexible than the 8080A IN and OUT instructions. For example, there are a total of 12 output instructions including transfers of entire blocks of register indirect addressed data and transfers of data from any internal register to a register indirect addressed I/O port.

Output signaling is accomplished with a $\overline{WR}$ signal, while $\overline{IORQ}$ and $\overline{MREQ}$ indicate whether the address on the bus is an I/O or memory address. (Note that during I/O operations only the lower 8 address bits are valid).

Timing on the Z80 is particularly convenient for AD558 interfacing, since the data bus is stable and contains valid information while $\overline{WR}$ is low. The low time of $\overline{WR}$ is 220 nanoseconds minimum for memory writes on the higher-speed Z80A, and 470 nanoseconds minimum during I/O writes. Therefore, $\overline{WR}$ can be applied directly to $\overline{CE}$.

Address decoding can be as simple or complex as the system requirements dictate. In the simplest case, shown in Figure 14, the inverse of A15 is used for the AD558 $\overline{CS}$ signal.

Complex systems might decode more address bits to further partition the memory space or use $\overline{IORQ}$ instead of $\overline{MREQ}$ to accomplish accumulator I/O.

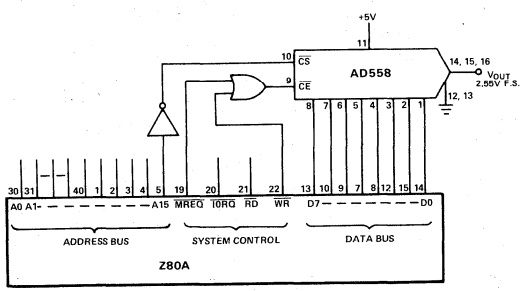


Figure 14. Z80A – AD558 Interface

1802 Interface

The 1802 CMOS microprocessor is used extensively in applications where low power consumption is critical. Many of these systems use a single supply (usually 5 volts), which makes the AD558 an ideal analog output port.

The 1802, like the 8080 series, features both accumulator and memory-mapped I/O formats. Accumulator I/O addresses appear on the N0, N1, and N2 lines with the $\overline{MRD}$ (memory read) signal indicating direction of data flow. This allows direct addressing of 14 I/O devices (device address 0 is not valid). In systems where more than 14 I/O devices are used, or where decoding of the N lines is undesirable, memory-mapped I/O is also possible. Address information on the 1802 appears on the address bus in two parts: the high-order 8 bits appear first and are latched with the falling edge of the TPA clock; the low order byte of address information then appears. The active low signal which indicates presence of the chosen address can be applied directly to the AD558 $\overline{CS}$ input. The DACPORT $\overline{CE}$ input is operated by the 1802 $\overline{MWR}$ signal. Fortunately the data is stable on the bus during the low time of $\overline{MWR}$. Figure 15 shows a generalized configuration for locating a DACPORT in the 1802 memory space.

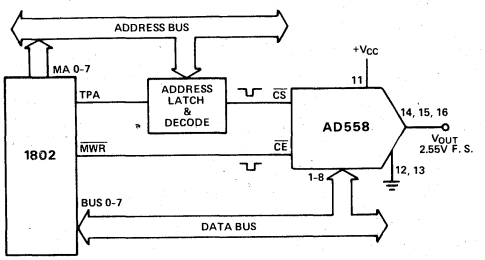


Figure 15. 1802 – DACPORT Connection

APPLICATIONS

The AD558 DACPORT can be used in any system which requires an analog output from a microprocessor bus. Several applications follow which demonstrate the capabilities of the device.

Ramp Generation

Systems such as vector graphic displays and digitally-swept VCO's require digitally-controlled analog voltage ramps. Such ramps are easily generated by an AD558 driven by a relatively simple software routine. The 8080A subroutine below accepts input arguments of initial and final ramp value in the B and C registers, and timing between steps in the D register. It is assumed that the HL register pair points to the DACPORT address when the subroutine is called. Ramp time is variable from 51 microseconds to 3.87 milliseconds per point, corresponding to full-scale sweep times of 13 milliseconds to 0.992 seconds, respectively, when this program is executed at 1MHz.

```
RAMP:   MOV A, B
        MOV M, A
        INR B
        MOV E, D
LOOP:   DCR E
        JNZ LOOP
        CMP C
        JNZ RAMP
        RET
```

Analog-To-Digital Conversion

The process of A-to-D conversion often involves comparing the (unknown) analog input signal to the output of a DAC controlled by some algorithm. Examples include the staircase or single-ramp ADC which uses a counter-driven DAC and a comparator. When the comparator detects that the DAC output has exceeded the analog input, the counter is stopped and the digital value can be read. A similar example is the tracking ADC, where the counter used is an up/down type, with its direction controlled by the comparator.

These ADC types are usually implemented in hardware using standard MSI logic, low-cost IC comparators, and DACs. The counting (or other) algorithm can just as easily be performed in software in a microprocessor system if the DAC is easily interfaced. The AD558 DACPORT offers convenient digital interfacing for such applications. Furthermore, the internal output amplifier can be operated open-loop to perform the comparator function directly.

Figure 16 shows the circuit diagram for the software-controlled ADC. The internal gain-setting resistors are used to attenuate the 10V full-scale input signal to a 0 to 400 millivolt scale and present approximately a 40kΩ load resistance to the analog input. The open-loop output amplifier slews in several tens of microseconds since it is not optimally compensated for comparator operation. The NPN buffer provides adequate current sink capability for the LSTTL tri-state buffer. It is also possible to substitute a CMOS tri-state driven directly from the DACPORT output. As shown, the DAC appears to the microprocessor as a memory location which accepts an 8-bit data word and when read back uses the LSB state to determine whether the processor's guess was higher or lower than the value of the analog input signal.

The successive-approximation algorithm is a popular method for accomplishing A to D conversion. It has the advantages of fixed conversion time regardless of analog input signal magnitude and reasonably fast conversion times. The algorithm consists of testing the MSB (most-significant-bit) to determine whether the signal resides above or below mid-scale. The result of this test determines whether the MSB should be kept or dropped. If it is kept, the next test is whether the signal is above or below 3/4 of full scale; if the MSB was dropped, the test is done at 1/4 full scale. This process repeats until all eight bits have been exercised.

The following 22 line 8080-language subroutine performs the successive-approximation algorithm with the circuit shown in Figure 16. The routine assumes that the HL register pair points to the DAC location. the conversion result is returned in the accumulator, and the conversion cycle executes in approximately 2.5 milliseconds on a 1MHz 8080A.

```
START:  PUSH B          ; SAVE B + C
        LXI B, 8000H    ; CLEAR C
                        ; SET MSB IN B
        MOV A, B        ; AND ACC.
TRY:    ADD C           ; ADD PARTIAL ANSWER
        MOV M, A        ; SEND TO DACPORT
        MVI A, ODH      ; SET UP DELAY FOR
LOOP:   DCR A           ; COMPARATOR TO SETTLE.
        JNZ LOOP        ; 200 MICROSECONDS USED
                        ; HERE
        MOV A, M        ; READ COMPARATOR
                        ; OUTPUT
        ANI 01H         ; MASK ALL BUT LSB
        JZ NEXTRY       ; IF ZERO, GUESS IS TOO
                        ; HIGH
        MOV A, B        ; SO DROP BIT, OTHERWISE,
        ADD C           ; ADD THAT BIT TO OLD
                        ; PARTIAL
        MOV C, A        ; ANSWER AND STORE IN C.
NEXTRY: MOV A, B        ; GET LAST BIT TRIED +
                        ; MOVE RIGHT
        RAR             ; IF IT WAS LSB
        JC DONE         ; THEN EXIT
        MOV B, A        ; IF NOT, GO BACK
        JMP TRY         ; AND TRY IT.
DONE:   MOV A, C        ; WHEN DONE PUT
        POP B           ; ANSWER IN A
        RET             ; RESTORE BC AND EXIT
```

8080-Language successive-approximation subroutine.

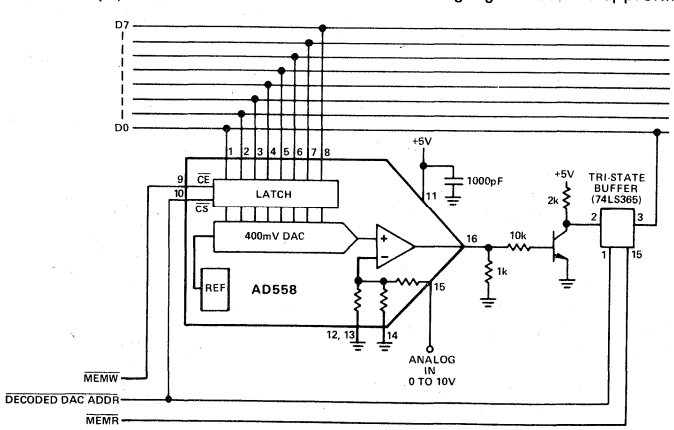


Figure 16. Software-Controlled ADC Using DACPORT Output Amplifier as Comparator

Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs

by Phil Burton

INTRODUCTION

This note is intended to provide an insight into factors which affect the "gain" of CMOS multiplying D/A converters. The emphasis is on developing an understanding of the phenomena involved and in creating rules of thumb and criteria which are easy to apply. The mathematical relationships which are derived are approximate and usually give worst case values which are worse than those that one might reasonably expect to occur. Almost every circuit application has its own unique set of parameters and clearly it is not possible to cover every eventuality. But, hopefully, with the information contained in this note, engineers will be in a position to assess the importance of related parameters for themselves.

GAIN ERROR AND GAIN TEMPERATURE COEFFICIENT

An ideal 12-bit D/A converter has full scale output voltage of

$$\left\{\frac{4095}{4096} \cdot V_{REF}\right\} \text{ Volts}$$

In practice the full-scale output voltage can differ from this and the transfer relationship V_{OUT}/V_{REF}, commonly called *"gain"*, is specified as having a "gain error" of ±x%. This means that the full scale output voltage can deviate by up to ±x% from the ideal output voltage.

Gain is also specified as having a gain temperature coefficient. For most modern CMOS DACs the "gain tempco" is of the order of ±5ppm/°C. This gives the worst case variation in gain of the D/A converter with temperature due to differences of temperature coefficients between the feedback resistor and the R/2R converter. The gain tempco varies with temperature and the specified worst case value usually applies to a 10°C segment of the operating temperature range. For a temperature variation of 100°C (+25°C to +125°C) the average temperature coefficient is generally a good deal less (better than ±3ppm/°C) than the specified worst case value. However, for the sake of simplicity and worst case analysis it is often convenient to assume that the specified worst case temperature coefficient applies over the whole temperature range.

GAIN TRIM CIRCUIT—THEORETICAL CONSIDERATIONS

Imperfection in "gain" is due to inevitable manufacturing tolerances in the process used to fabricate the resistors. The gain (or full scale value) may be restored to the ideal value by using a fixed resistor and a trim resistor as shown in the generalized circuit of Figure 1. Note that it is preferable to use a "select on test" fixed resistor in place of potentiometer R1 where possible—more about this later.

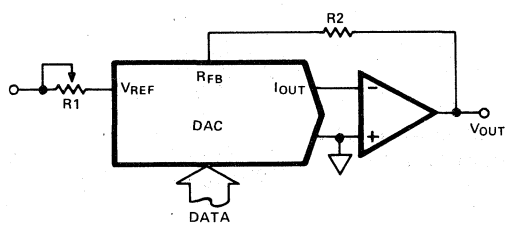


Figure 1. Generalized Gain Trim Arrangement for CMOS Multiplying D/A Converters

The maximum required value of R1 and R2 may be determined by using equations (1) and (2) given below where R_{DAC} is the input resistance of the R-2R ladder (i.e., the input resistance at the reference input of the D/A converter), $R_{DAC\ max}$ is the maximum specified value of R_{DAC} and x is the gain error in %.

$$R_{1\,max} = \frac{2\,|x|\,R_{DAC\,max}}{100} \qquad (1)$$

$$R_{2\,max} = \frac{|x|\,R_{DAC\,max}}{100} = \frac{R_{1\,max}}{2} \qquad (2)$$

The full scale output (or gain) of a D/A converter varies with temperature because of the temperature coefficients of the D/A converter itself and the temperature coefficients of the additional components (R1 and R2 and the op-amp) used to realize the circuit. The temperature coefficients of the R-2R ladder and the feedback resistor are around -300ppm/°C but they are carefully designed to track each other to better than ±5ppm/°C, so that the overall gain temperature coefficient is better than ±5ppm/°C. It may be shown that

the additional temperature coefficients (tempco) introduced into the circuit of Figure 1 by R1 and R2 are approximately given by:-

$$\text{Additional Tempco due to } R_1 = -\frac{R_1}{R_{DAC}}(\gamma_1 - \varsigma) \qquad (3)$$

$$\text{Additional Tempco due to } R_2 = +\frac{R_2}{R_{DAC}}(\gamma_2 - \varsigma) \qquad (4)$$

ς is the temperature coefficient of the D/A converter resistor material, expressed in ppm/°C units.

$\gamma 1$ and $\gamma 2$ are the temperature coefficients of R_1 and R_2 respectively, expressed in ppm/°C units.

From equations (3) and (4) it will be observed that the *additional* temperature coefficients are at a maximum when R_{DAC} is at a minimum, i.e., $R_{DAC\ min}$. By substituting equations (1) and (2) into equations (3) and (4) we obtain equations (5) and (6) which give the worst case (i.e., maximum) additional temperature coefficients due to R1 and R2. Note that these equations are expressed in terms of data which is directly available from the manufacturer's data sheet; in fact, the value -

$$\frac{|x|R_{DAC\ max}}{R_{DAC\ min}}$$

is a simple figure of merit for assessing potential D/A converter temperature coefficients.

$$\text{Worst case additional tempco due to } R_1 = \frac{-2\,|x|R_{DAC\ max}}{100R_{DAC\ min}}(\gamma_1 - \varsigma) \qquad (5)$$

$$\text{Worst case additional tempco due to } R_2 = \frac{+\,|x|R_{DAC\ max}}{100R_{DAC\ min}}(\gamma_2 - \varsigma) \qquad (6)$$

IMPLICATIONS OF COMPONENT TEMPERATURE COEFFICIENTS ON THE DESIGN AND SPECIFICATION OF D/A CONVERTERS

From equations (3) and (4) it can be seen that if R1 and R2 have the same temperature coefficient, then the overall additional (circuit) temperature coefficient is given by

$$\frac{R_2 - R_1}{R_{DAC}} \cdot (\gamma - \varsigma)\,.$$

If the D/A converter has no gain error then R2 = R1 and there is no additional temperature coefficient due to R1 and R2. Clearly then R1 and R2 should preferably be the same type of resistor with the same temperature coefficient. Hence, it is always best to use a "select on test" fixed resistor for R1. The temperature coefficient of potentiometers usually varies with setting, so that it is difficult to match potentiometer temperature coefficients to that of fixed resistors. Figure 2 shows a distribution of gain error for a batch of AD7542 12-bit D/A converters. The average gain error is zero, so that the average temperature coefficient of applications circuits will be zero. This is of little comfort to the worst case applications circuit designer, but a necessary consideration of the IC designer.

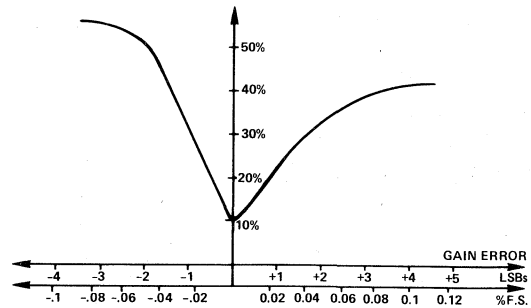


Figure 2. Cumulative Distribution of Gain Error for One Batch of AD7542s (All Grades)

An alternative strategy for the IC manufacturer would be to design and specify the D/A converter so that its gain error is always in one direction (as opposed to plus and minus) and the average gain error is centered some distance from zero. This has the advantage that R2 (or R1 depending on the direction of skew) could be omitted from circuit. However, R1 will always have a finite value and there will always be an additional temperature coefficient due to the gain trim circuit. Since precision resistor temperature coefficients are usually positive and the D/A converter resistor temperature coefficient is negative, the two will add (see equation 5) to give a significant temperature coefficient overall.

A better approach to minimizing additional temperature coefficients due to gain trim components is to improve the figure of merit

$$\frac{|x|R_{DAC\ max}}{R_{DAC\ min}}$$

and, if possible, to improve the temperature coefficient of the resistors used to manufacture the D/A converter. Unfortunately, it is not possible to change ς without changing other critical resistor parameters and the designer is left with the option of reducing the specified gain error spread x and minimizing the spread of R_{DAC} values. Recognizing this requirement, Analog Devices has introduced a "G" selection on gain error (x) for some of its more recent D/A converter products. "G" selected products have a specified gain error at 25°C of not more than plus or minus 1LSB (least significant bit). This represents more than a twelve fold improvement in the figure of merit. For many applications such a tight gain-error specification will be sufficient to eliminate any requirement for gain trimming, but where gain trims are still used, the additional temperature coefficients introduced by the very small values of R1 and R2 required for "G" selected parts will be so small as to be negligible. This is considered in more detail in the next section.

It is also possible to select R_{DAC} to a narrower spread of values, and to improve the figure of merit even more. However, the net improvement in gain temperature coefficient which results from such a selection is difficult to justify on a commerical basis.

PRACTICAL EFFECTS OF COMPONENT TEMPERATURE COEFFICIENTS

Table I shown on next page summarizes the worst case component gain drifts over a 100°C range for the AD7542TD, AD7542GTD, 12-bit D/A converters and the AD7527UD and AD7527GUD 10-bit D/A converters. In drawing up this table it has been assumed that precision wire-wound resisors with a temperature coefficient of +50ppm/°C have been used for R1 and R2. The actual values of R1 and R2 are given in this table. R_{DAC} temperature coefficient has been assumed to be -300ppm/°C.

It will be seen that for the "G" selected parts, the worst case additional temperature coefficient due to R1 and R2 is so small as to be negligible compared with the worst case 5ppm/°C temperature coefficient of gain error for the D/A converter itself.

LEAKAGE CURRENT EFFECTS ON GAIN

This note is primarily intended to cover the effects of external gain trim resistors on overall gain temperature coefficient.

However, it is worth noting that apparent gain shifts with temperature can be caused by op amp offset and bias current drifts, changes in V_{REF} and by D/A converter leakage currents at the I_{OUT} terminal of Figure 1.

The I_{OUT} leakage current effect on gain is negligible at 25°C, but at higher temperatures it can have some effect. Leakage current has two components:-

1. Leakage from the V_{DD} supply to the I_{OUT} terminal. This is more or less independent of input code.
2. Leakage from the R-2R ladder through off-switches. This leakage is a maximum for all zeros at the input because all switches are off, and is a minimum with all ones at the input, i.e., all switches on.

Usually the two components of leakage current are roughly equal, but this depends a great deal upon circuit design and layout, fabrication process, and temperature. Leakage from the V_{DD} supply produces a constant shift on the D/A converter transfer function as depicted in Figure 3—the magnitude of the shift is exaggerated in the diagram to make it clearer. Leakage from the R-2R ladder produces a rotation

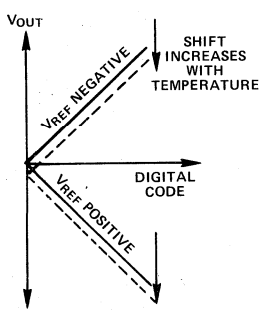


Figure 3. Graph Showing Shift of DAC Transfer Function Due to Leakage From V_{DD}

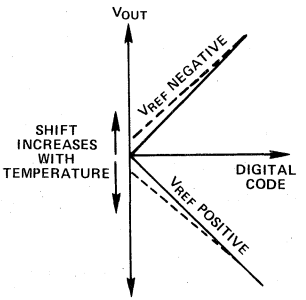


Figure 4. Graph Showing Effect of Off-Switch Leakage on DAC Transfer Function

of the D/A transfer function as shown in Figure 4. The magnitude and direction of rotation due to leakage across "Off Switches" is determined by V_{REF} as shown.

Leakage current effects on gain error are usually only of significance at operating temperatures above 100°C where the worst case error voltages due to leakage current begins to become comparable to 1LSB worth of current. The user should be aware of leakage current effects because they have often in the past, been erroneously interpreted as being due to gain trim components.

Some electrical cleaning solvents, used to wash printed circuit boards after soldering, leave a slightly conductive film on the components after drying. These films introduce leakage paths from V_{DD}, V_{REF} and other pins to I_{OUT} of the D/A converter and the effect can be similar to that due to leakage effects in the converter chip itself. The user should ensure that such films do not occur during the manufacturing processes for any precision analog circuits.

SPECIAL CASES OF LEAKAGE CURRENT EFFECTS

(a) V_{REF} = -10V

With a negative reference voltage the two leakage effects shown in Figures 3 and 4 tend to cancel each other at zero output, and give a net decrease in gain at full scale. The gain trim resistors R1 and R2, on the other hand, introduce a positive temperature coefficient of gain (i.e., increase in gain) so that the combined result of all these effects is to reduce the gain variation with temperature.

(b) V_{REF} = +10V

For a positive reference voltage the two leakage effects add to each other and add to any pcsitive gain temperature coefficient due to R1 and R2. The combined result is a positive increase in the gain temperatue coefficient due to all three effects. Positive reference applications, therefore, suffer more gain variation with temperature than negative reference applications.

SUMMARY

This text has been concerned with factors which cause the gain of CMOS multiplying D/A converters to vary with temperature.

The primary factors are:-

1. Gain temperature coefficient of the D/A converter itself.
2. Gain temperature coefficient due to the gain trim resistors R1 and R2.
3. Gain shift due to leakage from V_{DD}.
4. Offset shift due to leakage across off switches.

The additional gain temperature coefficient due to R1 and R2 is minimized by using the same type of resistor for R1 and R2 and by minimizing the specified maximum gain error of the D/A converter.

Leakage currents can produce gain errors. Applications using negative reference voltages are less sensitive to temperature variations than positive reference applications.

	Specified Values				Trim Values		Worst Case Additional Gain Tempco Due to R_1 & R_2 ppm/°C	Worst Case Full Scale Gain Shift Over 100°C Due to R_1 and R_2	
Part Number	$R_{DAC\ max}$ kΩ	$R_{DAC\ min}$ kΩ	Worst Case Gain Tempco (ppm/°C)	Worst Case Untrimmed Gain Error at +25°C	R1 Ω	R2 Ω		LSBs	%
AD7542TD	25	8	5	±0.3% (±12LSB)	150	75	3.28	1.34	0.033
AD7542GTD	25	8	5	±0.0244% (±1LSB)	12.4	6.2	0.27	0.11	0.0027
AD7527UD	20	7	5	±0.49% (±5LSB)	196	98	4.9	0.5	0.049
AD7527GUD	20	7	5	±0.098% (±1LSB)	40	20	1.0	0.1	0.01

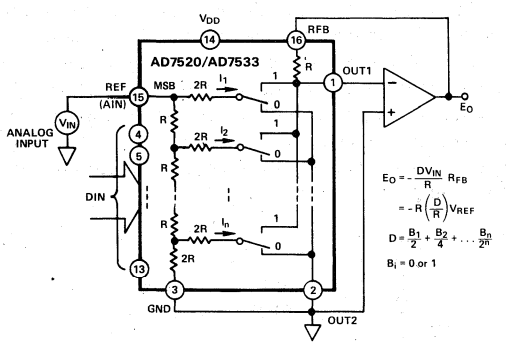
Note: AD7542 is a 12-bit D/A converter.
AD7527 is a 10-bit D/A converter.

Table I. Worst Case Full Scale Gain Error Due to Gain Trim Components R1 and R2 for a Selection of D/A Converters

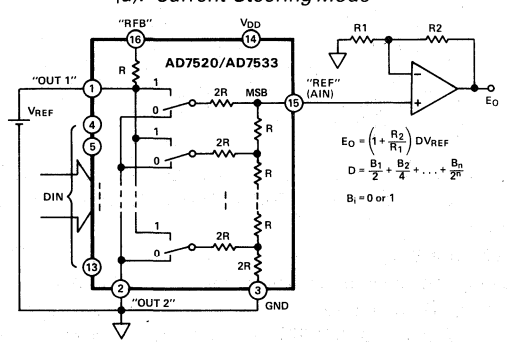
CMOS DACs in the Voltage-Switching Mode Can Work from a Single Supply, Including Output Op Amp, For Fast Response, No Offset-Induced Nonlinearity

by Steve Stephenson

The versatile R-2R ladder attenuator can be used as either a voltage or a current source, and it may be used in either a current-steering or a voltage-switching mode.[1] Figure 1a shows the familiar connection of a CMOS d/a converter, such as the 10-bit AD7520, in the current-steering mode; Figure 1b shows how the DAC can be connected for voltage switching by reversing the roles of the MSB node (REF/AIN) and the active switch bus (OUT1).



(a). Current-Steering Mode



(b). Voltage-Switching Mode

Figure 1. CMOS DAC Connected for Different Operating Modes

[1]Examples of current steering and voltage switching may be seen in the *Analog-Digital Conversion Notes* (Analog Devices, 1977, ed by D. Sheingold, available at $5.95 postpaid), pages 116–117 and pp. 133–138.

Reprinted from Analog Dialogue 14-1, 1980.

CURRENT STEERING

In the current-steering mode, since the OUT2 terminal is at ground potential, the operational amplifier maintains OUT1 at the same voltage (virtual ground), and the binary-weighted currents through the 2R switch legs are independent of switch position. As commented upon in an earlier article,[2] the output capacitance and resistance (as seen by the amplifier's input) vary as functions of the input digital code. This makes the feedback-circuit's *noise gain* dependent on the code. The variation of resistance can cause the linearity to be affected if the amplifier has sufficient offset voltage. The variation of the output time-constant means that feedback compensation can, at best, only be a compromise. To ensure circuit stability for all codes, overcompensation (and consequent reduced bandwidth and increased settling time) is required.

There is also some charge injection from the gate of the switch, via the inherent capacitance between the gate and channel of the FET switch. This charge must take the lowest-impedance path to ground, in this case through the virtual ground of the amplifier. At major code-changes, output glitches may be significant.

VOLTAGE SWITCHING

In the voltage-switching mode, the constant resistance at the amplifier input eliminates the problems caused by modulation of the amplifier's offset voltage. In addition, the switch capacitance is remote from the amplifier, and the charge is shunted to the input source or to ground. Furthermore, the output capacitance of the network is considerably lower. All of this results in cleaner and faster response of the circuit to code changes.

As an additional important feature, the system's output voltage is of the same polarity as the reference voltage; as will be seen, this makes it possible to *operate the DAC and its amplifier from a single-polarity supply*. Finally, only a single amplifier is required for bipolar digital operation, using offset binary or (with the MSB complemented) 2's complement coding.

[2]"Analog Signal-Handling for High Speed and Accuracy," by A. Paul Brokaw, *Analog Dialogue* 11-2 (1977), pages 10–16.

The configuration has a few minor disadvantages. Since the ON resistance of the FET switch increases the applied drain-source voltage approaches the value of the gate-drive voltage, and significant values of R_{ON} cause the division of voltage to depart from the ideal, large values of reference voltage will produce nonlinear performance.[3] However, for values of reference voltage less than +3.5V and V_{DD} = +15V, the 10-bit DACs in the AD7500 series will retain their linearity. The 12-bit DACs will maintain 11-bit accuracy over temperature when employing a +2.5V reference (eg., the AD580).

While the current-steering mode permits input voltages of either polarity and allows the circuit to function as a digitally controlled potentiometer (and as a four-quadrant multiplier), the voltage-switching mode permits only a single polarity of input (positive with respect to common).

CIRCUIT POSSIBILITIES

Single Supply, Unbuffered. In Figure 2, the circuit of Figure 1b, without a buffer, is implemented with an AD584 as an adjustable reference. Settling time of better than 1μs was observed, with overall conversion linearity to 10 bits, using a 3.5V (max) reference voltage. Although the network can be loaded resistively, buffering is preferred, since the different temperature sensitivities of an external load resistance and the ladder resistance will result in a temperature-sensitive scale factor.

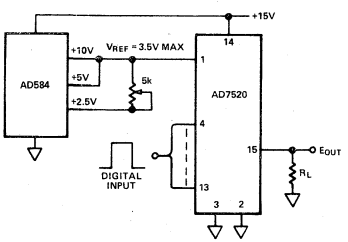


Figure 2. Single-Supply DAC with AD584 Reference, Unbuffered Output

Single Supply, Buffered. In Figure 3, the DAC and the CMOS op amp are both powered from a single + 15V supply. With this circuit, 10-bit linearity and good gain-temperature coefficient (since there are no external resistors sharing current with the ladder) were achieved over ambient temperatures up to 125°C. With a single-supply operational amplifier, offset is difficult to remove completely; therefore, some offset may have to be tolerated, usually amounting to less than one-half LSB at 3.5V reference. The observed settling time under these conditions, governed by the amplifier's performance, was found to be better than 2μs to one-half LSB.

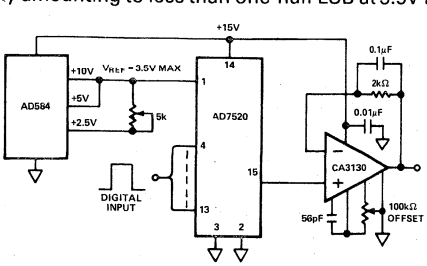


Figure 3. Single-Supply DAC, Buffered Output

[3] *Application Guide to CMOS Multiplying D/A Converters,* Analog Devices, 1978.

Shorter Voltage-Settling Times. Figure 4 shows a circuit in which the voltage-switched mode is employed to obtain a *current* output, by connection of the ladder output directly to the summing point of the output amplifer. This connection provides the *fastest response* (settling time of the order of 900ns was observed): however, the gain tempco is poor, because the external feedback resistance cannot be expected to track the network's resistance variation with temperature.

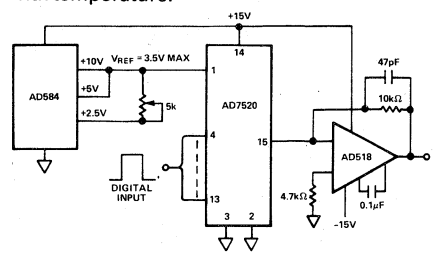
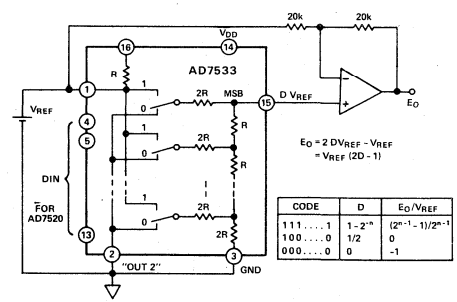


Figure 4. Increased Speed DAC

Simplified Bipolar Operation. Figure 5 shows how the voltage switched mode simplifies the conversion of bipolar digital signals.[4] The output voltage from the ladder is applied at the amplifier's positive input, as in Figure 1b; the reference is connected to the inverting input via a resistance equal to the feedback resistance. Thus, the output of the ladder has a gain of 2, and the reference has a gain of −1; as the equation and the table show, this provides conventional offset-binary response, but *with a single amplifier*, instead of the two called for in the current-steering mode.



CODE	D	EO/VREF
111....1	1 - 2^-n	(2^n-1 - 1)/2^n-1
100....0	1/2	0
000....0	0	-1

Figure 5. Connection for Bipolar Operation. If V_{REF} is Provided by the 2.5V AD580, Nominal Output Swing is ±2.5V

SUMMARY

Using the techniques described here, Analog Devices CMOS d/a converters in the series AD7520, AD7521, AD7522, AD7523, AD7524, AD7530, AD7531 and AD7533 may all be made to operate in the voltage-switching mode with their published specified linearity. System benefits include the possibility of single-supply operation, increased speed, freedom from offset-voltage modulation, and more-economical digital bipolar operation.

[4] "An Unusual Circuit Configuration Improves CMOS-MDAC Performance," by N. Sevastopoulos *et al EDN* Magazine, March 5, 1979, pp. 77–82.

Methods For Generating Complex Waveforms and Vectors Using Multiplying D/A Converters

by Phil Burton

Complex analog waveforms are used in a variety of equipment. They can define a process temperature profile, be used to generate high resolution graphics either on a CRT or X–Y plotter, or form the basis of a speech synthesizer. There are as many solutions to the problem of waveform generation as there are applications. This note describes some common methods for generating complex waveforms using CMOS multiplying D/A converters. The applications bias, is towards graphics displays because most engineers will understand the applications but designers of other equipment will immediately recognize the relevance of the various techniques to their own particular problem. The treatment is mostly in block diagram form with the emphasis on a systems approach rather than detailed circuit design. The implications of the various methods of interfacing D/A converters to computer systems are also covered with regard to the hardware and software requirements of the system.

STAIRCASE WAVEFORM SYNTHESIS

Figure 1 shows a simplified waveform generator consisting of a DAC driven from a ROM look-up table, and a counter which provides sequential addresses for the ROM. The frequency of the generated waveform is determined by the clock rate of the counter and the number of memory words used to define the waveform.

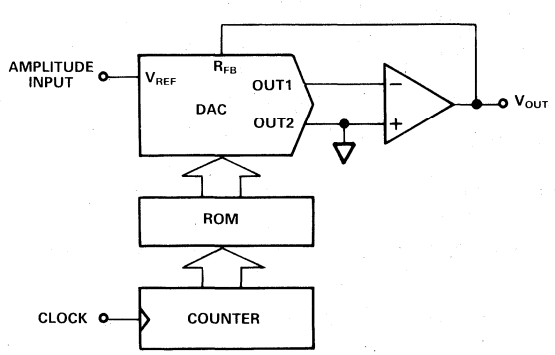


Figure 1. Simple ROM Waveform Generator

If the waveform is symmetric as in a sinusoid, then the size of the ROM can be reduced by only coding one quadrant and using digital arithmetic on the output and input of the ROM to generate the words for the other three quadrants.

When a ROM contains the values of sin θ for $0<\theta<90$ then the values for the other three quadrants can be computed as follows:

For $90<\theta<180°$ $\sin\theta = \sin(180-\theta)$
For $180<\theta<270°$ $\sin\theta = \sin(\theta-180)$
For $270<\theta<360°$ $\sin\theta = \sin(360-\theta)$

Suppose θ is represented by a 10-bit binary number to cover the range 0 to 360°, then the two most significant digits of θ will determine the quadrant of operation. Furthermore the most significant digit will determine the sign of sin θ and the second most significant digit will determine whether the remainder of the number is to be used as it stands, or substracted from the binary equivalent of 180°. Note that 180° in our chosen 10-bit notation is 10,0000,0000 and 2's complement subtraction is achieved by complementing the number and adding 1. Complementation can be achieved by exclusive–OR gates. Figure 2 shows in block diagram form a high resolution sine-wave synthesizer using a one quadrant look-up table.

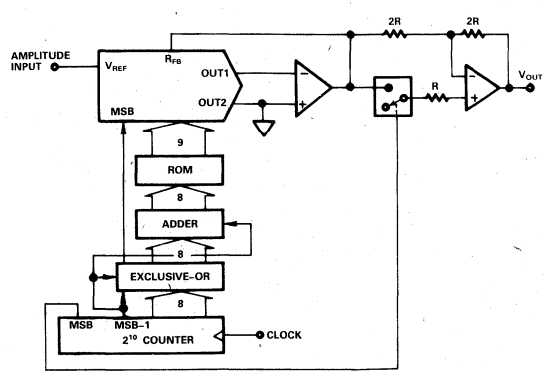


Figure 2. Block Diagram of Sinusoid Generator

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The 10-bit D/A converter is operated with sign plus magnitude coding, the most significant bit of the 10-bit word being fed to the sign switch. The second MSB of the 10-bit word, representing θ, determines whether the remaining bits are complemented or not using the exclusive OR gates, and it also provides the +1 required for 2's complemented subtraction. The eight-bit word from the adder is fed to the ROM look-up table which provides the appropriate digital word to the D/A converter.

If the addresses to the ROM are generated by a counter, the adder and exclusive OR circuits can be dispensed with by using a counter which alternately counts up to 1111,1111 and then counts down to 0000,0000. An additional flip-flop is required to generate the sign. This method is described on page 27 of "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices.

Sinusoid generators such as the one described above have been used in radar displays (A Scopes) and Synchro to Digital Converters. In both of these applications the ease with which the reference voltage V_{REF} can be varied, to change the magnitude of sinθ is a distinct advantage. This results directly from the multiplying properties of CMOS multiplying D/A converters. Some of the disadvantages of the approach described above are the relatively low frequencies that can be generated with any precision, and the presence of quantisizing noise due to the output being defined in discrete steps. Also, the D/A converter has a relatively long settling time (2μs approximately), so that the output waveform contains glitches at every change of digital input.

BASIC INTERPOLATION METHOD FOR WAVEFORM GENERATION

If the staircase method of waveform generation was used to draw a sawtooth on a X–Y plotter then the drawn waveform would have a staircase appearance due to the discrete output steps available from the D/A converter. Clearly such an appearance is not desirable and consequently analog graphic output systems have adopted an interpolative method of generating waveforms. Not only does this method give a cleaner looking waveform, but it also allows a much higher frequency of operation, and reduces to a minimum the number of digital words necessary to define a waveform.

An interpolative method uses two D/A converters to generate a waveform–one to define the starting point and another to define the finishing point. A straight line is drawn between the start and finish. Figure 3 shows a sinusoid drawn by an interpolative waveform generator, and the associated waveforms for the circuit of Figure 4.

Figure 4 shows a simple interpolation scheme such as might be used to drive one axis of an X–Y plotter or a CRT graphics display. The digital inputs to DAC P define the starting point and DAC Q inputs define the finishing point of the straight line to be drawn. The reference input to DAC P consists of a positive going ramp which goes from $-V_{MAX}$ to O in time T. The reference to DAC Q is an equal but opposite ramp which goes from O to $-V_{MAX}$ during

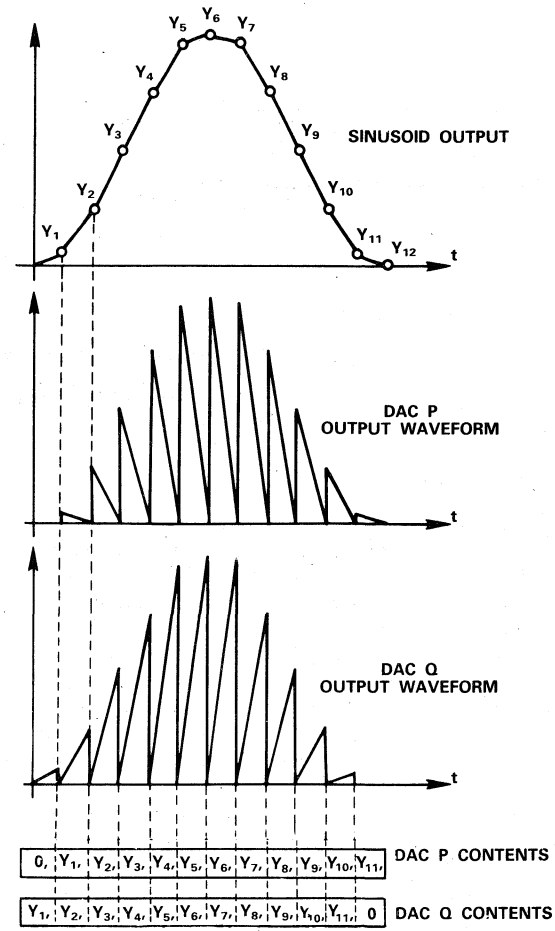


Figure 3. Synthesis of Sinusoid Using Circuit of Figure 4

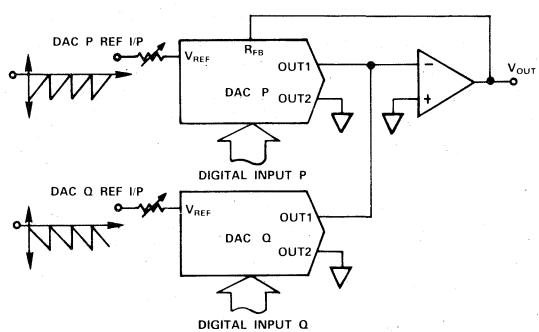


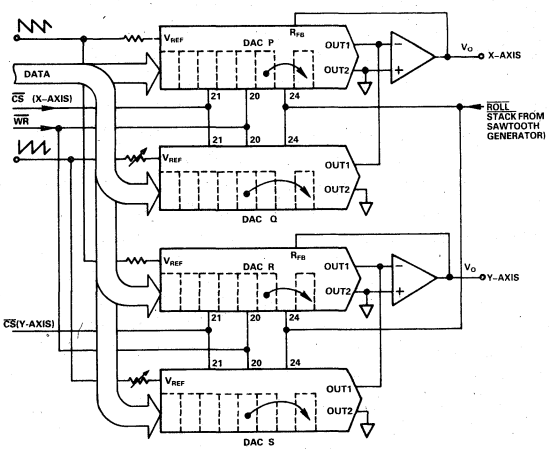
Figure 4. Elementary Interpolation Method

the same period T. The sum of the outputs of DAC P and DAC Q is given by:

$$V_{OUT} = N_p (V_{MAX} - V_{\frac{MAX}{T}}t) + N_q (V_{\frac{MAX}{T}}t)$$

$$= N_p V_{MAX} + (N_q - N_p) V_{\frac{MAX}{T}}t$$

which is a straight line between the two points defined by the binary number N_p in DAC P and the number N_q in DAC Q. For the next line to be drawn P is loaded with Q's value and Q is loaded with the new finishing point and the process is repeated. In drawing a number of points DAC P and DAC Q receive exactly the same binary input words except the DAC Q inputs are always one word in front of DAC P inputs. This suggests a FIFO (first-in, first-out) structure with DAC P being fed from the output end of the FIFO, and DAC Q being fed with the "next to the end" word of the FIFO. The FIFO has the additional advantage that a number of data points can be loaded into the FIFO by the main processor at one burst, and then the points can be clocked out of the FIFO at a rate determined by the repetition frequency of the reference sawtooth waveforms. This leads to very efficient software and minimizes the time the processor is tied up in I/O operations. Figure 5 shows a simplified graphic display system using the method described above. The main portion of the system is based on four AD7544s which are 12-bit D/A converters with integral 6-word FIFO registers. Each x coordinate is loaded by the computer to both x-axis DACs simultaneously, similarly for the y-axis DACs. This reduces the data transfer operation to one x and one y value per coordinate. DAC's Q and S are loaded from the next to the end word of the FIFO and DAC's P and R are loaded from the end word of the FIFO—this is shown in Figure 5 by the curved arrows. The DAC Register of the AD7544 can be loaded from either the top or next to top word of the FIFO. At the point when the data feeding the DACs is changed, the D/A outputs will exhibit some glitches, due to the settling time of the DAC and op amps, slew rate of the sawtooth, digital feedthrough, etc. During this update period, the CRT display should be blanked off. In electromechanical displays the transients are usually absorbed by the mechanical inertia of the system.



All D/A converters are AD7544.

The following pin connections have been omitted from all DACs in the above drawing to preserve clarity:

Pin 19	$\overline{\text{RESET}}$	Normally connected to the system reset.
Pin 22	SFUL	Stack Full – indicates stack full to processor.
Pin 23	SAMT	Stack Almost Empty – used to interrupt the processor to load another burst of data to the FIFOs.
Pin 25	$\overline{\text{RLEN}}$	Roll Enable – strapped low.
Pin 26	LDAC	Load DAC – strapped high. This makes the DAC register transparent.
Pin 27	W1/$\overline{\text{W2}}$	Selects top or next or top word of stack. DAC's P&R have this pin strapped high, DAC's Q&S have it strapped low.

Figure 5. Simplified Graphic Display System

IMPROVED INTERPOLATION METHOD FOR WAVEFORM GENERATION

In the scheme of section "Basic Interpolation Method for Waveform Generation", converter P always holds the starting value of the vector and converter Q the finishing value. Unwanted transients occur each time the digital values to the D/A converters are updated. These transients can be overcome by continuously alternating the roles of converters P and Q. In Figure 3 note that each digital value is first subjected to a positive going ramp in DAC Q and then subjected to a negative going ramp in DAC P. Instead of feeding each digital word to DAC Q and then one sawtooth later to DAC P, each word can be input to a single DAC and a triangle wave is now applied to the reference of the DAC. Figure 6 shows a circuit to achieve this together with the two reference waveforms for converters P and Q and the successive data words applied to P and Q. *Note in particular that the data words applied to the D/A converters are updated when the D/A reference input is zero.* This avoids most of the slew rate and settling time problems of the circuit of Figure 4, although there will still be a small glitch at the output of the D/A converter due to digital feedthrough. When using AD7544s, the effective memory capacity at the FIFO is doubled because there is no duplication of memory contents.

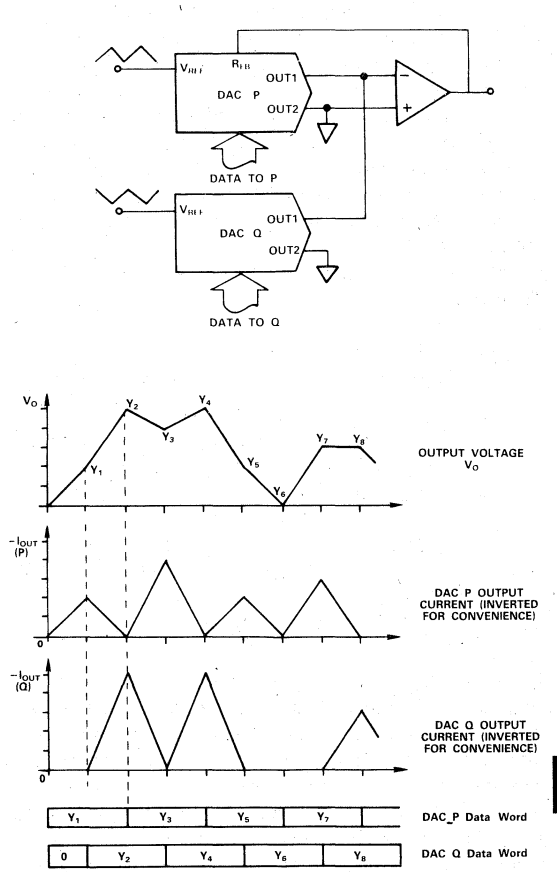


Figure 6. Improved Interpolation Method and Waveform

This improved method is particularly suitable for continuous waveform generation because there are no significant transients (or blanking periods) in the signal.

TRIANGLE AND SAWTOOTH WAVEFORM GENERATION

The triangle and sawtooth reference waveforms required for the circuits of sections "Basic Interpolation Method for Waveform Generation" and "Improved Interpolation Method for Waveform Generation" can, in some applications, be fixed frequency waveforms. However, in graphic display systems, this would allocate exactly the same time for each drawn vector. A short vector would take just as long a time to draw as a long vector, with the result that a CRT display would exhibit uneven brightness and an X–Y plotter would have to be restricted to drawing each vector at the time taken to traverse a full axis. Clearly a better solution for vectors drawn on a CRT would be to scale the waveform ramp rate in accordance with the length of the vector to be drawn. A long vector would be drawn using a slow ramp and a short one by a much faster ramp. For electromechanical X–Y plotters, the ramp rate would be determined by whichever axis has the greatest distance to travel. Figure 7 shows a simple circuit for generating programmable sawtooth waveforms suitable for the interpolation method described in section "Basic Interpolation Method for Waveform Generation". The circuit consists of a resetable integrator (A1), the ramp rate of which is determined by a D/A converter. A comparator determines when the ramp has reached its maximum value, and the output of the comparator is used to reset the integrator and to trigger a one-shot for blanking the screen during the reset period of the sawtooth and the settling time of the D/A converter. The output of the comparator is also used to clock the FIFOs associated with each D/A converter, so as to load the next vector coordinates to the DACs. Amplifier A2 provides the inverse sawtooth waveform which drives the reference input of DAC Q in Figure 4.

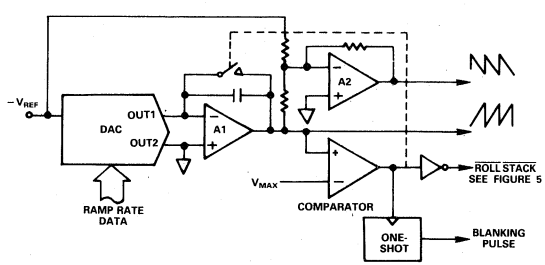


Figure 7. Simplified Sawtooth Generator

Figure 8 shows a programmable triangle waveform generator, which uses two D/A converters, one to determine the upward ramp and another to determine the downward ramp. The integrator A1 has two input resistors and switch S1 switches between the two D/A converters to provide the up and down ramps. The digital inputs to the D/A converters are changed during the half cycle when the converter output is not being used to drive the integrator. This allows the D/A converters adequate time to settle before its output is switched to the integrator.

Switch S1 is a two pole, N-Channel changeover switch such as normally used for the switches in a CMOS D/A converter. This type of switch ensures that the two D/A converter outputs see a constant load impedance, thereby preventing load induced glitches; it also provides a fast changeover for the integrator inputs. The switches can be formed from CD4016s or alternatively an AD7201 can be used which incorporates 5 changeover switches with resistors in one package. Amplifier A2 provides the inverse triangle waveform. Comparators A3 and A4 are used to detect the peak and the trough of the triangle waveform, and to generate the clock signals for the FIFOs feeding the D/A converters.

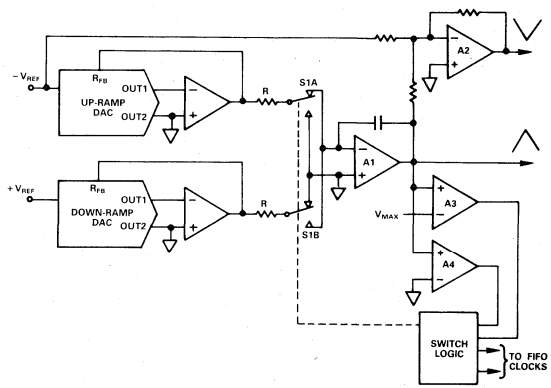


Figure 8. Programmable Triangle Waveform Generator

A COMPLETE GRAPHICS GENERATOR

Figure 9 shows a complete simplified schematic of a graphics vector generator using triangle waveforms (i.e., the scheme of section "Triangle and Sawtooth Waveform Generation"). All the D/A converters are AD7544's. DAC 1 is the odd-coordinate x-axis DAC and DAC 3 is the odd-coordinate y-axis DAC. Together DAC 1 and DAC 3 define the points $(x_1,y_1)(x_3,y_3)$ etc.; DAC 2 and DAC 4 are the x and y even-coordinate DACs respectively. DAC 5 defines the upward ramp of the triangle, from the integrator and DAC 6 defines the downward ramp. The 6-word on-chip FIFOs of the AD7544 enable 12 full vectors to be stored by the system.

The vector generator is entirely self-clocking and its effective "clock rate" is determined by the ramp-rates of the triangle wave generator (i.e., by the length of the vectors to be drawn). In operation the vector coordinates are loaded to the DAC's FIFOs by a burst of data words from the system's computer and the graphics generator clocks the data through the FIFOs to the DACs under its own control. When only one word of data remains in a FIFO, the AD7544 generates an "almost empty" signal which is used to interrupt the main processor and initiate the transfer of another block of data coordinates to the graphics circuit.

An undrawn line (i.e., beam blanked) is encoded as a full-scale value to the inputs of DAC 5 or DAC 6. Comparators

A5 and A6 detect a full-scale output and their outputs are used to provide the blanking pulse to the display. In CRT graphics an undrawn line will always be generated at maximum velocity, thus the blanking encoding information scheme is consistent with practice. The circuit is designed so that drawn lines are always drawn with a ramp rate much lower than defined by the full scale output of the DAC.

For electromechanical plotters the situtation is not quite so simple and the problem of undrawn lines has to be solved either by a separate FIFO to store pen lift signals, or by encoding an undrawn line as an ordinary line which is followed by a line of zero length drawn at maximum velocity. Comparators A5 and A6 and DAC 5 and DAC 6 give not only the ramp rate for the line to be plotted, but also the rate for the next line to be plotted (once the DAC has settled). If a comparator detects that the *next* line is to be plotted at maximum rate (a speed which is never used for a genuine drawn line), then the output of the comparator can be used to supply pen-lift signal for the current line. Once this undrawn line has been completed, the next line, which has the maximum ramp rate information in its DAC will simply cause the pen to remain in the same position–hence an undrawn line from one point to another could be created. This pen lift scheme is not shown in Figure 9, but it is a relatively simple matter to modify Figure 9 as discussed above.

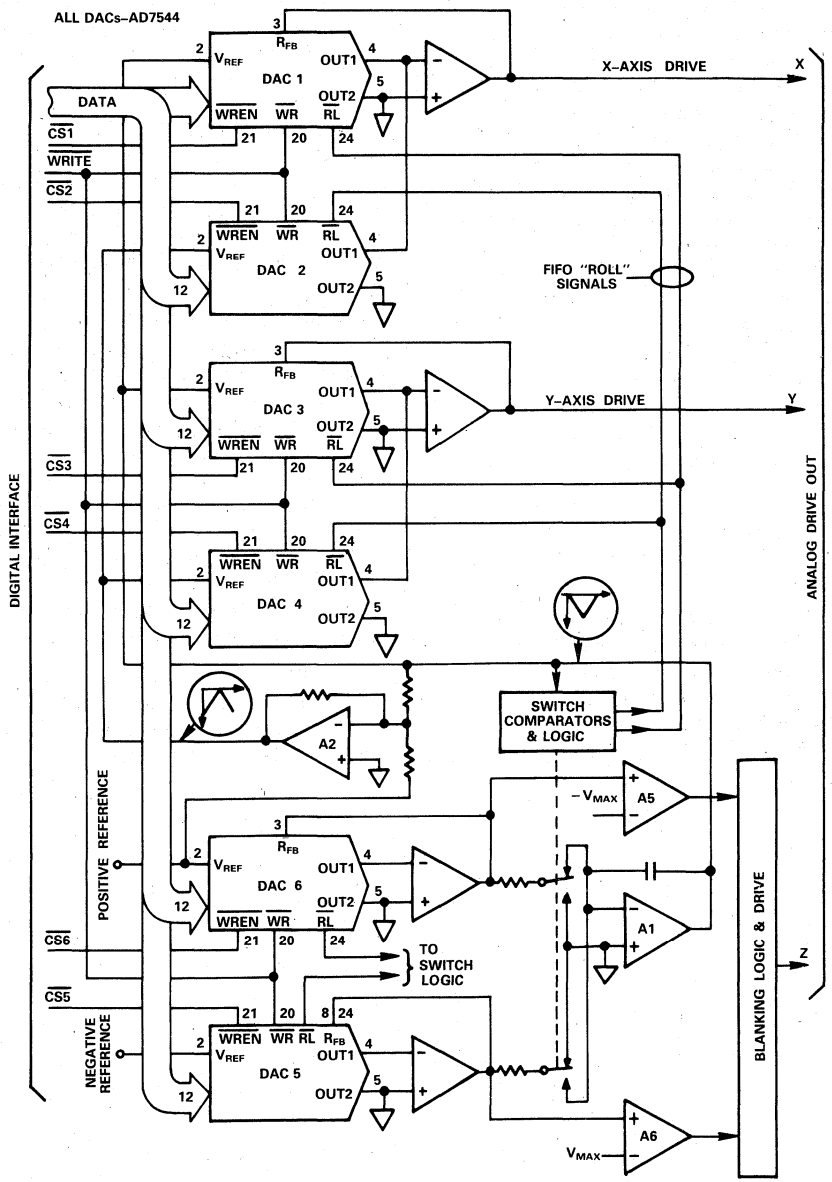


Figure 9. Simplified Graphics Generator Using Triangle Waves

THE PROCESSOR INTERFACE

As mentioned in the section "Triangle and Sawtooth Waveform Generation", the graphics system of Figure 8 is an asynchronous, self-clocking scheme. The on-chip FIFOs of the AD7544 provide a perfect interface between the high speed synchronous processor and the asynchronous graphics circuit. The FIFOs are self-clocking and generate "almost empty" and "full" signals so that the processor can be interrupted when more coordinates are required, and can signal when a full set of coordinates have been received. The design of the full digital interface between processor and graphics circuit is beyond the scope of this article. It is no simple matter to connect six 12-bit D/A converters to a high-speed microprocessor bus without incurring unwanted digital cross talk. It is preferable that the 12-bit bus feeding the graphics circuit should have its own set of data bus buffers which are only enabled when data is being transferred to the FIFOs. At all other times the bus to the converters should be tied to a logic high or a logic low. If the graphics circuit is being fed from an 8-bit data bus, the 8-bit data latch necessary to reassemble the 12-bit word for the FIFOs can also be used as part of the computer data bus to graphics data bus buffer suggested above. Very careful ground management should be used, with the graphics circuit having its own digital and analog grounds tied back to the "quiet point".

COMPUTING THE TRIANGLE RAMP DATA

The ramp rate of the triangle (or sawtooth) waveform is variously related to the distance between the two points to be drawn. For electromechanical plotters it is only necessary to ascertain which axis has to move the furthest and then scale the distance moved according to the equation.

$$\text{Ramp DAC data} = \text{Constant} \times \frac{1}{\text{Distance Moved}}$$

Calculating reciprocal of the distance moved is usually done in the microcomputer since electromechanical plotters are relatively slow and there is adequate time to make the calculation. Note, however, that if a DAC is connected as the feedback resistor of an inverting amplifier, the amplifier output voltage is proportional to the reciprocal of the digital code at the DAC inputs (see page 26 of "CMOS D/A Converter Application Guide"). This could be used as an analog "reciprocal taker" and scaler to ease the software burden on the microcomputer.

In CRT displays the ramp data is directly proportional to the distance along the vector, i.e., $\sqrt{(\Delta x)^2 + (\Delta y)^2}$ and it is difficult to solve such an equation at high speed. Fortunately it is not necessary to encode the CRT intensity information to a high degree of resolution and a lookup table method can be used. Addresses for the lookup table are generated by combining say the top 4-bits of Δx with the top 4-bits of Δy to create an 8-bit address for the intensity lookup table.

An alternative high speed method for evaluating either $1/x$ or $\sqrt{x^2 + y^2}$ is to use a logarithmic number scheme such as the FOCUS number scheme in reference 1. The FOCUS scheme makes it possible to do multiplication, division, addition and subtraction by the use of only addition and subtraction and lookup tables. A D/A converter (AD7118) is now available which accepts numbers encoded according to the FOCUS scheme and delivers a proportional linear output current. Such a converter could be used for DAC 5 and DAC 6 in Figure 8, although the AD7118 does not have an integral FIFO.

SUMMARY

This paper have been deliberately brief. It is intended to stimulate ideas rather than give definitive circuit designs. As mentioned in the introduction, the treatment has centered on the design of graphics displays. This was done because a graphics display is something with which most engineers are familiar. However, graphics has the added complication that two channels of waveforms (x and y) are required whereas many applications, e.g., speech synthesis, only requires one channel. Fortunately most designers are experts at simplifying circuits. Graphic output from computers is becoming increasingly important; it is hoped that this article stimulates more engineers to design their own circuits.

REFERENCE

A. D. Edgar and S. C. Lee, "FOCUS" Microcomputer Number System, ":Commun. Ass. Comput. Mach. Vol 22, No. 3 p.p. 166–177. March 1979.

Behind the Switch Symbol: Use CMOS Analog Switches More Effectively When You Consider Them as Circuits

by Jerry Whitmore

CMOS analog switches are widely used to make or break circuits in such applications as multiplexing and function switching. Ideally, they have zero resistance when closed, infinite resistance when open, no leakage, instantaneous glitch-free response, and no parasitic capacitance. While these assumptions are reasonably valid for low-frequency applications at moderate impedance levels, the good designer will always challenge them, to establish what errors may be introduced and even to determine whether the circuit configuration is viable.

SWITCH CIRCUITS

Figure 1 is a reasonable approximation of the circuitry in a single-pole dielectrically isolated CMOS switch (e.g., AD7510DI or AD7590DI series).The dielectric isolation makes possible protection against latchup and overvoltage to ±25V beyond the supplies. Note that, for one polarity, conduction is via an N-channel FET; for the other polarity, it is via a P-channel FET. The two types are not perfectly symmetrical.

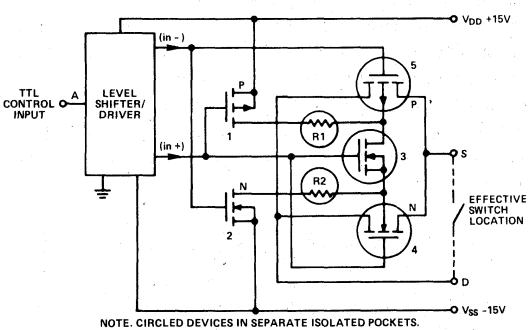


Figure 1. Typical Output Switch Circuitry of the AD7590DI Series

Figure 2 is an equivalent circuit of a pair of adjacent switches. The parameters are defined in Table I. There are three principal categories of error one should be concerned about: low-frequency errors due to resistances and current leakage (switch open or closed), high-frequency and signal-transient errors due to stray capacitances (switch open or closed) and dynamic errors due to switching transients while the state of the switch is changing. Because of the present limitations of space, we shall for now consider just the first category, since it answers the most urgent question, "How well does the switch actually work for low-frequency signals?"

C_{DS}	Open-switch capacitance
C_S,C_D	Source, drain capacitance
R_{ON}	Series on resistance
S,D	Source, drain; electrically interchangeable
C_{SS},C_{DD}	Capacitance between any two corresponding switch terminals
I_{LKG}	Leakage current of back-gate diode

Table I. Nomenclature

Although the leakage currents of the P- and N-channel transistors (devices 4 and 5 in Figure 1) might appear to tend to cancel, they don't, since the P channel is three times larger than the N channel. Because of the size mismatch of the reverse-biased source-or-drain-to-back-gate diodes, plus the differing lot-to-lot variations in breakdown voltage of the diodes, it is difficult to predict leakage or its tempco. However, maximum values at 25°C and over temperature are specified and 100% tested.

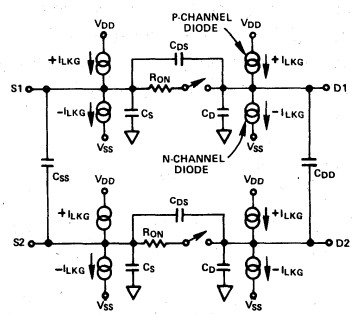


Figure 2. Equivalent Circuit of a Pair of Adjacent Switches

Figure 3 shows the factors affecting dc performance for the *on* switch condition and how the various parameters affect the output voltage. Figure 4 shows typical curves of R_{ON}, as they appear on the product data sheet. They indi-

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cate how R_{ON}, is affected, as a function of input voltage, by supply voltages and by temperature. R_{ON} is lower and less signal-dependent at the higher supply voltages and lower temperatures.

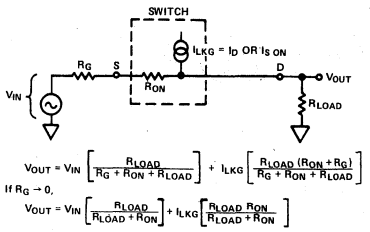
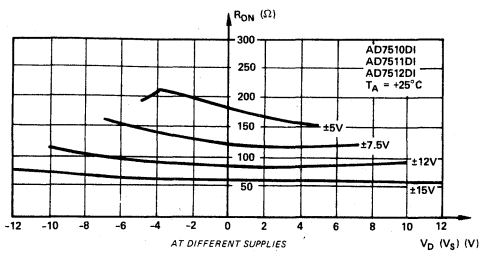
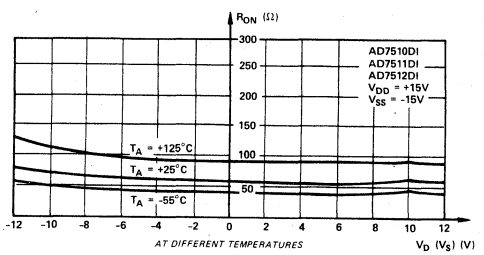


Figure 3. Effective Circuit of Switch in the ON Condition



a. R_{ON} vs. V_D (V_S), as a Function of $+V_{DD}$, ($-V_{SS}$)



b. R_{ON} vs. V_D (V_S), as a Function of Temperature

Figure 4. R_{ON} vs. Input Voltage as a Function of Supply Voltage and Temperature

How to minimize the influence of variable R_{ON} on circuit accuracy: Figure 5 shows a problem circuit–an inverting amplifier with four switched inputs. R_{ON}, in series with the 10-kilohm input resistor, affects the circuit gain. Even if it is compensated for at one level of supply voltage and analog input voltage, the input's variations will cause the gain to change and degrade the gain accuracy.

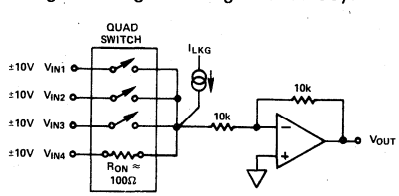


Figure 5. Unity-Gain Inverter with Switched Input

The most obvious solution–if the amplifier doesn't have to invert or act as a precision attenuator–is to use the amplifier in a noninverting mode, as shown in Figure 6. Since there are no resistors in series, there is no effect on gain.

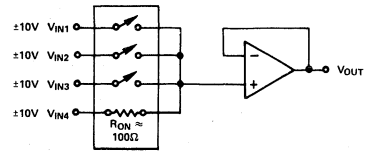


Figure 6. Noninverting Solution

Another solution (Figure 7) is to connect the quad switch at the amplifier's summing point. Then the switch sees only millivolts–rather than volts–of signal variation, minimizing the variation of R_{ON} with signal. This solution can impair bandwidth, since capacitance C_S may require a capacitor in parallel with the feedback resistor for compensation. Also, I_{LKG}, flowing through the feedback resistor, may cause significant error, depending on the accuracy requirements. ($\Delta V_{OUT} = I_{LKG} \times R_F$).

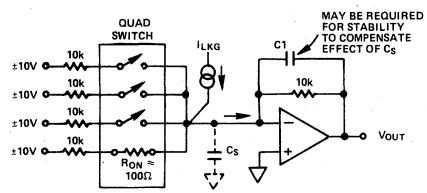


Figure 7. Connecting Switch at the Summing Point

Another possible solution is to use larger values of input and feedback resistance (Figure 8). Then the ΔR_{ON} variations will be small compared to the 1-megohm load. However, bandwidth will be affected by the larger R-C time constants.

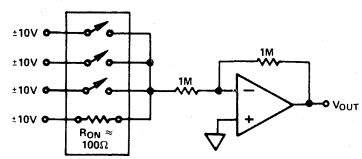


Figure 8. Using Larger Values of Resistance

Figures 7 and 8 do not compensate for the effects of variation of R_{ON} with temperature. A circuit that provides good compensation (Figure 9) uses one of the switches, wired *on*, in series with the feedback resistor. Its R_{ON} will tend to track that of the other switches on the same substrate with temperature; thus the feedback and input resistances will tend to track quite well, keeping the gain constant.

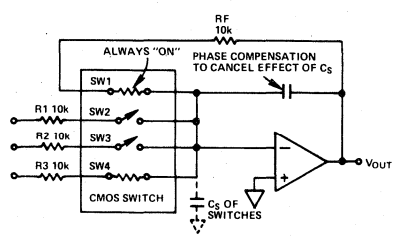


Figure 9. Switch in Series with Feedback Resistor to Compensate Gain

The principal dc effect in the switch *off* condition is that of I_{LKG} ($I_{D\ OFF}$ or $I_{S\ OFF}$), which will bias the output of a circuit by $I_{LKG} \times R_L$. Polarity of the error is determined by the dominant leakage polarity of a given switch.

AD7528 Dual 8-Bit CMOS DAC Application Note

By Paul Toomey and Bill Hunt

INTRODUCTION

The AD7528 is a monolithic dual 8-bit CMOS DAC packaged in a 20-pin DIP. Each DAC has its own 8-bit data latch which loads data from a common 8-bit data bus (see Figure 1). Since both DACs are fabricated on the same chip, precise matching and tracking between DACs is inherent. This property of the AD7528 dual DAC, along with the P.C. board space saving it allows, makes the AD7528 a unique and extremely useful device.

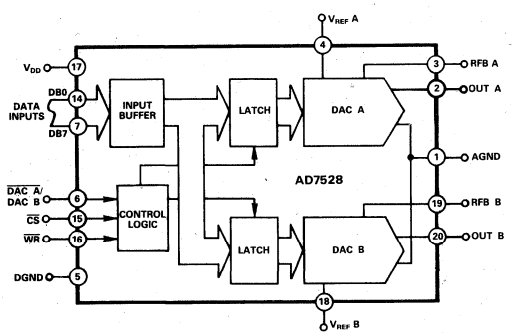


Figure 1. AD7528 Functional Diagram

This note discusses the AD7528 applications circuits listed below. Several of these circuits rely on the DAC to DAC matching provided by the AD7528. All of the circuits benefit from the high packing density the AD7528 allows, especially when used with dual and quad op-amps such as the AD644 or TL074. Not discussed in this note are basic details of AD7528 operation, consult the data sheet for this information.

AD7528 APPLICATIONS DISCUSSED IN THIS NOTE

1. State-variable filter (S.V.F.) with programmable center frequency, selectivity and gain.
2. Programmable sine wave oscillator with linear control.
3. Function fitting sine wave synthesizer with amplitude control facility and programmable phase shift.
4. Programmable voltage/current source, unipolar and bipolar circuits.
5. Programmable gain amplifier with no trimpots.
6. Programmable waveform generator for vector scan CRT displays.
7. AD7528 single-supply operation circuits for low budget applications requiring multiple analog outputs.

STATE VARIABLE FILTER WITH PROGRAMMABLE CENTER FREQUENCY, SELECTIVITY (Q) AND GAIN

The state variable filter (or universal filter as it is often called) is a convenient 2nd order filter block. It provides simultaneous low-pass, high-pass and bandpass outputs. All filter parameters can be readily adjusted. Figure 2 shows a typical filter circuit with expressions for center frequency, Q and gain for the bandpass output.

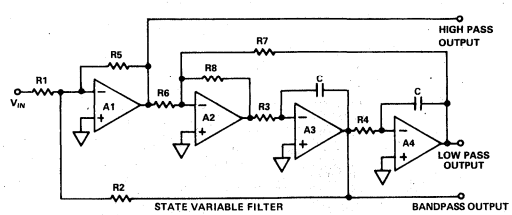


Figure 2. State Variable Filter

BANDPASS TRANSFER FUNCTION

$$\frac{V_{OUT}}{V_{IN}}(f) = \frac{A_O}{1 + jQ\left[\frac{f}{f_o} - \frac{f_o}{f}\right]}$$

$$f_o = \frac{1}{2\pi R3\,C} \cdot \sqrt{\frac{R8}{R7}} \quad (\text{For } R3 = R4)$$

$$Q = \frac{R6}{R8} \cdot \frac{R2}{R5} \cdot \sqrt{\frac{R8}{R7}}$$

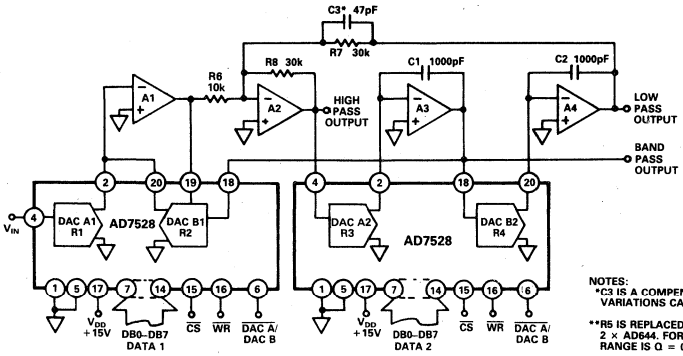
$$A_O = -\frac{R2}{R1}$$

Where f = frequency of V_{IN}

A_O = gain at $f = f_o$

Q = circuit Q factor, i.e., $\frac{f_o}{\text{3dB Bandwidth}}$

f_o = resonant frequency.



CIRCUIT EQUATIONS:

C1 = C2, R3 = R4, R7 = R8

$$f_o = \frac{1}{2\pi R3C1}$$

$$Q = \frac{R6}{R8} \cdot \frac{R2}{R5^{**}}$$

$$A_O = -\frac{R2}{R1}$$ **For Bandpass Output**

DAC EQUIVALENT RESISTANCE EQUALS

$$\frac{256 \times (\text{DAC LADDER RESISTANCE})}{\text{DAC DIGITAL CODE (DECIMAL)}}$$

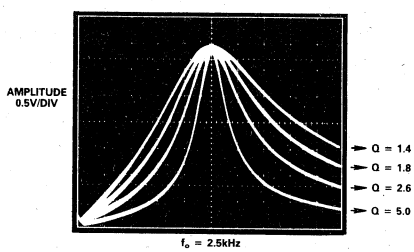
NOTES:
*C3 IS A COMPENSATION CAPACITOR TO ELIMINATE Q AND GAIN VARIATIONS CAUSED BY AMPLIFIER GAIN BANDWIDTH LIMITATIONS

**R5 IS REPLACED BY DAC B1 INTERNAL RFB ≈ 11kΩ, OP-AMPS ARE 2 × AD644. FOR COMPONENT VALUES SHOWN PROGRAMMABLE RANGE IS Q = 0.3 TO 4.5, f_o = 0 to 15kHz.

Figure 3. Digitally Controlled State Variable Filter

Introducing the DACs as Control Elements:

By replacing R1, R2 and R3, R4 with matched DAC pairs the filter parameters can be made programmable as shown in Figure 3. DAC A1 and DAC B1 control filter gain and Q, while DAC A2 and DAC B2 control center frequency (f_o). For the component values shown the programmable Q range is from 0.3 to 4.5 and is independent of f_o (see Figure 4). Center frequency (f_o) is programmable from 0 to 15kHz (see Figure 5) and is independent of Q.



Filter 4. Filter Q Variation

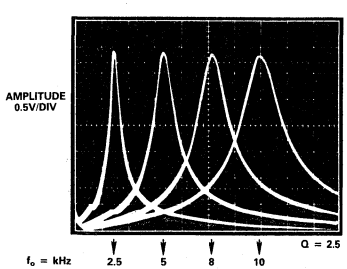


Figure 5. Filter f_o Variation

Programming

The graph in Figure 6 shows how the circuit Q varies with DAC B1 code and Figure 7 shows how the center frequency varies with DAC 2 (A and B) code for the component values given in Figure 3. Gain variation alone is accomplished by changing DAC A1 code. Unity gain occurs when the data in DAC A1 and DAC B1 latches is identical. Since the AD7528's logic inputs are TTL or CMOS compatible, the DACs are readily interfaced to most microprocessors, (see data sheet for hookups) thus providing an ideal microprocessor-to-filter interface.

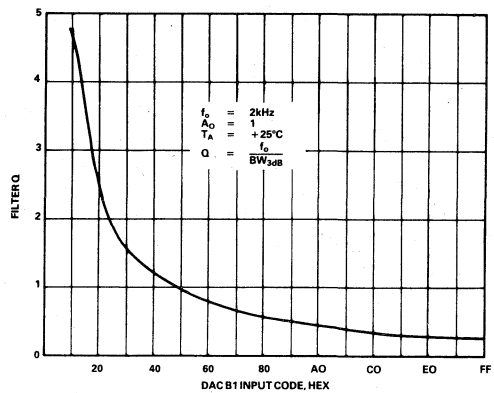


Figure 6. Filter Q Variation with Code

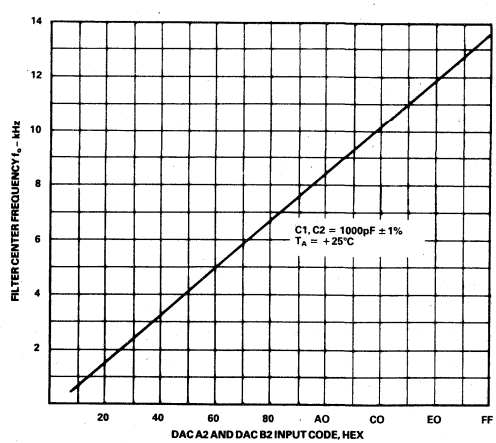


Figure 7. Filter f_o Variation with Code

PROGRAMMABLE SINE WAVE OSCILLATOR WITH LINEAR CONTROL

Frequency control of many oscillator circuits can be accomplished using two ganged potentiometers. However, the two potentiometers must track precisely over their full temperature range if a linear response is required. Figure 8 shows a high performance sine-wave oscillator realized using a state-variable filter. The frequency of oscillation is set by ganged potentiometers P1 and P2.

Figure 9 shows the same circuit with P1 and P2 replaced by the AD7528 matched pairs.

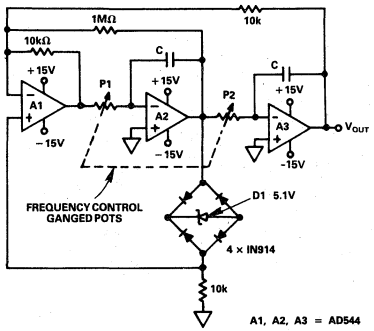


Figure 8. Sine Wave Oscillator Using a State Variable Filter

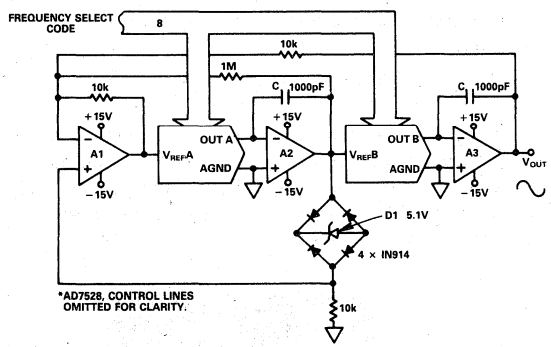


Figure 9. Programmable Sine Wave Oscillator Using a State Variable Filter and a Dual DAC

The equivalent resistance of each DAC, as seen by op-amps A2 and A3 varies with input code from infinity at code 00 Hex (0000 0000) to a minimum of ≈ 11kΩ (DAC ladder resistance) at code FF HEX (1111 1111).

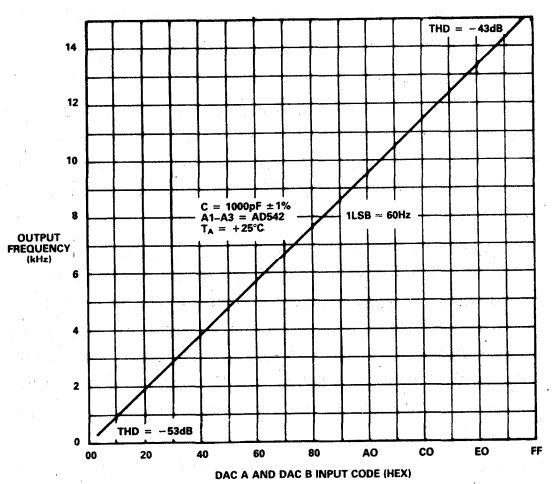


Figure 10. Frequency vs. DAC Code for Programmable Sine Wave Oscillator (Figure 9)

Loading each DAC latch with the same code provides a linear code versus frequency relationship as shown in Figure 10. The frequency of oscillation can be expressed as:

$$\text{Output Frequency} = \frac{N}{256\,(2\pi R\,C)}\ \text{Hz}$$

Where R = DAC ladder resistance i.e. V_{REF} input resistance.
C = is as shown in Figure 9.
N = decimal representation of digital input code. For example, N = 128 for input code 10000000.

For the component values given in Figure 9, output frequency is variable from 0 to 15kHz. Output amplitude is controlled by the zener diode D1. Total harmonic distortion for the circuit shown is −53dB at low frequencies (1kHz) and −43dB at higher frequencies (14kHz). Note that a cosine output is also available at the output of op-amp A2.

FUNCTION FITTING SINE WAVE SYNTHESIZER

In this application the multiplying capabilities of the two CMOS DACs are used to synthesize a sine wave based on a function fitting technique. This allows very low frequency, highly stable sine waves to be generated.

Function Fitting:

Function fitting is a technique for translating a mathematical or empirical relationship from one medium (such as a mathematical formula) to another medium (usually a physically realizable device or system). This application uses the dual DAC to implement a one quadrant sin X approximation in the form of the quadratic polynomial.

$$Y = 1.828N - 0.828N^2 \text{ where } 0 \le N \le 1 \text{ and } N = \frac{2}{\pi} X$$

The graph of Figure 11 shows the relationship between sin X and its quadratic approximation given above. The

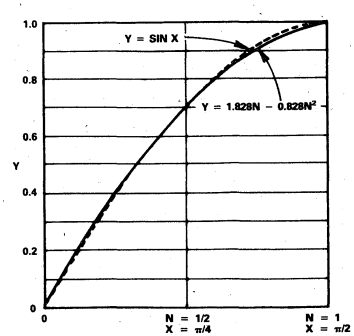


Figure 11. Relationship Between Sin X and its Quadratic Approximation

circuit of Figure 12 implements the function by ramping N up and down using an up/down counter, and switching the circuit output polarity. This generates sin X in four stages (see Figure 13).

Circuit Operation: (Figure 12)

An input clock drives the up/down counter in real time. The counter is connected so that it counts up and down continuously, providing an output pulse at "borrow" every time it reaches the all zeros count.

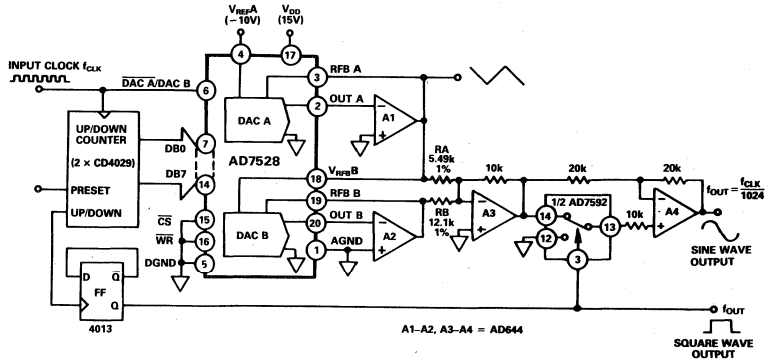


Figure 12. Function Fitting Sine Wave Generator

DAC A produces a triangle waveform consisting of two ramps of opposite slope, each generated in 256 steps at op-amp A1 output. This is the N variable.

DAC B is driven with the same digital word as DAC A. Its reference input is driven by op-amp A1, thus DAC B multiplies the digital version of N by the analog version of N to produce an output from op-amp A2 of $-N^2$ (negative sign is due to inversion through A2).

Since the N and $-N^2$ signals are of opposite polarity, the $Y = 1.828N - 0.828N^2$ expression is implemented by summing N and $-N^2$ signals in the correct ratios determined by RA and RB.

The analog switch, in conjunction with op-amp A4, changes the circuit's output polarity at one-half the triangle wave frequency, thus producing both positive and negative halves of the sine wave.

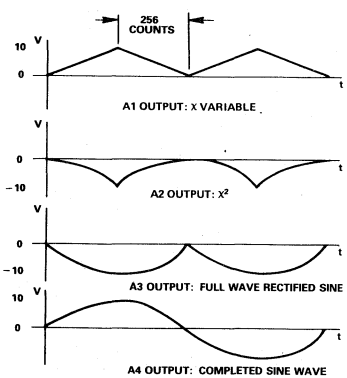


Figure 13. Sine Wave Synthesis Using Function Fitting

Distortion:
Distortion in the output sine wave is a function of the quadratic approximation fit to the sine curve. Errors in the values of R_A and R_B will, therefore, contribute directly to distortion. If R_A is made adjustable over a small range, it can be trimmed to minimize distortion. Distortion was measured for the circuit of Figure 12 at –33dB and was constant over sine-wave frequency 0–2.5kHz.

The circuit of Figure 12 generates constant amplitude sine waves in the 0–2.5kHz frequency range. Output frequency is given by

$$f_{OUT} = \frac{f\,clk}{1024}$$

It is possible to obtain rapid frequency sweeping by varing the input clock rate. The counter up/down output provides a useful zero crossing pulse. By applying an ac signal to the DAC A reference input, the output sine wave can be amplitude-modulated as shown in Figure 14.

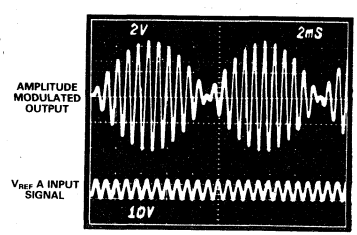


Figure 14. Amplitude Control Using DAC A Reference Input

Output amplitude is directly controlled by the voltage level on DAC A reference input. Ac or dc signals may be used within the range ±10 volts, 0 to 10kHz. Figure 14 shows the amplitude of a 1kHz sine wave being controlled by a 55Hz sine wave.

Programmable Phase
Two sine waves with 0 to 360°programmable phase relationship can be generated by running two of the circuits, shown in Figure 12, from the same input clock source. By allowing one circuit to start running from zero count a preset number of clock cycles before the other, a phase difference between their output sine waves is introduced (see Figure 15).

Since each complete cycle is generated by 1024 clock cycles, phase steps of 360/1024 degrees are programmable. Note also that the phase difference is independent of output frequency.

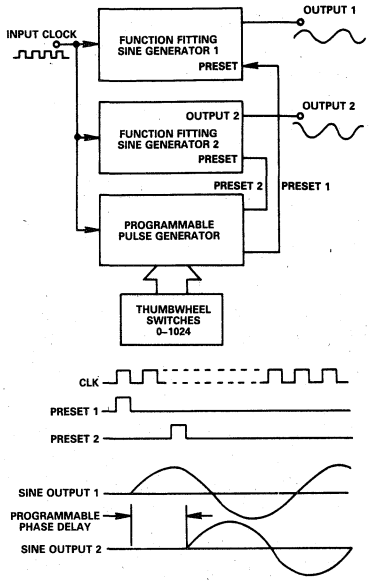


Figure 15. Programmable Phase Relationship

PROGRAMMABLE VOLTAGE/CURRENT SOURCE USING DUAL DAC AD7528

The circuit in Figure 16 is that of a unipolar V/I source. A negative reference is required for a positive output voltage.

The circuit provides;

(a) A programmable output voltage

$$V_{OUT} = +V_{REF}A \frac{N_A}{256}, \text{ for } N_A = 0 \text{ to } 255.$$

provided the current limit is not exceeded.

(b) In the voltage mode, a programmable load current limit given by:

$$I_{OUT(max)} = V_{REF}B \cdot \frac{R_1}{R_2} \cdot \frac{1}{R_{S2}} \cdot \frac{N_B}{256}$$

for $N_B = 0$ to 255.

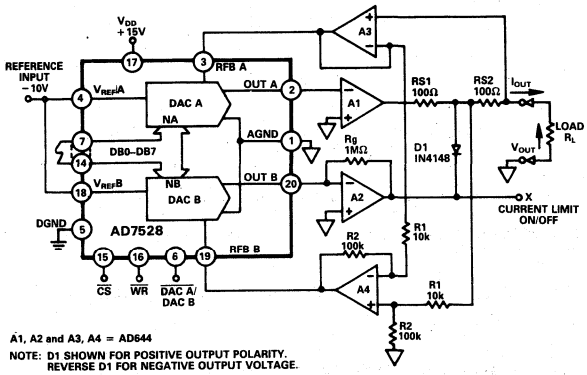


Figure 16. Programmable Voltage/Current Source V_{OUT} = 0 to +10V, I_{OUT} = 0 to +10mA

(c) A constant current feature by setting $N_A = 255$ i.e., maximum output voltage capability, and limiting the load resistance value R_L such that

$$I_{OUT(max)} \cdot R_L < \frac{255}{256} V_{REF}A$$

with $I_{OUT\ (max)} = V_{REF}B \cdot \frac{R_1}{R_2} \cdot \frac{1}{R_{S2}} \cdot \frac{N_B}{256}$

as in (b).

A useful feature of the circuit is the possibility of load current "readback" in the voltage mode (or load voltage readback in the current mode). By monitoring point X in Figure 16, as the current limit value is reduced, a state change will take place when current limit is attained. The set current limit value will correspond to the load current.

In the circuit DAC A with amplifier A1 and buffer A3 acts as a standard programmable voltage source when $V_{REF}A$ is held constant. The voltage drop across resistor R_{S2} provides a voltage proportional to load current with R_{S1} acting as a current limit on amplifier A2. Amplifier A4 with resistors R_1 and R_2 references the voltage across R_{S2} to ground and also provides gain $\left(\frac{R_2}{R_1}\right)$. The output of A4

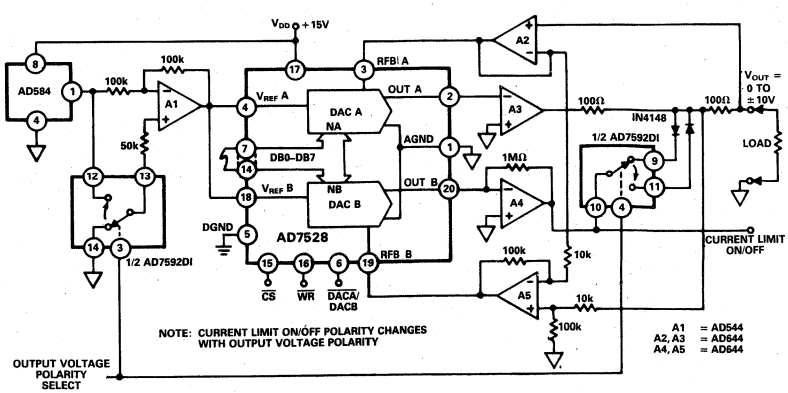


Figure 17. Programmable Voltage/Current Source with Bipolar Output

is compared with a proportion $\frac{N_B}{256}$ of $V_{REF}B$ (usually $V_{REF}A = V_{REF}B$) by amplifier A2. If $V_{OUT4} > V_{REF}B\frac{N_B}{256}$ then current limit is required and the output of A2 via diode D1 draws load current to maintain a constant load current.

If $V_{OUT4} < V_{REF}B\frac{N_B}{256}$ then the current limit is not required and amplifier A2 output is disconnected as diode D1 is reversed biased.

Figure 17 shows a similar circuit for bipolar operation, i.e., 0 to ±10V at 0 to ±10mA.

DUAL DAC PROGRAMMABLE GAIN AMPLIFIER WITH NO TRIMPOTS

A unique advantage of the matched DACs available in the AD7528 is utilized in the programmable gain/attenuation circuit shown in Figure 18. The equivalent resistance of each DAC from its reference input to its output is used to replace the input and feedback resistors in the standard inverting amplifier circuit. By loading DAC's A and B with suitable codes, programmable gain/attenuation over the range −48dB to +48dB can be achieved.

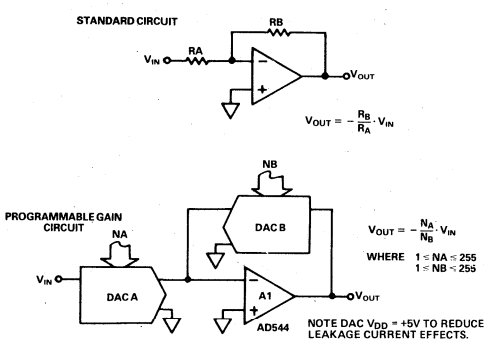


Figure 18. Dual DAC Programmable Gain Amplifier

In the circuit of Figure 18, the DAC equivalent resistances are given by:

$$R_{DAC}A = \frac{256\,R_{LD}A}{N_A} \text{ and } R_{DAC}B = \frac{256R_{LD}B}{N_B}$$

Where: $R_{LD}A$ and $R_{LD}B$ are DAC A and DAC B R-2R ladder resistances respectively, N_A and N_B are the DAC codes in decimal (1–255).

The resultant gain expression for the circuit is

$$\frac{V_{OUT}}{V_{IN}} = -\frac{256\,R_{LD}B}{N_B} \cdot \frac{N_A}{256\,R_{LD}A}$$

This simplifies to:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_{LD}B \cdot N_A}{R_{LD}A \cdot N_B}$$

But since DAC A and DAC B are a matched pair, $R_{LD}A = R_{LD}B$. This simplifies the expression even further to give:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{N_A}{N_B} \qquad 1 \le N_A \le 255 \qquad 1 \le N_B \le 255$$

Notice that DAC ladder resistance does not appear in the expression. Previous PGA circuits using DACs have always had to be trimmed to accommodate the DAC ladder resistance which usually has a wide tolerance (typically 8k to 20k). This circuit does not suffer from this problem since $R_{LD}A$ and $R_{LD}B$ are matched to better than 1%. Notice also that the circuit has a constant input resistance of $R_{LD}A$. The two unused feedback resistors, $R_{FB}A$ and $R_{FB}B$ are also precisely matched and could be used to provide other DAC code vs. gain relationships.

PROGRAMMABLE WAVEFORM GENERATOR FOR VECTOR SCAN CRT DISPLAYS

Figure 19 shows the dual DAC in a triangle/rectangle wave generator in which the period of each half cycle can be programmed. Such a circuit is useful for vector scan CRT displays to generate variable rate sweep signals (depending upon whether a long or short vector is to be drawn). DAC A determines the ramp rate for the positive going ramp of the triangle while DAC B determines the ramp rate for the negative going ramp. The integrator output voltage is sensed by comparators A4 and A5. When this voltage reaches +10V or −10V the comparators drive the R-S flip-flop G1 and G2 which selects the output of the appropriate DAC via the double-pole ganged analog switch SW1, SW2.

The switching arrangement shown has the advantage that high speed switches (such as CD 4016 or AD7519) can be used to change between the two DACs without introducing significant output glitches at the changeover.

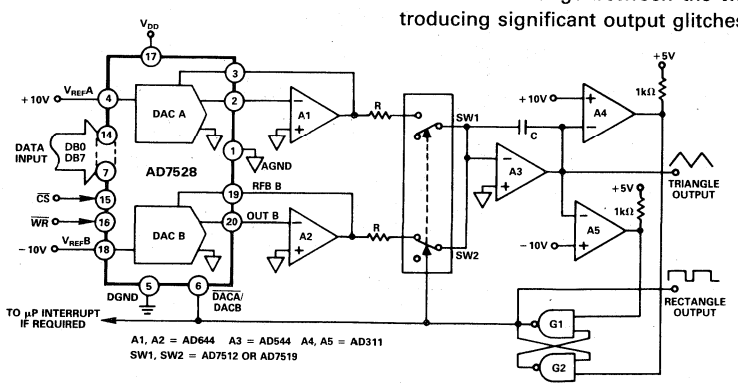


Figure 19. Digitally Programmable Waveform Generator

Furthermore, one DAC can be updated from the data bus and allowed to settle while the output of the other DAC is being used to generate the ramp signal. The output of flip-flop G1 and G2 automatically connects the "unused DAC" to the data bus for further data update if necessary. The output of the flip-flop can be used to drive the interrups of a microprocessor if required.

Selecting Waveform Parameters:

The period (t) of the waveforms generated by the circuit is given by:

$$t = 512\,RC\left[\frac{1}{N_A} + \frac{1}{N_B}\right]$$

where N_A and N_B are the DAC A, DAC B codes in decimal (1–255) respectively.

If DAC A and DAC B latches contain the same codes, the expression simplifies to:

$$t = \frac{1024\,RC}{N_A} \text{ i.e., output frequency } f = \frac{N_A}{1024\,RC}\ \text{Hz}$$

The mark-to-space ratio of the rectangle wave output is dependent on the ratio of N_B to N_A

$$\text{Mark to Space Ratio} = \frac{N_A}{N_B}$$

A special case, exists when the code in either DAC is zero. In this case the circuit will stop oscillating as the integrator input voltage will be zero. If the all zeros condition can occur, it is advisable to connect a 10MΩ resistor from the V_{REF} terminal to the output terminal of each DAC, i.e, V_{REF}A to OUT A and V_{REF}B to OUT B. This provides sufficient bias current to keep the circuit oscillating, and does not affect frequency calculations significantly as the 10M resistor introduces only 1/4 LSB of additional error into each DAC output.

AD7528 SINGLE SUPPLY OPERATION

In low budget digital designs requiring analog outputs, the cost of adding an extra power supply rail for the DAC circuits can be a limiting factor. The AD7528 in the single supply configurations shown below provides an ideal cost effective solution for such applications (especially where multiple analog outputs are required).

Single Supply, Voltage Switching Mode:

In this mode, the normal DAC R-2R ladder is inverted. The reference voltage is applied to the DAC OUT A or OUT B terminal and the output voltage is taken from the DAC V_{REF}A or V_{REF}B terminal. For the DACs to retain their specified linearity, the reference voltage range must be restricted as follows:

For $V_{DD} = +15V$, V_{REF} max $= +2.5V$

For $V_{DD} = +5V$, V_{REF} max $= +0.5V$

Figure 20 shows a circuit for use with a +15 volt power supply giving four separate 0 to +10V outputs. The op-amps used have a Class A output configuration for small signal levels, thus allowing their outputs to go to zero volts for zero volts input. At higher signal levels, the outputs convert to Class B.

Single Supply, Current Steering Mode:

This mode of operation is described in the AD7528 data sheet, and is suitable for single +10 volt to +15 volt supply operation. This is achieved by biasing the AD7528 analog ground (AGND) +5 volts above the power supply ground. Unlike the previous circuits the available drive for the DAC switches is now V_{DD} −5 volts so the 5 volt specifications apply for linearity. Figure 21 shows how a +2 volt to +8 volt analog output may be obtained using two op-amps per DAC. The two DAC reference inputs are tied

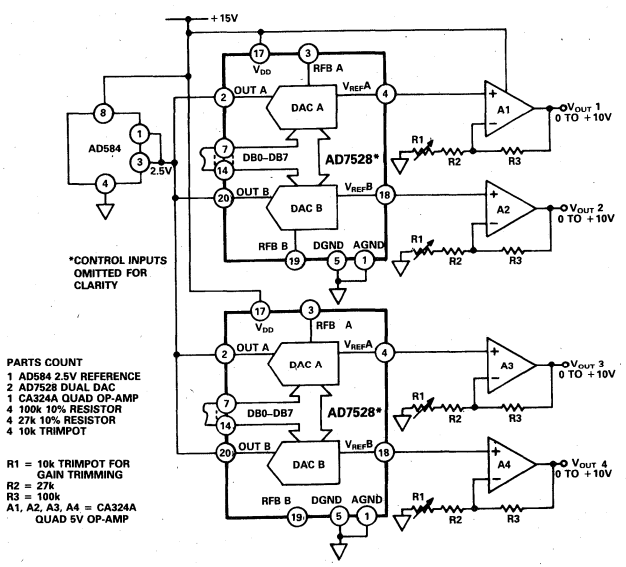


Figure 20. Four Channel Analog Output Circuit

20

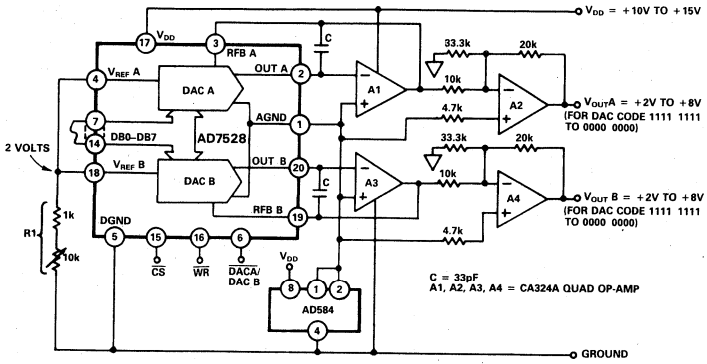


Figure 21. AD7528 Single Supply Operation with AGND Biased to +5 Volts

together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1; R1 is adjusted until V_{REF}A and V_{REF}B inputs are at +2 volts. The adjustment is independent of either DAC code.

Each analog output channel has a +2 to +8 volt range for DAC codes 1111 1111 to 0000 0000.

Reference

Dan H. Sheingold, "Nonlinear Circuits Handbook," available from Analog Devices.

D. P. Burton, Application Note "Methods For Generating Complex Waveforms And Vectors Using Multiplying D/A Converters" Analog Devices Publication Number: E671–15–9/81.

Application Guide to CMOS Multiplying D/A Converters, Analog Devices Publication Number: G479–15–8/78.

The AD7574 Analog to Microprocessor Interface

by Paul Toomey

INTRODUCTION

The AD7574 is a low cost 8-bit ADC designed for easy interface to microprocessors as a memory mapped input device.

It uses a successive-approximations conversion technique, runs with an internal or external clock and can complete an 8-bit A/D conversion in 15 microseconds.

The analog to digital conversion operations are controlled by two logic inputs labelled $\overline{CS}$ ($\overline{Chip\ Select}$) and $\overline{RD}$ ($\overline{READ}$). Conversion-in-progress indication is provided by a $\overline{BUSY}$ output signal (see Figure 1).

This note is intended to describe the AD7574 in its three main microprocessor interface modes with references to external clock source, input range switching and input multiplexing applications.

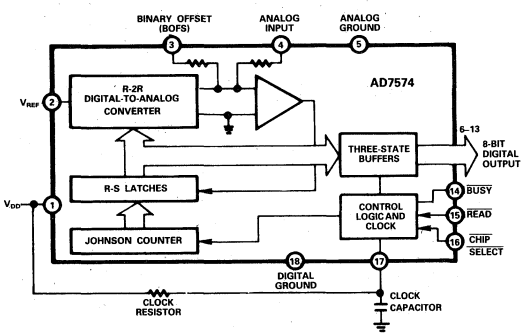


Figure 1. Inside the AD7574

INTERFACE MODES

Since the AD7574 is designed for use in memory mapped applications it can simulate RAM, ROM, or SLOW-ROM memories and can be controlled using standard chip select, READ and WRITE signals common to all memory systems.

ROM MODE

The ROM Mode is the easiest mode in which to use the AD7574. It appears in the processor memory map as one byte of Read Only Memory. One instruction from the CPU both reads conversion data and initiates a new conversion.

Basic Operation: The processor reads the 8 bits of data generated by a previous A/D conversion by executing a READ instruction from the memory address location assigned to the AD7574. When the processor $\overline{RD}$ signal goes LOW the AD7574 three state drivers are activated, placing the conversion data onto the processor data bus.

At the end of the READ instruction the AD7574 $\overline{RD}$ input is returned HIGH, resetting the device and initiating a new A/D conversion sequence (see Figure 2).

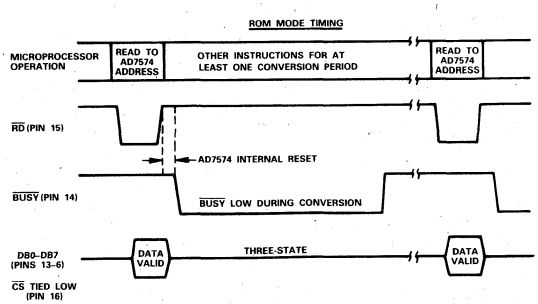


Figure 2.

Typical ROM MODE interface circuits for 8080 and 8085 microprocessors are shown in Figures 3 and 4. Most processors can be configured to operate with the AD7574 in this mode. Note: Any attempt to read data from the AD7574 during a conversion operation will result in incorrect data being read.

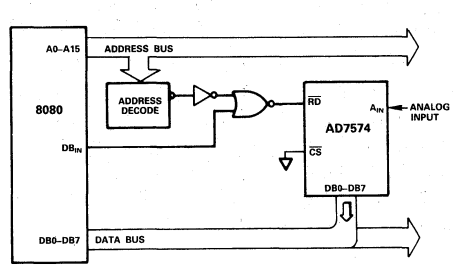


Figure 3. AD7574 to 8080 ROM-MODE Interface

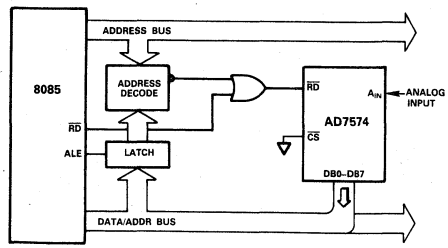


Figure 4. AD7574 to 8085 ROM-MODE Interface

Applications Of The Rom Mode

The advantage of this mode is its simplicity in both software and hardware terms. Reading conversion data is accomplished by just one memory READ instruction. However, it must be remembered that the data read will be the result of the previous conversion operation. This means that the time reference for the data sample will depend on when the previous READ operation finished. In applications where this uncertainty creates problems it can be eliminated by executing two READ operations separated by a software delay as shown in Figure 5.

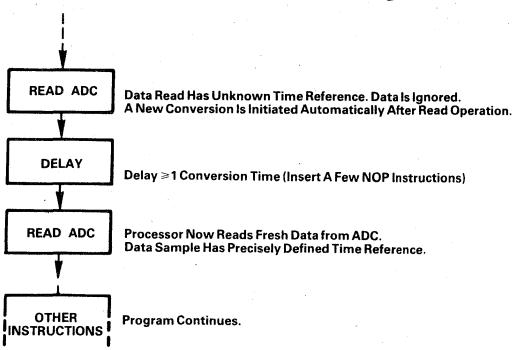


Figure 5. Defining the Data Sample Time Reference (ROM- MODE)

RAM MODE

Basic Operation

In the RAM MODE the AD7574 appears in the processor memory map as one byte of memory. A WRITE command initiates a conversion and a READ command reads the conversion data.

This mode offers complete control over the converter operation. The time reference for the data sample is defined by the WRITE command. The conversion data can be read any time after the conversion has finished.

In the RAM MODE a memory WRITE operation starts a conversion without modifying any of the microprocessor accumulators. (In the ROM mode, using a READ instruction to start a conversion means modifying an accumulator unnecessarily.) So, in situations where the age of a sample is important the RAM MODE makes for simpler, more logical software than the ROM MODE at the expense of requiring slightly more logic to drive $\overline{CS}$ and $\overline{RD}$ (see Figures 8 and 9).

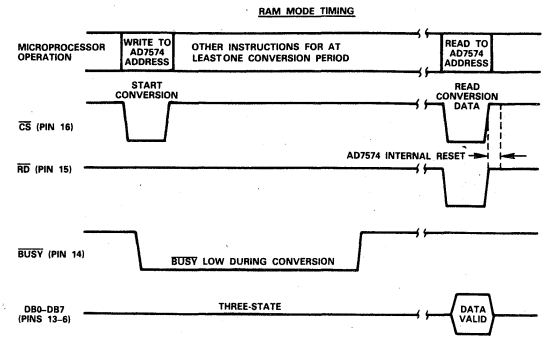


Figure 6.

Ram Mode Timing Considerations

1. $\overline{BUSY}$ must be high before a data read is attempted, i.e., delay from conversion start to data read must be at least as great as the AD7574 conversion time. In some situations it is possible to use the AD7574 $\overline{BUSY}$ output to halt the microprocessor for the duration of the conversion period thus simplifying the software requirements.
2. $\overline{CS}$ must return HIGH within 250ns after $\overline{RD}$ goes HIGH otherwise a new conversion may be initiated and the AD7574 will begin operating in the ROM mode (see Figure 7).

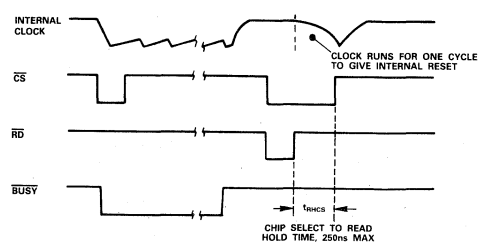


Figure 7. Chip Select to Read Timing

When $\overline{RD}$ returns high the AD7574 begins an internal reset cycle to prepare for the next conversion sequence. If $\overline{CS}$ has not returned high before the end of this reset operation, a conversion start will be detected and a new conversion initiated.

The duration of the internal reset cycle is dependent on the amount of capacitance on the clock pin (pin 17). The maximum value for t_{RHCS} guaranteed is 250ns at 25°C (see data sheet).

3. Conversion data may only be read from the AD7574 once, as after each read operation an internal reset is performed which destroys the data.
4. $\overline{CS}$ LOW has no effect while a conversion is in progress.
5. $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH.

Typical RAM Mode interface circuits for the 8085 and 6800 are shown in Figures 8 and 9 respectively.

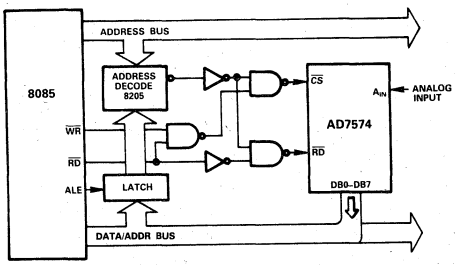


Figure 8. AD7574 to 8085 RAM Mode Interface

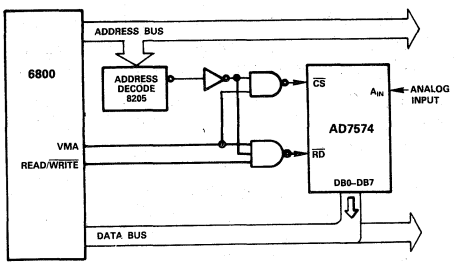


Figure 9. AD7574 to 6800 RAM Mode Interface

SLOW MEMORY MODE

This is by far the most elegant mode of operation for the AD7574. Every read instruction produces fresh data so that there is no doubt about the age of the sample.

Basic Operation

The slow memory mode is intended for use with processors which can be forced into a wait state for at least 15μs (such as the 8080, 8085 and SC/MP). It allows the processor to start a conversion, wait until the $\overline{BUSY}$ flag is HIGH and then read data, all during execution of a single memory read instruction (see Figure 10).

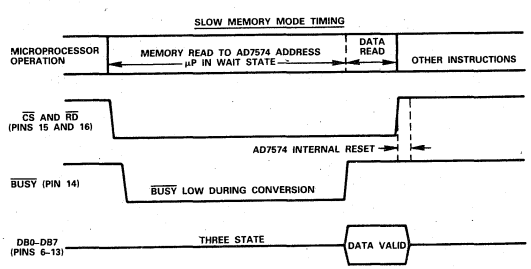


Figure 10.

Wait State

Many processors test the condition of the READY/WAIT input very soon after the start of an instruction cycle. For this reason the timing of the AD7574 and its associated address decode logic must be such that $\overline{BUSY}$ goes LOW early enough in the processor instruction cycle for the READY/WAIT input to be effective in forcing the processor into a WAIT State.

Bus Conflict

In applications where the processors memory READ/WRITE signal is not available early enough in the machine cycle for it to be used to enable or disable the address decode logic, the system software must be such that a WRITE operation to the AD7574 address is never attempted. If this precaution is not taken, Bus Conflicts will occur due to the AD7574 outputting data onto the data bus while the CPU is also driving the data bus.

Typical slow memory mode interface circuits for 8085 and SC/MP microprocessors are shown in Figures 11 and 12.

8085 Interface (Figure 11)

For simplicity, only the upper 8 address bits of the 8085 address bus are decoded to select the AD7574. Invalid address states are eliminated by using ALE to drive an address latch.

The processor SO status signal provides the earliest possible indication that a READ operation is about to occur, SO = 0 for a READ operation. Since, with the processor on a fast clock the READ signal could occur too late to enable the address decode logic, the SO signal is a convenient alternative, elminating any possibility of a bus conflict during WRITE operations.

SC/MP Interface (Figure 12)

Similar to the 8085 application. Address decode is gated with negative READ strobe and $\overline{BUSY}$ drives the SC/MP negative hold input.

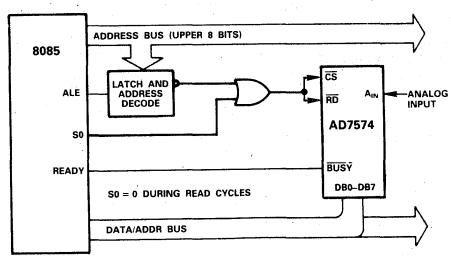


Figure 11. AD7574 to 8085 Slow Memory Mode Interface

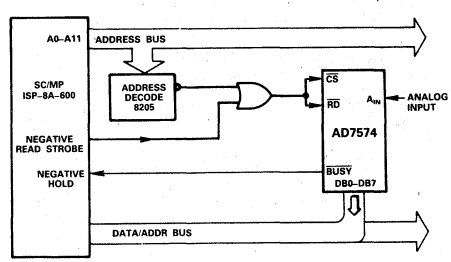


Figure 12. AD7574 to SC/MP Slow Memory Mode Interface

RANGE SWITCHING APPLICATIONS

By means of suitable switching on the AD7574 B_{OFS} and V_{REF} pins, the AD7574 can be made to operate with a range of different attenuation or gain factors. The B_{OFS} or bipolar offset input (pin 3) is used to modify the effective analog input voltage and is normally used to obtain bipolar operation. Figure 13 shows a simple, 3 range, switching arrangement for a 0–20V analog input signal. The full scale input ranges and LSB weights are given in Table I.

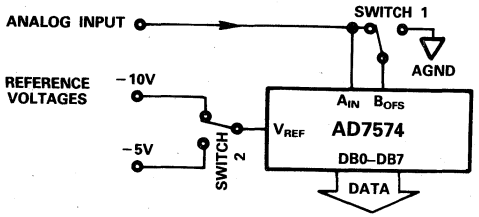


Figure 13. Range Switching the AD7574

BOFS	V_{REF}	Full Scale Input Range	LSB Weight
To A_{IN}	−5V	0V to +5V	19mV
To A_{IN}	−10V	0V to +10V	39mV
To GND	−10V	0V to +20V	78mV
To GND	−5V	0V to +10V	39mV

Table I. AD7574 Input Ranges

The range switching can easily be controlled by the processor using analog switches such as the AD7592 which contains 2 independent SPDT CMOS switches with data latches specifically designed for microprocessor interface.

Figure 14 shows a typical range switching applications circuit with the AD7574 operating in the the slow-memory mode. Since bus conflicts have been eliminated, a WRITE to the AD7574 address selects the analog input voltage range (see Table II) and a READ from the AD7574 address initiates a conversion and reads data when the conversion is complete.

The range selection code is latched by the AD7592 and so need only be considered when a change in analog input range is required.

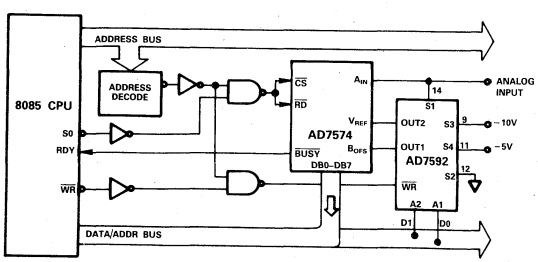


Figure 14. AD7574/8085 Interface with Range Switching

D1	D0	Analog Input Range
0	0	0V to +10V
0	1	0V to +5V
1	0	0V to +20V
1	1	0V to +10V

Table II. Analog Input Range vs. Digital Code to AD7592 for Figure 14

Note: If it is required to use this approach in a system where the WRITE operation bus conflict cannot be eliminated due to timing difficulties, then by decoding a separate address for the AD7574 and the AD7592 the need for a WRITE operation to the AD7574 address can be avoided.

INPUT MULTIPLEXING APPLICATIONS

This application uses the same principles as the range switching application. The analog switching devices have been changed to AD7590s to reduce the package count. The AD7590 consists of four independent SPST CMOS analog switches with on chip data latches (see Figure 15).

Using two AD7590 devices and connecting the data bus directly to the AD7590 control inputs, 8 analog input channels can be multiplexed. The software design must ensure that only one channel is selected at a time. Errors introduced by the analog switch resistance are not significant but can be eliminated by buffering the AD7574 B_{OFS} and A_{IN} inputs.

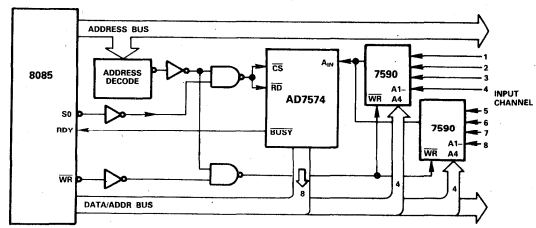


Figure 15. AD7574/8085 Interface with Input Multiplexing of 8 Analog Inputs

A WRITE to the AD7574 address selects an input channel and latches it. A READ from the AD7574 address initiates a conversion and reads data when the conversion is complete.

INTERNAL CLOCK OPERATION

Figure 16 shows a simplified equivalent circuit for the AD7574 internal clock. It operates only during conversion and reset operations, pulses are generated by the action of C charging through R, and discharging through switch 1.

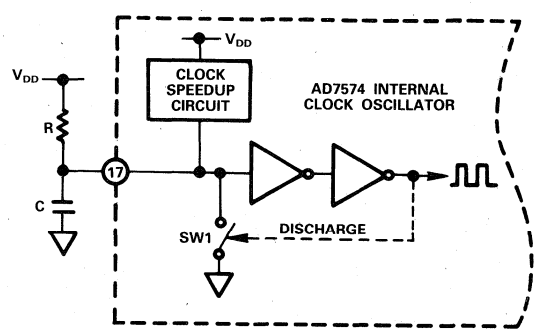


Figure 16. Simplified AD7574 Internal Clock Circuit

A clock speedup circuit shortens the last clock space period in each conversion cycle to reduce overall conversion time. Figure 17 shows a RAM mode timing sequence using the internal clock; other modes have similar timing.

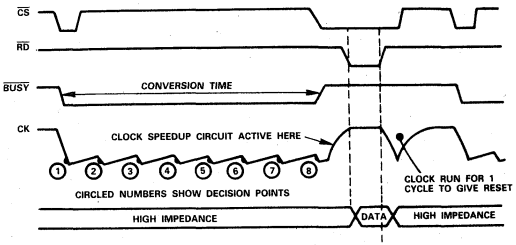


Figure 17. RAM Mode Timing Sequence

Typical values for internal clock timing components can be determined from the graph in the AD7574 data sheet (Figure 7a).

EXTERNAL CLOCK INFORMATION

To obtain dynamic conversion accurcy to rated specification the clock frequency must not exceed 500kHz. The user should understand that normal lot to lot variations in MOS transistor characteristics will cause lot to lot differences in the internal clock oscillator frequency for a given clock R and C.

Additionally, temperature dependence of these MOS characteristics results in thermal drift of internal clock frequency. For this reason, Analog Devices recommends using an external clock in the following situations:

1. Applications having clock frequency within 10% of the 500kHz maximum.
2. Applications where software constraints on time cannot accommodate conversion time differences which may occur due to temperature drift of the internal clock.

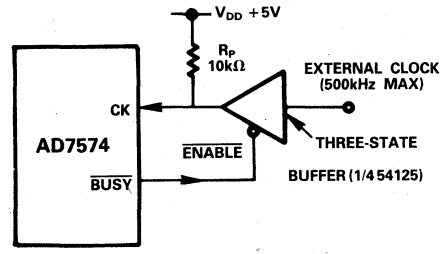


Figure 18. External Clock Connection

Conflicts between the external clock and the internal speedup and reset operations can be avoided by connecting the external clock using the arrangement shown in Figure 18. The three-state buffer is only enabled when the $\overline{BUSY}$ output is LOW. This ensures that the AD7574 uses the external clock only during the A/D conversion period, i.e., while $\overline{BUSY}$ is LOW. Internal clock operation is then used with R_P and internal capacitance to give the single clock pulse required for the internal reset.

Since the internal logic of the AD7574 is triggered on falling clock edges, conversion time is reduced if the clock input is at a HIGH level before a conversion starts. This is accomplished by using resistor R_p to pull up the device clock input after the internal reset operation. R_p can be in the range 6kΩ to 100kΩ and simply provides a charge path for the CLK pin capacitance.

ANALOG DEVICES

APPLICATION NOTE

Understanding LOGDACs™

INTRODUCTION TO THE ANTILOG D/A CONVERTER

Analog Devices' AD7100 Series LOGDACs are CMOS multiplying DACs characterized by an exponential (antilogarithmic) digital-to-analog transfer function.

Perhaps the easiest way to visualize what a LOGDAC does is to compare it to two well-known circuits—the classic 3-terminal potentiometer and a CMOS multiplying DAC (digitally controlled potentiometer). As shown in Figure 1a through Figure 1c, the transfer function of all three circuits is of the form:

$$V_{OUT} = \alpha V_{IN} \qquad \text{EQN1}$$

WHERE:
α = attenuation factor
$0 \leq \alpha \leq 1$

In each case shown in Figure 1, α is a dimensionless number which can range from 0 (maximum attenuation) to approximately 1 (minimum attenuation). Additionally, each circuit has an analog input (V_{IN}), an analog output (V_{OUT}) and a mechanism for controlling the attenuation factor α.

The above in conjunction with Figure 1a through Figure 1c illustrates the similarity of the pot, M-DAC and LOGDAC functions. How, then does the LOGDAC *DIFFER* from the linear M-DAC?

The answer is resolution. The basic differentiating feature of the LOGDAC versus the linear multiplying DAC is the way resolution is specified.

RESOLUTION OF LOGDACs VERSUS LINEAR DACs

From Figure 1b, the attenuation factor α of a linear DAC is:

$$\alpha = \left(\frac{N}{2^n}\right) \qquad \text{EQN2}$$

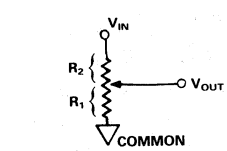
WHERE:
n = Number of digital input bits to the DAC
N = Integer value of DACs digital input

NOTE: Many treatments of multiplying DACs label the attenuation factor "D" where the digital input "D" is:

$$D = \alpha = \left(\frac{N}{2^n}\right) = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \ldots \frac{\text{Bit n}}{2^n}$$

WHERE: Bit 1 through Bit n = 1 or 0
n = Number of bits

Since N was postulated to be an integer, the smallest possible change of N is plus or minus one count. The resolution of α is, therefore, ± 1 part in 2^n or 1 part in full scale. Important to realize is that the voltage resolution of a linear DAC is the same (barring differential nonlinearity effects) at all points on its transfer function.



$V_{OUT} = \left(\frac{R_1}{R_1 + R_2}\right)(V_{IN})$

FORM: $V_{OUT} = \alpha V_{IN}$

WHERE: α = ATTENUATION FACTOR = $\left(\frac{R_1}{R_1 + R_2}\right)$

Figure 1a. Three Terminal Pot

The resolution of a LOGDAC is different, however. The following discussion shall endeavor to show that a LOGDAC's voltage resolution is different at all points on its transfer function, i.e., barring differential nonlinearity effects, the resolution expressed as a *percent of reading* (not percent of full scale) is constant throughout the LOGDACs range.

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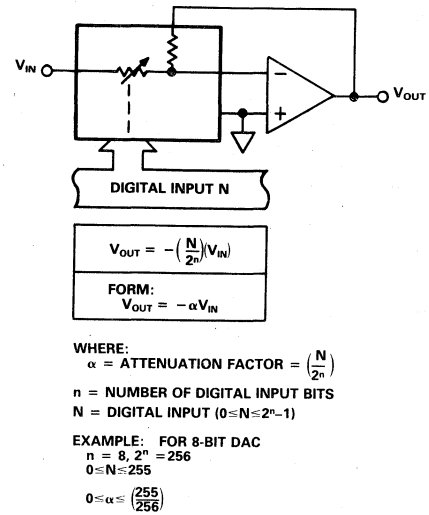


Figure 1b. Linear Multiplying DAC (Digitally Controlled Pot)

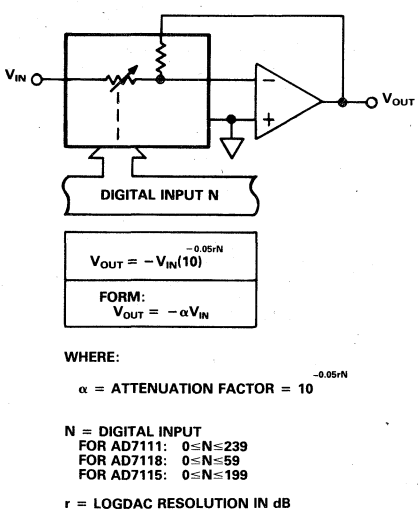


Figure 1c. LOGDAC (Digitally Controlled Pot)

From Figure 1c, the LOGDACs attenuation factor α is an exponential function (antilog) of the basic form:

$$y = a^{-x} \qquad \text{EQN3}$$

If base number 10 is chosen (other base numbers can be used, incidentally), the attenuation factor α for the LOGDAC of Figure 1c becomes:

$$\alpha = 10^{-\left(\frac{rN}{20}\right)} \qquad \text{EQN4}$$

WHERE:

N = Integer value of DACs digital input
- for AD7115: $0 \le N \le 199$
- for AD7111: $0 \le N \le 239$
- for AD7118: $0 \le N \le 59$

r = LOGDAC resolution in dB
- for AD7115: r = 0.1
- for AD7111: r = 0.375
- for AD7118: r = 1.5

Taking the LOG of both sides of EQN4 gives:

$$\log_{10}\alpha = -\left(\frac{rN}{20}\right)$$

$$20\log_{10}\alpha = -rN$$

$$\therefore \quad \alpha_{dB} = -rN \qquad \text{EQN5}$$

From EQN5, it is readily apparent that a plus one count change of N causes an attendant $-$(r)dB change in the attenuation factor α (and thus also a $-$(r)dB change in the DAC's output voltage).

Figure 2 is a graph of the general LOGDAC transfer function for the circuit of Figure 1c. It shows quite simply that increasing the digital input N causes a decrease in the output voltage V_{OUT}. Additionally, it shows the nonlinear relationship of V_{OUT} relative to N. Figure 3 is an expanded section of the transfer function shown in Figure 2. It illustrates the fact that the ratio of any two adjacent LOGDAC output voltage levels is the same throughout the transfer function. To further amplify the significance of this point, consider that a + one count change in the digital input N causes the output voltage to decrease in amplitude by a *fixed ratio relative to where it was before the change*. (At all points on its transfer function . . .) Thus, we have a DAC with *percent of reading* resolution as opposed to the linear DAC which defines resolution in terms of *percent of full scale*.

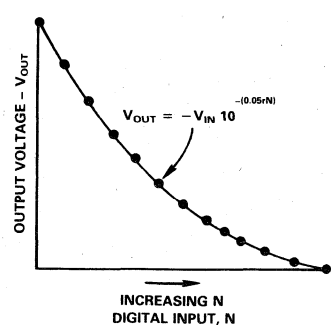


Figure 2. LOGDAC D/A Transfer Characteristic

To summarize, a linear DAC's voltage resolution is fixed throughout its transfer function. However, the LOGDAC

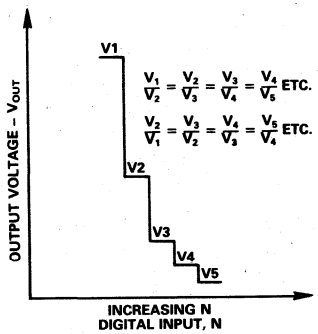


Figure 3. Expanded LOGDAC Transfer Function Illustrating the Concept of % of Reading Resolution

exhibits a continuously variable output voltage resolution throughout its transfer function range. The LOGDAC's voltage resolution is coarsest at or near full scale (0dB) and finest at or near 0 scale (mute). Table I shows the equivalent percent of reading resolution for various Analog Devices LOGDACs.

Model	dB Resolution (ΔN = ±1 Count)	% of Reading Resolution (ΔN = +1 Count)	(ΔN = −1 Count)
AD7118	±1.5dB	−15.9%	+18.9%
AD7111	±0.375dB	−4.2%	+4.4%
AD7115	±0.1dB	−1.1%	+1.2%

Table I.

BASIC CIRCUIT CONFIGURATIONS

ANTILOG DAC (Exponential with Negative Exponent)

The circuit of Figure 4 generates output voltage levels as determined by the equations:

$$V_{OUT} = -V_{IN}10^{-\left(\frac{rN}{20}\right)} \quad \text{EQN6}$$

and/or

$$V_{OUT} = -V_{IN}e^{-(0.11512rN)} \quad \text{EQN7}$$

WHERE:

r = LOGDAC resolution in dB
- for AD7118: r = 1.5
- for AD7111: r = 0.375
- for AD7115: r = 0.1

N = Integer equivalent of digital input
- for AD7118: 0≤N≤59
- for AD7111: 0≤N≤239
- for AD7115: 0≤N≤199

V_{IN} = ac or dc input voltage (nominal range ±10V)

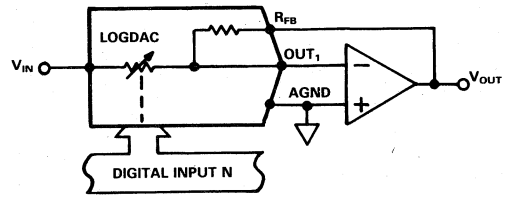


Figure 4. ANTILOG D/A Converter (Negative Exponent)

Features of the circuit of Figure 4 include:

1. It provides dB attenuation of V_{OUT} relative to V_{IN} as determined by the digital word N. (i.e., output range is 0dB to −dB)
2. The circuit provides % of *reading* resolution.
3. The analog input can be voltage or current, ac or dc, positive or negative polarity – i.e., the circuit is basically a CMOS multiplying DAC.

ANTILOG DAC (Exponential with Positive Exponent)

The circuit of Figure 5 is analogous to a multiplying DAC divider circuit. It provides signal gain of V_{OUT} relative to V_{IN} as determined by the equations:

$$V_{OUT} = -V_{IN}10^{+\left(\frac{rN}{20}\right)} \quad \text{EQN8}$$

and/or

$$V_{OUT} = -V_{IN}e^{+(0.11512rN)} \quad \text{EQN9}$$

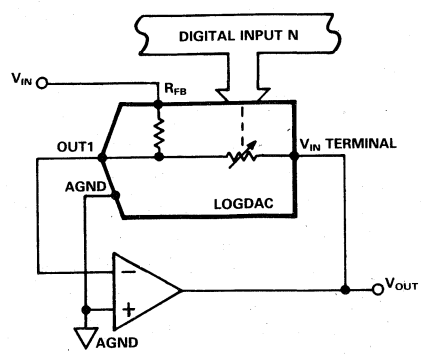


Figure 5. ANTILOG D/A Converter (Positive Exponent)

Basically, the analog input or reference voltage is applied to the on chip feedback resistor (RFB) and the amplifier output is connected to the V_{IN} terminal of the LOGDAC. The LOGDAC then ends up in the amplifier's feedback loop, thus the circuit provides *dB* gain of V_{OUT} relative to V_{IN} as determined by the digital input N (i.e., V_{OUT} range is 0dB to positive dB). As does the negative exponential DAC of Figure 4, this circuit provides % of *reading* resolution.

LOG OR LOG RATIO ADC

The circuit of Figure 6 provides an ADC function while performing a LOG compression. Its transfer function is:

$$N = \left(\frac{1}{-r}\right)\left(20\text{LOG}_{10}\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN10}$$

OR

$$N = \left(\frac{8.68659}{-r}\right)\left(\ln\left|\frac{-V_{IN}}{V_{REF}}\right|\right) \qquad \text{EQN11}$$

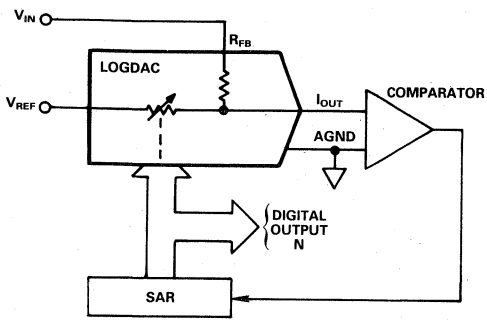


Figure 6. Log or Log Ratio A/D Converter

If the digital answer N (of EQN10) is multiplied by $-r$, the numerical value obtained is the dB value of the absolute value of V_{IN} relative to V_{REF} (answer 0dB to $-$dB).

If the digital answer N (of EQN11) is multiplied by $-r/8.68659$, the numerical value obtained is the natural log of the absolute value of V_{IN} relative to V_{REF}.

Circuit Constraints:

1. V_{IN} and V_{REF} must be of opposite polarity
2. $V_{IN} \leq |V_{REF}|$

CMOS D/A Converter Circuits for Single +5V Supplies

by Phil Burton

CMOS D/A converters can be used to provide analog outputs from microcomputers operating from a single +5V supply. They have the advantages of very low power consumption so that in many cases they can be added to an existing microcomputer without supplementing the existing +5V supply or adding additional supplies. This note covers the basic design techniques available for using three new CMOS D/A converters (AD7528, AD7545 and AD7548) with a single +5V supply and suggests methods for incorporating the circuits into microcomputers with minimal additional hardware.

CMOS D/A converters are normally operated in a current steering mode as shown in Figure 1. Current in the R-2R ladder is steered either to OUT1 or to AGND depending upon the state of the N-Channel switches. Since one of each pair of switches is always "on", the potential at the bottom of each 2R resistor leg and hence the current in each leg is constant and unaffected by the switch status.

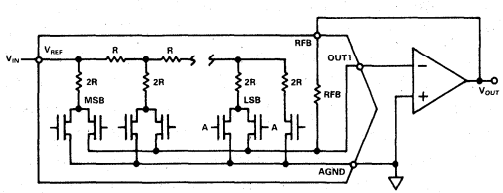


Figure 1. Basic Current Steering CMOS DAC Circuit

This holds true provided OUT1 and AGND are at the same voltage. In the conventional CMOS DAC circuit shown in Figure 1 OUT1 and AGND are held at the same potential by the external op-amp circuit. Due to the inverting configuration of the op amp the conventional current steering circuit of Figure 1 requires a negative reference voltage to generate positive outputs from the D/A converters. Methods of overcoming this constraint are given below.

VOLTAGE SWITCHING OPERATION

One way of obtaining single supply operation is to operate the CMOS DAC in the voltage switching mode as shown in Figure 2. The DAC connections have been essentially turned upside down—the reference voltage V_{IN} is applied to the OUT1 terminal, AGND is grounded and the V_{REF} terminal becomes the output. The RFB terminal

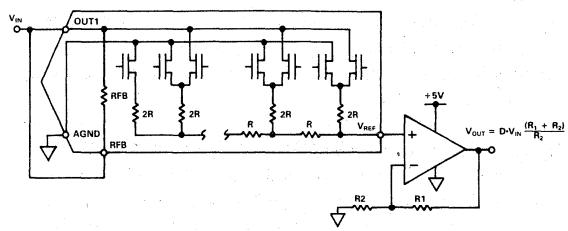


Figure 2. CMOS DAC Operated in Voltage Switching Mode

is not used and should be tied to OUT1 to prevent stray-pick-up. The N-Channel switches now select either V_{IN} or ground as the voltage to be supplied to the 2R resistor legs. Note that OUT1 and AGND are no longer at the same potential—this results in the N-Channel switch transistors getting different gate-source drive, which in turn changes the resistance of the NMOS transistor.

The device connected to AGND still receives a full +5V gate to source voltage (Vgs) when it is turned on, but the device connected to OUT1 has its Vgs reduced by the voltage at OUT1. The difference between the two Vgs voltages for an on device causes a difference in on-resistance which in turn can result in a deterioration of the DAC's linearity. As a rule of thumb, V_{IN} (i.e., the reference voltage applied to the OUT1 terminal) *should not exceed 0.7 volts when the CMOS DAC is operated from a +5V V_{DD} supply.* Values of V_{IN} greater than this value can cause DAC linearity problems.

Note that the input impedance of the D/A converter when operated in the voltage switching mode varies with the digital code, and consequently, the reference voltage V_{IN} should be supplied from a buffer op amp. The output impedance of the D/A converter when used in the voltage switching mode is constant and equal to R (typically 10kΩ). Figure 3 shows a complete dual 8-bit CMOS D/A converter circuit operated in the voltage switching mode. The DAC output voltage covers a range of 0 to 2.55V in 10mV steps. Total quiescent power consumption is approximately 10mW. The 1.2V AD589 bandgap reference is divided by 2 and buffered by op amp X1 to provide an ap-

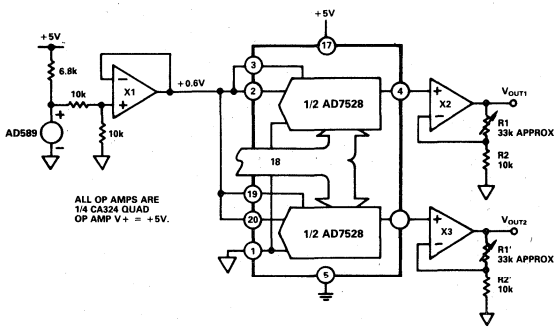


Figure 3. Dual DAC for Single +5V Supply

proximate 0.6 volt reference to the DAC. The outputs of the AD7528 dual D/A converter are buffered and amplified by amplifiers X2 and X3 to give the 0 to 2.55V output. Resistors R1 and R1′ are used to adjust full-scale outputs of the circuit.

SINGLE SUPPLY CURRENT SWITCHING OPERATION

An alternative method of obtaining single 5V supply operation of CMOS DACs is shown in Figure 4. This circuit uses the conventional current switching mode of operation but the AGND terminal is biased up to some positive reference voltage V_{IN}. The output op-amp bootstraps the OUT1 terminal to the same voltage as OUT2 and the V_{REF} terminal is connected to ground, so that V_{REF} is negative with respect to OUT1 and AGND by an amount equal to V_{IN}. For the circuit of Figure 4 the output voltage range is from

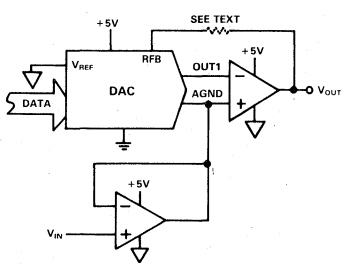


Figure 4. Current Steering Circuit for Single Supply Operation

$+V_{IN}$ for all zero's code to $+(2V_{IN} - 1LSB)$ for all 1's code. Although all the NMOS switches receive the same gate to source drive voltage, the value of Vgs is reduced by $(-V_{IN})$. Reduced gate drive can also cause linearity and gain errors and it is not recommended that V_{IN} exceeds 1 volt for a V_{DD} of +5 volts. Note that the current switching mode of operation retains the valuable bipolar multiplying capability of CMOS DACs. The reader is cautioned that the circuit of Figure 4 only operates with AD7528, AD7545 and AD7548 type devices. These CMOS DACs use a different internal circuit configuration which makes it possible to bias up AGND as shown. If other CMOS DACs are used in the circuit of Figure 4 there will be significant linearity errors (the AD7240 can also be used in this mode but it requires a V_{DD} of more than 7 volts).

The output range of Figure 4 circuit is restricted to going from $+V_{IN}$ to $(+2V_{IN} - 1LSB)$. To increase the voltage range (i.e., add gain) an additional resistor can be inserted in series with RFB as shown dotted in Figure 4, or alternatively the circuit of Figure 5 can be used. CMOS DACs have an absolute resistor temperature coefficient of about −300ppm/°C; as a result the simple expedient of increasing the output voltage range by inserting a resistor in series with RFB is only useful for operation over limited temperature excursions. The circuit of Figure 5 (reference 1) is an alternative solution which allows the output voltage range to be increased without causing severe component tempco mismatch problems. The output for all zero's code is fixed at V_{IN}, and the DAC gain is fixed by R1 and R2: R3 which is set equal to (R1,R2)/(R1 + R2), compensates for the temperature coefficient of R1 and R2.

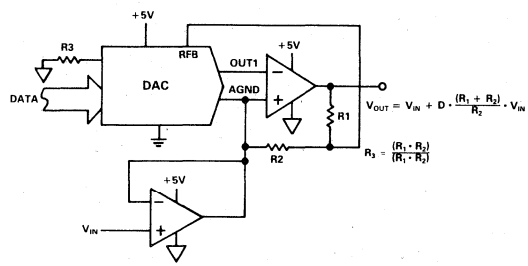


Figure 5. Single Supply Current Steering Circuit with Output Gain

CHOICE OF AMPLIFIER

Amplifier choice for +5V operation is critical. Relatively few op-amp designs can operate with +5V V_{CC} and a common mode voltage range which includes the negative supply—in this case ground. Suitable op amps for single +5V operation are CA324 and LM10 (both of which are bipolar type devices and have PNP type input stages), the CA3140 and CA3160 BIMOS op amps which have P-Channel MOS inputs and the TL091 JFET family which have N-Channel JFET inputs. The low input offset voltage of the bipolar op amps is a distinct advantage, particularly for +5V operation. On the other hand the BIMOS op amps tend to settle faster and their outputs can swing to both supply rails so that analog output can extend over the whole 0 to +5V supply range. The LM10 also includes a 200mV reference with amplifier which can be useful in some of the circuits discussed here. The JFETs usually provide the lowest noise.

Amplifier input offset voltage (V_{OS}) is important in single +5V CMOS DAC applications for two reasons; first, in current switching circuits V_{OS} causes OUT1 and AGND to be at different potentials so that the current in each 2R leg varies depending upon whether the 2R leg is connected to OUT1 or AGND. As a rule of thumb in current switching circuits the amplifier input offset voltage should not exceed 10% of the DAC's output voltage resolution in order to minimize effects on the DAC linearity. Second, the two single +5V supply circuits presented here (current switching and voltage switching) will both in general require some amplification of the DAC output, and the

amplifier input offset voltage will cause an output offset voltage. The output offset voltage will be equal to output amplifier gain x input offset voltage. For Figure 2 and Figure 5 circuits the contribution of V_{OS} to the output will be

$$\text{Output Offset Error} = V_{OS} \times \frac{(R_1 + R_2)}{R_2}$$

The output offset error of the circuit of Figure 3 is typically ±1LSb (10mV). Input offset error is easily trimmed out on single op amps since offset trim nodes are usually provided but for multiple op amps such as the CA324 no such nodes are available. Amplifier offset does not affect linearity in the voltage switching mode of operation.

The output stage of the amplifier determines the possible output range of the D/A converter. All of the amplifiers mentioned here have outputs which can go to ground in the unloaded condition. At the other end of the range the output of the CA324 and the TL091 is restricted to a maximum V_{OUT} of 3.5 volts while the LM10 and CA3140/60 can go almost to 5 volts. Figure 6 gives transfer characteristics for CA3160, TL091, CA324 and LM10 with different load conditions. It is particularly important to consider the circuit being driven by the output of the DAC amplifier because the amplifier's maximum and minimum output voltages may be constrained by the current sink or source capability of the op amp.

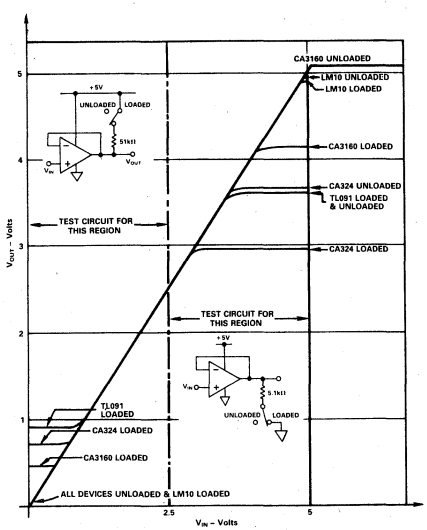


Figure 6. V_{OUT} vs. V_{IN} for Some Popular Op Amps

AN APPLICATION OF SINGLE +5V SUPPLY CMOS DACs

Figure 7 shows a simple stroke-writing X-Y plotter drive which demonstrates how the design methods described here can be used within a system. The X-Y plotter interface uses an interpolation scheme (reference 2) to draw straight lines between points defined by their X and Y coordinates. The microcomputer loads the X and Y coordinates for the start and finish points to the dual DAC's DAC1 and DAC2 which are operated in the voltage switching mode and a straight line between the points is drawn by linearly sweeping the reference inputs to the DAC's

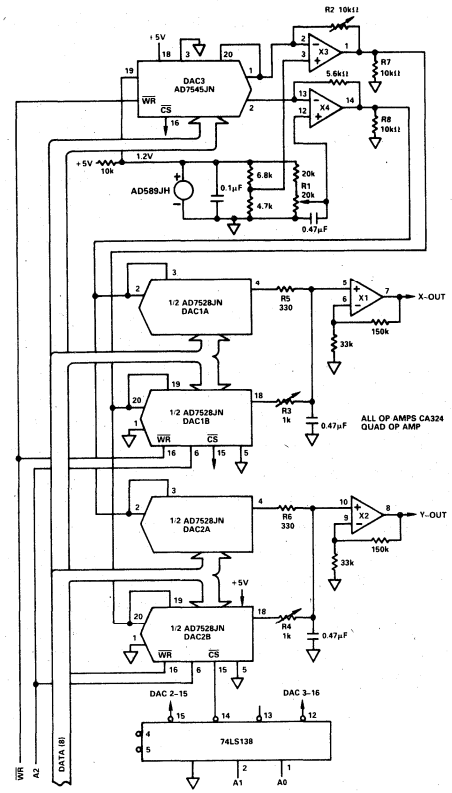


Figure 7. X-Y Plotter Interface Using +5V Supplies Only

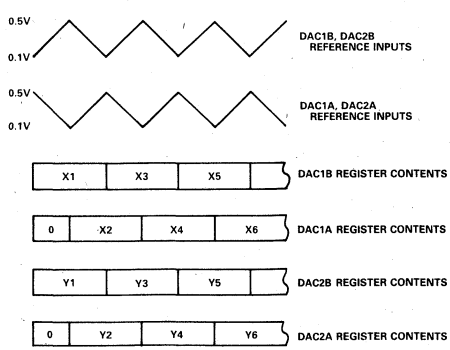


Figure 8. Triangle Waveforms and Related DAC Register Contents

with triangle waves. Figure 8 shows the phase relationship of the two triangle waves and the register contents for each of the four D/A converters. In the circuit shown here, the two triangle waveforms which are of equal amplitude but 180° out of phase, are generated by an additional D/A converter DAC3. The microcomputer uses an internal register to alternately count up and down between OOH to FFH. Every incremental count is loaded to DAC3. The output currents at the OUT1 and AGND terminals of DAC3 will have the required triangle waveform and phase relationship, and are converted into voltage waveforms by the current to voltage converters X3 and

X4. It will be observed that DAC3 is operated in the current switching mode with its two outputs OUT1 and AGND biased at about +0.5V and with a nominal V_{REF} of +1.2V. Each triangle waveform has exactly the same maximum and minimum values; R1 is used to compensate for amplifier offset mismatch and ensure that the maximum values of the triangle are the same (about 500mV) and R2, which sets the gain of one of the current to voltage converters, is used to trim the two minimum values to be the same (about 100mV).

The peak triangle value of approximately 500mV is determined by the maximum voltage that can be applied to DAC1 and DAC2 before linearity is degraded. The minimum value of 100mV is determined by the current sink capability of output amplifiers X3 and X4 which have to sink current from DAC1 and DAC2, and they must do this without any loss of linearity due to amplifier output impedance. Resistors R7 and R8 provide additional current sinking capability at the outputs of amplifiers X3 and X4 to assist the amplifier outputs to go down to +100mV. The outputs of each dual DAC are summed and amplified by the output amplifiers X1 and X2. Trim resistors R3 and R4 can be used to match the output impedances of the DAC pairs, although if AD7528LN DACs are used these are guaranteed to have their output impedances matched to within ±LSB and resistors R3, R4, R5 and R6 are then unnecessary. While the circuit in schematic form may look formidable, it in fact only uses five DIP packed ICs and a bandgap reference type AD589JH. Note that the AD7545 is a 12-bit wide DAC but in this application the four LSBs are strapped low.

INTERFACING SINGLE +5V DACs TO PROCESSORS

The three DACs discussed in this note (AD7528, AD7545 and AD7548) include on-board data latches with $\overline{CS}$ and $\overline{WR}$ pins. They are logic level and speed compatible with virtually all the popular microprocessors. Since DACs are in effect "write only memories" they can be connected so that they use the same address as existing ROMs provided the ROM outputs are gated to occur only on "READ" cycles. In practice this means that the same address decoder chip can often be used for ROM and for the DAC—the almost zero loading effect of the CMOS DAC $\overline{CS}$ input is an added advantage here, since it will not significantly add to the loading on the decoder output.

References

[1]A. P. Brokaw, *Input Resistor Stabilizes MDAC's Gain*, EDN Jan 7, 1981, pp210/211.
[2]P. Burton, *Generating Complex Waveforms & Vectors Using Multiplying D/A Converters*, Application Note available from Analog Devices, P.O. Box 280, Norwood, MA 02062.

ANALOG DEVICES

APPLICATION NOTE

Applications of High Performance BIFET Op Amps

By Don Travers

INTRODUCTION

Since the development of the monolithic operational amplifier each new operational amplifier that has come to market offers a unique set of performance advantages. As refinements to existing technologies and manufacturing processing techniques evolve the closer the total operational amplifier performance resembles that of an ideal amplifier. New techniques in BIFET operational amplifier processing have narrowed the gap between the practical and ideal amplifiers in the mutually exclusive characteristics of bandwidth and dc performance without sacrificing any other parameter. The improvement in overall performance simplifies many designs and reduces the cost of high accuracy applications.

The single BIFET operational amplifiers AD542, AD547 and the duals AD642, AD647 are recommended for any operational amplifier application requiring excellent dc performance at low cost. Precision instrument front ends requiring accurate amplification of millivolt level signals from megohm source impedances will benefit from the device's combination of low offset voltage and drift, low bias current, and low 1/F noise. The dual amplifiers, since they are closely matched, are ideal for true instrumentation amplifiers and log ratio amplifiers.

The single AD544 and dual AD644 operational amplifiers are recommended for any application requiring excellent ac and dc performance. The wide bandwidth, low offset voltage, and high open loop gain ensures superior accuracy in high impedance buffer and sample and hold applications. The AD644 with matched amplifiers can be used for true wideband instrumentation amplifiers, low dc drift active filters and output amplifiers for four quadrant multiplying D/A converters such as the AD7541, 12-bit CMOS DAC.

D/A CONVERTER APPLICATIONS

The BIFET series of operational amplifiers can be used with CMOS DACs to perform both 2-quadrant and 4-quadrant operation. The output impedance of a CMOS DAC varies with the digital word, thus changing the noise gain of the amplifier circuit. The effect will cause a nonlinearity the magnitude of which is dependent on the offset voltage of the amplifier. The BIFET series with trimmed offset will minimize this effect. Additionally, the Schottky protection diodes recommended for use with many older CMOS DACs are not required when using one of the BIFET series amplifiers.

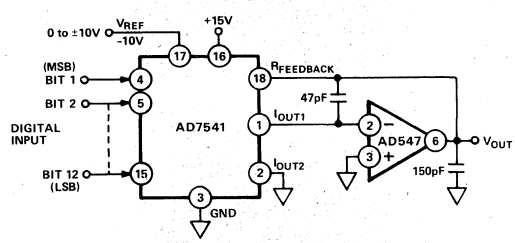


Figure 1a. AD547 Used as DAC Output Amplifier

Figure 1a shows the AD547 and AD7541 configured for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at pin 17, the circuit operates as a unipolar converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

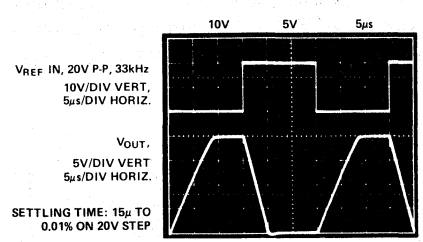


Figure 1b. Voltage Output DAC Settling Characteristic

The oscilloscope photo of Figure 1b shows the output of the circuit of Figure 1a. The upper trace represents the reference input, and the bottom trace shows the output voltage for a digital input of all ones on the DAC (Gain $1-2^{-n}$). The 47pF capacitor across the feedback resistor compensates for the DAC output capacitance, and the 150pF load capacitor serves to minimize output glitches.

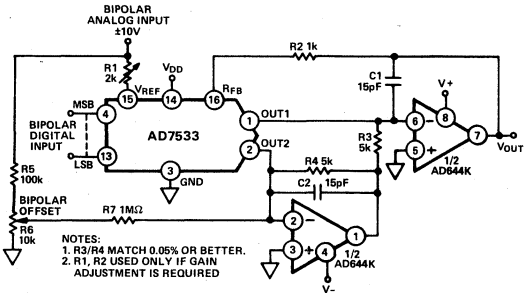


Figure 2a. AD644 Used as DAC Output Amplifiers

Figure 2a illustrates the 10-bit digital-to-analog converter, AD7533, connected for bipolar operation. Since the digital input can accept bipolar numbers and V_{REF} can accept a bipolar analog input, the circuit can perform a 4-quadrant multiplying function.

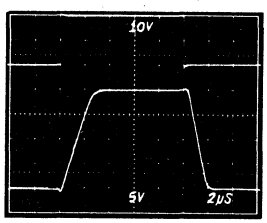


Figure 2b. Large Signal Response

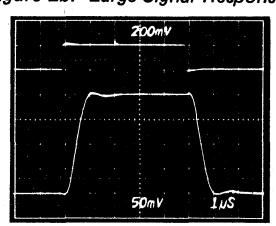


Figure 2c. Small Signal Response

The photos exhibit the response to a step input at V_{REF}. Figure 2b is the large signal response and Figure 2c is the small signal response. C1 phase compensation (15pF) is required for stability when using high speed amplifiers. C1 is used to cancel the pole formed by the DAC internal feedback resistance and the output capacitance of the DAC.

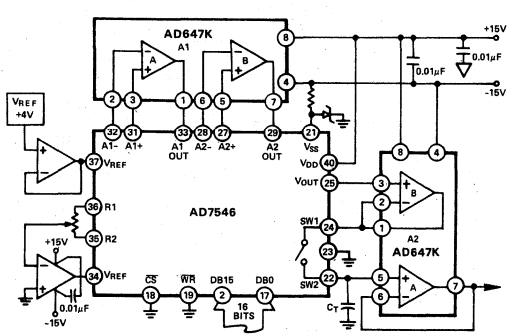


Figure 3. AD647 Used with AD7546 16-Bit DAC

Figure 3 shows the AD647 used with the AD7546 16-bit segment DAC. In this application, amplifier performance is critical to the overall performance of the AD7546. A1 is used as a dual precision buffer. Here the offset voltage match, low offset voltage and high open loop gain of the AD647 ensure monotonicity and high linearity over the entire operating temperature range. A2 serves a dual function: amplifier A is a Track and Hold circuit that deglitches the DAC output and amplifier B acts as an output amplifier. The performance of the amplifiers of A2 is crucial to the accuracy of the system. The errors of these amplifiers are added to the errors due strictly to DAC imperfections. For this reason great care should be used in the selection of these amplifiers. The matching characteristics, low bias current and low temperature coefficients of the AD647 make it ideal for this application.

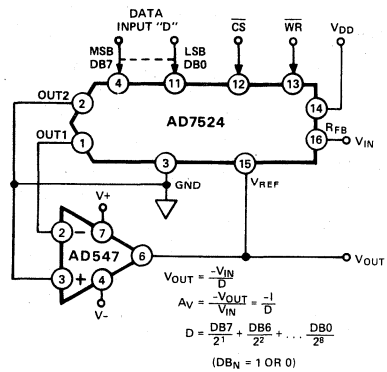


Figure 4. Digital Divider

If a CMOS DAC is connected in the feedback circuit around an op amp rather than at its input, it will act as a divider, the inverse of multiplication. Observe that the reduction of feedback causes amplifier noise and errors to be magnified at the higher gains. Since the incremental step changes of gain become increasingly large for small values of D, any errors in these gain steps are magnified correspondingly. To limit the gain at all zeros, to prevent the amplifier from "taking off", a large value of shunt feedback resistance, e.g., 22MΩ may be used.

In this state variable or universal filter configuration (Figure 5) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cut-off frequency, fc. DACs A2 and B2 must track accurately for the simple expression for fc to hold. This is readily accomplished by the AD7528. C3 compensates for the effects of op amp gain-bandwidth limitations.

The filter provides low pass, high pass and bandpass outputs and is ideally suited for applications where microprocessors control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is fc = 0 to 15kHz and Q = 0.3 to 4.5.

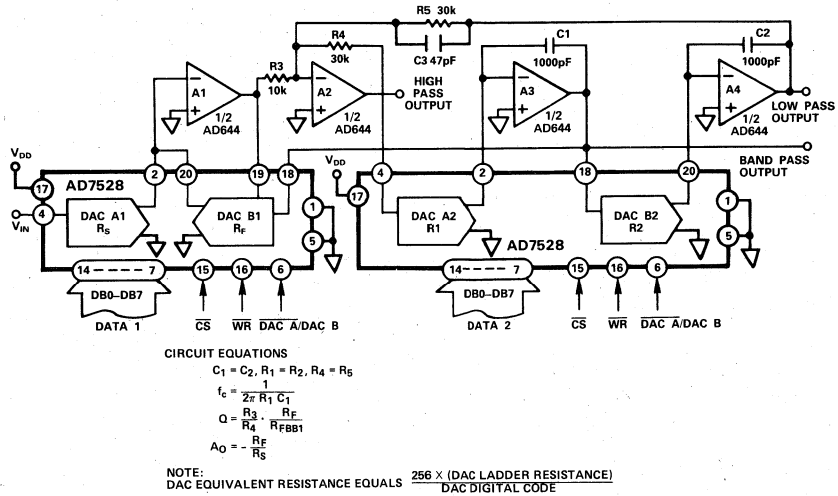


Figure 5. Digitally Controlled State Variable Filter

INSTUMENTATION AMPLIFIER

The circuit shown in Figure 6 uses the AD647 to construct an ultra high precision instrumentation amplifier. In this type of application the matching characteristics of a monolithic dual amplifier are crucial to ensure high performance.

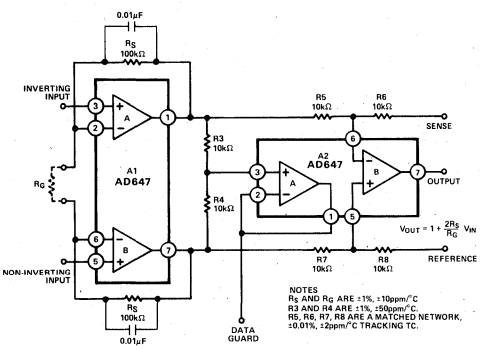


Figure 6. Precision FET Input Instrumentation Amplifier

The use of an AD647L as the input amplifier A1, guarantees maximum offset voltage of 250µV, drift of 2.5µV/°C and bias currents of 35pA. A2 serves two less critical functions in the amplifier and, therefore, can be an AD647J. Amplifier A is an active data guard which increases ac CMRR and minimizes extraneous signal pickup and leakage. Amplifier B is the output amplifier of the instrumentation amplifier. To attain the precision available from this

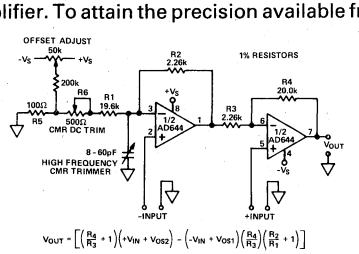


Figure 7. Wide Bandwidth Instrumentation Amplifier

configuration, a great deal of care should be taken when selecting the external components. CMRR will depend on the matching of resistors R5, R6, R7, and R8. The gain drift performance of this circuit will be affected by the matching TC of the resistors used.

The AD644 in the circuit of Figure 7 provides highly accurate signal conditioning with high frequency input signals. It provides an offset voltage drift of 10µV/°C, CMRR of 80dB over the range of dc to 10kHz and a bandwidth of 200kHz (−3dB) at 1V p-p output. The circuit of Figure 7 can be configured for a gain range of 2 to 1000 with a typical nonlinearity of 0.01% at a gain of 10.

LOG RATIO AMPLIFIER

Log amplifiers or log ratio amplifiers are useful in a wide range of analog computational applications, ranging from the simple linearization of exponential transducer outputs to the use of logarithms in computations involving multi-term products or arbitrary exponents. Log amps also facilitate the compression of wide ranging analog input signals into a range that can be easily handled using standard circuit techniques.

The picoamp level input current and low offset voltage of the AD647 make it suitable for wide dynamic range log

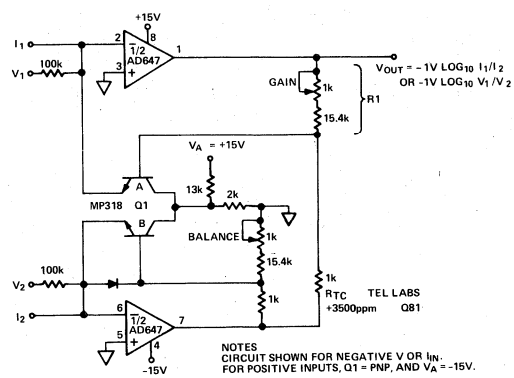


Figure 8. Log-Ratio Amplifier

amplifiers. Figure 8 is a schematic of a log ratio circuit employing the AD647 that can achieve less than 1% conformance error over 5 decades of current input, 1nA to 100μA. For voltage inputs, the dynamic range is typically 50mV to 10V for 1% error, limited on the low end by the amplifiers' input offset voltage.

The conversion between current (or voltage) input and log output is accomplished by the base-emitter junctions of the dual transistor Q1. Assuming Q1 has β>100, which is the case for the specified transistor, the base-emitter voltage on side 1 is to a close approximation:

$$V_{BE\,A} = kT/q \ln I_1/I_{S1}$$

This circuit is arranged to take the difference of the V_{BE}'s of Q1A and Q1B, thus producing an output voltage proportional to the log of the *ratio* of the inputs:

$$V_{OUT} = -K(V_{BE\,A} - V_{BE\,B}) = -\frac{KkT}{q}(\ln I_1/I_{S1} - \ln I_2/I_{S2})$$

$$V_{OUT} = -KkT/q \ln I_1/I_2$$

The scaling constant, K is set by R1 and R_{TC} to about 16, to produce a 1V change in output voltage per decade difference in input signals. R_{TC} is a special resistor with a +3500ppm/°C temperature coefficient, which makes K inversely proportional to temperature, compensating for the "T" in kT/q. The log-ratio transfer characteristic is, therefore, independent of temperature.

This particular log ratio circuit is free from the dynamic problems that plague many other log circuits. The −3dB bandwidth is 50kHz over the top 3 decades, 100nA to 100μA, and decreases smoothly at lower input levels. This circuit needs no additional frequency compensation for stable operation from input current sources, such as photodiodes, which may have 100pF of shunt capacitance. For larger input capacitances a 20pF integration capacitor around each amplifier will provide a smoother frequency response.

This log ratio amplifier can be readily adjusted for optimum accuracy by following this simple procedure. First, apply V1 = V2 = −10.00V and adjust "Balance" for V_{OUT} = 0.00V. Next apply V1 = −10.00V, V2 = −1.00V and adjust gain for V_{OUT} = +1.00V. Repeat this procedure until gain and balance readings are within 2mV of ideal values.

ACTIVE FILTER APPLICATIONS

Literature on active filter techniques and characteristics based on operational amplifiers is readily available. The successful application of an active filter, however, depends on the component selection to achieve the desired performance. The AD544 (and AD644 dual amplifier) is recommended for filters in medical, instrumentation, data acquisition and audio applications, because of its high gain bandwidth figure, symmetrical slewing, low noise, and low offset voltage.

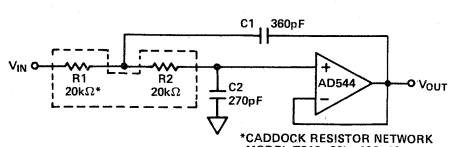


Figure 9. Second Order Low Pass Filter – f_{cp} = 20kHz

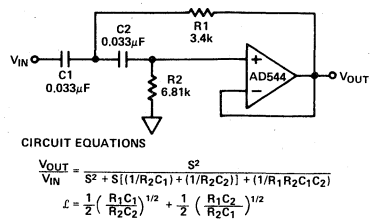


Figure 10. Second Order High Pass Filter – f_{cp} = 1kHz

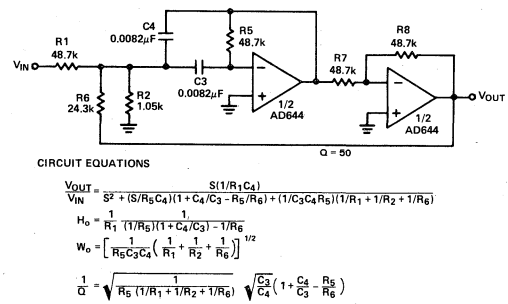


Figure 11. Multiple-Feedback Bandpass Circuit – f_o = 20kHz

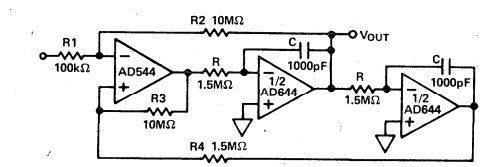


Figure 12. Bandpass State Variable Filter

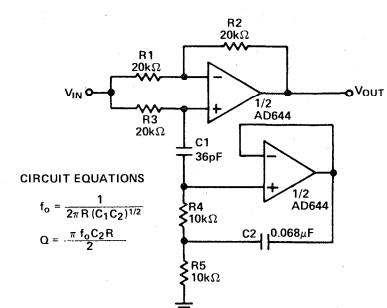


Figure 13. Notch Filter with an Active Inductive f_o = 10kHz

SENSOR INTERFACE

The BIFET series is guaranteed for a maximum safe input potential equal to the power supply potential. The input stage design also allows differential input voltages of up to ±1 volt while maintaining the full differential input resistance of $10^{12}\Omega$. This makes the BIFET series suitable for comparator situations employing a direct connection to high impedance source.

Many instrumentation situations, such as flame detectors in gas chromatographs, involve measurement of low level currents from high-voltage sources. In such applications, a sensor fault condition may apply a very high potential to the input of the current-to-voltage converting amplifier. This possibility necessitates some form of input protection. Many electrometer type devices, especially CMOS designs, can require elaborate zener protection schemes which often compromise overall performance. The BIFET series requires input protection only if the source is not current-limited, and as such is similar to many JFET-input designs. The failure mode would be overheating from excess current rather than voltage breakdown. If the source is not current-limited, all that is required is a resistor in series with the affected input terminal so that the maximum overload current is 1.0mA (for example, 100kΩ for a 100 volt overload). This simple scheme will cause no significant reduction in performance and give complete overload protection. Figure 14 shows proper connections.

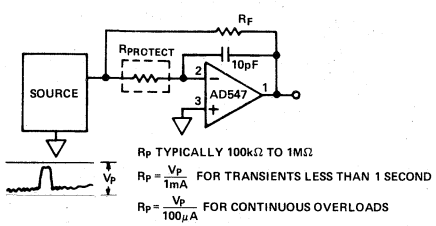


Figure 14. Input Protection

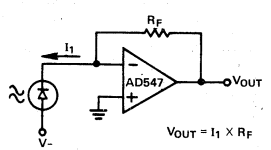


Figure 15. Photodiode Amplifier — Photoresistive Mode

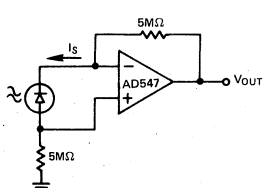


Figure 16. Photodiode Amplifier — Photovoltage Mode

To obtain higher sensitivity in current to voltage converters it is simple to use a higher value of feedback resistor. However, high value resistors above $10^9\Omega$ tend to be expensive, large, noisy and unstable. To avoid this, it may be desirable to use a circuit configuration with output gain, as in Figure 17. The drawback is that input errors of offset voltage drift and noise are multiplied by the same gain, but the precision performance of the AD547 makes the tradeoff easier.

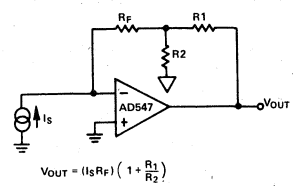


Figure 17. Current to Voltage Conversion with Gain

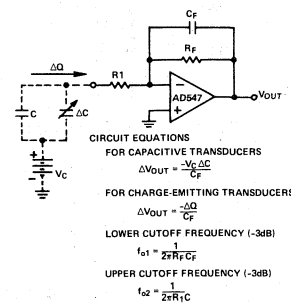


Figure 18. Charge-Sensitive Amplifier

High-impedance transducers such as proportional counters and some accelerometers require an amplifier which converts a transfer of change into a change of voltage. The voltage across the transducer in many cases is held constant. Since the potential remains constant then only the capacitance of the transducer changes by dc or a change of ΔQ is emitted from the transducer. The equation relating the two are $\Delta Q = V_C \Delta C$.

One of the problems with low-level leakage current testing or low-level current transducers (such as Clark oxygen sensors) is finding a way to apply voltage bias to the device while still grounding the device and the bias source. Figure 19 shows a technique in which the desired bias is applied at the noninverting terminal thus forcing that voltage at the inverting terminal. The current is sensed by R_F, and the AD524 instrumentation amplifier converts the floating differential signal to a single-ended output.

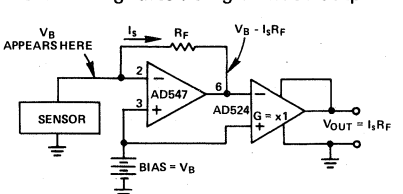


Figure 19. Current-to-Voltage Converters with Grounded Bias and Sensor

SAMPLE AND HOLD APPLICATIONS

The sample and hold circuit, shown in Figure 20 is suitable for use with 8-bit A/D converters. The acquisition time using a 3900pF capacitor and fast CMOS SPST (ADG200) switch is 15μs.

The droop rate is very low 25×10^{-9} V/μs due to the low input bias currents of the AD644. Care should be taken to minimize leakage paths. Leakages around the hold capacitor will increase the droop rate and degrade performance.

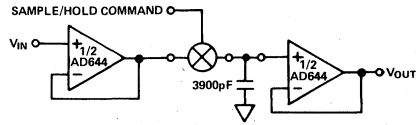


Figure 20. Sample and Hold Circuit

BIFET Applications

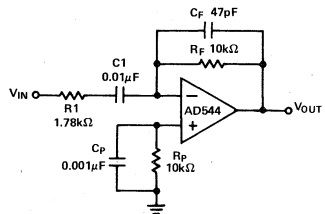


Figure 21. Differentiator

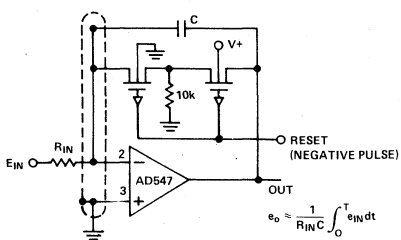


Figure 22. Low Drift Integrator and Low-Leakage Guarded Reset

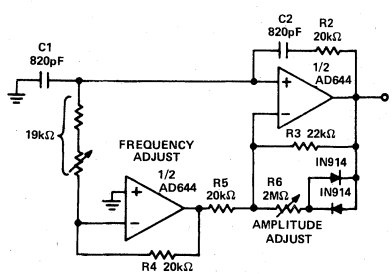


Figure 23. Wien-Bridge Oscillator — f_O = 10kHz

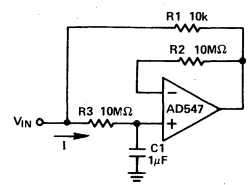


Figure 24. Capacitance Multiplier

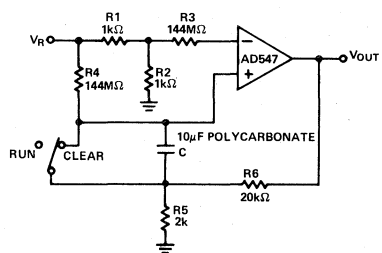


Figure 25. Long Interval Timer — 1,000 Seconds

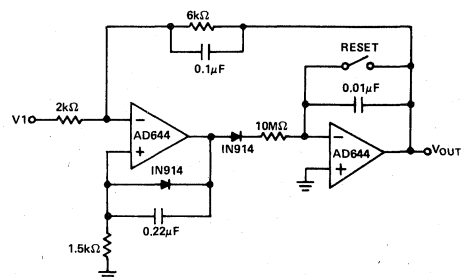
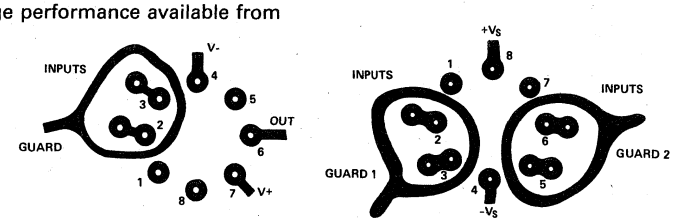


Figure 26. Positive Peak Detector

GUARDING

The low input bias current (25pA) and low noise characteristics of the high performance BIFET op amp make it suitable for electrometer applications such as photo diode preamplifiers and picoampere current-to-voltage converters. The use of guarding techniques in printed circuit board layout and construction is critical for achieving the ultimate in low leakage performance available from these amplifiers. The input guarding scheme shown in Figure 27 will minimize leakage as much as possible; the guard ring is connected to a low impedance potential at the same level as the inputs. High impedance signal lines should not be extended for any unnecessary length on a printed circuit.



Single Versions *Dual Versions*

Figure 27. Board Layout for Guarding Inputs

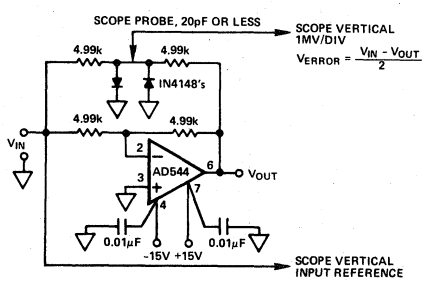


Figure 28. Settling Time Test Circuit

The fast settling time, low bias current and low offset voltage of the AD544 make it an excellent choice as an output amplifier for current output D/A converters.

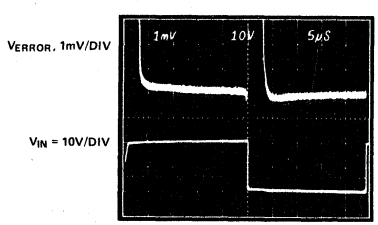


Figure 29. Settling Characteristic Detail

The upper trace of the oscilloscope photograph of Figure 29 shows the settling characteristic of the AD544. The lower trace represents the input to Figure 28. The AD544 has been designed for fast settling to 0.01%, however, feedback components, circuit layout and circuit design must be carefully considered to obtain the optimum settling time.

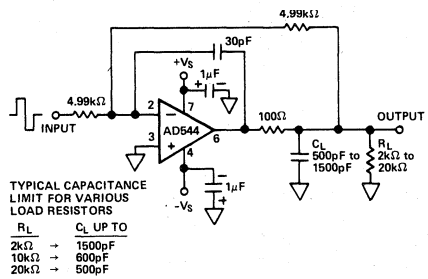


Figure 30. Circuit for Driving a Large Capacitance Load

The circuit in Figure 30 employs a 100Ω isolation resistor which enables the amplifier to drive capacitance loads exceeding 500pF; the resistor effectively isolates the high frequency feedback from the load and stabilizes the circuit. Low frequency feedback is returned to the amplifier summing junction via the low pass filter formed by the 100Ω series resistor and the load capacitance, C_L.

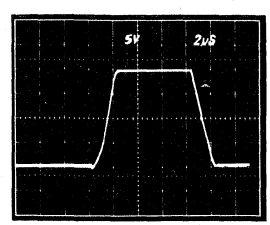


Figure 31. Transient Response R_L = 2kΩ C_L = 500pF

GENERAL PURPOSE FET INPUT SPECIFICATIONS (typical @ $V_S = \pm 15V$, $T_A = +25°C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/μs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ μV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD503J	20k	10/5	1.0	3.0	50	75	15	70	C	H
AD503K	50k	10/5	1.0	3.0	20	25	10	80	C	H
AD503S	50k	10/5	1.0	3.0	20	50	10	80	M	H
AD506J	20k	10/5	1.0	3.0	3.5	75	15	70	C	H
AD506K	50k	10/5	1.0	3.0	1.5	25	10	80	C	H
AD506L	75k	10/5	1.0	3.0	1.0	10	5	80	C	H
AD506S	50k	10/5	1.0	3.0	1.5	50	10	80	M	H
AD528J	25k	10/5	10	50	3	50	30	70	C	H
AD528K	50k	10/5	10	50	1	25	15	80	C	H
AD528S	50k	10/5	10	50	1	25	15	80	M	H
AD540J	20k	10/5	1.0	6.0	50	75	50	70	C	H
AD540K	50k	10/5	1.0	6.0	20	25	25	70	C	H
AD540S	50k	10/5	1.0	6.0	20	50	25	70	M	H
AD542J	100k	10/5	1.0	3.0	2.0	20	50	76	C	H
AD542K	300k	10/5	1.0	3.0	1.0	10	25	80	C	H
AD542L	300k	10/5	1.0	3.0	0.5	5	25	80	C	H
AD542S	300k	10/5	1.0	3.0	1.0	15	25	80	M	H
AD544J	30k	10/5	2.0	13	2.0	20	50	74	C	H
AD544K	50k	10/5	2.0	13	1.0	10	25	80	C	H
AD544L	50k	10/5	2.0	13	0.5	5	25	80	C	H
AD544S	50k	10/5	2.0	13	1.0	15	25	80	M	H
AD547J	100k	10/5	1.0	3.0	1.0	5	50	76	C	H
AD547K	250k	10/5	1.0	3.0	0.5	2	25	80	C	H
AD547L	250k	10/5	1.0	3.0	0.25	1	25	80	C	H
AD547S	250k	10/5	1.0	3.0	0.5	5	25	80	M	H
AD642J	100k	10/5	1.0	3.0	2.0[3]	3.5mV[4]	75	76	C	H
AD642K	300k	10/5	1.0	3.0	1.0[3]	2.0mV[4]	35	80	C	H
AD642L	300k	10/5	1.0	3.0	0.5[3]	1.0mV[4]	35	80	C	H
AD642S	300k	10/5	1.0	3.0	1.0[3]	3.5mV[4]	35	80	M	H
AD644J	30k	10/5	2.0	13	2.0[3]	3.5mV[4]	75	76	C	H
AD644K	50k	10/5	2.0	13	1.0[3]	2.0mV[4]	35	80	C	H
AD644L	50k	10/5	2.0	13	0.5[3]	1.0mV[4]	35	80	C	H
AD644S	50k	10/5	2.0	13	1.0[3]	3.5mV[4]	35	80	M	H
AD647J	100k	10/5	1.0	3.0	1.0[3]	10	50	76	C	H
AD647K	250k	10/5	1.0	3.0	0.5[3]	5	25	80	C	H
AD647L	250k	10/5	1.0	3.0	0.25[3]	2	25	80	C	H
AD647S	250k	10/5	1.0	3.0	0.5[3]	5	25	80	M	H

[1] C = 0 to +70°C; M = −55°C to +125°C
[2] H = TO-99 can
[3] Dual amplifiers with matched side to side offset voltage
[4] Guaranteed max offset error from T_{min} to T_{max}

HIGH ACCURACY LOW BIAS CURRENT SPECIFICATIONS (typical @ $V_S = \pm 15V$, $T_A = +25°C$ unless otherwise noted)

Model	Gain min	Output V/mA min	Unity Gain MHz	Slew Rate V/μs	V_{OS} mV max	$\Delta V_{OS}/\Delta T$ μV/°C max	I_b pA max	CMR dB min	Temp Range[1]	Package[2]
AD515J	20k	10/5	0.35	0.3	3.0	50	0.300	66	C	H
AD515K	40k	10/5	0.35	0.3	1.0	15	0.150	80	C	H
AD515L	25k	10/5	0.35	0.3	1.0	25	0.075	70	C	H
AD523J	20k	10/5	0.5	5.0	50	90	1.0	70	C	H
AD523K	40k	10/5	0.5	5.0	20	30	0.5	80	C	H
AD523L	40k	10/5	0.5	5.0	20	60	0.25	80	C	H
AD545J	20k	10/5	0.7	1.0	1.0	25	2	66	C	H
AD545K	40k	10/5	0.7	1.0	1.0	15	1	70	C	H
AD545L	40k	10/5	0.7	1.0	0.5	5	1	76	C	H
AD545M	40k	10/5	0.7	1.0	0.25	3	1	76	C	H

[1] C = 0 to +70°C
[2] H = TO-99 can

UNDERSTANDING INTERFERENCE-TYPE NOISE

How to Deal with Noise without Black Magic

There Are Rational Explanations for—and Solutions to—Noise Problems

by Alan Rich

If the circuit doesn't work, add a decoupling capacitor anywhere—a 0.01μF ceramic disc, of course; they'll fix anything! Or when your circuit is broadcasting its noise, a shield will cure it; just wrap a piece of metal around the circuit, connect that shield to "ground," and watch the noise disappear!

Unfortunately, Nature is not that kind to us in real life. That 0.01μF disc you added only increased the noise; and the shield you added was totally ineffective—or, worse yet, the noise reappeared in a remote part of the circuit.

This article is the first of a two-part series to help you understand and deal effectively with interference noise in electronic systems. We will consider here the mechanism that causes noise to be picked up, since the first step in solving any noise problem is to identify the source of the noise and the coupling mechanism; only then can an effective solution be implemented.

The second article will suggest specific techniques and guidelines for effective shielding against electrostatic and magnetically coupled noise.*

WHAT KIND OF NOISE ARE WE TALKING ABOUT?

Any electronic system contains many sources of noise. Three basic forms in which it appears are: *transmitted noise*, received with the original signal and indistinguishable from it, *intrinsic noise*, (such as thermally generated Johnson noise, shot noise, and popcorn noise) originating within the devices that constitute a circuit, and *interference noise*, picked up from outside the circuit. This last may either be due to natural disturbances (e.g., lightning) or be coupled in from other electrical apparatus in the system or its vicinity, for example computers, switching power supplies, SCR controlled heaters, radio transmitters, switch contacts, etc.

This article will consider only the last category, man-made noise, the most pervasive form of system noise in data-acquisition or test systems. Although it is most annoying in low-level circuits, no part of the system is immune to it. But it is the only form of noise that can be influenced by choices of wiring and shielding.

ASSUMPTIONS AND ANALYTICAL TOOLS

Although Maxwell's equations—with all the mathematical agony that they imply—are necessary for a complete and accurate description of how electrical systems behave, conventional circuit analysis is a useful tool in most cases. The assumptions that permit circuit analysis to be valid in solving these problems are:

1. All electric fields are confined to the interior of capacitors.
2. All magnetic fields are confined to the immediate vicinity of inductors.
3. Dimensions of the circuits are small compared to the wavelengths under consideration.

*Another helpful and relevant article that appeared in these pages was "Analog Signal Handling for High Speed and Accuracy," by A. Paul Brokaw, *Analog Dialogue* 11-2, 1977, pp. 10-16.

Using these assumptions, we can model noise-coupling channels as lumped circuit elements. A magnetic field coupling two conductors is modeled as a mutual inductance. Stray capacitance can be modeled as two conductors with an electric field between them. Figure 1 shows an equivalent circuit of a situation where two short wires are adjacent to one another over a system ground.

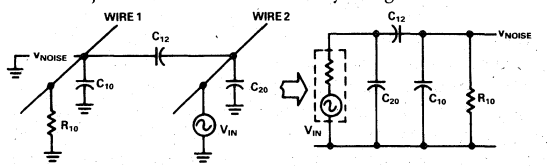


Figure 1. Noise-equivalent circuit of two adjacent wires and a ground plane.

Once the complete noise equivalent-circuit is obtained for a system, the problem becomes one of solving network equations for a desired parameter. All standard linear circuit analysis techniques can be applied, including node equations, loop equations, matrix algebra, state variables, superposition, Laplace transforms, etc. When circuits exceed 5 or 6 nodes, manual calculation becomes difficult; at this point, computer-aided programs, such as SPICE, and other CAD techniques become necessary. Experienced designers can make appropriate simplifying assumptions; but their validity should always remain in question until proven.

The lumped-element approach will not always give an accurate numerical answer, but it will show clearly how noise depends on system parameters. Just the act of drawing a reasonably faithful equivalent circuit may offer clues to methods to reduce noise levels. Once network equations or CAD programs are written, the quantitative effects of noise-suppression techniques can be studied.

In spite of all the modern technical advances, such as microprocessors and switching power supplies, wires still have resistance and inductance, capacitance still exists in the real world, and such phenomena must be reckoned with.

THE BASIC PRINCIPLE

There are always three elements involved in a noise problem: a *noise source* (line transients, relays, magnetic fields, etc.), a *coupling medium* (capacitance, mutual inductance, wire), and a *receiver*, a circuit that is susceptible to the noise (Figure 2).

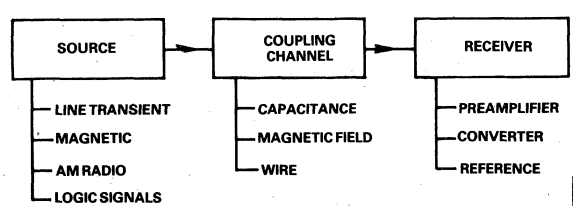


Figure 2. Noise pickup always involves a source, a coupling medium, and a receiver.

To solve the problem, one or more of these three elements must be removed, reduced, or diverted. Their role in the problem must be thoroughly understood before the problem can be solved. If the

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solution is inappropriate, it may only make the noise problem worse! Different noise problems require different solutions; adding a capacitor or a shield will not solve every such problem.

TYPES OF SYSTEM NOISE

Noise in any electronic system can originate at a large number of sources, including computers, fans, power supplies, adjacent equipment, test devices; noise sources can even include improperly connected shields and ground wires that were intended to combat noise. Our discussion of noise sources and coupling mechanisms will include the following topics:

Common-impedance noise
Capacitively coupled noise
Magnetically coupled noise
Power-line transients
Miscellaneous noise sources

Common-Impedance Noise. As the name implies, common-impedance noise is developed by an impedance that is common to several circuits. Figure 3 shows the basic configuration, which might occur when a pulse output source and an op amp's reference terminal are both connected to a "ground" point having tangible impedance to the power-supply return terminal. The noise current (the noisy return current of Circuit 1) will develop across impedance, Z, a voltage, V_{noise}, which will appear as a noise signal to Circuit 2.

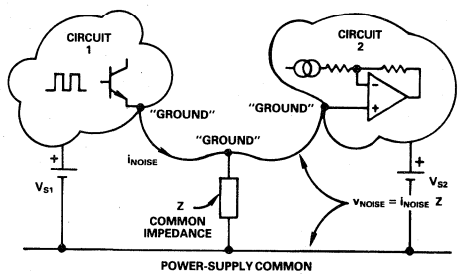


Figure 3. How noise is developed by a common circuit impedance.

Typically, this type of noise has a repetition rate that is set by the rate of the noise source. The actual waveshape is determined by the characteristics of the impedance, Z. For example, if Z is purely resistive, the noise voltage will be proportional to the noise current and of similar shape (Figure 4a). If Z is an R-L-C, the noise voltage will ring at a frequency, $1/(2\pi\sqrt{LC})$ and decay exponentially at a rate set by L/R (b).

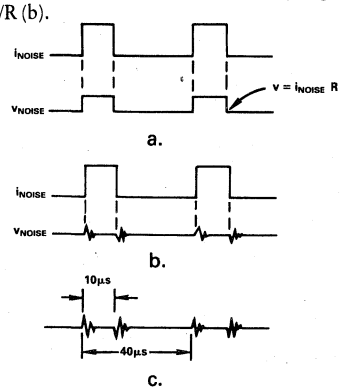


Figure 4. Noise effects in a common impedance. (a) Resistance. (b) An R-L-C circuit. (c) Switching-supply noise response.

If noise of this kind is found in a circuit, its origin may be readily deduced from the repetition rate and waveshape. The *repetition rate* will point to the source of noise, since the noise and its source are synchronized. For example, a noise waveform like that shown in (c), at a 25kHz repetition rate and a 25% duty cycle, might be typical of a switching power supply containing a regulating loop using pulse-width modulation.

The *waveform* will help identify the impedance that is actually generating the undesired noise. If, for example, the waveform of the noise is the simple damped sinusoid shown in Figure 5, the following features allow us to deduce the nature of Z:

•A constant resistance, R, is in series with the line. The voltage change, V_1, is the product of R and a current step, I_1.

•The natural frequency of the oscillation, f_1, is determined by the series L and shunt C, $f = 1/(2\pi\sqrt{LC})$.

•The damping time constant, τ, is determined by L/R.

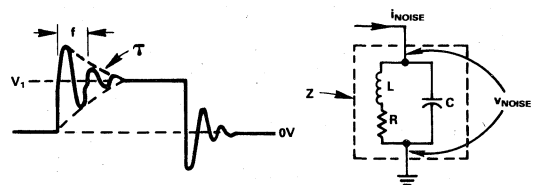


Figure 5 Waveshape for an underdamped R-L-C circuit.

Capacitively Coupled Noise. Noise is also produced by capacitive coupling from a noise source to another circuit. This type of noise is often seen when signals with fast rise-and-fall times or high frequency content are in close proximity to high-impedance circuits. Stray capacitance couples the fast edges of the signal into adjacent circuits, as the circuit model of Figure 6 shows. The nature of the impedance, Z, determines the shape of the response. Typical capacitances are listed in Table 1.

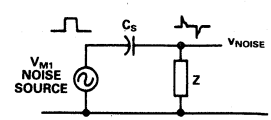


Figure 6. Stray capacitance couples noise into high-impedance circuits.

Table 1. Typical capacitances.[1]

Condition	Capacitance
Human standing on an insulator to earth	700 pF
Power input (ac) to output (dc) of ± 15-V dc supply	100 pF
Two-conductor shielded cable:	
Conductor to conductor	40 pF/ft
Conductor to shield	65 pF/ft
RG58 coaxial cable, center conductor to shield	33 pF/ft
Connector, pin to pin	2 pF
Optical isolator, LED to photodetector	2 pF
½-watt resistor (end to end)	1.5 pF

Capacitive pickup can occur in many ways, shapes, and sizes. Here are a few examples:

•A TTL digital signal produces fast edges, with a typical rise time of 10 nanoseconds and voltage swings of 5 volts. If Z is a 1-megohm resistor, even 0.1pF will produce 5-volt spikes with decay time constants of 100 nanoseconds.

[1]Sources: Excerpts from Ralph Morrison, *Grounding and Shielding Techniques in Instrumentation*, Second Edition (New York: John Wiley & Sons, 1977), p.30, and actual measurements.

•Crosstalk may result between two adjacent wires. For example, if two wires in a 10-foot (3-meter) length of cable have a capacitance of 40 pF/ft, the total capacitance is 400 pF. If a test voltage of 10 V at 1 kHz is on one conductor, 250 mV at 1 kHz will be coupled into the adjacent wire if Z is a 10 k resistance.

•Noise on the ac power line, developed through common impedances, will couple into other circuits. A common case is when transients couple through the interwinding capacitance of power-supply transformers.

It is amazing how little capacitance can cause serious problems. For example, consider the situation where high noise-immunity CMOS logic is used in an industrial circuit where 2500-volt, 1.5 MHz noise transients (IEEE Standard 472-1974) are present. Suppose that stray capacitance of only 0.1 pF exists between a CMOS input and the noise source, as shown in Figure 7. The calculated noise voltage, V_c, will be 2.4 volts, steady state, with an initial 50-V transient, which will cause improper logic operation or worse!

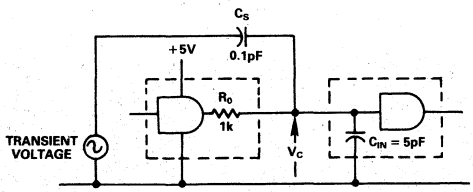


Figure 7. Coupling of high-voltage transients from test generator to logic.

Magnetically Coupled Noise. Strong magnetic fields are found where cables carry current, where ac power is distributed, and near machinery, power transformers, fans, etc. There is an analogous relationship between circuits coupled magnetically and those coupled capacitively, as shown in Figure 8 and Table 2.

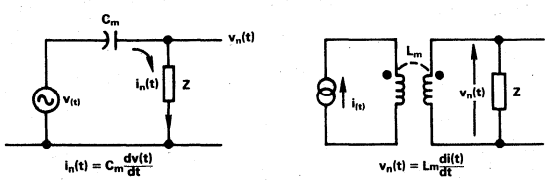


Figure 8. Comparison of magnetic and capacitive noise coupling.

Table 2. Characteristics of capacitive and magnetic coupling.

	Capacitive Coupling	Magnetic Coupling
Noise Source	Voltage change (dV/dt)	Current change (dI/dt)
Coupling Medium	Mutual capacitance	Mutual inductance
Coupled Noise	Current (frequently converted to voltage by Z)	Voltage

This analogy helps us consider some differences between capacitively and magnetically coupled noise:

•When the noise is magnetically coupled, voltage noise (V_n) appears in series with the receiver circuit; in the capacitive situation, the voltage noise produced between the receiver and ground is the voltage in Z caused by the noise current, i_n.

•Reducing the receiver impedance, Z, will reduce capacitively coupled noise. This is not the case in magnetically coupled circuits; lowering Z will not dramatically reduce voltage noise.

The voltage, V_n, induced in a closed loop (single turn) by a magnetic field is given by

$$V_n = 2\pi f B A \cos\theta \times 10^{-8} \quad (1)$$

volts, where f is the frequency of the sinusoidally varying flux density, B is the rms value of the flux density (gauss), A is the area of the closed loop (cm^2), and θ is the angle of B to area A.

For example, consider the circuit of Figure 9. It shows the calculation for two one-foot conductors, separated by 1 inch, in a 10-gauss 60-Hz magnetic field (typical of fans, power wiring, transformers). The maximum voltage induced in the wires is 3 mV.

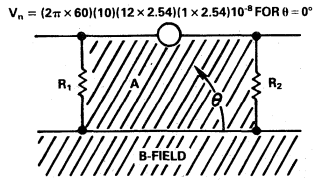


Figure 9. Example demonstrating magnitude of magnetic pickup.

The equation tells us that the noise voltage can be reduced by reducing B, A, or cosθ. The *B term* can be reduced by increasing the distance from the source of the field or—if the field is caused by currents flowing through nearby pairs of wires—twisting those wires to reduce the net field to zero by alternating its direction.

The loop area, A, can be reduced by placing the conductors closer together. For example, if the conductors in the example were placed 0.1″ apart (separated only by insulation), the noise voltage would be reduced to 0.3mV. If they can be twisted together, the area is, in effect, reduced to small positive and negative increments that cancel, practically nullifying the magnetic pickup.

The cos θ term can be reduced by proper orientation of the receiving wires to the field. For example, if the conductors were perpendicular to the field, the pickup would be minimized, while if they were run together in the same cable (θ = 0), pickup would be maximized.

The rms induced voltage, V_n, in a conductor in parallel with a second conductor, carrying a current I_2 at an angular frequency $\omega = 2\pi f$, with a given mutual inductance, M, is

$$V_n = \omega M I_2 \quad (2)$$

The application of this relationship shown in Figure 10 illustrates why only one end of a shield should be grounded. A 100-ft length of shielded cable is used to carry a high-level low-impedance signal

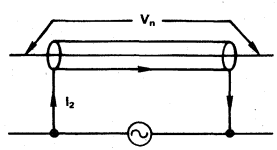


Figure 10. Magnetic pickup from current flowing through a cable shield.

(10V) to a 12-bit data-acquisition system (1 LSB = 2.4 mV). The shield, which has series resistance of 0.01 ohms per foot and mutual inductance to the conductor of 0.6μH/ft, has been grounded at both the source and the destination. A potential of 1 volt at 60 Hz exists between the two ground points, causing a current of 1 ampere to flow in the 1-ohm total resistance of the shield. By (2), the noise voltage induced in the conductor is

$$V_n = (2\pi\,60\,\text{Hz})(100 \times 0.6 \times 10^{-6}\,\text{H})(1\,\text{A}) = 23\,\text{mV},$$

or 10 LSBs, thereby reducing the effective resolution of the system to less than 9 bits. This noise voltage is a direct consequence of the large current flowing in the shield because it is grounded at both ends. And the 1-volt potential assumed between the grounds was conservative! In heavy-industry environments, 10 to 50 volts between earth grounds is not uncommon.

Power-Line Transients. Another type of system noise is that generated by high-voltage transients in inductive circuits, such as relays, solenoids, and motors, when they are turned on and off. When devices having high self-inductance are turned off, the collapsing fields can generate transients of the order of kilovolts, with frequencies from 0.1 to 3 megahertz, that appear on the power line.

Besides creating noise in sensitive circuitry, via capacitive and conductive coupling and radiated energy, these transients are hazardous to equipment and people. Standards exist to characterize certain transient waveforms for the purpose of protection; however, besides being designed to withstand them, systems should also be designed to deal with their potential interference with signals. Figure 11 shows 4 typical waveforms existing in industry standards.

Miscellaneous Noise Sources Finally, there is a group of noise sources that can be considered as miscellaneous—or just "flakey."

For low-level signals at high impedance, the cable itself can become a noise source. A charge can be produced on the dielectric material within the cable; if the dielectric does not maintain contact with the conductors, this charge will act as a noise source within the cable, unless the cable can be kept rigid. This noise is highly dependent on any motion of the cable; noise levels of 5 to 100 mV were reported by Belden Corporation. Noise of similar character (5 to 25 mV) was observed in the laboratory for RG188 coaxial cable, as it was moved and flexed.

Another type of motion-related noise occurs when a cable is moved through a magnetic field. Voltage will be induced in the cable as the cable cuts fixed flux lines or the flux density, B, changes. This kind of noise is troublesome in a high-vibration environment, where the cables can be in rapid motion. If the cable can be kept from vibrating relative to the field, this noise will not occur.

Finally, if instrumentation is operating in close proximity to a radio or television station, signals may be picked up from the transmissions. In addition to AM, FM, and television transmitters, the RFI may come from CB radios, amateur radios, walkie-talkies, paging systems, etc. High-frequency noise should be considered as a possible source of mysterious drifts in dc circuitry, due to rectification of picked-up rf; investigations of drift should always be conducted with a wideband oscilloscope.

SUMMARY

We have described here the different types of interference noise that will exist in any electronic system. Table 3 lists the noise sources discussed above and some effective approaches to solving the pickup problem. It is important to understand the complete noise system (source, coupling medium, receiver, and relationships) before noise-reduction techniques are employed.

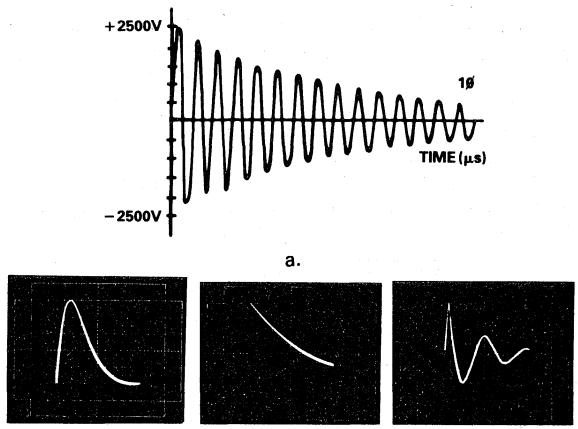
Noise reduction is not a mystical job for wizards; it is a practical and analytical job for engineers. Needless to say, the most effective approach is *prevention*—applying noise-reduction analysis and minimization techniques *before the system is built.*

In part 2 of this article, we will describe the proper application of shielding and guarding techniques for noise reduction.

Further Reading:

Ralph Morrison, *op. cit.*

Henry W. Ott, *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley & Sons, 1976).



Courtesy of Key Tek Instrument Corp., Burlington, MA

Figure 11. Examples of transients existing in standards for industrial power-line equipment. (a) IEEE Standard 472-1974 "Guide for Surge Withstand Capability." (b) Impulse wave, 8 × 20, 1000V peak, 5μs/div. (c) Impulse wave, 10 × 1000, 1500V peak, 0.2ms/div. (d) 100kHz ac surge, 6kV peak (500kHz leading edge); successive peaks down by 40% (1kV/div, 2μs/div).

Table 3. Noise sources and possible solutions.

Common-Impedance Noise
- Proper circuits for distributing power
- Isolation transformers, optical isolators, analog isolators
- Shielding of sensitive circuits

Capacitively Coupled Noise
- Reducing noise sources
- Properly implemented shields (very effective)
- Reducing stray capacitance

Magnetically Coupled Noise
- Careful routing of wiring
- High-permeability (mumetal) shields (the most effective)
- Reducing area of receiver circuit (twisted pairs, physical wire placement)
- Reducing the noise source (twisted pairs, driven shields to cancel field)

Power-Line Transients
- Coil suppression on relays, solenoids, etc.
- Zero-crossing turnoff for relays, solenoids, etc.
- Shielding
- Reducing stray capacitance

Miscellaneous
- Rigid wiring
- Low-noise cable
- Shielding from RFI source

SHIELDING AND GUARDING

How to Exclude Interference-Type Noise
What to Do and Why to Do It—A Rational Approach

by Alan Rich

This is the second of two articles dealing with interference noise. In the last issue of *Analog Dialogue* (Vol. 16, No. 3, pp. 16-19), we discussed the nature of interference, described the relationship between sources, coupling channels, and receivers, and considered means of combatting interference in systems by reducing or eliminating one of those three elements.

One of the means of reducing noise coupling is *shielding*. Our purpose in this article is to describe the correct uses of shielding to reduce noise. The major topics we will discuss include noise due to capacitive coupling, noise due to magnetic coupling, and driven shields and guards. A set of guidelines will be included, with do's and don'ts.

From the outset, it should be noted that shielding problems are always rational and do not involve the occult; but they are not always straightforward. Each problem must be analyzed carefully. It is important first to identify the noise source, the receiver, and the coupling medium. Improper shielding and grounding, based on faulty identification of any of these elements, may only make matters worse or create a new problem.

You can think of shielding as serving two purposes. First, shielding can be used to confine noise to a small region; this will prevent noise from extending its reach and getting into a nearby critical circuit. However, the problem with such shields is that noise captured by the shield can still cause problems if the return path the noise takes is not carefully planned and implemented by understanding of the ground system and making the connections correctly.

Second, if noise is present in a system, shields can be placed around critical circuits to prevent the noise from getting into sensitive portions of the circuits. These shields can consist of metal boxes around circuit regions or cables with shields around the center conductors. Again, where and how the shields are connected is important.

CAPACITIVELY COUPLED NOISE

If the noise results from an electric field, a shield works because a charge, Q_2, resulting from an external potential, V_1, cannot exist on the interior of a closed conducting surface (Figure 1).

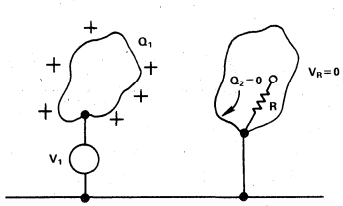


Figure 1. Charge Q_1 cannot create charge inside a closed metal shell.

Coupling by mutual, or stray, capacitance can be modeled by the circuit of Figure 2. Here, V_n is a noise source (switching transistor, TTL gate, etc.), C_s is the stray capacitance, Z is the impedance of a receiver (for example, a bypass resistor connected between the input of a high-gain amplifier and ground), and V_{no} is the output noise developed across Z.

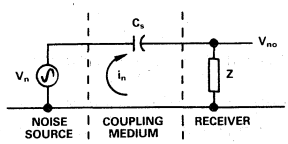


Figure 2. Equivalent circuit of capacitive coupling between a source and a nearby impedance.

A noise current, $i_n = V_n/(Z + Z_{Cs})$, will result, producing a noise voltage, $V_{no} = V_n/(1 + Z_{Cs}/Z)$. For example, if C_s = 2.5 pF, Z = 10kΩ (resistive), and V_n = 100mV at 1.3 MHz, the output noise will be 20 mV (0.2% of 10V, i.e., 8 LSBs of 12 bits).

It is important to recognize the effect that very small amounts of stray capacitance will have on sensitive circuits. This becomes increasingly critical as systems are being designed to combine circuits operating at lower power (implying higher impedance levels), higher speed (implying lower nodal stray capacitance, faster edges, and higher frequencies), and higher resolution (much less output noise permitted).

When a shield is added, the change to the situation of Figure 2 is exemplified by the circuit model of Figure 3. With the assumption that the shield has zero impedance, the noise current in loop A-B-D-A will be V_n/Z_{Cs1}, but the noise current in loop D-B-C-D will be zero, since there is no driving source in that loop. And, since no current flows, there will be no voltage developed across Z. The sensitive circuit has thus been shielded from the noise source, V_n.

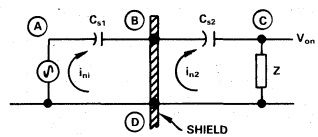


Figure 3. Equivalent circuit of the situation of Figure 2, with a shield interposed between the source and the impedance.

Guidelines for Applying Electrostatic Shields

- An electrostatic shield, to be effective, should be connected to the reference potential of any circuitry contained within the shield. If the signal is earthed or grounded (i.e., connected to a metal chassis or frame, and/or to earth), the shield must be earthed or grounded. But grounding the shield is useless if the signal is not grounded.
- The shield conductor of a shielded cable should be connected to the reference potential at the signal-reference node (Figure 4).
- If the shield is split into sections, as might occur if connectors are used, the shield for each segment must be tied to those for the

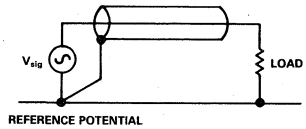


Figure 4. Grounding a cable shield.

adjoining segments, and ultimately connected (only) to the signal-reference node (Figure 5).

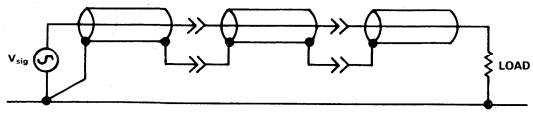


Figure 5. Shields must be interconnected if interrupted.

•The number of separate shields required in a system is equal to the number of independent signals that are being measured. Each signal should have its own shield, with no connections to other shields in the system, unless they share a common reference potential (signal "ground"). If there is more than one signal ground (Figure 6), each shield should be connected to its own reference potential.

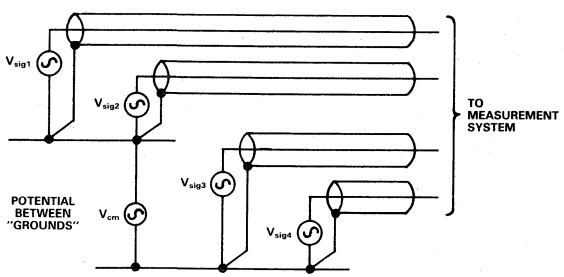


Figure 6. Each signal should have its own shield connected to its own reference potential.

•*Don't connect both ends of the shield to "ground".* The potential difference between the two "grounds" will cause a shield current to flow (Figure 7). The shield current will induce a noise voltage into the center conductor via magnetic coupling. An example of this can be found in Part 1 of this series, *Analog Dialogue* 16-3, page 18, Figure 10.

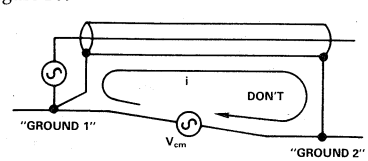
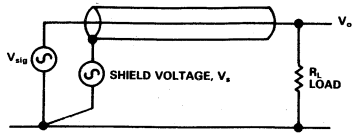


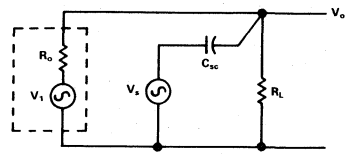
Figure 7. Don't connect the shield to ground at more than one point.

•*Don't allow shield current to exist* (except as noted later in this article). The shield current will induce a voltage in the center conductor.

•*Don't allow the shield to be at a voltage with respect to the reference potential* (except in the case of a guard shield, to be described). The shield voltage will couple capacitively to the center conductor (or conductors in a multiple-conductor shield). With a noise voltage, V_s, on the shield, the situation is as shown in Figure 8.



a. Shield at potential V_S.



b. Equivalent circuit.

Figure 8. Don't permit the shield to be at a potential with respect to the signal.

The fraction of V_s appearing at the output will be

$$V_o = \frac{V_s}{\sqrt{1 + \frac{1}{(2\pi f R_{eq} C_{sc})^2}}} \quad (1)$$

where V_1 is the open-circuit signal voltage, R_o is the signal's source impedance, C_{sc} is the cable's shield-to-conductor capacitance, and R_{eq} is the equivalent parallel resistance of R_o and R_L. For example, if V_s = 1V at 1.5MHz, C_{sc} = 200pF (10 feet of cable), R_o = 1000 ohms, and R_L = 10kΩ, the output noise voltage will be 0.86 volts.

This is an often-ignored guideline; serious noise problems can be *created* by inadvertently applying undesired potentials to the shield.

•*Know by careful study how the noise current that has been captured by the shield returns to "ground."* An improperly returned shield can cause shield voltages, can couple into other circuits, or couple into other shields. The shield return should be as short as possible to minimize inductance.

Here is an example that illustrates the problems that can arise in relation to these last two guidelines: Consider the improperly configured shield system shown in Figure 9, in which a precision voltage source, V1, and a digital logic gate share a common shield connection. This situation can occur in a large system where analog and digital signals are cabled together.

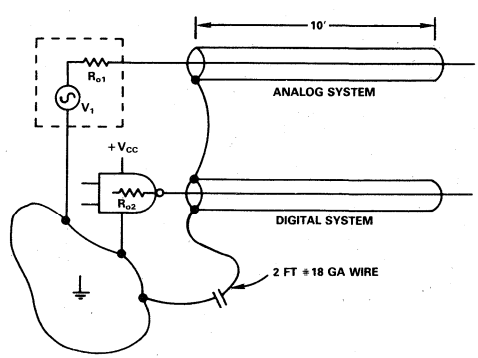


Figure 9. A situation that generates transient shield voltages.

A step voltage change in the output of the logic circuit couples capacitively to its shield, creating a current in the common 2-foot

shield return. This, in turn, develops a shield voltage common to both the analog and digital shields. An equivalent circuit is shown in Figure 10, in which V(t) is a 5-volt step from a TTL logic gate, R_{o2} is the 13-ohm output impedance of the logic gate, C_{ws} is the 470-pF capacitance from the shield to the center conductor of the shielded cable, and R_s and L_s are the 0.1-ohm resistance and 1-microhenry inductance of the 2-foot wire connecting the shield to the system ground.

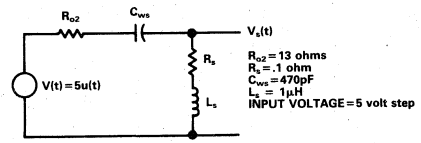


Figure 10. Equivalent circuit for generating shield voltage.

The shield voltage, $V_s(t)$, can be solved for by conventional circuit-analysis techniques, or simulated by actually building and carefully making measurements on a circuit with the given parameters. For the purpose of demonstration, the calculated response waveform, illustrated in Figure 11, with a 5-volt initial spike, resonant frequency of 7.3 MHz, and damping time constant of 0.15μs, is sufficient to illustrate the nature of the voltage that appears on the shield and is capacitively coupled to the analog input. If the voltage is looked at with a wideband oscilloscope, it will look like a noise "spike." We can see that this transient will couple a fast damped waveform of significant peak amplitude to the analog system input.

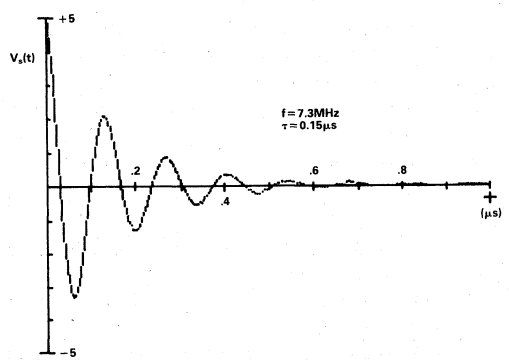


Figure 11. Computed response of circuit of Figure 10.

Even in a purely digital system, noise glitches can be caused to appear in apparently remote portions of a system having the kind of situation shown. This can often explain some otherwise inexplicable system bugs.

In quite a few cases, the proper choice of shield connection among the many possibilities may not be immediately obvious, and the guidelines may not provide us with a clear choice. There is no alternative but to analyze the various possibilities and choose the approach for which the lowest noise may be calculated.

For example, consider the case illustrated in Figure 12, in which the measurement system and the source have differing ground potentials. Should we connect the shield to A: the low side at the measurement-system input, B: ground at the system input, C: ground at the signal source, or D: the low side at the source?

A is a poor choice, since noise current is allowed to flow in a signal

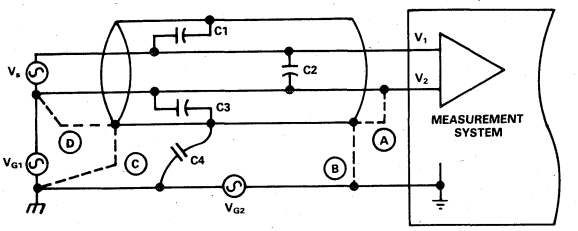


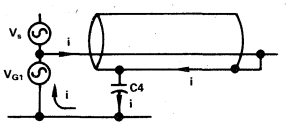
Figure 12. Possible grounds where system and source have differing ground potentials.

conductor. The path of the noise current due to V_{G1}, as it returns through C4, is shown in Figure 13a.

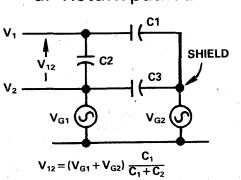
B is also a poor choice, since the two noise sources in series, V_{G1} and V_{G2}, produce a component across the two signal wires, developed by the source impedance in parallel with C_2, in series with C_1, as shown in Figure 13b.

C is poor, too, since V_{G1} produces a voltage across the two signal wires, by the same mechanism as (B), as Figure 13c shows.

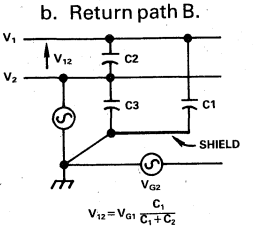
D is the best choice, under the given assumptions, as can be seen in Figure 13d. It also tends to confirm the grounding guideline to connect the shield at the signal's reference potential.



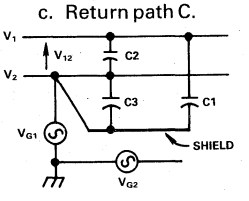
a. Return path A.



b. Return path B.



c. Return path C.



d. Return path D.

Figure 13. Equivalent circuits.

NOISE RESULTING FROM A MAGNETIC FIELD

Noise in the form of a magnetic field induces voltage in a conductor or circuit; it is much more difficult to shield against than elec-

tric fields because it can penetrate conducting materials. A typical shield placed around a conductor and grounded at one end has little if any effect on the magnetically induced voltage in that conductor.

As a magnetic field, B, penetrates a shield, its amplitude decreases exponentially (Figure 14). The skin depth, δ, of the shield material, is defined as the depth of penetration required for the field to be attenuated to 37% (exp (-1)) of its value in free air. Table 1[1] lists typical values of δ for several materials at various frequencies. You can see that any of the materials will be more effective as a shield at high frequency, because δ decreases with frequency, and that steel provides at least an order of magnitude more effective shielding at any frequency than copper or aluminum.

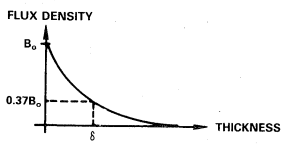


Figure 14. Magnetic field in a shield as a function of penetration depth.

Figure 15 compares absorption loss as a function of frequency for two thicknesses of copper and steel. ⅛-inch steel becomes quite effective for frequencies above 200 Hz, and even a 20-mil (0.5 mm) thickness of copper is effective at frequencies above 1 MHz. However, all show a glaring weakness at lower frequencies, including 50-60-Hz line frequencies—the principal source of magnetically coupled noise at low frequency.

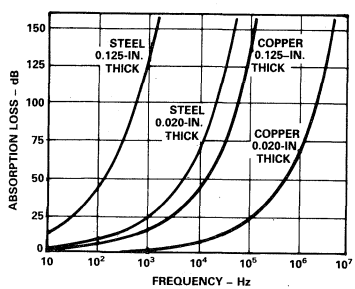


Figure 15. Absorption loss vs. frequency for two thicknesses of copper and steel.

For improved low-frequency magnetic shielding, a shield consisting of a high-permeability magnetic material (e.g., Mumetal) should be considered. Figure 16 compares a 30-mil thickness of Mumetal with various materials at several frequencies. It shows that, below 1 kHz, Mumetal is more effective than any of the other materials, while at 100kHz it is the least effective. However, Mumetal is not especially easy to apply, and if it is saturated by an excessively strong field, it will no longer provide an advantage.

Table 1. Skin depth, δ, vs. frequency

Frequency	δ for Copper (in.)	δ for Copper (mm)	δ for Aluminum (in.)	δ for Aluminum (mm)	δ for Steel (in.)	δ for Steel (mm)
60Hz	0.335	8.5	0.429	10.9	0.034	0.86
100Hz	0.260	6.6	0.333	8.5	0.026	0.66
1kHz	0.082	2.1	0.105	2.7	0.008	0.2
10kHz	0.026	0.66	0.033	0.84	0.003	0.08
100kHz	0.008	0.2	0.011	0.3	0.0008	0.02
1MHz	0.003	0.08	0.003	0.08	0.0003	0.008

[1]Table 1 and Figures 15 and 16 are from Ott, H.W., *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley & Sons, © 1976).

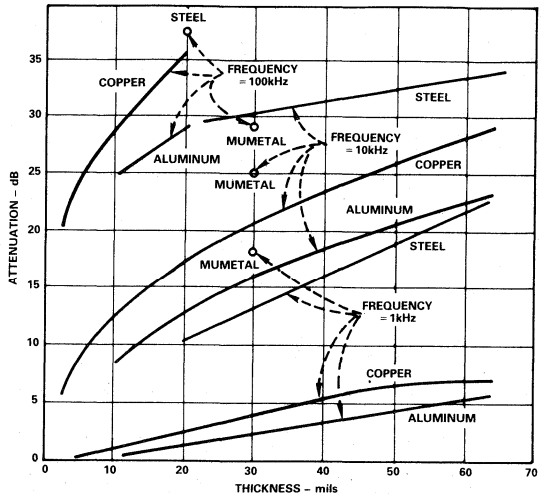
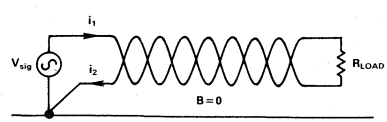


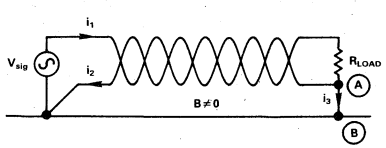
Figure 16. Shielding attenuation of Mumetal and other materials at several frequencies.

As you can see, it is very difficult to shield against magnetic fields, i.e., to modify the coupling medium by shielding. Therefore, the most effective approaches at low frequency are to minimize the strength of the interfering magnetic field, minimize the receiver loop area, and minimize coupling by optimizing wiring geometries. Here are some guidelines:

- Locate the receiving circuits as far as possible from the source of the magnetic field.
- Avoid running wires parallel to the magnetic field; instead, cross the magnetic field at right angles.
- Shield the magnetic field with an appropriate material for the frequency and field strength.
- Use a twisted pair of wires for conductors carrying the high-level current that is the source of the magnetic field. If the currents in the two wires are equal and opposite, the net field in any direction



a. Correct connection with balanced currents.



b. Incorrect connection forming ground loop.

Figure 17. Connections to a twisted pair.

over each cycle of twist will be zero (Figure 17a). For this arrangement to work, none of the current can be shared with another conductor, for example, a ground plane. Figure 17b shows what can happen if a ground loop is formed; if part of the current flows through the ground plane (depending on the ratio of conductor resistance to ground resistance), it will form a loop with the twisted pair, generating a field determined by $i_3 (= i_1 - i_2)$.

The ground connection between A and B need not be as simple as a short circuit to cause trouble. Any stray unbalanced capacitance or resistance from R_{load} circuits to the ground plane will also unbalance the currents and produce a net current through the wires and the ground plane, producing a ground loop and a related magnetic field. For this reason, it is also good practice to run the twisted pair close to the ground plane to tend to balance the capacitances from each side to ground, as well as to minimize loop area.

•Use a shielded cable with the high-level source circuit's return current carried in the shield (Figure 18). If the shield current, I_2 is equal and opposite to that in the center conductor, the center-conductor field and the shield field will cancel, producing a zero net field. In this case, which seems to violate the "no shield current" rule for receiver circuits, the concentric cable is not used to shield the center lead; instead, the geometry produces cancellation.

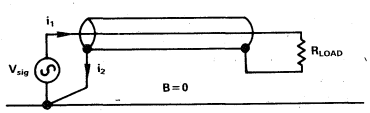


Figure 18. Use of shield for return current to noisy source.

This scheme can be usefully employed in an ATE system where accurate measurements must be performed on devices with high power-supply currents that may be noisy. For example, Figure 19 shows the application of this technique to the connections for the high-current logic supply for an a/d converter under test—at the end of a test cable.

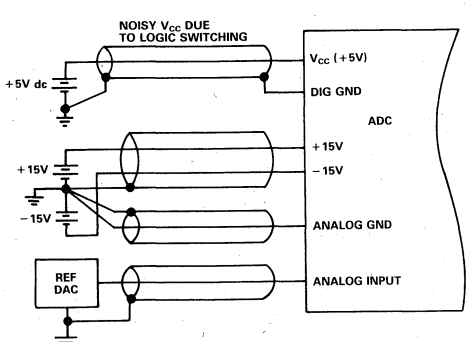


Figure 19. Application of circuit of Figure 18 in a test system.

•Since magnetically induced noise depends on the area of the receiver loop, the induced voltage due to magnetic coupling can be reduced by reducing the loop's area. What is the receiver loop? In the example shown in Figure 20, the signal source and its load are connected by a pair of conductors of length L and separation D. The circuit (assuming it has a rectangular configuration) forms a loop with area D · L.

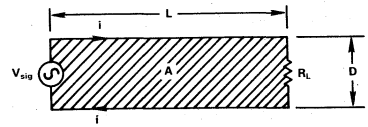


Figure 20. Area of a loop that receives magnetically coupled noise.

The voltage induced in series with the loop is proportional to the area and the cosine of its angle to the field. Thus, to minimize noise, the loop should be oriented at right angles to the field, and its area should be minimized.

The area can be reduced by decreasing the length of and/or decreasing the distance between the conductors. This is easily accomplished with a twisted pair, or at least a tightly cabled pair, of conductors. It is good practice to pair conductors so that the circuit wire and its return path will always be together. To do this, the designer must be certain of the actual path that the return current takes in getting back to the signal source. Quite often, the current returns by a path not intended in the original design layout.

If wires are moved (for example, by a technician troubleshooting some other problem), the loop area and orientation to the field may change, so that yesterday's acceptable noise level may be transformed to tomorrow's disastrous noise level. Which may lead to a service call . . . and another repetition of the cycle. The bottom line: Know the loop area and orientation, do what must be done to minimize noise—*and permanently secure the wiring*!

DRIVEN SHIELDS AND GUARDING

We have discussed the role of a current-driven shield carrying an equal and opposite current to reduce generated noise by reducing the magnetic field around a conductor.

Guarding is similar, in that it involves driving a shield, at low impedance, with a potential essentially equal to the common-mode voltage on the signal wire contained within the shield. Guarding has many useful purposes: It reduces common-mode capacitance, improves common-mode rejection, and eliminates leakage currents in high-impedance measurement circuits.

Figure 21 shows an example of an op amp with negligible bias current connected as a high-impedance non-inverting amplifier with gain. The purpose of the cable is to shield the high input-impedance signal conductor from capacitively coupled noise and to minimize leakage currents. The signal comes from a 10-megohm source, and the cable is assumed to have 1000 megohms of leakage resistance (which may change as a function of temperature, humidity, etc.) from conductor to shield. If connected as shown, the equivalent input circuit is an attenuator which loses 1% of the

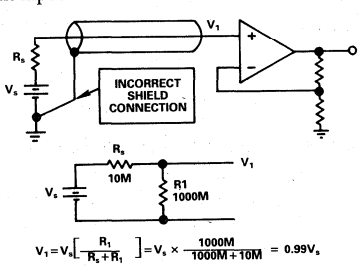


Figure 21. Op amp connected as high-impedance non-inverting amplifier with gain, with shielded input lead.

signal at the time it is measured, and an unknown fraction at other times. Also, the cable capacitance produces a substantial lag time constant, R_sC_c.

Figure 22 has the same players, but the shield is connected to the tap of the gain divider (usually at low impedance). Being connected to the inverting input of the op amp, it should be at the same potential as the amplifier's non-inverting input. Since there is no voltage across the cable's leakage resistance, there is no current through it and its resistance value doesn't matter; V_1 must therefore be equal to V_s, since bias current was assumed negligible.

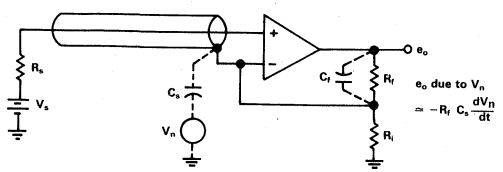
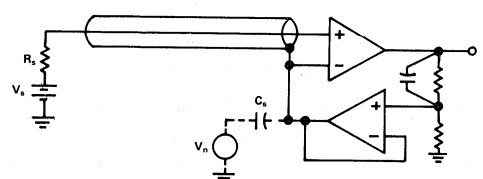


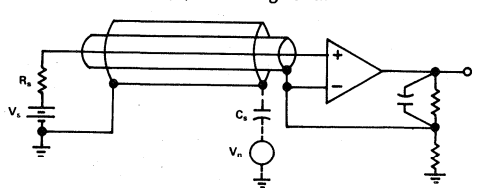
Figure 22. Same as Figure 21, but cable shield connected as a guard.

Also, there is no voltage across the cable capacitance, hence no charging or discharging of the cable; thus the lag time constant depends mainly on circuit strays and the amplifier's input capacitance. For stability, capacitance should be connected between the output and the negative input, such that $C_fR_F = C_sR_i$, where C_s is sum of the stray capacitance between shield and ground and the input capacitance.

There must be no noise voltage applied to the guard. In noisy systems, as Figure 22 shows, capacitively coupled noise will be differentiated, emphasizing the higher-frequency components. This can be avoided (Figure 23) by either using a buffer follower with fast response and low output impedance to drive the guard (a) or a second shield, around the guard, grounded to the signal common (b).



(a) Driven guard.



(b) Shielded guard.

Figure 23. Avoiding noise pickup on the guard.

In high-impedance current-input inverting configurations, where a length of shielded wire is used to guard the lead from the current source to the amplifier's inverting input, the guard should either be driven by a buffer at the same potential as the non-inverting input (and connected nowhere else), or be tied directly to the non-inverting input, with a second outer shield connected to the signal's reference point.

SUMMARY

Table 2 summarizes the important points made in this article. All are important to maintaining a high-integrity shield system. However, we cannot emphasize too strongly the two subjects that are most-often ignored: appearance of noise voltage on signal shields and proper disposition of shield noise currents. *Noise voltage must not exist on the shield*; shield-to-conductor capacitance will couple the noise directly to the center conductor. *If shield currents are not returned properly, they can show up in a remote part of the system* and perhaps cause trouble in a location totally unrelated to the shielding problem that was "solved." ▶

Table 2. Applicability of shielding considerations

Consideration	Universal	Electric	Magnetic
Know the noise source, coupling medium, and receiver.	X	X	X
Different shielding techniques are required for different noise sources, coupling channels, and receivers.	X	X	X
In most situations, conventional circuit analysis using lumped elements can be used.	X	X	X
Connect the shield at the signal-source end only.		X	
Carry shields through connectors.		X	
Individual shields should not be tied together.		X	
Do not ground both ends of a shield.		X	
Do not allow shield current to flow, except for driven shields - to cancel magnetic fields		X	X
Do not allow voltage on a shield, except for guarding.		X	
Know *exactly* where noise current from the shield will flow.		X	
Use short connections to return noise current from the shield.		X	
Electrostatic shields have little effect in reducing noise resulting from magnetic fields.			X
Reduce magnetic fields by physical separation proper orientation, twisted pairs, and/or driven shields.			X
Know the receiver loop area and orientation to the field. Keep field at right angles and reduce the loop area by using paired conductors, preferably twisted pairs, and minimize wire lengths.			X
Use guarding in high-impedance circuits	X	X	
In high-impedance circuits, be extremely careful of shield noise	X	X	

BRIEF BIBLIOGRAPHY

For further reading, see:

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Ott, Henry W. *Noise Reduction Technique in Electronic Systems.* (New York: John Wiley & Sons, 1976).

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AD108A/208A/308A	ADC-8S	DAS1151	THS-0225	424
AD111/211/311	ADC-10Z	MAS-0801	40	426
AD351	ADC-12QZ	MAS-1001	42	428
AD370/371	ADC-14I/17I	MDA-10Z	43	432
AD502	ADC-16Q	MDH-0870	44	433
AD511	ADC1100	MDH-1001	45	434
AD512	ADC1102	MDH-1202	46	435
AD514	ADC1103	MDS-0815	48	436
AD520	ADC1105	MDS-0815E	52	440
AD523	ADC1109	MDS-1020	105	441
AD528	ADC1111	MDS-1020E	118	450
AD530	ADC1133	MDS-1240	119	452
AD531	ADG200	MDSL-0825	141	454
AD540	ADG201	MDSL-1035	146	456
AD559	BDM1615/1616/1617	MDSL-1250	148	605
AD801	DAC-M	RTI-1200	165	606
AD2003	DAC-QG	RTI-1201	180	610
AD2008	DAC-QM	RTI-1202	183	751
AD2009	DAC-QS	RTI-1220	184	752
AD2020	DAC-QZ	RTI-1221	230	756
AD2022	DAC-10DF	SCM1677	232	934
AD2023	DAC-10Z	SDC1604	233	942
AD2033	DAC1009	SHA-1A	260	944
AD7513	DAC1106	SHA-2A	261	946
AD7519	DAC1108	SHA-3	272	947
AD7527	DAC1118	SHA-4	273	956
AD7544	DAC1125	SHA-5	275	
AD7555	DAC1132	SHA-1114	276	
AD7570	DAC1420	SHA-1134	285	
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ADC-QM	DAC1423	THC-1500	310	

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AD508	AD517
AD513	AD503
AD516	AD506
AD550	None
AD551	None
AD553	None
AD555	AD7519
AD810-813	None
AD814-816	None
AD818	None
AD820-822	None
AD830-833	None
AD835-839	None
AD840-842	None
AD7516	AD7510DI
ADC1121	AD7550
ADM501	ADM501/506
ADP501	ADP511
DAC-10H	DAC-10Z
DAC1112	DAC12QS
DAC1122	AD7541
IDC1703	IRDC1730/1731
MDA-LB	None
MDA-LD	None
MDA-UB	None
MDA-UD	None
MDA-8H	MDA-10Z
MDA-10H	MDA-10Z
MDA-11MF	AD7521
MDS-0830	HDS-0820
MDS-0850	HDS-0820
MDS-1040	HDS-1025
MDS-1080	HDS-1025
MDSL-0802	HDS-0820
MDSL-1002	HDS-1025
MDSL-1201	HDS-1250
SERDEX	μMAC-5000
SHA-6	SHA1144
TSDC1608-1611	TSL1612
2N3954	None
2N5900	None
41	AD515
47	48
101 (module)	45
102	48
106	118
107	118
108	52
110	48
111	AD308
114	119
115	43
120	50
142	48
143	52
149	50
153	AD517
161	165
163	165
170	171
220	234
231	233
274J	284J
279	286J
280	281
282J	292A
283J	292A
301 (module)	52
302	310 (module)
350	None
427	424
602J10	AD524
602J100	AD524
602K100	AD524
603	AD524
901	904
907	921
908	921
909	921
931	None
932	None
933	None
935	None
948	947
971	921
AD612	AD524
AD614	AD524

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